AOI321 Domino Logic

Group Number: 9

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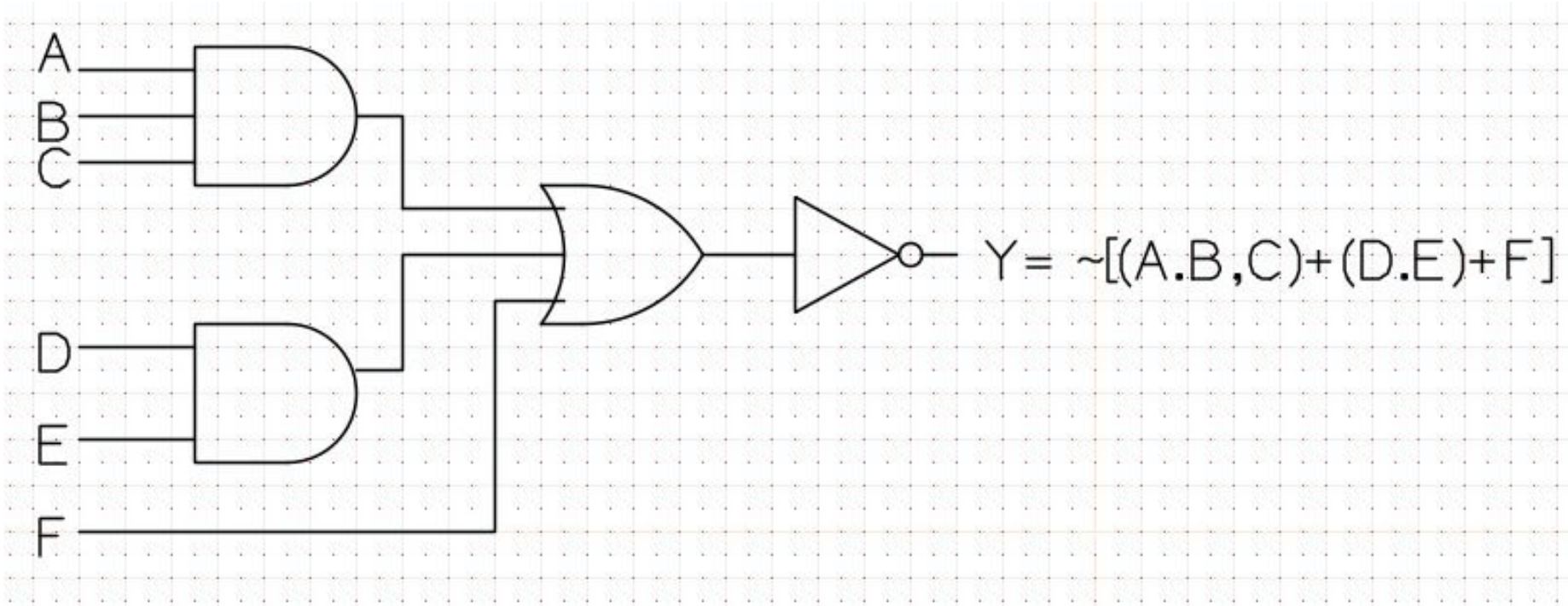
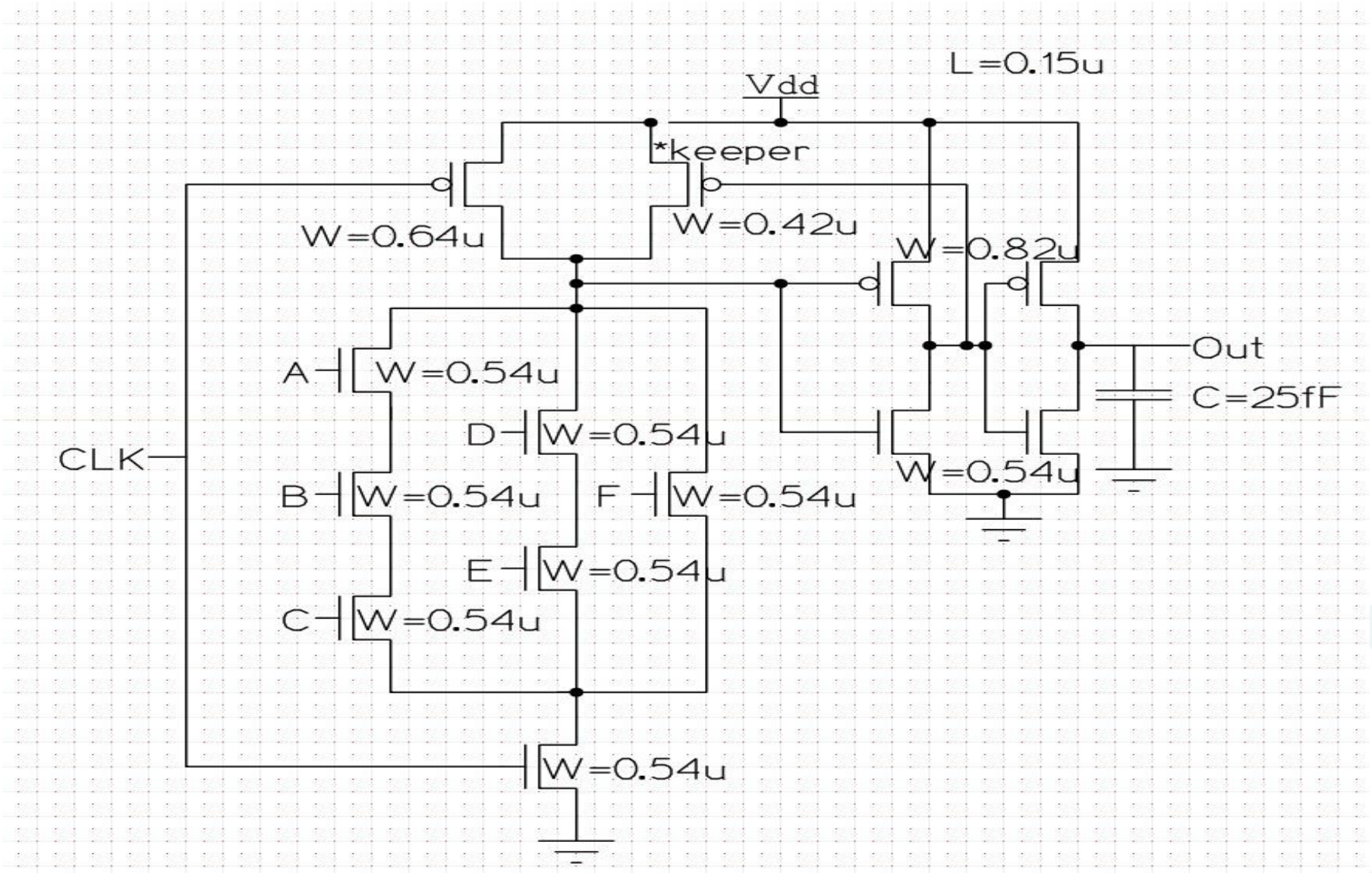
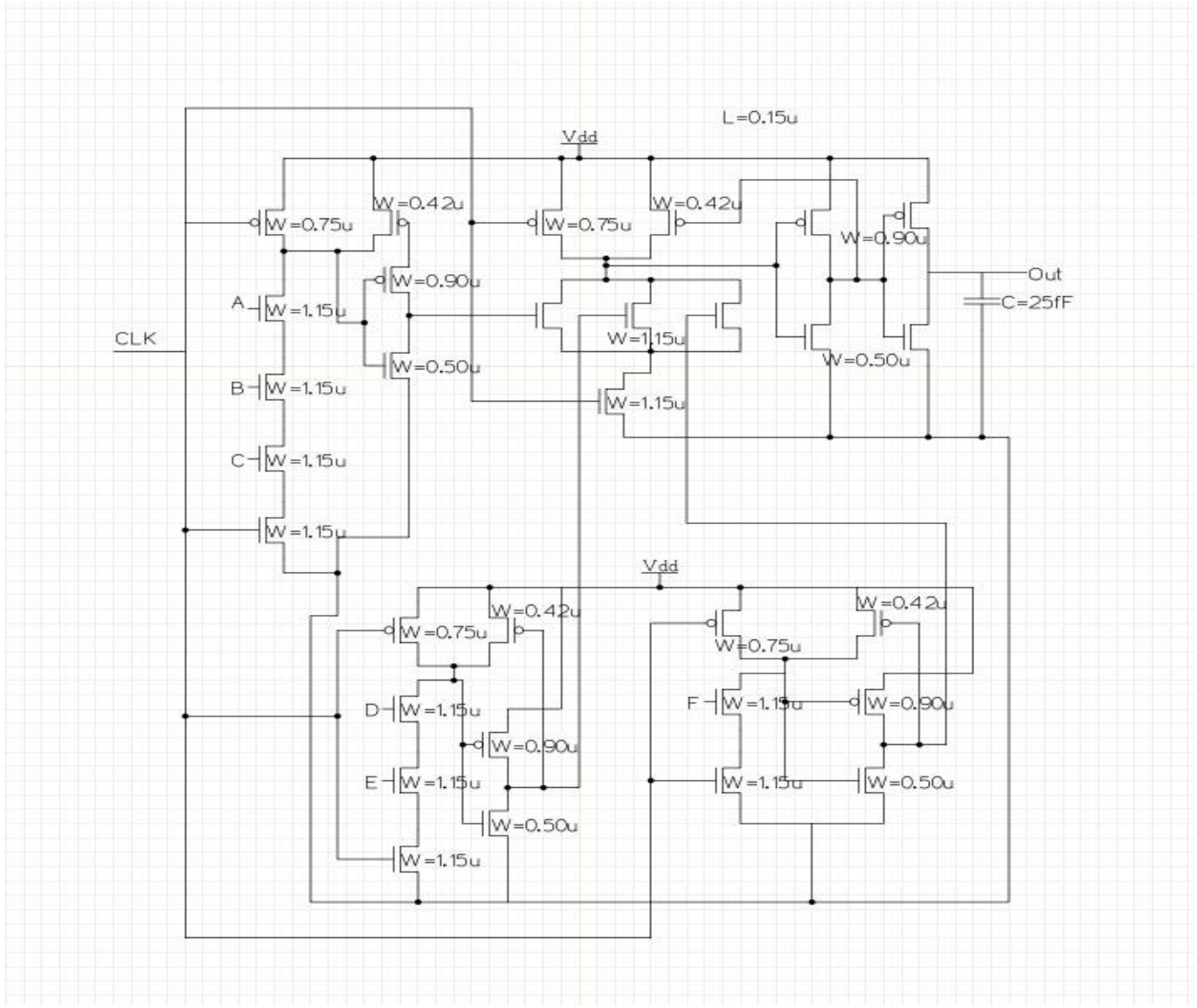
AOI321



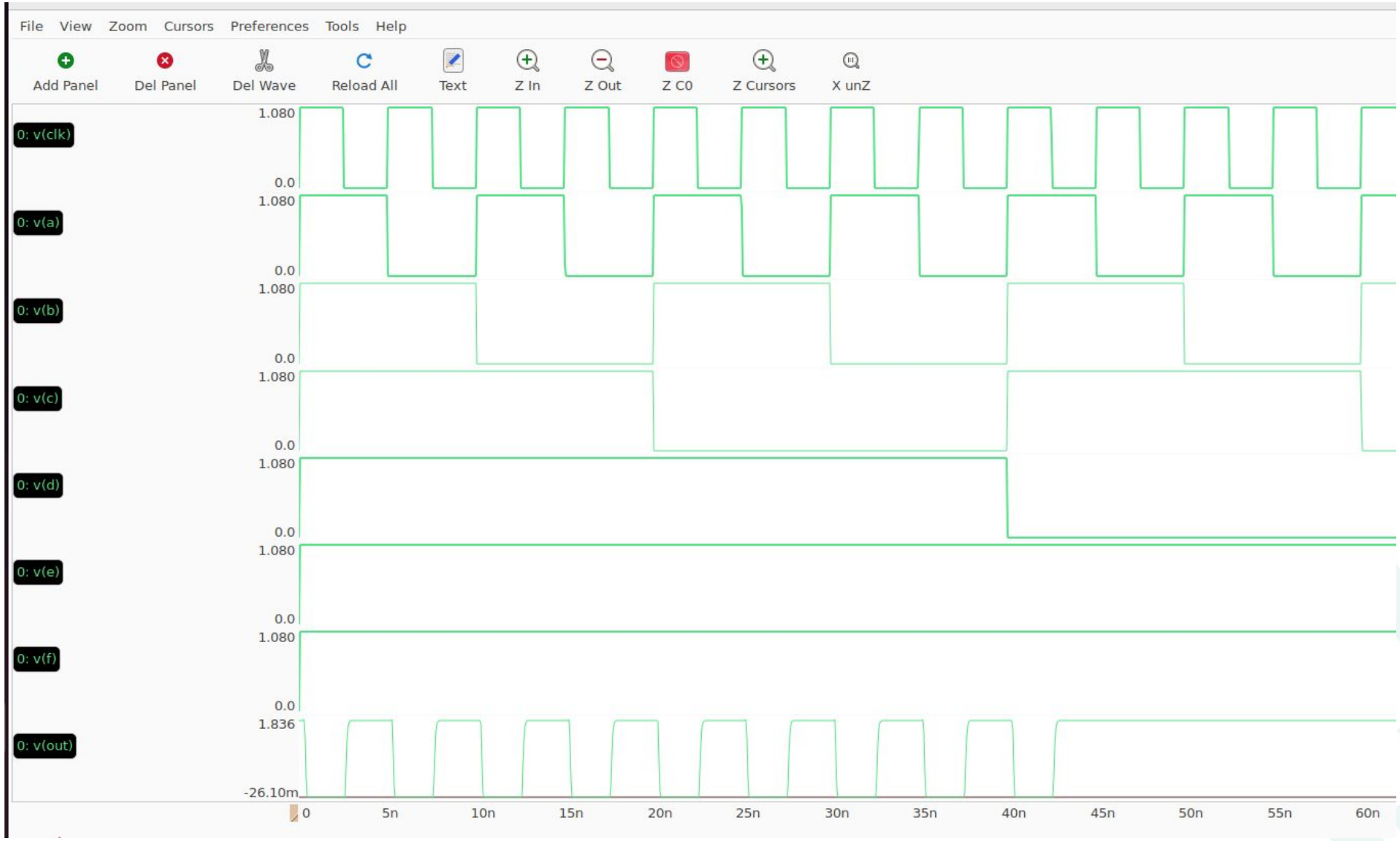
Schematic + Sizing (Complex)



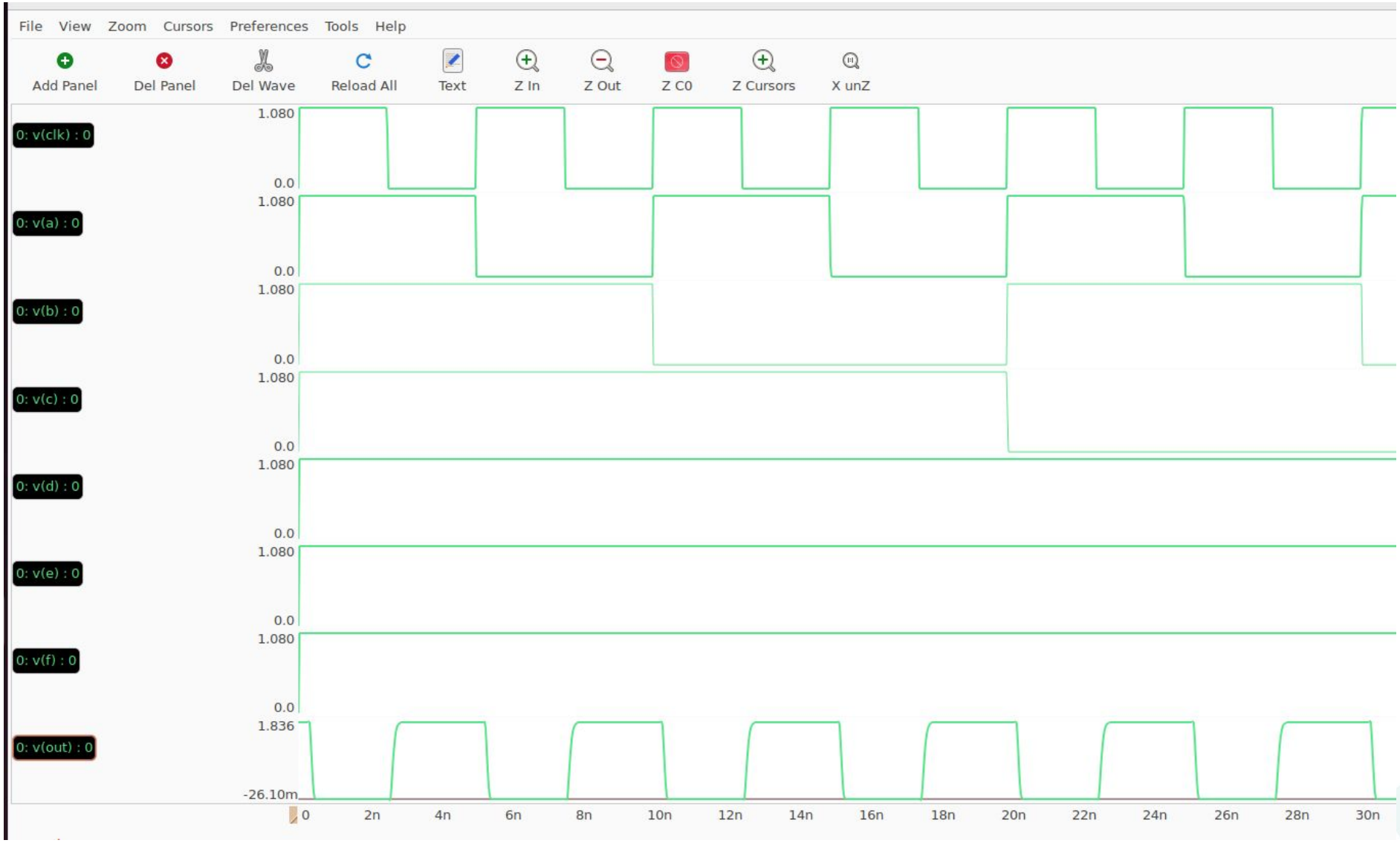
Schematic + Sizing (Non Complex)



Stimuli For Verification & Verification Plan (Complex)



Stimuli For Verification & Verification Plan (Non-Complex)



Delay Comparison

Contamination Delay (TCD)

The contamination delay is best in the case of PVT :- FF, 1.8,-40 when inputs are

B,C,E = 1 A,D,F = 0->1
(For Complex)

B,C,E = 1, A,D,F = 0->1
(For Non-Complex)

Conditions	Parameters	Complex		Non Complex	
		Pre Layout	Post Layout	Pre Layout	Post Layout
PVT -FF, 1.8,-40 B,C,E = 1 A,D,F = 0->1 (For Complex) B,C,E = 1, A,D,F = 0->1 (For Non-Complex)	Trise	8.505e-11	8.624e-11	3.519e-11	6.869e-11
	Tfall	5.532e-11	5.634e-11	3.400e-11	6.505e-11
	TPHL	2.008e-10	1.949e-10	2.587e-10	3.121e-10
	TPLH	2.360e-09	2.359e-09	2.400e-09	2.374e-09
	Delay	1.795e-10	9.849e-10	3.416e-10	3.750e-10
PVT -SS, 1.2,125C	Trise	4.943e-10	5.013e-10	1.716e-10	3.306e-10
	Tfall	3.981e-10	4.036e-10	1.881e-10	3.618e-10
	TPHL	6.921e-10	7.180e-10	6.025e-10	8.152e-10
	TPLH	1.681e-09	1.676e-09	2.068e-09	2.168e-09
	Delay	1.887e-10	1.202e-10	4.315e-10	1.589e-10
PVT -SS, 1.2, -40C	Trise	1.327e-09	1.346e-09	6.696e-10	9.273e-11
	Tfall	3.875e-10	3.927e-10	1.749e-10	7.940e-11
	TPHL	9.095e-10	9.007e-10	9.864e-10	3.185e-10
	TPLH	7.390e-10	7.259e-10	1.184e-09	2.337e-09
	Delay	5.400e-10	5.378e-10	3.942e-10	8.500e-10
PVT -TT, 1.62, 25C	Trise	1.443e-10	1.463e-10	6.113e-11	1.188e-10
	Tfall	9.552e-11	9.683e-11	5.352e-11	1.026e-10
	TPHL	3.178e-10	3.157e-10	3.692e-10	4.5200e-10
	TPLH	2.263e-09	2.261e-09	2.327e-09	2.282e-09
	Delay	8.138e-10	8.151e-10	7.943e-10	6.888e-10

Delay Comparison

Propagation Delay (TPD)

The Propagation delay is best in the case of PVT :- SS, 1.2,125C when inputs are

A,B,C = 0->1 D,E,F
(For Complex)

A,B,C,D,E,F = 0->1
(For Non-complex)

Conditions	Parameters	Complex		Non Complex	
		Pre Layout	Post Layout	Pre Layout	Post Layout
PVT -FF, 1.8,-40 A,B,C = 0->1 D,E,F (For Complex) A,B,C,D,E,F = 0->1 (For Non-complex)	Trise	8.505e-11	8.624e-11	3.519e-11	6.869e-11
	Tfall	5.554e-11	5.630e-11	3.500e-11	6.555e-11
	TPHL	1.480e-08	1.480e-08	2.597e-10	3.321e-10
	TPLH	2.236e-08	2.236e-08	2.450e-09	2.674e-09
	Delay	2.598e-08	2.598e-08	5.466e-10	8.780e-10
PVT -SS, 1.2,125C	Trise	4.944e-10	5.013e-10	1.816e-10	3.406e-10
	Tfall	3.981e-10	4.037e-10	1.884e-10	3.620e-10
	TPHL	1.428e-08	1.428e-08	6.028e-10	8.150e-10
	TPLH	2.169e-08	2.168e-08	2.028e-09	2.128e-09
	Delay	3.487e-10	3.512e-08	9.415e-10	9.689e-10
PVT -SS, 1.2, -40C	Trise	1.327e-09	3.928e-09	6.706e-10	9.303e-11
	Tfall	3.875e-10	1.345e-10	2.049e-10	8.040e-11
	TPHL	1.426e-08	1.426e-08	9.864e-10	3.185e-10
	TPLH	2.075e-08	2.074e-08	1.184e-09	2.337e-09
	Delay	2.464e-08	2.463e-08	4.042e-10	8.800e-10
PVT -TT, 1.62, 25C	Trise	1.473e-10	1.463e-10	6.013e-11	1.088e-10
	Tfall	9.622e-11	9.694e-11	5.252e-11	0.926e-10
	TPHL	1.468e-08	1.467e-08	3.702e-10	4.530e-10
	TPLH	2.226e-08	2.226e-08	2.327e-09	2.282e-09
	Delay	2.580e-08	2.580e-08	8.043e-10	7.088e-10

Leakage Current and Dynamic Power

Complex

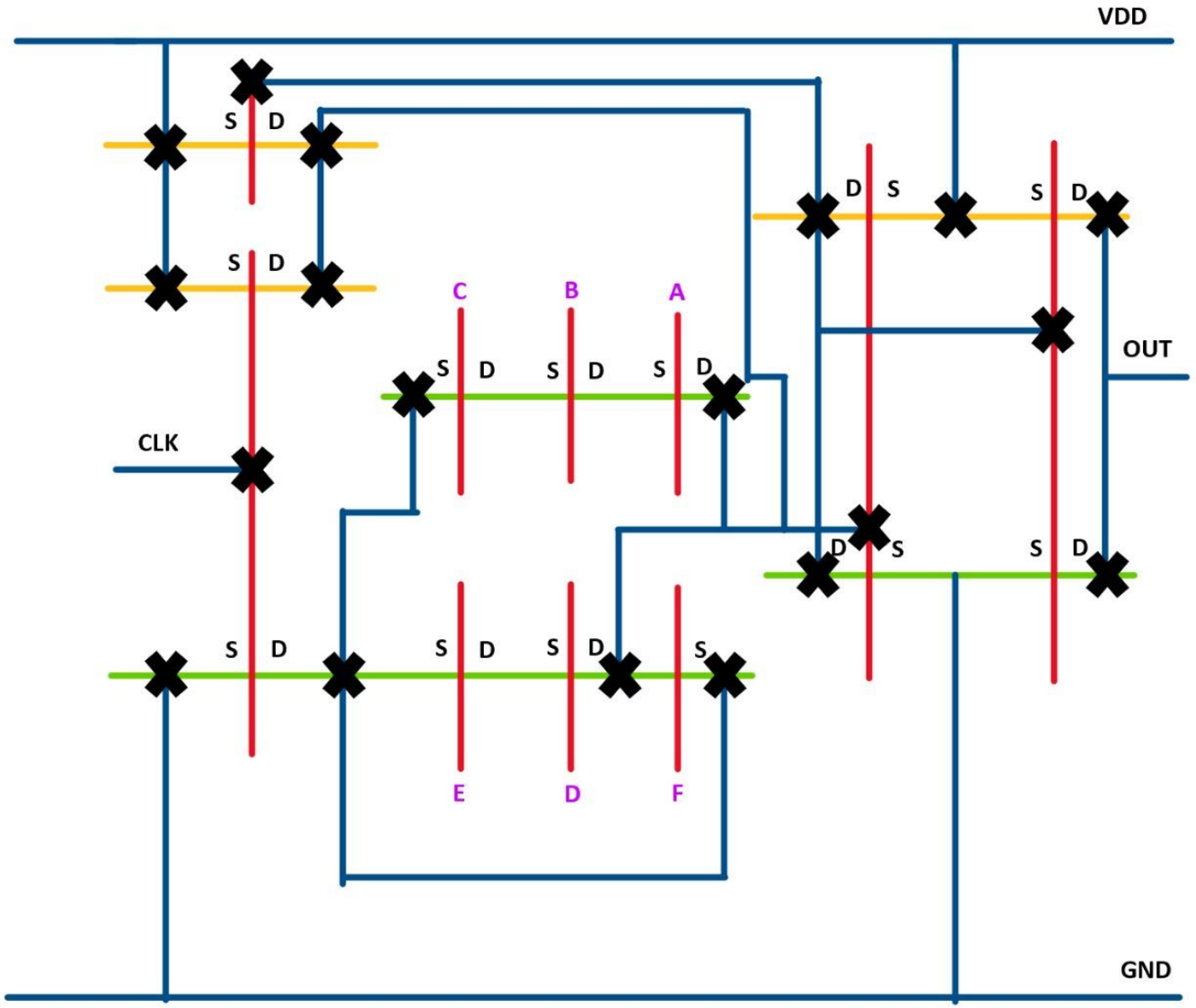
	PVT = FF, HV, HT	PVT = TT, Nominal Voltage, 25C
Inputs	Leakage Current	Dynamic Power
A,B,C,D,E,F = OFF	4.988e-07	8.081e+01
A,D,F = 1 B,C,E = 0	1.986e-07	3.218e+01
A,D,F = 0 B,C,E = 1	4.547e-07	7.366e+01

Leakage Current and Dynamic Power

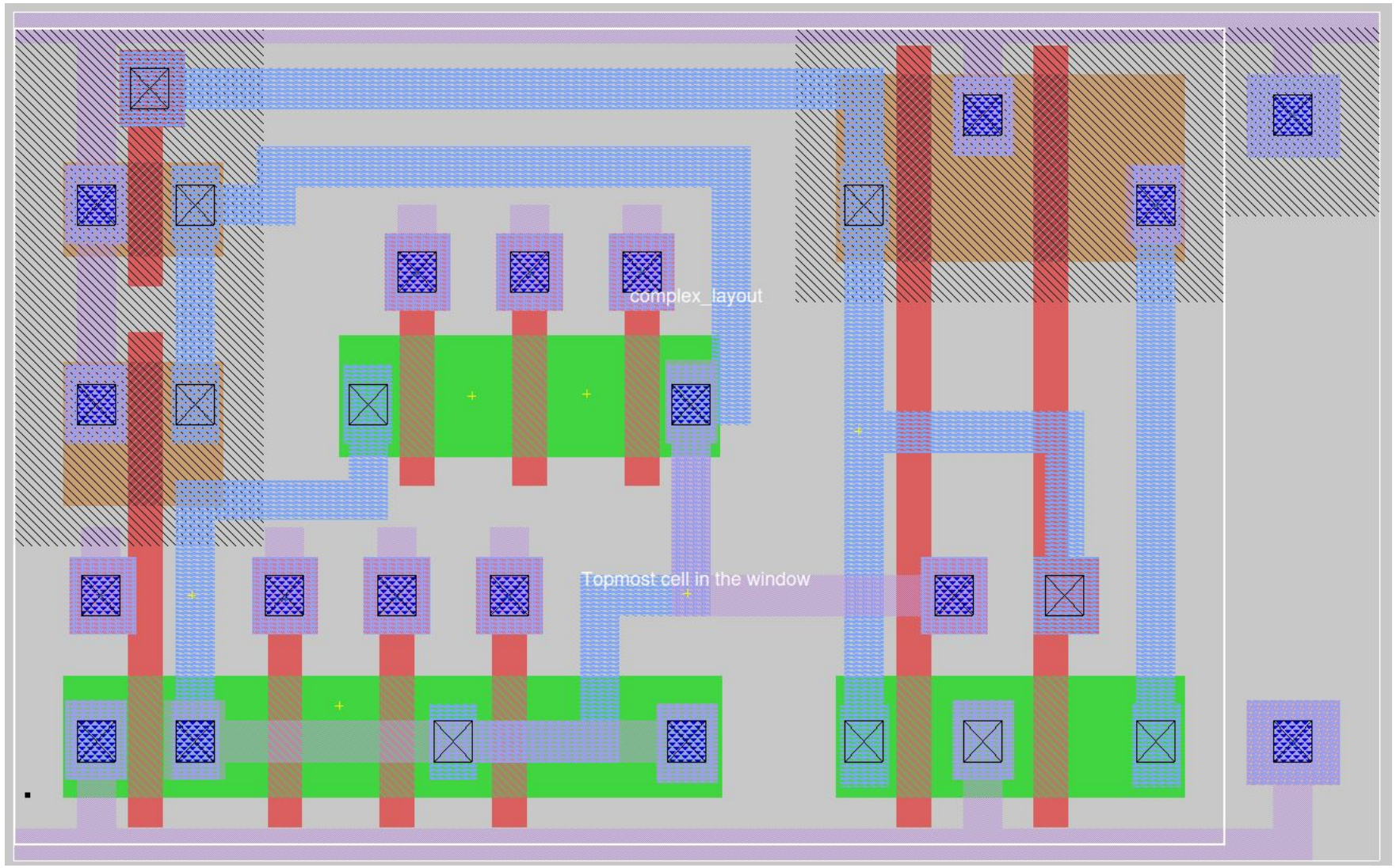
Non Complex

	PVT = FF, HV, HT	PVT = TT, Nominal Voltage, 25C
Inputs	Leakage Current	Dynamic Power
A,B,C,D,E,F = OFF	3.149e-07	5.101e+01
A,D,F = 1 B,C,E = 0	2.456e-07	3.979e+01
A,D,F = 0 B,C,E = 1	5.814e-07	9.419e+01

Stick Diagram (Complex)



Layout (Complex)

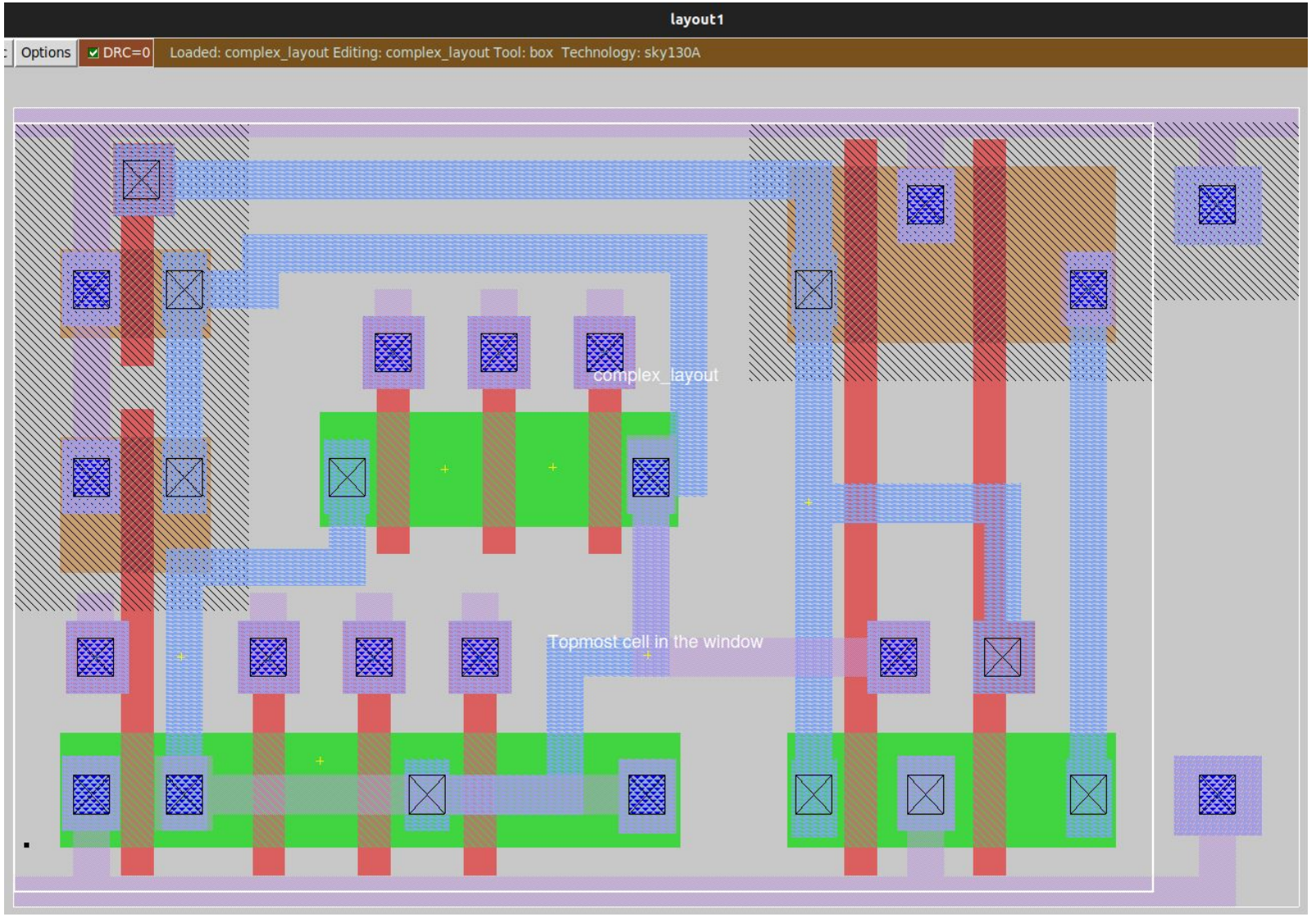


Length :
5.39um

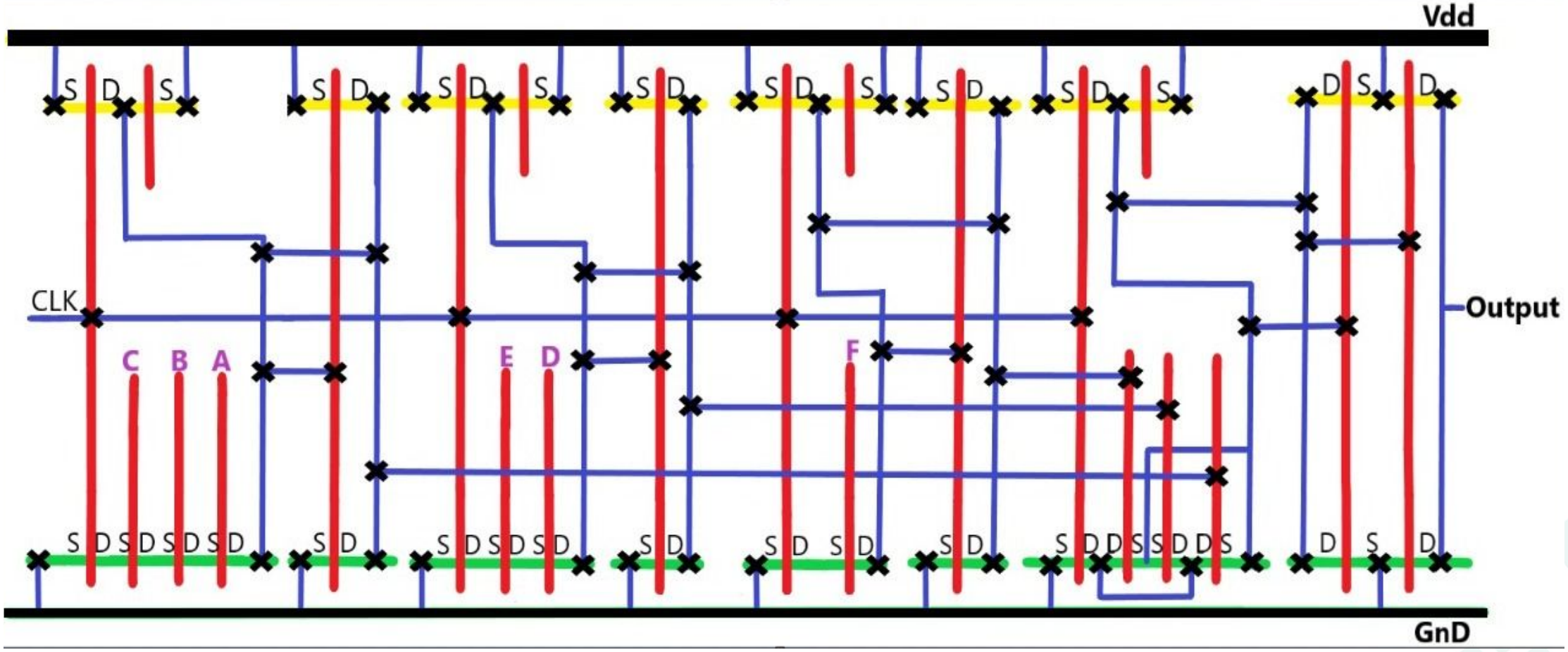
Height :
3.64um (13 tracks)

Area :
19.62um^2

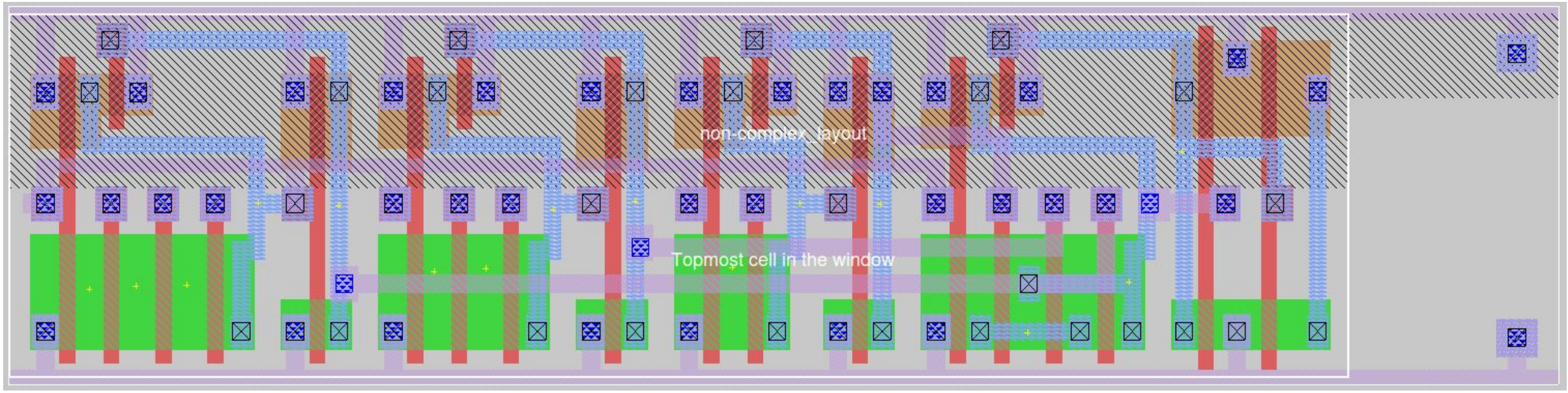
DRC (Complex)


layout1
Options
DRC=0
Loaded: complex_layout Editing: complex_layout Tool: box Technology: sky130A
complex_layout
Topmost cell in the window

Stick Diagram (Non-Complex)



Layout (Non-Complex)

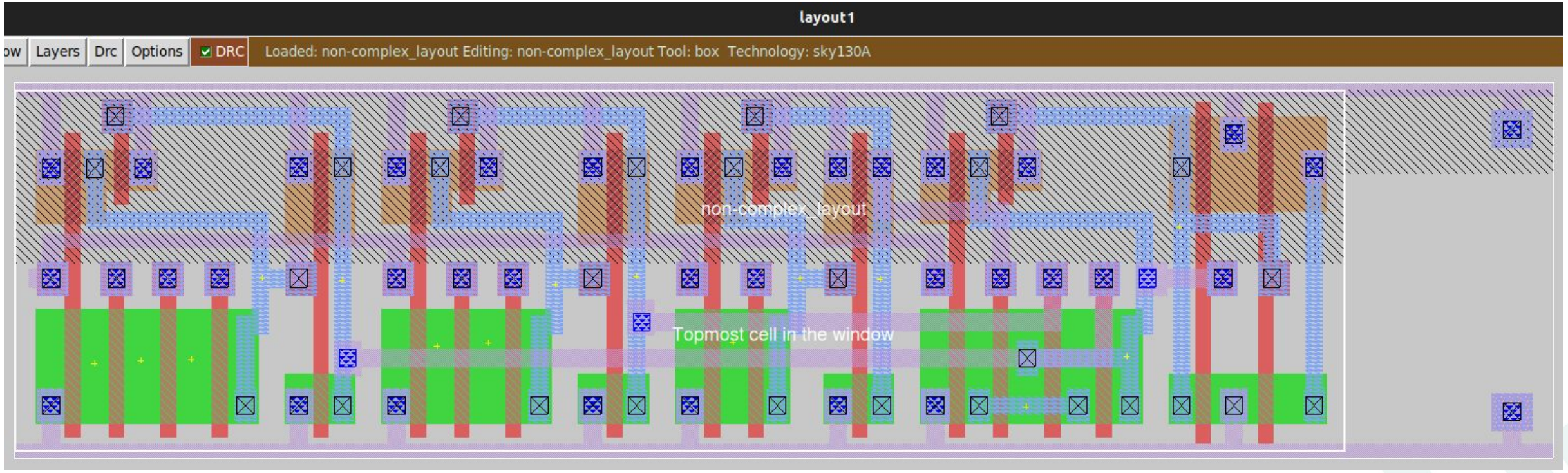


Length : 13.4um

Height : 3.64um (13 tracks)

Area : 48.776um^2

DRC (Non-Complex)



Conclusion

1. Area of the layout is optimized by :-

- Keeping minimum DRC between Poly to Poly by placing vias vertically and making vertical contact pins.
- Sharing the diffusion layers wherever possible.
- Removing the metal layer running vertically by adjusting the stick diagram.

2. Area and power consumed are lesser in Complex logic implementation as compared to Non-Complex logic implementation.

3. While Domino logic can achieve high-speed operation, its dynamic power consumption can limit its energy efficiency.

4. Leakage current contributes to static power dissipation, leading to increased overall power consumption in Domino logic circuits.

5. While short propagation delays enhance performance, the dynamic nature of Domino logic makes it susceptible to contamination effects.

6. Contamination may disrupt the pre charged state, leading to unintended logic transitions and potential logic errors.

Work Distribution

Sizing and Schematic: Krishna Ayyagari, Nikhil Kumar

Stimuli For Verification & Verification Plan: Nikhil Kumar, Rajat Vatwani, Krishna Ayyagari

Delay Comparison, Leakage Current and Dynamic Power: Rajat Vatwani

Stick Diagram and Layout: N. Vignesh Chowdary, Nikhil Kumar, Krishna Ayyagari