



INDRAPRASTHA INSTITUTE *of*  
INFORMATION TECHNOLOGY  
DELHI

Department  
of  
Electronics & Communication Engineering

VLSI DESIGN FLOW | ECE-513

Dr. Sneh Saurabh

RTL to GDS Flow Automation  
Project Part-II

Group Number 18  
Animesh Pareek 2021131  
Krishna Ayyagari 2021158  
Rajat Vatwani 2021186

# TABLE OF CONTENT

Description:	5
Block Design:	6
Assumptions:	6
Objective	7
Choice of Tools	7
Library Used	7
Interpretation of the results obtained in various steps of Physical Design:	7
For large utilisation (0.8)	8
For small utilisation (0.5)	8
Setup Slack	9
Hold Slack	9
Cells and Area	9
Power	9
Interpretation of the routability on the change in floorplan:	9
<b>1. Before starting Physical Design</b>	<b>10</b>
STA after DFT (PBA and GBA)	10
Inputs: Synthesized netlist, library file, and constraints file.	10
Output:	10
Software Used:	11
Cadence Tempus	11
Commands Used:	11
Constraints used:	11
Remarks	11
Timing Information:-	11
Effect of slew on timing:-	12
Effect of load on timing:-	12
Effect of positive/negative unateness:-	12
Effect of GBA and PBA on timing:-	12
STA for Minimum Area	13
TCL File:	13
Violations Report:	14
Timing Reports:	15
GBA Path	15
Setup Slack	15
Hold Slack	15
Slack Computation (worst path):	16
PBA Path	17

Setup Slack	17
Hold Slack	17
Slack Computation (worst path):	18
STA for Optimal Case:	19
TCL File:	19
Violations Report:	19
Timing Reports:	20
GBA Path	20
Setup Slack	20
Hold Slack	21
Slack Computation (worst path):	21
PBA Path	22
Setup Slack	23
Hold Slack	23
Slack Computation (worst path):	23
STA for Tight Constraints:	25
TCL File:	25
Violations Report:	25
Timing Reports:	26
GBA Path	26
Setup Slack	26
Hold Slack	26
Slack Computation (worst path):	27
PBA Path	28
Setup Slack	28
Hold Slack	29
Slack Computation (worst path):	29
Area Report:	30
Power Report:	31
<b>2. After Placement</b>	<b>32</b>
Inputs:	32
Software Used:	32
Commands Used:	32
Layout Design Core Utilization:- 0.5	33
TCL file:	33
Constraints used:	34
Timing Reports:	34
Setup Analysis:-	34
Hold Analysis:-	36
Power Report:	37
Area Report:	40

Snap-shot of layout of design and connectivity showing Fly-Lines:	42
Layout Design Core Utilization:- 0.8	44
TCL file:	44
Constraints used:	45
Timing Reports:	45
Setup Analysis:-	45
Hold Analysis:-	47
Power Report:	48
Area Report:	50
Snap-shot of layout of design and connectivity showing Fly-Lines:	52
Effect of placement of timing	54
<b>3. Clock Tree Synthesis</b>	<b>54</b>
Software Used:	54
Commands Used:	54
Layout Design Core Utilization:- 0.5	55
TCL file	55
DoCTS.tcl:	55
Constraints used:	55
Timing Reports:	55
Setup Reports:	56
Hold Report:-	57
Power Report:	59
Area Report:	61
Clock Tree:-	63
After Clock Tree Synthesis:-	63
Layout Design Core Utilization:- 0.8	66
TCL file:	66
DoCTS.tcl:	66
Constraints used:	66
Timing Reports:	66
Setup Analysis:-	67
Hold Analysis:-	68
Power Report:	69
Area Report:	71
Clock Tree:-	73
After Clock Tree Synthesis:-	73
Effect of clock path on overall timing slack	75
<b>4. After Detailed Routing</b>	<b>76</b>
Software Used:	76
Commands Used:	76
Layout Design Core Utilization:- 0.5	76

TCL file:	76
Constraints used:	77
Timing Reports:-	77
Setup Analysis:-	77
Hold Analysis:-	79
Area Report:-	80
Power Report:-	82
Layout Screenshot	84
Layout Design Core Utilization:- 0.8	89
TCL file:	89
Constraints used:	90
Timing Reports:	90
Setup Analysis:-	90
Hold Analysis:-	91
Area Report:	92
Power Report:	94
Layout Screenshot	96
Effect of metal layers on overall timing	103

## RTL to GDS Synthesis of a 2x2 Network on Chip

Description:

NoC is a proper interconnection network that addresses the communication complexity among hundreds to thousands of cores in a many-core system on chip (SoC).

We have tried to design a simple 2x2 NoC design that helps in identifying the possible paths between any two routers to transfer a maximum of 256 packets.

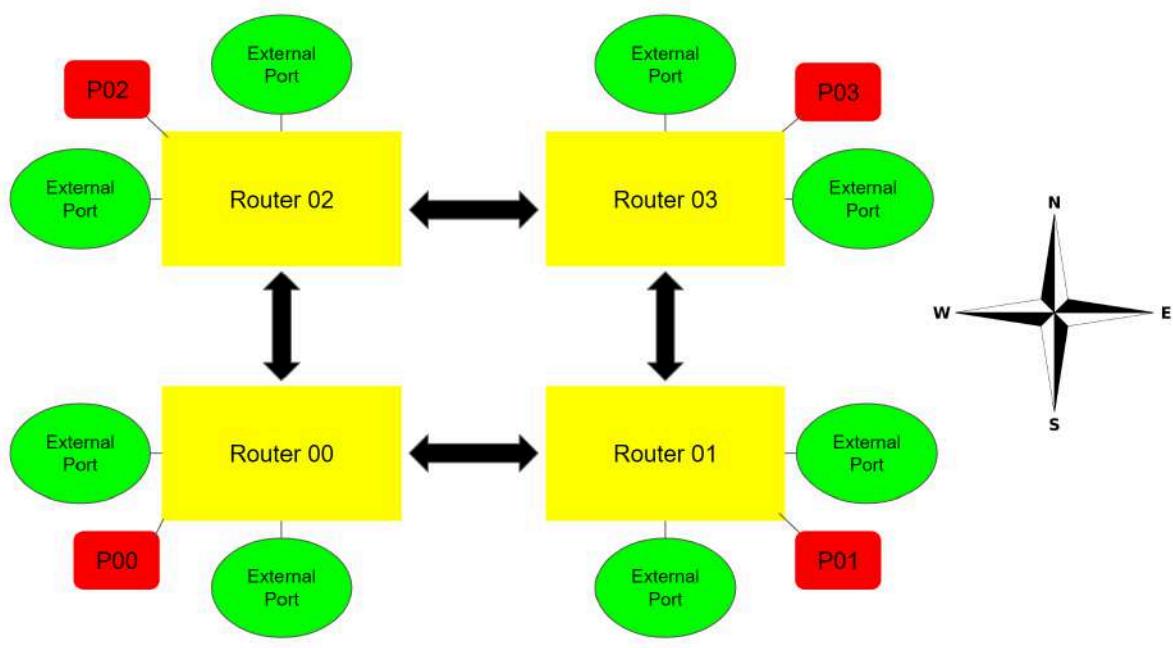
**Router:** This module assists in implementing each core and serves as the building block of our NoC mesh. It receives input of select lines from the master module and ensures the transmission of data to the next hop along the required path.

**Master:** This module helps in assigning the path for data transfer between any two processors

**ProcessorUnit:** This module demonstrates the working of the processor of each router. It has counters which ensure the data has reached the assigned destination up until the last filt.

**Main:** This is the top module for the entire design. It includes instances of Router, Master and ProcessorUnit.

### Block Design:



### Assumptions:

- We have taken an assumption that this NOC design is going to operate on a byte addressable system, i.e, the size of a single packet is going to be one byte.
- We have designed a scalable NOC structure which could be utilized in making up a bigger NOC design. This is to say that this design could be used even for a bigger NOC as a constituent black box, which would automatically route internal paths to process the transaction.
- To make the design more realistic we have utilized the concept of burst size factor.
- We have assumed that a processor in a single transfer can have a maximum burst size of 256 packets.
- NoC allows multiple transactions to occur parallelly. But we can't afford intermixing of packets from different processing units. To avoid this we utilize a mechanism of request and acknowledgement.
- We assume that a processor cannot request for another transfer until all the packets of previous transfer are not transmitted to its corresponding router.
- Now since all transfers of multiple processors are requested parallelly in the system we also needed a mechanism to ensure that requests don't

overlap. We have no restrictions on processing units ( $P\_unit(s)$ ). They can request anything at any point in time.

- We assume that master processes all the requests at the rising edge of the clock and It processes requests of transfer in a priority fashion where the  $P\_unit-0$  gets the highest priority followed by  $P\_unit-1$  and so on.
- Most importantly, we assume that our design works in a synchronous fashion, that is the transfer of a packet from one unit to another happens only at posedge of the clock. ( 1 packet transfer from  $P_0$  to  $P_1$  takes 3 cycles after master approval )
- Also please note that since our design is synchronous and completely pipelined it takes a cycle to see the transfer. (+1 cycle to see the data at  $P_1$  {in above example})
- At last we have an assumption that inputs to this design are constant at the rising edge of the clock. This is because we have flip flops at the input and the output ports.

## Objective

The objective of this part of the project is to gain a hands-on experience on the state-of-the-art CAD tool used for Physical Design and understanding various trade-offs that are involved in Physical Design.

This project is a continuation of VDF Group Project: Part I.

## Choice of Tools

Cadence Innovus for Physical Design

Cadence Tempus for STA

## Library Used

Cadence Fast.lib (90nm)

Interpretation of the results obtained in various steps of Physical Design:  
(Timing/Area/Power trade-offs)

For large utilisation (0.8)

	Setup Slack (ns)	Hold Slack (ns)	Cells	Area ( $\mu m^2$ )	Power (mW)
Before starting physical design	0.730	-0.165	2567	22704.729	8.62
After Placement	0.020	0.022	2790	23096.047	23.51
After Clock Tree Synthesis	0.045	0.025	2797	23228.504	23.12
After Detailed Routing	0.105	0.021	2797	23228.504	22.88

For small utilisation (0.5)

	Setup Slack (ns)	Hold Slack (ns)	Cells	Area ( $\mu m^2$ )	Power (mW)
Before starting Physical design	0.730	-0.165	2567	22704.729	8.62
After Placement	0.024	0.022	2578	22155.220	21.36
After Clock Tree Synthesis	0.020	0.059	2587	22293.733	20.67
After Detailed Routing	0.116	0.016	2579	22308.871	20.53

## Setup Slack

$$\text{Setup Slack} = \text{RT} - \text{AT}$$

Required Time is the difference between the clock period and setup time, while Arrival Time is the time data takes to reach the input pin of the flip-flop. Slack is the difference between the required time and arrival time.

We can see setup slack varies during different design steps. During placement, the tool tries to optimize wire length between cells, affecting critical paths and reducing slack. Clock Tree Synthesis (CTS) adds clock networks and buffers, further reducing slack. Detailed routing increases slack due to actual interconnect delays, which increases the required time more than the arrival time.

## Hold Slack

$$\text{Hold Slack} = \text{AT-RT}$$

Hold violations are resolved after clock tree synthesis and are not considered in the initial two steps. CTS adds buffers to increase delay, improving overall slack. Post routing, hold slack reduces further.

## Cells and Area

In placement, the tool optimizes the logic and removes unnecessary and redundant components, thereby reducing the areas. After doing CTS, it adds additional buffers to increase the area and number of cells. There are no additional cells after routing, so the area remains the same or differs in magnitude by a small amount in the last two stages.

## Power

Power increases after placement due to higher device switching rates, dynamic power dissipation, and device leakages. CTS adds extra inverters and clock buffers, increasing power consumption. No new cells are added during routing, and only small area changes are there, so the power dissipation remains almost constant.

Interpretation of the routability on the change in floorplan:

Core utilization= Area of standard cells+macro area+halo area / Total area allocated for chip

In 0.5 core utilization, 50% area of the chip is used for standard cell placement and 50% area for routing while, for 0.8 core utilization 80% area of the chip is used for standard cell placement and 20% area is used for routing.

## 0.8 core utilization

```
s] Average module density = 0.788.  
s] Density for the design = 0.788.  
s]          = stdcell area 32408 sites (24530 um^2) / alloc_area 41105 sites (31112 um^2).  
s] Pin Density = 0.2687.  
s]          = total # of pins 11348 / total area 42228.  
s] OPERPROF: Starting spMPad at level 1, MEM:1515.2M  
s] OPERPROF: Starting spMPad at level 1, MEM:1515.2M
```

## 0.5 core utilization

```
Average module density = 0.512.  
Density for the design = 0.512.  
    = stdcell_area 29979 sites (22691 um^2) / alloc_area 58560 sites (44324 um^2).  
Pin Density = 0.1781.  
    = total # of pins 10688 / total area 60021.  
OPERPROF: Starting spMPad at level 1, MEM:1515.2M
```

For 0.8 area utilization, 80% of the chip area is used for standard cell placement. Therefore, the area in the case of core utilization is 0.8, and the area used for standard cell placement is more than in the case of core utilization 0.5. Therefore, there is less area for routing, and thus congestion increases, thereby increasing the delays.

Also, as the area for routing is less, interconnects are close to each other so coupling capacitances increase, thereby increasing power dissipation.

In the case of 0.8 utilization, higher metal layers may also be required to reduce the congestion.

## 1. Before starting Physical Design

## STA after DFT (PBA and GBA)

Inputs: Synthesized netlist, library file, and constraints file.

## Output:

## Violation report

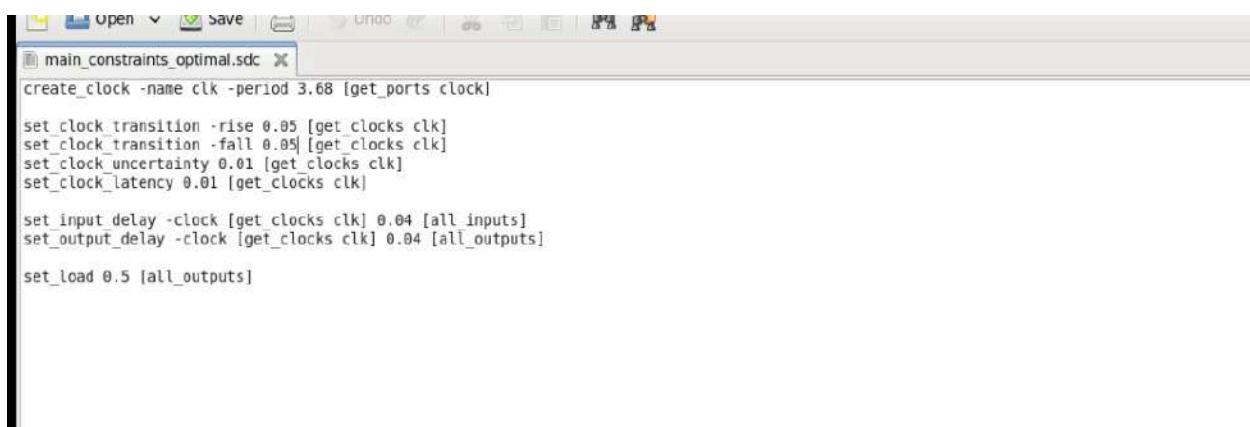
Software Used:

Cadence Tempus

Commands Used:

1. csh
2. source /cadence/cshrc
3. tempus -nowin
4. Source (name of TCL file)

Constraints used:



```
main_constraints_optimal.sdc
create_clock -name clk -period 3.68 [get_ports clock]
set_clock_transition -rise 0.05 [get_clocks clk]
set_clock_transition -fall 0.05 [get_clocks clk]
set_clock_uncertainty 0.01 [get_clocks clk]
set_clock_latency 0.01 [get_clocks clk]
set_input_delay -clock [get_clocks clk] 0.04 [all_inputs]
set_output_delay -clock [get_clocks clk] 0.04 [all_outputs]
set_load 0.5 [all_outputs]
```

## Remarks

The Static Timing Analysis (STA) indicates that no Setup Violations were observed. All data reliably reaches the input of the flip-flops before the setup time of the subsequent clock edge. Hold violations will be resolved during clock tree synthesis.

## Timing Information:-

report\_timing command in Cadence Tempus provides information regarding various paths in the design. The start node and end node of each path is identified.

Static Timing Analysis is done internally by the tool by building a graph for the corresponding circuit, and then through forward traversal of the graph starting from the begin point, we find the arrival time (AT) and then by backward traversal starting from the end point we find the Required Time (RT). The slack is then calculated as RT - AT.

## Effect of slew on timing:-

Slew is the rate at which the transition of signal happens, which is provided to do real-time modeling of signals, i.e., slow rising and falling of signals for nodes to prevent the timing violation. So, delay increases when slew decreases.

We use the following commands to model slew in constraints:-

```
set_clock_transition -rise 0.05 [get_clocks clk]  
set_clock_transition -fall 0.05 [get_clocks clk]
```

## Effect of load on timing:-

The delay of a path is a function of output load. We use set\_load to model the load driven by the output port for correct static timing analysis. Whenever the load increases, the delay will increase.

```
set_load 0.5 [all_outputs]
```

## Effect of positive/negative unateness:-

For a given timing arc, how input transition may lead to a change in output transition defines the timing sense of an arc i.e. unateness. Three types of unateness are there.

- Positive unate:- If rise transition at the input results in a fall transition at the output and fall transition in input results in a fall at the output Ex. And gate, Buffer.
- Negative unate:- If rise transition at the input results in fall transition at the output, and fall transition on the input results in rise in output. Ex. Inverter , NAND gate.

Different cells in the library have different unateness. Based on the unateness of the particular cell, corresponding delays are calculated. The unateness concept reduces the problem space so the complexity of static timing analysis is reduced.

## Effect of GBA and PBA on timing:-

During GBA, we choose the maximum arrival time and slew (that comes from different input timing arcs) at a vertex of a given timing arc to calculate the delay at each stage so that GBA can achieve a safe bound for timing analysis, i.e., pessimistic.

During PBA, we compute the delay of a given timing arc by considering the actual arrival time and the difference between the input and output of the standard cell in the design.

**Command:** **- report\_timing -retime path\_slew\_propagation -max\_path 50 -nworst 50 -path\_type full\_clock >**

Path-based analysis can be done using this command for a maximum of 50 paths.

**Retime:-** This is used to analyze the paths using the specified method (i.e., path-based in this case).

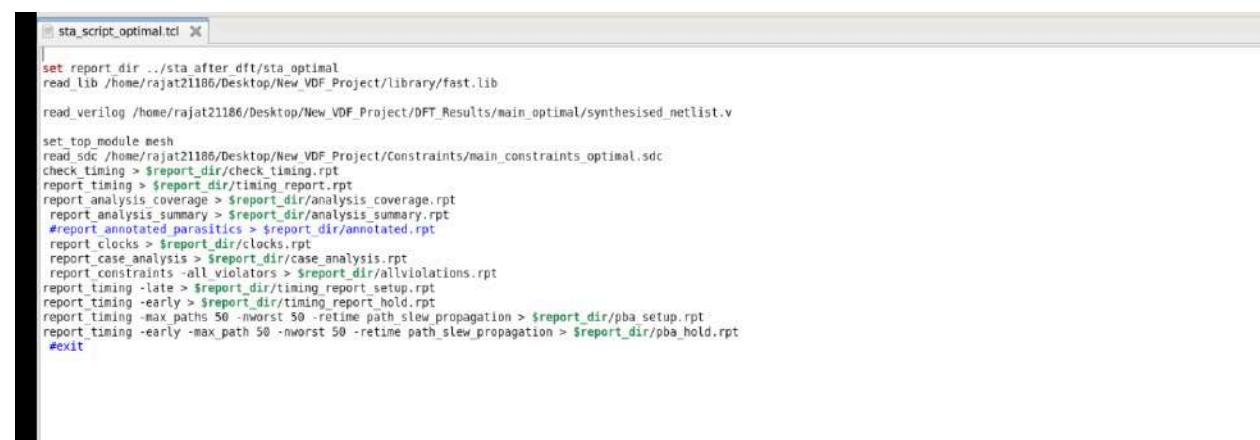
**Path\_slew\_propagation:** -RE -evaluates the given set of Graph-based analysis paths by recalculating the delay values based on the actual propagated slew across the path.

nworst specifies the maximum number of paths to report per endpoint. The default is 1, which reports only the single worst path ending at a given endpoint. Here we have specified 50 paths per end point.

PBA is calculated by taking the exact delay and slew associated with that path. So, Slack is obtained for the same path as GBA, which is done more than the analysis done by GBA, i.e., the improvement in Slack in the case of PBA.

## STA for Minimum Area

TCL File:



```
sta_script_optimal.tcl
set report_dir ..//sta after dft/sta_optimal
read_lib /home/rajat21186/Desktop/New_VDF_Project/library/fast.lib
read_verilog /home/rajat21186/Desktop/New_VDF_Project/DFT_Results/main_optimal/synthesised_netlist.v
set_top_module mesh
read_sdc /home/rajat21186/Desktop/New_VDF_Project/Constraints/main_constraints_optimal.sdc
check_timing > $report_dir/check_timing.rpt
report_timing > $report_dir/timing_report.rpt
report_analysis coverage > $report_dir/analysis_coverage.rpt
report_analysis summary > $report_dir/analysis_summary.rpt
#report annotated_parasitics > $report_dir/annotated.rpt
report_clocks > $report_dir/clocks.rpt
report_case_analysis > $report_dir/case_analysis.rpt
report_constraints_all_violators > $report_dir/allviolations.rpt
report_timing_late > $report_dir/timing_report_setup.rpt
report_timing_early > $report_dir/timing_report_hold.rpt
report_timing -max_paths 50 -nworst 50 -retime path_slew_propagation > $report_dir/pba_setup.rpt
report_timing -early -max_path 50 -nworst 50 -retime path_slew_propagation > $report_dir/pba_hold.rpt
#exit
```

## Violations Report:

192.168.3.58:9072 (edaviewer4:5172 (raja21186)) - RealVNC Viewer

Applications Places System 192.168.3.58:9072 (edaviewer4:5172 (raja21186)) - RealVNC Viewer

File Edit View Search Tools Documents Help

alviolations.rpt (~/Desktop/New\_VDF\_Project/sta\_after\_dft/sta\_minarea) - gedit

main\_constraints\_optimal.sdc timing\_report\_setup.rpt alviolations.rpt

```
# Generated by: Cadence Tools 20.1b-p003_1
# OS: Linux-5.4.0-64-generic-x86_64
# Generated on: wed Apr 17 08:14:39 2024
# Design: mesh
# Command: report constraints -all_violators > ../../sta_after_dft/sta_minarea/alviolations.rpt
# Format : Frame B : split 1

max_delay/setup
-----
No paths found

min_delay/hold
-----
End Point Slack Cause
processor ready signal@2 reg[3]/SE f -0.196 VIOLATED
processor ready signal@2 reg[2]/SE f -0.196 VIOLATED
processor ready signal@2 reg[1]/SE f -0.196 VIOLATED
processor ready signal@2 reg[0]/SE f -0.196 VIOLATED
p1 tlast reg@SE f -0.196 VIOLATED
p3 tlast prev reg@SE f -0.196 VIOLATED
p3 data to routerl reg[7]/SE f -0.196 VIOLATED
p3 data to routerl reg[6]/SE f -0.196 VIOLATED
p3 data to routerl reg[5]/SE f -0.196 VIOLATED
p3 data to routerl reg[4]/SE f -0.196 VIOLATED
p3 data to routerl reg[3]/SE f -0.196 VIOLATED
p3 data to routerl reg[2]/SE f -0.196 VIOLATED
p3 data to routerl reg[1]/SE f -0.196 VIOLATED
p3 data to routerl reg[0]/SE f -0.196 VIOLATED
p3 counter value reg[7]/SE f -0.196 VIOLATED
p3 counter value reg[6]/SE f -0.196 VIOLATED
p3 counter value reg[5]/SE f -0.196 VIOLATED
p3 counter value reg[4]/SE f -0.196 VIOLATED
p3 counter value reg[3]/SE f -0.196 VIOLATED
p3 counter value reg[2]/SE f -0.196 VIOLATED
p3 counter value reg[1]/SE f -0.196 VIOLATED
p3 counter value reg[0]/SE f -0.196 VIOLATED
p2 tlast reg@SE f -0.196 VIOLATED
p2 data to routerl reg[7]/SE f -0.196 VIOLATED
p2 data to routerl reg[6]/SE f -0.196 VIOLATED
p2 data to routerl reg[5]/SE f -0.196 VIOLATED
p2 data to routerl reg[4]/SE f -0.196 VIOLATED
p2 data to routerl reg[3]/SE f -0.196 VIOLATED
p2 data to routerl reg[2]/SE f -0.196 VIOLATED
p2 data to routerl reg[1]/SE f -0.196 VIOLATED
p2 data to routerl reg[0]/SE f -0.196 VIOLATED
```

Main Text Tab Width: 8 Ln 1, Col 1 INS

work\_ground New\_VDF\_Project postPlaceArea alviolations.rpt (~/Desktop/New\_VDF\_Project/sta\_after\_dft/sta\_minarea) sta\_after\_dft sta\_minarea

91% Haze

192.168.3.58:9072 (edaviewer4:5172 (raja21186)) - RealVNC Viewer

Applications Places System 192.168.3.58:9072 (edaviewer4:5172 (raja21186)) - RealVNC Viewer

File Edit View Search Tools Documents Help

alviolations.rpt (~/Desktop/New\_VDF\_Project/sta\_after\_dft/sta\_minarea) - gedit

main\_constraints\_optimal.sdc timing\_report\_setup.rpt alviolations.rpt

```
m0#0 control signal@2 reg[1]/SE f -0.196 VIOLATED
m0#0 control signal@2 reg[9]/SE f -0.196 VIOLATED
m0#0 control signal@2 reg[8]/SE f -0.196 VIOLATED
m0#0 control signal@2 reg[7]/SE f -0.196 VIOLATED
m0#0 control signal@2 reg[6]/SE f -0.196 VIOLATED
m0#0 control signal@2 reg[5]/SE f -0.196 VIOLATED
m0#0 control signal@2 reg[4]/SE f -0.196 VIOLATED
m0#0 control signal@2 reg[2]/SE f -0.196 VIOLATED
m0#0 control signal@2 reg[0]/SE f -0.196 VIOLATED

Check type : clock_period
-----
No paths found

Check type : skew
-----
No paths found

Check type : pulse_width
-----
No violating Checks with given description found

Check type : max_transition
-----
No Violations found

Check type : min_transition
-----
No Violations found

Check type : max_capacitance
-----


| Pin Name   | Required | Actual | Slack  |
|------------|----------|--------|--------|
| m0/11990/Y | 0.243    | 0.449  | -0.206 |
| m0/1177/Y  | 0.243    | 0.335  | -0.092 |


Main Text Tab Width: 8 Ln 1, Col 1 INS
```

work\_ground New\_VDF\_Project postPlaceArea alviolations.rpt (~/Desktop/New\_VDF\_Project/sta\_after\_dft/sta\_minarea) sta\_minarea

91% Haze

## Timing Reports:

### GBA Path

#### Setup Slack

```
#####
Path 1: MET Setup Check with Pin m0/R1 control_signals2_reg[19]/CK
Endpoint: m0/R1 control_signals2_reg[19]/0 (^) checked with leading edge of 'clk'
Beginpoint: p0_configure1_reg[0]/0 (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.010
+ Setup 0.117
+ Phase Shift 3.680
+ Uncertainty 0.010
= Required Time 3.563
- Arrival Time 3.689
- Slack Time 0.474
Clock Rise Edge 5.680
+ Clock Network Latency (Ideal) 0.010
= Beginpoint Arrival Time 0.010
Instance Arc Cell Delay Arrival Required
           Time Time
-----
p0_configure1_reg[0] CK ^ - - 0.810 0.484
p0_configure1_reg[0] CK ^ -> 0 ^ SDFFOX1 0.080 0.090 0.563
g567 A ^ -> Y ^ AND2X1 0.038 0.128 0.602
g551 B ^ -> Y ^ AND2X1 0.144 0.271 0.745
m0/g19212 A ^ -> Y v CLKINVX2 0.063 0.335 0.609
m0/g19004 B v -> Y ^ NAND2XL 0.173 0.508 0.981
m0/g18968 A ^ -> Y v CLKINVX2 0.091 0.599 1.673
m0/g18441 B0 v -> Y ^ AO121X1 0.081 0.680 1.144
m0/g18463 B0 v -> Y ^ AO121X1 0.081 0.727 1.111
m0/g18428 A ^ -> Y v CLKINVX1 0.010 0.747 1.221
m0/g18375 B0 v -> Y ^ AO121X1 0.030 0.777 1.251
m0/g18291 A1 ^ -> Y v AO1211X1 0.023 0.880 1.274
m0/g18209 A v -> Y ^ NOR3X1 0.679 1.479 1.952
m0/g18288 A ^ -> Y v CLKINVX2 0.069 1.548 2.622
m0/g18253 A1 v -> Y ^ AO121X1 0.099 1.647 2.121
m0/g18234 A1 ^ -> Y ^ AO222X1 0.051 1.698 2.172
m0/g18229 C0 ^ -> Y v AO1221X1 0.013 1.711 2.184
m0/g18227 A v -> Y ^ CLKINVX1 0.022 1.732 2.206
m0/g18225 B0 ^ -> Y v AO1211X1 0.013 1.746 2.219
m0/g18223 C v -> Y ^ NAND3XL 0.118 1.864 2.338
m0/g18222 A -> Y ^ CLKINVX3 0.105 1.969 2.443
m0/g18182 A1 v -> Y ^ AO121X1 0.052 2.021 2.495
m0/g18103 A1 ^ -> Y ^ AO222X1 0.043 2.065 2.538
m0/g18158 C0 ^ -> Y v CLKINVX1 0.027 2.092 2.566
m0/g18156 A v -> Y ^ CLKINVX1 0.021 2.113 2.586
m0/g18153 B0 ^ -> Y v AO1211X1 0.025 2.138 2.611
m0/g18152 C v -> Y ^ NOR4BX1 0.724 2.861 3.335
m0/g18151 A ^ -> Y v CLKINVX2 0.063 2.925 3.399
m0/g18149 B0 v -> Y ^ AO121X1 0.093 3.018 3.491
m0/g18885 B0 ^ -> Y v AO121X1 0.000 3.024 3.498
```

#### Hold Slack

The screenshot shows the Cadence Tempus interface with several tabs open. The tabs include: main\_constraints\_optimal.sdc, timing\_report\_setup.rpt, allviolations.rpt, innovus.logv16, innovus.logv15, timing\_report\_hold.rpt, and timing\_report\_hold.rpt. The timing\_report\_hold.rpt tab is active.

```
#####
# Generated by: Cadence Tempus 20.10-p003.1
# OS: Linux x86_64 (Host ID: edaserver4)
# Generated on: Wed Apr 17 00:14:19 2024
# Design: mesh
# Command: report timing -early > sreport dir/timing_report_hold.rpt
#####
Path 1: VIOLATED Hold Check with Pin m0/R0 control_signals2_reg[0]/CK
Endpoint: m0/R0 control_signals2_reg[0]/SE (v) checked with leading edge of 'clk'
Beginpoint: scan en (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.010
+ Hold 0.226
+ Phase Shift 9.000
+ Uncertainty 0.010
= Required Time 9.246
- Arrival Time 9.050
Arrival Time 9.050
Slack Time -0.196
Clock Rise Edge 0.000
+ Input Delay 0.040
+ Network Insertion Delay 0.010
= Beginpoint Arrival Time 0.050
Instance Arc Cell Delay Arrival Required
           Time Time
-----
- scan en v - - 0.050 0.246
m0/R0 control_signals2_reg[0] SE v SDFFRHQX1 0.000 0.050 0.246
```

**Slack Computation (worst path):**

**Setup case:**

Tclk = 3.68ns, Tsetup = 0.117ns , Begin point : p0\_configure1\_reg[0]/Q, End point : m0/R1\_control\_signals2\_reg[19]

**Required Time:** The data must reach the next flip-flop ‘setup time’ before the next clock edge arrives. Since Tclk= 3.68ns, we have an uncertainty of 0.010ns. In the worst case for setup analysis, the clock can only come after 3.67ns. However, we have a delay of 0.010 ns too. This delay and uncertainty cancel, leaving us with 3.68 ns as the time to the next clock edge. The setup time of a flip-flop is 0.117ns. Hence, we want our data to be available within 3.563ns (3.68-0.117) from when the current clock edge has arrived.

**Arrival Time:**

This is the time our data took to reach the input pin of the flip-flop. The tool estimates it to be 3.089ns. We wanted our data to come before 3.563 ns, which came at 3.089 ns only. This implies our constraint is met, and we don’t have a violation.

**Slack Time:**

Slack = Required Time - Arrival Time = 3.563 - 3.089 = 0.474ns.

**Hold case:**

BeginPoint : scan\_en, Endpoint: m0/R0\_control\_signals2\_reg[0]

**Required Time:** Other End Arrival time(+ 0.010ns) + Hold time (+ 0.026) + Uncertainty(+0.010) = 0.246ns

**Arrival Time:** This is the time our data took to reach the input pin of the flip-flop. The tool estimates it to be 0.050ns. We wanted our data to come before 0.246 ns, which came at 3.089 ns only. This implies our constraint is not met, and we have a violation.

**Slack:** AT-RT = -0.196ns

## PBA Path

### Setup Slack

```
#####
# Generated by: Cadence Tempus 20.10-p063_1
# OS: Linux x86_64 (Host ID edserver4)
# Generated on: Tue Apr 16 23:58:53 2024
# Design: mesh
# Command: report_timing -retime path_slew_propagation -max_path 50 -rworst 50 -path_type full_clock > $report_dir/pba.rpt
#####
Path 1: MET Setup Check with Pin m0/R1 control_signals2_reg[19]/CK
Endpoint: m0/R1 control_signals2_reg[19]/0 (^) checked with leading edge of 'clk'
Beginpoint: p0_configure1_reg[0]/0 (^) triggered by leading edge of 'clk'
Path Groups: (clk)
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.010
- Setup 0.002
+ Phase Shift 3.600
- Uncertainty 0.010
= Required Time 3.598
- Arrival Time 3.598
= Slack Time 0.000
= Slack Time(original) 0.474
    Clock Rise Edge 0.000
        + Network Insertion Delay 0.010
        = Beginpoint Arrival Time 0.010
Timing Path:
-----  

Instance Arc Cell Retime Arrival Required  

Delay Time Time
-----  

- clock ^ - - 0.010 0.578
p0_configure1_reg[0] - SDFF0X1 0.000 0.010 0.578
p0_configure1_reg[0] CK ^ -> Q ^ SDFF0X1 0.000 0.099 0.658
g507 - - 0.000 0.000 0.000
g507 A ^ -> Y ^ AND2X1 0.106 0.128 0.690
g551 - - 0.000 0.000 0.000
g551 B ^ -> Y ^ AND2X1 0.144 0.271 0.840
m0/g19212 - CLKINVX2 0.000 0.271 0.840
m0/g19212 A ^ -> Y Y CLKINVX2 0.064 0.335 0.903
m0/g19004 NAND2XL 0.000 0.333 0.903
m0/g19004 B v -> Y ^ NAND2XL 0.173 0.508 1.076
m0/g18968 - - 0.000 0.508 1.076
m0/g18968 A ^ -> Y v CLKINVX2 0.091 0.599 1.167
m0/g18611 - - 0.000 0.599 1.167
m0/g18611 BB v -> Y ^ AO121X1 0.001 0.680 1.248
m0/g18463 - - 0.000 0.680 1.248
m0/g18463 BB ^ -> Y ^ AO21X1 0.057 0.737 1.305
m0/g18428 - - 0.000 0.737 1.305
m0/g18428 A ^ -> Y Y CLKINVX1 0.010 0.747 1.315
m0/g18375 - - 0.000 0.747 1.315
m0/g18375 BB v -> Y ^ AO121X1 0.030 0.777 1.345
m0/g18375 - - 0.000 0.777 1.345
-----
```

### Hold Slack

```
#####
# Generated by: Cadence Tempus 20.10-p063_1
# OS: Linux x86_64 (Host ID edserver4)
# Generated on: Wed Apr 17 00:14:19 2024
# Design: mesh
# Command: report_timing -early -max_path 50 -rworst 50 -retime path_slew_propagation > $report_dir/pba_hold.rpt
#####
Path 1: VIOLATED Hold Check with Pin m0/R2 control_signals2_reg[14]/CK
Endpoint: m0/R2 control_signals2_reg[14]/SE (v) checked with leading edge of 'clk'
Beginpoint: scan_en (v) triggered by leading edge of 'clk'
Path Groups: (clk)
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.010
+ Hold 0.226
+ Phase Shift 6.800
+ Uncertainty 0.010
= Required Time 6.246
Arrival Time 6.050
Slack Time -0.196
= Slack Time(original) -0.196
    Clock Rise Edge 0.000
        + Input Delay 0.040
        + Network Insertion Delay 0.010
        = Beginpoint Arrival Time 0.050
Timing Path:
-----  

Instance Arc Cell Retime Arrival Required  

Delay Time Time
-----  

- scan_en v - - 0.050 0.246
m0/R2_control_signals2_reg[14] - SDFFRH0X4 0.000 0.050 0.246
-----  

Path 2: VIOLATED Hold Check with Pin m0/R2 control_signals2_reg[13]/CK
Endpoint: m0/R2 control_signals2_reg[13]/SE (v) checked with leading edge of 'clk'
Beginpoint: scan_en (v) triggered by leading edge of 'clk'
Path Groups: (clk)
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.010
+ Hold 0.226
+ Phase Shift 6.800
+ Uncertainty 0.010
= Required Time 6.246
Arrival Time 6.050
Slack Time -0.196
= Slack Time(original) -0.196
    Clock Rise Edge 0.000
        + Input Delay 0.040
        + Network Insertion Delay 0.010
        = Beginpoint Arrival Time 0.050
-----
```

*Slack Computation (worst path):*

Tclk = 3.68ns, Tsetup = 0.082ns , Begin point : p0\_configure1\_reg[0]/Q, End point : m0/R1\_control\_signals2\_reg[19]

**Required Time:** The data must reach the next flip-flop ‘setup time’ before the next clock edge arrives. Since Tclk= 3.68ns, we have an uncertainty of 0.010ns. In the worst case for setup analysis, the clock can only come after 3.67ns. However, we have a delay of 0.010 ns too. This delay and uncertainty cancel, leaving us with 3.68 ns as the time to the next clock edge. The setup time of a flip-flop is 0.082ns. Hence, we want our data to be available within 3.598ns (3.68-0.082) from when the current clock edge has arrived.

**Arrival Time:**

This is the time our data took to reach the input pin of the flip-flop. The tool estimates it to be 3.030ns. We wanted our data to come before 3.598 ns, which came at 3.030 ns only. This implies our constraint is met, and we don't have a violation.

**Slack Time:**

Slack = Required Time - Arrival Time = 3.598 - 3.030 = 0.568ns.

In the STA after DFT, in the case of graph-based analysis, the slack time is 0.474ns, and in the case of path-based analysis, the slack time is 0.568ns.

**Hold case:**

BeginPoint : scan\_en, Endpoint: m0/R0\_control\_signals2\_reg[0]

**Required Time:** Other End Arrival time(+ 0.010ns) + Hold time (+ 0.026) + Uncertainty(+0.010) = 0.246ns

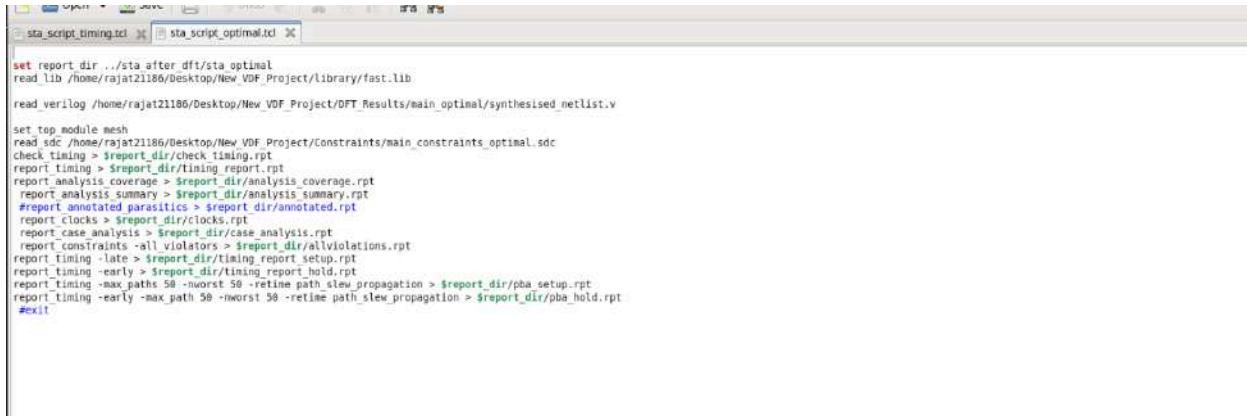
**Arrival Time:** This is the time our data took to reach the input pin of the flip-flop. The tool estimates it to be 0.050ns. We wanted our data to come before 0.246 ns, which came at 3.089 ns only. This implies our constraint is not met, and we have a violation.

**Slack:** AT-RT = -0.196ns

The graph-based analysis is a more pessimistic way to calculate the slack time, while path-based analysis gives the actual slack time, which should be greater than or equal to the slack time from the graph-based analysis.

## STA for Optimal Case:

TCL File:



```
sta_script.timing.tcl sta_script_optimal.tcl

set report_dir ../sta_after_dft/sta_optimal
read lib /home/rajat21186/Desktop/New_VDF_Project/library/fast.lib
read_verilog /home/rajat21186/Desktop/New_VDF_Project/DFT_Results/main_optimal/synthesised_netlist.v

set_top module mesh
read_sdc /home/rajat21186/Desktop/New_VDF_Project/Constraints/main_constraints_optimal.sdc
check_timing > $report_dir/stack_timing.rpt
report_timing > $report_dir/timing.rpt
report_analysis coverage > $report_dir/analysis coverage.rpt
report_analysis summary > $report_dir/analysis summary.rpt
#report annotated_statistics > $report_dir/annotated.rpt
report_clocks > $report_dir/clocks.rpt
report_case_analysis > $report_dir/case_analysis.rpt
report_constraints -all_violators > $report_dir/allviolations.rpt
report_timing -late > $report_dir/timing_report_setup.rpt
report_timing -early > $report_dir/timing_report_hold.rpt
report_timing -max_paths 50 -worst 50 -retime path slew_propagation > $report_dir/pba_setup.rpt
report_timing -early -max_path 50 -worst 50 -retime path slew_propagation > $report_dir/pba_hold.rpt
#exit
```

## Violations Report:



```
#####
# Generated by: Cadence Tempus 20.10-p001
# OS: Linux x86_64 (Host ID: edaserver4)
# Generated on: Wed Apr 17 12:08:15 2024
# Design: mesh
# Command: report_constraints -all_violators > ./sta_after_dft/sta_optimal/allviolations.rpt
#####
# format : frame # : split 1

max_delay/setup
-----
No paths found

min_delay/hold
-----
End Point Slack Cause
-----
processor ready_signals2 reg[3]/SE f -0.165 VIOLATED
processor ready_signals2 reg[2]/SE f -0.165 VIOLATED
processor ready_signals2 reg[1]/SE f -0.165 VIOLATED
processor ready_signals2 reg[0]/SE f -0.165 VIOLATED
p3_tlast_req/SE f -0.165 VIOLATED
p3_data_to_router1 reg[7]/SE f -0.165 VIOLATED
p3_data_to_router1 reg[6]/SE f -0.165 VIOLATED
p3_data_to_router1 reg[5]/SE f -0.165 VIOLATED
p3_data_to_router1 reg[4]/SE f -0.165 VIOLATED
p3_data_to_router1 reg[3]/SE f -0.165 VIOLATED
p3_data_to_router1 reg[2]/SE f -0.165 VIOLATED
p3_data_to_router1 reg[1]/SE f -0.165 VIOLATED
p3_data_to_router1 reg[0]/SE f -0.165 VIOLATED
p3_counter_value_reg[7]/SE f -0.165 VIOLATED
p3_counter_value_reg[6]/SE f -0.165 VIOLATED
p3_counter_value_reg[5]/SE f -0.165 VIOLATED
p3_counter_value_reg[4]/SE f -0.165 VIOLATED
p3_counter_value_reg[3]/SE f -0.165 VIOLATED
p3_counter_value_reg[2]/SE f -0.165 VIOLATED
p3_counter_value_reg[1]/SE f -0.165 VIOLATED
p3_counter_value_reg[0]/SE f -0.165 VIOLATED
p2_tlast_req/SE f -0.165 VIOLATED
p2_tlast_prev_req/SE f -0.165 VIOLATED
p2_data_to_router1 reg[7]/SE f -0.165 VIOLATED
p2_data_to_router1 reg[6]/SE f -0.165 VIOLATED
p2_data_to_router1 reg[5]/SE f -0.165 VIOLATED
p2_data_to_router1 reg[4]/SE f -0.165 VIOLATED
p2_data_to_router1 reg[3]/SE f -0.165 VIOLATED
p2_data_to_router1 reg[2]/SE f -0.165 VIOLATED
p2_data_to_router1 reg[1]/SE f -0.165 VIOLATED
p2_data_to_router1 reg[0]/SE f -0.165 VIOLATED
```

```

m0/R1_control_signals2_reg[10]/SE f -0.165 VIOLATED
m0/R1_control_signals2_reg[9]/SE f -0.165 VIOLATED
m0/R1_control_signals2_reg[8]/SE f -0.165 VIOLATED
m0/R1_control_signals2_reg[7]/SE f -0.165 VIOLATED
m0/R1_control_signals2_reg[6]/SE f -0.165 VIOLATED
m0/R1_control_signals2_reg[5]/SE f -0.165 VIOLATED
m0/R1_control_signals2_reg[4]/SE f -0.165 VIOLATED
m0/R1_control_signals2_reg[2]/SE f -0.165 VIOLATED
m0/R1_control_signals2_reg[1]/SE f -0.165 VIOLATED
m0/R1_control_signals2_reg[0]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[13]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[12]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[11]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[10]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[9]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[8]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[7]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[6]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[5]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[4]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[13]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[12]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[11]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[10]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[9]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[8]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[7]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[6]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[5]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[4]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[2]/SE f -0.165 VIOLATED
m0/R0_control_signals2_reg[0]/SE f -0.165 VIOLATED
-----
Check type : clock_period
No paths found
Check type : skew
No paths found
Check type : pulse_width
No violating Checks with given description found
Check type : max_transition
No Violations found
Check type : min_transition
No Violations found

```

## Timing Reports:

### GBA Path

#### Setup Slack

```

#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64 [Host ID edaserver4]
# Generated on: Wednesday April 17 12:08:15 2024
# Design: mesh
# Command: report_timing -late > $report_dir/timing_report_setup.rpt
#####
Path 1: MET Setup Check with Pin m0/R1_control_signals2_reg[19]/0 (^) checker with leading edge of 'clk'
Beginpoint: p1_configure1_reg[0]/0 (^) triggered by leading edge of 'clk'
Path Groups: (clk)
Other End Arrival Time 0.018
- Setup 0.098
+ Phase Shift 3.688
- Uncertainty 0.018
= Required Time 3.582
- Arrival Time 2.851
= Slack Time 0.730
Clock Rise Edge 0.000
+ Clock Network Latency (Ideal) 0.018
= Beginpoint Arrival Time 0.018
-----
Instance Arc Cell Delay Arrival Required
Time Time
p1_configure1_reg[0] CK ^ - 0.010 0.748
p1_configure1_reg[0] CK ^ -> 0 ^ S0FFQX1 0.088 0.099 0.829
g569 A ^ -> Y ^ AND2X1 0.038 0.128 0.858
q55 A ^ -> Y ^ AND2X1 0.038 0.052 0.951
m0/q19004 B ^ -> Y ^ OR2X1 0.162 0.283 1.113
m0/q18968 A ^ -> Y v CLKINWVX1 0.198 0.493 1.214
m0/q18612 B0 v -> Y ^ A0I21X1 0.072 0.555 1.286
m0/q18465 B0 ^ -> Y ^ O2I21X1 0.055 0.611 1.341
m0/q18431 A ^ -> Y v CLKINWVX1 0.018 0.621 1.351
m0/q18377 B0 v -> Y ^ A0T21X1 0.034 0.654 1.385
m0/q18304 A1 ^ -> Y v OA2221X1 0.038 0.684 1.415
m0/g18301 A v -> Y v INVX1 0.018 0.703 1.433
m0/g18292 B ^ -> Y ^ AND4X2 0.504 1.266 1.997
m0/g18291 A ^ -> Y v CLKINWVX1 0.073 1.348 2.078
m0/g18256 A1 v -> Y ^ OA1221X1 0.087 1.426 2.157
m0/g18235 A1 ^ -> Y v A0S21X1 0.068 1.477 2.207
m0/g18228 CB ^ -> Y v A0I2221X1 0.011 1.487 2.218
m0/g18225 B v -> Y ^ NM02ZXL 0.023 1.510 2.240
m0/g18224 D ^ -> Y ^ OR4X1 0.123 1.633 2.363
m0/g18223 A ^ -> Y v CLKINWVX3 0.104 1.737 2.467
m0/g18183 A1 v -> Y ^ A0I21X1 0.047 1.784 2.514
m0/g18163 A1N ^ -> Y ^ OA12BB1X1 0.039 1.823 2.553
m0/g18154 C0 ^ -> Y v OA1211X1 0.028 1.851 2.581
m0/g18153 B0 v -> Y ^ A0T21X1 0.038 1.888 2.619
m0/g2 AN ^ -> Y ^ NOR4BX1 0.742 2.631 3.361

```

```

Path 1: NET Setup Check with Pin m0/R1_control_signals2_reg[19]/CK
Endpoint: m0/R1_control_signals2_reg[19]/Q (^) checked with leading edge of 'clk'
Beginpoint: p0_configure1_reg[0]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.010
+ Setup 0.008
+ Phase Shift 3.680
+ Uncertainty 0.010
+ Required Time 3.582
+ Arrival Time 2.851
+ Slack Time 0.730
Clock Rise Edge 0.006
+ Clock Network Latency (Ideal) 0.010
+ Beginpoint Arrival Time 0.010
+ -----
Instance Arc Cell Delay Arrival Required
Time Time
-----
p0_configure1_reg[0] CK ^ - 0.010 0.740
p0_configure1_reg[0] CK ^ -> Q ^ SDFFQX1 0.080 0.090 0.820
g560 A ^ -> Y ^ AND2X1 0.038 0.128 0.858
g553 B ^ -> Y ^ AND2X1 0.092 0.220 0.951
m0/g10804 B ^ -> Y ^ OR2X1 0.162 0.383 1.113
m0/g10805 A ^ -> Y ^ CLKINVX1 0.038 0.093 1.214
m0/g10812 B0 ^ -> Y ^ AO121X1 0.072 0.255 1.286
m0/g10465 B0 ^ -> Y ^ OA1X1 0.055 0.611 1.341
m0/g10431 A ^ -> Y v CLKINVX1 0.010 0.621 1.351
m0/g10377 B0 v -> Y ^ AO121X1 0.034 0.654 1.385
m0/g10304 A1 ^ -> Y v AO1221X1 0.030 0.684 1.415
m0/g10301 A V -> Y ^ INVX1 0.018 0.703 1.433
m0/g10292 B ^ -> Y ^ AND4XL 0.564 1.266 1.997
m0/g10291 A ^ -> Y v CLKINVX2 0.073 1.340 2.076
m0/g10256 A1 v -> Y ^ AO121X1 0.087 1.426 2.157
m0/g10235 A1 ^ -> Y ^ AO22X1 0.050 1.477 2.297
m0/g10228 C0 ^ -> Y v AO1221X1 0.030 1.487 2.218
m0/g10225 B V -> Y ^ NAND4XL 0.023 1.502 2.046
m0/g10224 D ^ -> Y ^ OR4X1 0.123 1.633 2.363
m0/g10233 A ^ -> Y v CLKINVX3 0.104 1.737 2.467
m0/g10185 A1 v -> Y ^ AO121X1 0.047 1.784 2.514
m0/g10163 A1N ^ -> Y ^ OA12B1X1 0.039 1.823 2.593
m0/g10154 C0 ^ -> Y v OA121X1 0.028 1.851 2.581
m0/g10153 B0 v -> Y ^ AO121X1 0.038 1.888 2.619
m0/g2 AN ^ -> Y ^ NOR4BX1 0.742 2.631 3.361
m0/g10151 A ^ -> Y v CLKINVX2 0.063 2.694 3.425
m0/g10149 B0 v -> Y ^ AO121X1 0.093 2.787 3.517
m0/g10085 B0 ^ -> Y v AO121X1 0.006 2.793 3.524
m0/g10063 A V -> Y ^ NAND4XL 0.058 2.851 3.582
m0/R1_control_signals2_reg[19] D - SDFFRHQX1 0.000 2.851 3.582
-----
```

## Hold Slack

```

#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64 Host ID edserver4)
# Generated on: Wed Apr 17 12:08:15 2024
# Design: nesh
# Command: report timing -early > $report_dir/timing_report_hold.rpt
#####
Path 1: VIOLATED Hold Check with Pin m0/R0 control_signals2_reg[0]/CK
Endpoint: m0/R0_control_signals2_reg[0]/SE (v) checked with leading edge of 'clk'
Beginpoint: scan_en (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.010
+ Hold 0.195
+ Phase Shift 0.000
+ Uncertainty 0.010
+ Required Time 0.215
Arrival Time 0.050
Slack Time -0.165
Clock Rise Edge 0.000
+ Input Delay 0.040
+ Network Insertion Delay 0.010
= Beginpoint Arrival Time 0.050
-----
Instance Arc Cell Delay Arrival Required
Time Time
-----
- scan_en v - 0.050 0.215
m0/R0_control_signals2_reg[0] SE v SDFFRHQX1 0.000 0.050 0.215
-----
```

## Slack Computation (worst path):

Tclk = 3.68ns, Tsetup = 0.082ns , Begin point : p0\_configure1\_reg[0]/Q, Endpoint : m0/R1\_control\_signals2\_reg[19]

**Required Time:** The data must reach the next flip-flop ‘setup time’ before the next clock edge arrives. Since Tclk= 3.68ns, we have an uncertainty of 0.010ns. In the worst case for setup analysis, the clock can only come after 3.67ns. However, we have a delay of 0.010 ns too. This delay and uncertainty cancel, leaving us with 3.68 ns as the time to the next clock edge. The

setup time of a flip-flop is 0.098ns. Hence, we want our data to be available within 3.582ns (3.68-0.098) from when the current clock edge has arrived.

**Arrival Time:**

This is the time our data took to reach the input pin of the flip-flop. The tool estimates it to be 2.851ns. We wanted our data to come before 3.582 ns, which came at 2.851 ns only. This implies our constraint is met, and we don't have a violation.

**Slack Time:**

$$\text{Slack} = \text{Required Time} - \text{Arrival Time} = 3.582 - 2.851 = 0.730\text{ns}$$

In the STA after DFT, in the case of graph-based analysis, the slack time is 0.730 ns. This implies our constraint is met, and we don't have a violation.

**Hold case:**

BeginPoint : scan\_en, Endpoint: m0/R0\_control\_signals2\_reg[0]

**Required Time:** Other End Arrival time(+ 0.010ns) + Hold time (+ 0.195ns) + Uncertainty(+0.010) = 0.215ns

**Arrival Time:** This is the time our data took to reach the input pin of the flip-flop. The tool estimates it to be 0.050ns. We wanted our data to come before 0.246 ns, which came at 3.089 ns only. This implies our constraint is not met, and we have a violation.

**Slack:** AT-RT = -0.165ns

PBA Path

## Setup Slack

```
#####
# Generated by: Cadence Tempus 20.10-p003_1
# Linux x86_64 Host ID edaserver4
# Generated on: Wed Apr 17 12:08:15 2024
# Design: mesh
# Command: report timing -max paths 50 -worst 50 -retime path_slew_propagation > $report_dir/pba_setup.rpt
#####
Path 1: MET Setup Check with Pin m0/R1 control_signals2 reg[19]/CK
Endpoint: m0/R1_control_signals2_reg[19]/D (^) checked with leading edge of 'clk'
Beginpoint: p1_configure1_reg[0]/Q (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.018
  + Setup 0.000
  + Phase Shift 3.598
  + Uncertainty 0.018
  = Required Time 3.598
  Arrival Time 2.804
  Slack Time 0.798
  = Slack Time(original) 0.798
    Clock Rise Edge 0.000
    + Clock Network Latency (Ideal) 0.010
    = Beginpoint Arrival Time 0.010
    - Slack Time 0.798
      Instance Arc Cell Retime Arrival Required
      ----- Delay Time Time
      p1_configure1_reg[8] CK ^ - 0.010 0.796
      p1_configure1_reg[8] CK ^ -> 0 ^ AND2X1 0.000 0.000 0.876
      g568 - CLKINXX1 0.000 0.000 0.876
      g568 A ^ -> Y ^ AND2X1 0.038 0.128 0.914
      g553 - AND2X1 0.000 0.128 0.914
      g553 B ^ -> Y ^ AND2X1 0.032 0.226 1.005
      m0/q19084 - AND2X1 0.000 0.226 1.005
      m0/q19084 B ^ -> Y ^ DR2X1 0.162 0.283 1.169
      m0/q19068 - CLKINXX1 0.000 0.283 1.169
      m0/q19068 A ^ -> Y v CLKINXX1 0.100 0.483 1.269
      m0/q18612 - A0121X1 0.000 0.483 1.269
      m0/q18612 B0 v -> Y ^ A0121X1 0.072 0.555 1.341
      m0/q18465 - D021X1 0.000 0.555 1.341
      m0/q18465 B0 ^ -> Y ^ D021X1 0.056 0.611 1.396
      m0/q18431 - CLKINXX1 0.000 0.611 1.396
      m0/q18431 A ^ -> Y v CLKINXX1 0.010 0.621 1.406
      m0/q18377 - A0121X1 0.000 0.621 1.406
      m0/q18377 B0 v -> Y ^ A0122X1 0.034 0.654 1.440
      m0/q18304 - D0221X1 0.000 0.654 1.440
      m0/q18304 A1 ^ -> Y v D0221X1 0.030 0.684 1.479
      m0/q18301 - INVX1 0.000 0.684 1.479
      m0/q18301 A v -> Y ^ INVX1 0.015 0.699 1.485
      m0/q18292 - AND4XL 0.000 0.699 1.485
```

## Hold Slack

```
#####
# Generated by: Cadence Tempus 20.10-p003_1
# Linux x86_64 Host ID edaserver4
# Generated on: Wed Apr 17 12:08:15 2024
# Design: mesh
# Command: report timing -early -max_path 50 -worst 50 -retime path_slew_propagation > $report_dir/pba_hold.rpt
#####
Path 1: VIOLATED Hold Check with Pin m0/R2 control_signals2 reg[14]/CK
Endpoint: m0/R2_control_signals2_reg[14]/SE (v) checked with leading edge of 'clk'
Beginpoint: scan_en (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.010
  + Hold 0.195
  + Phase Shift 0.000
  + Uncertainty 0.010
  = Required Time 0.215
  Arrival Time 0.050
  Slack Time -0.165
  = Slack Time(original) -0.165
    Clock Rise Edge 0.000
    + Input Delay 0.040
    + Network Insertion Delay 0.010
    = Beginpoint Arrival Time 0.050
    - Slack Time 0.000
      Instance Arc Cell Retime Arrival Required
      ----- Delay Time Time
      - scan_en v - 0.050 0.215
      m0/R2_control_signals2_reg[14] - SDFFRM0X4 0.000 0.050 0.215
      Path 2: VIOLATED Hold Check with Pin m0/R2 control_signals2 reg[13]/CK
Endpoint: m0/R2_control_signals2_reg[13]/SE (v) checked with leading edge of 'clk'
Beginpoint: scan_en (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.010
  + Hold 0.195
  + Phase Shift 0.000
  + Uncertainty 0.010
  = Required Time 0.215
  Arrival Time 0.050
  Slack Time -0.165
  = Slack Time(original) -0.165
    Clock Rise Edge 0.000
    + Input Delay 0.040
    + Network Insertion Delay 0.010
    = Beginpoint Arrival Time 0.050
    - Slack Time 0.000
      Instance Arc Cell Retime Arrival Required
      ----- Delay Time Time
      - scan_en v - 0.050 0.215
```

Slack Computation (worst path):

Tclk = 3.68ns, Tsetup = 0.082ns , Begin point : p0\_configure1\_reg[0]/Q, End point : m0/R1\_control\_signals2\_reg[19]

**Required Time:** The data must reach the next flip-flop ‘setup time’ before the next clock edge arrives. Since Tclk= 3.68ns, we have an uncertainty of 0.010ns. In the worst case for setup analysis, the clock can only come after 3.67ns. However, we have a delay of 0.010 ns too. This delay and uncertainty cancel, leaving us with 3.68 ns as the time to the next clock edge. The setup time of a flip-flop is 0.090ns. Hence, we want our data to be available within 3.59ns (3.68-0.090) from when the current clock edge has arrived.

#### **Arrival Time:**

This is the time our data took to reach the input pin of the flip-flop. The tool estimates it to be 2.804 ns. We wanted our data to come before 3.59 ns, which came at 2.804 ns only. This implies our constraint is met, and we don’t have a violation.

#### **Slack Time:**

Slack = Required Time - Arrival Time = 3.598 - 2.804 = 0.786s.

In the STA after DFT, in the case of graph-based analysis, the slack time is 0.730ns, and in the case of path-based analysis, the slack time is 0.786ns.

The graph-based analysis is a more pessimistic way to calculate the slack time, while path-based analysis gives the actual slack time, which should be greater than or equal to the slack time from the graph-based analysis.

#### **Hold case:**

BeginPoint : scan\_en, Endpoint: m0/R0\_control\_signals2\_reg[0]

**Required Time:** Other End Arrival time(+ 0.010ns) + Hold time (+ 0.195) + Uncertainty(+0.010) = 0.215ns

**Arrival Time:** This is the time our data took to reach the input pin of the flip-flop. The tool estimates it to be 0.050ns. We wanted our data to come before 0.246 ns, which came at 3.089 ns only. This implies our constraint is not met, and we have a violation.

**Slack:** AT-RT = -0.165ns

The graph-based analysis is a more pessimistic way to calculate the slack time, while path-based analysis gives the actual slack time, which should be greater than or equal to the slack time from the graph-based analysis.

In this case, the slack in the GBA and PBA analysis is equal.

## STA for Tight Constraints:

### TCL File:

```
set report_dir ../sta_after_dft/sta_timing
read_lib /home/rajat21186/Desktop/New_VDF_Project/library/fast.lib
read_verilog /home/rajat21186/Desktop/New_VDF_Project/DFT_Results/main_timing/synthesised_netlist.v

set_top_module mesh
read_sdc /home/rajat21186/Desktop/New_VDF_Project/Constraints/main_constraints_optimal.sdc
check_timing > $report_dir/check_timing.rpt
report_timing > $report_dir/timing_report.rpt
report_analyst_coverage > $report_dir/analysis_coverage.rpt
report_analysis_summary > $report_dir/analysis_summary.rpt
#report_annotated_paritics > $report_dir/annotated.rpt
report_clocks > $report_dir/clocks.rpt
report_case_analysis > $report_dir/case_analysis.rpt
report_constraints -all_violators > $report_dir/allviolations.rpt
report_timing -late > $report_dir/timing_report_hold.rpt
report_timing -max_paths 50 -worst 50 -retime path_slew_propagation > $report_dir/pba_setup.rpt
report_timing -early -max_path 50 -worst 50 -retime path_slew_propagation > $report_dir/pba_hold.rpt
#exit[
```

### Violations Report:

```
#####
# Generated by: Cadence Tempus 20.10-p003.1
# OS: Linux x86_64 (Host ID edaserver4)
# Generated on: Wed Apr 17 11:59:20 2024
# Design: mesh
# Command: report_constraints -all_violators > ../sta_after_dft/sta_timing/allviolations.rpt
#####
# format : frame 0 : split 1
#
max_delay/setup
-----
No paths found
min_delay/hold
-----
End Point Slack Cause
-----
g r3_output2_reg[17]/SE f -0.196 VIOLATED
r3_output2_reg[16]/SE f -0.196 VIOLATED
r3_output2_reg[15]/SE f -0.196 VIOLATED
r3_output2_reg[14]/SE f -0.196 VIOLATED
r3_output2_reg[13]/SE f -0.196 VIOLATED
r3_output2_reg[12]/SE f -0.196 VIOLATED
r3_output2_reg[11]/SE f -0.196 VIOLATED
r3_output2_reg[10]/SE f -0.196 VIOLATED
r3_output2_reg[9]/SE f -0.196 VIOLATED
r3_output2_reg[8]/SE f -0.196 VIOLATED
r3_output2_reg[7]/SE f -0.196 VIOLATED
r3_output2_reg[6]/SE f -0.196 VIOLATED
r3_output2_reg[5]/SE f -0.196 VIOLATED
r3_output2_reg[4]/SE f -0.196 VIOLATED
r3_output2_reg[3]/SE f -0.196 VIOLATED
r3_output2_reg[2]/SE f -0.196 VIOLATED
r3_output2_reg[1]/SE f -0.196 VIOLATED
r3_output2_reg[0]/SE f -0.196 VIOLATED
r2_output2_reg[17]/SE f -0.196 VIOLATED
r2_output2_reg[16]/SE f -0.196 VIOLATED
r2_output2_reg[15]/SE f -0.196 VIOLATED
r2_output2_reg[14]/SE f -0.196 VIOLATED
r2_output2_reg[13]/SE f -0.196 VIOLATED
r2_output2_reg[12]/SE f -0.196 VIOLATED
r2_output2_reg[11]/SE f -0.196 VIOLATED
r2_output2_reg[10]/SE f -0.196 VIOLATED
r2_output2_reg[9]/SE f -0.196 VIOLATED
r2_output2_reg[8]/SE f -0.196 VIOLATED
r2_output2_reg[7]/SE f -0.196 VIOLATED
r2_output2_reg[6]/SE f -0.196 VIOLATED
r2_output2_reg[5]/SE f -0.196 VIOLATED
r2_output2_reg[4]/SE f -0.196 VIOLATED
```

```

m0/R1 control_signals2_reg[9]/SE f      -0.196  VIOLATED
m0/R1 control_signals2_reg[8]/SE f      -0.196  VIOLATED
m0/R1 control_signals2_reg[7]/SE f      -0.196  VIOLATED
m0/R1 control_signals2_reg[6]/SE f      -0.196  VIOLATED
m0/R1 control_signals2_req[5]/SE f      -0.196  VIOLATED
m0/R1 control_signals2_req[4]/SE f      -0.196  VIOLATED
m0/R1 control_signals2_req[2]/SE f      -0.196  VIOLATED
m0/R1 control_signals2_req[1]/SE f      -0.196  VIOLATED
m0/R1 control_signals2_req[0]/SE f      -0.196  VIOLATED
m0/R0 control_signals2_req[19]/SE f     -0.196  VIOLATED
m0/R0 control_signals2_req[18]/SE f     -0.196  VIOLATED
m0/R0 control_signals2_req[17]/SE f     -0.196  VIOLATED
m0/R0 control_signals2_req[16]/SE f     -0.196  VIOLATED
m0/R0 control_signals2_req[15]/SE f     -0.196  VIOLATED
m0/R0 control_signals2_req[14]/SE f     -0.196  VIOLATED
m0/R0 control_signals2_req[13]/SE f     -0.196  VIOLATED
m0/R0 control_signals2_req[12]/SE f     -0.196  VIOLATED
m0/R0 control_signals2_req[11]/SE f     -0.196  VIOLATED
m0/R0 control_signals2_req[10]/SE f     -0.196  VIOLATED
m0/R0 control_signals2_req[9]/SE f      -0.196  VIOLATED
m0/R0 control_signals2_req[8]/SE f      -0.196  VIOLATED
m0/R0 control_signals2_req[7]/SE f      -0.196  VIOLATED
m0/R0 control_signals2_req[6]/SE f      -0.196  VIOLATED
m0/R0 control_signals2_req[5]/SE f      -0.196  VIOLATED
m0/R0 control_signals2_req[4]/SE f      -0.196  VIOLATED
m0/R0 control_signals2_req[2]/SE f      -0.196  VIOLATED
m0/R0 control_signals2_req[0]/SE f      -0.196  VIOLATED
block_all_paths/reg[5] f              -0.196  VIOLATED

-----
Check type : clock_period
-----
No paths found

Check type : skew
-----
No paths found

Check type : pulse_width
-----
No violating Checks with given description found

Check type : max_transition
-----
No Violations found

Check type : min_transition
-----
No Violations found

```

## Timing Reports:

### GBA Path

#### Setup Slack

```

#####
# Generated by:   Cadence Tempus 20.10-p083.1
# OS:             Linux x86_64 (Host ID edserver4)
# Generated on:  Wed Apr 17 11:59:20 2024
# Design:        reg
# Command:       report timing -late > $report_dir/timing/report_setup.rpt
#####
Path 1: MET Recovery Check with Pin m0/R0_control_signals2_req[0]/CK
Endpoint: m0/R0_control_signals2_req[0]/RM (*) checked with leading edge of 'clk'
Beginpoint: reset (V) triggered by leading edge of 'clk'
Path Groups: (async_default)
Other End Arrival Time    6.018
- Recovery                0.000
+ Propag. Delays          3.668
= Uncertainty              6.018
- Required Time            2.984
- Arrival Time             1.265
= Slack Time               1.738
Clock Rise Edge           0.000
+ Input Delay              0.040
+ Network Insertion Delay  0.010
= Beginpoint Arrival Time  0.050
Instance          Arc      Cell      Delay  Arrival  Required
                           Time    Time    Time
- m0/g7217      reset: V  -      0.050  1.768
                         A V -> Y ~  INVXL  1.215  1.265  2.984
                         RN ~  SOFFMOX1  0.460  1.265  2.984

```

#### Hold Slack

```

#####
# Generated by: Cadence Tempus 20.10-p003_1
# OS: Linux x86_64(Host ID edaserver4)
# Generated on: Wed Apr 17 11:59:28 2024
# Design: me
# Command: report_timing -early > $report_dir/timing/report_hold.rpt
#####
Path 1: VIOLATED Hold Check with Pin m0/R0 control_signals2_reg[0]/OK
Endpoint: m0/R0 control_signals2_reg[0]/SE (v) checked with leading edge of 'clk'
Beginpoint: scan_en (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Other End Arrival Time 0.010
+ Hold 0.226
+ Phase Shift 0.000
+ Uncertainty 0.010
= Required Time 0.246
Arrival Time 0.050
Slack Time -0.196
    Clock Rise Edge 0.000
    Input Delay 0.040
    + Network Insertion Delay 0.010
    = Beginpoint Arrival Time 0.050
-----
Instance Arc Cell Delay Arrival Required
Time Time Time
-----+
* scan_en v SE V SDFFRHQXL 0.000 0.050 0.246
-----+

```

### **Slack Computation (worst path):**

Tclk = 3.68ns, Recovery = 0.696ns , Beginpoint:reset, Endpoint : m0/R0\_control\_signals2\_reg[0]

**Required Time:** The data must reach the next flip-flop ‘setup time’ before the next clock edge arrives. Since Tclk= 3.68ns, we have an uncertainty of 0.010ns. In the worst case for setup analysis, the clock can only come after 3.67ns. However, we have a delay of 0.010 ns too. This delay and uncertainty cancel, leaving us with 3.68 ns as the time to the next clock edge. The recovery time of a flip-flop is 0.696ns. Hence, we want our data to be available within 2.984 ns (3.68-0.696) from when the current clock edge has arrived.

### **Arrival Time:**

This is the time our data took to reach the input pin of the flip-flop. The tool estimates it to be 1.265ns. We wanted our data to come before 2.984 ns, which came at 1.265 ns only. This implies our constraint is met, and we don’t have a violation.

### **Slack Time:**

$$\text{Slack} = \text{Required Time} - \text{Arrival Time} = 2.984 - 1.265 = 1.718\text{ns}$$

In the STA after DFT, in the case of graph-based analysis, the slack time is 0.730 ns. This implies our constraint is met, and we don’t have a violation.

### **Hold case:**

BeginPoint : scan\_en, Endpoint: m0/R0\_control\_signals2\_reg[0]

**Required Time:** Other End Arrival time(+ 0.010ns) + Hold time (+ 0.226ns) + Uncertainty(+0.010) = 0.246ns

**Arrival Time:** This is the time our data took to reach the input pin of the flip-flop. The tool estimates it to be 0.050ns. We wanted our data to come before 0.246 ns, which came at 3.089 ns only. This implies our constraint is not met, and we have a violation.

**Slack:** AT-RT = -0.196ns

PBA Path

*Setup Slack*

```

timing_report_setup.rpt  timing_report_hold.rpt  pba_setup.rpt
#####
# Generated by: Cadence Tempus 20.10-p003
# OS: Linux #86_64[Host ID edaserver4]
# Generated on: Wed Apr 17 11:59:28 2024
# Design: netlist
# Command:
#       report timing -max paths 50 -mworst 50 -retime path_slew_propagation > $report_dir/pba_setup.rpt
#####
Path 1: MET Recovery Check with Pin m0/R3 control_signals2_reg[14]/CK
Endpoint: m0/R3_control_signals2_reg[14]/RN (^) checked with 'leading edge of 'clk'
Beginpoint: reset (v) triggered by 'leading edge of 'clk'
Path Groups: {async default}
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.010
- Recovery 0.095
+ Phase Shift 3.680
- Uncertainty 0.010
= Required Time 2.984
- Arrival Time 1.265
= Slack Time 1.718
= Slack Time(original) 1.718
    Clock Rise Edge 0.000
    + Input Delay 0.040
    + Network Insertion Delay 0.010
    = Beginpoint Arrival Time 0.050
-----
Instance Arc Cell Retime Arrival Required
-----  

- reset v 0.050 1.268
m0/g7217 INVXL 0.000 0.000 1.706
m0/g7217 A V -> Y ^ INVXL 1.215 1.265 2.984
m0/R3_control_signals2_reg[14] - SDFFRHDX1 0.000 1.265 2.984
-----
Path 2: MET Recovery Check with Pin m0/R3 control_signals2_reg[13]/CK
Endpoint: m0/R3_control_signals2_reg[13]/RN (^) checked with 'leading edge of 'clk'
Beginpoint: reset (v) triggered by 'leading edge of 'clk'
Path Groups: {async default}
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.010
- Recovery 0.095
+ Phase Shift 3.680
- Uncertainty 0.010
= Required Time 2.984
- Arrival Time 1.265
= Slack Time 1.718
= Slack Time(original) 1.718
    Clock Rise Edge 0.000
    + Input Delay 0.040
    + Network Insertion Delay 0.010
    = Beginpoint Arrival Time 0.050

```

## Hold Slack

```
#####
# Generated by: Cadence Tempus 20.1b-p031
# OS: Linux x86_64 (Host ID edaserver4)
# Generated on: Wed Apr 17 11:59:20 2024
# Design: mesh
# Command: report_timing -early -max_path 50 -worst 50 -retime path_slew_propagation > $report_dir/pba_hold.rpt
#####
Path 1: VIOLATED Hold Check with Pin m0/R2_control_signals2_reg[14]/CK
Endpoint: m0/R2_control_signals2_reg[14]/SE (v) checked with leading edge of 'clk'
Beginpoint: scan_en (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.018
+ Hold 0.226
+ Phase Shift 0.000
+ Uncertainty 0.018
= Required Time 0.246
Arrival Time 0.058
Slack Time -0.196
= Slack Time(original) -0.196
Clock Rise Edge 0.000
+ Input Delay 0.040
+ Network Insertion Delay 0.010
= Beginpoint Arrival Time 0.050
-----
Instance Arc cell Retime Delay Arrival Required Time
-----  

scan_en v - 0.050 0.246  

m0/R2_control_signals2_reg[14] SDFFRM0X1 0.000 0.050 0.246
-----
Path 2: VIOLATED Hold Check with Pin m0/R2_control_signals2_reg[13]/SE (v) checked with leading edge of 'clk'
Endpoint: m0/R2_control_signals2_reg[13]/SE (v) checked with leading edge of 'clk'
Beginpoint: scan_en (v) triggered by leading edge of 'clk'
Path Groups: {clk}
Retime Analysis { Data Path-Slew }
Other End Arrival Time 0.016
+ Hold 0.226
+ Phase Shift 0.000
+ Uncertainty 0.018
= Required Time 0.246
Arrival Time 0.058
Slack Time -0.196
= Slack Time(original) -0.196
Clock Rise Edge 0.000
+ Input Delay 0.040
+ Network Insertion Delay 0.010
= Beginpoint Arrival Time 0.050
-----
Instance Arc cell Retime Delay Arrival Required Time
-----  


```

## Slack Computation (worst path):

Tclk = 3.68ns, Recovery time = 0.696ns , Begin point : reset, End point : m0/R3\_control\_signals2\_reg[14]

**Required Time:** The data must reach the next flip-flop ‘setup time’ before the next clock edge arrives. Since Tclk= 3.68ns, we have an uncertainty of 0.010ns. In the worst case for setup analysis, the clock can only come after 3.67ns. However, we have a delay of 0.010 ns too. This delay and uncertainty cancel, leaving us with 3.68 ns as the time to the next clock edge. The setup time of a flip-flop is 0.090ns. Hence, we want our data to be available within 2.984ns (3.68-0.696) from when the current clock edge has arrived.

### Arrival Time:

This is the time our data took to reach the input pin of the flip-flop. The tool estimates it to be 1.265 ns. We wanted our data to come before 2.984 ns, which came at 1.265 ns only. This implies our constraint is met, and we don’t have a violation.

### Slack Time:

Slack = Required Time - Arrival Time = 2.984 - 1.265 = 1.718ns.

In the STA after DFT, in the case of graph-based analysis, the slack time is 1.718ns, and in the case of path-based analysis, the slack time is 1.718ns.

The graph-based analysis is a more pessimistic way to calculate the slack time, while path-based analysis gives the actual slack time, which should be greater than or equal to the slack time from the graph-based analysis.

However, GBA and PBA give the same slack as reported in this case.

### Hold case:

BeginPoint : scan\_en, Endpoint: m0/R0\_control\_signals2\_reg[14]

**Required Time:** Other End Arrival time(+ 0.010ns) + Hold time (+ 0.226ns) + Uncertainty(+0.010) = 0.246ns

**Arrival Time:** This is the time our data took to reach the input pin of the flip-flop. The tool estimates it to be 0.050ns. We wanted our data to come before 0.246 ns, which came at 3.089 ns only. This implies our constraint is met, and we have a violation.

**Slack:** AT-RT = -0.196 ns

The graph-based analysis is a more pessimistic way to calculate the slack time, while path-based analysis gives the actual slack time, which should be greater than or equal to the slack time from the graph-based analysis.

The slack in the GBA and PBA analysis is equal in this case.

### Area Report:

Instance	Module	Cell Count	Cell Area	Net Area	Total Area	Wireload
mesh		2567	22784.729	0.000	22784.729	<none> (D)
m0	master	1095	6618.334	0.000	6618.334	<none> (D)
r1	router_355	229	1999.730	0.000	1999.730	<none> (D)
r0	router	232	1971.725	0.000	1971.725	<none> (D)
r3	router_353	228	1963.399	0.000	1963.399	<none> (D)
r2	router_354	228	1962.642	0.000	1962.642	<none> (D)
inc_p3_add_175_41_increment_unsigned_162		16	74.933	0.000	74.933	<none> (D)
inc_p2_add_175_41_increment_unsigned_142		16	74.933	0.000	74.933	<none> (D)
inc_p1_add_175_41_increment_unsigned_122		16	74.933	0.000	74.933	<none> (D)
inc_p0_add_175_41_increment_unsigned_102		16	74.933	0.000	74.933	<none> (D)

(D) = wireload is default in technology library

Area of standard cells : 22704.729  $\mu\text{m}^2$

Area of Buffers : 0.000  $\mu m^2$

Area of Inverters :  $659.260 \mu\text{m}^2$

Area of Combinational: 8786.095  $\mu\text{m}^2$

Area of flip-flops :  $13201.850 \mu\text{m}^2$  (SDFFHQX1 + SDFFQX1)

## Power Report:

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	1.69463e-04	4.68477e-03	1.86614e-03	6.72037e-03	77.87%
latch	8.64028e-07	6.89691e-07	7.24677e-08	1.62679e-06	0.02%
logic	7.40387e-05	1.02206e-03	4.89412e-04	1.57651e-03	18.27%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	3.31270e-04	3.31270e-04	3.84%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	2.44366e-04	5.70752e-03	2.67789e-03	8.62978e-03	100.00%
Percentage	2.83%	66.14%	31.03%	100.00%	100.00%

In this report, internal power is the power dissipated inside the cell boundary during the charging and discharging of existing capacitances. Total Internal Power is 5.707 mW.

Switching power of driving cell is the power dissipated by charging load capacitance at the output. The total switching power is 2.677 mW.

Leakage power is generated from the leakage current that flows between VDD and GND when there is no switching. The total leakage power is 0.244 mW

The total power which is the sum of all these is 8.629 mW.

## 2. After Placement

After placement, we will now continue our physical design process from netlist by doing floor planning, CTS, routing and finally GDS

Inputs:

.io file, gsclib090\_translated\_ref.lef, fast.lib file, constraints file, synthesized netlist

The io file defines the different pins of the circuit in particular direction. The direction of the pins are as follows: Inputs in North (N), Outputs in South (S), Clocks and reset in East (E) and Scan chain in West (W)

The LEF file contains design information for our 90nm design

View file contains the delay corners, constraints netlist that will be used.

Software Used:

Cadence Innovus

Commands Used:

1. csh
2. source /cadence/cshrc
3. Innovus
4. source (tcl file)

We have done floor planning for core utilisation 0.5 and 0.8 by modifying the DoFloorPlan.tcl script.

```
#!/usr/bin/csh
getIoFlowFlag
setIoFlowFlag 0
floorPlan -site gsclib090site -r 1 0.5 4.06 4.06 4.06 4.06
```

In the script, 1 is the aspect ratio (width to height), 0.5 is the core utilisation and 4.06 is the boundary area on each side.

After floor planning, we will do power planning by defining our VDD and GND levels for both 0.5 core utilisation and 0.8 core utilisation by modifying our DoFloorPlan.tcl script.

We have used metal 8 and 9 from top to bottom and left to right respectively because of their relatively lower resistance to form rings and nets.

```
#Power Planning/
#Adding Rings/
addRing -skip_via on wire shape Noshape -skip_via on pin Standardcell -center 1 -stacked_via_top_layer Metal9 -type core_rings -jog_distance 0.435 -threshold 0.435 -nets {GND VDD} -follow core -
stacked_via_bottom_layer Metal11 -layer {bottom Metal8 top Metal8 right Metal9 left Metal9} -width 1.25 -spacing 0.4 -offset 0.435
```

In the script width of lines is 1.25 with spacing of 0.4 between the rails.

## Layout Design Core Utilization:- 0.5

TCL file:

### 1. DesignInit.tcl

```
set init_gnd net GND
# Create file IO
set init_io_file /home/rajat21186/Desktop/New_VDF_Project/Physical_Design/iopadplacement.io
set init_lef_file /home/rajat21186/Desktop/New_VDF_Project/library/gsclib090_translated_ref.lef
# Create View File
set init_mmmc_file /home/rajat21186/Desktop/New_VDF_Project/Physical_Design/mesh.view
set init_pwr_net VDD
set init_top_cell mesh
# After DFT
set init_verilog /home/rajat21186/Desktop/New_VDF_Project/DFT_Results/main_optimal/synthesised_netlist.v
|
init_design
```

### 2. DoFloorPlan.tcl

```
#loopPlanning/
getDfFlag
setDfFlag 0
floorPlan -site gsclib090@site -r 1 0.5 4.06 4.06 4.06 4.06

# Change to 0.8
#Power Planning/
#Adding Rings/
addRing -skip_via on wire shape Noshape -skip_via on pin Standardcell -center 1 -stacked_via_top_layer Metal9 -type core_rings -jog_distance 0.435 -threshold 0.435 -nets {GND VDD} -follow core -
stacked_via_bottom_layer Metal11 -layer {bottom Metal8 top Metal8 right Metal9 left Metal9} -width 1.25 -spacing 0.4 -offset 0.435

# Add extra command
specifyScanChain test s11 -start DFT_sdl_1 -stop DFT_sdo_1
specifyScanChain test s12 -start DFT_sdl_2 -stop DFT_sdo_2
# VDD & GND Rings on Squares
#Adding Stripes/
addStripe -skip_via on wire shape Noshape -block_ring_top_layer_limit Metal9 -max_same_layer_jog_length 0.88 -padcore_ring_bottom_layer_limit Metal7 -number_of_sets 10 -skip_via_on_pin Standardcell -
stacked_via_top_layer Metal9 -padcore_ring_top_layer_limit Metal9 -spacing 0.4 -merge_stripes_value 0.435 -layer Metal8 -block_ring_bottom_layer_limit Metal7 -width 0.44 -nets {VDD GND} -
stacked_via_bottom_layer Metal

#Placement/
setPlaceMode -fp false
placeDesign
optDesign -preCTS
#Power Analysis/
set power_analysis_mode -reset
set_power_analysis_node -method static -analysis_view view1 -corner max -create_binary_db true -write_static_currents true -honor_negative_energy true -ignore_control_signals true
set_power_output_dir -reset
set_power_output_dir ../Physical_Design_scripts/PostPlacementPowerRpt
set default_switching_activity -reset
set default_switching_activity -input_activity 0.2 -period 10.0
read_activity_file -reset
set_power -reset
set_powerup_analysis -reset

set dynamic_power_simulation -reset
report_power -rail_analysis_format VS -outfile ../Physical_Design_scripts/PostPlacementPowerRpt/rtl_module_post_placement.rpt

# Area
summaryReport -outdir ../Physical_Design_scripts/postPlaceArea -noHTML
report_area -detail -show_leaf_cells -table_style (vertical)
setAnalysisNode -checkType setup
report_timing -check_type setup > ../Physical_Design_scripts/TimingReports/setup_analysis_after_placement.rpt
```

```

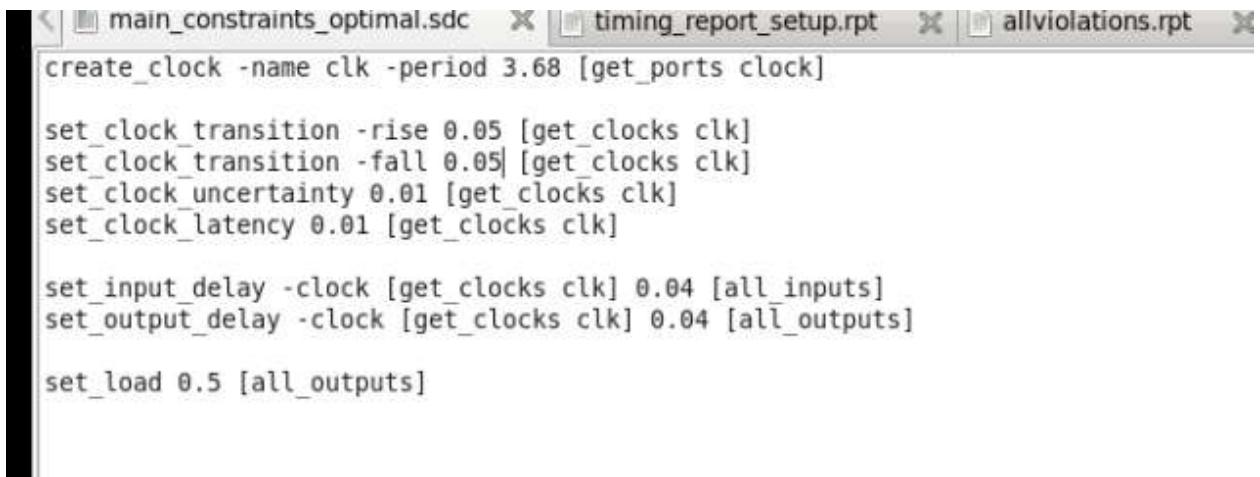
set_dynamic_power_simulation -reset
report_power -rail_analysis_format VS -outfile ..../Physical_Design_scripts/PostPlacementPowerRpt/rtl_module_post_placement.rpt

# Area
summaryReport -outdir ..../Physical_Design_scripts/postPlaceArea -noHtml
report area -detail -show_leaf_cells -table_style {vertical}
setAnalysisMode -checkType setup
report_timing -check_type setup > ..../Physical_Design_scripts/TimingReports/setup_analysis_after_placement.rpt

setAnalysisMode -checkType hold
report_timing -check_type hold > ..../Physical_Design_scripts/TimingReports/hold_analysis_after_placement.rpt
report area > ..../Physical Design scripts/postPlaceArea/Area_report.rpt

```

Constraints used:



```

create_clock -name clk -period 3.68 [get_ports clock]

set_clock_transition -rise 0.05 [get_clocks clk]
set_clock_transition -fall 0.05 [get_clocks clk]
set_clock_uncertainty 0.01 [get_clocks clk]
set_clock_latency 0.01 [get_clocks clk]

set_input_delay -clock [get_clocks clk] 0.04 [all_inputs]
set_output_delay -clock [get_clocks clk] 0.04 [all_outputs]

set_load 0.5 [all_outputs]

```

Timing Reports:

Setup Analysis:-

```

DesignInit.tcl mesh.view DoFloorPlan.tcl DoCTS.tcl setup_analysis_after_placement.rpt
#####
# Generated by: Cadence Innovus 20.10-p004.1
# OS: Linux x86_64(Host ID edaserver4)
# Generated on: Wed Apr 17 12:11:12 2024
# Design: new
# Command: report timing -check type setup > ../../Physical_Design_scripts/TimingReports/setup_analysis_after_placement.rpt
#####
Path 1: MET Setup Check with Pin m0/R2_control_signals2_reg[13]/D
Endpoint: m0/R2_control_signals2_reg[13]/D (-) checked with leading edge of
'clk'
Beginpoint: reset (v) triggered by leading edge of
'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time 0.010
- Setup 0.126
+ Phase Shift 3.680
Uncertainty 0.010
= Required Time 3.554
Arrival Time 3.530
= Slack Time 0.024
Clock Rise Edge 0.000
+ Input Delay 0.040
+ Network Insertion Delay 0.010
= Beginpoint Arrival Time 0.050
+-----+
| Instance | Arc | Cell | Delay | Arrival Time | Required Time |
+-----+
| reset v | A v -> Y ^ | INVX1 | 0.405 | 0.455 | 0.479 |
| FE_OFCl2_FE_DBTN0_reset g551 | A ^ -> Y ^ | BUFX2 | 0.365 | 0.821 | 0.844 |
| m0/g18096 | A ^ -> Y ^ | AND2X1 | 0.312 | 1.132 | 1.156 |
| m0/g18970 | B ^ -> Y ^ | OR2X1 | 0.312 | 1.266 | 1.284 |
| m0/g18614 | A ^ -> Y v | CLKINVX1 | 0.289 | 1.469 | 1.493 |
| m0/g18467 | BB v -> Y ^ | AO121X1 | 0.157 | 1.626 | 1.650 |
| m0/g18432 | BB v -> Y ^ | OA21X1 | 0.069 | 1.694 | 1.718 |
| m0/g18376 | BB v -> Y ^ | CLKINVX1 | 0.012 | 1.786 | 1.730 |
| m0/g18307 | A1 ^ -> Y v | AO1221X1 | 0.046 | 1.751 | 1.775 |
| m0/g18293 | BB v -> Y ^ | AO121X1 | 0.055 | 1.841 | 1.865 |
| m0/g18292 | A ^ -> Y ^ | AND4X2 | 0.385 | 2.146 | 2.176 |
| m0/g18256 | A ^ -> Y v | CLKINVX1 | 0.289 | 2.358 | 2.374 |
| m0/g18235 | A1 v -> Y ^ | OA21X1 | 0.185 | 2.467 | 2.497 |
| m0/g18228 | C0 ^ -> Y v | AO1221X1 | 0.053 | 2.589 | 2.533 |
| m0/g18225 | BB v -> Y v | NAND2X1 | 0.035 | 2.559 | 2.582 |
| m0/g18224 | D ^ -> Y ^ | OR4X2 | 0.115 | 2.674 | 2.697 |
| m0/FE_OFCl8_n_B16 | A ^ -> Y v | CLKINVX2 | 0.117 | 2.798 | 2.814 |
| m0/g18185 | A1 v -> Y ^ | AO121X1 | 0.075 | 2.866 | 2.889 |
| m0/g18163 | AIN ^ -> Y ^ | AO12BB1X1 | 0.04 | 2.908 | 2.932 |
| m0/g18154 | C0 ^ -> Y v | AO121X1 | 0.032 | 2.941 | 2.964 |
| m0/g18153 | BB v -> Y v | AO121X1 | 0.052 | 2.997 | 3.016 |
| m0/g18152 | AN ^ -> Y v | NOR4X1 | 0.065 | 3.057 | 3.081 |
| m0/FE_OFCl4_n_25 | A ^ -> Y ^ | BUFX2 | 0.235 | 3.291 | 3.315 |
| m0/g18151 | A ^ -> Y v | CLKINVX2 | 0.118 | 3.410 | 3.433 |
| m0/g18148 | BB v -> Y ^ | AO121X1 | 0.068 | 3.478 | 3.502 |
| m0/g18100 | BB v -> Y v | AO121X1 | 0.015 | 3.493 | 3.516 |
| m0/g18055 | BB v -> Y ^ | AO121X1 | 0.037 | 3.530 | 3.554 |
| m0/R2_control_signals2_reg[13] | D ^ -> Y v | SDFFRH0X1 | 0.008 | 3.538 | 3.554 |

```

```

Analysis View: view1
Other End Arrival Time 0.010
- Setup 0.126
+ Phase Shift 3.680
Uncertainty 0.010
= Required Time 3.554
Arrival Time 3.530
= Slack Time 0.024
Clock Rise Edge 0.000
+ Input Delay 0.040
+ Network Insertion Delay 0.010
= Beginpoint Arrival Time 0.050
+-----+
| Instance | Arc | Cell | Delay | Arrival Time | Required Time |
+-----+
| reset v | A v -> Y ^ | INVX1 | 0.405 | 0.455 | 0.479 |
| FE_OFCl2_FE_DBTN0_reset g551 | A ^ -> Y ^ | BUFX2 | 0.365 | 0.821 | 0.844 |
| m0/g18096 | A ^ -> Y ^ | AND2X1 | 0.312 | 1.132 | 1.156 |
| m0/g18970 | B ^ -> Y ^ | OR2X1 | 0.312 | 1.266 | 1.284 |
| m0/g18614 | A ^ -> Y v | CLKINVX1 | 0.289 | 1.469 | 1.493 |
| m0/g18467 | BB v -> Y ^ | AO121X1 | 0.157 | 1.626 | 1.650 |
| m0/g18432 | BB v -> Y ^ | OA21X1 | 0.069 | 1.694 | 1.718 |
| m0/g18376 | BB v -> Y ^ | CLKINVX1 | 0.012 | 1.786 | 1.730 |
| m0/g18307 | A1 ^ -> Y v | AO1221X1 | 0.046 | 1.751 | 1.775 |
| m0/g18293 | BB v -> Y ^ | AO121X1 | 0.055 | 1.841 | 1.865 |
| m0/g18292 | A ^ -> Y ^ | AND4X2 | 0.385 | 2.146 | 2.176 |
| m0/g18256 | A ^ -> Y v | CLKINVX1 | 0.289 | 2.358 | 2.374 |
| m0/g18235 | A1 v -> Y ^ | OA21X1 | 0.185 | 2.467 | 2.497 |
| m0/g18228 | C0 ^ -> Y v | AO1221X1 | 0.053 | 2.589 | 2.533 |
| m0/g18225 | BB v -> Y v | NAND2X1 | 0.035 | 2.559 | 2.582 |
| m0/g18224 | D ^ -> Y ^ | OR4X2 | 0.115 | 2.674 | 2.697 |
| m0/FE_OFCl8_n_B16 | A ^ -> Y v | CLKINVX2 | 0.117 | 2.798 | 2.814 |
| m0/g18185 | A1 v -> Y ^ | AO121X1 | 0.075 | 2.866 | 2.889 |
| m0/g18163 | AIN ^ -> Y ^ | AO12BB1X1 | 0.04 | 2.908 | 2.932 |
| m0/g18154 | C0 ^ -> Y v | AO121X1 | 0.032 | 2.941 | 2.964 |
| m0/g18153 | BB v -> Y v | AO121X1 | 0.052 | 2.997 | 3.016 |
| m0/g18152 | AN ^ -> Y v | NOR4X1 | 0.065 | 3.057 | 3.081 |
| m0/FE_OFCl4_n_25 | A ^ -> Y ^ | BUFX2 | 0.235 | 3.291 | 3.315 |
| m0/g18151 | A ^ -> Y v | CLKINVX2 | 0.118 | 3.410 | 3.433 |
| m0/g18148 | BB v -> Y ^ | AO121X1 | 0.068 | 3.478 | 3.502 |
| m0/g18100 | BB v -> Y v | AO121X1 | 0.015 | 3.493 | 3.516 |
| m0/g18055 | BB v -> Y ^ | AO121X1 | 0.037 | 3.530 | 3.554 |
| m0/R2_control_signals2_reg[13] | D ^ -> Y v | SDFFRH0X1 | 0.008 | 3.538 | 3.554 |

```

In this timing report it shows the critical path of all the paths present in the circuit. The critical path starts from reset and ends at m0/R2\_control\_signals2\_reg[13] /D that is at the D pin of the Flip Flop.

### Arrival Time Computation:-

Starting from the already computed arrival time (other end arrival time) 0.050 ns at beginpoint reset and traversing to the end point through different cells with experiencing different delays are added up. So subsequent vertices arrival time is calculated by adding up the already computed arrival time. Finally, from the above timing report we can infer that AT at the end point is 3.530 ns.

#### Required Time Computation:-

Here in the above timing report RT is computed as other end arrival time (0.050 ns) + Phase Shift (3.68ns , clock period) – setup (0.126 ns, time required by the clock to setup) - uncertainty (0.010 ns). Required Time (RT) at the endpoint evaluates to 3.554 ns.

Slack = Required Time - Arrival Time = 0.024 ns.

#### Hold Analysis:-

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64(Host ID: edaserver4)
# Generated on: Wed Apr 17 12:11:12 2024
# Design: mesh
# Command: report_timing -check_type hold > ../../Physical_Design_Scripts/TimingReports/hold_analysis_after_placement.rpt
#####
Path 1: MET Hold Check with Pin p0_configure1_reg[0]/CK
Endpoint: p0_configure1_reg[0]/D ('') checked with leading edge of 'clk'
Beginpoint: p0_configure[0] ('') triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time      0.050
+ Hold                      0.008
+ Phase Shift                0.000
+ Uncertainty                0.010
= Required Time              0.028
Arrival Time                 0.050
Slack Time                  0.022
  Clock Rise Edge           0.000
  + Input Delay              0.040
  + Network Insertion Delay  0.010
  = Beginpoint Arrival Time  0.050
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|-----+-----+-----+-----+-----+-----+
| p0_configure1_reg[0] | p0_configure[0] ^ | SDFFQX1 | 0.000 | 0.050 | 0.028 |
+-----+
```

In this timing report it shows the critical path of all the paths present in the circuit. The critical path starts from p0\_configure[0] and ends at p0\_configure1\_reg[0] / D that is at the D pin of the Flip Flop.

#### Arrival Time Computation:-

Starting from the already computed arrival time (other end arrival time) 0.050 ns at beginpoint reset and traversing to the end point through different cells with experiencing different delays

are added up. So subsequent vertices arrival time is calculated by adding up the already computed arrival time. Finally, from the above timing report we can infer that AT at the end point is 0.050 ns. In this case the path is from p0\_configure[0] to p0\_configure1\_reg[0] / D which is the D pin of the first flop SDFFQX1.

#### Required Time Computation:-

Here in the above timing report RT is computed as other end arrival time (0.010 ns). clock + hold (0.008 ns, time required by the clock to setup) + uncertainty (0.010 ns). Required Time (RT) at the endpoint evaluates to 0.028 ns.

$$\text{Slack} = \text{Arrival Time} - \text{Required Time} = 0.050 - 0.028 = 0.022\text{ns.}$$

#### Power Report:

```

Innovus 20.10-p004.1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)

Date & Time: 2024-Apr-17 12:11:11 (2024-Apr-17 06:41:11 GMT)

-----
Design: mesh
Liberty Libraries used:
    view1: /home/rajat21106/Desktop/New_VDF_Project/library/fast.lib
Power Domain used:
Power View : view1
User-Defined Activity : N.A.
Activity File: N.A.
Hierarchical Global Activity: N.A.
Global Activity: N.A.
Sequential Element Activity: N.A.
Primary Input Activity: 0.200000
Default icg ratio: N.A.
Global Comb ClockGate Ratio: N.A.
Power Units = 1mW
Time Units = 1e-09 secs
Temperature = 0
report_power -outfile ../Physical_Design_scripts/PostPlacementPowerRpt/rtl_module_post_placement.rpt -rall_analysis_format vs

Cell          Internal      Switching      Total      Leakage      Cell
          Power       Power       Power       Power      Name
-----
r3_output2_reg[17]  0.82216  0.1683  | 0.1909  0.0004846  SDFFQX4
p3_data_got1_reg[0]  0.01812  0.08528  0.1037  0.0002999  SDFFQX2
p3_data_got1_reg[2]  0.01813  0.08521  0.1036  0.0002999  SDFFQX2
p3_data_got1_reg[1]  0.01799  0.0851  0.1034  0.0002999  SDFFQX2
p3_data_got1_req[3]  0.018  0.08509  0.1034  0.0002999  SDFFQX2

```

p0_data_got1_reg[8]	0.018	0.00444	0.1827	0.0002999	SDFFOX2
p2_data_got1_reg[2]	0.01821	0.00415	0.1827	0.0002999	SDFFOX2
p0_data_got1_reg[6]	0.01804	0.00421	0.1826	0.0002999	SDFFOX2
p1_data_got1_reg[11]	0.01819	0.00462	0.1825	0.0002999	SDFFOX2
p1_data_got1_reg[7]	0.01821	0.00388	0.1824	0.0002999	SDFFOX2
p0_data_got1_reg[4]	0.01804	0.00403	0.1824	0.0002999	SDFFOX2
p0_data_got1_reg[5]	0.01807	0.00391	0.1823	0.0002999	SDFFOX2
p0_data_got1_reg[2]	0.01815	0.00382	0.1823	0.0002999	SDFFOX2
p2_data_got1_reg[4]	0.01821	0.00374	0.1822	0.0002999	SDFFOX2
p0_data_got1_reg[3]	0.01821	0.00372	0.1822	0.0002999	SDFFOX2
p2_data_got1_reg[0]	0.0182	0.00371	0.1822	0.0002999	SDFFOX2
p1_data_got1_reg[0]	0.0182	0.00367	0.1822	0.0002999	SDFFOX2
p2_data_got1_reg[5]	0.01823	0.00386	0.1821	0.0002999	SDFFOX2
p2_data_got1_reg[8]	0.01804	0.00372	0.1821	0.0002999	SDFFOX2
p1_data_got1_reg[3]	0.01817	0.00358	0.1821	0.0002999	SDFFOX2
r3_output2_reg[15]	0.01797	0.00378	0.1802	0.0002999	SDFFOX2
p0_data_got1_reg[1]	0.01824	0.00385	0.1802	0.0002999	SDFFOX2
r0_output2_reg[17]	0.01818	0.00349	0.1802	0.0002999	SDFFOX2
p1_data_got1_reg[6]	0.01821	0.00344	0.1802	0.0002999	SDFFOX2
p2_data_got1_reg[3]	0.01821	0.00343	0.1819	0.0002999	SDFFOX2
r0_output2_reg[15]	0.01816	0.00347	0.1819	0.0002999	SDFFOX2
p3_data_got1_reg[6]	0.01822	0.00384	0.1819	0.0002999	SDFFOX2
r3_output2_reg[14]	0.01796	0.00365	0.1819	0.0002999	SDFFOX2
r1_output2_reg[9]	0.01814	0.00345	0.1819	0.0002999	SDFFOX2
p0_data_got1_reg[0]	0.01821	0.00338	0.1819	0.0002999	SDFFOX2
p3_data_got1_reg[7]	0.01825	0.00333	0.1819	0.0002999	SDFFOX2
r2_output2_reg[6]	0.01799	0.00359	0.1819	0.0002999	SDFFOX2
p1_data_got1_reg[4]	0.0182	0.00338	0.1819	0.0002999	SDFFOX2
p1_data_got1_reg[2]	0.0182	0.00337	0.1819	0.0002999	SDFFOX2
p2_data_got1_reg[7]	0.01822	0.00337	0.1819	0.0002999	SDFFOX2
r0_output2_reg[16]	0.01817	0.00339	0.1819	0.0002999	SDFFOX2
r3_output2_reg[9]	0.01792	0.00361	0.1818	0.0002999	SDFFOX2
p1_data_got1_reg[5]	0.01822	0.00333	0.1818	0.0002999	SDFFOX2
r3_output2_reg[16]	0.01796	0.00356	0.1818	0.0002999	SDFFOX2
r0_output2_reg[6]	0.01797	0.00353	0.1818	0.0002999	SDFFOX2
r3_output2_reg[11]	0.01794	0.00354	0.1818	0.0002999	SDFFOX2
r1_output2_reg[5]	0.01812	0.00336	0.1818	0.0002999	SDFFOX2
r3_output2_reg[12]	0.01792	0.00354	0.1818	0.0002999	SDFFOX2
p2_data_got1_reg[6]	0.01822	0.00324	0.1818	0.0002999	SDFFOX2
r0_output2_reg[8]	0.01814	0.00333	0.1817	0.0002999	SDFFOX2
r3_output2_reg[7]	0.01785	0.00358	0.1817	0.0002999	SDFFOX2
r1_output2_reg[13]	0.01796	0.00347	0.1817	0.0002999	SDFFOX2
r2_output2_reg[4]	0.01796	0.00347	0.1817	0.0002999	SDFFOX2
p3_data_got1_reg[8]	0.0181	0.00331	0.1817	0.0002999	SDFFOX2
r0_output2_reg[7]	0.01799	0.00342	0.1817	0.0002999	SDFFOX2
r3_output2_reg[10]	0.01795	0.00346	0.1817	0.0002999	SDFFOX2
r1_output2_reg[6]	0.01799	0.00339	0.1817	0.0002999	SDFFOX2
p2_data_got1_reg[1]	0.01812	0.00317	0.1817	0.0002999	SDFFOX2
r2_output2_reg[7]	0.01795	0.00341	0.1817	0.0002999	SDFFOX2
r2_output2_reg[11]	0.01916	0.00319	0.1816	0.0002888	SDFFOX2

r2_output2	reg[6]	0.01799	0.08359	0.1019	0.0002999	SDFF0X2
p1_data	got1.reg[4]	0.0182	0.08338	0.1019	0.0002999	SDFF0X2
p1_data	got1.reg[2]	0.0182	0.08337	0.1019	0.0002999	SDFF0X2
p2_data	got1.reg[7]	0.01821	0.08337	0.1019	0.0002999	SDFF0X2
r0_output2	reg[16]	0.01817	0.08339	0.1019	0.0002999	SDFF0X2
r3_output2	reg[9]	0.01792	0.08361	0.1018	0.0002999	SDFF0X2
p1_data	got1.reg[5]	0.01822	0.08333	0.1018	0.0002999	SDFF0X2
r3_output2	reg[16]	0.01796	0.08356	0.1018	0.0002999	SDFF0X2
r0_output2	reg[6]	0.01797	0.08353	0.1018	0.0002999	SDFF0X2
r2_output2	reg[11]	0.01794	0.08354	0.1018	0.0002999	SDFF0X2
r1_output2	reg[5]	0.01812	0.08336	0.1018	0.0002999	SDFF0X2
r3_output2	reg[12]	0.01792	0.08354	0.1018	0.0002999	SDFF0X2
p2_data	got1.reg[6]	0.01822	0.08324	0.1018	0.0002999	SDFF0X2
r0_output2	reg[8]	0.01814	0.08333	0.1017	0.0002999	SDFF0X2
r3_output2	reg[7]	0.01785	0.08358	0.1017	0.0002999	SDFF0X2
r1_output2	reg[13]	0.01796	0.08347	0.1017	0.0002999	SDFF0X2
r2_output2	reg[4]	0.01796	0.08347	0.1017	0.0002999	SDFF0X2
p3_data	got1.reg[8]	0.0181	0.08331	0.1017	0.0002999	SDFF0X2
r0_output2	reg[7]	0.01799	0.08342	0.1017	0.0002999	SDFF0X2
r3_output2	reg[10]	0.01795	0.08346	0.1017	0.0002999	SDFF0X2
r1_output2	reg[0]	0.01799	0.08339	0.1017	0.0002999	SDFF0X2
p2_data	got1.reg[1]	0.0182	0.08317	0.1017	0.0002999	SDFF0X2
r2_output2	reg[7]	0.01795	0.08341	0.1017	0.0002999	SDFF0X2
r0_output2	reg[14]	0.01816	0.08318	0.1018	0.0002999	SDFF0X2
r2_output2	reg[10]	0.01789	0.08342	0.1018	0.0002999	SDFF0X2
r2_output2	reg[12]	0.01794	0.08337	0.1018	0.0002999	SDFF0X2
r2_output2	reg[0]	0.01795	0.08335	0.1018	0.0002999	SDFF0X2
r1_output2	reg[10]	0.01796	0.08333	0.1018	0.0002999	SDFF0X2
r3_output2	reg[0]	0.01763	0.08366	0.1016	0.0002999	SDFF0X2
r1_output2	reg[6]	0.01797	0.08331	0.1016	0.0002999	SDFF0X2
p1_data	got1.reg[8]	0.01782	0.08345	0.1016	0.0002999	SDFF0X2
r0_output2	reg[13]	0.01798	0.08329	0.1016	0.0002999	SDFF0X2
r1_output2	reg[11]	0.01799	0.08327	0.1016	0.0002999	SDFF0X2
r1_output2	reg[14]	0.01796	0.08328	0.1015	0.0002999	SDFF0X2
r0_output2	reg[5]	0.01801	0.08319	0.1015	0.0002999	SDFF0X2
r2_output2	reg[16]	0.01797	0.08322	0.1015	0.0002999	SDFF0X2
r2_output2	reg[17]	0.01799	0.08318	0.1015	0.0002999	SDFF0X2
r0_output2	reg[3]	0.01784	0.08332	0.1015	0.0002999	SDFF0X2
r0_output2	reg[4]	0.01797	0.08319	0.1015	0.0002999	SDFF0X2
r1_output2	reg[8]	0.01798	0.08318	0.1015	0.0002999	SDFF0X2
r3_output2	reg[11]	0.01781	0.08335	0.1015	0.0002999	SDFF0X2
r3_output2	reg[6]	0.01781	0.08334	0.1015	0.0002999	SDFF0X2
r2_output2	reg[13]	0.0179	0.08325	0.1014	0.0002999	SDFF0X2
r2_output2	reg[14]	0.01795	0.08322	0.1014	0.0002999	SDFF0X2
r0_output2	reg[10]	0.01795	0.08318	0.1014	0.0002999	SDFF0X2
r1_output2	reg[4]	0.018	0.08313	0.1014	0.0002999	SDFF0X2
r2_output2	reg[5]	0.01784	0.08329	0.1014	0.0002999	SDFF0X2
r2_output2	reg[3]	0.01795	0.08317	0.1014	0.0002999	SDFF0X2
r3_output2	reg[2]	0.01783	0.08329	0.1014	0.0002999	SDFF0X2

r1/regR_req	0.01605	0.002655	0.01898	0.000258	SDFFSHDX1
p2/last_prev_req	0.01387	0.004725	0.01898	0.0002688	SDFFRMNX1
r3/regR_req	0.01598	0.002639	0.01884	0.0002688	SDFFSHDX1
m0/R1 control signals2_reg[12]	0.01522	0.003333	0.01882	0.0002688	SDFFRMNX1
p0/data_to_router1_reg[2]	0.01368	0.003625	0.01878	0.0002688	SDFFRMNX1
p0/data_to_router1_reg[2]	0.01237	0.004747	0.01872	0.0002688	SDFFRMNX1
p0/last_prev_req	0.01469	0.003632	0.01859	0.0002688	SDFFRMNX1
m0/R2 control signals2_reg[17]	0.01237	0.005902	0.01854	0.0002688	SDFFRMNX1
p0/data_to_router1_reg[3]	0.01464	0.003558	0.01847	0.0002688	SDFFRMNX1
p0/data_to_router1_reg[6]	0.01339	0.004285	0.01845	0.0002688	SDFFRMNX1
m0/R3 control signals2_reg[17]	0.01462	0.003471	0.01836	0.0002688	SDFFRNQX1
p3/data_to_router1_reg[0]	0.0143	0.003795	0.01833	0.0002688	SDFFRMNX1
p2/data_to_router1_reg[4]	0.01474	0.003259	0.01828	0.0002688	SDFFRMNX1
m0/R1 control signals2_reg[9]	0.01445	0.003474	0.01819	0.0002688	SDFFRMNX1
p1/data_to_router1_reg[0]	0.01369	0.003699	0.01817	0.0002688	SDFFRMNX1
m0/R2 control signals2_reg[12]	0.01415	0.003317	0.01793	0.0002688	SDFFRMNX1
m0/R2 control signals2_reg[11]	0.01413	0.003212	0.01792	0.0002688	SDFFRMNX1
p2/counter_value_req[1]	0.01526	0.002335	0.01786	0.0002688	SDFFRMNX1
p2/data_to_router1_reg[3]	0.01418	0.003358	0.01781	0.0002688	SDFFRMNX1
p3/data_to_router1_reg[6]	0.01419	0.003394	0.01777	0.0002688	SDFFRMNX1
p3/data_to_router1_reg[7]	0.01451	0.002936	0.01771	0.0002688	SDFFRMNX1
p1/data_to_router1_reg[6]	0.01483	0.003494	0.01777	0.0002688	SDFFRMNX1
r3/output_west2_reg[2]	0.01360	0.004082	0.01737	0.0002575	SDFFOX1
r3/output_west2_reg[1]	0.01360	0.004082	0.01737	0.0002575	SDFFOX1
p0/data_to_router1_reg[2]	0.01375	0.003347	0.01731	0.0002568	SDFFRMNX1
p0/data_to_router1_reg[9]	0.01385	0.003849	0.01729	0.0002688	SDFFRMNX1
m0/R2 control signals2_reg[16]	0.01411	0.002889	0.01727	0.0002688	SDFFRMNX1
m0/R1 control signals2_reg[8]	0.01579	0.001183	0.01724	0.0002688	SDFFRMNX1
r3/output_processor2_reg[7]	0.01405	0.002934	0.01724	0.0002575	SDFFOX1
p3/data_to_router1_reg[5]	0.01419	0.002777	0.01724	0.0002688	SDFFRMNX1
r3/output_south2_reg[6]	0.01338	0.003563	0.01712	0.0002575	SDFFOX1
r1/output_processor2_reg[5]	0.01441	0.002479	0.01714	0.0002575	SDFFOX1
m0/R1 control signals2_reg[4]	0.01582	0.001027	0.01712	0.0002688	SDFFRMNX1
r3/output_south2_reg[3]	0.01274	0.004117	0.01711	0.0002575	SDFFOX1
m0/R2 control signals2_reg[10]	0.01404	0.002903	0.01708	0.0002575	SDFFRMNX1
r2/output_processor2_reg[2]	0.01382	0.003093	0.01708	0.0002575	SDFFOX1
p0/data_to_router1_reg[7]	0.01365	0.003097	0.01702	0.0002688	SDFFRMNX1
r1/output_north2_reg[8]	0.01332	0.003411	0.01699	0.0002575	SDFFOX1
p3/data_to_router1_reg[1]	0.0136	0.003095	0.01697	0.0002688	SDFFRMNX1
p3/data_to_router1_reg[3]	0.01381	0.002882	0.01698	0.0002688	SDFFRMNX1
p0/counter_value_req[8]	0.01345	0.003283	0.01692	0.0002688	SDFFRMNX1
p0/data_to_router1_reg[1]	0.01407	0.002568	0.01691	0.0002688	SDFFRMNX1
r1/output_north2_reg[7]	0.01321	0.003434	0.01691	0.0002575	SDFFOX1
r3/output_processor2_reg[6]	0.01382	0.002903	0.01687	0.0002575	SDFFOX1
p0/counter_value_req[1]	0.01447	0.003897	0.01684	0.0002688	SDFFRMNX1
p0/counter_value_req[4]	0.01394	0.002463	0.01667	0.0002688	SDFFRMNX1
p3/data_to_router1_reg[4]	0.01382	0.002558	0.01665	0.0002688	SDFFRMNX1
m0/R2 control signals2_reg[3]	0.01553	0.0068261	0.01662	0.0002688	SDFFRMNX1
r3/output_west2_reg[5]	0.01245	0.003987	0.01662	0.0002575	SDFFOX1
m3/last_prev_rm	0.013	0.002795	0.01662	0.0002688	SDFFRMNX1

m0/g18127	8.845e-05	2.188e-05	0.0001312	2.087e-05	OAI211XL
m0/g18121	8.999e-05	2.01e-05	0.000131	2.087e-05	OAI211XL
r1/g1102	7.945e-05	3.03e-05	0.0001308	2.097e-05	NAND2XL
m0/g18122	8.804e-05	2.161e-05	0.0001305	2.087e-05	OAI211XL
m0/g18124	8.918e-05	2.041e-05	0.0001305	2.087e-05	OAI211XL
m0/g18118	8.747e-05	2.21e-05	0.0001304	2.087e-05	OAI211XL
m0/g18135	8.951e-05	1.895e-05	0.0001293	2.087e-05	OAI211XL
m0/g18146	6.347e-05	4.202e-05	0.0001265	2.097e-05	NAND2XL
m0/g18642	3.193e-05	7.159e-05	0.0001245	2.097e-05	NAND2XL
r1/g1111	7.48e-05	2.769e-05	0.0001235	2.097e-05	NAND2XL
m0/g18691	7.676e-05	2.534e-05	0.000123	2.085e-05	OAI21XL
m0/g18145	7.582e-05	2.613e-05	0.0001229	2.097e-05	NAND2XL
m0/g18643	4.622e-05	3.785e-05	0.0001194	3.532e-05	NOR2XL
m0/g18641	3.72e-05	4.572e-05	0.0001182	3.532e-05	NOR2XL
m0/g18438	6.22e-05	3.278e-05	0.0001116	2.097e-05	NAND2XL
m0/g18439	6.817e-05	2.676e-05	0.0001159	2.097e-05	NAND2XL
m0/g18440	5.86e-05	2.531e-05	0.0001049	2.097e-05	NAND2XL
m0/g18624	5.82e-05	2.5e-05	0.0001041	2.085e-05	OAI21XL
g1105	5.094e-05	3.068e-05	0.0001026	2.103e-05	NAND4XL
m0/g18644	2.67e-05	3.982e-05	0.0001018	3.532e-05	NOR2XL
m0/g18636	2.01e-05	5.768e-05	9.875e-05	2.097e-05	NAND2XL
g1103	4.567e-05	2.657e-05	9.326e-05	2.103e-05	NAND4XL
g1098	3.261e-05	2.241e-05	9.034e-05	3.532e-05	NOR2XL
g1097	3.099e-05	1.507e-05	8.138e-05	3.532e-05	NOR2XL
m0/g18645	1.459e-05	4.446e-05	8.003e-05	2.097e-05	NAND2XL
inc_p2_add_175_41/g93	1.871e-05	2.386e-05	7.789e-05	3.532e-05	NOR2XL
m0/g18653	2.105e-05	3.548e-05	7.75e-05	2.097e-05	NAND2XL
m0/g18165	1.718e-05	1.634e-05	6.266e-05	2.914e-05	OAI221X1
inc_p0_add_175_41/g88	1.162e-05	2.744e-05	6.004e-05	2.097e-05	NAND2XL
g1096	1.498e-05	6.801e-06	5.71e-05	3.532e-05	NOR2XL
m0/g18655	8.54e-06	8.952e-06	5.281e-05	3.532e-05	NOR2XL
m0/g18646	1.199e-05	1.57e-05	4.867e-05	2.097e-05	NAND2XL
m0/g18648	5.373e-06	4.249e-06	4.494e-05	3.532e-05	NOR2XL
m0/g18647	6.749e-06	1.566e-05	4.338e-05	2.097e-05	NAND2XL
g1095	4.708e-06	2.843e-06	4.287e-05	3.532e-05	NOR2XL
m0/g19241	9.103e-06	3.95e-06	4.234e-05	2.928e-05	OAI21X1
inc_p3_add_175_41/g88	5.715e-06	1.296e-05	3.965e-05	2.097e-05	NAND2XL
inc_p1_add_175_41/g88	5.777e-06	1.276e-05	3.951e-05	2.097e-05	NAND2XL
m0/g18238	6.263e-06	2.446e-06	3.787e-05	2.914e-05	OAI221X1
m0/g18073	2.356e-06	4.845e-06	3.659e-05	2.939e-05	OAI211XL
m0/g19242	4.479e-06	1.556e-06	3.532e-05	2.928e-05	OAI21X1
m0/g19240	2.133e-06	4.674e-07	3.188e-05	2.928e-05	OAI21X1
inc_p2_add_175_41/g88	1.964e-06	4.666e-06	2.76e-05	2.097e-05	NAND2XL
m0/g18144	8.137e-07	3.578e-07	2.215e-05	2.097e-05	NAND2XL

```
Total ( 2579 of 2579 )      9.541    11.59    21.36    0.2295
Total Capacitance          9.005E-11 F
Power Density               *** No Die Area ***

```

Dhveirat Dacian errint

The report is too big to incorporate into the report

In this report, internal power is the power dissipated inside the cell boundary during charging and discharging of existing capacitances. Total Internal Power is 9.541mW

Switching power of driving cell is the power dissipated by charging load capacitance at the output. The total switching power is 11.59mW

Leakage power is generated from the leakage current that flows between VDD and GND when there is no switching. The total leakage power is 0.2295mW

The total power which is the sum of all these is 21.36mW

## Area Report:

General Design Information			
Design Status: Routed			
Design Name: mesh			
# Instances: 2578			
# Hard Macros: 0			
# Std Cells: 2578			
Standard Cells in Netlist			
Cell Type	Instance Count	Area (um^2)	
OA12BBLXL	11	58.2813	
AO122XL	31	187.7112	
OR2XL	1	4.5414	
AO12BBXL	2	12.1104	
NAND4XL	1	6.8121	
BUF2X2	16	72.6624	
CLK0X0R2XL	9	74.9331	
TLMXN0	4	57.5244	
OR2XI	7	31.7898	
AO12BB1XL	3	18.1656	
AND2XI	37	168.0318	
AO133XL	4	39.2766	
OA1211XL	122	646.3926	
SDF0X1	297	6069.5811	
XNOR2XL	4	33.3036	
MK2XL	13	88.5573	
AND2XL	12	54.4968	
XOR2XL	11	91.5849	
OA1222XL	171	1423.7289	
OA121X3	89	404.1846	
OA1221XL	71	537.3990	
OA131XL	2	12.1104	
OA21X3	15	102.1815	
CLKINVX1	221	501.8247	
AO1211XL	24	127.1592	
NAND2BX1	24	108.9936	
OA1211XL	140	741.7620	
OA22X1	1	7.5696	
XNOR2XL	4	33.3036	

XNOR2XL	4	33.3036
NAND3XL	15	68.1210
NAND2XL	328	993.6528
SDFFRHQX1	149	3721.6773
OA21XL	1	6.8121
ADDHX1	4	48.4416
NOR2BX1	22	99.9198
OA122XL	3	18.1656
OA121XL	24	108.9936
A0121X1	105	476.8470
NOR3BX1	40	242.2080
A01221X1	15	113.5350
A0131X1	10	60.5520
NAND3BX1	8	48.4416
A0121X1	2	13.0242
OA1221XL	5	37.8450
NOR3XL	35	158.9490
NOR4BX1	1	6.8121
OR4X2	1	8.3259
AO22XL	1	7.5690
NOR4X1	4	24.2208
A01211XL	2	10.5966
AND4X4	1	9.6397
SDFFSHQX1	13	354.2292
INVX1	50	113.5350
OA122XL	1	6.8552
NOR2XL	144	435.9744
SDFFQX4	1	24.9777
OA133XL	2	16.6518
CLKINVX2	2	7.5690
SDFFQX2	111	2436.4611
A0122X1	48	290.6496
OA132XL	5	34.6605
NOR3XL	4	18.1656
A0121XL	14	63.5796
A0132X1	21	143.6541
OA12B1XL	2	10.5966
OA1221XL	1	7.5690
NAND4XL	37	190.6371

```
# Pads: 0
# Net: 2747
# Special Net: 2
# Tq Pins:
```

```
=====
Flooring/Placement Information
=====
Total area of Standard cells: 22155.220 um^2
Total area of Standard cells(Subtracting Physical Cells): 22155.220 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 45429.099 um^2
Total area of Chip: 48957.095 um^2
Effective Utilization: 4.8760e-01
Number of Cell Rows: 81
% Pure Gate Density #1 (Subtracting BLOCKAGES): 48.768%
% Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 48.768%
% Pure Gate Density #3 (Subtracting MACROS): 48.768%
% Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 48.768%
% Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 48.768%
% Pure Gate Density #6 (Counting Std Cells and MACROS): 48.768%
Core Density (Counting Std Cells and MACROS): 48.768%
Core Density #2(Subtracting Physical Cells): 48.768%
Chip Density (Counting Std Cells and MACROS and IOs): 45.254%
Chip Density #2(Subtracting Physical Cells): 45.254%
# Macros within 5 sites of IO pad: No
Macro halo defined?: No

=====
Wire Length Distribution
=====
Total Metal1 wire length: 6.0000 um
Total Metal2 wire length: 36786.2850 um
Total Metal3 wire length: 33931.6500 um
Total Metal4 wire length: 15926.1100 um
Total Metal5 wire length: 3985.9050 um
Total Metal6 wire length: 545.2700 um
Total Metal7 wire length: 0.0000 um
Total Metal8 wire length: 0.0000 um
Total Metal9 wire length: 0.0000 um
```

Hinst Name Gate	Module Name Macro	Inst Count Physical	Total Area	Buffer	Inverter	Combinational	Flop	Latch	Clock
mesh		2579	22155.220	72.662	627.470	8798.637	12606.926	57.524	
0.000	0.000	0.000							
inc p0_add_175_41	increment_unsigned_162	16	74.933	0.000	4.541	70.392	0.000	0.000	
0.000	0.000	0.000							
inc p1_add_175_41	increment_unsigned_122	16	74.933	0.000	4.541	70.392	0.000	0.000	
0.000	0.000	0.000							
inc p2_add_175_41	increment_unsigned_142	16	74.933	0.000	4.541	70.392	0.000	0.000	
0.000	0.000	0.000							
inc p3_add_175_41	increment_unsigned_162	16	74.933	0.000	4.541	70.392	0.000	0.000	
0.000	0.000	0.000							
n0	master	1098	6346.606	9.083	359.528	4854.713	1923.293	0.000	
0.000	0.000	0.000							
r1	inverter	231	1969.454	0.000	63.588	904.495	1001.379	0.000	
0.000	0.000	0.000							
r1	router_355	228	1997.459	0.000	56.767	912.065	1028.627	0.000	
0.000	0.000	0.000							
r2	router_354	227	1960.371	0.000	54.497	904.495	1001.379	0.000	
0.000	0.000	0.000							
r3	router_353	227	1961.128	0.000	54.497	905.252	1001.379	0.000	
0.000	0.000	0.000							

Area of standard cells :  $22155.220 \mu\text{m}^2$

Area of Buffers :  $72.664 \mu\text{m}^2$

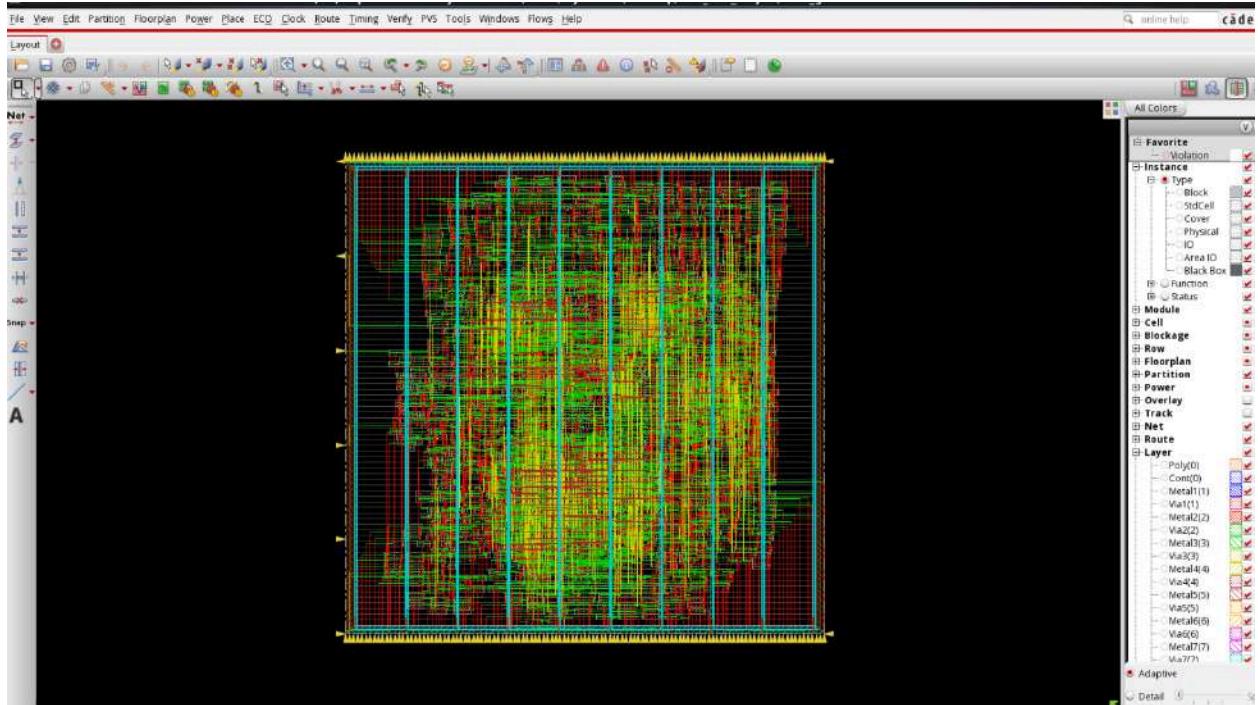
Area of Inverters :  $627.470 \mu\text{m}^2$

Area of Combinational:  $8798.637 \mu\text{m}^2$

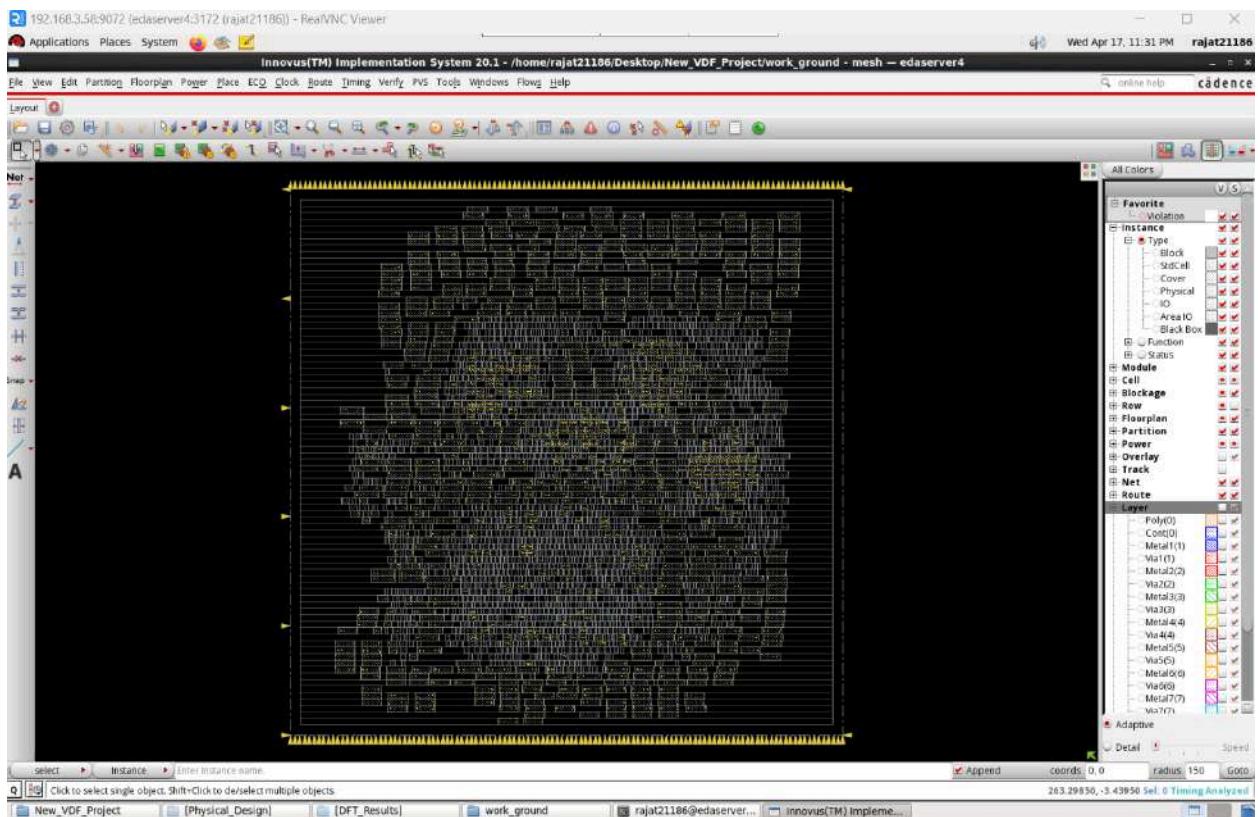
Area of flip-flops :  $12606.926 \mu\text{m}^2$  (SDFFHQX1 + SDFFQX1)

Snap-shot of layout of design and connectivity showing Fly-Lines:

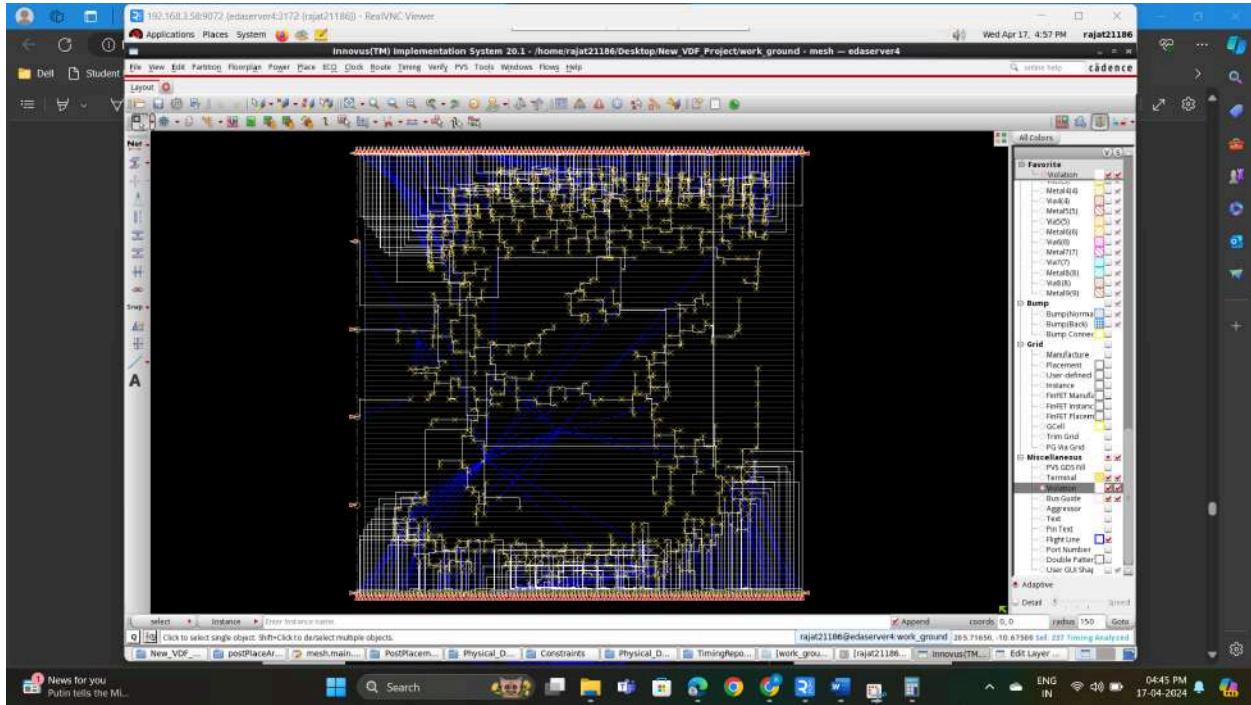
## Layout after Placement:



## Standard Cells after Placement:



## Flight Lines:



Layout Design Core Utilization:- 0.8

TCL file:

### 1. DesignInit.tcl

```
set init_gnd net GND
# Create file IO
set init_io_file /home/rajat21186/Desktop/New_VDF_Project/Physical_Design/iopadplacement.io
set init_lef_file /home/rajat21186/Desktop/New_VDF_Project/library/gsclib090_translated_ref.lef
# Create View File
set init_mmc_file /home/rajat21186/Desktop/New_VDF_Project/Physical_Design/mesh.view
set init_pwr_net VDD
set init_top_cell mesh
# After DFT
set init_verilog /home/rajat21186/Desktop/New_VDF_Project/DFT_Results/main_optimal/synthesised_netlist.v
init_design
```

### 2. DoFloorPlan.tcl

```

D:\FloorPlan_2.tcl :c |
#/Floorplanning/
getFloorFlag
setFloorFlag 0
floorPlan -site gscelib090site -r 1 0.0 4.06 4.06 4.06 4.06

# Change to 0.8

#/Power Planning/
#Adding Rings/
addingRing -skip_via_on_wire shape Noshape -skip_via_on_pin Standardcell -center 1 -stacked_via_top_layer Metal9 -type core rings -jog_distance 0.435 -threshold 0.435 -nets {GND VDD} -follow core -
stacked_via_bottom_layer Metal1 -layer (bottom Metal8 top Metal9 left Metal9) -width 1.25 -spacing 0.4 -offset 0.435

# Add extra command
specifyScanChain test_sil_1 -start DFT_sdi_1 -stop DFT_sdo_1
specifyScanChain test_sil_2 -start DFT_sdi_2 -stop DFT_sdo_2
# VDD & GND Rings on Squares
#Adding Stripes/
addStripe -skip_via_on_wire shape Noshape -block_ring_top_layer_limit Metal9 -max_same_layer_jog_length 0.88 -padcore_ring_bottom_layer_limit Metal7 -number_of_sets 10 -skip_via_on_pin Standardcell -
stacked_via_top_layer Metal9 -padcore_ring_top_layer_limit Metal9 -spacing 0.4 -merge_stripes_value 0.435 -layer Metal8 -block_ring_bottom_layer_limit Metal7 -width 0.44 -nets {VDD GND} -
stacked_via_bottom_layer Metal1

#/Placement/
setPlaceMode -fp false
placeDesign

optDesign -preCTS

#/Power Analysis/
set power_analysis_mode -reset
set power_analysis_mode -method static -analysis_view view1 -corner max -create_binary_db true -write_static_currents true -honor_negative_energy true -ignore_control_signals true
set power_output_dir -reset
set power_output_dir ../Physical_Design_Scripts2/PostPlacementPowerRpt
set default_switching_activity -reset
set default_switching_activity -input_activity 0.2 -period 10.0
read_activity_file -reset
set power -reset
set_powerup_analysis -reset

set dynamic_power_simulation -reset
report_power -rail_analysis_format VS -outfile ..\Physical_Design_Scripts2\PostPlacementPowerRpt/rtl_module_post_placement.rpt

# Area
summaryReport -outdir ..\Physical_Design_Scripts2/postPlaceArea -noHTML
report_area -detail -show_leaf_cells -table_style {vertical}
setAnalysisMode -checkType setup
report_timing -check_type setup > ..\Physical_Design_Scripts2/TimingReports/setup_analysis_after_placement.rpt

set dynamic_power_simulation -reset
report_power -rail_analysis_format VS -outfile ..\Physical_Design_scripts/PostPlacementPowerRpt/rtl_module_post_placement.rpt

# Area
summaryReport -outdir ..\Physical_Design scripts/postPlaceArea -noHTML
report_area -detail -show_leaf_cells -table_style {vertical}
setAnalysisMode -checkType setup
report_timing -check_type setup > ..\Physical_Design scripts/TimingReports/setup_analysis_after_placement.rpt

setAnalysisMode -checkType hold
report_timing -check type hold > ..\Physical_Design scripts/TimingReports/hold_analysis_after_placement.rpt
report area > ..\Physical Design scripts/postPlaceArea/Area report.rpt

```

Constraints used:

```

main_constraints_optimal.sdc  X timing_report_setup.rpt  X allviolations.rpt  X
create_clock -name clk -period 3.68 [get_ports clock]

set_clock_transition -rise 0.05 [get_clocks clk]
set_clock_transition -fall 0.05 [get_clocks clk]
set_clock_uncertainty 0.01 [get_clocks clk]
set_clock_latency 0.01 [get_clocks clk]

set_input_delay -clock [get_clocks clk] 0.04 [all_inputs]
set_output_delay -clock [get_clocks clk] 0.04 [all_outputs]

set_load 0.5 [all_outputs]

```

Timing Reports:

Setup Analysis:-

```

#####
# Generated by: Cadence Innovus 28.10-0004.1
# OS: Linux x86_64(Most IO edaserver4)
# Generated on: Wed Apr 17 17:48:23 2024
# Design: mesh
# Command: report timing -check type setup > ../../Physical_Design_Scripts2/TimingReports/setup_analysis_after_placement.rpt
#####
Path 1: MET Setup Check with Pin m0/R3_control_signals2_reg[1]/D
Endpoint: m0/R3_control_signals2_reg[1]/D (*) checked with leading edge of
`clk`
Beginpoint: p0_configure1_reg[0]/Q      (*) triggered by leading edge of
`clk`
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time    0.010
- Setup          0.122
+ Phase Shift   3.688
- Uncertainty   0.018
= Required Time 3.558
- Arrival Time   3.527
= Slack Time    0.031
Clock Rise Edge  0.000
+ Clock Network Latency (Ideal) 0.010
= Beginpoint Arrival Time 0.010
+-----+
| Instance        | Arc           | Cell          | Delay | Arrival Time | Required Time |
+-----+
| p0_configure1_reg[0] | CK ^          | SDFFQX1       | 0.090 | 0.010 | 0.041 |
| p0_configure1_reg[0] | CK ^ -> Q ^  | NOR2XL        | 0.140 | 0.120 | 0.122 |
| q465               | A ^ -> Y v    | CLKINVX1       | 0.640 | 0.140 | 0.122 |
| g551               | C ^ -> Y v    | NOR2XL        | 0.354 | 0.494 | 0.525 |
| m0/FE_DBTC14_P0_signals_1 | A ^ -> Y v    | INVXL         | 0.371 | 0.865 | 0.356 |
| m0/g15886          | B v -> Y ^    | NAND2XL       | 0.460 | 1.325 | 1.356 |
| m0/g15828          | A ^ -> Y v    | CLKINVX1       | 0.231 | 1.555 | 1.587 |
| m0/g15326          | B0 v -> Y ^   | AOI21X1       | 0.090 | 1.645 | 1.676 |
| m0/g15238          | B ^ -> Y v    | NAND2XL       | 0.031 | 1.676 | 1.707 |
| m0/g15866          | A0 v -> Y ^   | AOI21X1       | 0.036 | 1.712 | 1.743 |
| m0/g15942          | B ^ -> Y v    | NAND2XL       | 0.624 | 1.735 | 1.766 |
| m0/g15919          | A v -> Y ^    | NOR2XL        | 0.118 | 1.851 | 1.882 |
| m0/g15918          | A ^ -> Y v    | NAND3X4       | 0.187 | 2.038 | 2.069 |
| m0/fopt16569        | A v -> Y ^    | CLKINVX1       | 0.537 | 2.575 | 2.596 |
| m0/g14934          | A1 v -> Y v   | INVXL         | 0.371 | 2.611 | 2.642 |
| m0/g14889          | A1 v -> Y v   | OAI21X1       | 0.066 | 2.709 | 2.738 |
| m0/g14875          | B ^ -> Y v    | NOR2XL        | 0.630 | 2.789 | 2.748 |
| m0/g14871          | B v -> Y ^    | NAND2XL       | 0.637 | 2.746 | 2.777 |
| m0/g14870          | B ^ -> Y v    | NAND2XL       | 0.036 | 2.746 | 2.777 |
| m0/FE_OFCl4_n_968  | A ^ -> Y ^    | BUFX2         | 0.320 | 3.066 | 3.097 |
| m0/g14761          | A1 ^ -> Y v   | OAI21X1       | -0.000 | 3.066 | 3.097 |
| m0/g14729          | B v -> Y ^    | NAND2BXL     | 0.047 | 3.113 | 3.144 |
| m0/g14708          | A ^ -> Y v    | NAND3X1       | 0.028 | 3.133 | 3.164 |
+-----+

```

setup\_analysis\_after\_placement.rpt (~/Desktop/New\_VDF\_Project/Physical\_Design\_Scripts2/)

```

#####
# MET SETUP LIVENESS MAIN PATH m0/R3_control_signals2_reg[1]/D
Endpoint: m0/R3_control_signals2_reg[1]/D (*) checked with leading edge of
`clk`
Beginpoint: p0_configure1_reg[0]/Q      (*) triggered by leading edge of
`clk`
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time    0.010
- Setup          0.122
+ Phase Shift   3.688
- Uncertainty   0.018
= Required Time 3.558
- Arrival Time   3.527
= Slack Time    0.031
Clock Rise Edge  0.000
+ Clock Network Latency (Ideal) 0.010
= Beginpoint Arrival Time 0.010
+-----+
| Instance        | Arc           | Cell          | Delay | Arrival Time | Required Time |
+-----+
| p0_configure1_reg[0] | CK ^          | SDFFQX1       | 0.090 | 0.010 | 0.041 |
| p0_configure1_reg[0] | CK ^ -> Q ^  | NOR2XL        | 0.140 | 0.120 | 0.122 |
| q465               | A ^ -> Y v    | CLKINVX1       | 0.640 | 0.140 | 0.122 |
| g551               | C ^ -> Y v    | NOR2XL        | 0.354 | 0.494 | 0.525 |
| m0/FE_DBTC14_P0_signals_1 | A ^ -> Y v    | INVXL         | 0.371 | 0.865 | 0.356 |
| m0/g15886          | B v -> Y ^    | NAND2XL       | 0.460 | 1.325 | 1.356 |
| m0/g15828          | A ^ -> Y v    | CLKINVX1       | 0.231 | 1.555 | 1.587 |
| m0/g15326          | B0 v -> Y ^   | AOI21X1       | 0.090 | 1.645 | 1.676 |
| m0/g15238          | B ^ -> Y v    | NAND2XL       | 0.031 | 1.676 | 1.707 |
| m0/g15866          | A0 v -> Y ^   | AOI21X1       | 0.036 | 1.712 | 1.743 |
| m0/g15942          | B ^ -> Y v    | NAND2XL       | 0.624 | 1.735 | 1.766 |
| m0/g15919          | A v -> Y ^    | NOR2XL        | 0.118 | 1.851 | 1.882 |
| m0/g15918          | A ^ -> Y v    | NAND3X4       | 0.187 | 2.038 | 2.069 |
| m0/fopt16569        | A v -> Y ^    | CLKINVX1       | 0.537 | 2.575 | 2.596 |
| m0/g14934          | A1 v -> Y v   | INVXL         | 0.371 | 2.611 | 2.642 |
| m0/g14889          | A1 v -> Y v   | OAI21X1       | 0.066 | 2.709 | 2.738 |
| m0/g14875          | B ^ -> Y v    | NOR2XL        | 0.630 | 2.789 | 2.748 |
| m0/g14871          | B v -> Y ^    | NAND2XL       | 0.637 | 2.746 | 2.777 |
| m0/FE_OFCl4_n_968  | A ^ -> Y ^    | BUFX2         | 0.320 | 3.066 | 3.097 |
| m0/g14761          | A1 ^ -> Y v   | OAI21X1       | -0.000 | 3.066 | 3.097 |
| m0/g14729          | B v -> Y ^    | NAND2BXL     | 0.047 | 3.113 | 3.144 |
| m0/g14788          | A ^ -> Y v    | NAND3X1       | 0.028 | 3.133 | 3.164 |
| m0/g14704          | B v -> Y ^    | NOR2XL        | 0.940 | 3.173 | 3.204 |
| m0/g14782          | A ^ -> Y ^    | AND2X4        | 0.144 | 3.317 | 3.348 |
| m0/g14701          | A ^ -> Y v    | CLKINVX4       | 0.106 | 3.423 | 3.454 |
| m0/g14597          | A1 v -> Y ^   | OAI21X1       | 0.103 | 3.526 | 3.558 |
| m0/R3_control_signals2_reg[1] | D ^          | SDPFRRQX1     | 0.960 | 3.527 | 3.558 |
+-----+

```

In this timing report it shows the critical path of all the paths present in the circuit. The critical path starts from p0\_configure1\_reg[0]/Q and ends at m0/R3\_control\_signals2\_reg[1] /D that is at the D pin of the Flip Flop.

### Arrival Time Computation:-

Starting from the already computed arrival time (other end arrival time) 0.010 ns at beginpoint and traversing to the end point through different cells with experiencing different delays are added up. So subsequent vertices arrival time is calculated by adding up the already computed arrival time. Finally, from the above timing report we can infer that AT at the end point is 3.527 ns.

#### Required Time Computation:-

Here in the above timing report RT is computed as other end arrival time (0.010 ns) + Phase Shift (3.680ns , clock period) – setup (0.122 ns, time required by the clock to setup) - uncertainty (0.010 ns). Required Time (RT) at the endpoint evaluates to 3.558 ns.

$$\text{Slack} = \text{Required Time} - \text{Arrival Time} = 0.031 \text{ ns.}$$

If we compare the results before and after placement we see the worst slack of the critical path has decreased.

#### Hold Analysis:-

```
# Generated by: Cadence Innovus 20.10-p04_1
# OS: Linux x86_64(Host ID edaserver4)
# Generated on: Wed Apr 17 17:48:23 2024
# Design: mesh
# Command: report timing -check type hold > ./Physical_Design_Scripts2/TimingReports/hold_analysis_after_placement.rpt
#####
Path 1: MET Hold Check with Pin p0_configure1_reg[1]/CK
Endpoint: p0_configure1_reg[1]/(") checked with leading edge of 'clk'
Beginpoint: p0_configure[1] ("") triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time 0.010
+ Hold 0.008
+ Phase Shift 0.008
+ Uncertainty 0.010
= Required Time 0.028
Arrival Time 0.056
Slack Time 0.022
    Clock Rise Edge 0.009
    + Input Delay 0.040
    + Network Insertion Delay 0.010
    = Beginpoint Arrival Time 0.059
+
| Instance | Arc | Cell | Delay | Arrival Time | Required Time |
|-----|-----|-----|-----|-----|-----|
| p0_configure1_reg[1] | p0_configure[1] ^ | SORROX1 | 0.000 | 0.050 | 0.028 |
```

In this timing report it shows the critical path of all the paths present in the circuit. The critical path starts from p0\_configure[1] and ends at p0\_configure1\_reg[1] / D that is at the D pin of the Flip Flop.

#### Arrival Time Computation:-

Starting from the already computed arrival time (other end arrival time) 0.050 ns at beginpoint reset and traversing to the end point through different cells with experiencing different delays are added up. So subsequent vertices arrival time is calculated by adding up the already computed arrival time. Finally, from the above timing report we can infer that AT at the end point is 0.050 ns. In this case the path is from p0\_configure[1] to p0\_configure1\_reg[1] / D which is the D pin of the first flop SDFFQX1.

### Required Time Computation:-

Here in the above timing report RT is computed as other end arrival time (0.010 ns). clock + hold (0.008 ns, time required by the clock to setup) + uncertainty (0.010 ns). Required Time (RT) at the endpoint evaluates to 0.028 ns.

$$\text{Slack} = \text{Arrival Time} - \text{Required Time} = 0.050 - 0.028 = 0.022\text{ns.}$$

### Power Report:

```

-----
*          Innovus 20.10-p004_1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
*
*          Date & Time: 2024-Apr-17 17:48:23 (2024-Apr-17 12:18:23 GMT)
*
*          Design: mesh
*
*          Liberty Libraries used:
*          viewl: /home/rajat211B6/Desktop/New_VDF_Project/library/fast.lib
*
*          Power Domain used:
*
*          Power View : viewl
*
*          User-Defined Activity : N.A.
*
*          Activity File: N.A.
*
*          Hierarchical Global Activity: N.A.
*
*          Global Activity: N.A.
*
*          Sequential Element Activity: N.A.
*
*          Primary Input Activity: 0.280000
*
*          Default icg ratio: N.A.
*
*          Global Comb ClockGate Ratio: N.A.
*
*          Power Units = 1mW
*
*          Time Units = 1e-09 secs
*
*          Temperature = 0
*
*          report_power -outfile ./Physical_Design_Scripts2/PostPlacementPowerRpt/rtl_module_post_placement.rpt -rail_analysis_format V5
*
-----
```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
r3_output2_reg[17]	0.02129	0.1575	0.1792	0.000484	SDFFQX4
p0_data_got1_reg[8]	0.0179	0.08477	0.103	0.000299	SDFFQX2
r0_output2_reg[9]	0.01779	0.08419	0.1023	0.000299	SDFFQX2
p1_data_got1_reg[6]	0.01775	0.08488	0.1021	0.000299	SDFFQX2
p3_data_got1_reg[8]	0.01793	0.08388	0.1021	0.000299	SDFFQX2

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
<hr/>					
r3_output2_reg[17]	0.0126	0.1573	0.1792	0.000404	SDFFOX2
r0_output2_reg[8]	0.0179	0.08477	0.102	0.0002999	SDFFOX2
r0_output2_reg[9]	0.01779	0.08419	0.1023	0.0002999	SDFFOX2
p3_data_g01_reg[6]	0.01775	0.08408	0.1021	0.0002999	SDFFOX2
p3_data_g01_reg[0]	0.01793	0.08388	0.1021	0.0002999	SDFFOX2
r0_output2_reg[11]	0.01794	0.08382	0.1021	0.0002999	SDFFOX2
p3_data_g01_reg[1]	0.01802	0.08373	0.1021	0.0002999	SDFFOX2
r0_output2_reg[14]	0.01788	0.08387	0.102	0.0002999	SDFFOX2
r0_output2_reg[12]	0.01787	0.08379	0.102	0.0002999	SDFFOX2
r0_output2_reg[0]	0.0179	0.08371	0.1019	0.0002999	SDFFOX2
p3_data_g01_reg[3]	0.01798	0.08363	0.1019	0.0002999	SDFFOX2
r0_output2_reg[16]	0.01772	0.08301	0.1018	0.0002999	SDFFOX2
r0_output2_reg[17]	0.0177	0.08376	0.1018	0.0002999	SDFFOX2
p0_data_g01_reg[5]	0.01787	0.08357	0.1017	0.0002999	SDFFOX2
p3_data_g01_reg[4]	0.01791	0.08353	0.1017	0.0002999	SDFFOX2
p0_data_g01_reg[0]	0.01786	0.08353	0.1017	0.0002999	SDFFOX2
p3_data_g01_reg[2]	0.01789	0.08344	0.1016	0.0002999	SDFFOX2
r2_output2_reg[1]	0.01887	0.08323	0.1016	0.0002999	SDFFOX2
p1_data_g01_reg[7]	0.0178	0.0835	0.1016	0.0002999	SDFFOX2
p0_data_g01_reg[3]	0.01788	0.08332	0.1016	0.0002999	SDFFOX2
p0_data_g01_reg[2]	0.01786	0.08333	0.1015	0.0002999	SDFFOX2
r3_output2_reg[6]	0.01806	0.08321	0.1013	0.0002999	SDFFOX2
r3_output2_reg[2]	0.01806	0.08321	0.1015	0.0002999	SDFFOX2
r1_output2_reg[12]	0.01794	0.08322	0.1015	0.0002999	SDFFOX2
p0_data_g01_reg[6]	0.01785	0.08329	0.1014	0.0002999	SDFFOX2
r1_output2_reg[2]	0.01788	0.08326	0.1014	0.0002999	SDFFOX2
p0_data_g01_reg[4]	0.01785	0.08328	0.1014	0.0002999	SDFFOX2
r3_output2_reg[12]	0.01778	0.08332	0.1014	0.0002999	SDFFOX2
r1_output2_reg[5]	0.01795	0.08314	0.1014	0.0002999	SDFFOX2
r3_output2_reg[11]	0.01779	0.08329	0.1014	0.0002999	SDFFOX2
r1_output2_reg[15]	0.01793	0.08315	0.1014	0.0002999	SDFFOX2
r0_output2_reg[3]	0.0177	0.08338	0.1014	0.0002999	SDFFOX2
p0_data_g01_reg[1]	0.01766	0.0832	0.1014	0.0002999	SDFFOX2
r2_output2_reg[7]	0.01779	0.08323	0.1013	0.0002999	SDFFOX2
p0_data_g01_reg[7]	0.01787	0.08315	0.1013	0.0002999	SDFFOX2
r1_output2_reg[1]	0.01781	0.08317	0.1013	0.0002999	SDFFOX2
r3_output2_reg[0]	0.01885	0.08294	0.1013	0.0002999	SDFFOX2
p3_data_g01_reg[5]	0.0179	0.08368	0.1013	0.0002999	SDFFOX2
r1_output2_reg[14]	0.01793	0.0844	0.1012	0.0002999	SDFFOX2
p2_data_g01_reg[1]	0.01787	0.08309	0.1013	0.0002999	SDFFOX2
p1_data_g01_reg[3]	0.01775	0.08344	0.1012	0.0002999	SDFFOX2
r3_output2_reg[8]	0.01795	0.08299	0.1012	0.0002999	SDFFOX2
p0_data_g01_reg[2]	0.01788	0.08305	0.1012	0.0002999	SDFFOX2
r1_output2_reg[6]	0.01781	0.08312	0.1012	0.0002999	SDFFOX2
r1_output2_reg[13]	0.01792	0.08299	0.1012	0.0002999	SDFFOX2
r3_output2_reg[1]	0.01799	0.08291	0.1012	0.0002999	SDFFOX2
r2_output2_reg[0]	0.01781	0.08368	0.1012	0.0002999	SDFFOX2
<hr/>					
m0/g15439	4.178e-05	6.837e-05	0.0001455	3.532e-05	NOR2XL
m0/g16130	6.237e-05	7.176e-06	0.0001421	7.256e-05	NAND2BX1
g1097	6.055e-05	3.761e-05	0.0001335	3.532e-05	NOR2XL
m0/g16127	4.083e-05	1.815e-05	0.0001315	7.256e-05	NAND2BX1
inc_p3_add_175_41/g94	5.582e-05	2.73e-05	0.0001263	4.322e-05	AND3X1
m0/g15473	5.62e-05	3.305e-05	0.0001246	3.532e-05	NOR2XL
g1103	6.312e-05	3.874e-05	0.0001229	2.103e-05	NAND4XL
g1104	5.661e-05	3.678e-05	0.0001144	2.103e-05	NAND4XL
m0/g14819	5.029e-05	1.464e-05	0.0001138	4.89e-05	AOI31X1
m0/g15438	4.523e-05	3.145e-05	0.0001112	3.532e-05	NOR2XL
m0/g15413	5.243e-05	2.605e-05	9.933e-05	2.085e-05	OA121XL
m0/g15451	1.481e-05	6.066e-05	9.645e-05	2.097e-05	NAND2XL
m0/g15153	4.957e-05	2.585e-05	9.639e-05	2.097e-05	NAND2XL
m0/g15468	2.609e-05	4.697e-05	9.403e-05	2.097e-05	NAND2XL
g1098	3.834e-05	2.016e-05	9.381e-05	3.532e-05	NOR2XL
inc_p2_add_175_41/g95	2.161e-05	4.986e-05	9.244e-05	2.097e-05	NAND2XL
m0/g15440	1.797e-05	3.695e-05	9.024e-05	3.532e-05	NOR2XL
m0/g15154	3.669e-05	2.95e-05	8.716e-05	2.097e-05	NAND2XL
inc_p1_add_175_41/g95	1.947e-05	4.496e-05	8.541e-05	2.097e-05	NAND2XL
m0/g14910	2.729e-05	2.308e-05	7.976e-05	2.939e-05	OA1211X1
inc_p1_add_175_41/g94	2.225e-05	1.017e-05	7.563e-05	4.322e-05	AND3X1
inc_p2_add_175_41/g94	2.192e-05	8.512e-06	7.365e-05	4.322e-05	AND3X1
inc_p6_add_175_41/g90	1.669e-05	3.472e-05	7.238e-05	2.097e-05	NAND2XL
m0/g15404	2.946e-05	2.153e-05	7.197e-05	2.097e-05	NAND2XL
m0/g15466	2.065e-05	2.51e-05	6.672e-05	2.097e-05	NAND2XL
m0/g15259	1.447e-05	2.462e-06	6.609e-05	4.916e-05	AOI21X1
m0/g15441	1.366e-05	2.662e-05	6.126e-05	2.097e-05	NAND2XL
g1096	1.591e-05	7.043e-06	5.827e-05	3.532e-05	NOR2XL
m0/g14673	1.391e-05	5.543e-06	5.477e-05	3.532e-05	NOR2XL
g1095	1.23e-05	5.153e-06	5.277e-05	3.532e-05	NOR2XL
m0/g14983	1.936e-05	5.406e-06	4.574e-05	2.097e-05	NAND2XL
m0/g15443	1.426e-05	8.884e-06	4.412e-05	2.097e-05	NAND2XL
inc_p3_add_175_41/g90	7.097e-06	1.564e-05	4.371e-05	2.097e-05	NAND2XL
m0/g16156	9.56e-06	1.437e-06	4.028e-05	2.928e-05	OA121X1
m0/g15410	9.775e-06	8.326e-06	3.907e-05	2.097e-05	NAND2XL
m0/g15393	4.445e-06	1.71e-06	3.565e-05	2.95e-05	CLKINVX1
m0/g15442	5.275e-06	4.039e-06	3.029e-05	2.097e-05	NAND2XL
inc_p1_add_175_41/g90	2.639e-06	5.905e-06	2.952e-05	2.097e-05	NAND2XL
m0/g15444	4.494e-06	3.868e-06	2.934e-05	2.097e-05	NAND2XL
inc_p2_add_175_41/g90	2.278e-06	5.058e-06	2.831e-05	2.097e-05	NAND2XL
m0/g15445	3.489e-06	3.049e-06	2.751e-05	2.097e-05	NAND2XL
m0/g15414	4.626e-06	1.84e-06	2.744e-05	2.097e-05	NAND2XL
m0/g15457	4.203e-06	1.853e-06	2.703e-05	2.097e-05	NAND2XL
m0/gopt16284	2.988e-06	2.105e-06	2.606e-05	2.097e-05	INVXL
<hr/>					
Total ( 2790 of 2790 )	10.68	12.59	23.51	0.2407	
Total Capacitance	9.166e-11 F				
Power Density	*** No Die Area ***				

rtl\_module\_post\_placement.rpt (~/Desktop/New\_VDF\_Proje

The report is too big to incorporate into the report

In this report, internal power is the power dissipated inside the cell boundary during charging and discharging of existing capacitances. Total Internal Power is 10.68mW

Switching power of driving cell is the power dissipated by charging load capacitance at the output. The total switching power is 12.59mW

Leakage power is generated from the leakage current that flows between VDD and GND when there is no switching. The total leakage power is 0.2407mW

The total power which is the sum of all these is 23.51mW

## Area Report:

```
#####
# Generated by: Cadence Innovus 20.10-p004.1
# OS: Linux x86_64 (Host ID: edaserver4)
# Generated on: Wed Apr 17 17:48:23 2024
# Design: mesh
# Command: summaryReport -outdir ./Physical Design Scripts2/postPlaceArea -noHtml
#####

=====
General Design Information
=====

Design Status: Routed
Design Name: mesh
# Instances: 2790
# Hard Macros: 0
# Std Cells: 2790

=====
Standard Cells in Netlist
=====



| Cell Type  | Instance Count | Area (μm <sup>2</sup> ) |
|------------|----------------|-------------------------|
| OA12B8I1X1 | 5              | 26.4915                 |
| A0122XL    | 1              | 6.0552                  |
| NAND3X4    | 1              | 14.3811                 |
| A0132XL    | 1              | 6.8121                  |
| OA12B8I1XL | 4              | 24.2208                 |
| BUFX2      | 15             | 68.1210                 |
| NR3BX2     | 1              | 9.8397                  |
| CLKXOR2X1  | 9              | 74.9331                 |
| TLATNK1    | 4              | 57.5244                 |
| OA1222XL   | 1              | 8.3259                  |
| OR2X1      | 3              | 13.6242                 |
| OA12B8I1X1 | 32             | 193.7664                |
| AND2X1     | 53             | 249.6942                |
| OA133XL    | 4              | 30.2760                 |
| OA1211X1   | 76             | 482.6708                |
| AND3X1     | 8              | 48.4416                 |
| SDFFOX1    | 297            | 6069.5811               |
| XNOR2X1    | 3              | 24.9777                 |
| MUX2X1     | 21             | 143.0541                |
| AND2XL     | 16             | 72.6624                 |
| XOR2XL     | 4              | 33.3030                 |
| OA1222XL   | 173            | 1440.3887               |
| OA121X1    | 138            | 599.3820                |
| OA1221X1   | 27             | 204.3630                |
| OA131X1    | 4              | 24.2208                 |
| OA21X1     | 18             | 122.6178                |
| CLKINVX1   | 234            | 531.3438                |
| OA1211X1   | 66             | 349.6878                |
| NAND2BX1   | 33             | 149.8662                |


```

```

DoFloorPlan_2.tcl ] [ setup_analysis_after_placement.rpt ] [ hold_analysis_after_placement.rpt ] [ rtl_module_post_placement.rpt ] [ Area_detail.rpt ] [ mesh.main.htm.ascii ] 
CLKINVX1 229 321.3430
A0I211X1 66 349.6678
NAND2BX1 33 149.8662
OAI211XL 104 551.0232
OAI22X1 1 7.5690
CLKINVX4 1 6.0552
XNOR2XL 12 99.9108
NAND3X1 24 108.9936
NAND2XL 334 1011.2184
SDFFRHGX1 149 3721.6773
NOR2BX1 23 104.4522
OA122XL 43 266.3736
OA121XL 33 149.8662
OA132X1 6 46.8726
A0T21X1 124 563.1336
NOR2XL 2 7.5690
NOR3BX1 37 224.0424
INVXL 16 36.3312
A0I221XL 8 68.5520
A0I31X1 9 54.4968
NAND3BX1 6 36.3312
AO21X1 4 27.2484
OA1221XL 34 257.3460
NOR3X1 42 196.7388
AND2X4 1 8.3259
NOR4BX1 1 6.8121
NOR4XL 4 24.2288
A0I211XL 2 10.5966
NAND2BX1 3 13.6242
SDFFSHOX1 13 354.2292
INVXL 70 158.9490
OA122XL 25 151.3800
NOR2XL 135 408.7260
SDFFOX4 1 24.9777
OA133X1 2 16.6518
SDFFOX2 111 2436.4611
AO122XL 50 302.7600
OA132XL 7 47.6847
NOR3XL 4 18.1656
AO121XL 4 18.1656
OR3X1 1 6.0552
AOI32X1 12 81.7452
OA12BB1XL 28 148.3524
NAND4XL 10 52.9830
MXI2XL 50 302.7600

# Pads: 0
# Net: 2957
# Special Net: 2
# IO Pins: 0

```

mesh.main.htm.ascii /> /Packton/Nano\_VME\_Devkit/

```

***** Placement Information *****
=====
Total area of Standard cells: 23096.047 um^2
Total area of Standard cells(Subtracting Physical Cells): 23096.047 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of All cells: 23096.047 um^2
Total area of Core: 21962.377 um^2
Total area of Chip: 34931.776 um^2
Effective Utilization: 7.2260e-01
Number of Cell Rows: 68
% Pure Gate Density #1 (Subtracting BLOCKAGES): 72.260%
% Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 72.260%
% Pure Gate Density #3 (Subtracting MACROS): 72.260%
% Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 72.260%
% Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 72.260%
% Pure Gate Density #6 ((Unreplaced Standard Inst + Unreplaced Black Blob Inst + Fixed Clock Inst Area) / (Free Site Area + Fixed Clock Inst Area) for insts are placed): 72.260%
% Core Density (Counting Std Cells and MACROS): 72.260%
% Core Density #1 (Subtracting Physical Cells): 72.260%
% Chip Density (Counting Std Cells and MACROS and IOs): 66.118%
% Chip Density #2(Subtracting Physical Cells): 66.118%
# Macros within 5 sites of IO pad: No
Macro halo defined?: No
=====
```

Inst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop	Latch	Clock
			Physical						
mesh		2790	23096.047	68.121	732.679	9530.796	12600.926	57.524	
0.000	0.000	0.000							
inc_p0_add_175_41	increment_unsigned_138	16	74.933	0.000	0.000	74.933	0.000	0.000	
0.000	0.000	0.000							
inc_p1_add_175_41	increment_unsigned_158	16	74.933	0.000	0.000	74.933	0.000	0.000	
0.000	0.000	0.000							
inc_p2_add_175_41	increment_unsigned_178	16	74.933	0.000	0.000	74.933	0.000	0.000	
0.000	0.000	0.000							
inc_p3_add_175_41	increment_unsigned_198	16	74.933	0.000	0.000	74.933	0.000	0.000	
0.000	0.000	0.000							
r0	master	1292	7265.483	4.541	444.300	4893.359	1923.283	0.000	
0.000	0.000	0.000							
r0	router	232	1970.211	0.000	65.858	902.982	1601.379	0.000	
0.000	0.000	0.000							
r1	router_355	229	1998.216	0.000	59.038	910.551	1828.627	0.000	
0.000	0.000	0.000							
r2	router_354	228	1961.128	0.000	56.757	902.982	1601.379	0.000	
0.000	0.000	0.000							
r3	router_353	227	1961.128	0.000	54.497	905.252	1601.379	0.000	
0.000	0.000	0.000							

Area of standard cells :  $23096.047 \mu m^2$

Area of Buffers :  $68.121 \mu m^2$

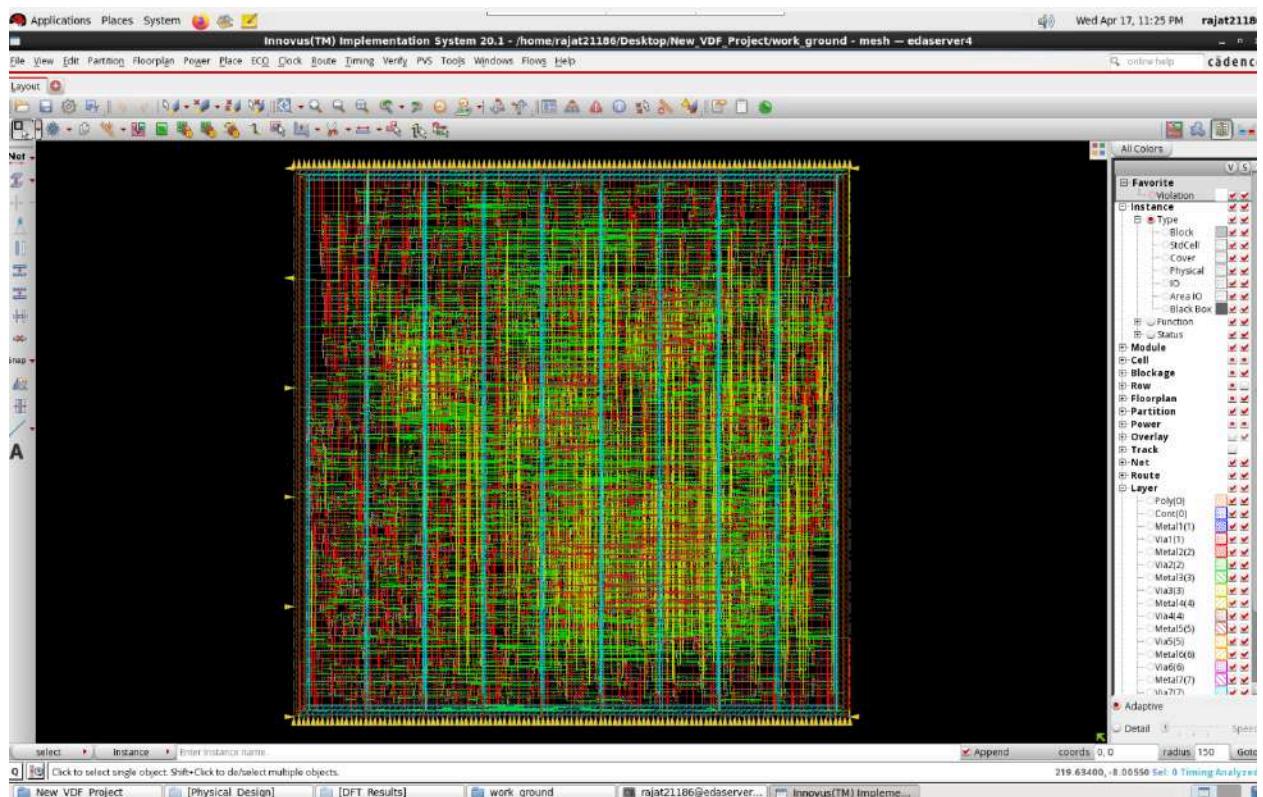
Area of Inverters :  $732.679 \mu m^2$

Area of Combinational:  $9630.796 \mu m^2$

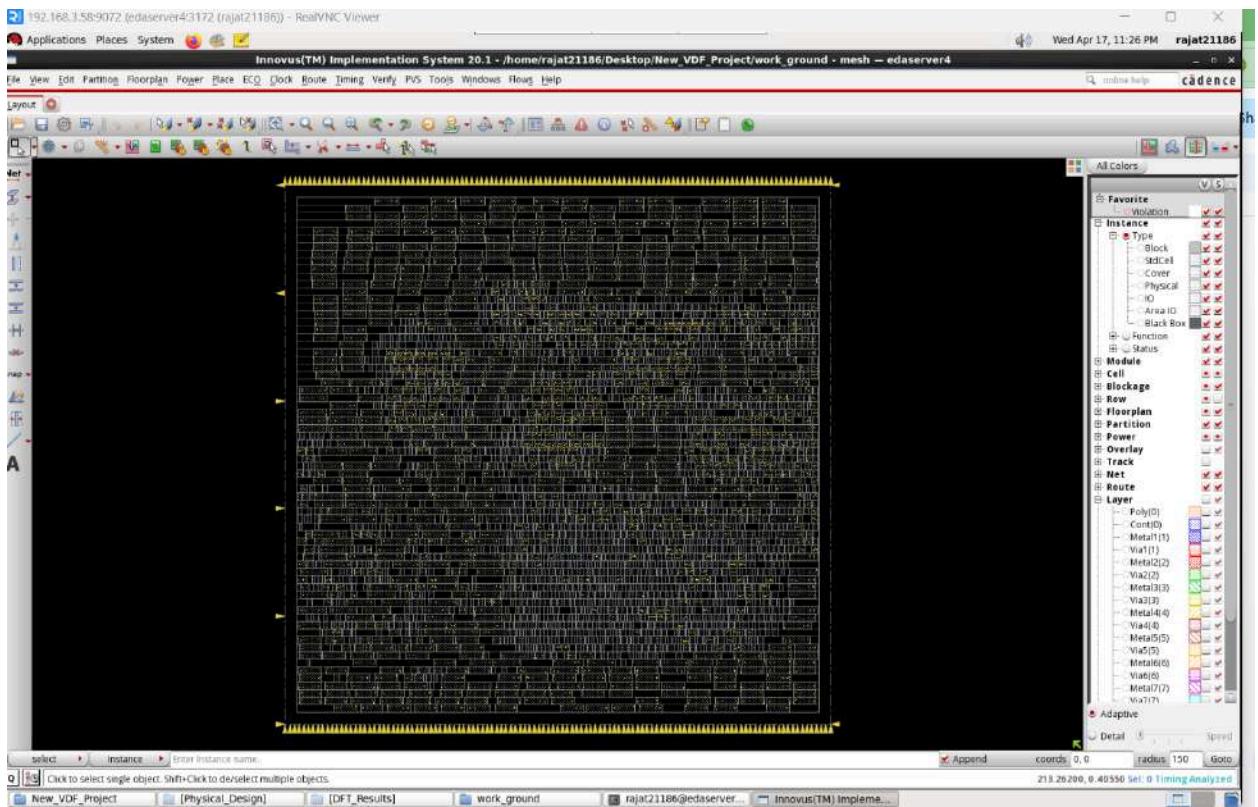
Area of flip-flops :  $12606.926 \mu m^2$  (SDFFHQX1 + SDFFQX1)

Snap-shot of layout of design and connectivity showing Fly-Lines:

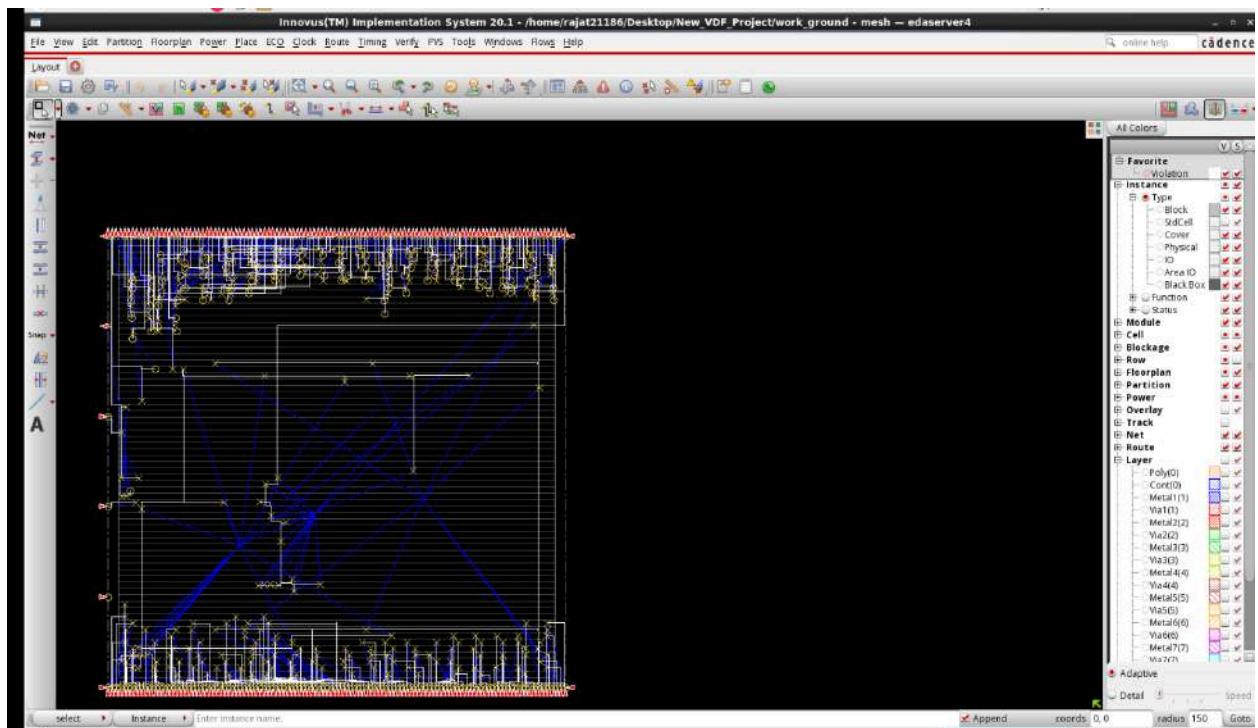
Layout after Placement:



Standard Cells after Placement:



## Flight Lines:



## Effect of placement of timing

After placement the Required Time and Arrival Time will also increase because static Timing Analysis will only take into account the delays of the standard cells while the tool while doing placement of cells will take into account delays of wire length, timing and congestion in the design. So the worst slack decreases.

If we compare the results before and after placement we see the worst slack of the critical path has decreased.

## 3. Clock Tree Synthesis

Software Used:

Cadence Innovus

Commands Used:

1. csh
2. source /cadence/cshrc
3. Innovus
4. source (tcl file)

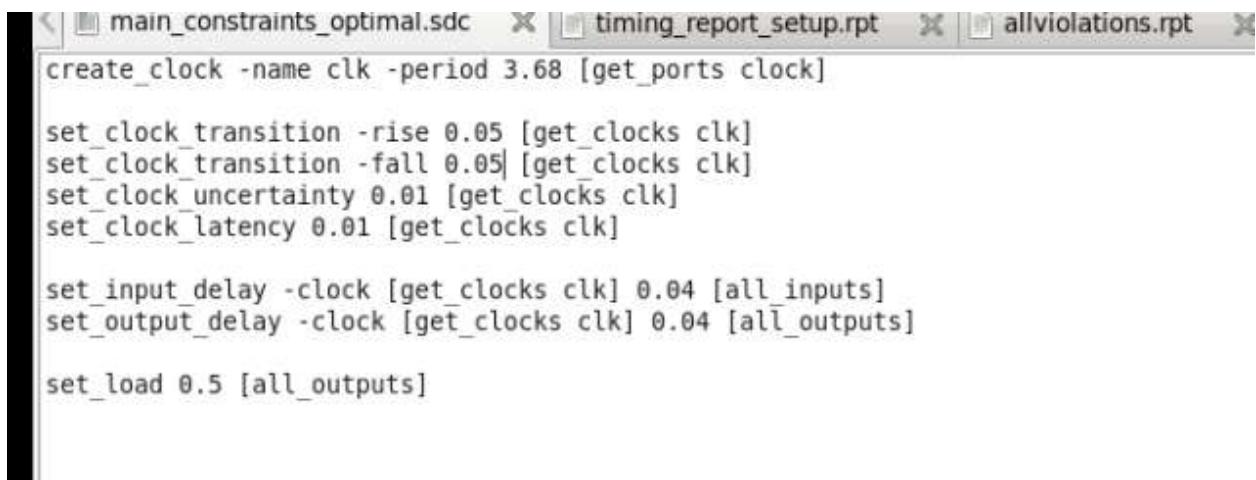
## Layout Design Core Utilization:- 0.5

TCL file

DoCTS.tcl:

```
set ccopt mode -cts buffer_cells {CLKBUFX12 CLKBUFX16 CLKBUFX2 CLKBUFX20 CLKBUFX3 CLKBUFX4 CLKBUFX6 CLKBUFX8 CLKINVX1 CLKINVX12 CLKINVX16 CLKINVX20 CLKINVX3 CLKINVX4 CLKINVX6 CLKINVX8} -  
cts opt priority all  
create_ccopt_clock_tree_spec -file file_cts.spec -keep_all_sdc_clocks -views {view1}  
  
source file_cts.spec  
ccopt design -check_prerequisites  
ccopt design  
optDesign -postCTS -setup  
optDesign -postCTS -hold; #for hold violation  
  
#Power Analysis/  
  
set power_analysis_mode -reset  
set power_analysis_mode -method static -analysis_view view1 -corner max -create_binary_db true -write_static_currents true -honor_negative_energy true -ignore_control_signals true  
set power_output_dir -reset  
set power_input_dir ..\Physical_Design_scripts\PostCTSPowerRPT  
set default_switching_activity -reset  
set default_switching_activity -input activity 0.2 -period 10.0  
read activity_file -reset  
set power_reset  
set powerup_analysis -reset  
  
set dynamic_power_simulation -reset  
report_power -rail_analysis_format VS -outfile ..\Physical_Design_scripts\PostCTSPowerRPT\rtl_module_post_cts.rpt  
  
# Area  
summaryReport -outdir ..\Physical_Design_scripts/postCTSArea -noHTML  
report_area -detail -show_leaf_cells -table_style {vertical}  
  
setAnalysisMode -checkType setup  
report_timing -check_type setup > ..\Physical_Design_scripts/TimingReports/setup_analysis_after_CTS.rpt  
  
setAnalysisMode -checkType hold  
report_timing -check_type hold > ..\Physical_Design_scripts/TimingReports/hold_analysis_after_CTS.rpt  
report_area > ..\Physical_Design_scripts/postCTSArea/Area_report.rpt
```

Constraints used:



The screenshot shows a terminal window with three tabs: 'main\_constraints\_optimal.sdc', 'timing\_report\_setup.rpt', and 'allviolations.rpt'. The 'main\_constraints\_optimal.sdc' tab contains the following constraint script:

```
create_clock -name clk -period 3.68 [get_ports clock]  
  
set_clock_transition -rise 0.05 [get_clocks clk]  
set_clock_transition -fall 0.05 [get_clocks clk]  
set_clock_uncertainty 0.01 [get_clocks clk]  
set_clock_latency 0.01 [get_clocks clk]  
  
set_input_delay -clock [get_clocks clk] 0.04 [all_inputs]  
set_output_delay -clock [get_clocks clk] 0.04 [all_outputs]  
  
set_load 0.5 [all_outputs]
```

Timing Reports:

## Setup Reports:

Setup Report for Path 1: MET Setup Check with Pin #0/response signals2 reg[3]/0 (v) checked with leading edge of 'clk'						
Beginpoint: reset (v) triggered by leading edge of 'clk'						
Path Groups: {clk}						
Analysis View: view1						
Other End Arrival Time 0.089						
- Setup 0.123	+ Phase Shift 3.688	- Uncertainty 0.018	= Required Time 3.556	- Arrival Time 3.522	= Slack Time 0.034	
Clock Rise Edge 0.000	+ Input Delay 0.040	+ Network Insertion Delay 0.010	= Beginpoint Arrival Time 0.050			
Instance	Arc	Cell	Delay	Arrival Time	Required Time	
FE_DBTC0_reset	reset v	INVX1	0.467	0.517	0.551	
FE_OFCl1_FE_DBTN0_reset	A ^ -> Y ^	BUFX2	0.299	0.816	0.850	
FE_OFCl2_FE_DBTN0_reset	A ^ -> Y ^	BUFX2	0.406	1.223	1.256	
g551	A ^ -> Y ^	AND2X1	0.226	1.511	1.545	
m0/FE_OFCl0_P0_signals_1	A ^ -> Y ^	CLKINVX1	0.226	1.737	1.770	
m0/g18893	I v -> Y ^	OR2X1	0.153	1.899	1.923	
m0/g18738	A v -> Y ^	CLKINVX1	0.107	1.987	2.031	
m0/g18647	B ^ -> Y v	NAND2X1	0.057	2.054	2.088	
m0/g18538	B v -> Y v	AND2X1	0.048	2.102	2.136	
m0/g18407	A0 v -> Y ^	OA122XL	0.044	2.149	2.182	
m0/g18319	A ^ -> Y ^	NOR2XL	0.035	2.183	2.217	
m0/g18292	C v -> Y v	AND4X4	0.117	2.306	2.333	
m0/FE_OFCl5_n_749	A v -> Y ^	CLKINVX2	0.160	2.468	2.494	
m0/g18256	A1 ^ -> Y v	DA121XL	0.028	2.469	2.522	
m0/g18257	A1 v -> Y v	AO1221X1	0.026	2.549	2.593	
m0/g18228	CO v -> Y v	AO1221X1	0.064	2.613	2.646	
m0/g18225	B ^ -> Y v	NAND2X1	0.026	2.633	2.667	
m0/g18224	D v -> Y v	OR4X2	0.166	2.799	2.833	
m0/FE_OFCl7_n_B16	A v -> Y ^	CLKINVX4	0.124	2.924	2.957	
m0/g18185	A1 ^ -> Y v	AO121XL	0.041	2.965	2.998	

Setup Report for Path 1: MET Setup Check with Pin #0/response signals2 reg[3]/0 (v) checked with leading edge of 'clk'						
Beginpoint: reset (v) triggered by leading edge of 'clk'						
Path Groups: {clk}						
Analysis View: view1						
Other End Arrival Time 0.089						
- Setup 0.123	+ Phase Shift 3.688	- Uncertainty 0.018	= Required Time 3.556	- Arrival Time 3.522	= Slack Time 0.034	
Clock Rise Edge 0.000	+ Input Delay 0.040	+ Network Insertion Delay 0.010	= Beginpoint Arrival Time 0.050			
Instance	Arc	Cell	Delay	Arrival Time	Required Time	
FE_DBTC0_reset	reset v	INVX1	0.467	0.517	0.551	
FE_OFCl1_FE_DBTN0_reset	A ^ -> Y ^	BUFX2	0.299	0.816	0.850	
FE_OFCl2_FE_DBTN0_reset	A ^ -> Y ^	BUFX2	0.406	1.223	1.256	
g551	A ^ -> Y ^	AND2X1	0.226	1.511	1.545	
m0/FE_OFCl0_P0_signals_1	A ^ -> Y ^	CLKINVX1	0.226	1.737	1.770	
m0/g18893	I v -> Y ^	OR2X1	0.153	1.899	1.923	
m0/g18738	A v -> Y ^	CLKINVX1	0.107	1.987	2.031	
m0/g18647	B ^ -> Y v	NAND2X1	0.057	2.054	2.088	
m0/g18538	B v -> Y v	AND2X1	0.048	2.102	2.136	
m0/g18407	A0 v -> Y ^	OA122XL	0.046	2.149	2.182	
m0/g18319	A ^ -> Y ^	NOR2XL	0.035	2.183	2.217	
m0/g18292	C v -> Y v	AND4X4	0.117	2.306	2.333	
m0/FE_OFCl5_n_749	A v -> Y ^	CLKINVX2	0.160	2.468	2.494	
m0/g18256	A1 ^ -> Y v	DA121XL	0.028	2.469	2.522	
m0/g18257	A1 v -> Y v	AO1221X1	0.026	2.549	2.593	
m0/g18228	CO v -> Y v	AO1221X1	0.064	2.613	2.646	
m0/g18225	B ^ -> Y v	NAND2X1	0.026	2.633	2.667	
m0/g18224	D v -> Y v	OR4X2	0.166	2.799	2.833	
m0/FE_OFCl7_n_B16	A v -> Y ^	CLKINVX4	0.124	2.924	2.957	
m0/g18185	A1 ^ -> Y v	AO121XL	0.041	2.965	2.998	
m0/g18163	A1N v -> Y v	OA128XL	0.040	3.013	3.047	
m0/g18154	CO v -> Y ^	OA121XL	0.044	3.057	3.090	
m0/g18153	B0 ^ -> Y v	OA121XL	0.013	3.078	3.184	
m0/g2	AN v -> Y v	NOR4BX	0.837	3.107	3.141	
m0/FE_OFCl4_n_25	A v -> Y ^	BUFX2	0.174	3.281	3.315	
m0/g18151	A v -> Y ^	CLKINVX2	0.172	3.453	3.487	
m0/g18073	A1 ^ -> Y v	OA121XL	0.068	3.522	3.555	
m0/response_signals2_reg[3]   D v	SDFFRHQX1	0.001	3.522	3.556		

In this timing report it shows the critical path of all the paths present in the circuit. The critical path starts from reset and ends at m0/response\_signals2\_reg[3] /D that is at the D pin of the Flip Flop.

#### Arrival Time Computation:-

Starting from the already computed arrival time (other end arrival time) 0.050 ns at beginpoint reset and traversing to the end point through different cells with experiencing different delays are added up. So subsequent vertices arrival time is calculated by adding up the already computed arrival time. Finally, from the above timing report we can infer that AT at the end point is 3.522 ns.

#### Required Time Computation:-

Here in the above timing report RT is computed as other end arrival time (0.009 ns) + Phase Shift (3.680ns , clock period) – setup (0.123 ns, time required by the clock to setup) - uncertainty (0.010 ns). Required Time (RT) at the endpoint evaluates to 3.556 ns.

Slack = Required Time - Arrival Time = 0.034 ns.

#### Hold Report:-

```

rti_module_post_placement.rpt Area_report.rpt mesn.main.htm.ascii lopadplacement.io synthesised_netlist.v Area_detail.rpt setup_analysis_after_CTS.rpt hold_analysis_after_CTS.rpt
#####
# Generated by: Cadence Innovus 28.1e-0604.1
# OS: Linux x86_64(Host ID edaserver4)
# Generated on Wed Apr 17 17:09:23 2024
# Design: mesn
# Command: report timing -check type hold > ../../Physical_Design_Scripts/TimingReports/hold_analysis_after_CTS.rpt
#####

Path 1: MET Hold Check with Pin p0_configure1_reg[5]/OK
Endpoint: p0_configure1_reg[5]/D (^) checked with leading edge of 'clk'
Beginpoint: p0_configure[5] (^) triggered by leading edge of 'clk'
Path Groups: (clk)
Analysis View: view1
Other End Arrival Time 0.010
+ Hold 0.002
+ Phase Shift 0.000
+ Uncertainty 0.010
= Required Time 0.022
Arrival Time 0.050
Slack Time | 0.034
Clock Rise Edge 0.000
+ Input Delay 0.040
+ Network Insertion Delay 0.010
= Beginpoint Arrival Time 0.050
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
| p0_configure1_reg[5] | p0_configure[5] ^ | SDFIFOX1 | 0.000 | 0.050 | 0.022 |
+-----+

```

In this timing report it shows the critical path of all the paths present in the circuit. The critical path starts from p0\_configure[5] and ends at p0\_configure1\_reg[5] / D that is at the D pin of the Flip Flop.

#### Arrival Time Computation:-

Starting from the already computed arrival time (other end arrival time) 0.050 ns at beginpoint reset and traversing to the end point through different cells with experiencing different delays are added up. So subsequent vertices arrival time is calculated by adding up the already computed arrival time. Finally, from the above timing report we can infer that AT at the end point is 0.050 ns. In this case the path is from p0\_configure[5] to p0\_configure1\_reg[5] / D which is the D pin of the first flop SDFFQX1.

#### Required Time Computation:-

Here in the above timing report RT is computed as other end arrival time (0.010 ns). clock + hold (0.002 ns, time required by the clock to setup) + uncertainty (0.010 ns). Required Time (RT) at the endpoint evaluates to 0.022 ns.

$$\text{Slack} = \text{Arrival Time} - \text{Required Time} = 0.050 - 0.022 = 0.028\text{ns.}$$

## Power Report:

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
r3_output2_reg[17]	0.0191	0.136	0.1555	0.0004046	SDFFQX4
CTS_ccl_a_buf_00013	0.05685	0.08263	0.1391	0.0004104	CLKBUFX16
CTS_ccl_a_buf_00019	0.05589	0.06779	0.1241	0.0004104	CLKBUFX16
CTS_ccl_a_buf_00023	0.05561	0.06706	0.1231	0.0004104	CLKBUFX16
CTS_ccl_a_buf_00017	0.05571	0.06219	0.1183	0.0004104	CLKBUFX16
o3_data_got1_reg[1]	0.01763	0.08388	0.1018	0.0002999	SDFFQX2
r3_output2_reg[2]	0.01778	0.08334	0.1014	0.0002999	SDFFQX2
r3_output2_reg[3]	0.0174	0.08364	0.1013	0.0002999	SDFFQX2
o3_data_got1_reg[2]	0.01734	0.08359	0.1012	0.0002999	SDFFQX2
r3_output2_reg[3]	0.01764	0.08292	0.1009	0.0002999	SDFFQX2
o3_data_got1_reg[3]	0.01761	0.08285	0.1008	0.0002999	SDFFQX2
o3_data_got1_reg[6]	0.01675	0.08122	0.09827	0.0002999	SDFFQX2
processor_ready_signals2_reg[0]	0.01725	0.08034	0.09789	0.0002999	SDFFQX2
o3_data_got1_reg[8]	0.01697	0.07986	0.09714	0.0002999	SDFFQX2
o3_data_got1_reg[4]	0.01724	0.07939	0.09694	0.0002999	SDFFQX2
r1_output2_reg[15]	0.01784	0.07874	0.09668	0.0002999	SDFFQX2
r1_output2_reg[14]	0.01699	0.07871	0.0966	0.0002999	SDFFQX2
r1_output2_reg[16]	0.01693	0.07886	0.09583	0.0002999	SDFFQX2
r0_output2_reg[8]	0.01668	0.07877	0.09575	0.0002999	SDFFQX2
r0_output2_reg[3]	0.01717	0.07798	0.09545	0.0002999	SDFFQX2
o3_data_got1_reg[5]	0.01679	0.07811	0.0952	0.0002999	SDFFQX2
r1_output2_reg[17]	0.0169	0.07787	0.09507	0.0002999	SDFFQX2
r3_output2_reg[5]	0.0169	0.07768	0.09488	0.0002999	SDFFQX2
r3_output2_reg[0]	0.0165	0.07773	0.09453	0.0002999	SDFFQX2
CTS_ccl_a_buf_00025	0.03058	0.06346	0.0945	0.0004585	CLKBUFX12
r0_output2_reg[0]	0.0166	0.07695	0.09386	0.0002999	SDFFQX2
r0_output2_reg[4]	0.01644	0.0766	0.09334	0.0002999	SDFFQX2
r1_output2_reg[6]	0.01674	0.07627	0.09331	0.0002999	SDFFQX2
r1_output2_reg[11]	0.01684	0.07606	0.0932	0.0002999	SDFFQX2
r0_output2_reg[9]	0.01639	0.07633	0.09382	0.0002999	SDFFQX2
r0_output2_reg[2]	0.01648	0.07596	0.09274	0.0002999	SDFFQX2
r1_output2_reg[12]	0.01653	0.07579	0.09262	0.0002999	SDFFQX2
CTS_ccl_a_buf_00021	0.03046	0.06145	0.09237	0.0004585	CLKBUFX12
r0_output2_reg[11]	0.01641	0.07565	0.09237	0.0002999	SDFFQX2
r0_output2_reg[6]	0.01624	0.07549	0.09263	0.0002999	SDFFQX2
r0_output2_reg[5]	0.01624	0.07424	0.09079	0.0002999	SDFFQX2
r3_output2_reg[9]	0.01624	0.07357	0.09011	0.0002999	SDFFQX2
o3_data_got1_reg[7]	0.0158	0.07392	0.09062	0.0002999	SDFFQX2
r1_output2_reg[13]	0.01685	0.07325	0.08896	0.0002999	SDFFQX2
r2_output2_reg[16]	0.01664	0.07301	0.08935	0.0002999	SDFFQX2
r3_output2_reg[6]	0.01597	0.07297	0.08924	0.0002999	SDFFQX2
r2_output2_reg[15]	0.016	0.07279	0.08969	0.0002999	SDFFQX2
r3_output2_reg[14]	0.01614	0.07213	0.08856	0.0002999	SDFFQX2
r2_output2_reg[17]	0.01587	0.07235	0.08852	0.0002999	SDFFQX2
r3_output2_reg[15]	0.01611	0.07203	0.08844	0.0002999	SDFFQX2
r1_output2_reg[5]	0.01637	0.0716	0.08828	0.0002999	SDFFQX2
o2_data_got1_reg[4]	0.01568	0.07211	0.08889	0.0002999	SDFFQX2

'l_output2_reg[2]	0.01567	0.07027	0.08623	0.0002999	SDFQX2
'2_output2_reg[10]	0.01559	0.07871	0.08598	0.0002999	SDFQX2
'3_output2_reg[13]	0.01561	0.06958	0.08559	0.0002999	SDFQX2
'3_output2_reg[8]	0.01568	0.06938	0.08536	0.0002999	SDFQX2
'2_data_got1_reg[7]	0.01523	0.06977	0.08529	0.0002999	SDFQX2
'0_output2_reg[10]	0.01543	0.06943	0.08516	0.0002999	SDFQX2
'3_output2_reg[10]	0.01573	0.06913	0.08516	0.0002999	SDFQX2
'3_output2_reg[12]	0.01569	0.06879	0.08479	0.0002999	SDFQX2
'1_output2_reg[1]	0.01554	0.06888	0.08472	0.0002999	SDFQX2
'1_output2_reg[10]	0.01552	0.06885	0.08467	0.0002999	SDFQX2
'2_output2_reg[9]	0.01514	0.06889	0.08439	0.0002999	SDFQX2
'2_output2_reg[3]	0.01549	0.06857	0.08435	0.0002999	SDFQX2
'1_output2_reg[3]	0.01549	0.06849	0.08428	0.0002999	SDFQX2
'2_output2_reg[1]	0.01562	0.06823	0.08415	0.0002999	SDFQX2
'1_output2_reg[0]	0.01543	0.06862	0.08393	0.0002999	SDFQX2
'0_output2_reg[14]	0.01521	0.06831	0.08382	0.0002999	SDFQX2
'2_output2_reg[12]	0.01532	0.06797	0.08359	0.0002999	SDFQX2
processor_ready_signals2_reg[3]	0.01569	0.06726	0.08325	0.0002999	SDFQX2
'0_data_got1_reg[4]	0.0155	0.06723	0.08302	0.0002999	SDFQX2
'2_output2_reg[11]	0.01532	0.06736	0.08298	0.0002999	SDFQX2
'0_output2_reg[9]	0.01519	0.06725	0.08274	0.0002999	SDFQX2
'2_output2_reg[7]	0.01541	0.067	0.08271	0.0002999	SDFQX2
'0_output2_reg[16]	0.01565	0.0671	0.08244	0.0002999	SDFQX2
'2_output2_reg[8]	0.01522	0.06684	0.08236	0.0002999	SDFQX2
'1_output2_reg[9]	0.01477	0.06679	0.08186	0.0002999	SDFQX2
'2_output2_reg[2]	0.01517	0.06624	0.08171	0.0002999	SDFQX2
'0_output2_reg[17]	0.01513	0.06622	0.08165	0.0002999	SDFQX2
'2_output2_reg[4]	0.01517	0.06596	0.08143	0.0002999	SDFQX2
'0_data_got1_reg[3]	0.0152	0.0658	0.0813	0.0002999	SDFQX2
'2_data_got1_reg[3]	0.0144	0.06625	0.08096	0.0002999	SDFQX2
'2_data_got1_reg[1]	0.01534	0.06648	0.07992	0.0002999	SDFQX2
'2_output2_reg[0]	0.01498	0.0646	0.07988	0.0002999	SDFQX2
'0_output2_reg[13]	0.01468	0.06474	0.07972	0.0002999	SDFQX2
processor_ready_signals2_reg[2]	0.01568	0.06379	0.07917	0.0002999	SDFQX2
'0_output2_reg[15]	0.0146	0.06416	0.07906	0.0002999	SDFQX2
'2_output2_reg[5]	0.0149	0.06381	0.07901	0.0002999	SDFQX2
'2_output2_reg[6]	0.01473	0.06322	0.07825	0.0002999	SDFQX2
processor_ready_signals2_reg[1]	0.01495	0.06256	0.07781	0.0002999	SDFQX2
'2_data_got1_reg[6]	0.01579	0.06068	0.07677	0.0002999	SDFQX2
'0_data_got1_reg[8]	0.01477	0.06187	0.07614	0.0002999	SDFQX2
'0_output2_reg[12]	0.01474	0.06048	0.07552	0.0002999	SDFQX2
'0_data_got1_reg[5]	0.01529	0.05946	0.07505	0.0002999	SDFQX2
'0_data_got1_reg[7]	0.01437	0.06037	0.07503	0.0002999	SDFQX2
'2_data_got1_reg[0]	0.01423	0.06023	0.07476	0.0002999	SDFQX2
'0_data_got1_reg[2]	0.01408	0.05991	0.0743	0.0002999	SDFQX2
'0_output2_reg[11]	0.01495	0.05995	0.07429	0.0002999	SDFQX2
'1_data_got1_reg[3]	0.01423	0.05767	0.0722	0.0002999	SDFQX2
'2_data_got1_reg[5]	0.01427	0.05739	0.07196	0.0002999	SDFQX2
'1_data_got1_reg[7]	0.01442	0.05723	0.07195	0.0002999	SDFQX2
'0_data_got1_reg[1]	0.01420	0.05704	0.07194	0.0002999	SDFQX2
r1/g1182	6.089103	4.003e-05	0.080164	2.097e-05	NAND2XL
m0/g18145	0.0001060	3.639e-05	0.0001639	2.097e-05	NAND2XL
g1168	9.009e-05	4.876e-05	0.0001599	2.103e-05	NAUD4XL
m0/g18658	6.612e-05	5.37e-05	0.0001551	3.532e-05	NOR2XL
m0/g18441	8.264e-05	3.585e-05	0.0001538	3.532e-05	NOR2XL
m0/g18692	7.459e-05	3.964e-05	0.0001493	3.566e-05	OA121XL
m0/g18690	9.518e-05	3.293e-05	0.0001409	2.085e-05	OA121XL
r1/g1111	9.192e-05	3.492e-05	0.0001478	2.097e-05	NAND2XL
m0/g18691	8.322e-05	2.86e-05	0.0001321	2.085e-05	OA121XL
g1165	6.553e-05	3.973e-05	0.0001263	2.103e-05	NAND4XL
m0/g18642	2.985e-05	6.811e-05	0.0001189	2.097e-05	NAND2XL
m0/g18438	6.297e-05	3.457e-05	0.0001183	2.097e-05	NAND2XL
m0/g18439	6.777e-05	2.773e-05	0.0001165	2.097e-05	NAND2XL
g1164	6.886e-05	3.341e-05	0.0001115	2.103e-05	NAND4XL
m0/g18641	3.586e-05	4.269e-05	0.0001133	3.532e-05	NOR2XL
m0/g18440	6.231e-05	2.746e-05	0.0001107	2.097e-05	NAND2XL
m0/g18643	4.111e-05	3.37e-05	0.0001101	3.532e-05	NOR2XL
inc_p1_add_175_41/g93	3.274e-05	3.836e-05	0.0001064	3.532e-05	NOR2XL
m0/g18624	5.849e-05	2.516e-05	0.0001045	2.085e-05	OA121XL
m0/g18644	2.649e-05	3.963e-05	0.0001014	3.532e-05	NOR2XL
g1097	4.388e-05	2.123e-05	0.0001004	3.532e-05	NOR2XL
m0/g18636	6.886e-05	3.341e-05	0.0001115	2.103e-05	NAND4XL
g1103	3.586e-05	4.269e-05	0.0001133	3.532e-05	NOR2XL
m0/g18645	6.231e-05	2.746e-05	0.0001107	2.097e-05	NAND2XL
m0/g18653	4.111e-05	3.37e-05	0.0001101	3.532e-05	NOR2XL
inc_p2_add_175_41/g93	1.859e-05	2.375e-05	0.0001064	3.532e-05	NOR2XL
g1098	2.331e-05	1.592e-05	7.455e-05	3.532e-05	NOR2XL
m0/g18165	1.655e-05	1.506e-05	6.155e-05	2.914e-05	OA121XL
inc_p0_add_175_41/g88	1.153e-05	2.768e-05	5.958e-05	2.097e-05	NAND2XL
m0/g18655	7.996e-06	8.472e-05	5.179e-05	3.532e-05	NOR2XL
g1096	9.807e-06	4.469e-05	4.954e-05	3.532e-05	NOR2XL
m0/g18646	9.85e-06	1.438e-05	4.521e-05	2.097e-05	NAND2XL
m0/g18648	5.451e-06	4.311e-06	4.500e-05	3.532e-05	NOR2XL
m0/g18073	4.555e-06	9.357e-06	4.33e-05	2.939e-05	OA121XL
m0/g19241	9.957e-06	3.958e-06	4.32e-05	2.928e-05	OA121XL
g1095	4.656e-06	2.796e-06	4.277e-05	3.532e-05	NOR2XL
m0/g18647	6.082e-06	1.471e-05	4.118e-05	2.097e-05	NAND2XL
m0/g18238	7.827e-06	3.045e-06	4.001e-05	2.914e-05	OA121XL
m0/g19242	4.993e-06	1.735e-06	3.661e-05	2.928e-05	OA121XL
m0/g19240	4.153e-06	9.613e-07	3.434e-05	2.928e-05	OA121XL
inc_p1_add_175_41/g88	3.946e-06	8.662e-06	3.358e-05	2.097e-05	NAND2XL
inc_p3_add_175_41/g88	3.773e-06	8.683e-06	3.335e-05	2.097e-05	NAND2XL
inc_p2_add_175_41/g88	1.961e-06	4.668e-06	2.76e-05	2.097e-05	NAND2XL
m0/g18144	1.755e-06	7.866e-07	2.352e-05	2.097e-05	NAND2XL
Total { 2587 of 2587 }	9.468	10.97	20.67	0.2326	
Total Capacitance		9.139e-11 F			
Power Density		*** No Die Area ***			

The report is too big to incorporate into this pdf

In this report, internal power is the power dissipated inside the cell boundary during charging and discharging of existing capacitances. Total Internal Power is 9.468mW

Switching power of driving cell is the power dissipated by charging load capacitance at the output. The total switching power is 10.97mW

Leakage power is generated from the leakage current that flows between VDD and GND when there is no switching. The total leakage power is 0.2326mW

The total power which is the sum of all these is 20.67mW

## Area Report:

Design Status: Routed			
Design Name: mesh			
# Instances: 2587			
# Hard Macros: 0			
# Std Cells: 2587			
-----			
Standard Cells in Netlist			
Cell Type	Instance Count	Area (um^2)	
OAI2BB1X1	11	58.2813	
A0I22XL	31	187.7112	
OR2XL	1	4.5414	
A0I2BB1XL	2	12.1104	
CLKBUFX8	2	22.7070	
NAND4BXL	1	6.8121	
CLKBUFX12	2	31.7898	
BUFX2	16	72.6624	
CLKXOR2X1	9	74.9331	
TLATNX1	4	57.5244	
OR2X1	7	31.7898	
A0I2BB1X1	3	18.1656	
AND2X1	37	168.0318	
A0I33XL	4	30.2760	
OAI211X1	122	646.3926	
SDFFFQX1	297	6069.5811	
XNOR2X1	4	33.3036	
MX2X1	13	88.5573	
AND2XL	12	54.4968	
XOR2XL	11	91.5849	
A0I222XL	171	1423.7289	
OAI21X1	89	404.1846	
CLKBUFX16	4	84.7728	
OAI221X1	71	537.3990	
OAI31X1	2	12.1104	
OA21X1	15	102.1815	
CLKINVX1	220	499.5540	
OAI211X1	24	127.1592	
NAND2BX1	24	108.9936	
OAI211XL	140	741.7620	
OA22X1	1	7.5690	
CLKINVX4	1	6.0552	
XNOR2XL	4	33.3036	
NAND3X1	15	68.1210	
NAND2XL	328	993.0528	
SDFFRHQX1	149	3721.6773	
OA21XL	1	6.8121	
ADDHX1	4	48.4416	
NOR2BX1	22	99.9108	
OAT32X1	2	10.1656	

OAI21X1	89	404.1846
CLKBUFX16	4	84.7728
OAI221X1	71	537.3990
OAI31X1	2	12.1184
OAI21X1	15	162.1815
CLKINVX1	226	499.5546
AOI211X1	24	127.1592
NAND2BX1	24	108.9936
OAI211XL	140	741.7620
OA22X1	1	7.5696
CLKINVX4	1	6.0552
XNOR2XL	4	33.3036
NAND3X1	15	68.1210
NAND2XL	328	993.0528
SDFRRHQX1	149	3721.6773
OAI21XL	1	6.8121
ADDHX1	4	48.4416
NOR2BX1	22	99.9108
OAI22X1	3	18.1656
OAI21XL	24	168.9936
AOI21X1	105	476.8470
NOR3BX1	40	242.2080
AOI221X1	15	113.5356
AOI31X1	16	60.5526
NAND3BX1	8	48.4416
A021X1	2	13.6242
OAI221XL	5	37.8450
NOR3X1	35	158.9496
NOR4BX1	1	6.8121
OR4X2	1	8.3259
A022X1	1	7.5696
NOR4X1	4	24.2288
A0I211XL	2	10.5966
AND4X4	1	9.8397
SDFFSHQX1	13	354.2292
INVX1	50	113.5356
OAI22XL	1	6.0552
NOR2XL	144	435.9744
SDFFOX4	1	24.9777
OAI33X1	2	16.6518
CLKINVX2	2	7.5696
SDFFQX2	111	2436.4611
A0I22X1	48	296.6496
OAI32XL	5	34.0665
NOR3XL	4	18.1656
A0I21XL	14	63.5796
A0I32X1	21	143.0541
OAI2BB1XL	2	10.5966
A0I221XL	1	7.5696
NAND4XL	37	196.0371

Minst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop	Latch	Clock
Gate	Macro	Physical							
mesh		2587	22293.733	211.932	626.713	8790.637	12666.926	57.524	
0.000	0.000	0.000	0.000	0.000	4.541	70.392	0.000	0.000	
i0c_p0_add_175_41	increment_unsigned_102	16	74.933	0.000	4.541	70.392	0.000	0.000	
0.000	0.000	0.000	0.000	0.000	4.541	70.392	0.000	0.000	
i0c_p1_add_175_41	increment_unsigned_122	16	74.933	0.000	4.541	70.392	0.000	0.000	
0.000	0.000	0.000	0.000	0.000	4.541	70.392	0.000	0.000	
i0c_p2_add_175_41	increment_unsigned_142	16	74.933	0.000	4.541	70.392	0.000	0.000	
0.000	0.000	0.000	0.000	0.000	4.541	70.392	0.000	0.000	
i0c_p3_add_175_41	increment_unsigned_162	16	74.933	0.000	4.541	70.392	0.000	0.000	
0.000	0.000	0.000	0.000	0.000	4.541	70.392	0.000	0.000	
m0	master	1098	6345.850	9.083	358.771	4054.713	1923.283	0.000	
0.000	0.000	0.000	0.000	0.000	4.541	70.392	0.000	0.000	
r0	router	231	1969.454	0.000	63.580	904.495	1081.379	0.000	
0.000	0.000	0.000	0.000	0.000	4.541	70.392	0.000	0.000	
r1	router_355	228	1997.459	0.000	56.767	912.865	1028.627	0.000	
0.000	0.000	0.000	0.000	0.000	4.541	70.392	0.000	0.000	
r2	router_354	227	1966.371	0.000	54.497	904.495	1081.379	0.000	
0.000	0.000	0.000	0.000	0.000	54.497	905.252	1081.379	0.000	
r3	router_353	227	1961.128	0.000	54.497	905.252	1081.379	0.000	
0.000	0.000	0.000	0.000	0.000	54.497	905.252	1081.379	0.000	

Area of standard cells : 22293.733  $\mu\text{m}^2$

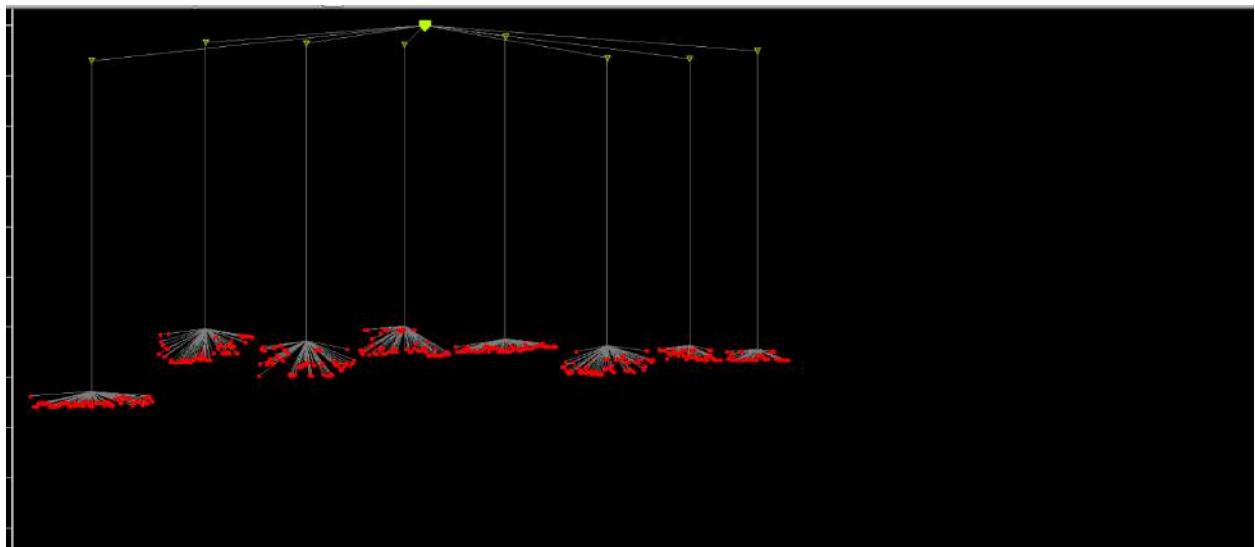
Area of Buffers : 211.932  $\mu\text{m}^2$

Area of Inverters : 626.713  $\mu\text{m}^2$

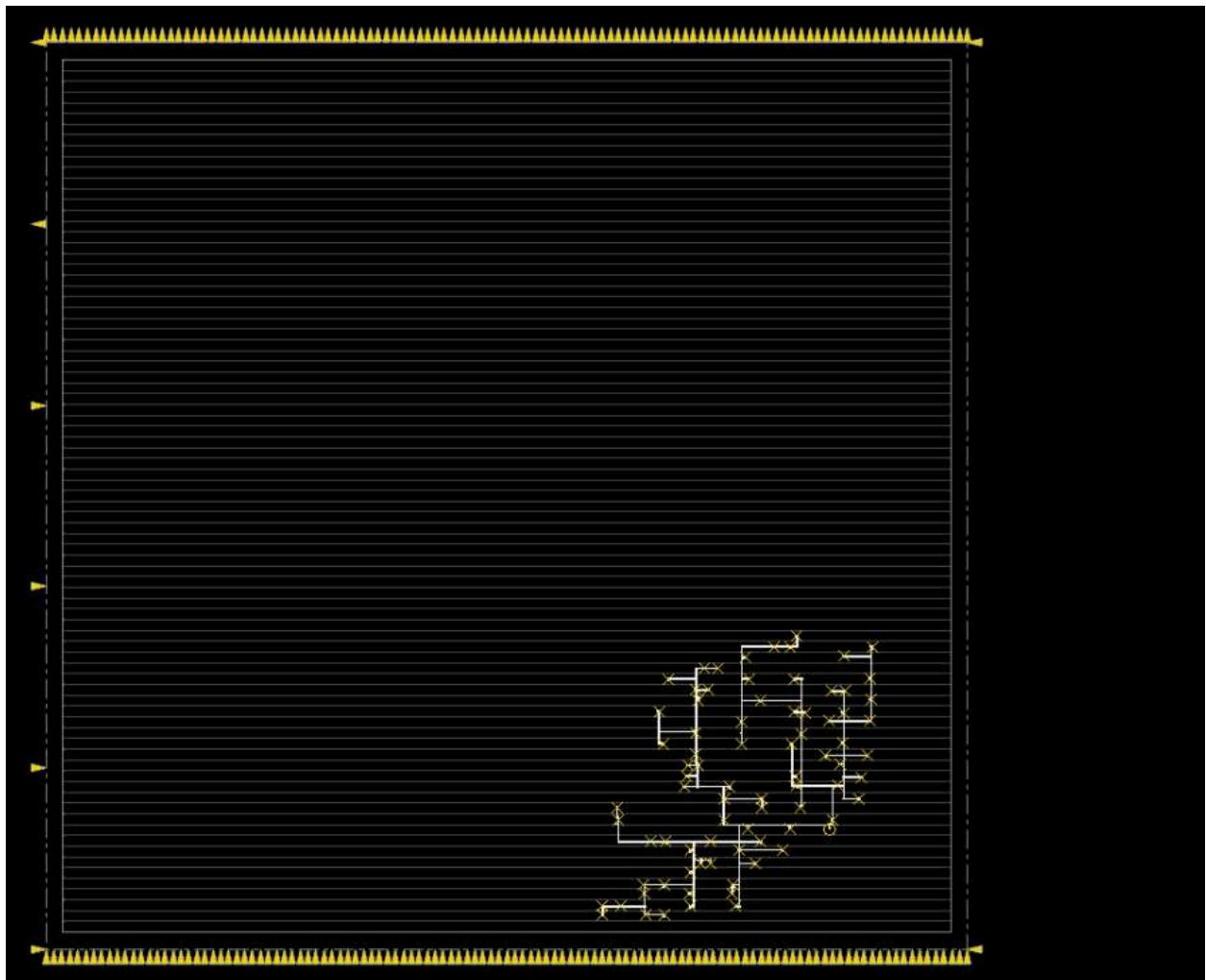
Area of Combinational: 8790.637  $\mu\text{m}^2$

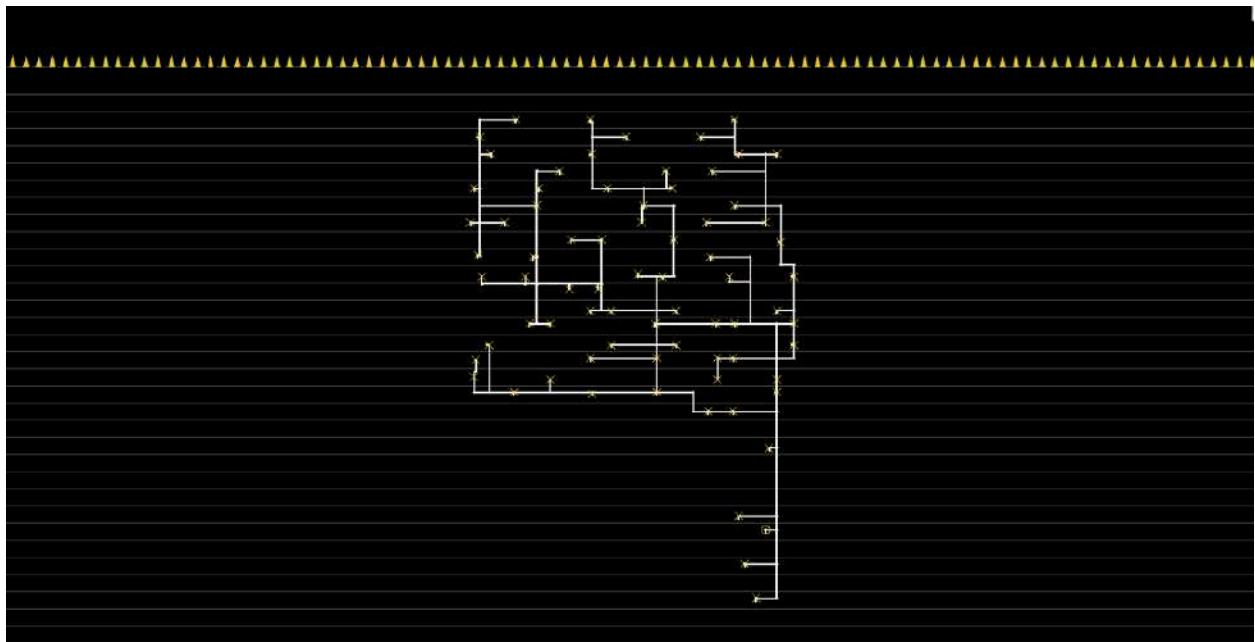
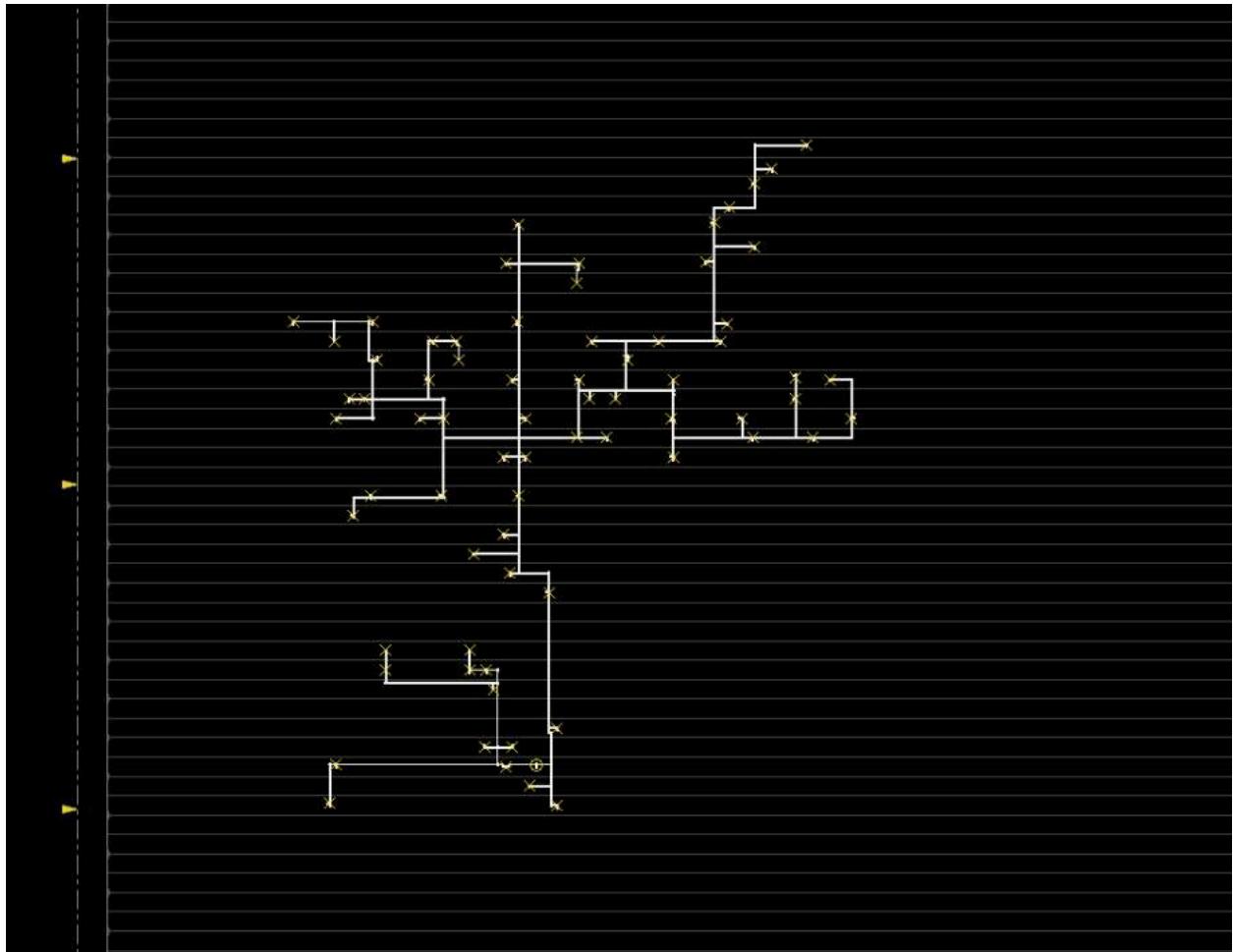
Area of flip-flops :  $12606.926 \mu m^2$  (SDFFHQX1 + SDFFQX1)

Clock Tree:-



After Clock Tree Synthesis:-





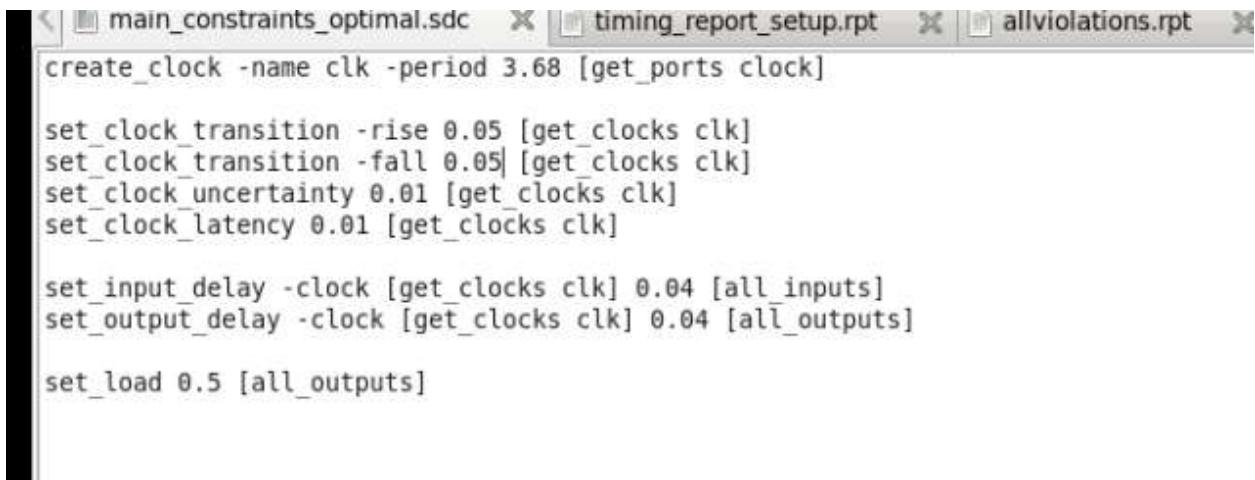
## Layout Design Core Utilization:- 0.8

TCL file:

DoCTS.tcl:

```
set ccopt_mode -cts buffer_cells {CLKBUFX12 CLKBUFX16 CLKBUFX2 CLKBUFX20 CLKBUFX3 CLKBUFX4 CLKBUFX6 CLKBUFX8 CLKINVX1 CLKINVX12 CLKINVX16 CLKINVX2 CLKINVX20 CLKINVX3 CLKINVX4 CLKINVX6 CLKINVX8} -  
cts_opt_priority all  
create_copt_clock_tree_spec -file file_cts.spec -keep_all_sdc_clocks -views {view1}  
  
source file_cts.spec  
ccopt_design -check_prerequisites  
ccopt_design  
optDesign -postCTS -setup  
optDesign -postCTS -hold; #for hold violation  
  
#/Power Analysis/  
  
set power_analysis mode -reset  
set power_analysis mode -method static -analysis_view view1 -corner max -create_binary_db true -write_static_currents true -honor_negative_energy true -ignore_control_signals true  
set power_output_dir -reset  
set power_output_dir ..../Physical_Design_scripts/PostCTSPowerRPT  
set default_switching_activity -reset  
set default_switching_activity -input_activity 0.2 -period 10.0  
read_activity_file -reset  
set power -reset  
set powerup_analysis -reset  
  
set_dynamic_power_simulation -reset  
report_power -rail_analysis_format V5 -outfile ..../Physical_Design_scripts/PostCTSPowerRPT/rtl_module_post_cts.rpt  
  
# Area  
summaryReport -outdir ..../Physical_Design_scripts/postCTSArea -noHtml  
report_area -detail -show_leaf_cells -table_style {vertical}  
  
setAnalysisMode -checkType setup  
report_timing -check_type setup > ..../Physical_Design_scripts/TimingReports/setup_analysis_after_CTS.rpt  
  
setAnalysisMode -checkType hold  
report_timing -check_type hold > ..../Physical_Design_scripts/TimingReports/hold_analysis_after_CTS.rpt  
report_area > ..../Physical_Design_scripts/postCTSArea/Area_report.rpt
```

Constraints used:



```
main_constraints_optimal.sdc  X timing_report_setup.rpt  X allviolations.rpt  X  
  
create_clock -name clk -period 3.68 [get_ports clock]  
  
set_clock_transition -rise 0.05 [get_clocks clk]  
set_clock_transition -fall 0.05 [get_clocks clk]  
set_clock_uncertainty 0.01 [get_clocks clk]  
set_clock_latency 0.01 [get_clocks clk]  
  
set_input_delay -clock [get_clocks clk] 0.04 [all_inputs]  
set_output_delay -clock [get_clocks clk] 0.04 [all_outputs]  
  
set_load 0.5 [all_outputs]
```

Timing Reports:

## Setup Analysis:-

```

#####
# Generated by: Cadence Innovus 20.10-p064.1
# OS: Linux x86_64/Host ID edaserver4
# Generated on: Wed Apr 17 18:01:07 2024
# Design: mesh
# Command: report timing -check type setup > ./Physical_Design_Scripts2/TimingReports/setup_analysis_after_CTS.rpt
#####

Path 1: MET Setup Check with Pin m0/R3_control_signals2_reg[1]/QK
Endpoint: m0/R3_control_signals2_reg[1]/D (^) checked with leading edge of
`clk'
Beginpoint: p0_configure1_reg[0] (^) triggered by leading edge of
`clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time 0.013
- Setup 0.123
+ Phase Shift 3.680
- Uncertainty 0.010
= Required Time 3.560
- Arrival Time 3.535
= Slack Time 0.025
Clock Rise Edge 0.000
+ Clock Network Latency (Prop) 0.014
= Beginpoint Arrival Time 0.014

| Instance | Arc | Cell | Delay | Arrival Time | Required Time | |
|---|---|---|---|---|---|---|
| p0_configure1_reg[0] | CK ^ -> Q | SDFFQX1 | 0.090 | 0.104 | 0.129 |
| p0_configure1_reg[0] | CK ^ -> Y v | CLKINVX1 | 0.039 | 0.143 | 0.168 |
| q45 | A ^ -> Y v | NAND2XL | 0.354 | 0.477 | 0.522 |
| q51 | C v -> Y v | INVX1 | 0.272 | 0.607 | 0.694 |
| m0/FE_DBTC14_P0_signals_1 | B v -> Y ^ | NAND2XL | 0.461 | 1.330 | 1.355 |
| m0/g15886 | m0/g15828 | A ^ -> Y v | CLKINVX1 | 0.231 | 1.560 | 1.586 |
| m0/g15326 | B0 v -> Y ^ | AD121X1 | 0.099 | 1.650 | 1.676 |
| m0/g15338 | B ^ -> Y v | NAND2XL | 0.031 | 1.681 | 1.706 |
| m0/g15066 | A0 v -> Y ^ | AD121X1 | 0.036 | 1.717 | 1.742 |
| m0/g15842 | B ^ -> Y v | NAND2XL | 0.025 | 1.742 | 1.767 |
| m0/g15019 | A v -> Y ^ | NOR2XL | 0.118 | 1.860 | 1.885 |
| m0/g15318 | A ^ -> Y v | NAND2XL | 0.187 | 2.037 | 2.073 |
| m0/foot16569 | A ^ -> Y v | CLKINVX1 | 0.237 | 2.593 | 2.616 |
| m0/g1934 | A1 ^ -> Y v | AD121X1 | 0.035 | 2.620 | 2.645 |
| m0/g14889 | A1 v -> Y v | OA1211X1 | 0.067 | 2.687 | 2.712 |
| m0/g14875 | B ^ -> Y v | NOR2XL | 0.036 | 2.718 | 2.743 |
| m0/g14871 | B v -> Y ^ | NAND2XL | 0.037 | 2.754 | 2.780 |
| m0/FE_OFCl4_n_968 | A ^ -> Y ^ | BUF2X | 0.328 | 3.074 | 3.099 |
| m0/g14761 | A1 ^ -> Y v | OA121X1 | -0.006 | 3.074 | 3.099 |
| m0/g14729 | B v -> Y ^ | NAND2XL | 0.047 | 3.121 | 3.146 |
| m0/g14708 | A ^ -> Y v | NAND3XL | 0.028 | 3.141 | 3.166 |
| m0/g14704 | B v -> Y ^ | NOR2XL | 0.031 | 3.141 | 3.167 |
| m0/g14782 | A ^ -> Y v | AN02X4 | 0.143 | 3.325 | 3.350 |
| m0/g14791 | A ^ -> Y v | CLKINVX4 | 0.106 | 3.431 | 3.457 |
| m0/g14597 | A1 v -> Y ^ | OA121X1 | 0.183 | 3.534 | 3.560 |
| m0/R3_control_signals2_reg[1] | D ^ | SDFFRHDX1 | 0.000 | 3.533 | 3.560 |

Path 1: MET Setup Check with Pin m0/R3_control_signals2_reg[1]/CK
Endpoint: m0/R3_control_signals2_reg[1]/D (^) checked with leading edge of
`clk'
Beginpoint: p0_configure1_reg[0] (^) triggered by leading edge of
`clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time 0.013
- Setup 0.123
+ Phase Shift 3.680
- Uncertainty 0.010
= Required Time 3.560
- Arrival Time 3.535
= Slack Time 0.025
Clock Rise Edge 0.000
+ Clock Network Latency (Prop) 0.014
= Beginpoint Arrival Time 0.014

| Instance | Arc | Cell | Delay | Arrival Time | Required Time | |
|---|---|---|---|---|---|---|
| p0_configure1_reg[0] | CK ^ -> Q | SDFFQX1 | 0.090 | 0.104 | 0.129 |
| p0_configure1_reg[0] | CK ^ -> Y v | CLKINVX1 | 0.039 | 0.143 | 0.168 |
| q45 | A ^ -> Y v | NAND2XL | 0.354 | 0.497 | 0.522 |
| q51 | C v -> Y v | INVX1 | 0.287 | 2.847 | 2.973 |
| m0/FE_DBTC14_P0_signals_1 | B v -> Y ^ | NAND2XL | 0.461 | 1.330 | 1.355 |
| m0/g15886 | m0/g15828 | A ^ -> Y v | CLKINVX1 | 0.231 | 1.560 | 1.586 |
| m0/g15326 | B0 v -> Y ^ | AD121X1 | 0.099 | 1.650 | 1.676 |
| m0/g15338 | B ^ -> Y v | NAND2XL | 0.031 | 1.681 | 1.706 |
| m0/g15066 | A0 v -> Y ^ | AD121X1 | 0.036 | 1.717 | 1.742 |
| m0/g15842 | B ^ -> Y v | NAND2XL | 0.025 | 1.742 | 1.767 |
| m0/g15019 | A v -> Y ^ | NOR2XL | 0.118 | 1.860 | 1.885 |
| m0/g15318 | A ^ -> Y v | NAND2XL | 0.187 | 2.037 | 2.073 |
| m0/foot16569 | A ^ -> Y v | CLKINVX1 | 0.237 | 2.593 | 2.616 |
| m0/g1934 | A1 ^ -> Y v | AD121X1 | 0.035 | 2.620 | 2.645 |
| m0/g14889 | A1 v -> Y v | OA1211X1 | 0.067 | 2.687 | 2.712 |
| m0/g14875 | B ^ -> Y v | NOR2XL | 0.036 | 2.718 | 2.743 |
| m0/g14871 | B v -> Y ^ | NAND2XL | 0.037 | 2.754 | 2.780 |
| m0/FE_OFCl4_n_968 | A ^ -> Y ^ | BUF2X | 0.328 | 3.074 | 3.099 |
| m0/g14761 | A1 ^ -> Y v | OA121X1 | -0.006 | 3.074 | 3.099 |
| m0/g14729 | B v -> Y ^ | NAND2XL | 0.047 | 3.121 | 3.146 |
| m0/g14708 | A ^ -> Y v | NAND3XL | 0.028 | 3.141 | 3.166 |
| m0/g14704 | B v -> Y ^ | NOR2XL | 0.031 | 3.141 | 3.167 |
| m0/g14782 | A ^ -> Y v | AN02X4 | 0.143 | 3.325 | 3.350 |
| m0/g14791 | A ^ -> Y v | CLKINVX4 | 0.106 | 3.431 | 3.457 |
| m0/g14597 | A1 v -> Y ^ | OA121X1 | 0.183 | 3.534 | 3.560 |
| m0/R3_control_signals2_reg[1] | D ^ | SDFFRHDX1 | 0.000 | 3.533 | 3.560 |

```

In this timing report it shows the critical path of all the paths present in the circuit. The critical path starts from p0\_configure1\_reg[0]/Q and ends at m0/R3\_control\_signals2\_reg[1] /D that is at the D pin of the Flip Flop.

## Arrival Time Computation:-

Starting from the already computed arrival time (other end arrival time) 0.014 ns at beginpoint reset and traversing to the end point through different cells with experiencing different delays are added up. So subsequent vertices arrival time is calculated by adding up the already computed arrival time. Finally, from the above timing report we can infer that AT at the end point is 3.535 ns.

#### Required Time Computation:-

Here in the above timing report RT is computed as other end arrival time (0.013 ns) + Phase Shift (3.680ns , clock period) – setup (0.123 ns, time required by the clock to setup) - uncertainty (0.010 ns). Required Time (RT) at the endpoint evaluates to 3.560 ns.

$$\text{Slack} = \text{Required Time} - \text{Arrival Time} = 0.025 \text{ ns.}$$

#### Hold Analysis:-

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64 (Host ID edaserver4)
# Generated on: Wed Apr 17 18:01:07 2024
# Design: mesh
# Command: report timing -check type hold > ../../Physical_Design_Scripts2/TimingReports/hold_analysis_after_CTS.rpt
#####
Path 1: MET Hold Check with Pin p0_configure1_reg[1]/D
Endpoints: p0_configure1_reg[1]/D (^) checked with leading edge of 'clk'
Beginpoint: p0_configure[1] (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time      0.012
+ Hold                      0.006
+ Phase Shift                0.000
+ Uncertainty                0.010
= Required Time              0.028
Arrival Time                 0.050
Slack Time                  0.022
Clock Rise Edge              0.000
+ Input Delay                0.040
+ Network Insertion Delay    0.010
= Beginpoint Arrival Time   0.050
+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          | p0_configure[1] ^ | SDFQX1 | 0.000 | 0.050 | 0.028 |
| p0_configure1_reg[1] | D ^ |          |        | 0.050 | 0.028 |
+
```

In this timing report it shows the critical path of all the paths present in the circuit. The critical path starts from p0\_configure[1] and ends at p0\_configure1\_reg[1] / D that is at the D pin of the Flip Flop.

#### Arrival Time Computation:-

Starting from the already computed arrival time (other end arrival time) 0.050 ns at beginpoint reset and traversing to the end point through different cells with experiencing different delays

are added up. So subsequent vertices arrival time is calculated by adding up the already computed arrival time. Finally, from the above timing report we can infer that AT at the end point is 0.050 ns. In this case the path is from p0\_configure[1] to p0\_configure1\_reg[1] / D which is the D pin of the first flop SDFFQX1.

#### Required Time Computation:-

Here in the above timing report RT is computed as other end arrival time (0.012 ns). clock + hold (0.006 ns, time required by the clock to setup) + uncertainty (0.010 ns). Required Time (RT) at the endpoint evaluates to 0.028 ns.

$$\text{Slack} = \text{Arrival Time} - \text{Required Time} = 0.050 - 0.028 = 0.022\text{ns.}$$

#### Power Report:

```

Innovus 20.10-p064_1 (64bit) 05/07/2020 28:02 (Linux 2.6.32-431.11.2.el6.x86_64)
Date & Time: 2024-Apr-17 18:01:06 (2024-Apr-17 12:31:06 GMT)

Design: mesh
Liberty Libraries used:
    view1: /home/rajat21186/Desktop/New_VDF_Project/library/fast.lib
Power Domain used:
Power View : view1
User-Defined Activity : N.A.
Activity File: N.A.
Hierarchical Global Activity: N.A.
Global Activity: N.A.
Sequential Element Activity: N.A.
Primary Input Activity: 0.200000
Default icg ratio: N.A.
Global Comb ClockGate Ratio: N.A.
Power Units = 1mW
Time Units = 1e-09 secs
Temperature = 0
report_power -outfile ../../Physical_Design_Scripts2/PostCTS_PowerRPT/rtl_module_post_cts.rpt -rail_analysis_format VS

Cell          Internal Power   Switching Power   Total Power   Leakage Power   Cell Name
-----+-----+-----+-----+-----+-----+-----+
r3_output2_reg[17]      0.02147  0.1627  0.1845  0.0004846  SDFFQX4
C15_ccl_a_buf_00013     0.05582  0.08063  0.1369  0.0004104  CLKBUFX16
C15_ccl_a_buf_00015     0.0554   0.07883  0.1346  0.0004104  CLKBUFX16
C15_ccl_a_buf_00021     0.05585  0.0673   0.1236  0.0004104  CLKBUFX16
C15_ccl_a_buf_00017     0.05542  0.06705  0.1229  0.0004104  CLKBUFX16

```

```

    CTS_LCL_A_WU_WO23 0.0234 0.0102 0.1236 0.000409 CLKBUFX16
    CTS_ccl_a_buf_0021 0.05585 0.0673 0.1236 0.000410 CLKBUFX16
    CTS_ccl_a_buf_0017 0.05542 0.06705 0.1229 0.000410 CLKBUFX16
    p3_data_gotl_reg[3] 0.01772 0.08358 0.1016 0.000299 SDFF0X2
    p3_data_gotl_reg[9] 0.01744 0.08379 0.1015 0.000299 SDFF0X2
    p3_data_gotl_reg[1] 0.01752 0.08366 0.1015 0.000299 SDFF0X2
    r3_output2_reg[10] 0.01795 0.08312 0.1014 0.000299 SDFF0X2
    r0_output2_Reg[9] 0.0173 0.08366 0.1013 0.000299 SDFF0X2
    r3_output2_Reg[11] 0.01769 0.08326 0.1013 0.000299 SDFF0X2
    r1_output2_Reg[5] 0.0178 0.08311 0.1012 0.000299 SDFF0X2
    r3_output2_Reg[6] 0.01777 0.08308 0.1012 0.000299 SDFF0X2
    r3_output2_Reg[8] 0.01792 0.08292 0.1012 0.000299 SDFF0X2
    r3_output2_Reg[12] 0.01756 0.08528 0.1011 0.000299 SDFF0X2
    r1_output2_Reg[12] 0.01756 0.08528 0.1011 0.000299 SDFF0X2
    r1_output2_Reg[13] 0.01758 0.08311 0.101 0.000299 SDFF0X2
    r3_output2_Reg[15] 0.01798 0.08311 0.101 0.000299 SDFF0X2
    r3_output2_Reg[14] 0.01791 0.08279 0.101 0.000299 SDFF0X2
    p3_data_gotl_Reg[6] 0.01731 0.08238 0.1009 0.000299 SDFF0X2
    r1_output2_Reg[17] 0.01768 0.08291 0.1009 0.000299 SDFF0X2
    r1_output2_Reg[6] 0.01747 0.08309 0.1009 0.000299 SDFF0X2
    r3_output2_Reg[15] 0.01763 0.08292 0.1009 0.000299 SDFF0X2
    r3_output2_Reg[14] 0.01739 0.08313 0.1008 0.000299 SDFF0X2
    r3_output2_Reg[9] 0.01775 0.08274 0.1008 0.000299 SDFF0X2
    r1_output2_Reg[11] 0.01762 0.08286 0.1008 0.000299 SDFF0X2
    r3_output2_Reg[16] 0.01775 0.08272 0.1008 0.000299 SDFF0X2
    r1_output2_Reg[1] 0.0173 0.08309 0.1007 0.000299 SDFF0X2
    r1_output2_Reg[16] 0.01752 0.08284 0.1007 0.000299 SDFF0X2
    r1_output2_Reg[10] 0.01745 0.08287 0.1006 0.000299 SDFF0X2
    r3_output2_Reg[8] 0.01764 0.08258 0.1005 0.000299 SDFF0X2
    r0_output2_Reg[3] 0.01734 0.08273 0.1004 0.000299 SDFF0X2
    r3_output2_Reg[14] 0.01735 0.08271 0.1004 0.000299 SDFF0X2
    r3_output2_Reg[11] 0.01741 0.08255 0.1003 0.000299 SDFF0X2
    r1_output2_Reg[13] 0.01732 0.08263 0.1002 0.000299 SDFF0X2
    r1_output2_Reg[2] 0.01728 0.08263 0.1002 0.000299 SDFF0X2
    p2_data_gotl_Reg[2] 0.01695 0.08272 0.09997 0.000299 SDFF0X2
    r3_output2_Reg[1] 0.01754 0.08221 0.09994 0.000299 SDFF0X2
    r1_output2_Reg[6] 0.01738 0.08224 0.09991 0.000299 SDFF0X2
    r3_output2_Reg[7] 0.01757 0.08189 0.09976 0.000299 SDFF0X2
    r1_output2_Reg[7] 0.01739 0.08203 0.09972 0.000299 SDFF0X2
    p3_data_gotl_Reg[2] 0.01725 0.08021 0.09965 0.000299 SDFF0X2
    p3_data_gotl_Reg[4] 0.01756 0.08016 0.09981 0.000299 SDFF0X2
    r1_output2_Reg[8] 0.01725 0.08017 0.09982 0.000299 SDFF0X2
    r1_output2_Reg[9] 0.01787 0.080881 0.09981 0.000299 SDFF0X2
    r3_output2_Reg[2] 0.01739 0.08004 0.09809 0.000299 SDFF0X2
    r0_output2_Reg[12] 0.01709 0.08065 0.09804 0.000299 SDFF0X2
    r3_output2_Reg[3] 0.01627 0.08145 0.09801 0.000299 SDFF0X2
    r0_output2_Reg[14] 0.01699 0.08069 0.09794 0.000299 SDFF0X2
    r1_output2_Reg[17] 0.01795 0.080844 0.09779 0.000299 SDFF0X2
    r3_output2_Reg[5] 0.01714 0.080807 0.09777 0.000299 SDFF0X2
    r0_output2_Reg[1] 0.01685 0.080838 0.09753 0.000299 SDFF0X2
    r0_output2_Reg[1] 0.01717 0.080804 0.09751 0.000299 SDFF0X2

```

Detailed Power Consumption Breakdown						
	Total Power	VDDQ Power	VDDA Power	VSSQ Power	VSSA Power	Other Power
m0/g15155	8.145e-05	3.653e-05	0.000139	2.697e-05	MAND2XL	
g1165	7.140e-05	4.117e-05	0.0001337	2.103e-05	NAND4XL	
m0/g16127	4.122e-05	1.733e-05	0.0001311	2.756e-05	NAND2BX1	
m0/g15473	5.691e-05	3.349e-05	0.0001257	3.532e-05	NOR2XL	
inc_p2_add_175_41/g94	5.583e-05	2.659e-05	0.0001256	4.322e-05	AND3XL	
i1183	6.297e-05	4.127e-05	0.0001253	2.103e-05	MAND4XL	
m0/g14189	5.741e-05	3.694e-05	0.0001253	4.852e-05	AO121XL	
i1184	5.674e-05	3.269e-05	0.0001251	3.892e-05	NOR2XL	
m0/g15438	3.674e-05	3.050e-05	0.0001141	2.182e-05	MAND4XL	
m0/g15413	4.407e-05	3.856e-05	0.0001099	3.532e-05	NOR2XL	
m0/g15153	5.237e-05	2.587e-05	9.509e-05	2.085e-05	0A121XL	
m0/g15451	4.907e-05	2.863e-05	9.867e-05	2.097e-05	NAND2XL	
g1098	1.488e-05	6.622e-05	9.607e-05	2.097e-05	NAND2XL	
m0/g15468	3.834e-05	1.988e-05	9.354e-05	3.532e-05	NOR2XL	
m0/g15468	2.572e-05	4.597e-05	9.266e-05	2.097e-05	NAND2XL	
inc_p2_add_175_41/g95	2.161e-05	4.973e-05	9.232e-05	2.097e-05	NAND2XL	
m0/g15440	1.711e-05	3.517e-05	8.759e-05	3.532e-05	NOR2XL	
m0/g15154	3.563e-05	2.876e-05	8.536e-05	2.097e-05	NAND2XL	
inc_p1_add_175_41/g95	1.945e-05	4.477e-05	8.526e-05	2.097e-05	NAND2XL	
m0/g14971	3.010e-05	2.101e-05	8.402e-05	2.097e-05	AO121XL	
i1185	2.220e-05	8.112e-06	8.359e-05	4.322e-05	AND3XL	
inc_p2_add_175_41/g94	2.101e-05	8.407e-06	7.338e-05	4.322e-05	AND3XL	
m0/g15464	2.898e-05	2.102e-05	7.090e-05	2.097e-05	NAND2XL	
inc_p0_add_175_41/g98	1.463e-05	3.056e-05	6.616e-05	2.097e-05	NAND2XL	
m0/g15259	1.365e-05	2.318e-06	6.512e-05	4.916e-05	AO121XL	
m0/g15466	1.943e-05	2.371e-05	6.411e-05	2.097e-05	NAND2XL	
m0/g15441	1.324e-05	2.551e-05	5.972e-05	2.097e-05	NAND2XL	
g1099	1.595e-05	7.016e-06	5.823e-05	3.532e-05	NOR2XL	
m0/g14673	1.387e-05	5.535e-06	5.472e-05	3.532e-05	NOR2XL	
g1095	1.231e-05	5.154e-06	5.278e-05	3.532e-05	NOR2XL	
m0/g14983	2.009e-05	5.889e-06	4.69e-05	2.097e-05	NAND2XL	
m0/g15453	1.43e-05	8.953e-06	4.423e-05	2.097e-05	NAND2XL	
inc_p1_add_175_41/g96	7.059e-06	1.554e-05	4.301e-05	2.097e-05	NAND2XL	
m0/g15477	1.644e-05	7.531e-06	4.135e-05	2.928e-05	AO121XL	
m0/g15410	9.250e-06	7.531e-06	3.871e-05	2.928e-05	NAND2XL	
m0/g15393	4.359e-06	1.681e-06	3.552e-05	2.925e-05	CLKINVX1	
m0/g15442	5.118e-06	3.984e-06	3e-05	2.097e-05	NAND2XL	
inc_p1_add_175_41/g98	2.036e-05	5.876e-06	2.949e-05	2.097e-05	NAND2XL	
m0/g15444	4.254e-06	3.662e-06	2.889e-05	2.097e-05	NAND2XL	
inc_p2_add_175_41/g98	2.277e-06	4.975e-06	2.823e-05	2.097e-05	NAND2XL	
m0/g15445	3.423e-06	2.995e-06	2.739e-05	2.097e-05	NAND2XL	
m0/g15414	4.509e-06	1.797e-06	2.728e-05	2.097e-05	NAND2XL	
m0/g15457	3.929e-06	1.826e-06	2.673e-05	2.097e-05	NAND2XL	
m0/fopt16284	2.824e-06	1.989e-06	2.578e-05	2.097e-05	INVXL	
air	Total { 2797 of 2797 }	10.7	12.18	23.12	0.2437	
R	Total Capacitance	9.297e-11 F				
Power Density	*** No Die Area ***					

The report is too big to incorporate into the report

In this report, internal power is the power dissipated inside the cell boundary during charging and discharging of existing capacitances. Total Internal Power is 10.7mW

Switching power of driving cell is the power dissipated by charging load capacitance at the output. The total switching power is 12.18mW

Leakage power is generated from the leakage current that flows between VDD and GND when there is no switching. The total leakage power is 0.2437mW

The total power which is the sum of all these is 23.12mW

## Area Report:

# Generated by: Cadence Innovus 20.10 p094_1						
# OS:	Linux x86_64(Host ID edaserver4)					
# Generated on:	Wed Apr 17 10:01:66 2024					
# Design:	mesh					
# Command:	summaryReport -outdir ..\Physical Design Scripts2\postCTSArea -noHTML					
<hr/>						
<b>General Design Information</b>						
Design Status: Routed						
Design Name: mesh						
# Instances: 297						
# Hard Macros: 0						
# Std Cells: 297						
<hr/>						
<b>Standard Cells in Netlist</b>						
<hr/>						
Cell Type	Instance Count	Area (um^2)				
AO12BBLX1	5	26.4915				
AO122XL	1	6.0552				
NAND3X4	1	14.3811				
AO132XL	1	6.8121				
AO12BBLX1L	4	24.2288				
CLKBUFX12	3	47.6847				
BUFX2	15	68.1210				
NOR3BX2	1	9.8397				
CLKXOR2X1	9	74.9331				
TLATNX1	4	57.5244				
OA122XL	1	8.3259				
OR2X1	3	13.6242				
AO12BBLX1	32	193.7664				
AND2X1	53	240.6942				
AO133XL	4	30.2760				
OA1211X1	76	492.6788				
AND3X1	8	48.4416				
SDFFOX1	297	6669.5811				
XNOR2X1	3	24.9777				
MX2X1	21	143.0541				
AND2XL	16	72.6624				
XNOR2XL	4	33.3036				
AO122XL	173	1446.3987				
OA121X1	139	590.2320				
CLKBUFX16	4	84.7728				
OA1221X1	27	294.3630				
OA131X1	4	24.2288				
OA21X1	18	122.6178				
CLKINVX1	234	531.3438				

OA131X1	4	44.2290
OA21X1	18	122.6178
CLKINVX1	234	531.3438
AO1211X1	66	349.6878
NAND2BX1	33	149.8662
OA1211XL	104	551.0232
OA21X1	1	7.1998
CLKINVX4	1	6.0552
XNOR2XL	12	99.9198
NAND3X1	24	188.9530
NAND2XL	334	1811.2184
SDFRHDX1	149	3721.0773
NOR2BX1	23	194.4522
OA122XL	43	260.3736
OA121XL	33	149.8662
OA132XL	6	40.8726
AO121X1	124	563.3336
NOR2XL	2	7.5000
NOR3BX1	37	224.0424
INVXL	16	36.3312
AO1211X1	8	60.5528
AO131X1	9	54.4968
NAND3BX1	6	36.3312
AO21X1	4	27.2484
OA1221XL	34	257.3460
NOR3X1	42	190.7388
AND2X4	1	6.3259
NOR4BX1	1	6.0552
NOR4X1	4	24.2288
AO1211XL	2	16.5966
NAND2BX1	3	13.0242
SDFSHDX1	13	354.2292
INVX1	70	158.9499
OA122XL	25	151.3800
NOR2XL	135	408.7260
SDFFOX4	1	24.9777
DA121X1	2	16.6518
SDFFOX2	111	2436.4111
AO122XL	50	392.7680
OA132XL	7	47.6847
NOR3XL	4	18.1656
AO121XL	4	18.1656
OR3X1	1	6.0552
AO132X1	12	81.7452
OA12BBLX1L	28	148.3524
NAND4XL	10	52.9830
MUX2XL	56	302.7609

# Pads: 0  
# Nets: 2964  
# Special Net: 2

```

Overall XLL SCALE FACTOR: 1.000
=====
Placement Information
=====
Total area of Standard cells: 22293.733 um^2
Total area of Standard cells(Subtracting Physical Cells): 22293.733 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Chip: 45429.695 um^2
Total area of Chip: 46957.363 um^2
Effective Utilization: 4.9673e-01
Number of Cell Rows: 81
% Pure Gate Density #1 (Subtracting BLOCKAGES): 49.073%
% Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 49.073%
% Pure Gate Density #3 (Subtracting MACROS): 49.073%
% Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 49.073%
% Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 49.073%
% Pure Gate Density #6 ((Unreplaced Standard Inst + Unreplaced Block Inst + Unreplaced Black Blob Inst + Fixed Clock Inst Area) / (Free Site Area + Fixed Clock Inst Area) for insts are placed): 49.073%
% Core Density #1(Subtracting Physical Cells): 49.073%
% Core Density #2(Subtracting MACROS and IOs): 49.073%
% Chip Density (Counting Std Cells and MACROS and IOs): 45.537%
% Chip Density #2(Subtracting Physical Cells): 45.537%
# Macros within 5 sites of IO pad: No
Macro halo defined?: No

```

Inst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop	Latch	Clock
Gate	Macro	Physical							
			2797	23228.504	200.578	732.679	9630.796	12606.926	57.524
0.000	0.000	0.000							
inc_p0_add_175_41	increment_unsigned_138	16	74.933	0.000	0.000	74.933	0.000	0.000	0.000
0.000	0.000	0.000							
inc_p1_add_175_41	increment_unsigned_158	16	74.933	0.000	0.000	74.933	0.000	0.000	0.000
0.000	0.000	0.000							
inc_p2_add_175_41	increment_unsigned_178	16	74.933	0.000	0.000	74.933	0.000	0.000	0.000
0.000	0.000	0.000							
inc_p3_add_175_41	increment_unsigned_198	16	74.933	0.000	0.000	74.933	0.000	0.000	0.000
0.000	0.000	0.000							
r0	router	1292	7265.483	4.541	444.300	4893.359	1923.283	0.000	0.000
0.000	0.000	0.000							
r1	router	232	1970.211	0.000	65.850	982.982	1001.379	0.000	0.000
0.000	0.000	0.000							
r2	router_355	229	1990.216	0.000	59.938	910.551	1028.027	0.000	0.000
0.000	0.000	0.000							
r3	router_354	228	1961.128	0.000	56.767	982.982	1001.379	0.000	0.000
0.000	0.000	0.000							
r4	router_353	227	1961.128	0.000	54.497	985.252	1001.379	0.000	0.000
0.000	0.000	0.000							

Area of standard cells :  $23228.504 \mu\text{m}^2$

Area of Buffers :  $200.578 \mu\text{m}^2$

Area of Inverters :  $732.679 \mu\text{m}^2$

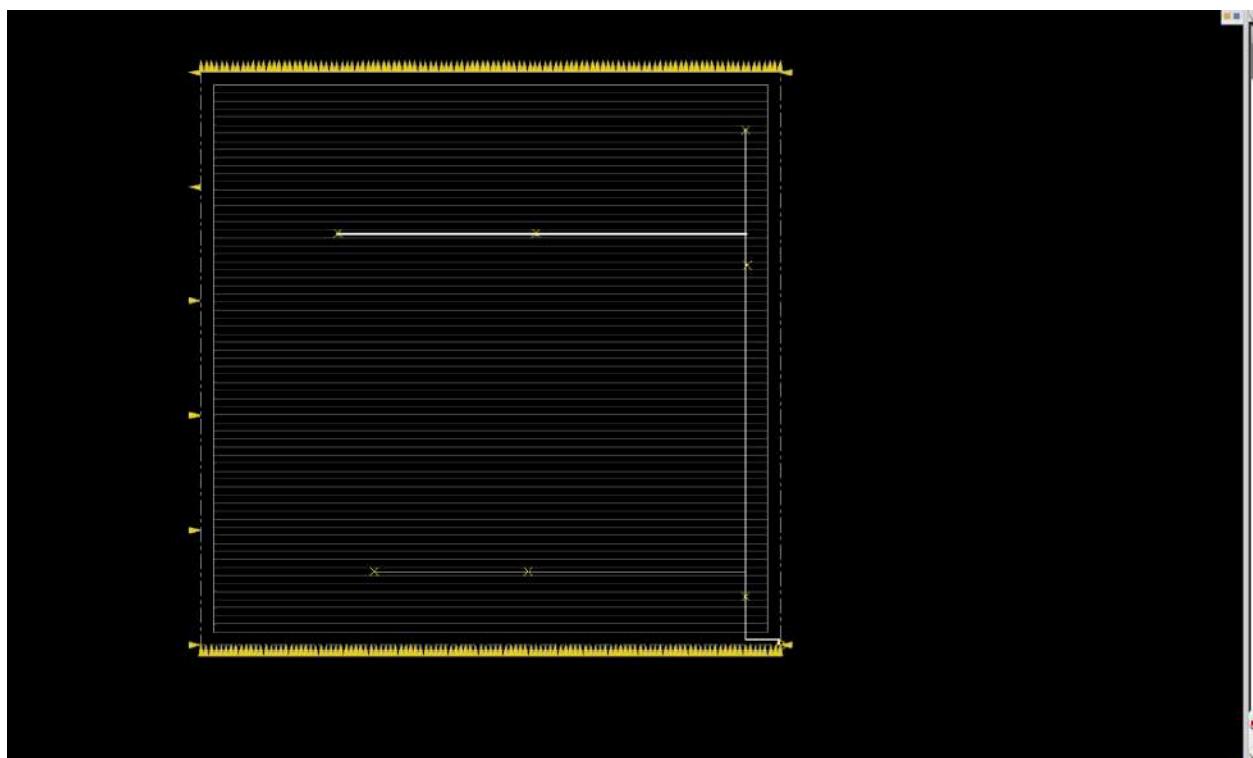
Area of Combinational:  $9630.796 \mu\text{m}^2$

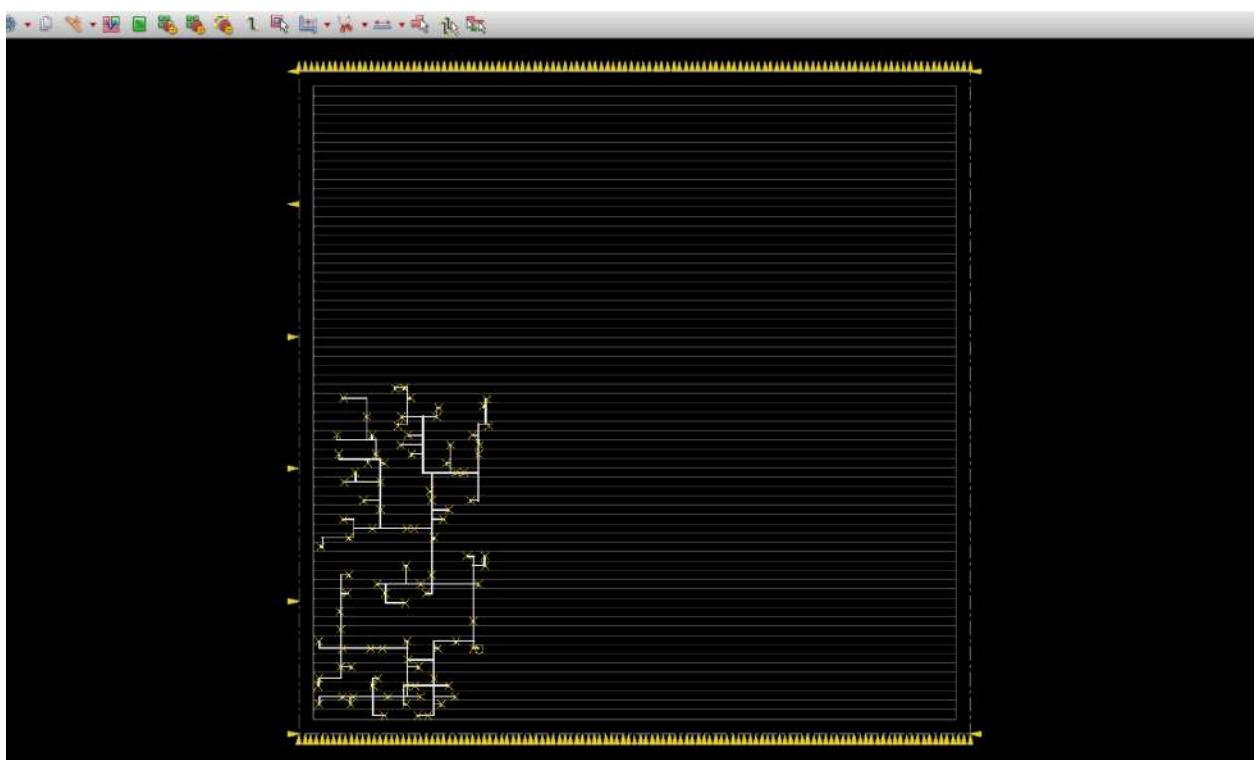
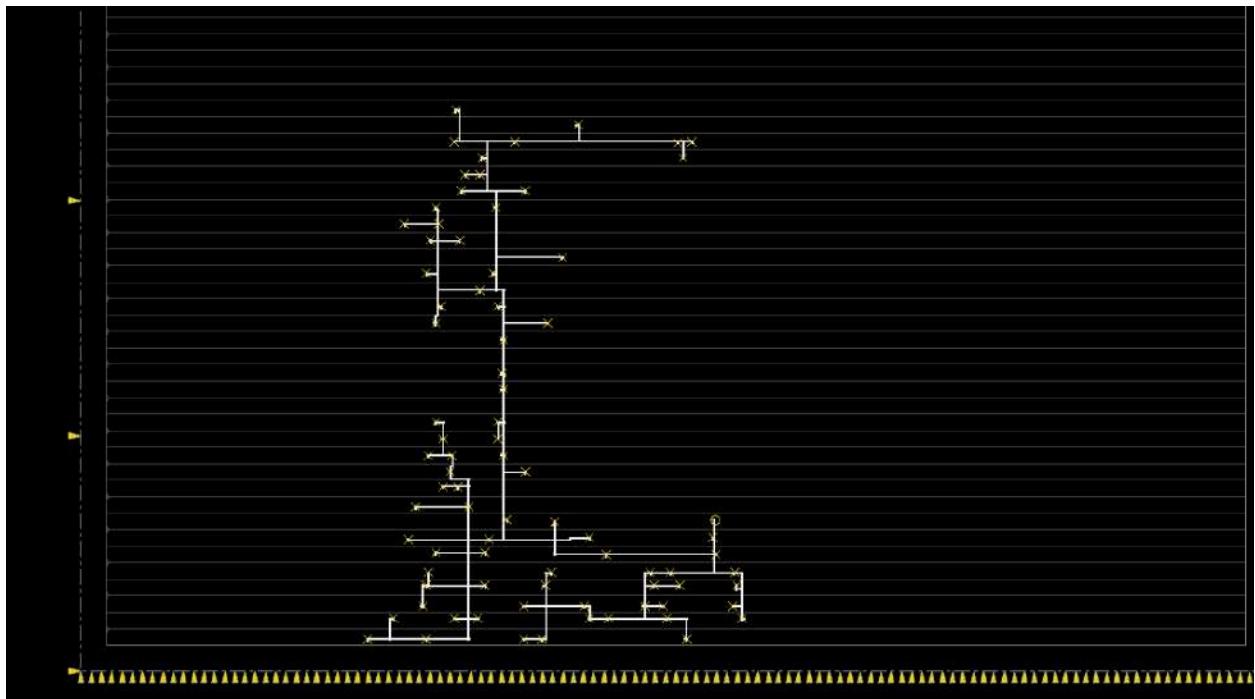
Area of flip-flops :  $12606.926 \mu\text{m}^2$  (SDFFHQX1 + SDFFQX1)

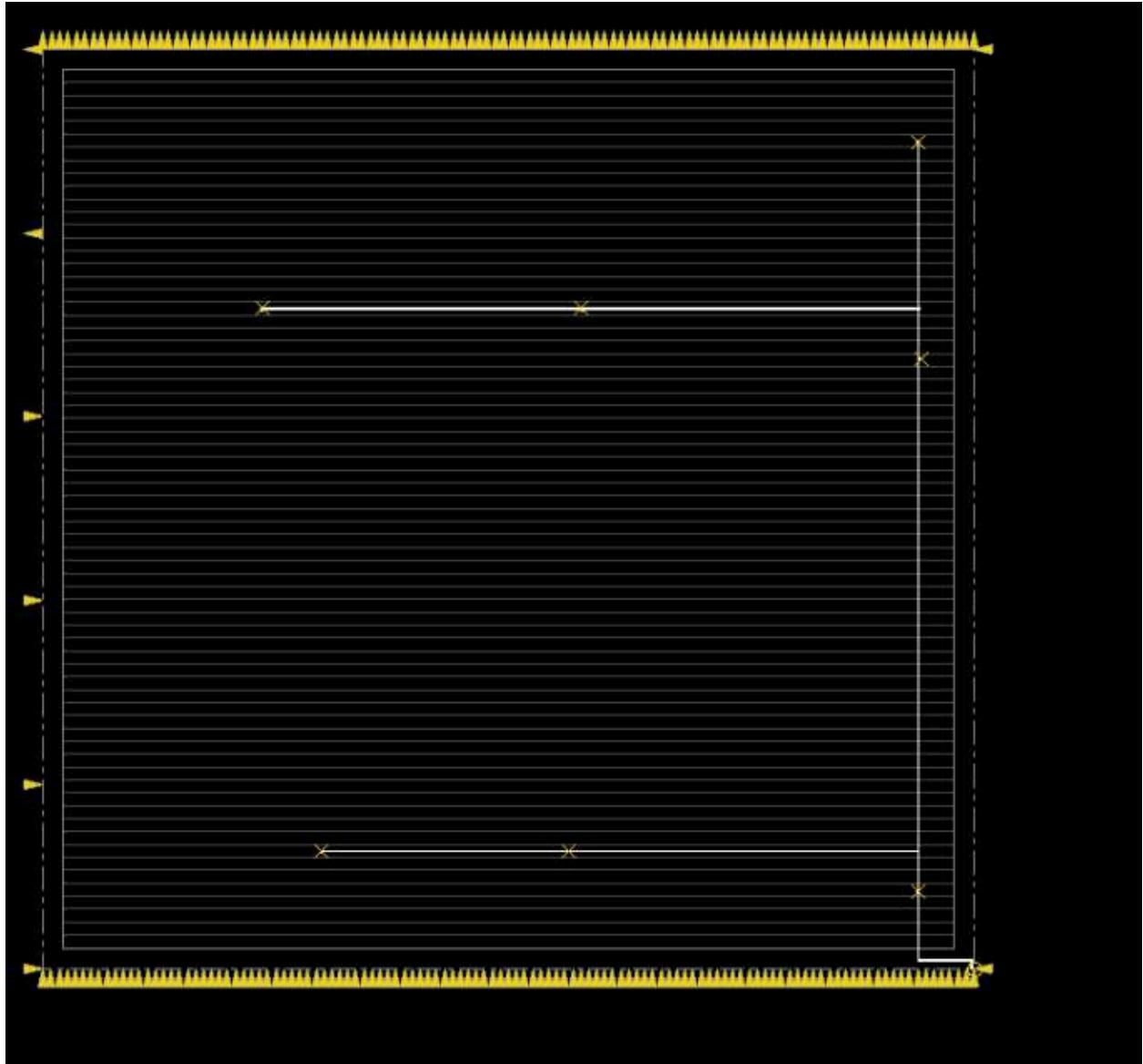
Clock Tree:-



After Clock Tree Synthesis:-







### Effect of clock path on overall timing slack

After doing CTS, our clock will have additional buffers and delay elements in path and inputs. Because of this additional delays, hold slack raises after CTS. These delays consequently also increase the setup time, reducing the setup slack.

## 4.After Detailed Routing

Software Used:

Cadence Innovus

Commands Used:

1. csh
2. source /cadence/cshrc
3. innovus
4. source (tcl file)

Layout Design Core Utilization:- 0.5

TCL file:

DoRoute.tcl

```
#Global & Detail Routing/
setNanoRouteMode -quiet -timingEngine {}
setNanoRouteMode -quiet -routeWithTimingDriven
setNanoRouteMode -quiet -drouteStartIteration default
setNanoRouteMode -quiet -routeTopRoutingLayer default
setNanoRouteMode -quiet -routeBottomRoutingLayer default
setNanoRouteMode -quiet -drouteEndIteration default
setNanoRouteMode -quiet -routeWithTimingDriven false
setNanoRouteMode -quiet -routeWithSISDriven false
routeDesign -globalDetail -wireOpt

# Timing Report
# optDesign -postRoute
# optDesign -postRoute -hold

extractRC
rcOut -spf ..//Physical_Design_scripts/rtl_module.spf

#Writing SDF file with interconnect and gates delay
write_sdf -ideal_clock_network ..//Physical_Design_scripts/physical_design_rtl_module.sdf

#Generating gate count report/
#summaryReport -outdir summaryReport
reportGateCount -level 5 -limit 100 -outfile ..//Physical_Design_scripts/rtl_module.gateCount

setAnalysisMode -analysisType onChipVariation
optDesign -postRoute
optDesign -postRoute -hold

#Power Analysis/
set power analysis node -reset
set power analysis node -method static -analysis_view view1 -corner max -create_binary_db true -write_static_currents true -honor_negative_energy true -ignore_control_signals true
set power output dir -reset
set power output dir ..//Physical_Design_scripts/PostRoutingPowerRpt
set default_switching_activity -reset
set_default_switching_activity -input_activity 0.2 -period 10.0
read_activity_file -reset
set_power -reset
set_powerup_analysis -reset
set_dynamic_power_simulation -reset
report_power -rail analysis format VS -outfile ..//Physical_Design_scripts/PostRoutingPowerRpt/rtl_module.rpt

#Generating GDS/
streamOut ..//Physical_Design_scripts/rtl_module.gds -mapFile streamOut.map -libName DesignLib -units 2000 -mode ALL

#/Saving the Design/
saveNetlist ..//Physical_Design_scripts/rtl module post route netlist.v
```

```

extractRC
rcout -spf ./Physical_Design_scripts/rtl_module.spf

<*/Writing SDF file with interconnect and gates delay/>
write_sdf -ideal_clock_network ./Physical_Design_scripts/physical_design_rtl_module.sdf

<*/Generating gate count report/
summaryReport -outdir summaryReport
reportGateCount -level 5 -limit 100 -outfile ./Physical_Design_scripts/rtl_module.gateCount

setAnalysisMode -analysisType onChipVariation
optDesign -postRoute
optDesign -postRoute -hold

<*/Power Analysis/
set power_analysis_mode -reset
set power_analysis_mode -method static -analysis_view view1 -corner max -create_binary_db true -write_static_currents true -honor_negative_energy true -ignore_control_signals true
set power_analysis_dir -reset
set power_output_dir ./Physical_Design_scripts/PostRoutingPowerRpt
set default_switching_activity -reset
set default_switching_activity -input_activity 0.2 -period 10.0
read_activity_file -reset
set power -reset
set powerup_analysis -reset

set dynamic_power_simulation -reset
report_power -rail_analysis_format vs -outfile ./Physical_Design_scripts/PostRoutingPowerRpt/rtl_module.rpt

<*/Generating GDS/
streamOut ./Physical_Design_scripts/rtl_module.gds -mapFile streamOut.map -libName DesignLib -units 2000 -mode ALL

<*/Saving the Design/
saveNetlist ./Physical_Design_scripts/rtl_module_post_route.netlist.v
defout -floorplan -netlist -routing ./Physical_Design_scripts/rtl_module.def
saveDesign ./Physical_Design_scripts/_uptoGDS.enc

verify_drc
verify_connectivity

<*/ Area
summaryReport -outdir ./Physical_Design_scripts/postRouteArea -noHTML
report_area -detail -show_leaf_cells -table_style {vertical}

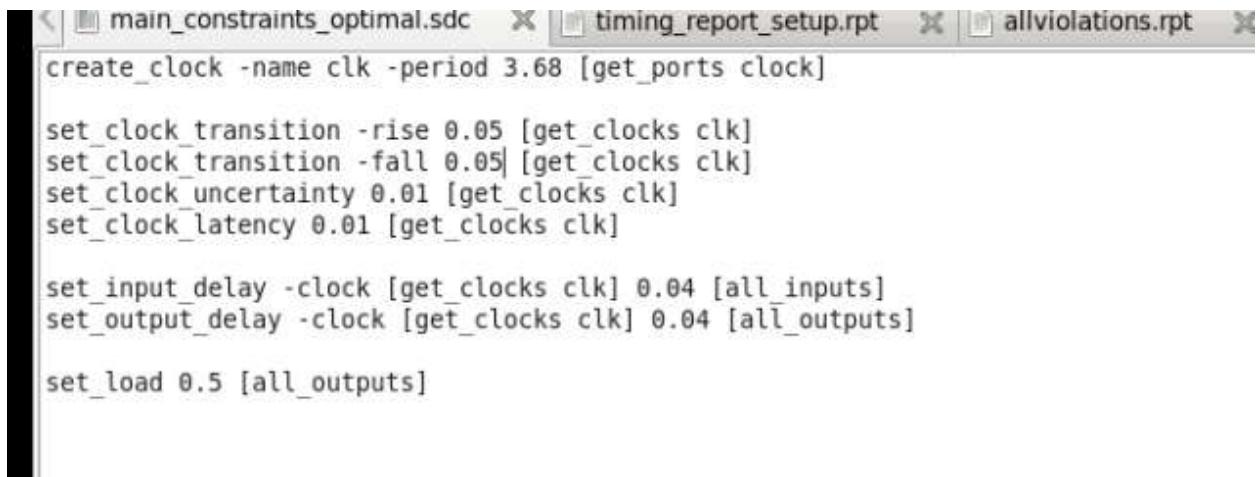
setAnalysisMode -checkType setup
report_timing -check_type setup > ./Physical_Design_scripts/TimingReports/setup_analysis_after_routing.rpt

setAnalysisMode -checkType hold
report_timing -check_type hold > ./Physical_Design_scripts/TimingReports/hold_analysis_after_routing.rpt
report_area > ./Physical_Design_scripts/postRouteArea/Area_report.rpt

```

Innovus(TM) Implementation System 20.1 - /home/rajat21186/ ]

Constraints used:



```

main_constraints_optimal.sdc  X timing_report_setup.rpt  X allviolations.rpt  X

create_clock -name clk -period 3.68 [get_ports clock]

set_clock_transition -rise 0.05 [get_clocks clk]
set_clock_transition -fall 0.05 [get_clocks clk]
set_clock_uncertainty 0.01 [get_clocks clk]
set_clock_latency 0.01 [get_clocks clk]

set_input_delay -clock [get_clocks clk] 0.04 [all_inputs]
set_output_delay -clock [get_clocks clk] 0.04 [all_outputs]

set_load 0.5 [all_outputs]

```

Timing Reports:-

Setup Analysis:-

# Generated by: Cadence Innovus 20.10-p004_1										
# OS:	Linux x86_64(Host ID edaserver4)									
# Generated on:	Wed Apr 17 10:14:47 2024									
# Design:	mesh									
# Command:	report timing -check type setup >../Physical_Design_scripts/TimingReports/setup_analysis_after_routing.rpt									
###### Path 1: MET Setup Check with Pin m0/R1_control_signals2_reg[19]/D (v) checked with leading edge of 'clk'										
Beginpoint: reset (v) triggered by: leading edge of 'clk'										
Path Groups: {clk}										
Analysis View: view1										
Other End Arrival Time 0.064										
- Setup	0.089									
+ Phase Shift	3.680									
- Uncertainty	0.010									
= Required Time	3.645									
- Arrival Time	3.535									
= Slack Time	0.110									
Clock Rise Edge	0.000									
+ Input Delay	0.040									
+ Network Insertion Delay	0.010									
= Beginpoint Arrival Time	0.050									
+										
Instance	Arc	Cell	Delay	Arrival Time	Required Time					
FE_DBTC0_reset	reset v	INVX1	0.474	0.058	0.160					
FE_OFCl1_FE_DBTN0_reset	A v -> Y ^	BUFX2	0.289	0.524	0.633					
FE_OFCl2_FE_DBTN0_reset	A ^ -> Y ^	BUFX2	0.416	0.813	0.923					
g551	A ^ -> Y ^	AND2X1	0.299	1.229	1.338					
m0/FE_OFCl6_P0_signals_1	A ^ -> Y ^	AND2X1	0.299	1.528	1.637					
m0/g18803	A v -> Y v	OR2X1	0.149	1.916	2.026					
m0/g18738	A v -> Y ^	CLKINVX1	0.098	2.014	2.123					
m0/g18647	B ^ -> Y v	NAND2X	0.056	2.069	2.179					
m0/g18538	B v -> Y v	AND2X1	0.046	2.116	2.226					
m0/g18407	AB v -> Y ^	OAIZ2X	0.043	2.156	2.269					
m0/g18319	A ^ -> Y v	NOR2XL	0.031	2.196	2.306					
m0/g18292	C v -> Y v	AND4X4	0.115	2.306	2.415					
m0/g18256	A v -> Y v	CLKINVX2	0.157	2.463	2.572					
m0/g18256	A1 ^ -> Y v	OAIZ1X1	0.028	2.496	2.606					
m0/g18256	C0 v -> Y v	INVX1	0.059	2.534	2.643					
m0/g18228	C0 v -> Y ^	AOI22X1	0.062	2.612	2.722					
m0/g18225	B ^ -> Y v	NAND2X	0.019	2.630	2.740					
m0/g18224	D v -> Y v	OR4X2	0.163	2.794	2.903					
m0/g18185	A v -> Y ^	CLKINVX4	0.121	2.914	3.024					
m0/g18183	A1 ^ -> Y v	OAIZB1X1	0.048	3.010	3.120					
m0/g18154	C0 v -> Y ^	OAIZ11X1	0.043	3.054	3.163					
m0/g18153	B0 ^ -> Y v	AOI211X1	0.014	3.067	3.177					
m0/g2	AN v -> Y v	NOR4BX1	0.037	3.104	3.214					
m0/FE_OFCl4_n_25	A v -> Y v	BUFX2	0.168	3.272	3.382					
m0/g18151	A v -> Y ^	CLKINVX2	0.168	3.440	3.550					
m0/g18149	B0 ^ -> Y v	AOI21X1	0.008	3.448	3.558					
m0/g18085	B0 v -> Y ^	AOI21X1	0.046	3.494	3.604					
m0/g18003	A ^ -> Y v	NAND4XL	0.041	3.535	3.645					
m0/R1_control_signals2_reg[19]	D v	SDFFRHDX1	0.000	3.535	3.645					

# Generated by: Cadence Innovus 20.10-p004_1										
# OS:	Linux x86_64(Host ID edaserver4)									
# Generated on:	Wed Apr 17 10:14:47 2024									
# Design:	mesh									
# Command:	report timing -check type setup >../Physical_Design_scripts/TimingReports/setup_analysis_after_routing.rpt									
###### Path 1: MET Setup Check with Pin m0/R1_control_signals2_reg[19]/D (v) checked with leading edge of 'clk'										
Beginpoint: reset (v) triggered by: leading edge of 'clk'										
Path Groups: {clk}										
Analysis View: view1										
Other End Arrival Time 0.064										
- Setup	0.089									
+ Phase Shift	3.680									
- Uncertainty	0.010									
= Required Time	3.645									
- Arrival Time	3.535									
= Slack Time	0.110									
Clock Rise Edge	0.000									
+ Input Delay	0.040									
+ Network Insertion Delay	0.010									
= Beginpoint Arrival Time	0.050									
+										
Instance	Arc	Cell	Delay	Arrival Time	Required Time					
FE_DBTC0_reset	reset v	INVX1	0.474	0.058	0.160					
FE_OFCl1_FE_DBTN0_reset	A v -> Y ^	BUFX2	0.289	0.524	0.633					
FE_OFCl2_FE_DBTN0_reset	A ^ -> Y ^	BUFX2	0.416	0.813	0.923					
g551	A ^ -> Y ^	AND2X1	0.299	1.229	1.338					
m0/FE_OFCl6_P0_signals_1	A ^ -> Y v	AND2X1	0.299	1.528	1.637					
m0/g18803	A v -> Y v	OR2X1	0.149	1.916	2.026					
m0/g18738	A v -> Y ^	CLKINVX1	0.098	2.014	2.123					
m0/g18647	B ^ -> Y v	NAND2X	0.046	2.069	2.179					
m0/g18538	B v -> Y v	AND2X1	0.019	2.630	2.740					
m0/g18407	AB v -> Y ^	OAIZ2X	0.043	2.156	2.269					
m0/g18319	A ^ -> Y v	NOR2XL	0.031	2.196	2.306					
m0/g18292	C v -> Y v	AND4X4	0.115	2.306	2.415					
m0/FE_OFCl5_n_749	A v -> Y ^	CLKINVX2	0.157	2.463	2.572					
m0/g18256	A1 ^ -> Y v	OAIZ1X1	0.028	2.496	2.606					
m0/g18235	A1 v -> Y v	AO22X1	0.059	2.550	2.659					
m0/g18225	C0 v -> Y ^	AOI22X1	0.062	2.612	2.722					
m0/g18224	B ^ -> Y v	NAND2X	0.019	2.630	2.740					
m0/g18224	D v -> Y v	OR4X2	0.163	2.794	2.903					
m0/FE_OFCl7_n_816	A v -> Y ^	CLKINVX4	0.121	2.914	3.024					
m0/g18185	A1 ^ -> Y v	AOI21X1	0.047	2.962	3.072					
m0/g18183	A1N v -> Y v	OAIZB1X1	0.048	3.010	3.120					
m0/g18154	C0 v -> Y ^	OAIZ11X1	0.043	3.054	3.163					
m0/g18153	B0 ^ -> Y v	AOI211X1	0.014	3.067	3.177					
m0/g2	AN v -> Y v	NOR4BX1	0.037	3.104	3.214					
m0/FE_OFCl4_n_25	A v -> Y v	BUFX2	0.168	3.272	3.382					
m0/g18151	A v -> Y ^	CLKINVX2	0.168	3.440	3.550					
m0/g18149	B0 ^ -> Y v	AOI21X1	0.008	3.448	3.558					
m0/g18085	B0 v -> Y ^	AOI21X1	0.046	3.494	3.604					
m0/g18003	A ^ -> Y v	NAND4XL	0.041	3.535	3.645					
m0/R1_control_signals2_reg[19]	D v	SDFFRHDX1	0.000	3.535	3.645					

In this timing report it shows the critical path of all the paths present in the circuit. The critical path starts from reset and ends at m0/R1\_control\_signals2\_reg[19] /D that is at the D pin of the Flip Flop.

### Arrival Time Computation:-

Starting from the already computed arrival time (other end arrival time) 0.050 ns at beginpoint reset and traversing to the end point through different cells with experiencing different delays are added up. So subsequent vertices arrival time is calculated by adding up the already computed arrival time. Finally, from the above timing report we can infer that AT at the end point is 3.535 ns.

### Required Time Computation:-

Here in the above timing report RT is computed as other end arrival time (0.064 ns) + Phase Shift (3.680ns , clock period) – setup (0.089 ns, time required by the clock to setup) - uncertainty (0.010 ns). Required Time (RT) at the endpoint evaluates to 3.645 ns.

Slack = Required Time - Arrival Time = 0.110 ns.

### Hold Analysis:-

```
#####
# Generated by: Cadence Innovus 20.10-p004_1
# OS: Linux x86_64 (Host ID edaserver4)
# Generated on: Wed Apr 17 16:14:47 2024
# Design: mesh
# Command: report_timing -check_type hold > ../Physical_Design_scripts/TimingReports/hold_analysis_after_routing.rpt
#####
Path 1: MET Hold Check with Pin p1_configure1_reg[6]/CK
Endpoint: p1_configure1_reg[6]/D (^) checked with leading edge of 'clk'
Beginpoint: p1_configure[6] (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time 0.812
+ Hold 0.003
+ Phase Shift 0.000
+ Uncertainty 0.010
= Required Time 0.825
Arrival Time 0.849
Slack Time 0.024
    Clock Rise Edge 0.000
    + Input Delay 0.040
    + Network Insertion Delay 0.010
    = Beginpoint Arrival Time 0.050
+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          |     |      |       | Time   | Time   |
|-----+-----+-----+-----+-----+-----|
|          | p1_configure[6] ^ |          | 0.050 | 0.026 |
| p1_configure1_reg[6] | D ^ | SDFFQXI | +8.001 | 0.849 | 0.025 |
|-----+-----+-----+-----+-----+
```

In this timing report it shows the critical path of all the paths present in the circuit. The critical path starts from p1\_configure[6] and ends at p1\_configure1\_reg[6] / D that is at the D pin of the Flip Flop.

### Arrival Time Computation:-

Starting from the already computed arrival time (other end arrival time) 0.050 ns at beginpoint reset and traversing to the end point through different cells with experiencing different delays are added up. So subsequent vertices arrival time is calculated by adding up the already computed arrival time. Finally, from the above timing report we can infer that AT at the end point is 0.049 ns. In this case the path is from p0\_configure[5] to p0\_configure1\_reg[5] / D which is the D pin of the first flop SDFFQX1.

### Required Time Computation:-

Here in the above timing report RT is computed as other end arrival time (0.012 ns). clock + hold (0.003 ns, time required by the clock to setup) + uncertainty (0.010 ns). Required Time (RT) at the endpoint evaluates to 0.025 ns.

$$\text{Slack} = \text{Arrival Time} - \text{Required Time} = 0.049 - 0.025 = 0.024\text{ns.}$$

### Area Report:-

```
=====
General Design Information
=====
Design Status: Routed
Design Name: mesh
# Instances: 2579
# Hard Macros: 0
# Std Cells: 2579

Standard Cells in Netlist
=====
Cell Type Instance Count Area (μm^2)
A012B81X1 11 58.2013
A0122XL 31 187.7112
OR2XL 1 4.5414
A012B81XL 2 12.1184
NAND4BX1 1 6.8121
BUF2X2 16 72.6624
CLK0R2X1 9 74.9331
TLATNX1 4 57.5244
CLK1INV6 1 6.8121
OR1XL 7 31.1556
A012B81X1 3 18.1556
AND2X1 37 168.0310
A0133XL 4 38.2766
OA1211X1 122 646.3926
SDFFQX1 297 6069.5811
XNOR2X1 4 33.3936
M02X1 13 88.5573
AND2XL 12 54.4968
XOR2XL 11 91.5849
A0122XL 171 1427.1836
OR12XL 89 404.1836
OA1221X1 71 537.3990
OA131X1 2 12.1184
OA21X1 15 102.1815
CLK1INV3 220 49.5546
AO1211X1 24 127.1592
NAND2BX1 24 108.9936
OA1211XL 140 741.7626
nayv1 1 7.4466
```

Usage_Summary_and_Access_Counts			
AND2XL	24	106.3530	
DAI21XL	140	741.7620	
DA22XL	1	7.5690	
XNOR2XL	4	33.3036	
NAND3XL	15	68.1210	
NAND2XL	328	993.6528	
SDFFR0XL	149	3721.6773	
DA21XL	1	6.8121	
AD0HXL	4	48.4416	
NOR2BXL	22	99.9198	
AOI22XL	3	18.1656	
AOI21XL	24	108.9926	
AOI21XL	195	476.8470	
NOR3BX1	40	242.2680	
AOI221XL	15	113.5390	
AOI31XL	10	66.5520	
NAND3BX1	8	48.4416	
AO21XL	2	13.6242	
AOI221XL	5	37.8450	
NOR3XL	35	158.9496	
NOR4BX1	1	6.8121	
OR4X2	1	8.3259	
AO22XL	1	7.5690	
NOR4XL	4	24.2208	
AOI221XL	2	16.5966	
AND4V4	1	8.8397	
SDFFSH0XL	13	354.2292	
INVXL	50	113.5380	
DAI22XL	1	6.6552	
NOR2XL	144	435.8744	
SDFF0X4	1	24.9777	
AOI33XL	2	16.6518	
CLKINV2	2	7.5690	
SDFF0X2	111	2436.4611	
AOI22XL	48	298.6496	
AOI32XL	5	34.6605	
NOR3XL	4	18.1656	
AOI21XL	14	63.5796	
AOI32XL	21	143.6541	
AOI2881XL	2	16.5966	
AOI221XL	1	7.5690	
NAND4XL	37	196.0371	

Pads: 8

Net: 2747

Special Net: 2

IO Pins:

-----

Issued IO Information

```
=====
blobfile/Placement Information
=====
Total area of Standard cells: 22308.871 um^2
Total area of Standard cells(Subtracting Physical Cells): 22308.871 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 45429.895 um^2
Total area of Chip: 48957.385 um^2
Effective Utilization: 4.9106e-01
Number of Cell Rows: 8
% Pure Gate Density #1 (Subtracting BLOCKAGES): 49.106%
% Pure Gate Density #2 (Subtracting MACROS and Physical Cells): 49.106%
% Pure Gate Density #3 (Subtracting MACROS): 49.106%
% Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 49.106%
% Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 49.106%
% Pure Gate Density #6 ((Unreplaced Standard Inst + Unreplaced Black Blob Inst + Fixed Clock Inst Area) / (Free Site Area + Fixed Clock Inst Area) for insts are placed): 49.106%
% Core Density #1(Subtracting Std Cells and MACROS): 49.106%
% Core Density #2(Subtracting Std Cells and MACROS): 49.106%
% Chip Density #1(Subtracting Std Cells and MACROS and IOs): 49.106%
% Chip Density #2(Subtracting Physical Cells): 45.568%
# Macros within 5 sites of IO pad: No
Macro halo defined?: No
```

Inst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop	Latch	Clock
mesh		2587	22308.871	227.070	626.713	8790.637	12666.926	57.524	
0_000	0.000	0.000	74.933	0.000	4.541	70.392	0.000	0.000	
0_000	inc_p0_add_175_41	increment_unsigned_162	16	0.000	0.000	4.541	70.392	0.000	
0_000	0_000	increment_unsigned_128	16	74.933	0.000	4.541	70.392	0.000	
0_000	inc_p1_add_175_41	increment_unsigned_128	16	0.000	0.000	4.541	70.392	0.000	
0_000	0_000	increment_unsigned_142	16	74.933	0.000	4.541	70.392	0.000	
0_000	inc_p2_add_175_41	increment_unsigned_162	16	0.000	0.000	4.541	70.392	0.000	
0_000	0_000	increment_unsigned_162	16	74.933	0.000	4.541	70.392	0.000	
0_000	0_000	increment_unsigned_162	16	0.000	0.000	4.541	70.392	0.000	
r0	master	1938	6345.856	9.003	358.771	4054.713	1923.283	0.000	
0_000	0_000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	
r0	ref	231	1969.454	0.000	63.580	994.495	1001.379	0.000	
0_000	0_000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	
r1	router_355	228	1997.459	0.000	36.767	912.065	1928.027	0.000	
0_000	0_000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	
r2	router_354	227	1960.371	0.000	54.497	994.495	1001.379	0.000	
0_000	0_000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	
r3	router_353	227	1961.128	0.000	54.497	985.252	1001.379	0.000	
0_000	0_000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	

Area of standard cells : 22308.871  $\mu\text{m}^2$

Area of Buffers : 227.070  $\mu m^2$

Area of Inverters : 626.713  $\mu m^2$

Area of Combinational: 8790.637  $\mu m^2$

Area of flip-flops : 12606.926  $\mu m^2$  (SDFFHQX1 + SDFFQX1)

## Power Report:-

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
r3.output2_reg[17]	0.01969	0.1355	0.155	0.0004846	SDFFQX1
CTS_ccl_a_buf_00013	0.05617	0.00056	0.1422	0.0004184	CLKBUFX16
CTS_ccl_a_buf_00019	0.056	0.00056	0.128	0.0004184	CLKBUFX16
CTS_ccl_a_buf_00023	0.05567	0.00056	0.1257	0.0004184	CLKBUFX16
CTS_ccl_a_buf_00025	0.05024	0.00543	0.1221	0.0004184	CLKBUFX16

```

p3_data_got1_reg[6] 0.01655 0.08883 0.09769 0.0002999 SDFFOX2
processor_ready_signals2_reg[0] 0.01691 0.08834 0.09755 0.0002999 SDFFOX2
p3_data_got1_reg[0] 0.0168 0.07962 0.09672 0.0002999 SDFFOX2
p3_data_got1_reg[4] 0.01799 0.07916 0.09654 0.0002999 SDFFOX2
r1_output2_reg[15] 0.01688 0.07868 0.09584 0.0002999 SDFFOX2
r1_output2_reg[14] 0.01682 0.07857 0.0957 0.0002999 SDFFOX2
r0_output2_reg[8] 0.01651 0.07876 0.09557 0.0002999 SDFFOX2
r1_output2_reg[16] 0.01676 0.07838 0.09544 0.0002999 SDFFOX2
r0_output2_reg[3] 0.017 0.07788 0.09518 0.0002999 SDFFOX2
p3_data_got1_reg[5] 0.01662 0.0779 0.09482 0.0002999 SDFFOX2
r1_output2_reg[17] 0.01672 0.07778 0.0948 0.0002999 SDFFOX2
r3_output2_reg[5] 0.0166 0.07755 0.09445 0.0002999 SDFFOX2
r3_output2_reg[8] 0.0162 0.07765 0.09415 0.0002999 SDFFOX2
r0_output2_reg[0] 0.01644 0.07687 0.09362 0.0002999 SDFFOX2
r1_output2_reg[6] 0.01655 0.07635 0.0932 0.0002999 SDFFOX2
r0_output2_reg[4] 0.01628 0.07648 0.09309 0.0002999 SDFFOX2
r1_output2_reg[11] 0.01665 0.07694 0.09299 0.0002999 SDFFOX2
r0_output2_reg[7] 0.01622 0.07632 0.09284 0.0002999 SDFFOX2
r0_output2_reg[2] 0.01632 0.07592 0.09235 0.0002999 SDFFOX2
r1_output2_reg[12] 0.01636 0.0758 0.09246 0.0002999 SDFFOX2
r0_output2_reg[1] 0.01624 0.07559 0.09213 0.0002999 SDFFOX2
r0_output2_reg[6] 0.01667 0.07548 0.09185 0.0002999 SDFFOX2
r0_output2_reg[5] 0.01668 0.07417 0.09055 0.0002999 SDFFOX2
r3_output2_reg[9] 0.01623 0.07349 0.08983 0.0002999 SDFFOX2
p3_data_got1_reg[7] 0.01579 0.07382 0.08991 0.0002999 SDFFOX2
r1_output2_reg[13] 0.01588 0.07333 0.08951 0.0002999 SDFFOX2
r2_output2_reg[16] 0.01683 0.07287 0.08892 0.0002999 SDFFOX2
r3_output2_reg[6] 0.01597 0.0728 0.08898 0.0002999 SDFFOX2
r2_output2_reg[15] 0.01599 0.07274 0.08982 0.0002999 SDFFOX2
r2_output2_reg[17] 0.01585 0.07236 0.08854 0.0002999 SDFFOX2
r3_output2_reg[14] 0.01612 0.07208 0.08815 0.0002999 SDFFOX2
r3_output2_reg[15] 0.01608 0.072 0.08819 0.0002999 SDFFOX2
r1_output2_reg[13] 0.01627 0.07149 0.08801 0.0002999 SDFFOX2
r1_output2_reg[5] 0.01568 0.07198 0.08796 0.0002999 SDFFOX2
p2_data_got1_reg[4] 0.01568 0.07198 0.08796 0.0002999 SDFFOX2
r0_output2_reg[7] 0.01601 0.07133 0.08753 0.0002999 SDFFOX2
r3_output2_reg[16] 0.01663 0.07092 0.08725 0.0002999 SDFFOX2
r2_output2_reg[13] 0.01576 0.07116 0.08722 0.0002999 SDFFOX2
r2_output2_reg[14] 0.0158 0.07055 0.08665 0.0002999 SDFFOX2
r1_output2_reg[4] 0.01561 0.07035 0.08626 0.0002999 SDFFOX2
r3_output2_reg[11] 0.01555 0.07026 0.08614 0.0002999 SDFFOX2
r1_output2_reg[2] 0.01565 0.07019 0.08614 0.0002999 SDFFOX2
r3_output2_reg[7] 0.01513 0.07063 0.08609 0.0002999 SDFFOX2
r3_output2_reg[4] 0.01557 0.0701 0.08597 0.0002999 SDFFOX2
r2_output2_reg[10] 0.01558 0.07092 0.08589 0.0002999 SDFFOX2
r3_output2_reg[13] 0.01559 0.06955 0.08544 0.0002999 SDFFOX2
p2_data_got1_reg[7] 0.01522 0.06958 0.0852 0.0002999 SDFFOX2
r3_output2_reg[8] 0.0154 0.06935 0.08505 0.0002999 SDFFOX2
r0_output2_reg[10] 0.01528 0.06944 0.08502 0.0002999 SDFFOX2
r3_output2_reg[10] 0.01544 0.069 0.08474 0.0002999 SDFFOX2
r1_output2_reg[11] 0.01553 0.06677 0.08459 0.0002999 SDFFOX2

```

rtl\_module.rpt (~\Desktop\New\_VDF\_Project)

```

m0/g18146 8.84e-05 5.191e-05 0.0001613 2.097e-05 NAND2XL
m0/g18145 0.000193 3.639e-05 0.0001603 2.097e-05 NAND2XL
m0/g18637 5.166e-05 6.987e-05 0.0001516 3.532e-05 NOR2XL
m0/g18658 6.642e-05 5.17e-05 0.0001534 3.532e-05 NOR2XL
m0/g18692 7.261e-05 4.555e-05 0.0001532 3.506e-05 AQ121XL
m0/g18441 8.166e-05 3.111e-05 0.0001511 3.102e-05 NOR2XL
r1/g111 8.993e-05 3.408e-05 0.0001456 2.097e-05 NAND2XL
m0/g18690 9.059e-05 3.198e-05 0.0001433 2.088e-05 OA121XL
m0/g18691 8.084e-05 2.944e-05 0.0001311 2.088e-05 OA121XL
g1135 6.329e-05 4.267e-05 0.000129 2.103e-05 NAND4XL
m0/g18438 5.918e-05 3.482e-05 0.0001152 2.097e-05 NAND2XL
g1104 5.911e-05 3.431e-05 0.0001144 2.103e-05 NAND4XL
m0/g18439 6.422e-05 2.699e-05 0.0001121 2.097e-05 NAND2XL
m0/g18642 2.943e-05 6.053e-05 0.0001109 2.097e-05 NAND2XL
m0/g18641 3.518e-05 3.796e-05 0.0001089 3.532e-05 NOR2XL
m0/g18448 6.148e-05 2.537e-05 0.0001078 2.097e-05 NAND2XL
inc_p1_add_175_41/g93 3.273e-05 3.912e-05 0.0001072 3.532e-05 NOR2XL
m0/g18643 4.008e-05 3.178e-05 0.0001072 3.532e-05 NOR2XL
m0/g18643 5.619e-05 2.563e-05 0.0001027 2.885e-05 OA121XL
g1997 4.393e-05 2.001e-05 9.926e-05 3.532e-05 NOR2XL
m0/g18644 2.643e-05 3.732e-05 9.976e-05 3.532e-05 NOR2XL
g1103 4.484e-05 2.975e-05 9.562e-05 2.103e-05 NAND4XL
m0/g18636 1.923e-05 4.484e-05 8.594e-05 2.097e-05 NAND2XL
inc_p2_add_175_41/g93 1.859e-05 2.379e-05 7.776e-05 3.532e-05 NOR2XL
m0/g18653 2.158e-05 3.338e-05 7.594e-05 2.097e-05 NAND2XL
g1998 2.335e-05 1.423e-05 7.289e-05 3.532e-05 NOR2XL
m0/g18645 1.441e-05 3.442e-05 6.98e-05 2.097e-05 NAND2XL
inc_p0_add_175_41/g88 1.152e-05 2.790e-05 5.956e-05 2.097e-05 NAND2XL
m0/g18615 1.654e-05 1.265e-05 5.834e-05 2.914e-05 OA121XL
m0/g18655 7.951e-06 8.597e-06 5.178e-05 3.532e-05 NOR2XL
g1896 9.801e-06 4.342e-06 4.946e-05 3.532e-05 NOR2XL
m0/g18648 5.415e-06 3.795e-06 4.453e-05 3.532e-05 NOR2XL
m0/g18646 9.754e-06 1.306e-05 4.378e-05 2.097e-05 NAND2XL
m0/g19241 9.839e-06 3.798e-06 4.283e-05 2.928e-05 OA121XL
g1995 4.657e-06 2.897e-06 4.276e-05 3.532e-05 NOR2XL
m0/g18973 4.596e-06 7.019e-06 4.099e-05 2.939e-05 OA121XL
m0/g18238 7.791e-06 2.763e-06 3.97e-05 2.914e-05 OA121XL
m0/g18647 5.888e-06 1.244e-05 3.328e-05 2.097e-05 NAND2XL
m0/g19242 4.976e-06 1.66e-06 3.592e-05 2.097e-05 OA121XL
inc_p1_add_175_41/g88 3.94e-06 9.122e-06 3.433e-05 2.097e-05 NAND2XL
m0/g19243 4.008e-06 8.590e-07 3.194e-05 2.097e-05 OA121XL
inc_p3_add_175_41/g88 3.779e-06 8.738e-06 3.498e-05 2.097e-05 NAND2XL
inc_p2_add_175_41/g88 1.957e-06 4.494e-06 2.742e-05 2.097e-05 NAND2XL
m0/g18144 1.701e-06 7.867e-07 2.346e-05 2.097e-05 NAND2XL

```

```

Total ( 2587 ) 9.459 10.84 20.53 0.2326
Total Capacitance 8.993e-11 F
Power Density *** No Die Area ***

```

rtl\_module.rpt (~\Desktop\New\_VDF\_Project)

The report is too big to incorporate into the report

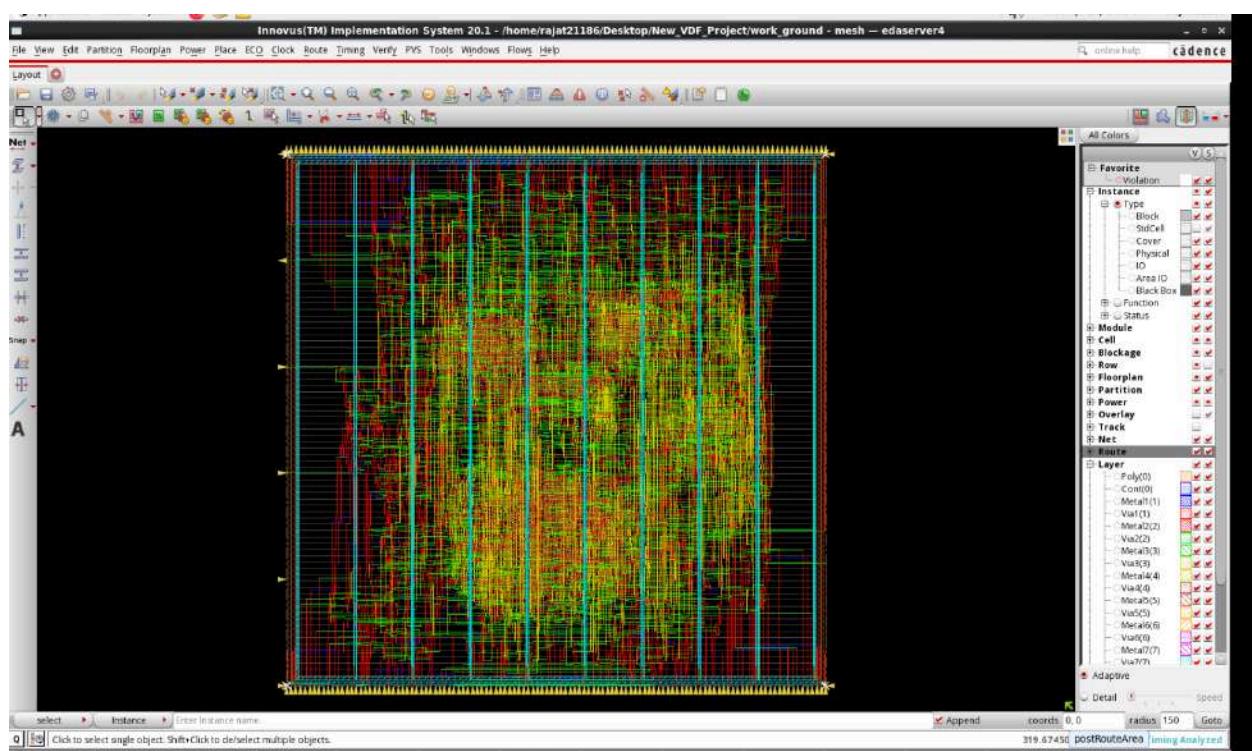
In this report, internal power is the power dissipated inside the cell boundary during charging and discharging of existing capacitances. Total Internal Power is 9.459mW

Switching power of driving cell is the power dissipated by charging load capacitance at the output. The total switching power is 10.84mW

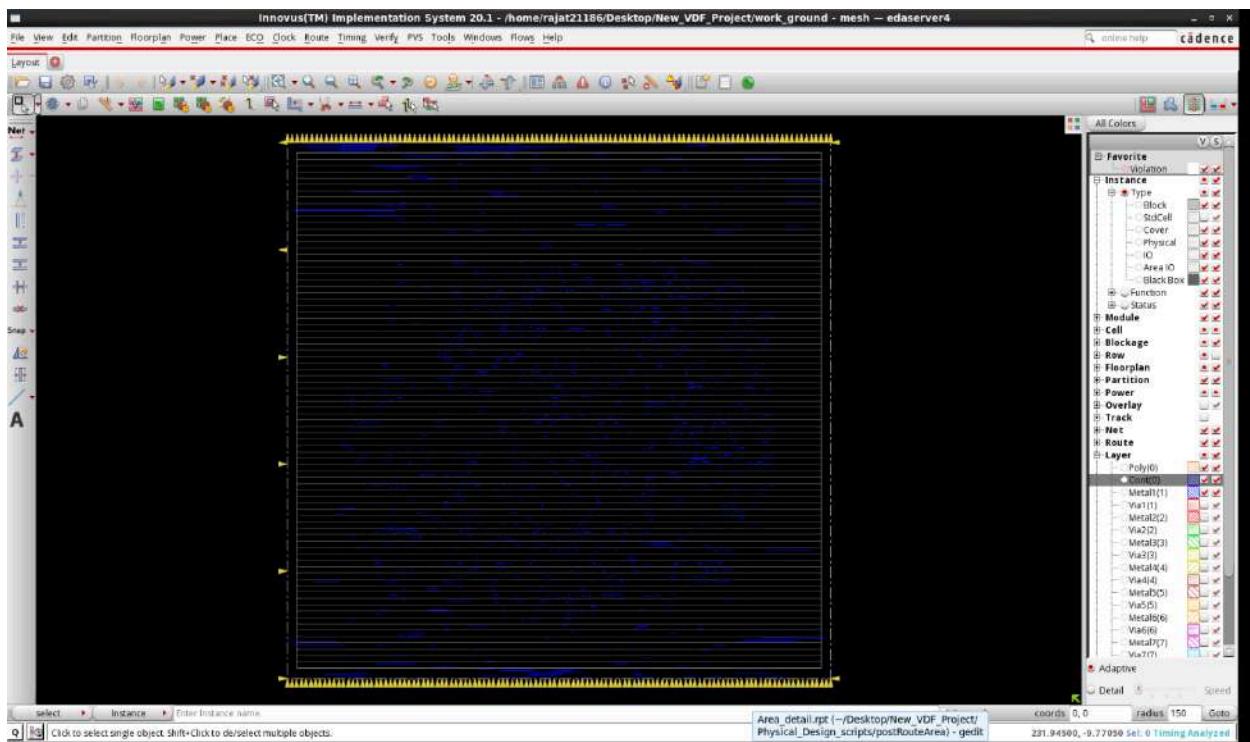
Leakage power is generated from the leakage current that flows between VDD and GND when there is no switching. The total leakage power is 0.2326mW

The total power which is the sum of all these is 20.53mW

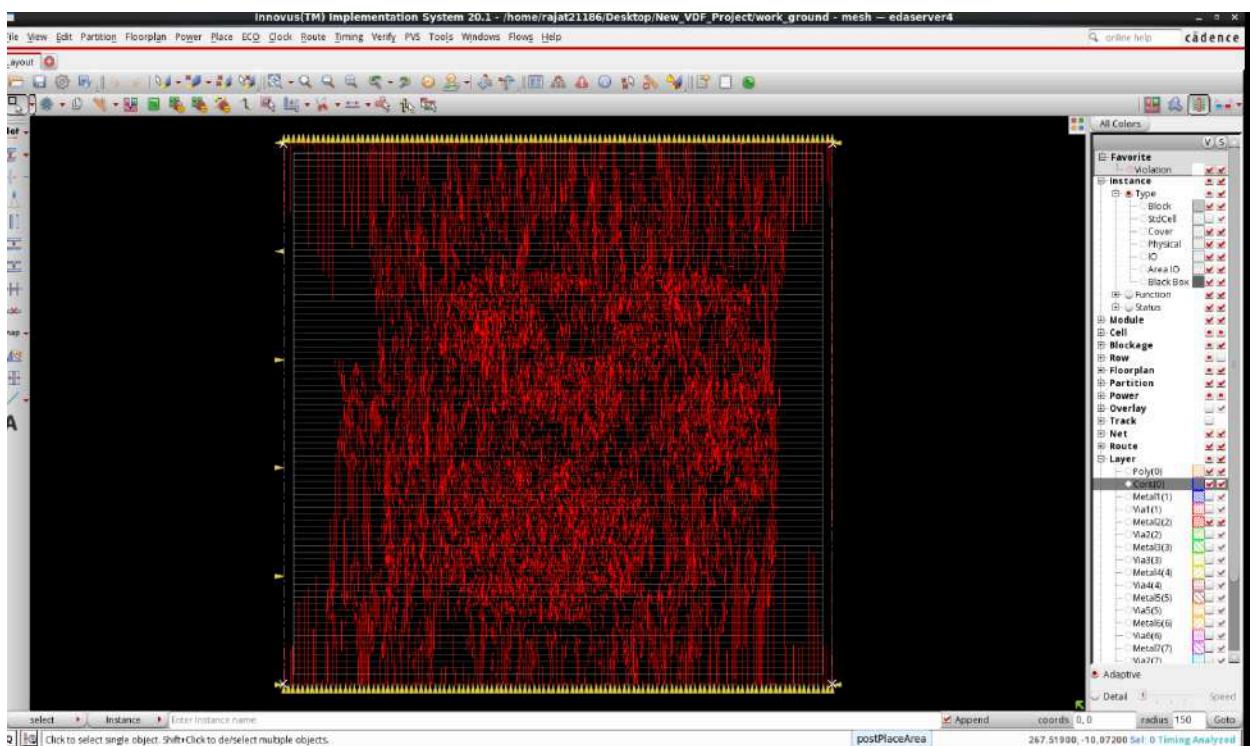
## Layout Screenshot



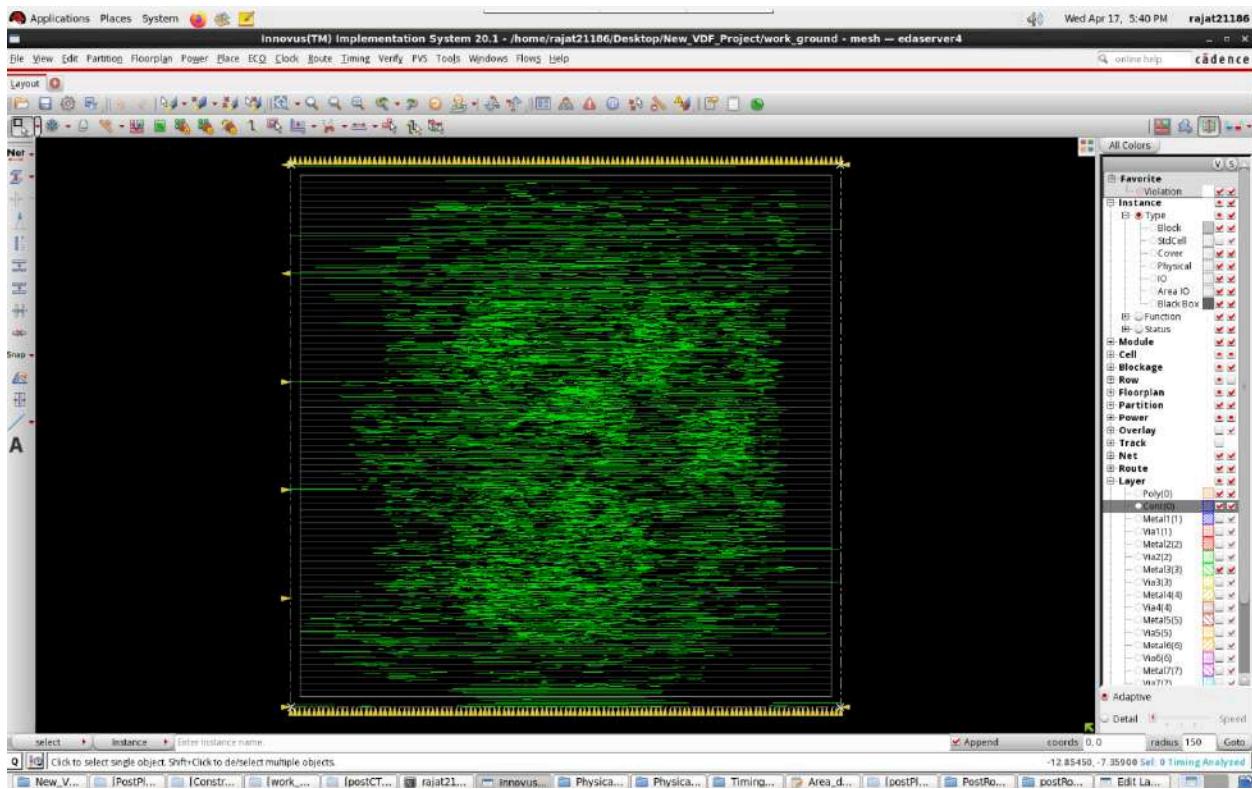
Metal 1 Layer



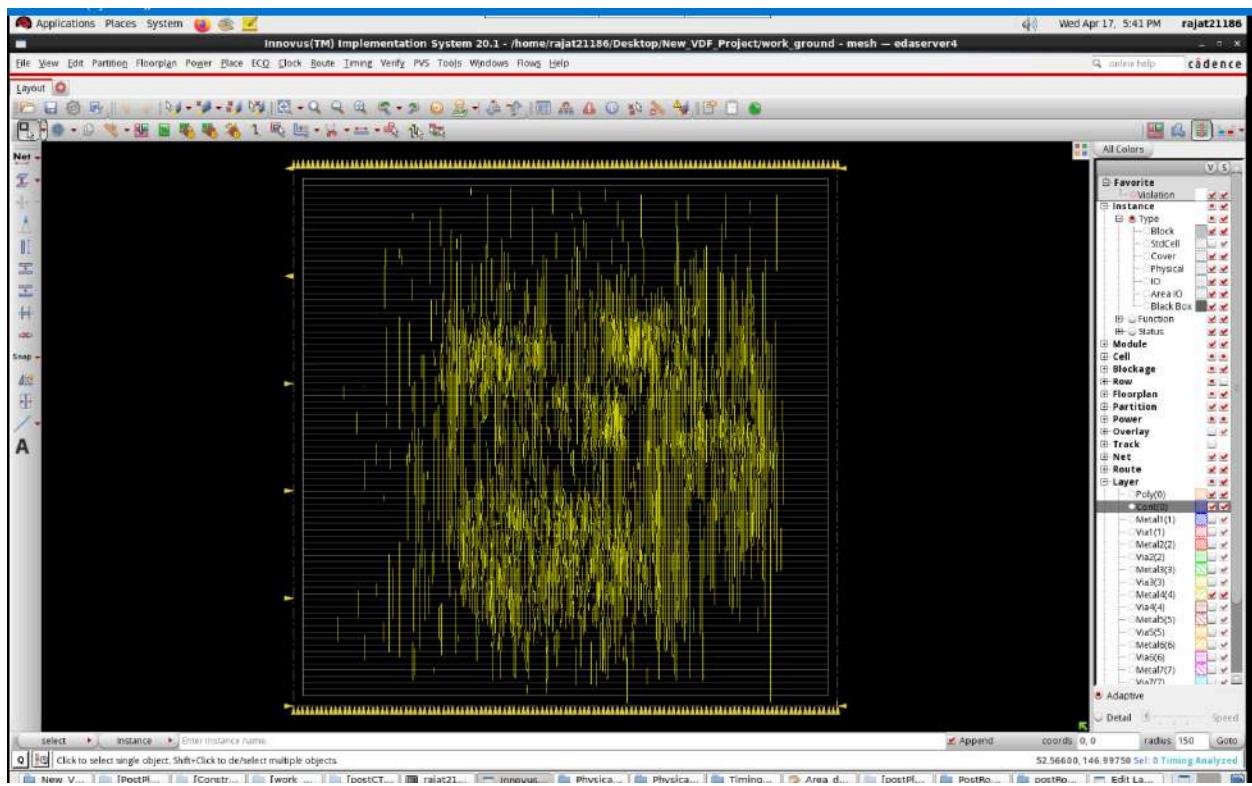
Metal 2 Layer



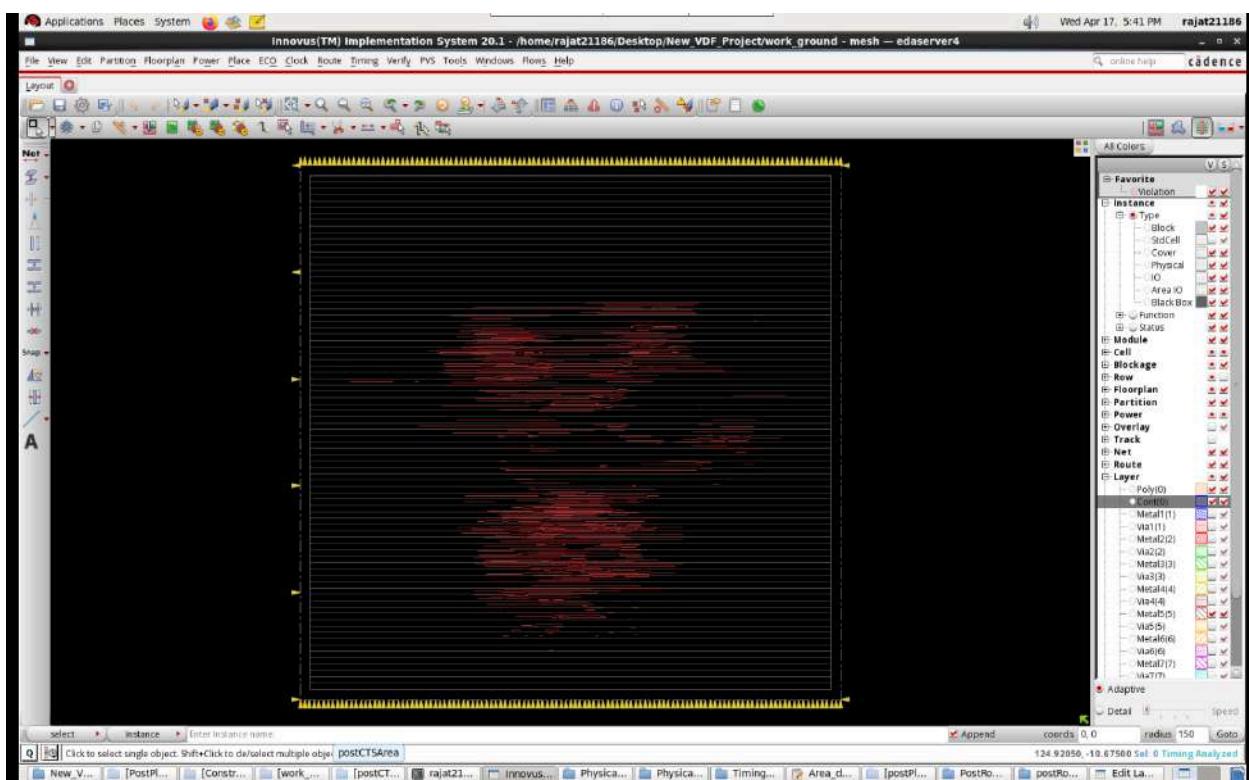
Metal 3



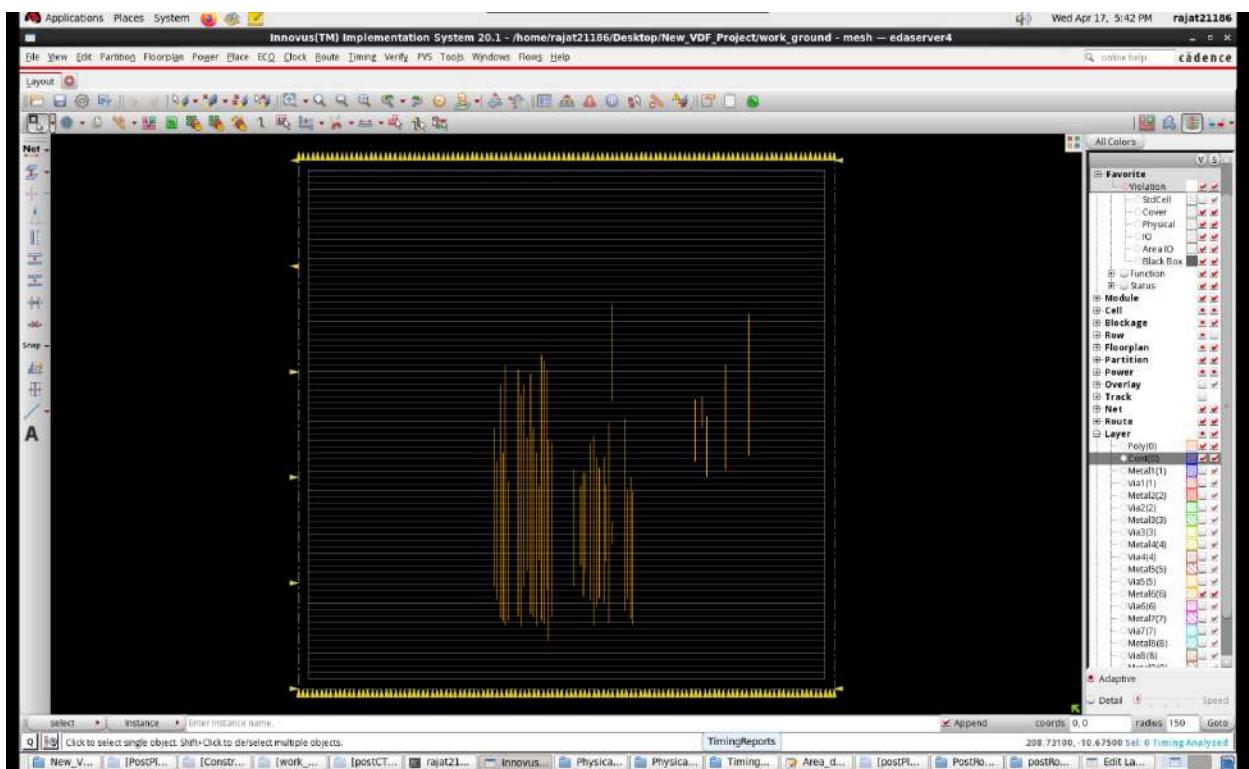
## Metal 4



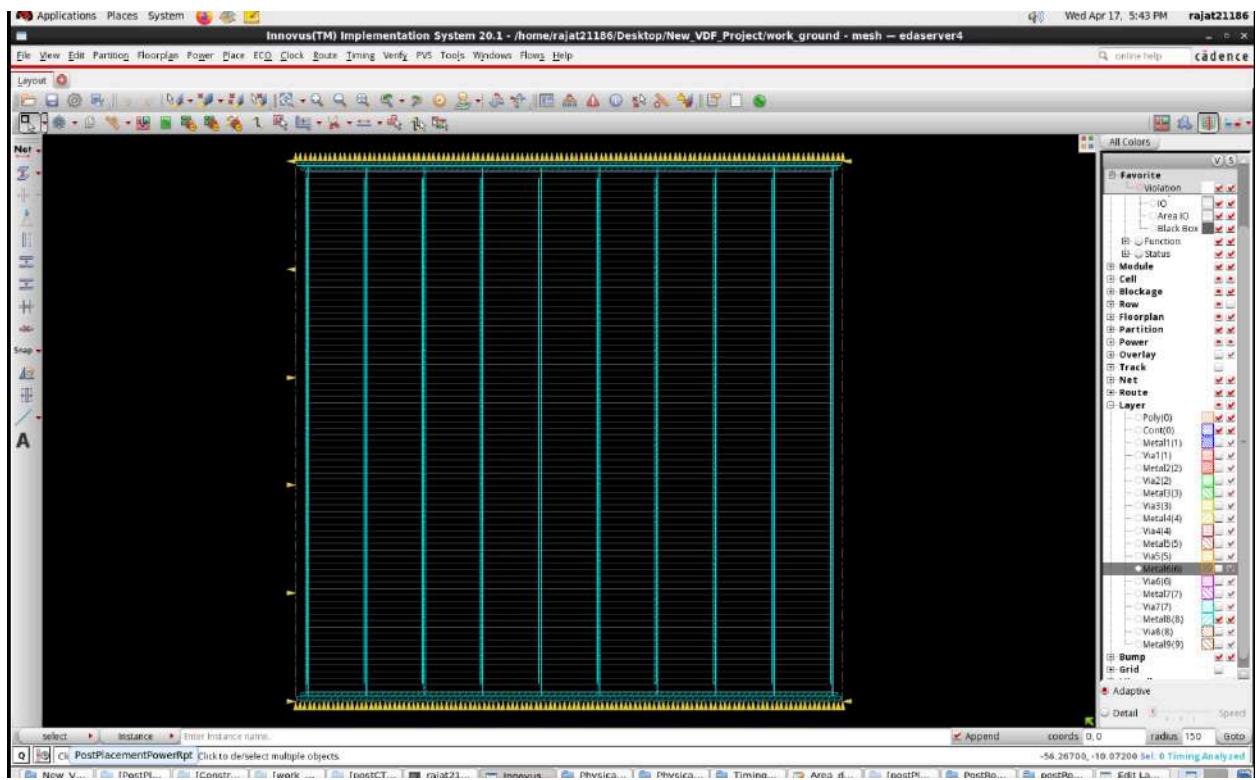
## Metal 5



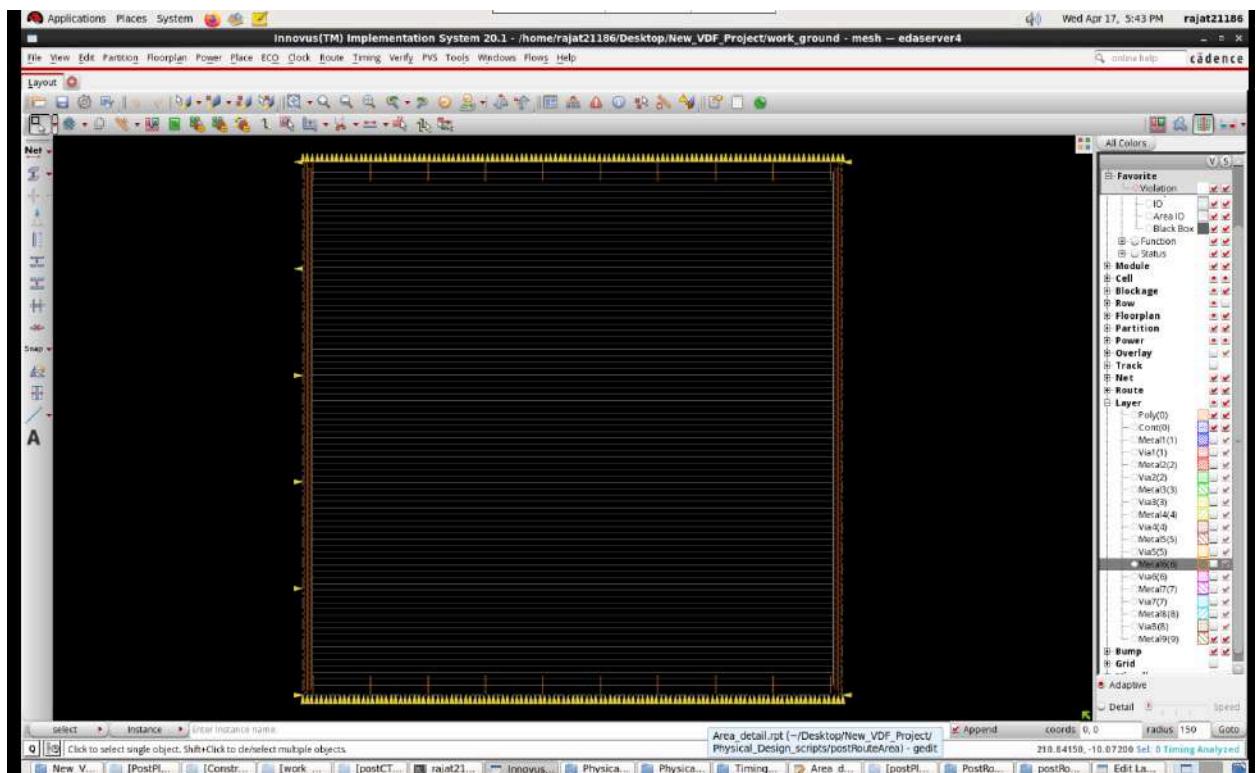
## Metal 6



## Metal 8



## Metal 9



## Layout Design Core Utilization:- 0.8

TCL file:

DoRoute.tcl

```
# Global & Detail Routing/
setNanRouteMode -quiet -timingEngine {}
setNanRouteMode -quiet -routeWithSiPostRouteFix 0
setNanRouteMode -quiet -drouteStartIteration default
setNanRouteMode -quiet -routeTopRoutingLayer default
setNanRouteMode -quiet -routeBottomRoutingLayer default
setNanRouteMode -quiet -drouteEndIteration default
setNanRouteMode -quiet -routeWithTimingDriven false
setNanRouteMode -quiet -routeWithSiDriven false
routeDesign -globalDetail -wireOpt

# Timing Report
# optDesign -postRoute
# optDesign -postRoute -hold

extractRC
rcOut -spf ./Physical_Design_scripts/rtl_module.spf

#Writing SDF file with interconnect and gates delay/
write_sdf -ideal_clock_network ../Physical_Design_scripts/physical_design_rtl_module.sdf

#/Generating gate count report/
#summaryReport -outdir summaryReport
reportGateCount -level 5 -limit 100 -outfile ../Physical_Design_scripts/rtl_module.gateCount

setAnalysisMode -analysisType onChipVariation
optDesign -postRoute
optDesign -postRoute -hold

#/Power Analysis/
set power analysis mode -reset
set power analysis mode -method static -analysis_view view1 -corner max -create_binary_db true -write_static_currents true -honor_negative_energy true -ignore_control_signals true
set power output dir -reset
set power output dir ../Physical_Design_scripts/PostRoutingPowerRpt
set default_switching_activity -reset
set default_switching_activity -input_activity 0.2 -period 10.0
read_activity_file -reset
set_power -reset
set_powerup_analysis -reset

set_dynamic_power_simulation -reset
report_power -rail_analysis_format VS -outfile ../Physical_Design_scripts/PostRoutingPowerRpt/rtl_module.rpt

#/Generating GDS/
streamOut ../Physical_Design_scripts/rtl_module.gds -mapFile streamOut.map -libName DesignLib -units 2000 -mode ALL

#/Saving the Design/
saveNetlist ../Physical_Design_scripts/rtl module post route netlist.v
```

```
extractRC
rcOut -spf ./Physical_Design_scripts/rtl_module.spf

#Writing SDF file with interconnect and gates delay/
write_sdf -ideal_clock_network ../Physical_Design_scripts/physical_design_rtl_module.sdf

#/Generating gate count report/
#summaryReport -outdir summaryReport
reportGateCount -level 5 -limit 100 -outfile ../Physical_Design_scripts/rtl_module.gateCount

setAnalysisMode -analysisType onChipVariation
optDesign -postRoute
optDesign -postRoute -hold

#/Power Analysis/
set power analysis mode -reset
set power analysis mode -method static -analysis_view view1 -corner max -create_binary_db true -write_static_currents true -honor_negative_energy true -ignore_control_signals true
set power output dir -reset
set power output dir ../Physical_Design_scripts/PostRoutingPowerRpt
set default_switching_activity -reset
set default_switching_activity -input_activity 0.2 -period 10.0
read_activity_file -reset
set_power -reset
set_powerup_analysis -reset

set_dynamic_power_simulation -reset
report_power -rail_analysis_format VS -outfile ../Physical_Design_scripts/PostRoutingPowerRpt/rtl_module.rpt

#/Generating GDS/
streamOut ../Physical_Design_scripts/rtl_module.gds -mapFile streamOut.map -libName DesignLib -units 2000 -mode ALL

#/Saving the Design/
saveNetlist ../Physical_Design_scripts/rtl module_post_route_netlist.v
defout -floorplan -netlist -routing ../Physical_Design_scripts/rtl_module.def
saveDesign ../Physical_Design_scripts/_uptoGDS.enc

verify_drc
verify_connectivity

# Area
summaryReport -outdir ../Physical_Design_scripts/postRouteArea -noHTML
report_area -detail -show_leaf_cells -table_style {vertical}

setAnalysisMode -checkType setup
report_timing -check_type setup > ../Physical_Design_scripts/TimingReports/setup_analysis_after_routing.rpt

setAnalysisMode -checkType hold
report_timing -check_type hold > ../Physical_Design_scripts/TimingReports/hold_analysis_after_routing.rpt
report_area > ../Physical_Design_scripts/postRouteArea/Area_report.rpt
```

Constraints used:

```

main_constraints_optimal.sdc  X timing_report_setup.rpt  X allviolations.rpt  X
create_clock -name clk -period 3.68 [get_ports clock]

set_clock_transition -rise 0.05 [get_clocks clk]
set_clock_transition -fall 0.05 [get_clocks clk]
set_clock_uncertainty 0.01 [get_clocks clk]
set_clock_latency 0.01 [get_clocks clk]

set_input_delay -clock [get_clocks clk] 0.04 [all_inputs]
set_output_delay -clock [get_clocks clk] 0.04 [all_outputs]

set_load 0.5 [all_outputs]

```

Timing Reports:

Setup Analysis:-

Instance	Arc	Cell	Delay	Arrival Time	Required Time
p0_configure1 req[0]	CK ^ -> Q ^	SDFFQX1	0.009	0.105	0.281
p0_configure1_req[0]	CK ^ -> Y v	CLKINVX1	0.042	0.147	0.323
g405	C v -> Y ^	NORBX1	0.331	0.477	0.653
g551	C v -> Y v	INX1	0.358	0.827	1.003
m0/FE_BTC14_P0_signals_1	A ^ -> Y v	INX1	0.358	1.285	1.461
m0/156809	B v -> Y ^	NAND2XL	0.117	1.275	1.461
m0/156828	A ^ -> Y v	CLKINVX1	0.228	1.495	1.671
m0/15326	B0 v -> Y ^	A012LX1	0.087	1.383	1.759
m0/15238	B ^ -> Y v	NAND2XL	0.028	1.610	1.786
m0/15666	A0 v -> Y ^	A012LX1	0.035	1.645	1.821
m0/15642	B ^ -> Y ^	NAND2XL	0.023	1.666	1.844
m0/15619	A v -> Y ^	NOR2XL	0.126	1.793	1.969
m0/15618	A ^ -> Y v	NAND3X4	0.181	1.979	2.155
m0/156569	A v -> Y ^	CLKINVX1	0.518	2.489	2.665
m0/g14934	A1 ^ -> Y v	A012LX1	0.042	2.530	2.706
m0/g14886	A1 v -> Y ^	A012LX1	0.061	2.596	2.772
m0/g14879	B ^ -> Y v	NOR2XL	0.031	2.627	2.803
m0/g14871	B v -> Y ^	NAND2XL	0.037	2.664	2.840
m0/g14870	A ^ -> Y v	BIFX1	0.113	2.771	3.153
m0/g14814_n_368	A ^ -> Y v	OAI2LX1	0.083	2.986	3.156
m0/g14781	A1 ^ -> Y v	OAI2LX1	0.083	3.086	3.262
m0/g14729	B v -> Y ^	NAND2XL	0.046	3.026	3.202
m0/g14708	A ^ -> Y v	NAND3X1	0.020	3.047	3.223

Path 1: MET Setup Check with Pin m0/R3 control_signals2_reg[1]/D					
Endpoint: m0/R3_control_signals2_reg[1]/D (^) checked with leading edge of 'clk'					
Beginpoint: p0_configure1_reg[0]/Q (^) triggered by leading edge of 'clk'					
Analysis View: view1					
Other End Arrival Time					
- Setup	0.068				
+ Phase Shift	0.126				
= Uncertainty	0.010				
= Required Time	3.612				
- Arrival Time	3.436				
= Slack Time	0.176				
Clock Rise Edge	0.060				
+ Clock Network Latency (Prop)	0.014				
= Beginpoint Arrival Time	0.014				
+-----+-----+-----+-----+-----+-----+					
Instance	Arc	Cell	Delay	Arrival Time	Required Time
p0_configure1_reg[0]	CK ^			0.014	0.198
p0_configure1_reg[0]	CK ^ -> Q ^	SDFFOX1	0.090	0.105	0.281
g465	A ^ -> Y v	CLKINVX1	0.042	0.147	0.323
g551	C v -> Y ^	NOR3BK2	0.331	0.477	0.653
m0/FE_DBTC14_P0_signals_1	A ^ -> Y v	INVXL	0.350	0.827	1.003
m0/g15886	B v -> Y ^	NAND2XL	0.447	1.275	1.451
m0/g15828	A ^ -> Y v	CLKINVX1	0.220	1.499	1.671
n0/g15326	B v -> Y ^	AO121X1	0.087	1.583	1.759
n0/g15738	B v -> Y v	NAND2XL	0.028	1.610	1.786
n0/g15660	AB ^ -> Y ^	AO121X1	0.039	1.645	1.821
n0/g15842	B v -> Y v	NAND2XL	0.023	1.668	1.844
n0/g15819	A v -> Y ^	NOR2XL	0.126	1.793	1.969
n0/g15818	A ^ -> Y v	NAW03X4	0.185	1.979	2.155
n0/Top16569	A v -> Y ^	CLKINVX1	0.519	2.488	2.665
n0/g14934	A1 ^ -> Y v	AO121X1	0.042	2.530	2.706
n0/g14880	A1 v -> Y ^	AO121X1	0.066	2.596	2.772
n0/g14875	B ^ -> Y v	NOR2XL	0.031	2.627	2.803
n0/g14871	B v -> Y ^	NAND2XL	0.037	2.664	2.840
n0/FE_OFCL14_n_968	A ^ -> Y ^	BUF1X1	0.313	2.977	3.153
n0/g14780	A1 ^ -> Y v	AO121X1	0.038	2.985	3.156
n0/g14729	B v -> Y ^	NAND2XL	0.046	3.025	3.202
n0/g14768	A ^ -> Y v	NAW03X4	0.020	3.047	3.223
n0/g14764	B v -> Y ^	NOR2XL	0.041	3.088	3.264
n0/g14702	A ^ -> Y ^	AND2X4	0.139	3.227	3.403
n0/g14761	A ^ -> Y v	CLKINVX4	0.103	3.330	3.506
n0/g14597	A1 v -> Y ^	AO121X1	0.106	3.436	3.612
m0/R3_control_signals2_reg[1]	D ^	SDFFRHQX1	0.000	3.436	3.612

In this timing report it shows the critical path of all the paths present in the circuit. The critical path starts from p0\_configure1\_reg[0]/Q and ends at m0/R3\_control\_signals2\_reg[1] /D that is at the D pin of the Flip Flop.

### Arrival Time Computation:-

Starting from the already computed arrival time (other end arrival time) 0.014 ns at beginpoint reset and traversing to the end point through different cells with experiencing different delays are added up. So subsequent vertices arrival time is calculated by adding up the already computed arrival time. Finally, from the above timing report we can infer that AT at the end point is 3.436 ns.

### Required Time Computation:-

Here in the above timing report RT is computed as other end arrival time (0.068 ns) + Phase Shift (3.680ns , clock period) – setup (0.126 ns, time required by the clock to setup) - uncertainty (0.010 ns). Required Time (RT) at the endpoint evaluates to 3.612 ns.

Slack = Required Time - Arrival Time = 0.176 ns.

### Hold Analysis:-

```

hold_analysis_after_routing.rpt  setup_analysis_after_routing.rpt
#####
# Generated by: Cadence Innovus 20.10-p004.1
# OS: Linux x86_64 (Host ID edaserver4)
# Generated on: Wed Apr 17 18:44:18 2024
# Design: mesh
# Command: report_timing -check_type hold > ../Physical_Design_Scripts2/TimingReports/hold_analysis_after_routing.rpt
#####
Path 1: MET Hold Check with Pin p0_configure1_reg[7]/CK
Endpoint: p0_configure1_reg[7]/D (^) checked with leading edge of 'clk'
Beginpoint: p0_configure[7] (^) triggered by leading edge of 'clk'
Path Groups: {clk}
Analysis View: view1
Other End Arrival Time 0.015
+ Hold 0.008
+ Phase Shift 0.000
+ Uncertainty 0.010
= Required Time 0.033
Arrival Time 0.050
Slack Time 0.017
Clock Rise Edge 0.000
+ Input Delay 0.040
+ Network Insertion Delay 0.010
= Beginpoint Arrival Time 0.050
+-----+
| Instance | Arc | Cell | Delay | Arrival | Required |
|          | p0_configure[7] ^ | SDFFQX1 | -0.000 | 0.050 | 0.033 |
+-----+

```

In this timing report it shows the critical path of all the paths present in the circuit. The critical path starts from p0\_configure[7] and ends at p0\_configure1\_reg[7] / D that is at the D pin of the Flip Flop.

#### Arrival Time Computation:-

Starting from the already computed arrival time (other end arrival time) 0.050 ns at beginpoint reset and traversing to the end point through different cells with experiencing different delays are added up. So subsequent vertices arrival time is calculated by adding up the already computed arrival time. Finally, from the above timing report we can infer that AT at the end point is 0.050 ns. In this case the path is from p0\_configure[7] to p0\_configure1\_reg[7] / D which is the D pin of the first flop SDFFQX1.

#### Required Time Computation:-

Here in the above timing report RT is computed as other end arrival time (0.015 ns). clock + hold (0.008 ns, time required by the clock to setup) + uncertainty (0.010 ns). Required Time (RT) at the endpoint evaluates to 0.033 ns.

$$\text{Slack} = \text{Arrival Time} - \text{Required Time} = 0.050 - 0.033 = 0.017\text{ns.}$$

#### Area Report:

```
#####
# Generated by: Cadence InnoVus 20.10-1604_1
# OS: Linux x86_64(Host ID edserver4)
# Generated on: wed Apr 17 18:44:18 2024
# Design: mesh
# Command: summaryReport -outdir ..\Physical Design Scripts2\postRouteArea -noHtml
#####

=====
General Design Information
=====

Design Status: Routed
Design Name: mesh
# Instances: 2797
# Has Macros: 0
# Std Cells: 2797

Standard Cells in Netlist
-----
Cell Type Instance Count Area (um^2)
AO128B1X1 5 26.4915
AO122XL 1 6.0552
NAND3X4 1 14.3811
AO132XL 1 6.8121
AO128B1XL 4 24.2288
CLKBUFX12 3 47.6847
BUFX2 15 68.1216
NOR3BX2 1 9.8397
COO2DX1 9 74.1621
TLATNX1 4 57.5244
OA122XL 1 8.3259
OR2X1 3 13.6242
AO128B1X1 32 193.7664
AND2X1 53 246.6942
AO133XL 4 30.2766
OA1211X1 76 402.6788
AND3X1 8 48.4416
SDFFOX1 297 6869.5811
XNOR2X1 3 24.9777
MX2X1 21 143.0541
AND2XL 16 72.6624
XOR2XL 4 33.3036
AO122XL 173 1446.3887
OA1211X1 130 596.4481
CLKBUFX16 4 84.7728
OA1221X1 27 204.3636
OA131X1 4 24.2288
OA21X1 18 122.6176
CLKINVX1 234 531.3438
```

```
=====
UM2LX1 10 122.0110
CLKINVX1 234 531.3438
AO1211X1 66 349.6878
NAND2BX1 33 149.8662
OA1211XL 164 551.0232
OA22X1 1 7.5699
CLKINVX4 1 6.0552
XNOR2XL 12 99.9108
NAND3X1 24 108.9936
NAND2XL 334 1011.2184
SDFFRMQX1 149 3721.6773
NOR2BX1 23 104.4522
OA122X1 43 260.3736
OA121XL 33 149.8662
OA132X1 6 40.8726
AO121X1 124 563.1336
NOR2X1 2 7.5699
NOR3BX1 37 224.6424
INVXL 16 36.3312
AO1221X1 8 60.5529
AO131X1 9 54.4968
NAND3BX1 6 36.3312
AO21X1 4 27.2484
OA1221XL 34 257.3469
NOR3X1 42 190.7388
AND2X4 1 8.3259
NOR4BX1 1 6.8121
NOR4X1 4 24.2288
AO1211XL 2 10.5966
NAND2BX1 3 13.6242
SDFFSMQX1 13 354.2292
INVX1 78 158.9499
OA122XL 25 151.3889
NOR2XL 135 488.7269
SDFFOX4 1 24.9777
OA133X1 2 16.6518
SDFFOX2 111 2436.4611
AO122X1 58 382.7600
OA132XL 7 47.6847
NOR3XL 4 18.1656
AO121XL 4 18.1656
OR3X1 1 6.0552
AO132X1 12 81.7452
OA128B1XL 28 146.3524
NAND4XL 18 52.9839
MX2XL 58 382.7600
```

ids: 0  
rt: 2964

```

=====  

Coriolis/Placement Information  

=====  

Total area of Standard cells: 23228.504 um2  

Total area of Standard cells(Subtracting Physical Cells): 23228.504 um2  

Total area of Macros: 0.000 um2  

Total area of Blockages: 0.000 um2  

Total area of Pad cells: 0.000 um2  

Total area of Core: 31962.373 um2  

Total area of Chip: 34931.776 um2  

Effective Utilization: 7.2675e-01  

Number of Cell Rows: 81  

% Pure Gate Density #1 (Subtracting BLOCKAGES): 72.675%  

% Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 72.675%  

% Pure Gate Density #3 (Subtracting MACROS): 72.675%  

% Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 72.675%  

% Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 72.675%  

% Pure Gate Density #6 ((Unreplaced Standard Inst + Unreplaced Block Inst + Unreplaced Black Blob Inst + Fixed Clock Inst Area) / (Free Site Area + Fixed Clock Inst Area) for insts are placed): 72.675%  

% Core Density (Counting Std Cells and MACROS): 72.675%  

% Chip Density #1(Counting Std Cells and MACROS and IOs): 66.497%  

% Chip Density #2(Subtracting Physical Cells): 66.497%  

# Macros within 5 sites of IO pad: No  

Macro halo defined?: No
=====
```

Inst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop	Latch	Clock
Date	Macro	Physical							
mesh		2797	23228.504	200.578	732.679	9630.796	12666.926	57.524	
0.000	0.000	0.000							
inc_p0_add_175_41	increment_unsigned_138	16	74.933	0.000	0.000	74.933	0.000	0.000	
0.000	0.000	0.000							
inc_p1_add_175_41	increment_unsigned_159	16	74.933	0.000	0.000	74.933	0.000	0.000	
0.000	0.000	0.000							
inc_p2_add_175_41	increment_unsigned_178	16	74.933	0.000	0.000	74.933	0.000	0.000	
0.000	0.000	0.000							
inc_p3_add_175_41	increment_unsigned_198	16	74.933	0.000	0.000	74.933	0.000	0.000	
0.000	0.000	0.000							
m0	master	1292	7265.483	4.541	444.390	4893.359	1923.283	0.000	
0.000	0.000	0.000							
r0	router	232	1978.211	0.000	65.856	902.982	1001.379	0.000	
0.000	0.000	0.000							
r1	router_355	229	1998.216	0.000	59.038	910.551	1028.627	0.000	
0.000	0.000	0.000							
r2	router_354	228	1961.128	0.000	56.767	902.982	1001.379	0.000	
0.000	0.000	0.000							
r3	router_353	227	1961.128	0.000	54.497	905.252	1001.379	0.000	
0.000	0.000	0.000							

Area of standard cells : 23228.504  $\mu\text{m}^2$

Area of Buffers : 200.578  $\mu\text{m}^2$

Area of Inverters : 732.679  $\mu\text{m}^2$

Area of Combinational: 9630.796  $\mu\text{m}^2$

Area of flip-flops : 12606.926  $\mu\text{m}^2$  (SDFFHQX1 + SDFFQX1)

## Power Report:

```

Innovus 20.10-p004.1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
Date & Time: 2024-Apr-17 18:44:05 (2024-Apr-17 13:14:05 GMT)

Design: mesh
Liberty Libraries used:
    viewl: /home/raja21186/Desktop/New_VDF_Project/library/fast.lib
Power Domain used:
Power View : view1
User-Defined Activity : N.A.
Activity File: N.A.
Hierarchical Global Activity: N.A.
Global Activity: N.A.
Sequential Element Activity: N.A.
Primary Input Activity: 0.200000
Default icg ratio: N.A.
Global Comb clockGate Ratio: N.A.
Power Units = 1mW
Time Units = 1e-09 secs
Temperature = 0
report_power -outfile ../Physical_Design_Scripts2/PostRoutingPowerRpt/rtl_module.rpt -rail_analysis_format vs

```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
r3_output2_reg[17]	0.02144	0.1625	0.1843	0.0004040	SDFFOX4
CTS_ccl_a_buf_00013	0.05583	0.08298	0.1392	0.0004194	CLKBUFX16
CTS_ccl_a_buf_00015	0.05539	0.08294	0.1378	0.0004194	CLKBUFX16
CTS_ccl_a_buf_00017	0.05542	0.0792	0.126	0.0004194	CLKBUFX16
CTS_ccl_a_buf_00021	0.05586	0.06947	0.1257	0.0004194	CLKBUFX16

rtl_module.rpt					
p3_data_got1_reg[8]	0.01721	0.08335	0.1009	0.0002999	SDFFOX2
r1_output2_reg[17]	0.01766	0.08219	0.1009	0.0002999	SDFFOX2
r3_output2_reg[15]	0.01761	0.08288	0.1008	0.0002999	SDFFOX2
r3_output2_reg[9]	0.01772	0.08273	0.1008	0.0002999	SDFFOX2
r1_output2_reg[8]	0.01747	0.08297	0.1007	0.0002999	SDFFOX2
r1_output2_reg[11]	0.01762	0.08282	0.1007	0.0002999	SDFFOX2
r3_output2_reg[14]	0.01739	0.08384	0.1007	0.0002999	SDFFOX2
r3_output2_reg[16]	0.01772	0.08266	0.1007	0.0002999	SDFFOX2
r1_output2_reg[1]	0.0173	0.08307	0.1007	0.0002999	SDFFOX2
r1_output2_reg[16]	0.01751	0.08282	0.1006	0.0002999	SDFFOX2
r1_output2_reg[10]	0.01743	0.08279	0.1005	0.0002999	SDFFOX2
r3_output2_reg[8]	0.0176	0.08253	0.1004	0.0002999	SDFFOX2
r1_output2_reg[14]	0.01734	0.08273	0.1003	0.0002999	SDFFOX2
r0_output2_reg[10]	0.01774	0.08269	0.1003	0.0002999	SDFFOX2
r3_output2_reg[11]	0.01738	0.08251	0.1003	0.0002999	SDFFOX2
r1_output2_reg[13]	0.01733	0.08252	0.1001	0.0002999	SDFFOX2
r1_output2_reg[2]	0.01720	0.08247	0.1	0.0002999	SDFFOX2
p2_data_got1_reg[2]	0.01693	0.08271	0.0994	0.0002999	SDFFOX2
r1_output2_reg[8]	0.01737	0.08226	0.0993	0.0002999	SDFFOX2
r3_output2_reg[13]	0.01752	0.08203	0.0993	0.0002999	SDFFOX2
r3_output2_reg[7]	0.01755	0.08184	0.0996	0.0002999	SDFFOX2
r1_output2_reg[7]	0.01738	0.08159	0.09967	0.0002999	SDFFOX2
r3_data_got1_reg[2]	0.01723	0.08191	0.0994	0.0002999	SDFFOX2
p3_data_got1_reg[4]	0.01755	0.08093	0.09878	0.0002999	SDFFOX2
r1_output2_reg[8]	0.01724	0.08099	0.09853	0.0002999	SDFFOX2
r0_output2_reg[14]	0.017	0.08181	0.09831	0.0002999	SDFFOX2
r1_output2_reg[9]	0.01787	0.08075	0.09813	0.0002999	SDFFOX2
r0_output2_reg[12]	0.01707	0.08061	0.09798	0.0002999	SDFFOX2
r3_output2_reg[2]	0.01737	0.08083	0.09797	0.0002999	SDFFOX2
r3_output2_reg[1]	0.01699	0.08072	0.09797	0.0002999	SDFFOX2
r2_output2_reg[17]	0.01704	0.08038	0.09772	0.0002999	SDFFOX2
r3_output2_reg[5]	0.01737	0.08003	0.0977	0.0002999	SDFFOX2
r0_output2_reg[1]	0.01685	0.08031	0.09746	0.0002999	SDFFOX2
r2_output2_reg[1]	0.01714	0.07995	0.09739	0.0002999	SDFFOX2
r2_output2_reg[4]	0.01694	0.07987	0.09711	0.0002999	SDFFOX2
r1_output2_reg[4]	0.01625	0.08047	0.09762	0.0002999	SDFFOX2
r2_output2_reg[3]	0.01687	0.07981	0.09699	0.0002999	SDFFOX2
r2_output2_reg[8]	0.01676	0.0791	0.09616	0.0002999	SDFFOX2
r2_output2_reg[2]	0.01691	0.07856	0.09577	0.0002999	SDFFOX2
r2_output2_reg[5]	0.01667	0.0784	0.09537	0.0002999	SDFFOX2
CTS_ccl_a_buf_00025	0.03049	0.06406	0.09501	0.0004583	CLKBUFX12
CTS_ccl_a_buf_00019	0.03034	0.06394	0.09474	0.0004583	CLKBUFX12
CTS_ccl_a_buf_00023	0.03065	0.06374	0.09492	0.0004583	CLKBUFX12
r2_output2_reg[7]	0.01656	0.07766	0.09452	0.0002999	SDFFOX2
p3_data_got1_reg[3]	0.01734	0.07614	0.09368	0.0002999	SDFFOX2
r2_output2_reg[1]	0.01645	0.07672	0.09347	0.0002999	SDFFOX2
p3_data_got1_reg[8]	0.017	0.07612	0.09342	0.0002999	SDFFOX2
r2_output2_reg[9]	0.01652	0.07647	0.0933	0.0002999	SDFFOX2
r0_output2_reg[2]	0.01625	0.07664	0.09319	0.0002999	SDFFOX2
r0_output2_reg[7]	0.01663	0.07613	0.09306	0.0002999	SDFFOX2

m0/g15155	7.836e-05	3.531e-05	0.0001346	2.097e-05	NAND2XL
m0/g16127	4.075e-05	1.713e-05	0.0001304	7.256e-05	NAND2BX1
m0/g15439	4.008e-05	5.273e-05	0.0001281	3.532e-05	NOR2XL
inc_p3_add_175_41/g94	5.568e-05	2.675e-05	0.0001256	4.322e-05	AND3X1
m0/g15473	5.573e-05	3.496e-05	0.0001251	3.532e-05	NOR2XL
g1183	6.255e-05	3.978e-05	0.0001234	2.103e-05	NAND4XL
m0/g14819	5.749e-05	1.587e-05	0.0001215	4.89e-05	A0I31X1
g1097	5.054e-05	2.855e-05	0.0001144	3.532e-05	NOR2XL
g1184	5.586e-05	3.748e-05	0.0001144	2.103e-05	NAND4XL
m0/g15438	4.292e-05	2.6e-05	0.0001042	3.532e-05	NOR2XL
m0/g15413	5.055e-05	2.325e-05	9.464e-05	2.085e-05	0A121XL
inc_p2_add_175_41/g95	2.161e-05	5.176e-05	9.435e-05	2.097e-05	NAND2XL
g1098	3.839e-05	2.624e-05	9.395e-05	3.532e-05	NOR2XL
m0/g15153	4.618e-05	2.477e-05	9.192e-05	2.097e-05	NAND2XL
m0/g15468	2.504e-05	4.452e-05	9.052e-05	2.097e-05	NAND2XL
inc_p3_add_175_41/g95	1.943e-05	4.798e-05	8.798e-05	2.097e-05	NAND2XL
m0/g15154	3.524e-05	2.626e-05	8.447e-05	2.097e-05	NAND2XL
m0/g15440	1.707e-05	2.871e-05	8.118e-05	3.532e-05	NOR2XL
m0/g14910	3.008e-05	4.075e-05	8.019e-05	2.097e-05	0A121X1
m0/g15451	1.49e-05	4.148e-05	7.280e-05	2.097e-05	NAND2XL
inc_p1_add_175_41/g94	2.22e-05	5.649e-06	7.506e-05	4.322e-05	AND3X1
inc_p2_add_175_41/g94	2.187e-05	9.156e-06	7.474e-05	4.322e-05	AND3X1
m0/g15464	2.818e-05	2.025e-05	6.941e-05	2.097e-05	NAND2XL
inc_p0_add_175_41/g90	1.463e-05	3.63e-05	6.591e-05	2.097e-05	NAND2XL
m0/g15259	1.349e-05	2.422e-06	6.507e-05	4.916e-05	0A121X1
m0/g15466	1.882e-05	2.381e-05	6.366e-05	2.097e-05	NAND2XL
g1096	1.589e-05	7.117e-06	5.832e-05	3.532e-05	NOR2XL
m0/g15441	1.247e-05	2.372e-05	5.717e-05	2.097e-05	NAND2XL
m0/g14673	1.369e-05	5.314e-06	5.431e-05	3.532e-05	NOR2XL
g1095	1.231e-05	4.911e-06	5.253e-05	3.532e-05	NOR2XL
m0/g14983	1.936e-05	5.314e-06	4.565e-05	2.097e-05	NAND2XL
inc_p3_add_175_41/g90	7.088e-06	1.523e-05	4.329e-05	2.097e-05	NAND2XL
m0/g15443	1.397e-05	7.522e-06	4.247e-05	2.097e-05	NAND2XL
m0/g16156	9.951e-06	1.544e-06	4.077e-05	2.920e-05	0A121X1
m0/g15410	9.035e-06	9e-06	3.991e-05	2.097e-05	NAND2XL
m0/g15393	4.411e-06	1.492e-06	3.545e-05	2.95e-05	CLKINVX1
m0/g15442	5.015e-06	3.852e-06	2.984e-05	2.097e-05	NAND2XL
inc_p1_add_175_41/g90	2.635e-06	5.788e-06	2.946e-05	2.097e-05	NAND2XL
inc_p2_add_175_41/g90	2.276e-06	5.266e-06	2.852e-05	2.097e-05	NAND2XL
m0/g15444	4.081e-06	3.232e-06	2.829e-05	2.097e-05	NAND2XL
m0/g15445	3.321e-06	3.062e-06	2.736e-05	2.097e-05	NAND2XL
m0/g15414	4.358e-06	1.729e-06	2.706e-05	2.097e-05	NAND2XL
m0/g15457	3.936e-06	1.587e-06	2.656e-05	2.097e-05	NAND2XL
m0/fopt16284	2.659e-06	2.025e-06	2.566e-05	2.097e-05	INVXL

Total ( 2797 of 2797 )      10.63      12.01      22.88      0.2437  
Total Capacitance      9.125e-11 F  
Power Density      \*\*\* No Die Area \*\*\*

The report is too big to incorporate into the report

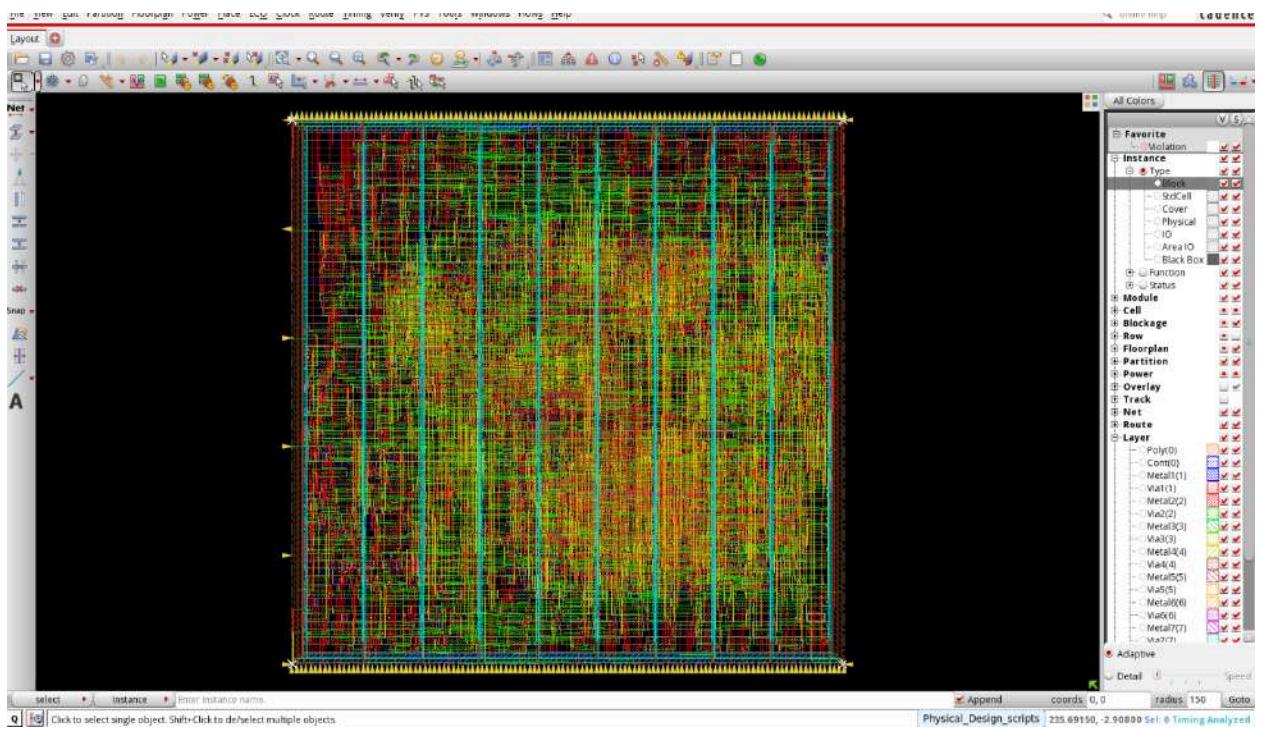
In this report, internal power is the power dissipated inside the cell boundary during charging and discharging of existing capacitances. Total Internal Power is 10.63mW

Switching power of driving cell is the power dissipated by charging load capacitance at the output. The total switching power is 12.01mW

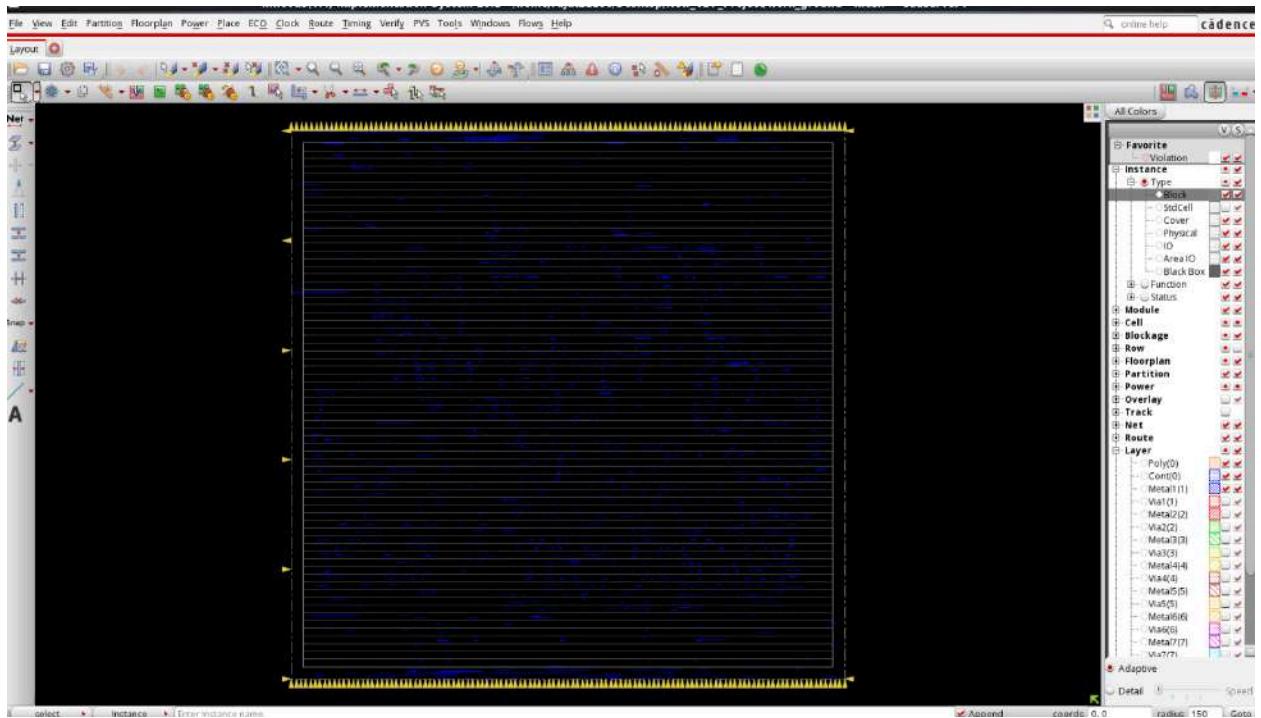
Leakage power is generated from the leakage current that flows between VDD and GND when there is no switching. The total leakage power is 0.2437mW

The total power which is the sum of all these is 22.88mW

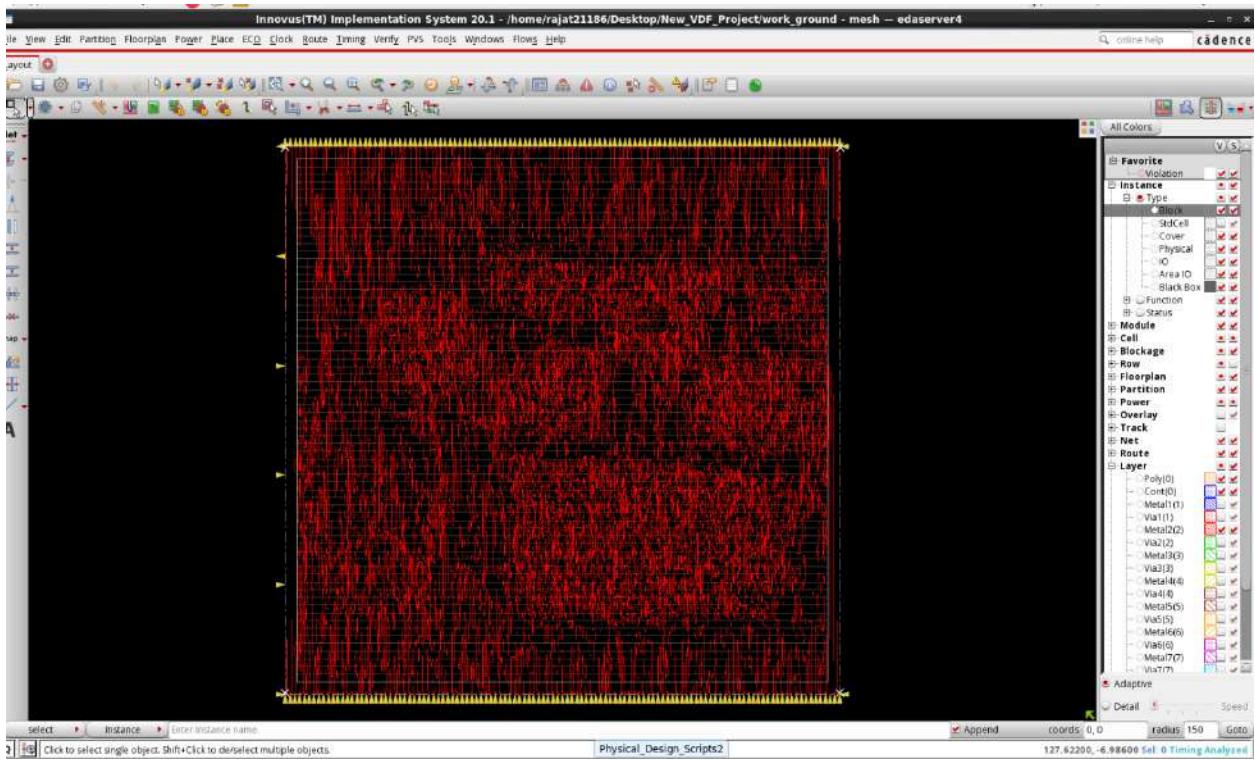
Layout Screenshot



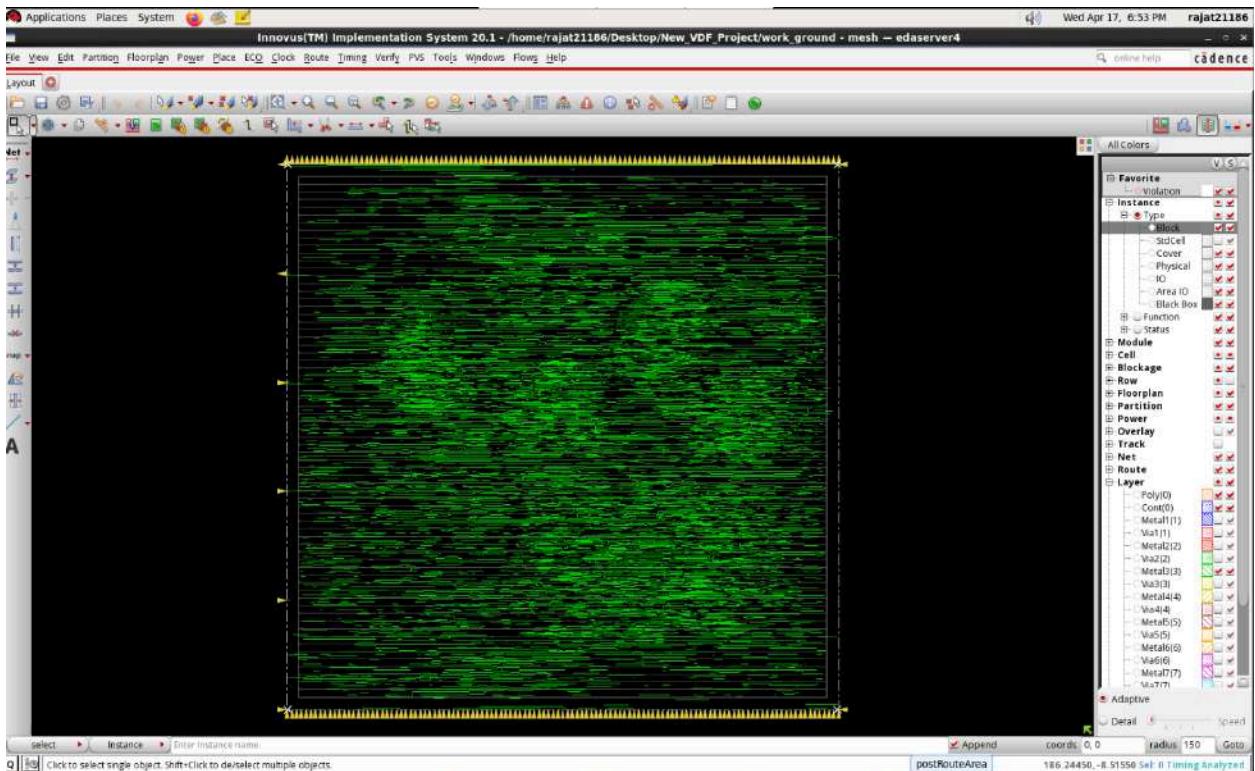
## Metal 1 Layer



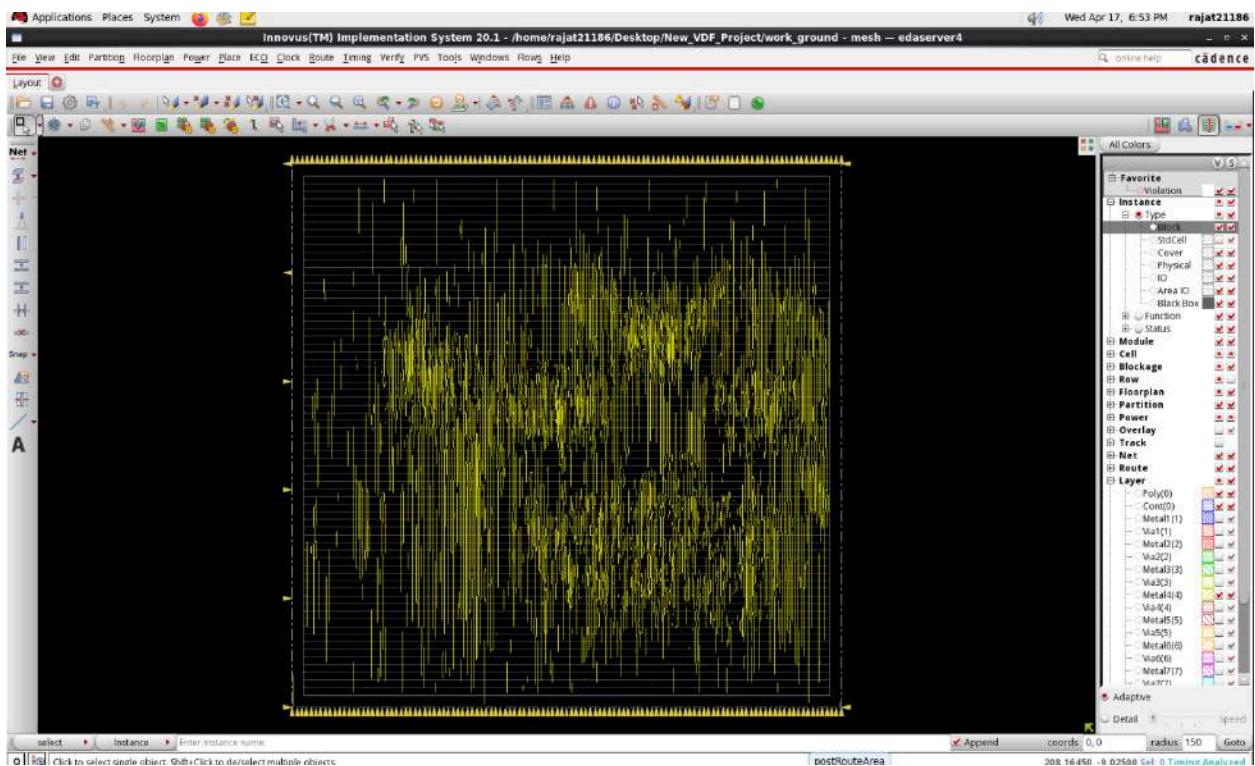
## Metal 2 Layer



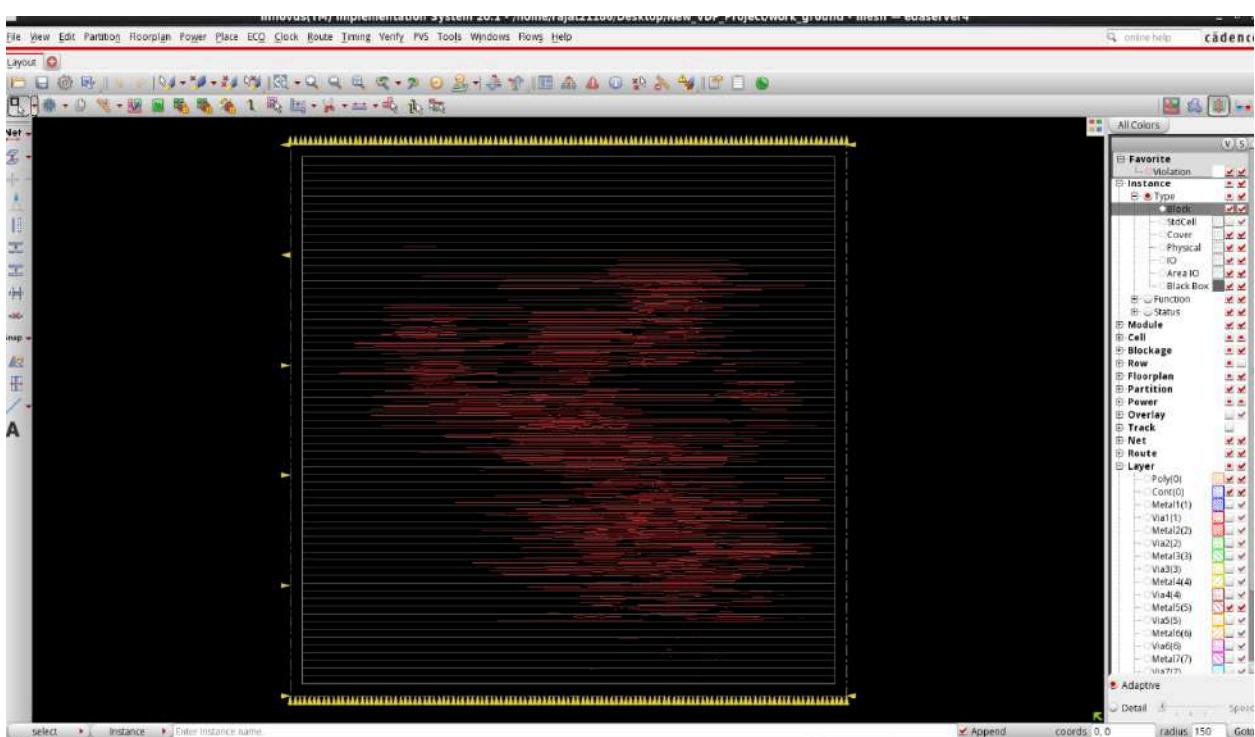
## Metal 3 Layer



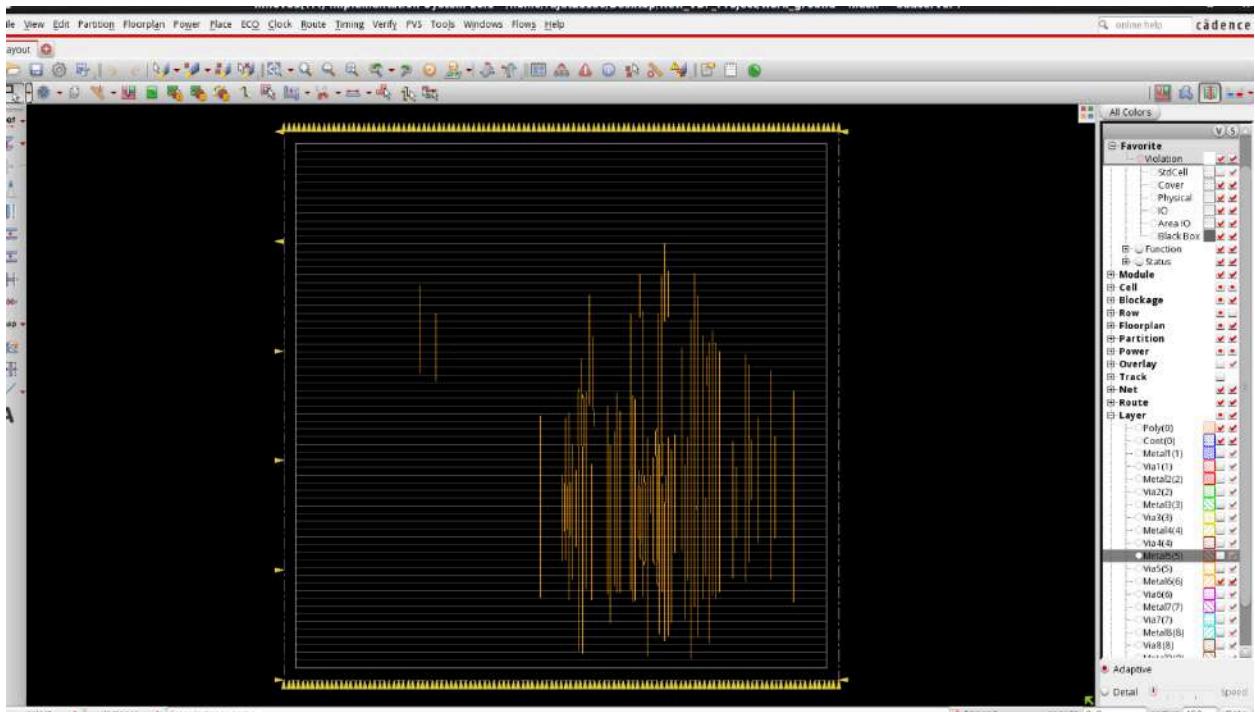
## Metal 4 Layer



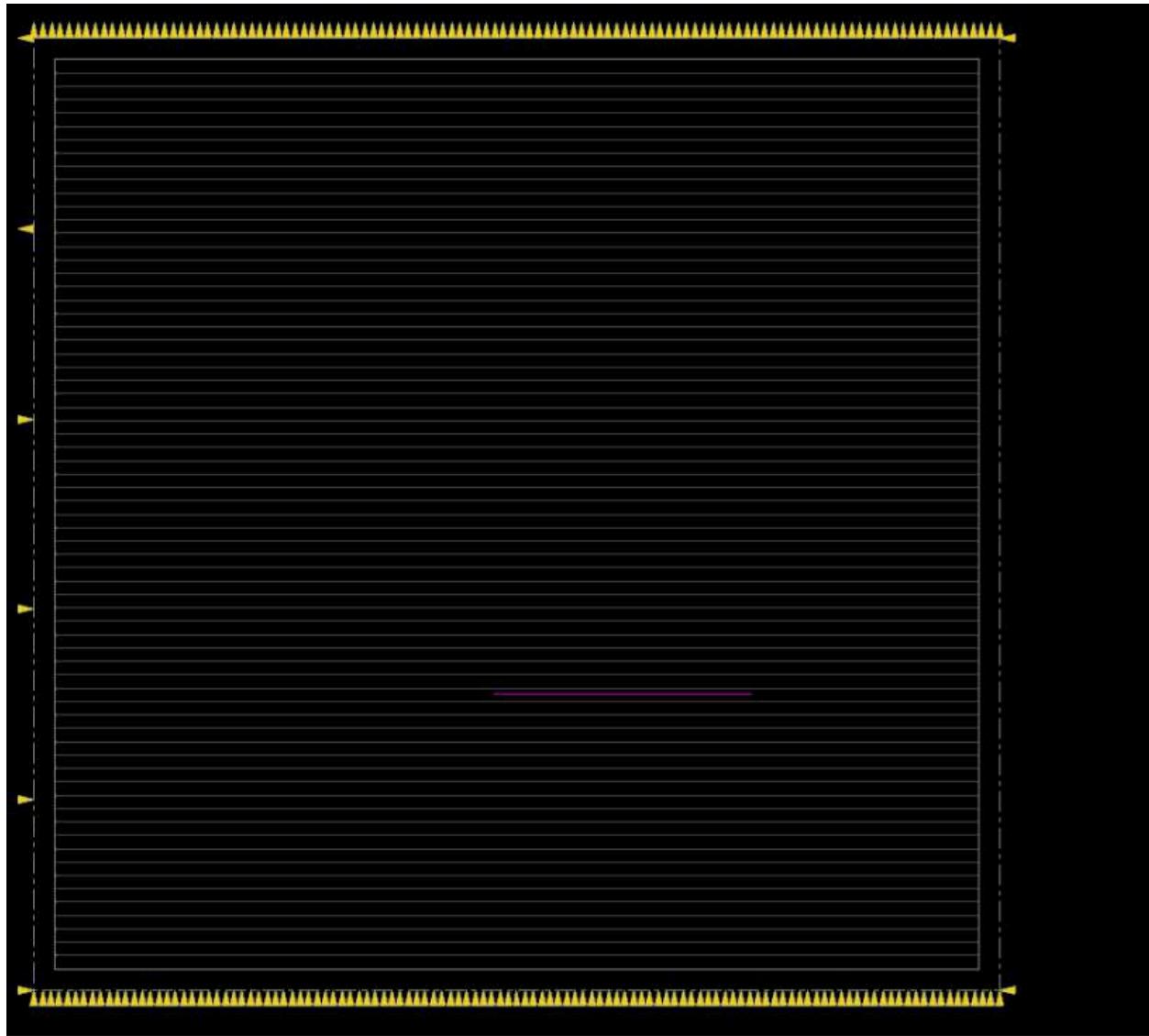
## Metal 5 Layer



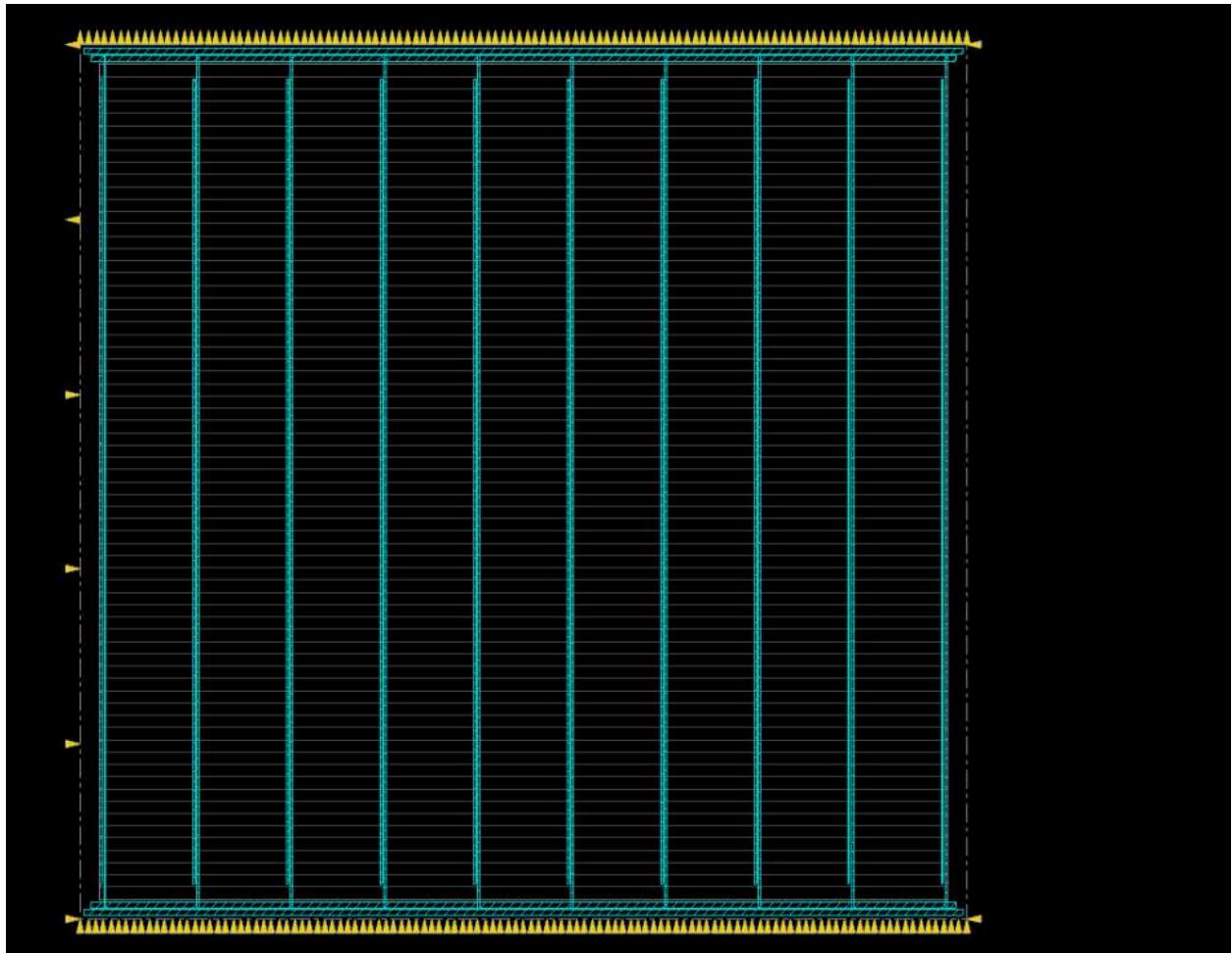
## Metal 6 Layer



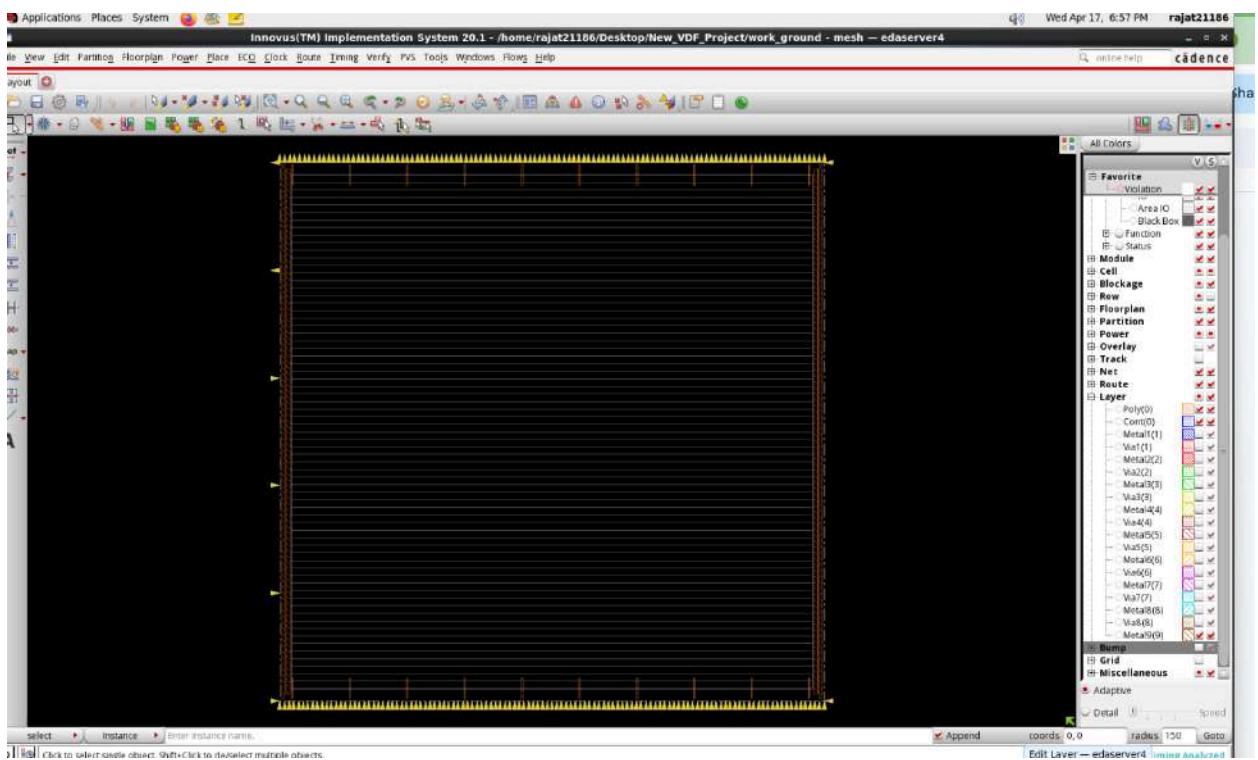
## Metal 7 Layer



Metal 8 Layer



## Metal 9 Layer



## Effect of metal layers on overall timing

As the number of metal layers increases, the resistance of the interconnects also increases, leading to higher delays. Also, with more metal layers, the slack decreases because signals would have to pass through vias to transition between layers. These vias also contribute to delays. Although, use of thicker metal layers can reduce resistance, the requirement for additional vias trades off this improvement, resulting in increased delays overall. This slows down the overall timing of the circuit.