Chapter 6 · Section 6.2 — Exercises (Mazidi)

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> Problems are paraphrased to respect copyright. Short, teachable answers below.

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15) True or false. In ARM the R13 is designated as stack pointer.

Answer: True. R13 is the architectural **SP** (banked per mode on classic ARM).

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16) When BL is executed, how many stack locations are used?

Answer: Zero. `BL` stores the **return address** in **LR (R14)**; the stack is used **only if** your code saves LR (e.g., `PUSH {LR}`).

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17) When B is executed, how many stack locations are used?

Answer: Zero. `B` is a plain branch and does **not** touch the stack.

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18) In ARM, stack pointer is _____ register.

Answer: R13 (SP).

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19) Describe how the return operation is performed in ARM.

Answer: Restore PC from LR. Common sequences:

```
BX   LR          ; preferred (keeps ARM/Thumb state)
; or
MOV  PC, LR      ; simple return
; if LR was saved on stack:
POP  {PC}         ; load PC from stack (also returns)
```

Prologue/epilogue pattern for subroutines that call others:

```
PUSH {LR}      ; save caller's return
...              ; body, may BL further routines
POP  {PC}      ; restore and return
```

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20) Give the size of the stack in ARM.

Answer: Not fixed by the ISA. Stack size is configured by your **linker/RTOS** and limited by **RAM**. Each pushed register occupies **4 bytes** (32-bit words); the stack **grows downward** on classic ARM (full-descending).

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21) In ARM, which address is saved when `BL` is executed?

Answer: The **address of the instruction following** `BL` (the **return address**) is saved into **LR (R14)**.

Notes for learners

- Many exception/privileged modes have **banked SP/LR**, so **R13/R14** can differ per mode (e.g., IRQ vs Thread).
- On Cortex-M, `PUSH/POP` mnemonics expand to `STMDB/ LDMIA` with SP and handle multiple registers in one go.