Project On:

Placement and Routing

Course No:

EEE 4231

Submitted To:

Mahmudul Hasan

Lecturer, Dept. of EEE,

Ahsanullah University of Science and Technology

Submitted By:

Name : KAZI MEJBUAL ISLAM
ID : 15.02.05.040
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Section : A

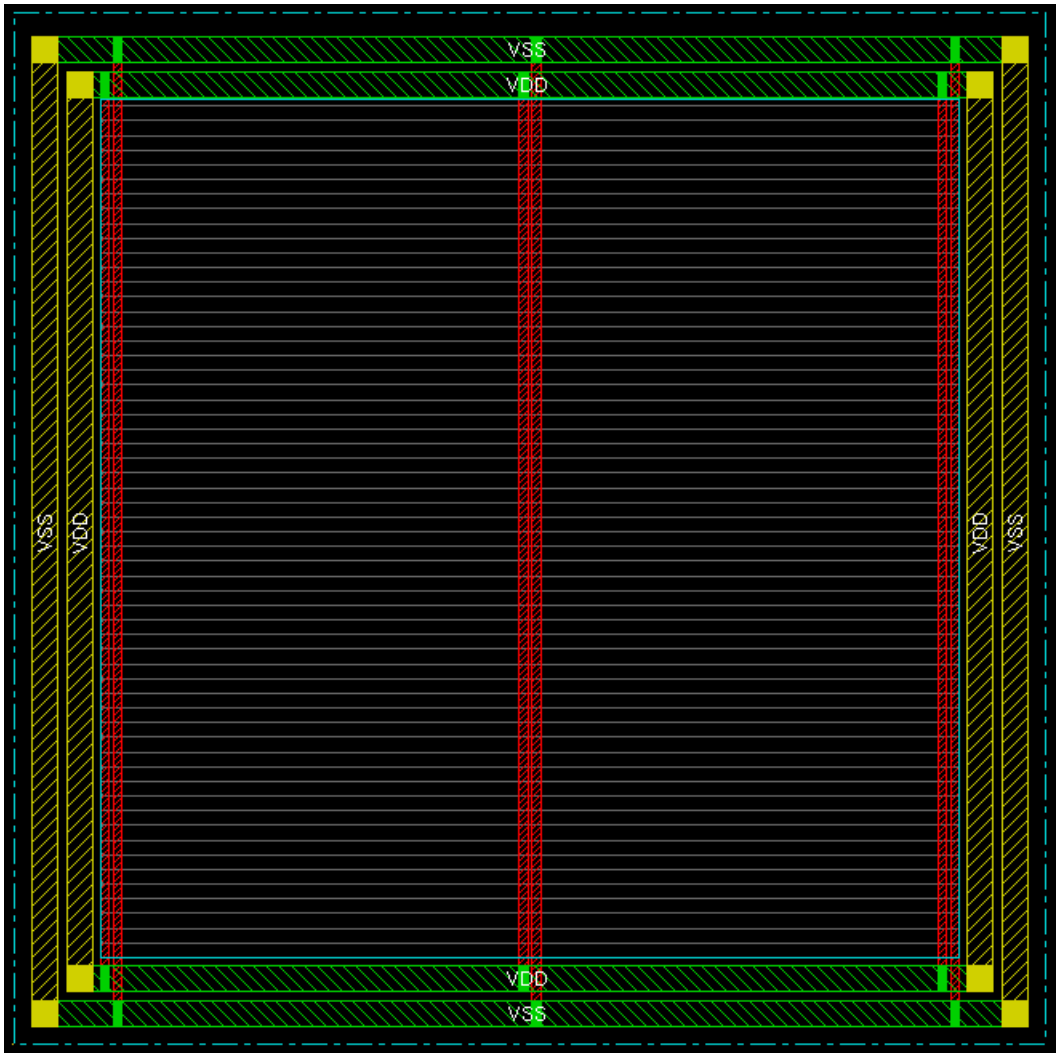
Objectives: The objective is to place and route a chip for which synthesized Verilog code is given. Given its constraints and timing libraries, it should be placed with minimum violations and following all constraints.

Tools: For placement and routing, we have used Encounter, the PnR tool of Cadence. There are other software as well but encounter has a GUI mode and also it can be operated in command window.

Procedures:

First of all the design has to be imported from the Design import section. Here the .lef and .v files are selected and the other files like timing libraries and constraints, captable etc. are introduced. Using all those information the chip will be place.

After that, power stripes should be set up. From power section, it can be done easily.



Here 3 sets of stripes are used for convenience and a ring is formed. All the power connections will go through this path. Then special routing is performed. And the blocks looks like the following:

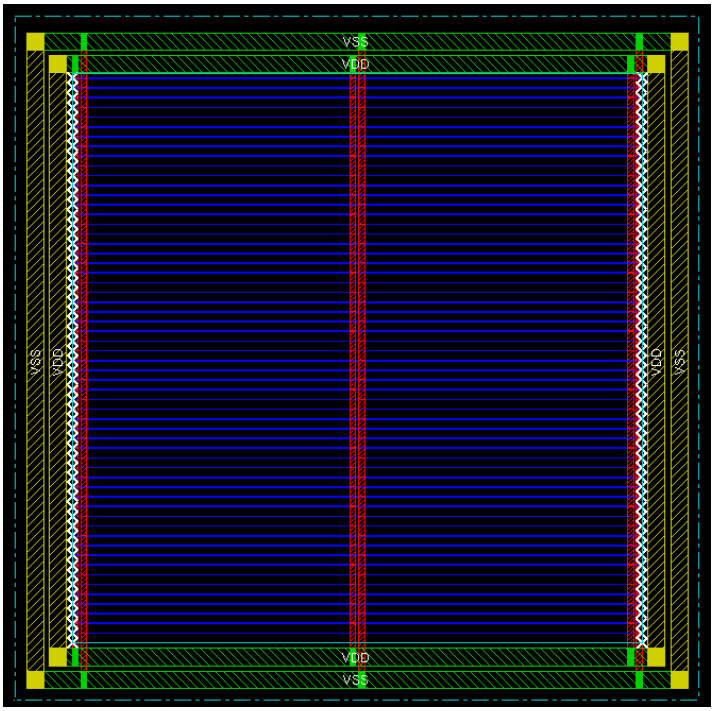


Fig: After Special Routing

After special routing, Pins should be connected. After connecting pins the blocks looked like below. Spacing was 1.4 micron and Metal 1 was used.

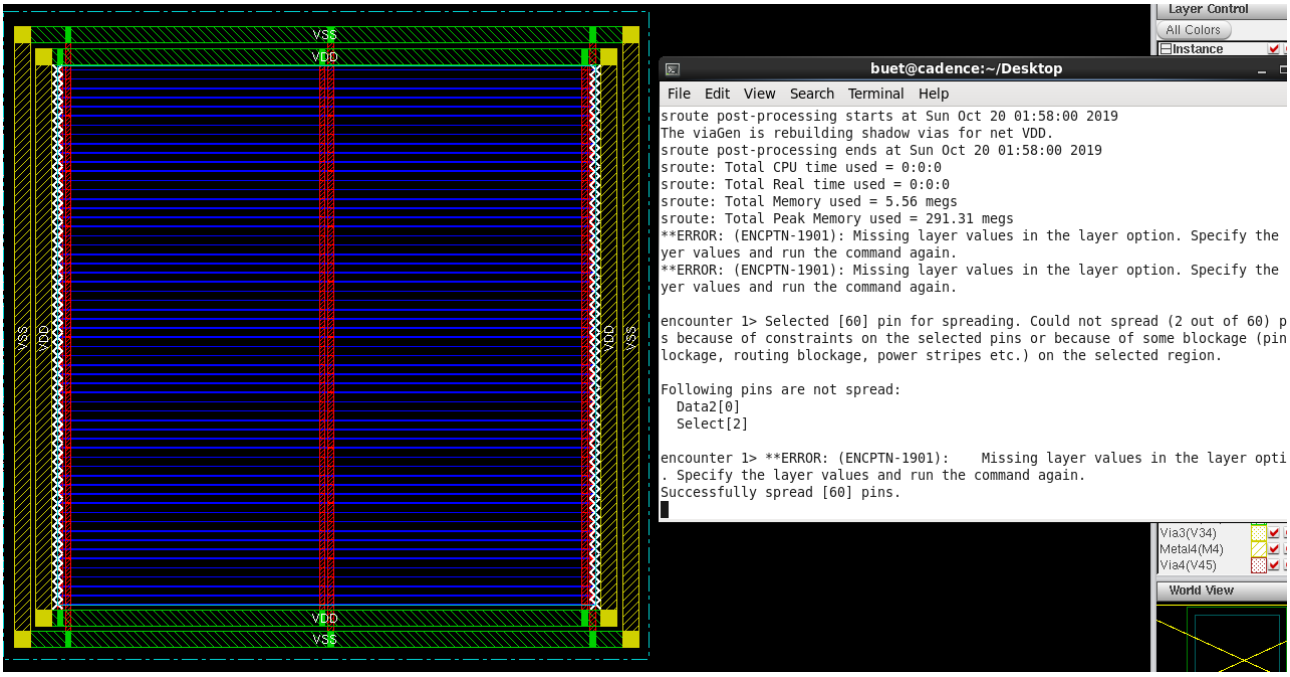


Fig: Pins are connected

After Special routing, the cells are placed. The area of the whole block was kept large intentionally. There was no intention of making it efficient and least place required. Rather, the intention was to lessen the errors only.

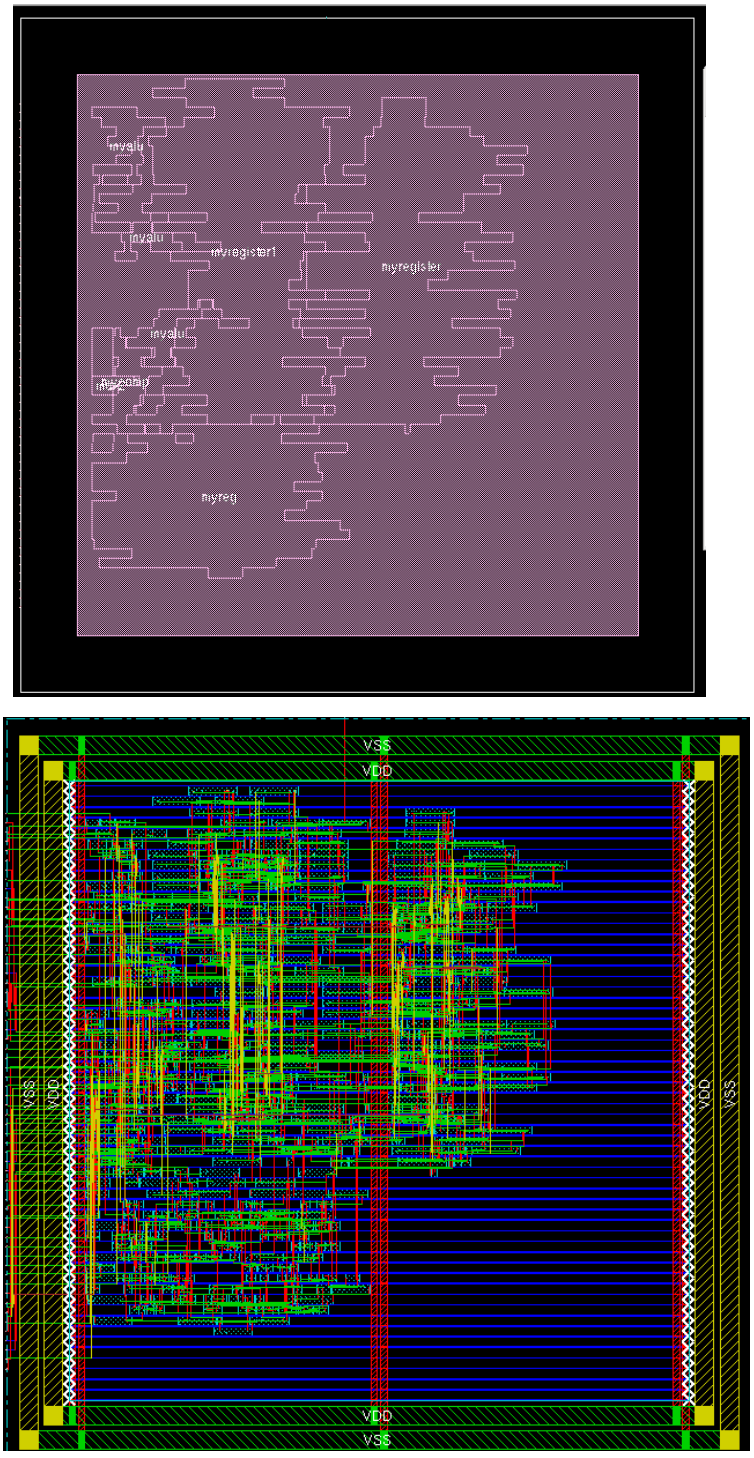


Fig: After placing cells

After placement, here comes the routing part. It can be done using CIW or GUI. I have tried GUI mode. After routing, the block looked like this

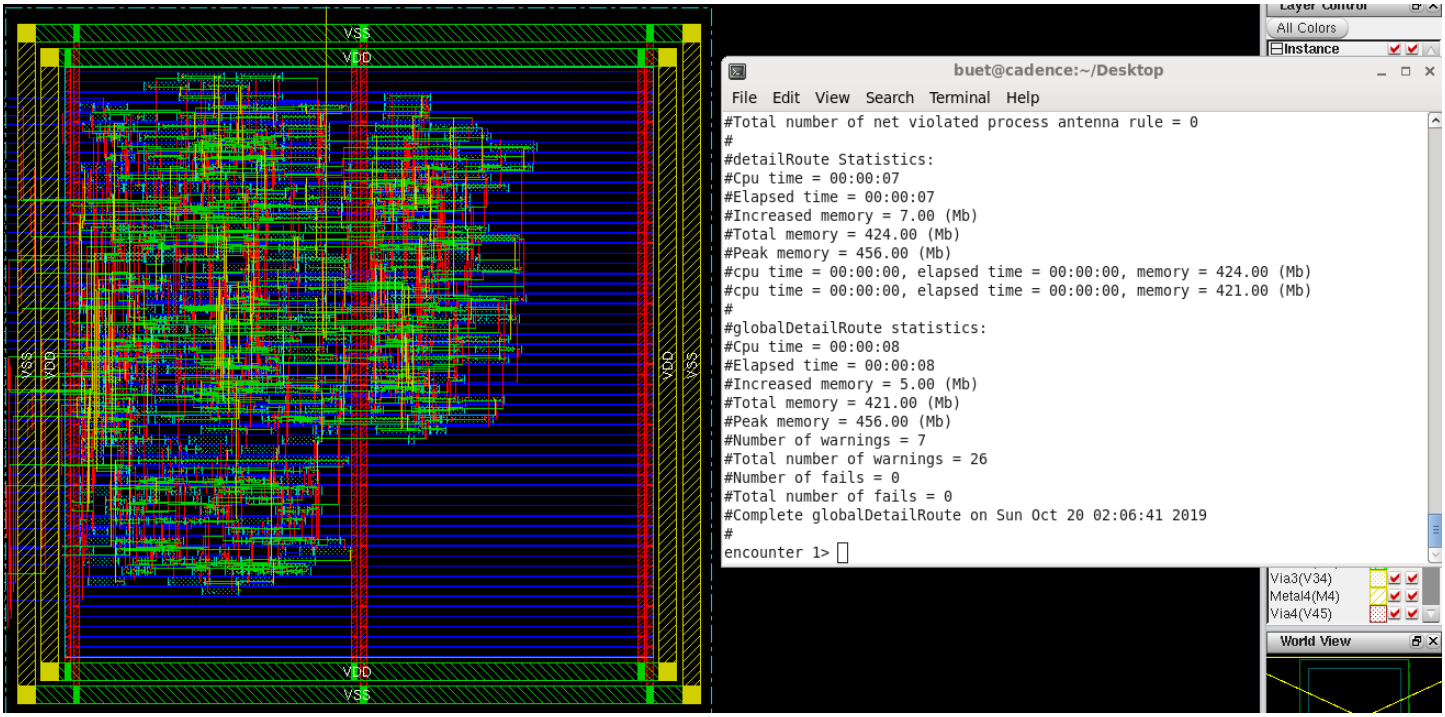
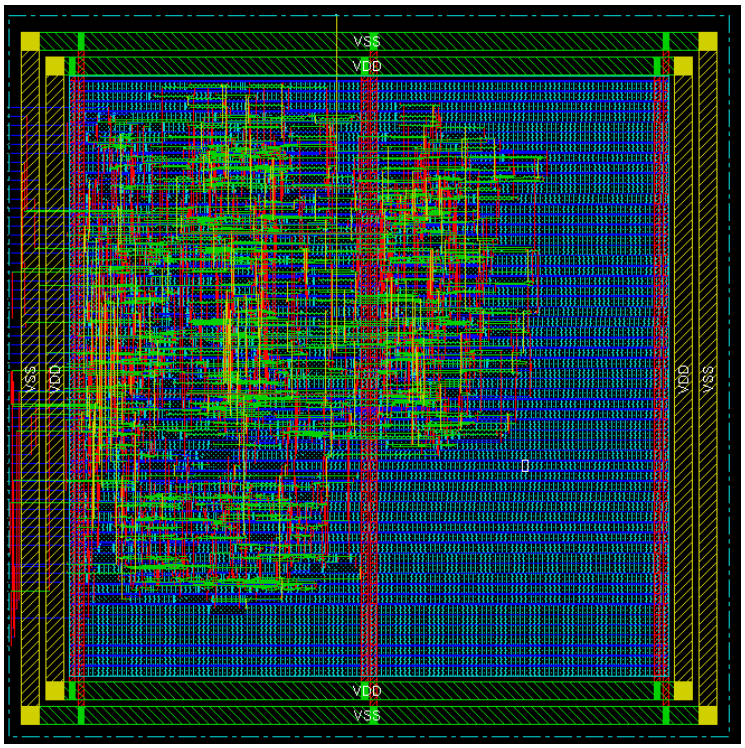


Fig: After Routing

We can see most of the places are blank. Here it needs to add some fillers. So It was done.



Primary placement and routing are done. Now it has to be checked. First the connectivity check

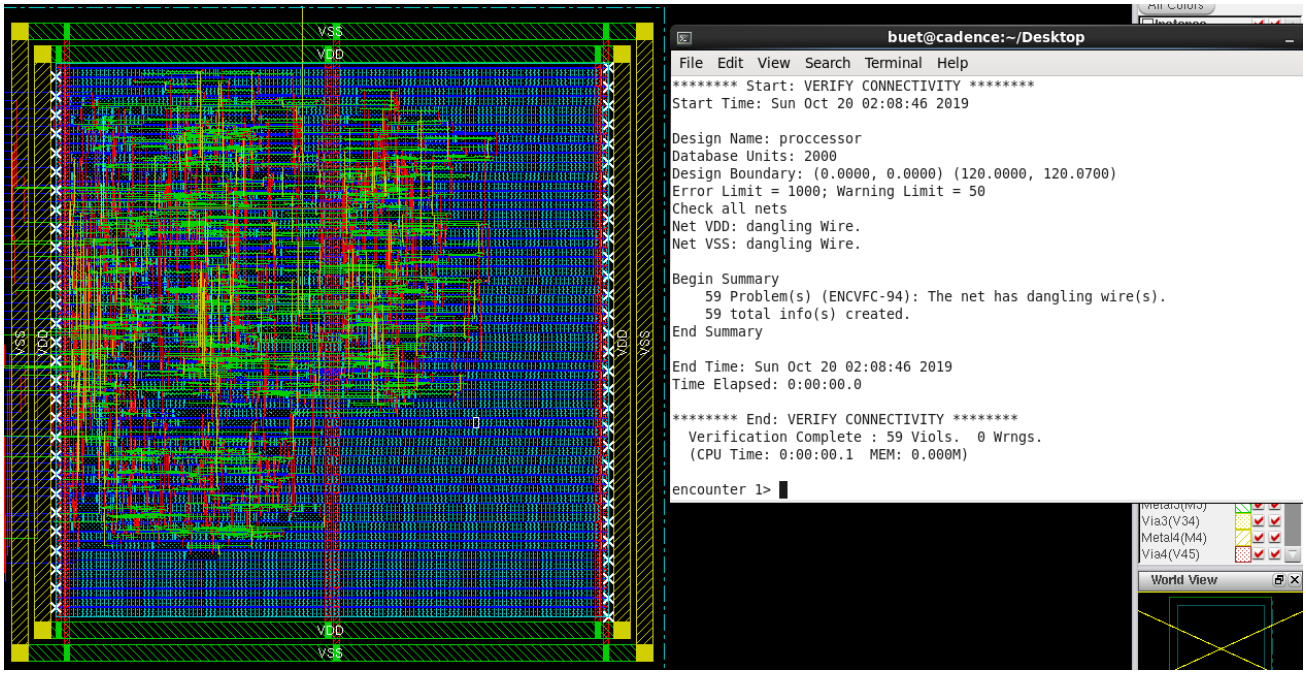


Fig : Connectivity check report

Here we can see 59 violations. We'll correct it later. Then I have poerformed geometry check

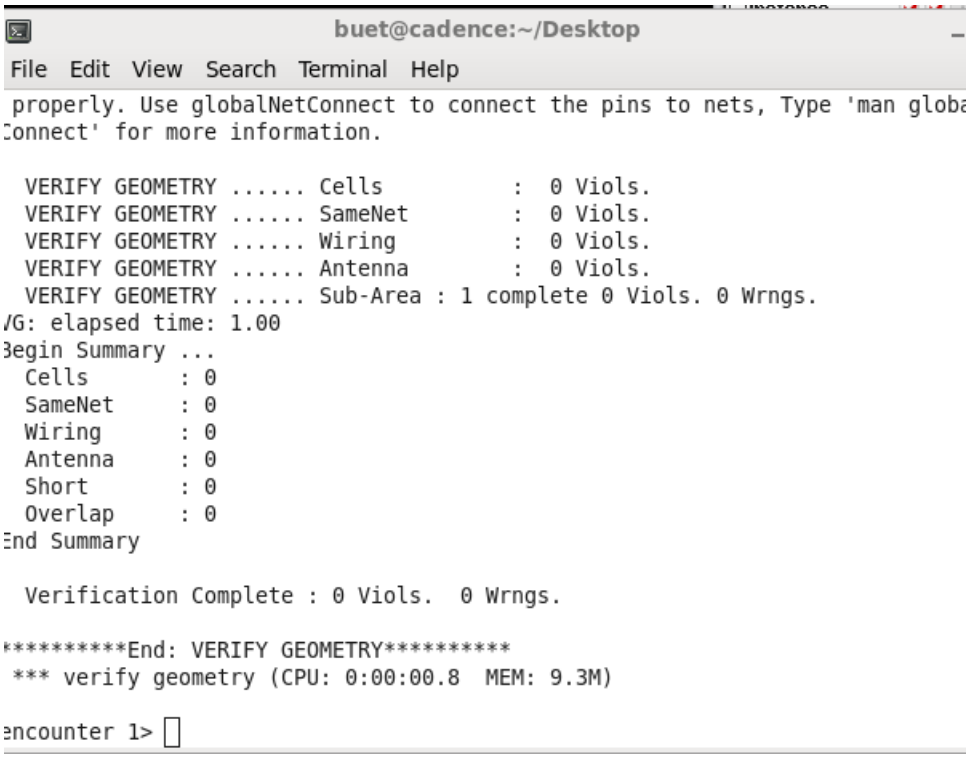


Fig: Geometry check report

We can see there are no voilations in geometry check

To solve connctivity violations, we'll have to make VDD and VSS global. After using commands it looks like the following

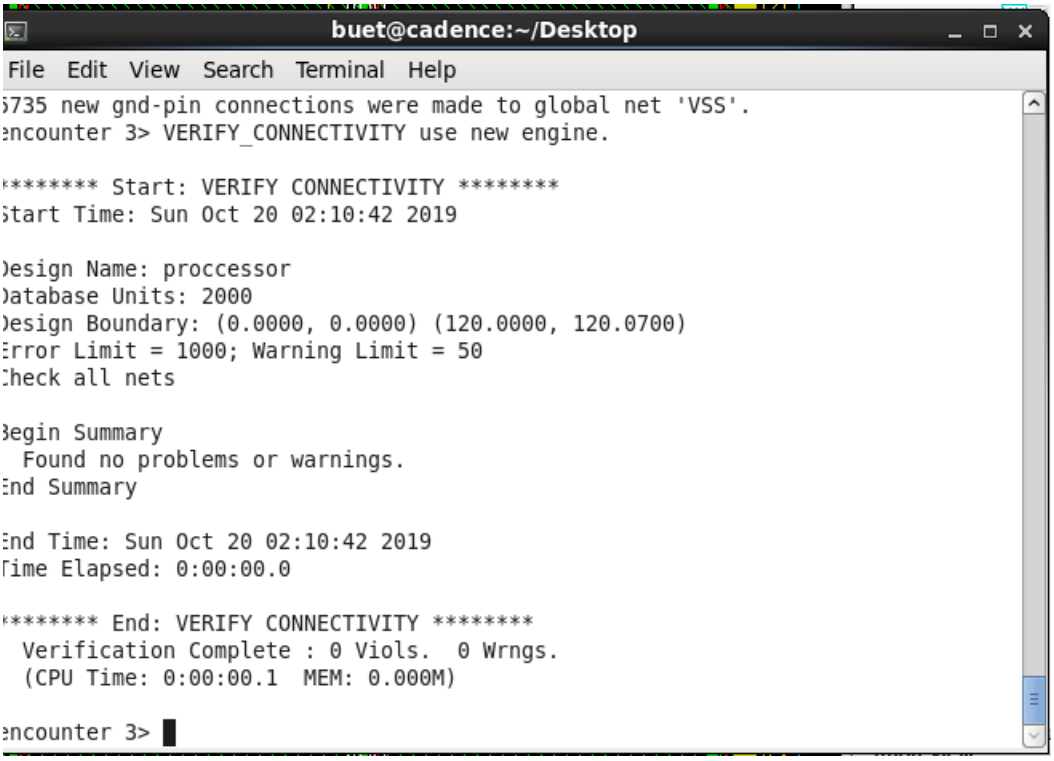


Fig: 0 connectivity violations

Then we have checked the timing violations, setup and hold. And also the DRVs. The reports are provided sequentially.

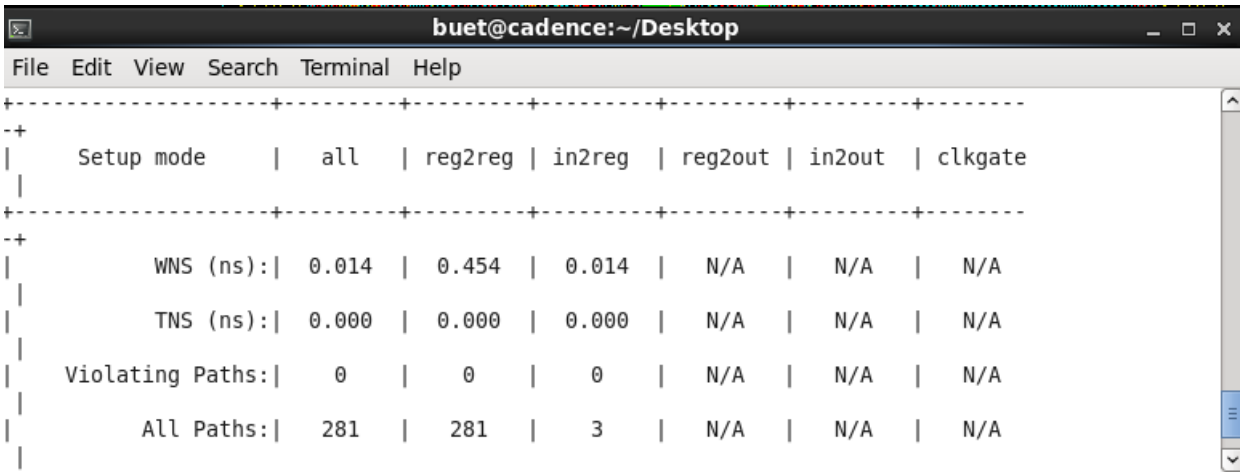


Fig: Setup violations

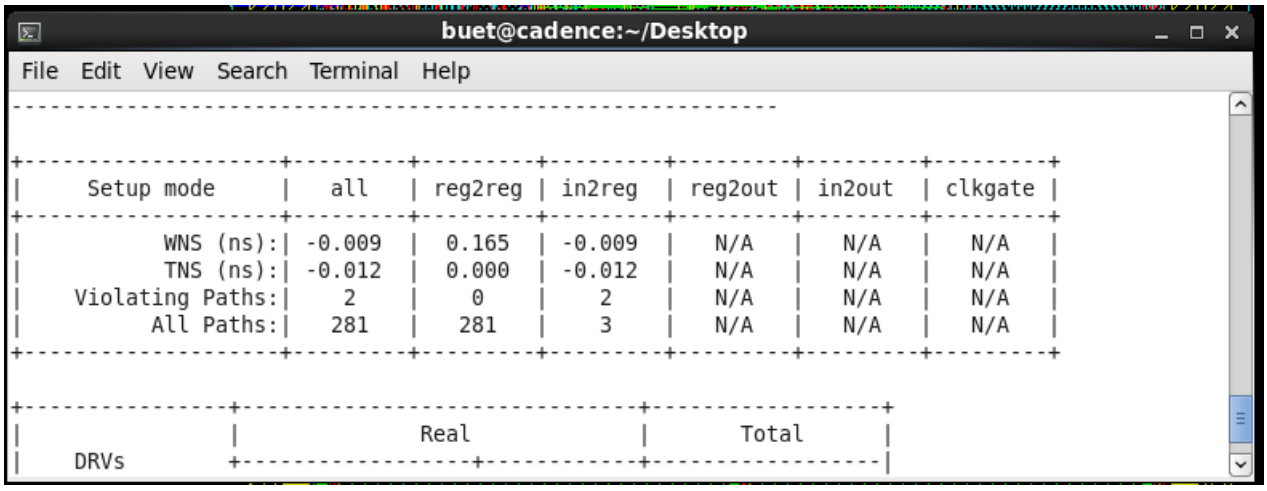
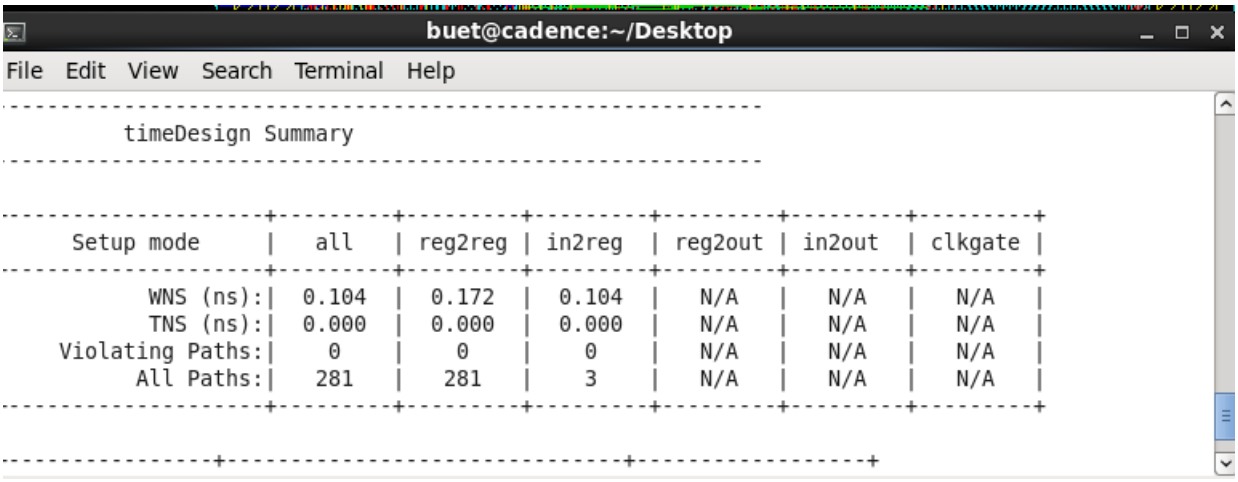


Fig: After preCTS



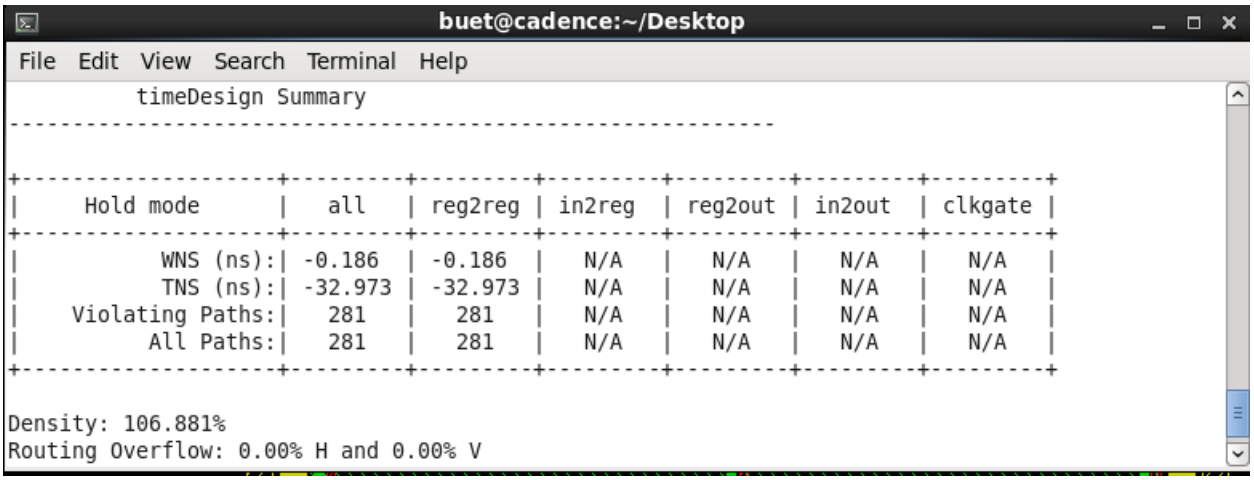


Fig: postCTS hold

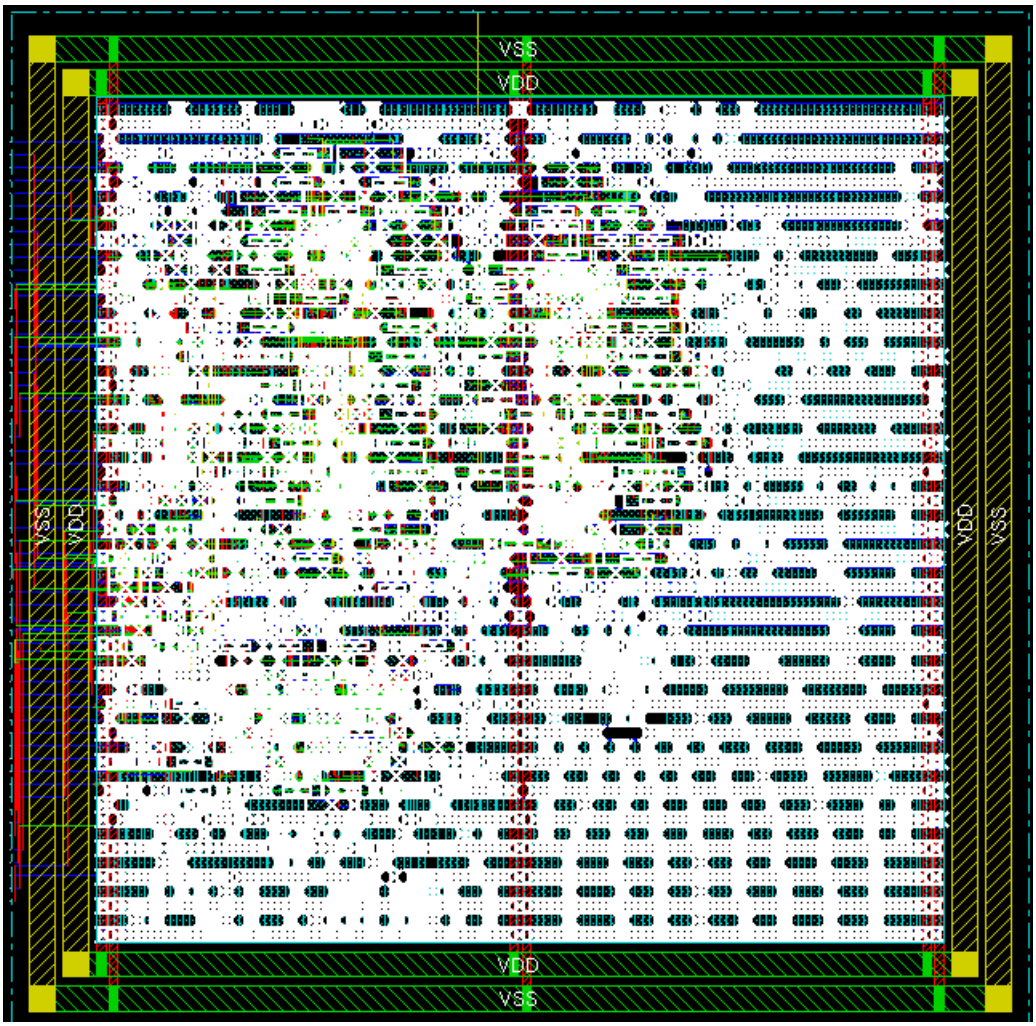


Fig: After 8th iteration, the circuit looked like this

```
# Format : Frame 1 : Split 1

Check type : max_transition
---------------------------
     +-------------------------------------------------------------------+
     | Pin Name                | Required | Actual | Slack  | View      |
     |-------------------------+----------+--------+--------+-----------|
     | mux2/g134/B             | 0.814    | 0.827  | -0.014 | func_slow |
     | myregister1/g2520/B     | 0.814    | 0.824  | -0.010 | func_slow |
     | myregister1/g2518/B     | 0.814    | 0.824  | -0.010 | func_slow |
     | myregister1/g2521/A     | 0.814    | 0.822  | -0.009 | func_slow |
     | myregister1/g2519/AN    | 0.814    | 0.821  | -0.008 | func_slow |
     | myalu/g886/A            | 0.814    | 0.817  | -0.003 | func_slow |
     | myalu/g887/AN           | 0.814    | 0.817  | -0.003 | func_slow |
     | FE_PDC4_immediate_1_/A  | 0.814    | 0.814  | -0.001 | func_slow |
     +-------------------------------------------------------------------+
encounter 22>
```

Fig: The maximum transition violators.

Conclusion:

All the errors could not be removed due to time constraints and tools. DRC could not be checked as the license is not available. Setup violations could be cleaned up but the hold violation remains. Further operation can be performed for fanout, drv and hold.