

Project On:

# Placement and Routing

Course No:  
EEE 4231

Submitted To:

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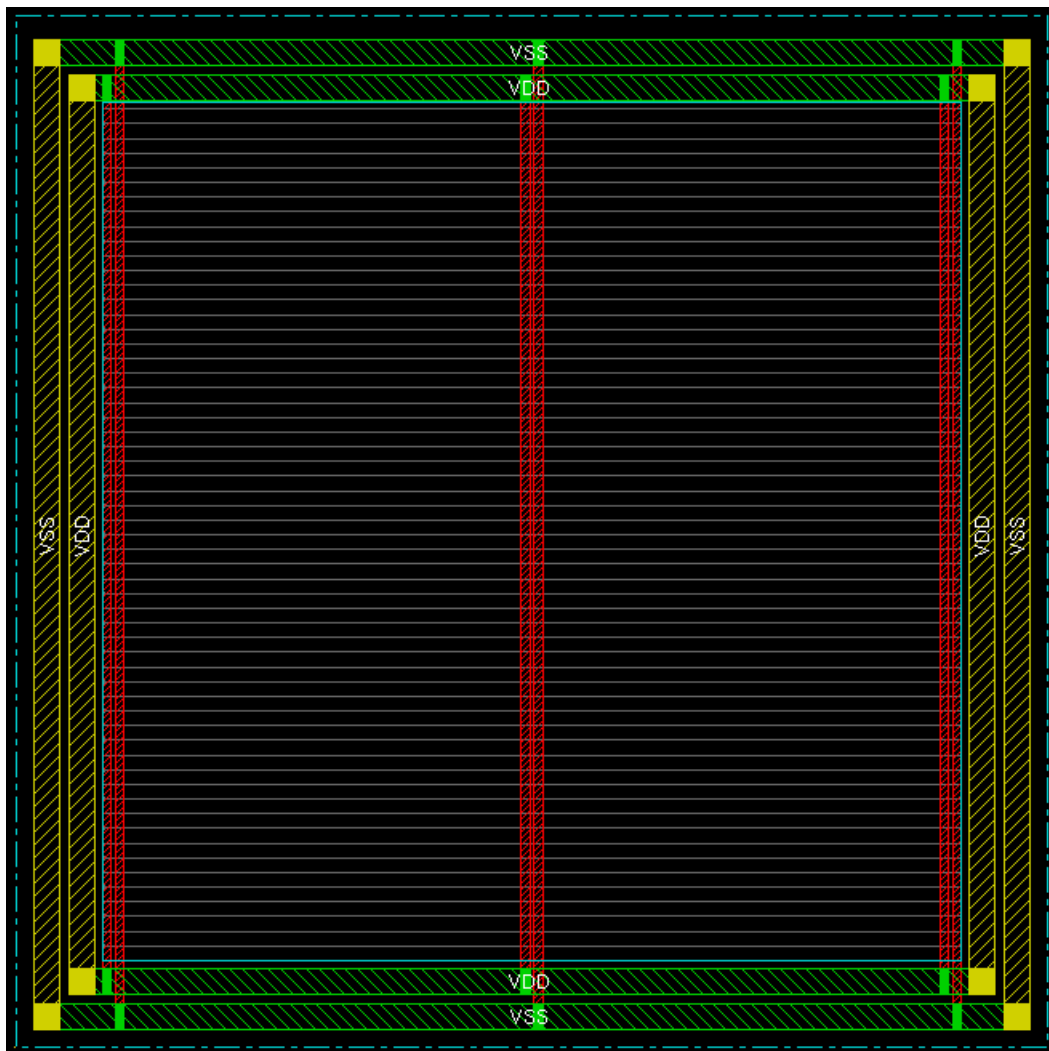
**Objectives:** The objective is to place and route a chip for which synthesized Verilog code is given. Given its constraints and timing libraries, it should be placed with minimum violations and following all constraints.

**Tools:** For placement and routing, we have used Encounter, the PnR tool of Cadence. There are other software as well but encounter has a GUI mode and also it can be operated in command window.

### Procedures:

First of all the design has to be imported from the Design import section. Here the .lef and .v files are selected and the other files like timing libraries and constraints, captable etc. are introduced. Using all those information the chip will be place.

After that, power stripes should be set up. From power section, it can be done easily.



Here 3 sets of stripes are used for convenience and a ring is formed. All the power connections will go through this path. Then special routing is performed. And the blocks looks like the following:

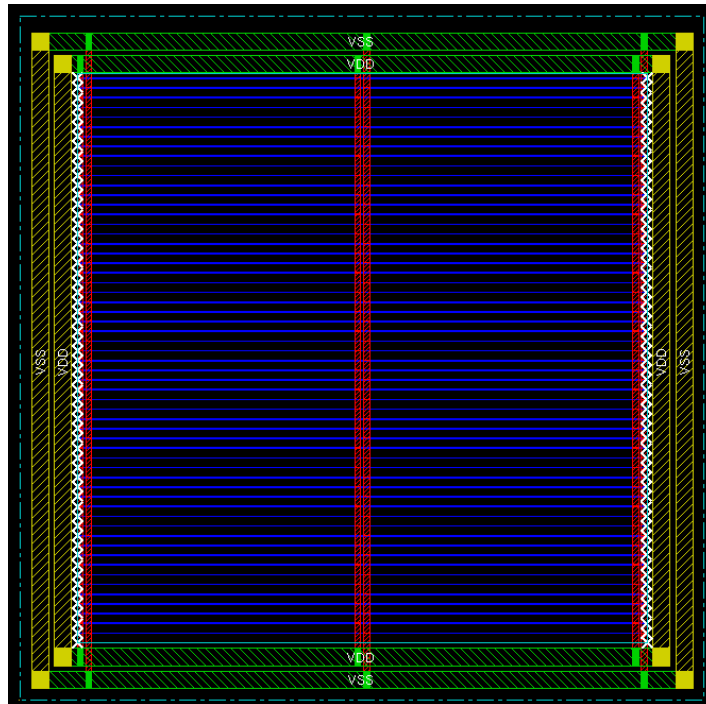


Fig: After Special Routing

After special routing, Pins should be connected. After connecting pins the blocks looked like below. Spacing was 1.4 micron and Metal 1 was used.

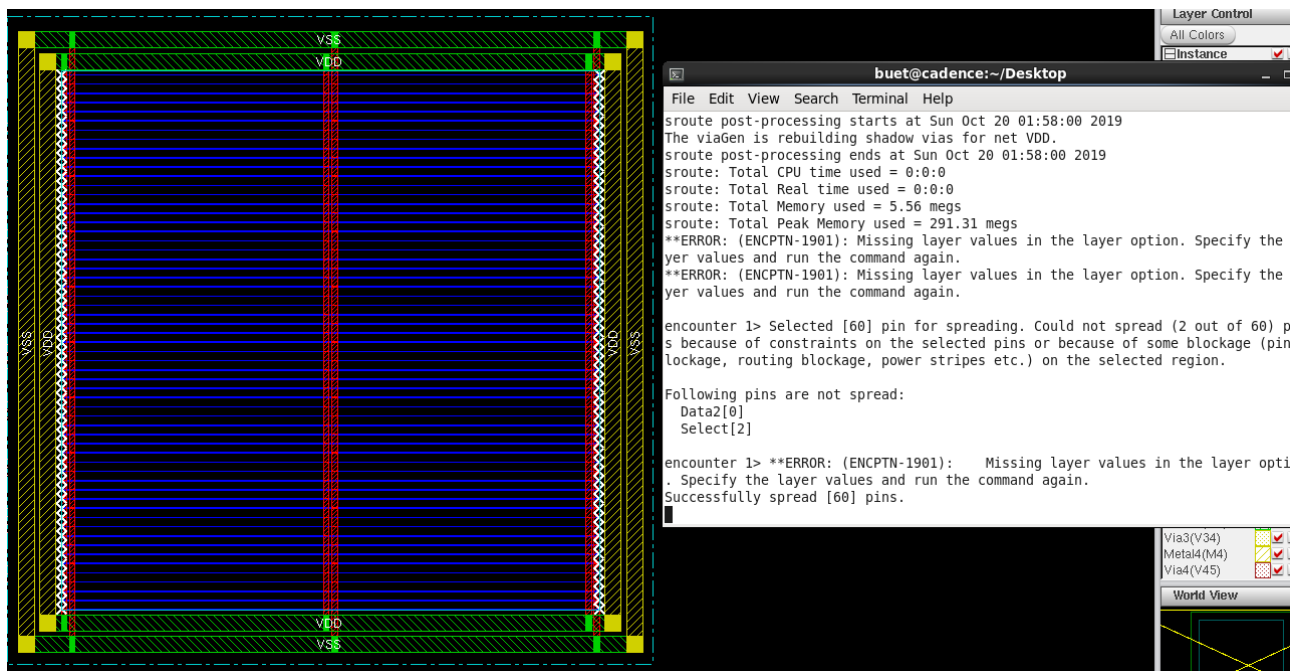


Fig: Pins are connected

After Special routing, the cells are placed. The area of the whole block was kept large intentionally. There was no intention of making it efficient and least place required. Rather, the intention was to lessen the errors only.

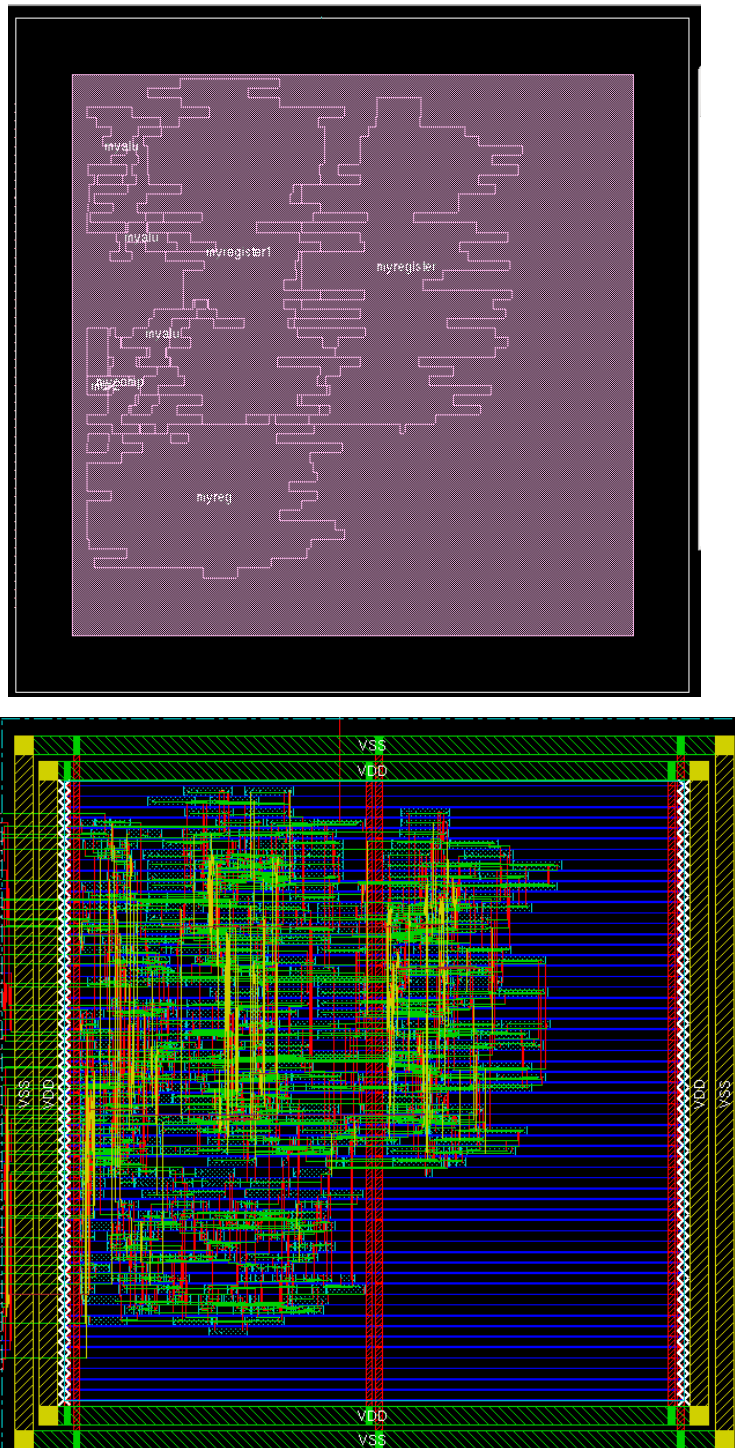


Fig: After placing cells

After placement, here comes the routing part. It can be done using CIW or GUI. I have tried GUI mode. After routing, the block looked like this

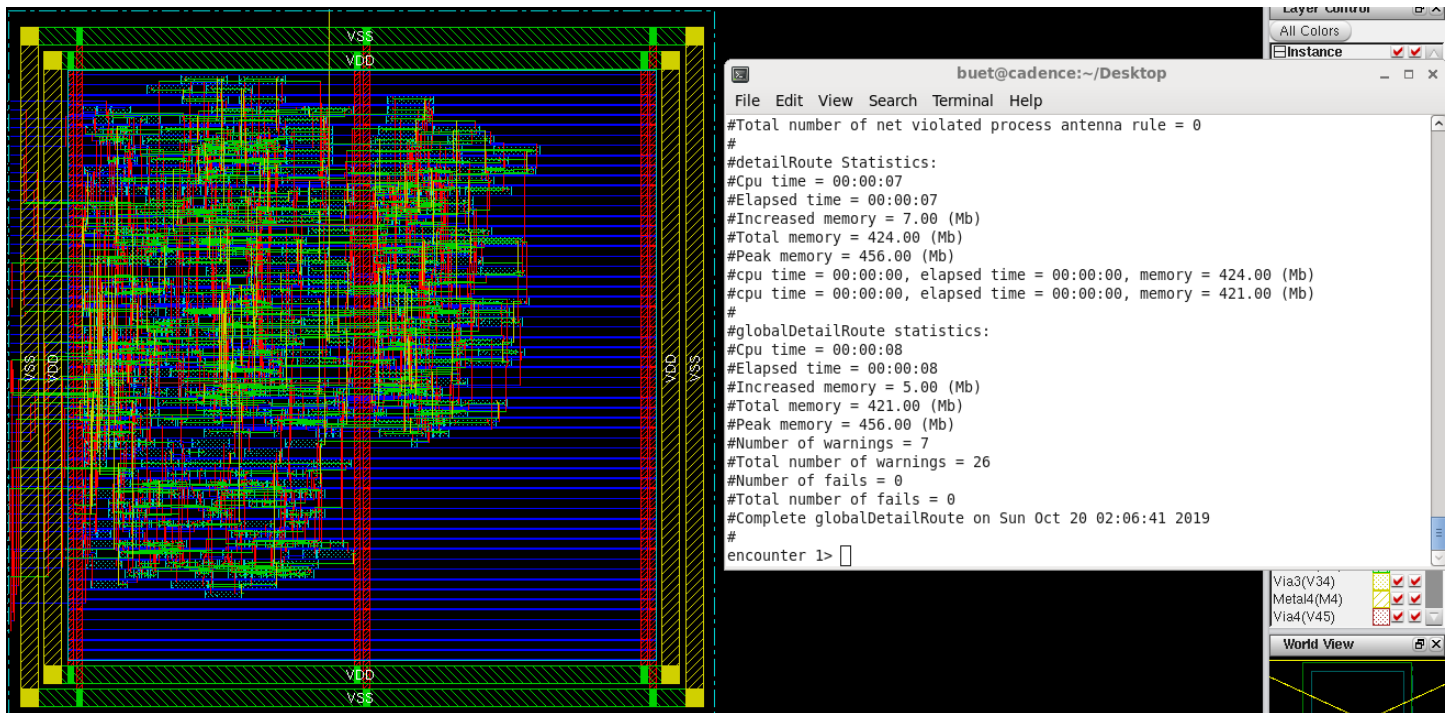
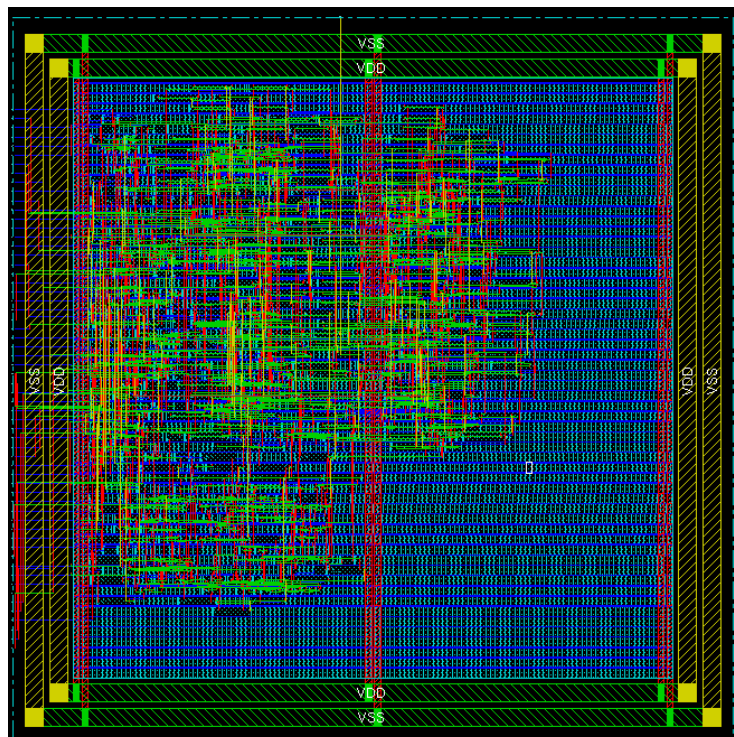


Fig: After Routing

We can see most of the places are blank. Here it needs to add some fillers. So It was done.





Primary placement and routing are done. Now it has to be checked. First the connectivity check

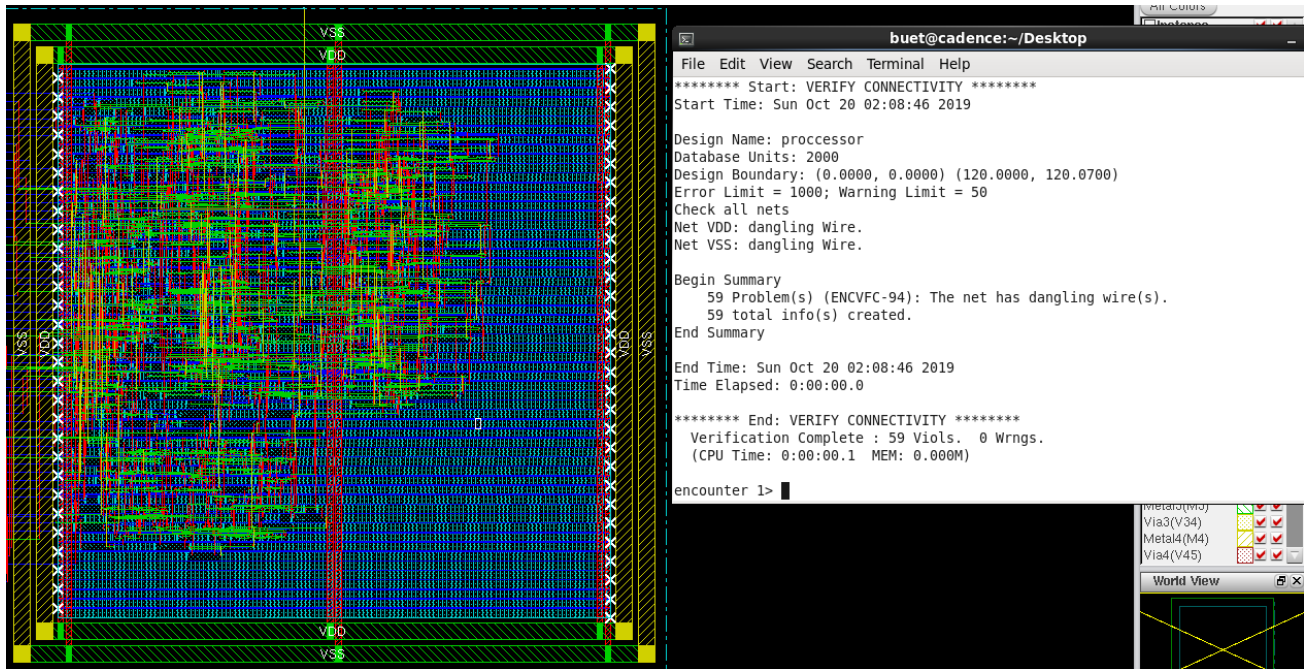


Fig : Connectivity check report

Here we can see 59 violations. We'll correct it later. Then I have performed geometry check

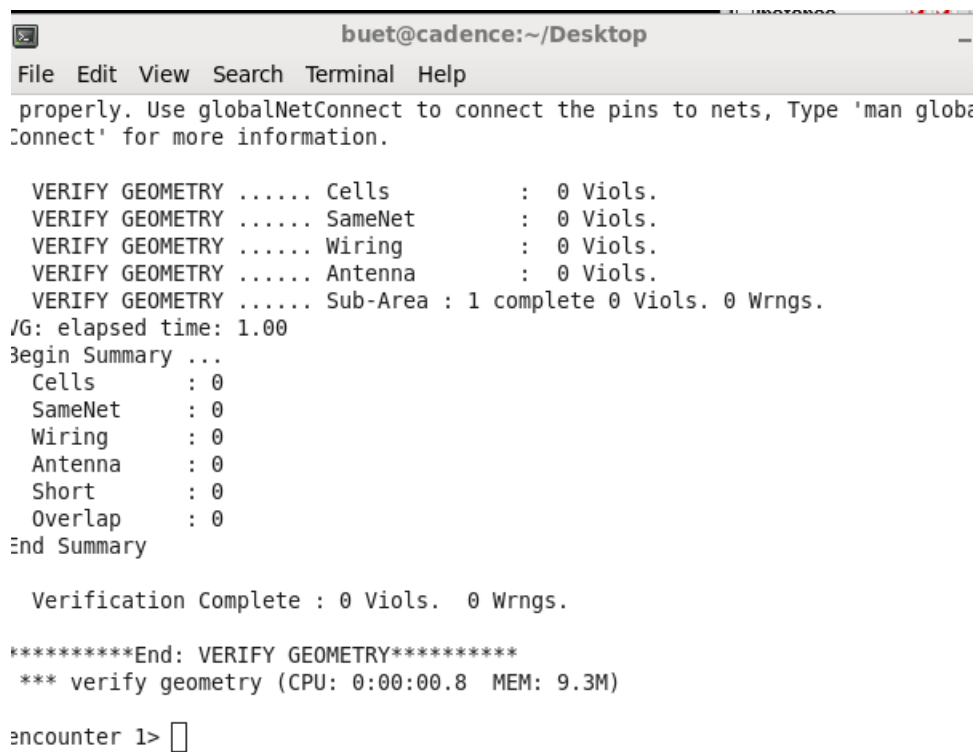
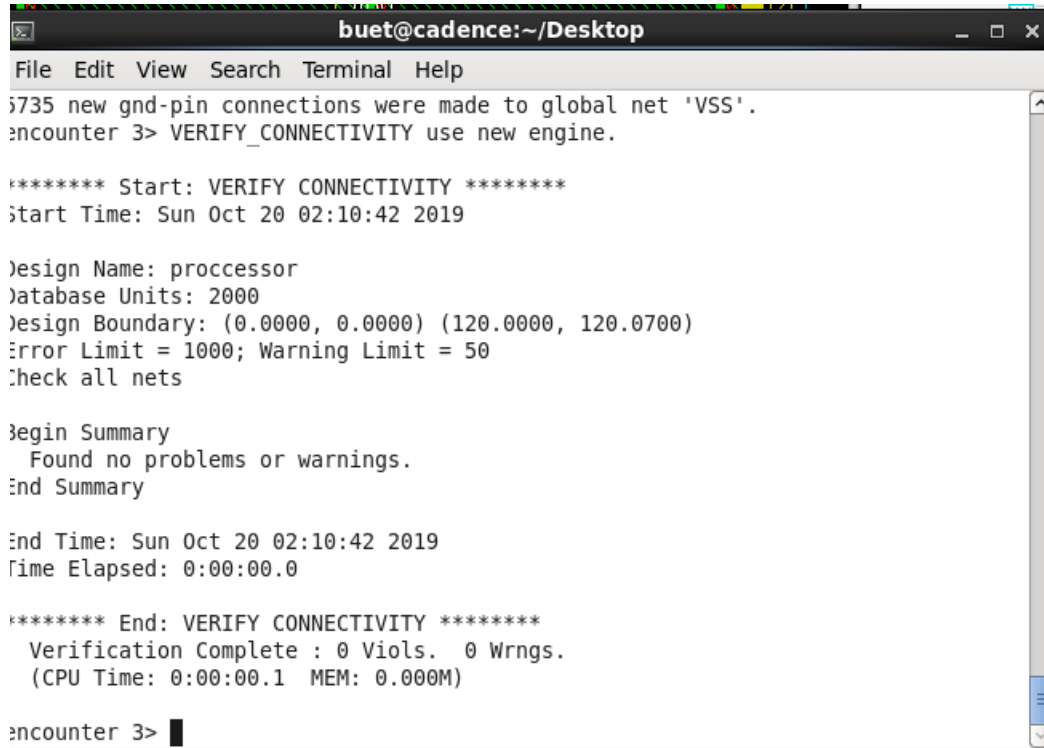


Fig: Geometry check report

We can see there are no violations in geometry check

To solve connectivity violations, we'll have to make VDD and VSS global. After using commands it looks like the following



```
bu et@cadence:~/Desktop
File Edit View Search Terminal Help
5735 new gnd-pin connections were made to global net 'VSS'.
encounter 3> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Sun Oct 20 02:10:42 2019

Design Name: processor
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (120.0000, 120.0700)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

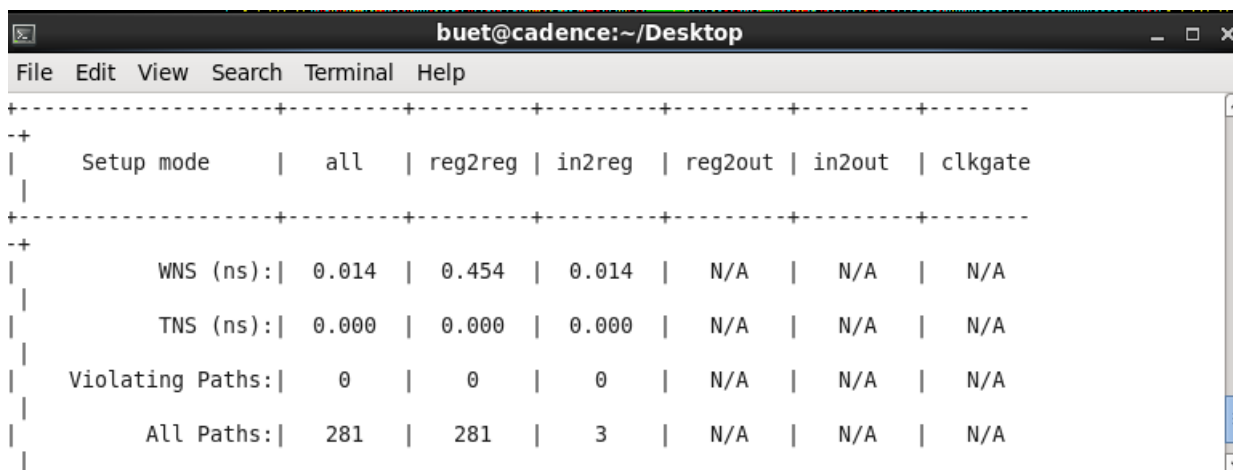
End Time: Sun Oct 20 02:10:42 2019
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols.  0 Wrngs.
(CPU Time: 0:00:00.1 MEM: 0.000M)

encounter 3> 
```

Fig: 0 connectivity violations

Then we have checked the timing violations, setup and hold. And also the DRVs. The reports are provided sequentially.



Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.014	0.454	0.014	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	281	281	3	N/A	N/A	N/A

Fig: Setup violations

```

buet@cadence:~/Desktop
File Edit View Search Terminal Help
-----
+-----+
| Setup mode | all | reg2reg | in2reg | reg2out | in2out | clkgate |
+-----+
| WNS (ns): | -0.009 | 0.165 | -0.009 | N/A | N/A | N/A |
| TNS (ns): | -0.012 | 0.000 | -0.012 | N/A | N/A | N/A |
| Violating Paths: | 2 | 0 | 2 | N/A | N/A | N/A |
| All Paths: | 281 | 281 | 3 | N/A | N/A | N/A |
+-----+
+-----+
| | Real | Total |
+-----+
| DRVs |
+-----+

```

Fig: After preCTS

buet@cadence:~/Desktop							
File Edit View Search Terminal Help							
timeDesign Summary							
-----							
Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate	
WNS (ns):	0.104	0.172	0.104	N/A	N/A	N/A	
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A	
Violating Paths:	0	0	0	N/A	N/A	N/A	
All Paths:	281	281	3	N/A	N/A	N/A	
-----							
-----							

buet@cadence:~/Desktop							
File Edit View Search Terminal Help							
timeDesign Summary							
-----							
Hold mode	all	reg2reg	in2reg	reg2out	in2out	clkgate	
WNS (ns):	-0.186	-0.186	N/A	N/A	N/A	N/A	
TNS (ns):	-32.973	-32.973	N/A	N/A	N/A	N/A	
Violating Paths:	281	281	N/A	N/A	N/A	N/A	
All Paths:	281	281	N/A	N/A	N/A	N/A	
-----							
-----							
Density: 106.881%							
Routing Overflow: 0.00% H and 0.00% V							

Fig: postCTS hold



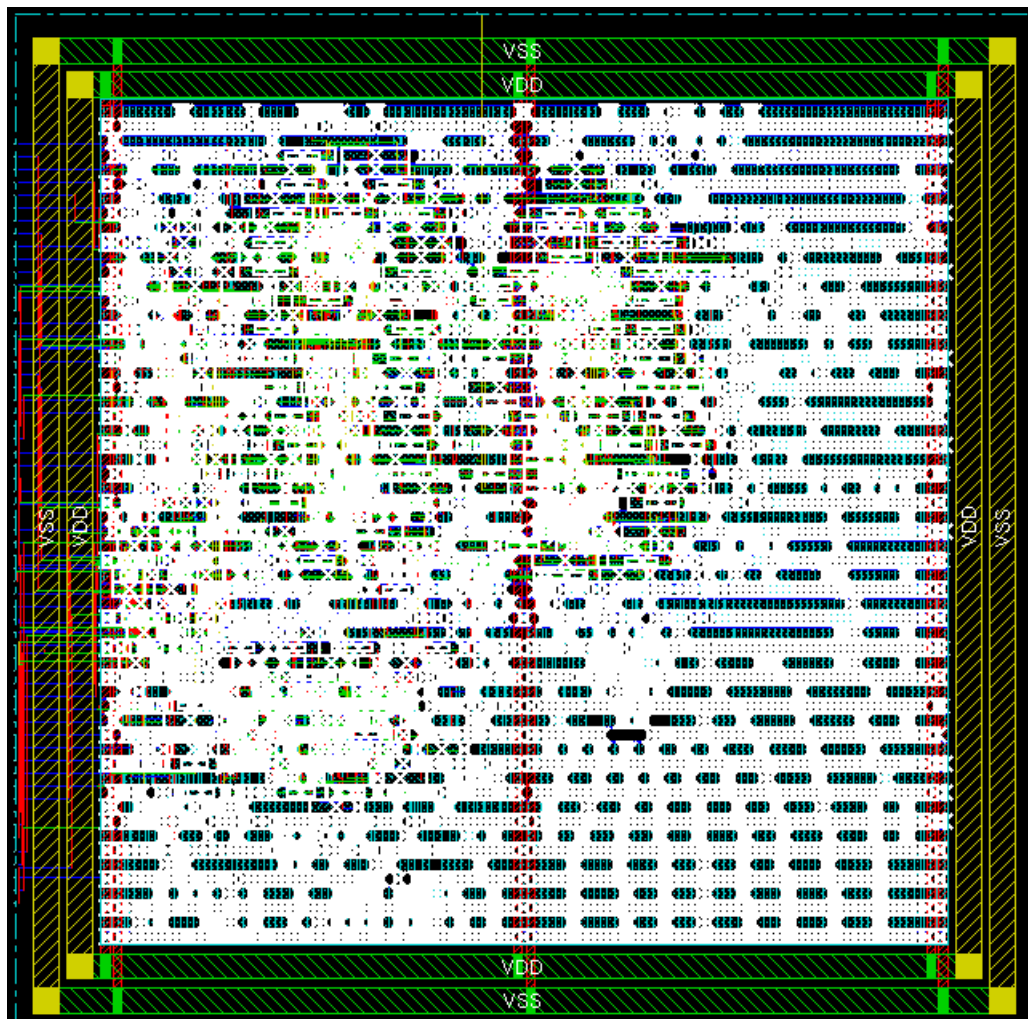


Fig: After 8<sup>th</sup> iteration, the circuit looked like this

```
# Format : Frame 1 : Split 1
Check type : max_transition
```

Pin Name	Required	Actual	Slack	View
mux2/g134/B	0.814	0.827	-0.014	func_slow
myregister1/g2520/B	0.814	0.824	-0.010	func_slow
myregister1/g2518/B	0.814	0.824	-0.010	func_slow
myregister1/g2521/A	0.814	0.822	-0.009	func_slow
myregister1/g2519/AN	0.814	0.821	-0.008	func_slow
myalu/g886/A	0.814	0.817	-0.003	func_slow
myalu/g887/AN	0.814	0.817	-0.003	func_slow
FE_PDC4_immediate_1_A	0.814	0.814	-0.001	func_slow

```
encounter 22>
```

Fig: The maximum transition violators.

**Conclusion:**

All the errors could not be removed due to time constraints and tools. DRC could not be checked as the license is not available. Setup violations could be cleaned up but the hold violation remains. Further operation can be performed for fanout, drv and hold.