# CSE341

## Theory Assignment - 2

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Section: 05

Date: ...../...../.....

# PIC

To service 48 hardware interrupts on 8086 microprocessor, we will need 7, 8259 (PIC) chips.

In the interrupt request register part the 8259A PIC has 8 pins. They are from IR0-IR7. In 8086 microprocessor, multiple PIC's can be connected through these pins. There is this master PIC, where we can connect multiple PIC's to the pins of master PIC. The concept is called cascading.

Now, we know each PIC has 8 pins, they have to be connected and perform cascading for 48 hardware interrupt, we will need: $\frac{48}{8} = 6$ additional PIC and one master PIC.

So, in total we need 7 PIC chips to service 48 hardware interrupts.

Lastly, only a total of 64 interrupts can be serviced with the help of cascading because in the master PIC there are 8 pins only. On those 8 pins, 8 PIC can be connected. The 8 PIC will give $(8 \times 8) = 64$ interrupts. The max amount of interrupt is 64. That is why only a total of 64 interrupts can be serviced with the help of cascading.

# Memory Bank

Data can be accessed from the memory in 4 different ways.

The ways are:

We might need to retrieve

1. 8 bits of data from even bank
2. 8 " " " " odd "
3. 16 " " " " even starting address
4. 16 " " " " odd " "

| $\overline{BHE}$ | $A_0$ | Type of transfer |
|---|---|---|
| 0 | 0 | 8 bit from each bank (starting from even address location) |
| 0 | 1 | 8 bit from odd bank |
| 1 | 0 | 8 bit from even bank. |
| 1 | 1 | None |

When, $A_0$ is low only then the even bank is activating.
When, $\overline{BHE}$ is high " " " odd " " ".

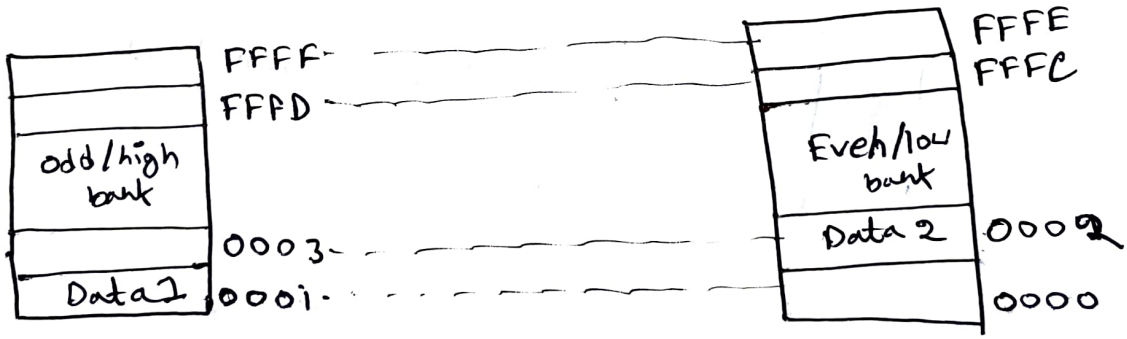
When, the starting address is from odd bank, we require 2 bus cycles. It is not possible to access a data of which starting address is from odd bank.

This is called unaligned word.

So, First bus cycle: $A_0 = 1$, $\overline{BHE} = 0$ (activating odd bank)

Second " " : $\overline{BHE} = 1$, $A_0 = 0$ (Activating even bank)

While, accessing 16-bit data with an odd starting address, it requires 2 bus-cycle instead of 1 because the memory banks (odd bank, even bank) are not aligned, that's why data couldn't be retrieve in one bus cycle. It must take 2 bus cycle.




1st bus cycle: $A_0 = 1$ (deactivating even bank)
$\overline{BHE} = 0$ (activating odd bank)

2nd bus cycle: $A_0 = 0$ (activating even bank)
$\overline{BHE} = 1$ (deactivating odd bank)

Thus, it requires 2 bus cycle, because in one bus cycle the whole data is not retriveable.

# Timing Diagram

(1)

We know,

1 bus cycle = 4 clock pulse

30 mhz, 40% duty cycle.

Now,

40% duty cycle = 1 clock pulse will remain high for 40% of time

and the " " " " low for 60% " "

Now,

30 Mhz = $30 \times 10^6$ hz clock pulses are generated in 1 second.

So, Time for 1 clock pulse: $\frac{1}{30 \times 10^6}$ s

$= \frac{1}{3} \times 10^{-7}$ s

$= \frac{100}{3} \times 10^{-9}$ s

$= \frac{100}{3}$ ns

So,

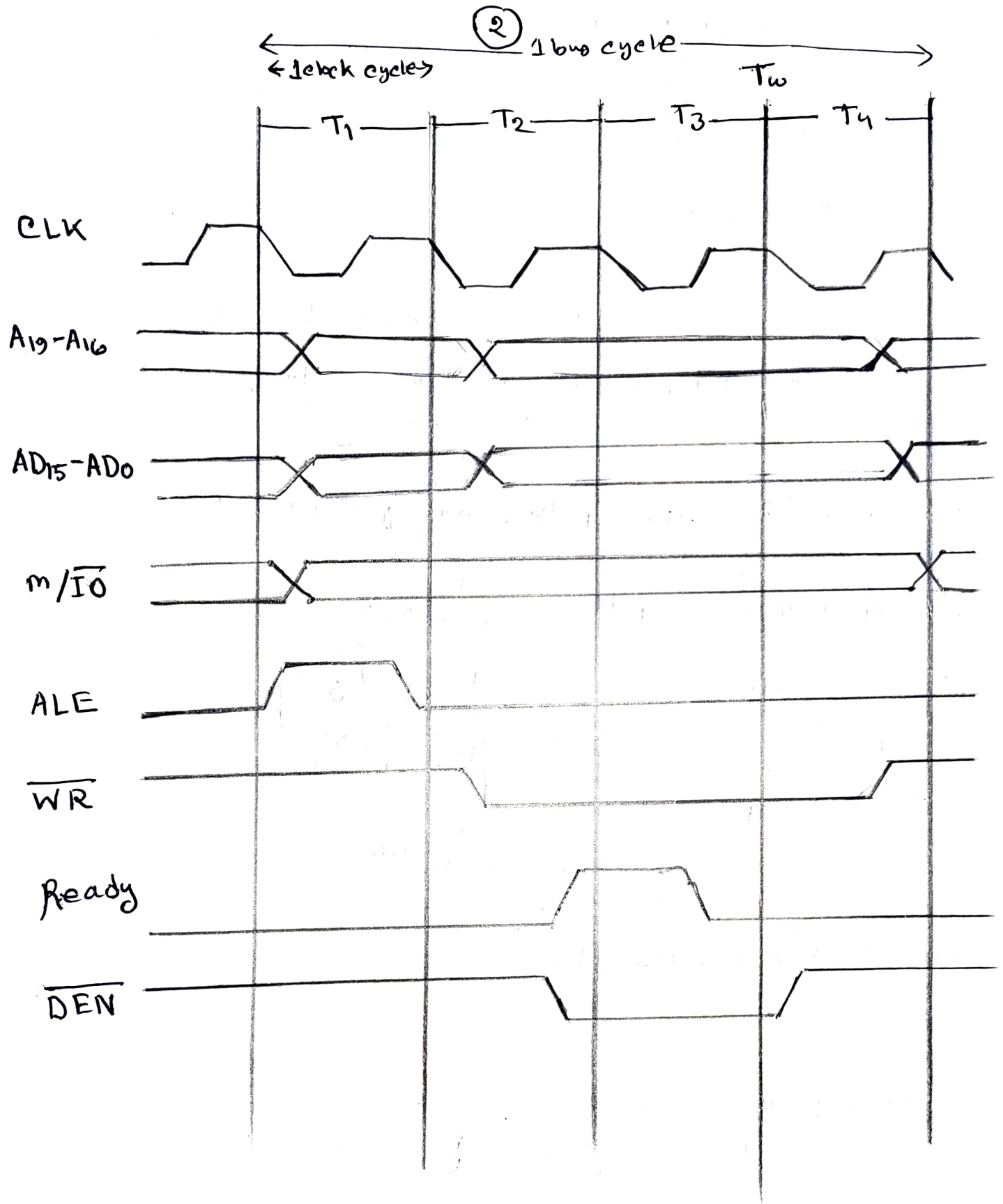
Time for 1 bus cycle = $4 \times \frac{100}{3}$ ns

$= \frac{400}{3}$ ns.

Now, each clock pulse stays low for 60% of the total time

So, the time = $\frac{60}{100} \times \frac{100}{3} = 20$ ns

So, ~~the~~ each clock pulse stays low for 20ns.


2
1 bus cycle
1 clock cycle
$T_1$
$T_2$
$T_3$
$T_w$
$T_4$
CLK
$A_{19}$-$A_{16}$
$AD_{15}$-$AD_0$
M/$\overline{IO}$
ALE
$\overline{WR}$
Ready
$\overline{DEN}$

# Interrupt

① Interrupt Type 123

$n = 123$

Memory location of IP $= 4n = 4 \times 123 = 492$

$= 001ECh$

(lower) 1st byte → 001ECh

(higher) 2nd byte → 001ECh + 1 = 001EDh

Memory location of CS $= 4n + 2 = (123 \times 4) + 2$

$= 494$

$= 001EEh$

(lower) 1st byte → 001EEh

(higher) 2nd byte → 001EEh + 1 = 001EFh

(2) The cs of the ISR of an interrupt is found to be in the memory location 2BBh

Now,

$00 2BBh = 699$

We know,

$4n + 2 = 699$

$\Rightarrow n = \frac{699-2}{4}$

$\Rightarrow n = 174.25$

$\Rightarrow n \cong 174$

The type of interrupt is 174.