Digital to Analog Converter

ADC and DAC 2

LECTURE 14

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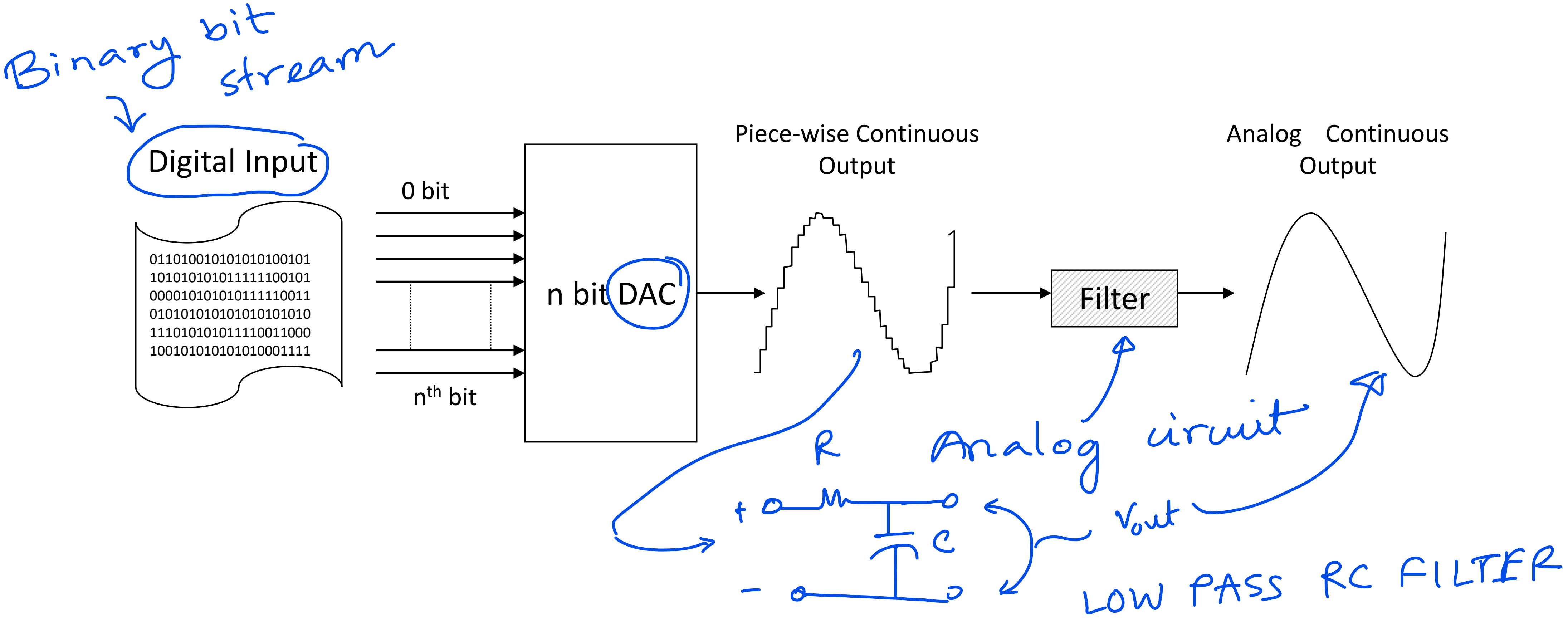
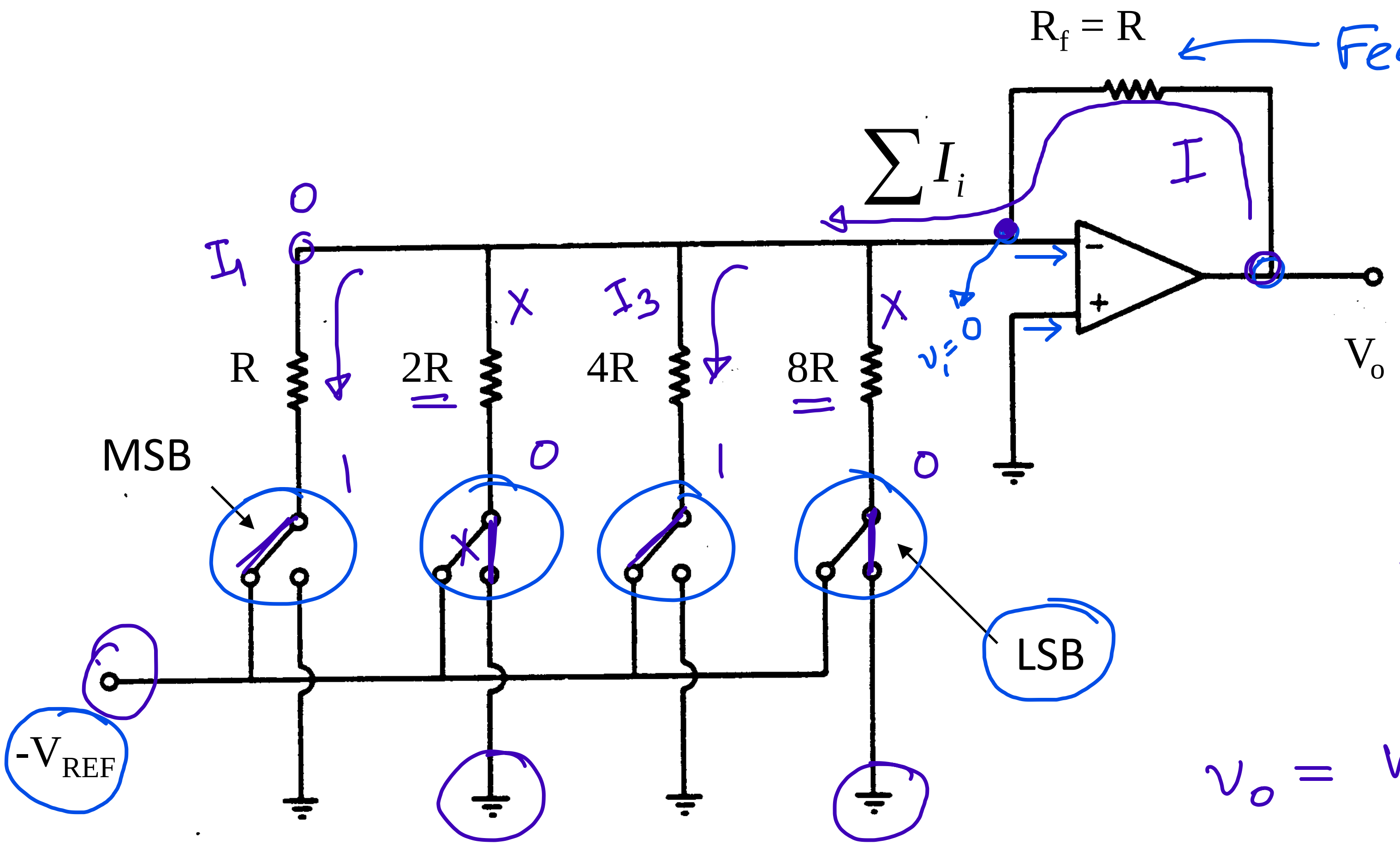
D/A Converter Operation



Binary Weighted Resistor



$$I = \frac{v_o - 0}{R} = \frac{v_o}{R}$$

$$I = I_1 + I_3$$

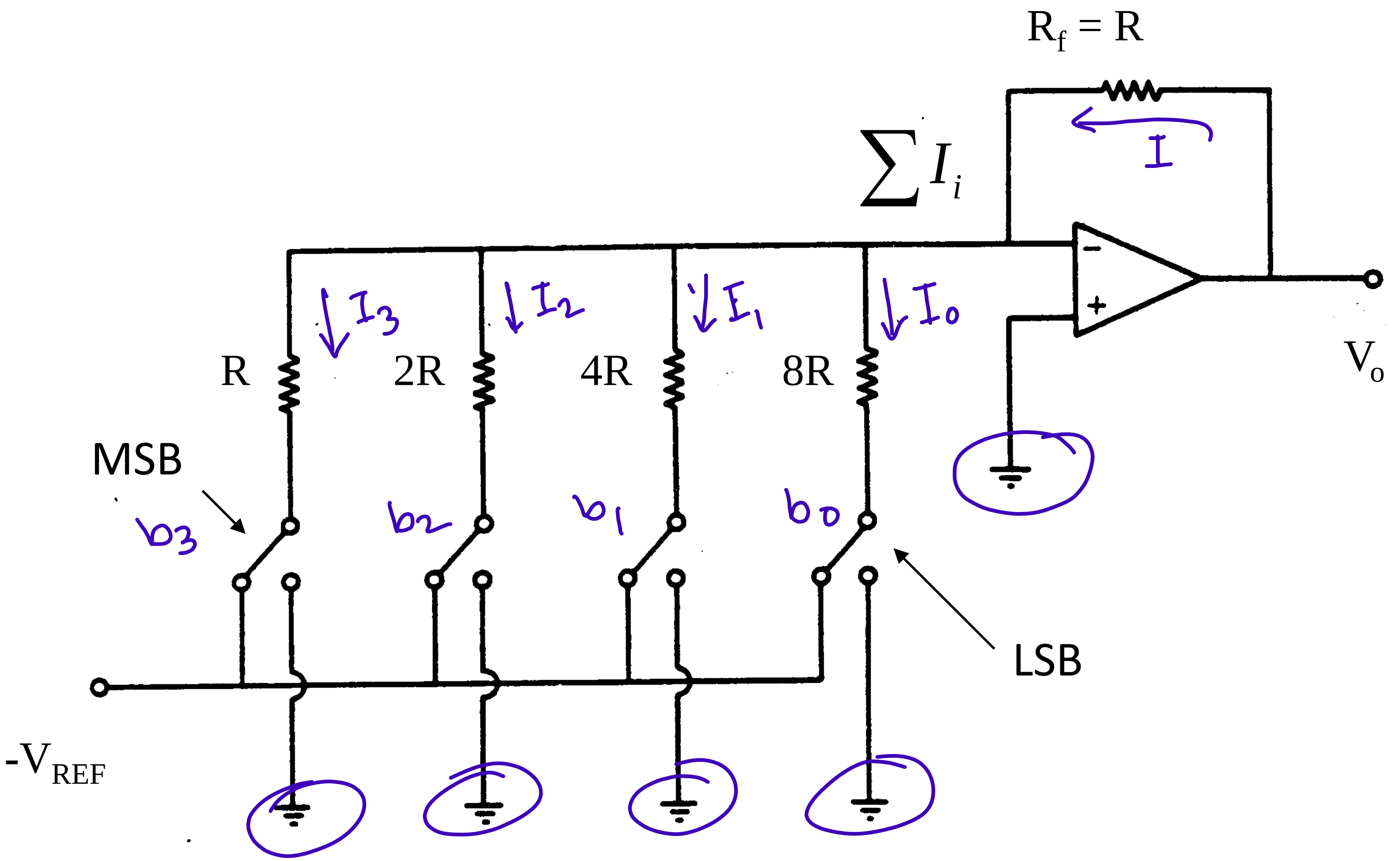
$$I_1 = \frac{0 - (-V_{REF})}{R} = \frac{V_{REF}}{R}$$

$$I_3 = \frac{V_{REF}}{4R}$$

1010

$$v_o = V_{REF} \times \left(\frac{1}{4} + 1\right)$$

Binary Weighted Resistor

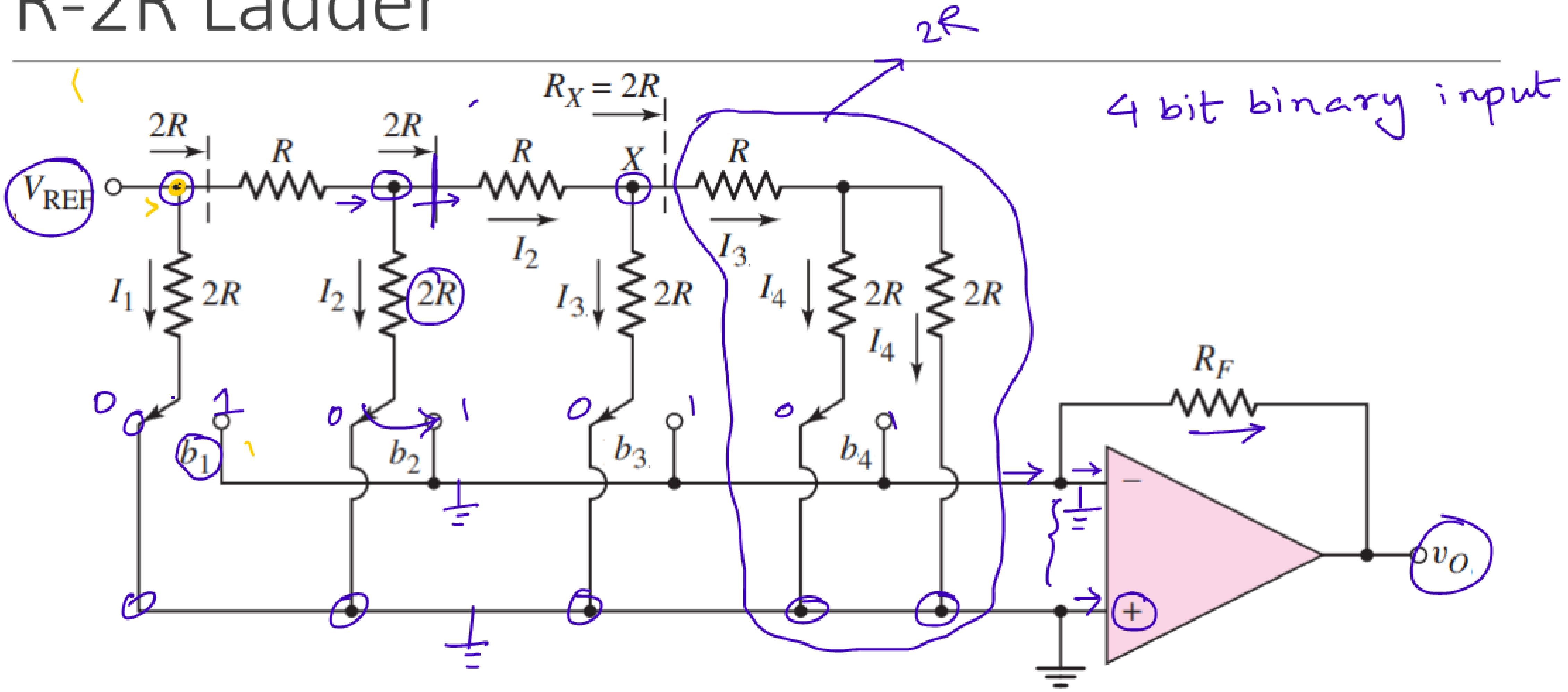


$$I_2 = b_2 \times \left(\frac{V_{REF}}{2R}\right)$$

$$I = I_1 + I_2 + I_3 + I_0$$

$$\Rightarrow V_o = V_{REF}\left(b_3 + \frac{b_2}{2} + \frac{b_1}{4} + \frac{b_0}{8}\right)$$

R-2R Ladder



2R
$R_X = 2R$
4 bit binary input
2R
R
2R
R
X
R
V_{REF}
I_2
I_3
I_1
2R
I_2
2R
I_3
2R
I_4
2R
2R
I_4
R_F
b_1
b_2
b_3
b_4
v_O

R-2R Ladder

$I_1 = \frac{V_{REF}}{2R}$

$I_1' = b_1 I_1 , \quad I_2' = b_2 I_2 , \quad I_3' = b_3 I_3 , \quad I_4' = b_3 I_4$

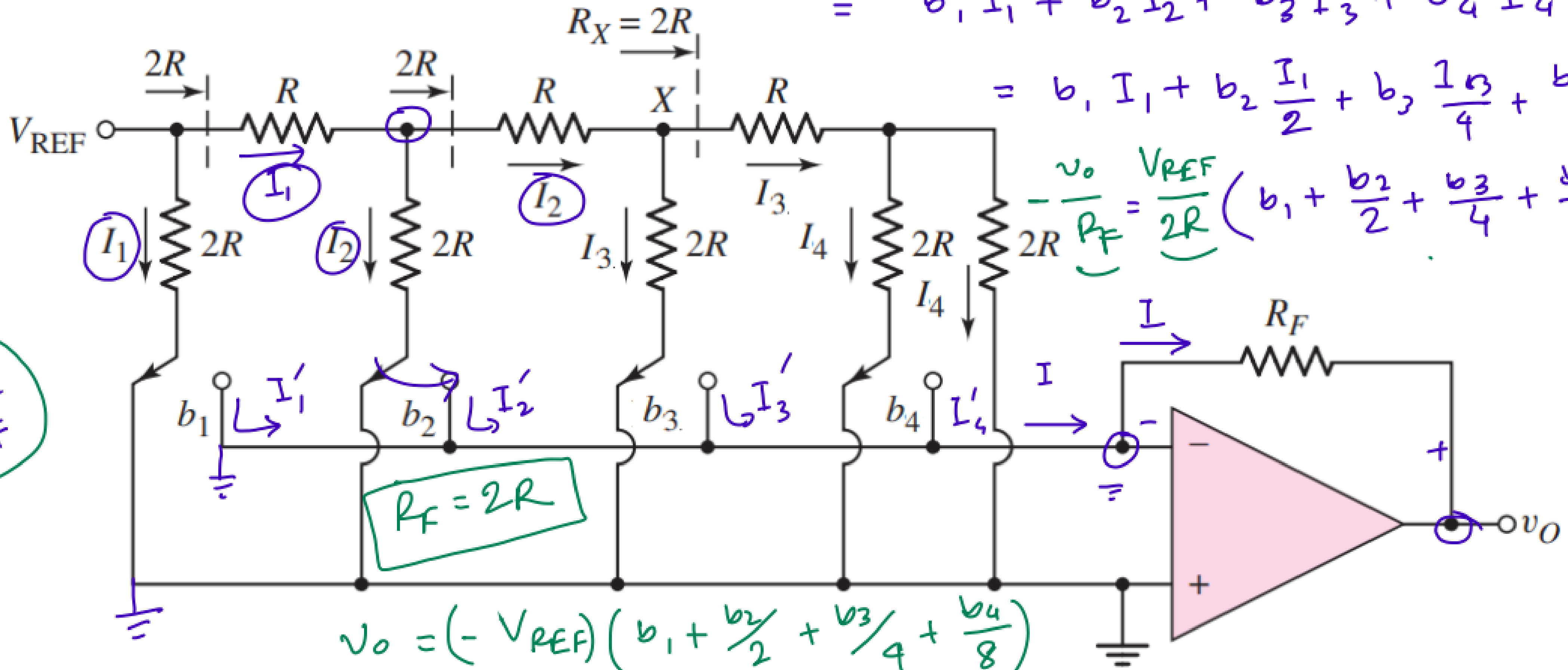
$I = I_1' + I_2' + I_3' + I_4'$

$= b_1 I_1 + b_2 I_2 + b_3 I_3 + b_4 I_4$

$= b_1 I_1 + b_2 \frac{I_1}{2} + b_3 \frac{I_3}{4} + b_4 \frac{I_4}{8}$

$-\frac{v_o}{R_F} = \frac{V_{REF}}{2R}\left(b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8}\right)$

$I = -\frac{v_o}{R_F}$

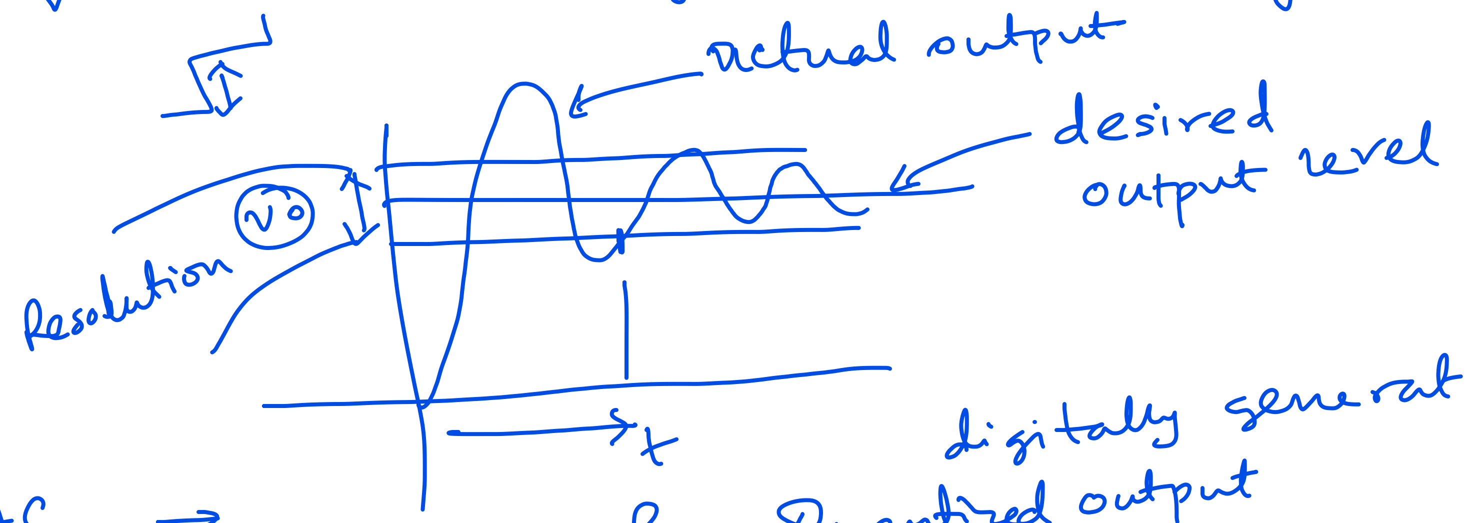


$R_F = 2R$

$v_o = (-V_{REF})\left(b_1 + b_2/2 + b_3/4 + \frac{b_4}{8}\right)$

Performance Specifications

1. Resolution → LSB 0 → 1 → change in output voltage
2. Reference Voltages →
3. Settling Time →
4. Linearity
5. Speed
6. Errors



D/AC → output = k × quantized output

digitally generated

R-2R

BWR

S A R ← Register

S R G

Shift Register Generator

Successive Approximation ADC

\# Binary Search

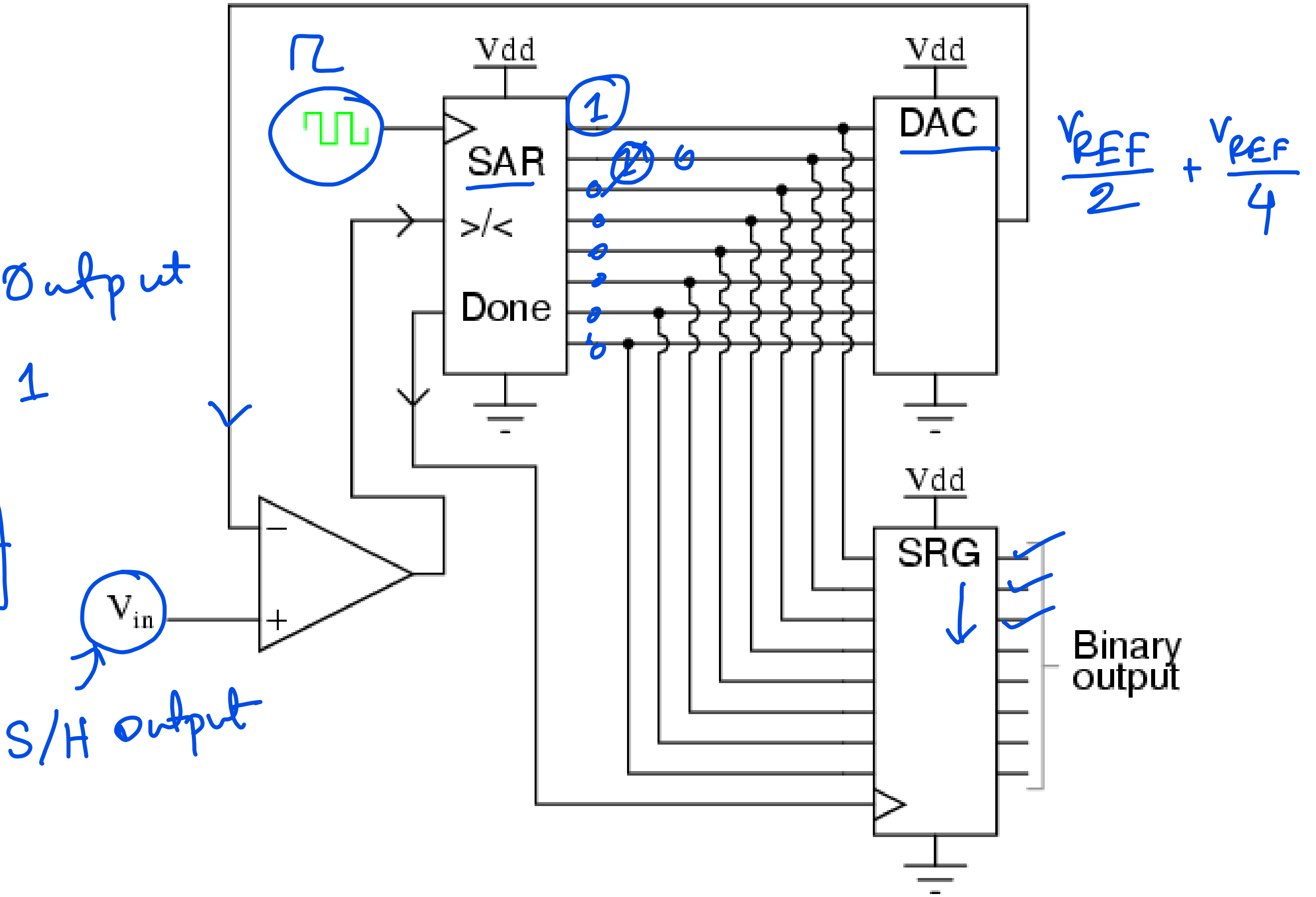
① S/H output is applied to the V_{in} at $t = 0$.

② Next pulse will reset Binary Output

③ if $V_{in} > \frac{V_{REF}}{2}$, set the MSB → 1

④ if $V_{in} > \left(\begin{cases} 0 \\ \frac{V_{REF}}{2} \end{cases} + \frac{V_{REF}}{4} \right)$ set 1 ☒ 01 ☒

$\frac{V_{REF}}{2} + \frac{V_{REF}}{4}$



Example → SAR

- 10 bit resolution or 0.0009765625V of Vref
- Vin= .6 volts
- Vref=1volts
- Find the digital value of Vin →

$\frac{1}{2} = 0.5$

↑

DAC

Bit	Voltage
9	.5
8	.25
7	.125
6	.0625
5	.03125
4	.015625
3	.0078125
2	.00390625
1	.001952125
0	.0009765625

* binary | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

$0.5 < 0.6$

* binary 1 ~~1~~ 00 0000 00 $\xrightarrow{DAC}$ $0.5 + 0.25 = 0.75$

$0.6 < 0.75$ → SAR → 1010000000

* $0.5 + 0.125$ → $0.625 > 0.6$

100 $\boxed{1}$ 00 00 0000 → $0.5 + 0.625 = 0.5625$

$0.6 > 0.5625$ → SAR → 1001100000

Example

1 001 1000 00 → DAC

* 0.5625
+ 0.03125
0.59375 < 0.6

1001 1100 00 → DAC

0.59375
+0.015625
0.609375 > 0.6

1001 1010 00 → DAC

0.59375
+0.0078125
0.6015625 > 0.6

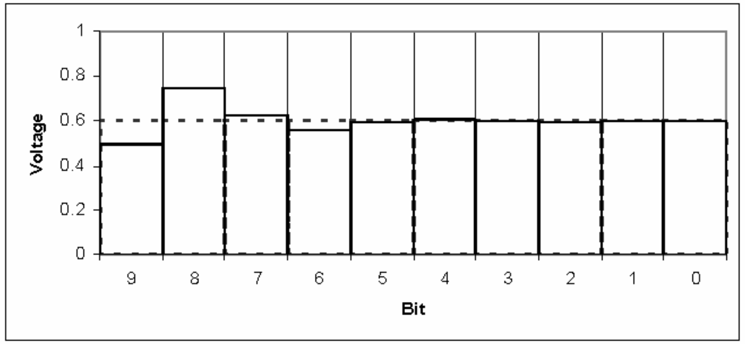
1001 100110

1
10bit

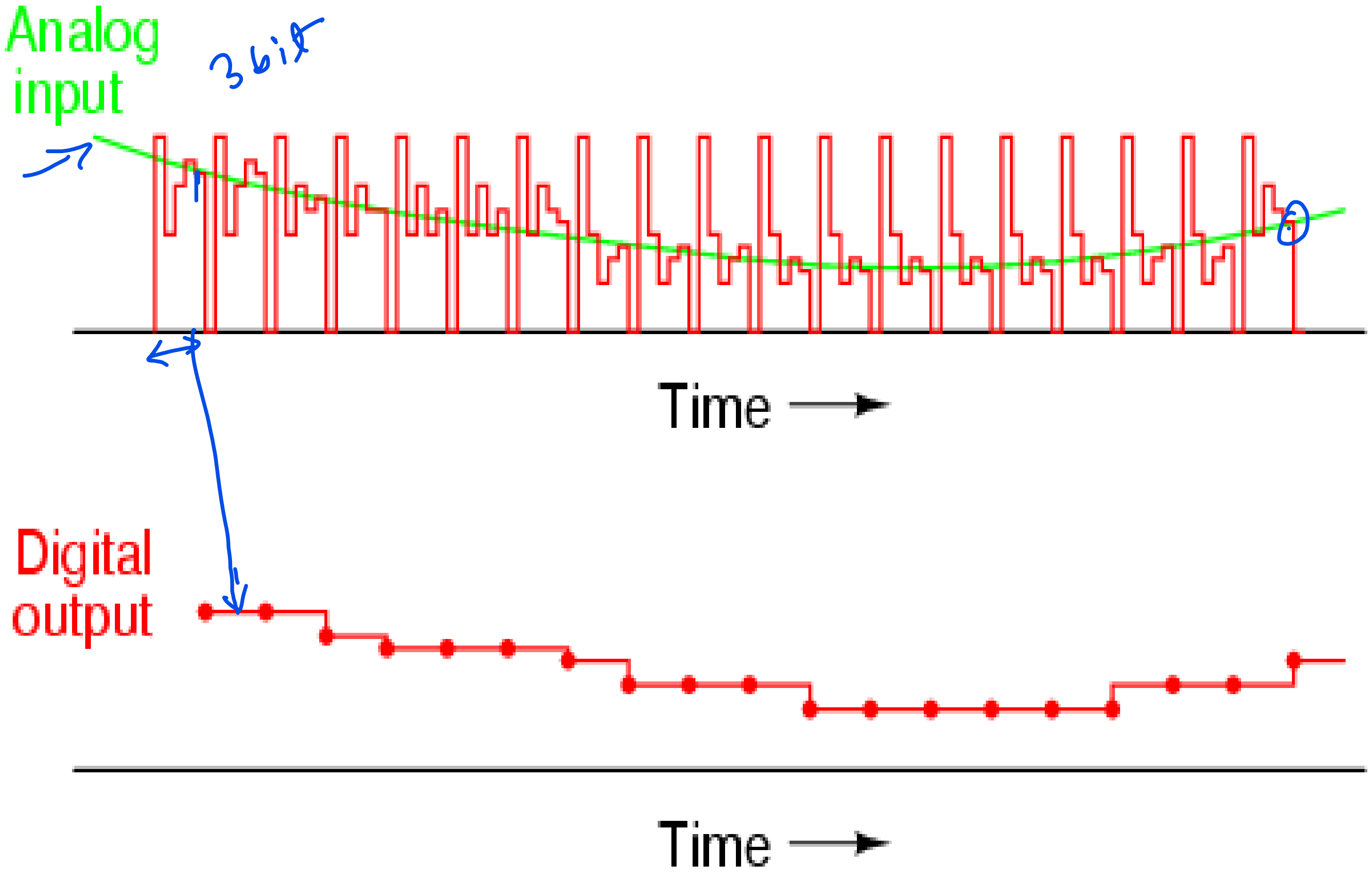
•Digital Results:

MSB	MSB-1	MSB-2	MSB-3	…					LSB
1	0	0	1	1	0	0	1	1	0

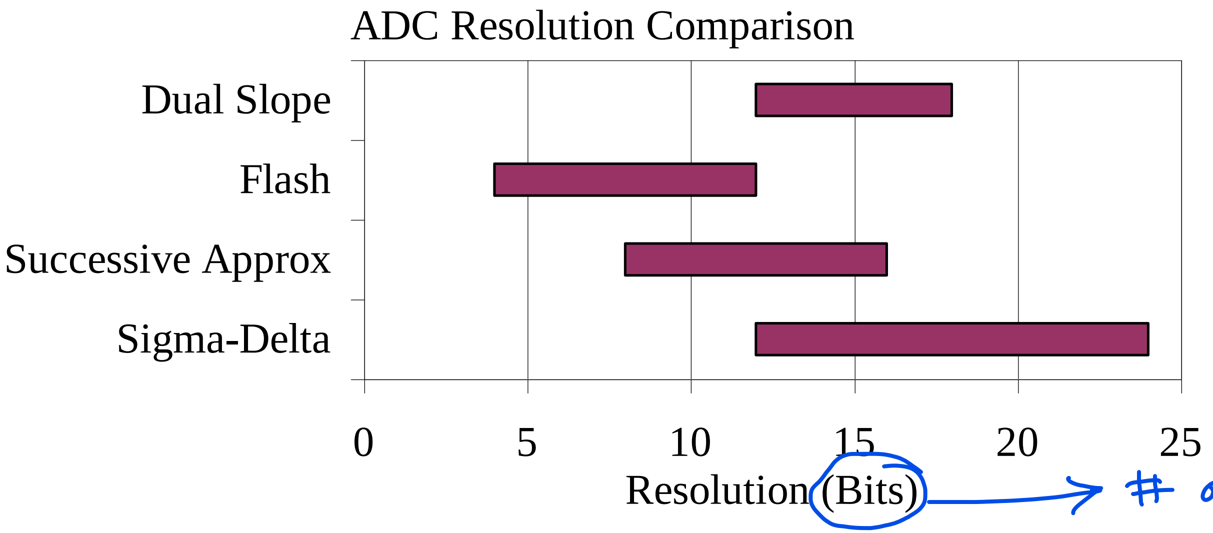
•Results: $\frac{1}{2}+\frac{1}{16}+\frac{1}{32}+\frac{1}{256}+\frac{1}{512}=.599609375\text{ V}$ → 0.6



Output



A/D Converter Types Comparison



→ # of bits could be used successfully accurately

Type	Speed (relative)	Cost (relative)
Dual Slope →	Slow	Med
Flash	Very Fast	High
Successive Appox	Medium – Fast	Low
Sigma-Delta	~~Slow~~	Low

1 clock →

→ Accurate →

→ 10 bit A/DC. 2^{10}, $2^{10}-1$

Reference

- https://ume.gatech.edu/mechatronics_course/ADC_F08.pdf
- http://ume.gatech.edu/mechatronics_course/DAC_S05.ppt
- Chapter 16 of Electronic Circuits Analysis and Design by Donald A Neamen, 4th Edition
- https://ebookbou.edu.bd/Books/Text/SST/DCSA/dcsa_2301/Unit-07.pdf