CSE350

LAB- 1

Name: Kazi Md. Al-Wakil

ID: 19301051

Section: 12

Lab: 1 (Report)

OR Gate:

V_A (v)	V_B (v)	V_{R1} (mV)	V_{R_2} (mV)	I_{R1} (A)	I_{R2} (A)	$Y = V_R$ (v)
0	0	0	0	1.19×10^{-20}	1.19×10^{-20}	1.39×10^{-15}
0	5	0	2.26	4.43×10^{-12}	4.43×10^{-5}	4.42326
5	0	2.26	0	4.43×10^{-5}	4.43×10^{-12}	4.42326
5	5	1.13	1.13	2.22×10^{-5}	2.22×10^{-5}	4.4421

AND Gate:

V_A (v)	V_B (v)	V_{R1} (mV)	V_{R2} (mV)	I_{R1} (A)	I_{R2} (A)	$V_R = Y$ (v)
0	0	1.13	1.13	2.22×10^{-5}	2.22×10^{-5}	0.558
0	5	2.26	0	4.43×10^{-5}	-1.44×10^{-11}	0.577
5	0	0	2.26	-1.44×10^{-11}	4.43×10^{-5}	0.577
5	5	0	0	-1.0007×10^{-11}	-1.00067×10^{-11}	4.99501

Inverter:

V_i	V_{R1} (v)	V_{R2} (v)	V_{RC} (v)	I_1 (mA)	I_2 (mA)	I_D (mA)	I_C (mA)	Y
0	0.65	4.35	0	0.0435	0.044	-3.79×10^{-9}	1.73×10^{-8}	5
5	4.30	5.70	4.89	0.2	5.7×10^{-2}	0.2	2.2	0.108

Report:

(1) The diode logic OR Gate's truth table

input logic low = 0V
" logic high = 5V

A	B	Output Voltage	
0	0	0	From Proteus
0	5	Output logic high (4.42326)	
5	0	Output logic high (4.42326)	
5	5	Output logic high (4.4421)	

The diode logic OR gate will only be output logical ~~high~~ low if input is logical low. Both the inputs have to be in logical low voltage.

(2) DL AND Gate:

By changing the input voltages,

$V_A = 0V$, $V_B = 0V$.

Keeping ~~Staying~~ $V_R = 5V$ we get logical high output.

From proteus:

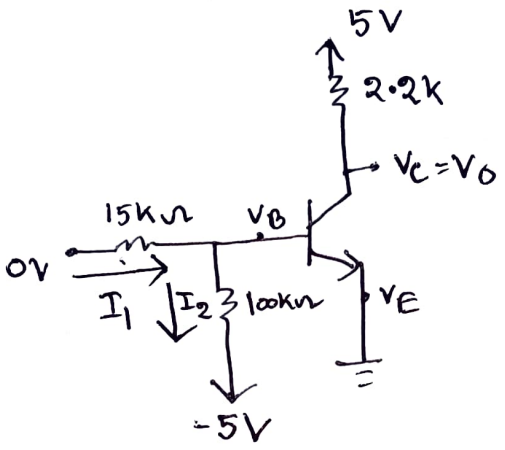
$V_o = 4.99$, Output logical high.

So, we can say that, ~~th~~ despite the changes the circuit will work as AND gate.

(3) For inverter circuit

Case (1): Transistor is in cut off mode

$V_i = 0\,V$

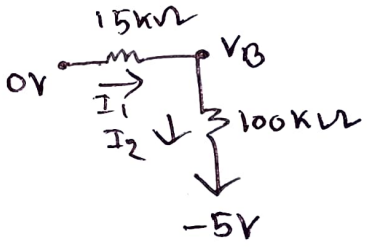


Here,

~~$I_1 + I_2 =$~~

$I_1 = I_2$

$I_B = 0$



$$V_B\left(\frac{1}{15} + \frac{1}{100}\right) - \frac{-5}{100} = 0$$

$$\Rightarrow V_B = -\frac{15}{23} = -0.6522\,V$$

Verification:

$V_{BE} < 0.7$ must satisfy the condition

$\Rightarrow V_B - V_E = -0.6522 - 0$

$= -0.6522$ which is less than 0.7

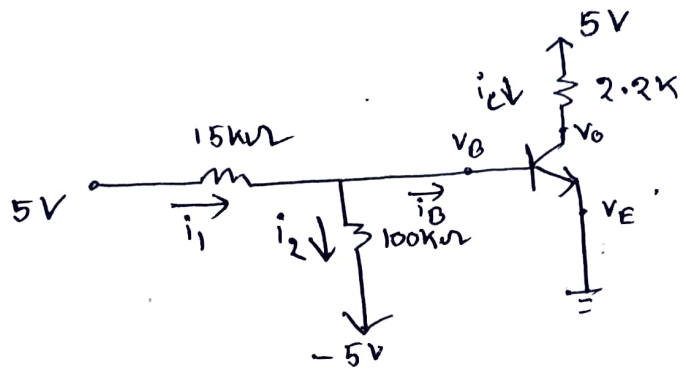
Assumption is correct.

Here, From Proteus: $I_2 = 0.044\,mA$

Now, $I_2 = \frac{V_B + 5}{100} = \frac{-0.6522 + 5}{100} = 0.043\,mA$. [verified]

So, the transistor will operate in cutoff mode.

Case: ② Transistor is in saturation mode.



We know,

$V_{BE} = 0.8$; $V_B = 0.8$, $V_{CE} = 0.2$; $V_C = 0.2V$

$$i_1 = \frac{5 - 0.8}{15} = 0.28 \text{ mA}$$

$$i_2 = \frac{0.8 + 5}{100} = 0.058 \text{ mA}$$

From proteus,

we got,

$i_1 = 0.2$ mA

$i_2 = 0.057$ mA

So, it matched with the calculated result.

Now,

$$i_B = i_1 - i_2 = 0.28 - 0.058 = 0.222 \text{ mA}$$

$$i_C = \frac{5 - 0.2}{2.2} = 2.18 \text{ mA}$$

$\beta = 30$

$$\Rightarrow \frac{I_C}{I_B} = \frac{2.18}{0.222} = 9.82$$ which is less than $\beta = 30$

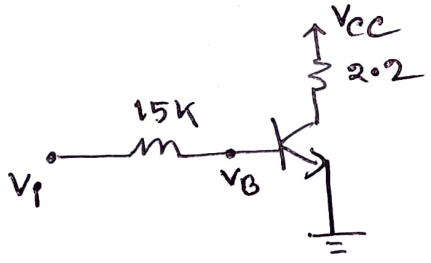
So, the transistor will operate in saturation mode.

(4) The inverter circuit function can not operate without $R_2 = 100k$ resistor.

The 100k resistor is a pull down resistor. which is connected to the base of the transistor. The resistor improves the noise margin.

To turn the BJT on we must apply $V_{BE} = 0.7$. This is the minimum voltage.

Let's remove the 100k Ω resistor



if $V_i = 0$, then, to turn the BJT on we would need

$V_{BE} = 0.7$

$V_B = 0.7$

| $V_I \leq 0.7 \rightarrow$ logical 0
| $V_I \geq 3V \rightarrow$ " 1
| ↳ Assuming

$V_{IL} = 0.7V$

$V_{IH} = V_{th} = 3V$

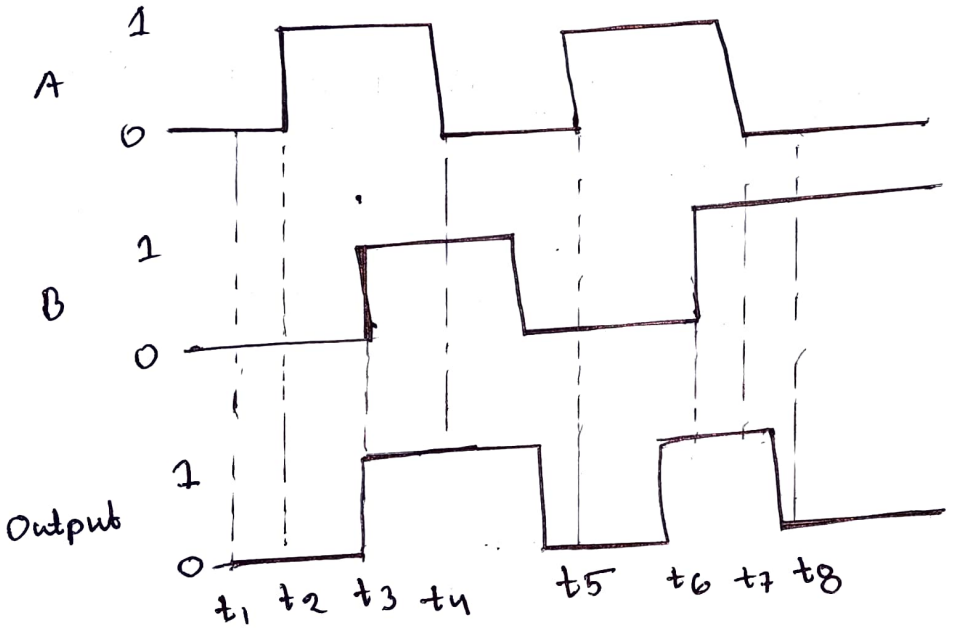
| Assuming, $V_{OL} = 0V$.

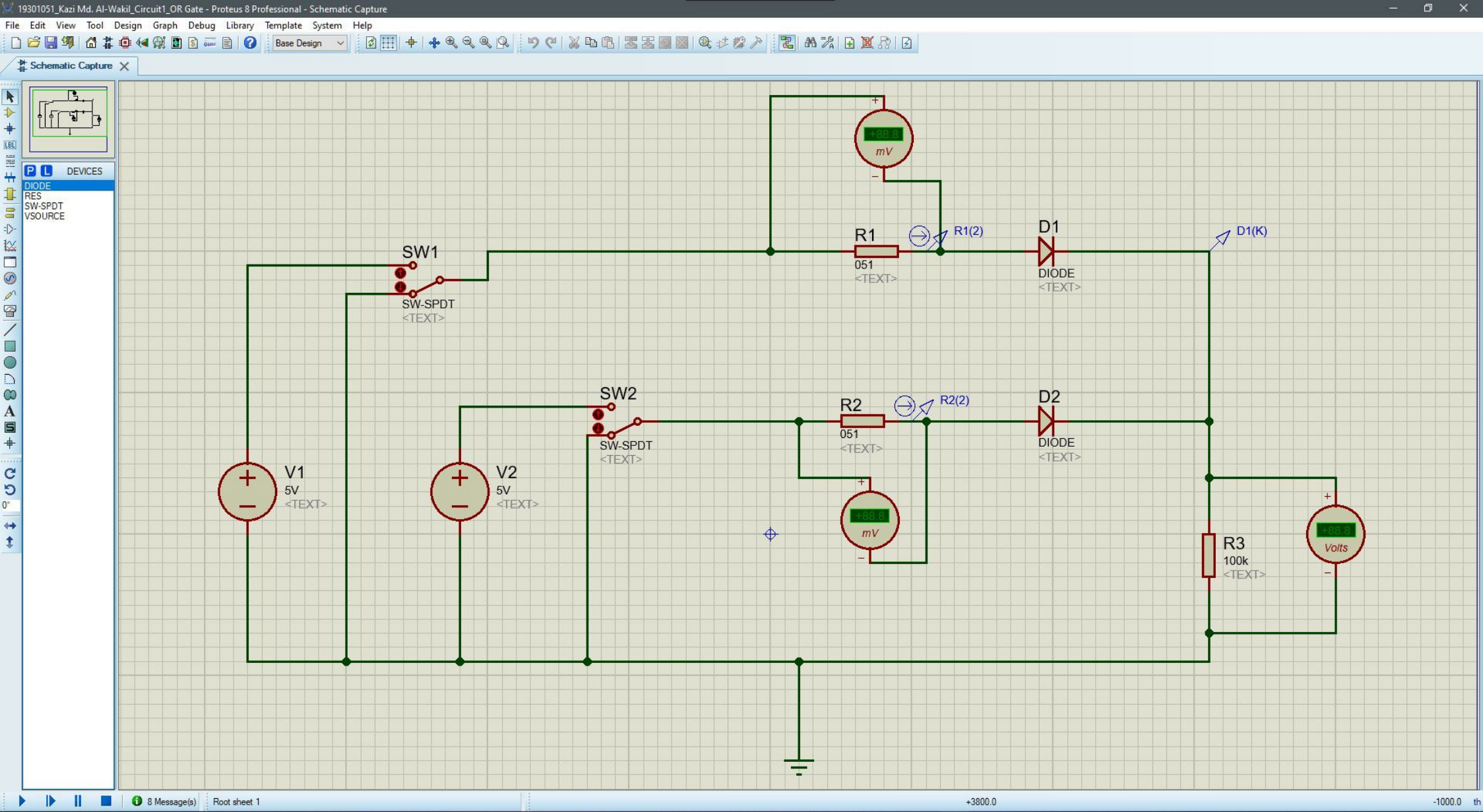
$NM_L = 0.7 - 0 = 0.7V$

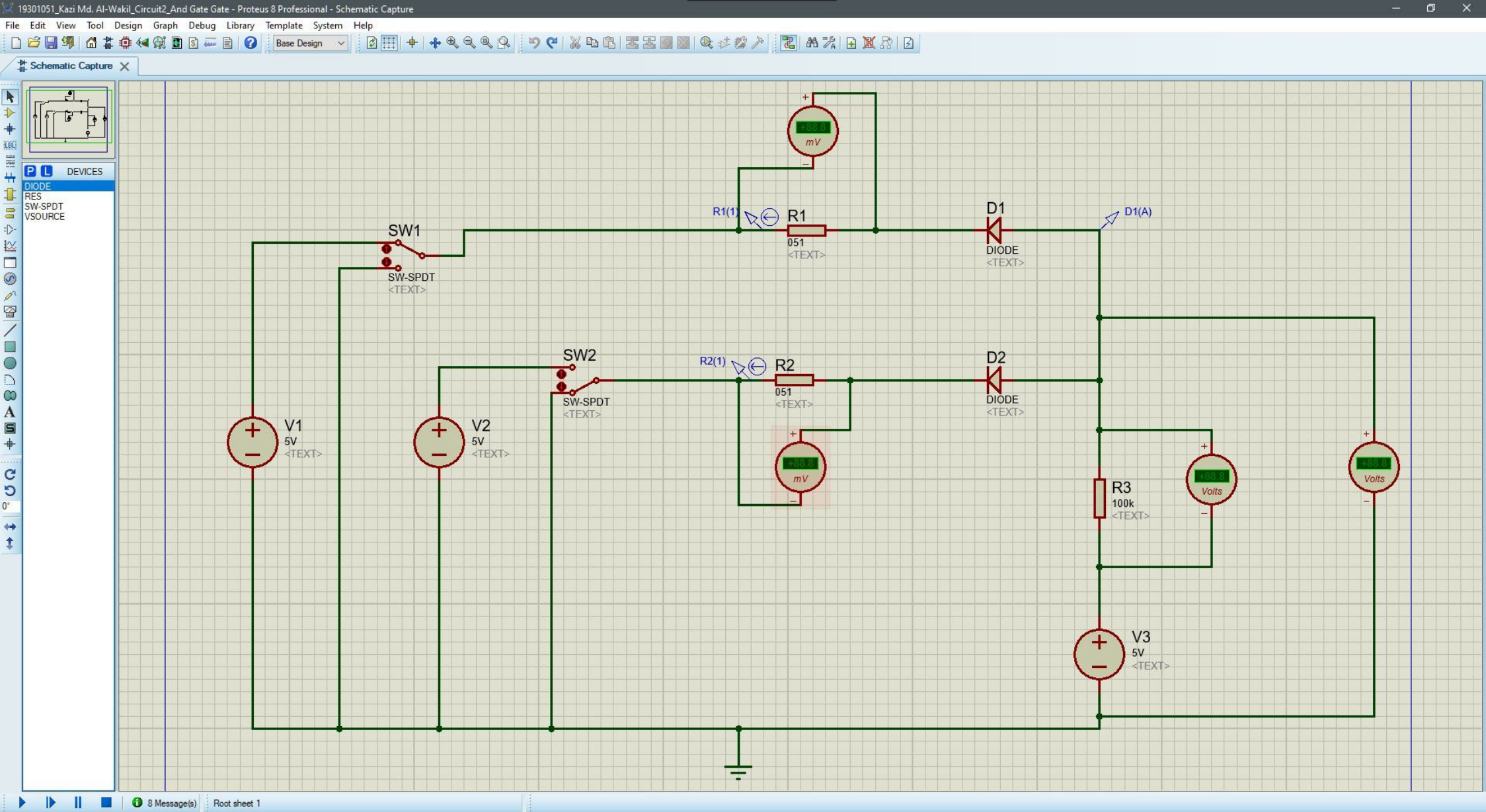
The noise is too high to work and the circuit will go in forbidden zone easily.

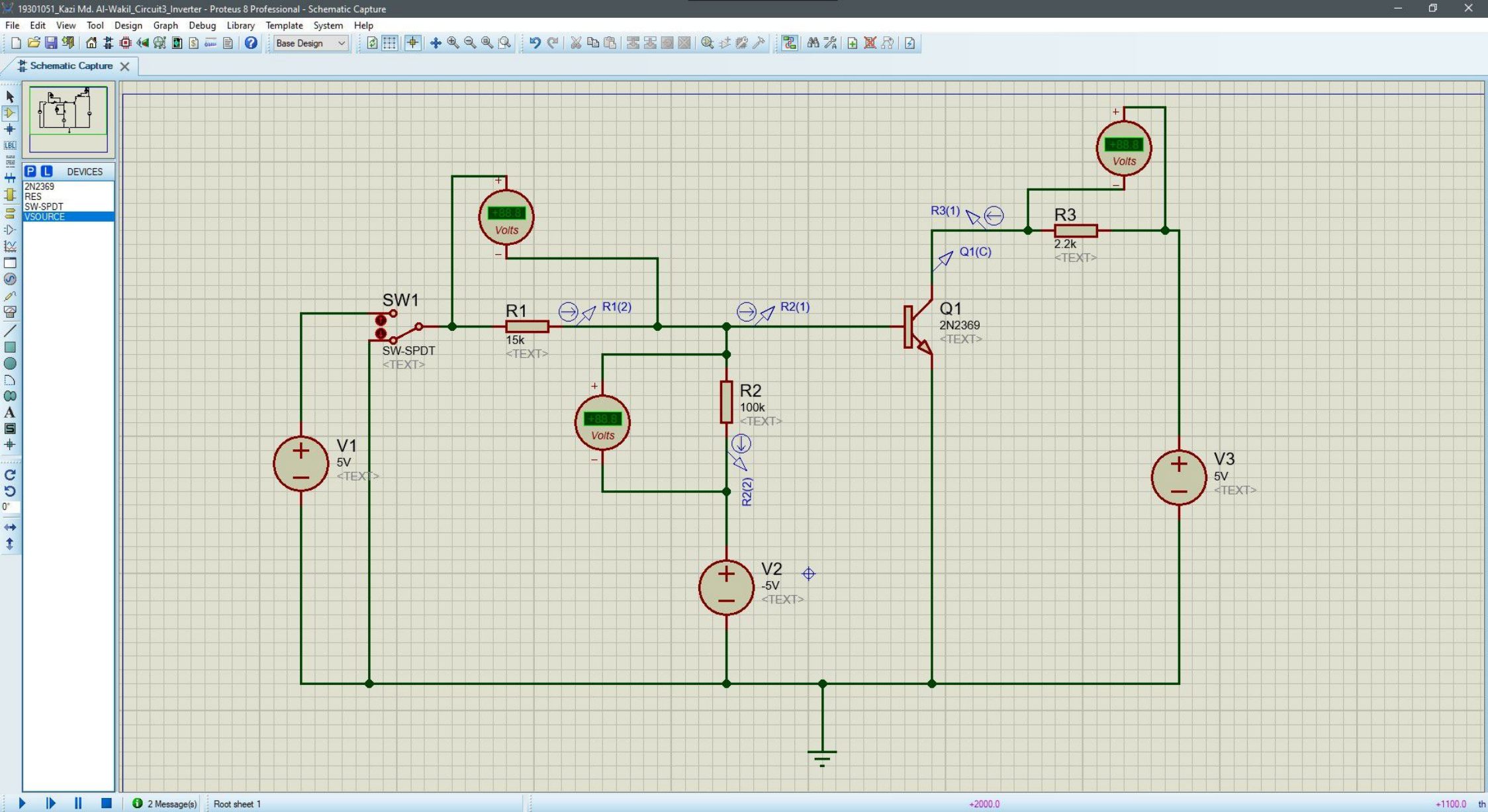
To conclude the inverter circuit can not operate without R2 = 100K resistor.

⑤ AND Gate:




19301051_Kazi Md. Al-Wakil_Circuit1_OR Gate - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
DIODE
RES
SW-SPDT
VSOURCE
SW1
SW-SPDT
<TEXT>
SW2
SW-SPDT
<TEXT>
V1
5V
<TEXT>
V2
5V
<TEXT>
R1
051
<TEXT>
R1(2)
D1
DIODE
<TEXT>
D1(K)
R2
051
<TEXT>
R2(2)
D2
DIODE
<TEXT>
R3
100k
<TEXT>
mV
mV
Volts
8 Message(s)
Root sheet 1
+3800.0
-1000.0


19301051_Kazi Md. Al-Wakil_Circuit2_And Gate Gate - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
DIODE
RES
SW-SPDT
VSOURCE
SW1
SW-SPDT
<TEXT>
SW2
SW-SPDT
<TEXT>
R1(1)
R1
051
<TEXT>
R2(1)
R2
051
<TEXT>
R3
100k
<TEXT>
D1
DIODE
<TEXT>
D2
DIODE
<TEXT>
D1(A)
V1
5V
<TEXT>
V2
5V
<TEXT>
V3
5V
<TEXT>
mV
Volts
8 Message(s)
Root sheet 1


19301051_Kazi Md. Al-Wakil_Circuit3_Inverter - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
2N2369
RES
SW-SPDT
VSOURCE
SW1
SW-SPDT
<TEXT>
R1
15k
<TEXT>
R1(2)
R2(1)
R2
100k
<TEXT>
R2(2)
V1
5V
<TEXT>
V2
-5V
<TEXT>
V3
5V
<TEXT>
Q1
2N2369
<TEXT>
Q1(C)
R3(1)
R3
2.2k
<TEXT>
+88.8
Volts
2 Message(s)
Root sheet 1
+2000.0
+1100.0