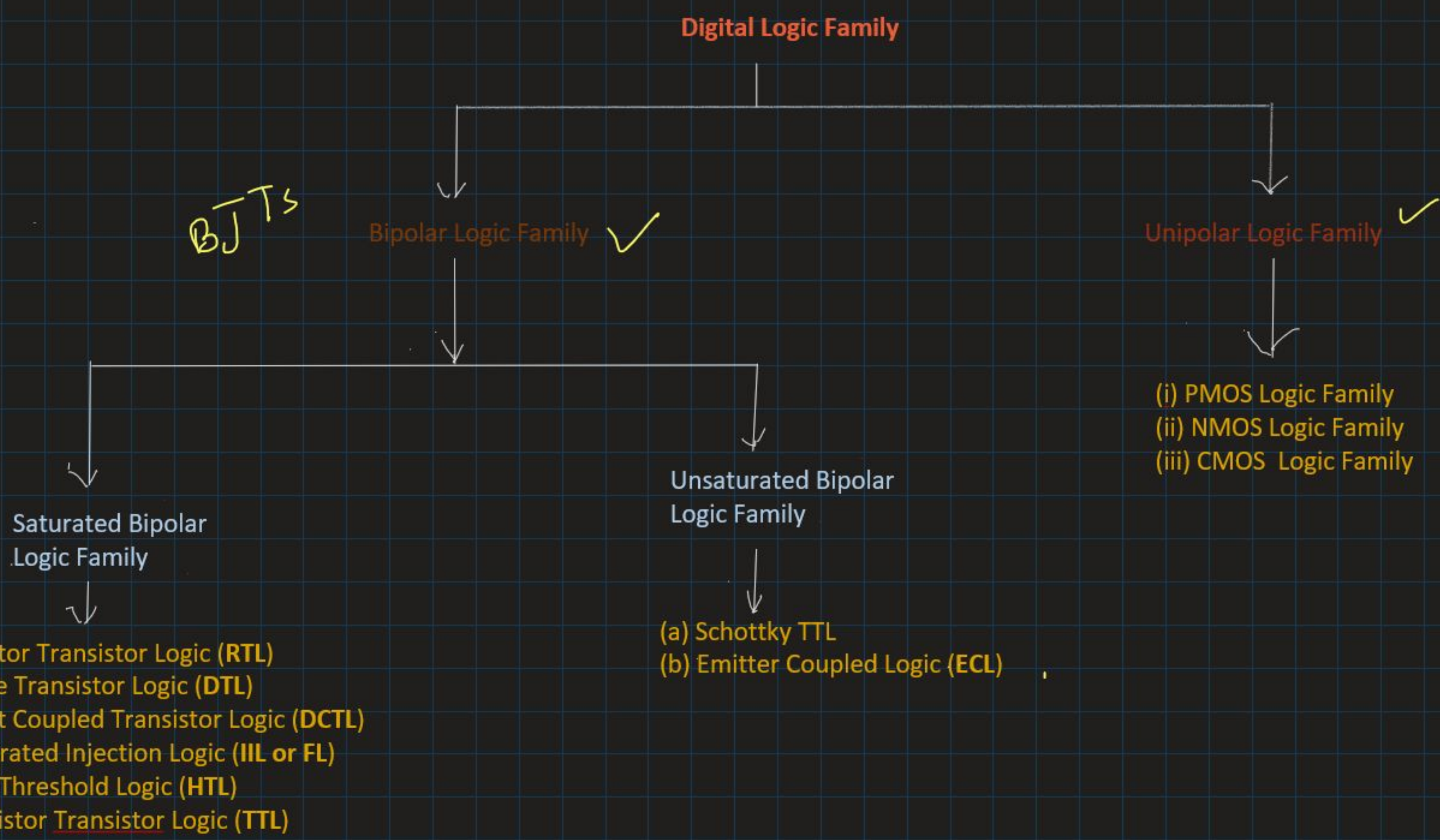


Lecture 3 part 2.png

Lecture 3 part 3.png

Lecture 3 part 4.png

Lecture 3 part 5.png



Operating Mode of BJT

- (b) Active region
- (c) Cutoff region
- (d) Reverse Active region

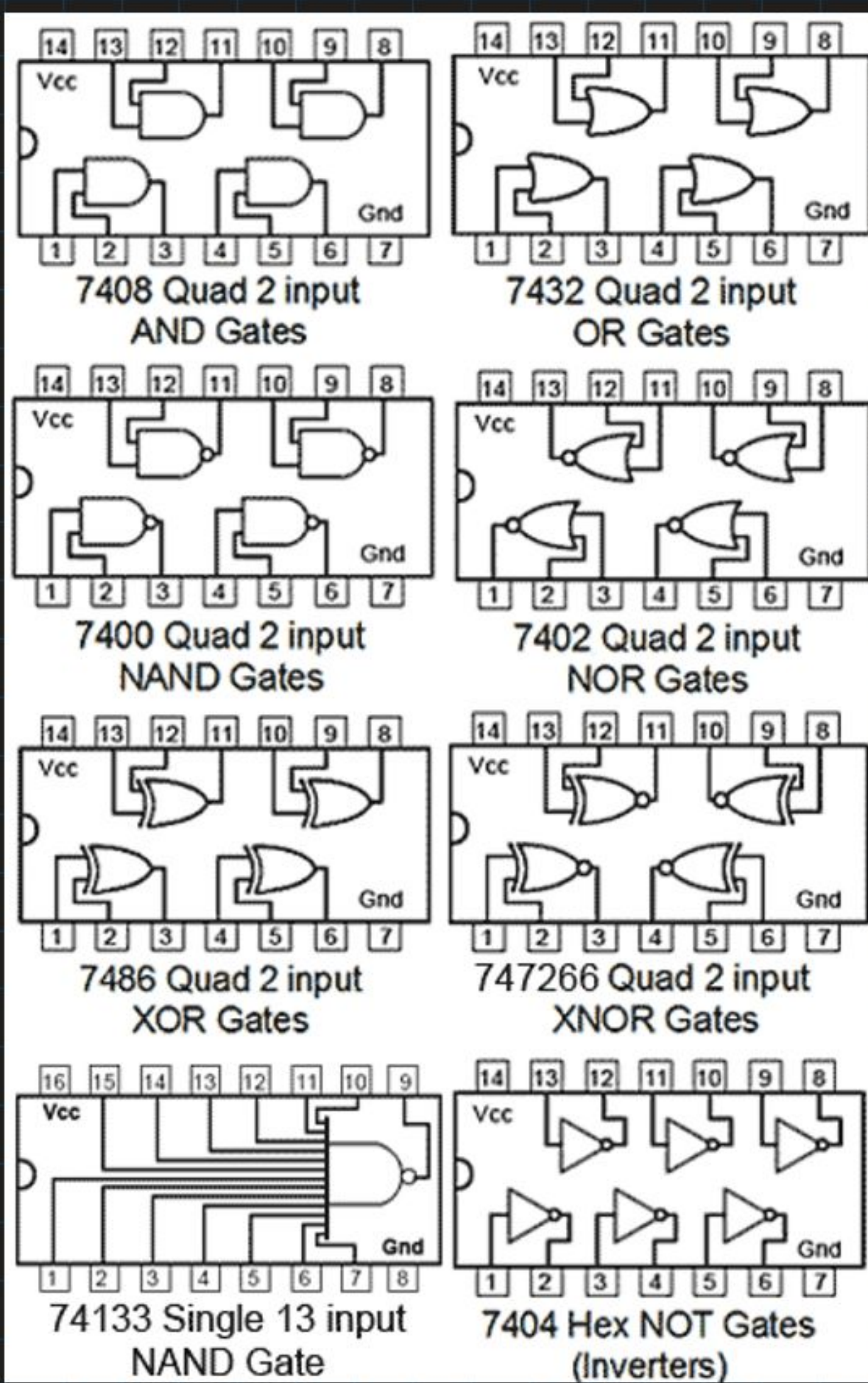
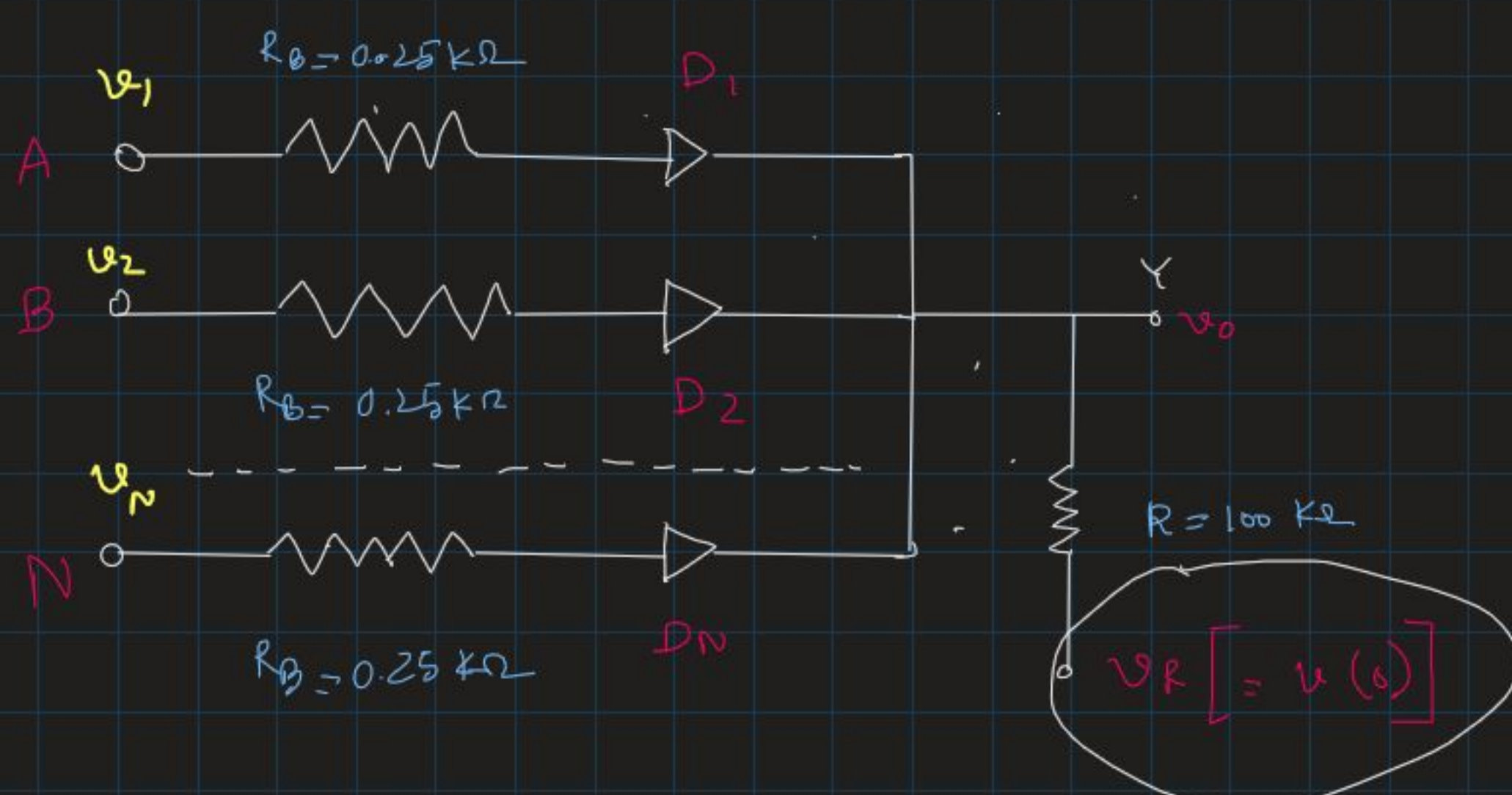


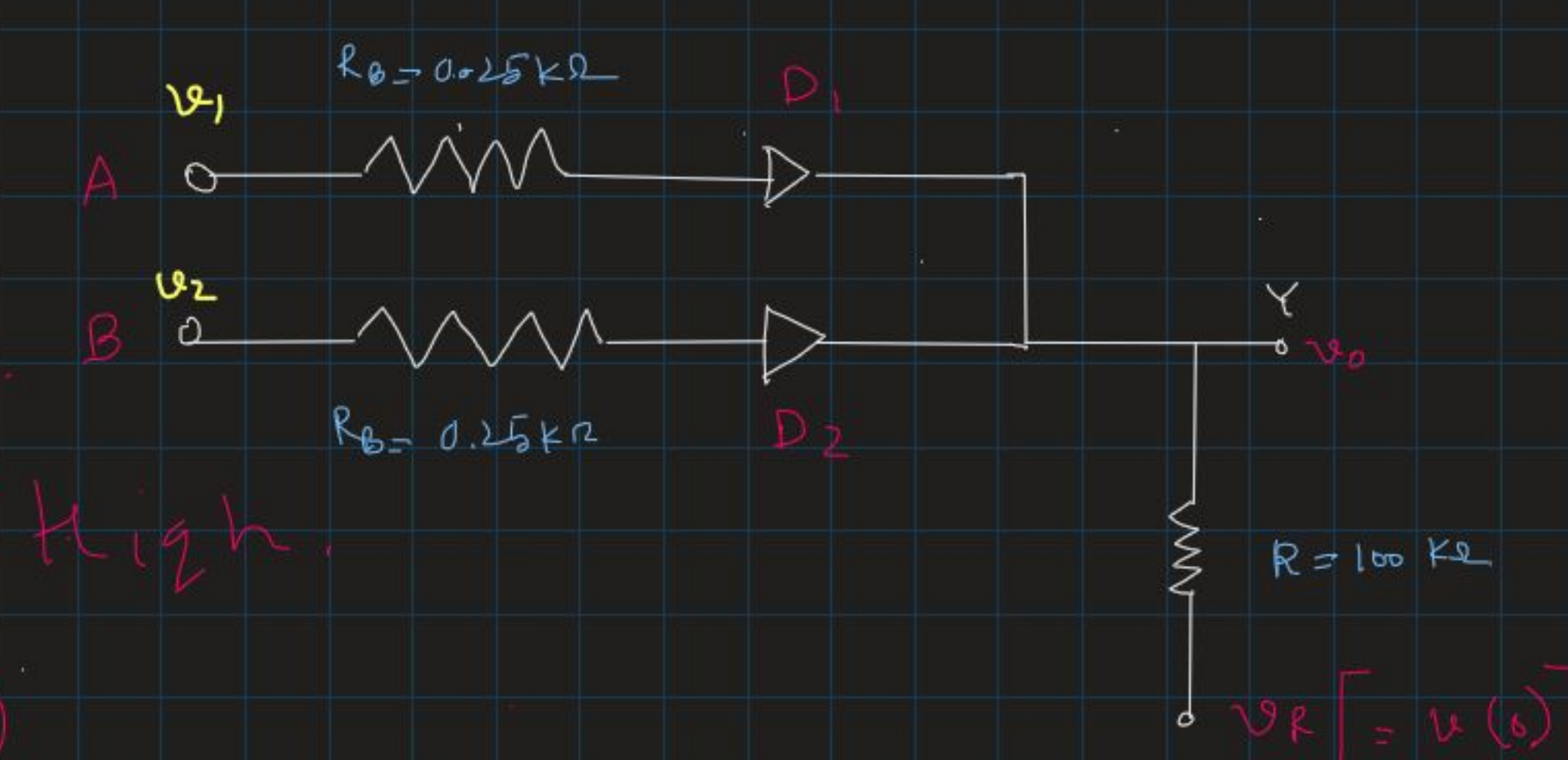
Figure : 74XX series ICs

Diode Logic OR Gate:

- ✓ **Problem:** If $V(0) = 0$ volt and $V(1) = 5$ volt and for a Fan In $N=2$
- (a) Find out the output voltage levels.
(b) Find out the maximum power dissipation.



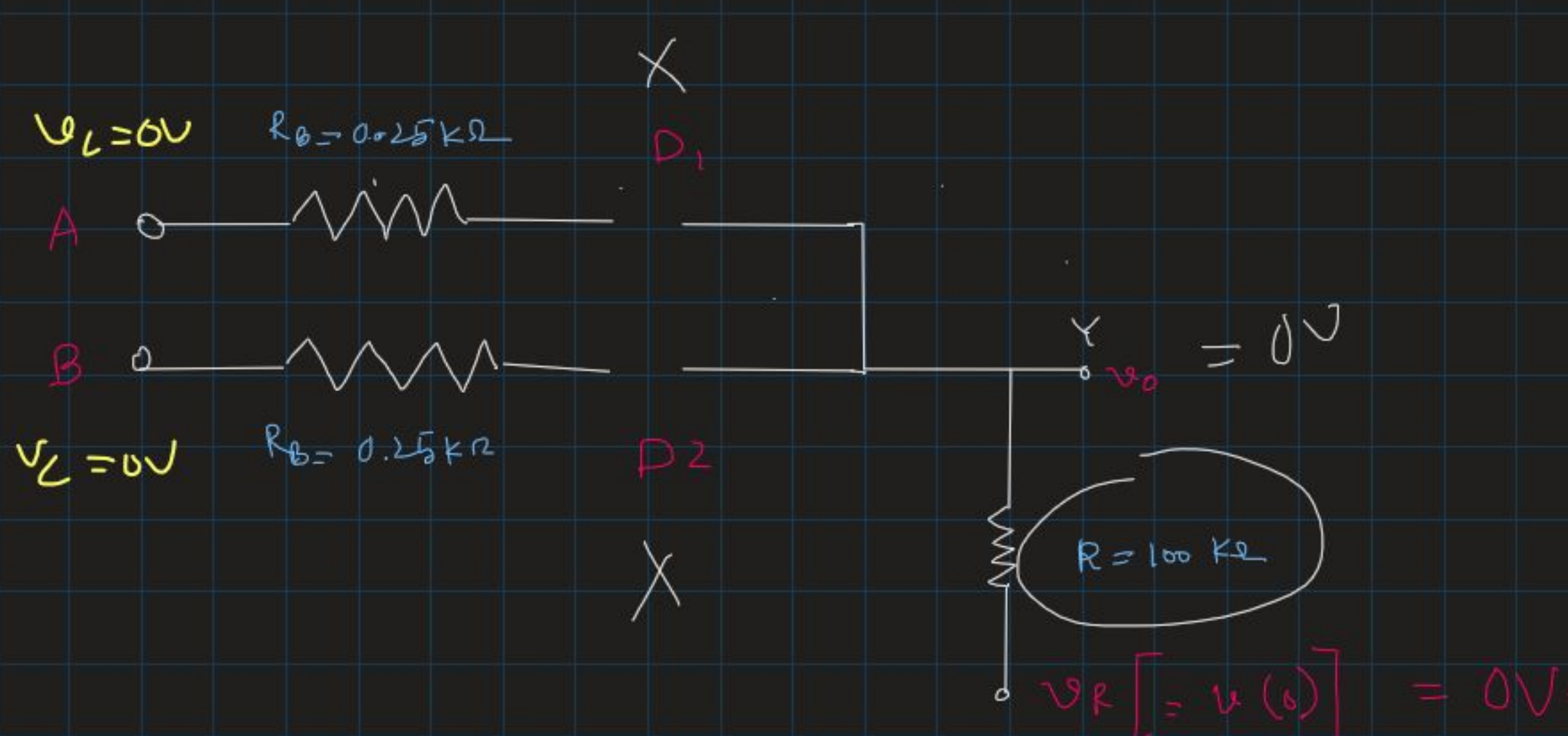
A	B	D1	D2	V0
0V	0V	X	X	0V
5V	0V	✓	X	4.2893V
0V	5V	X	✓	4.2893V
5V	5V	✓	✓	4.2946V



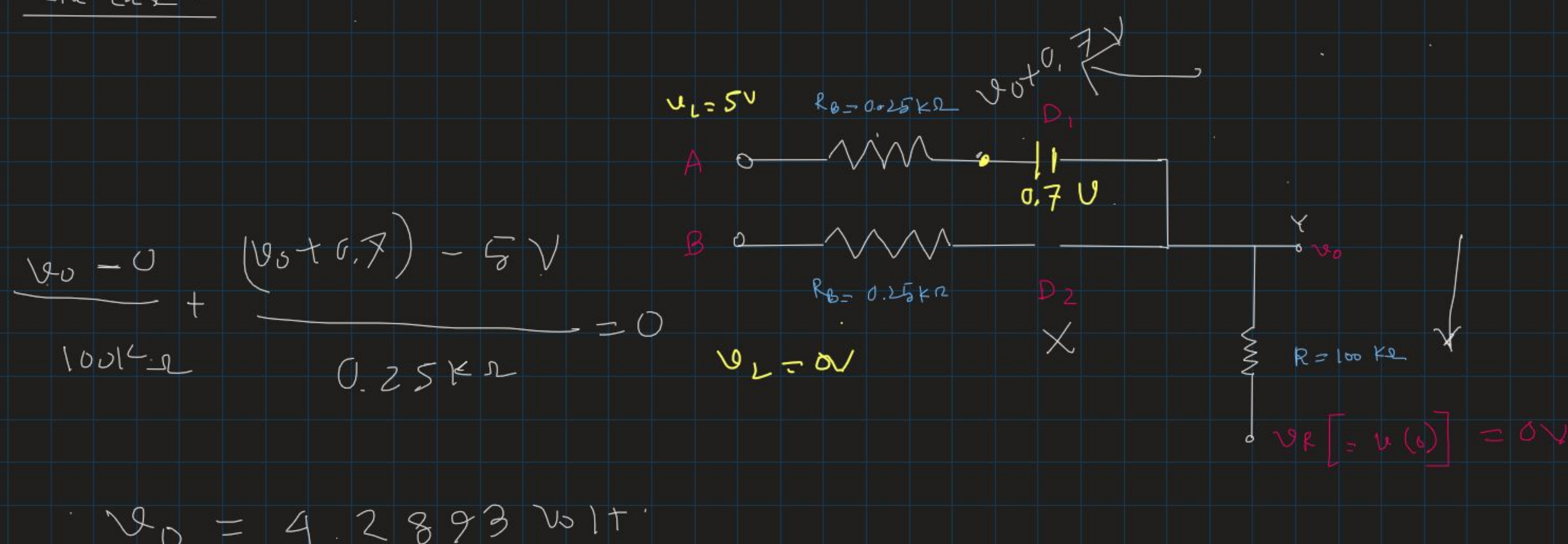
logic low $\rightarrow 0V$

logic high $\rightarrow 4.2893V$

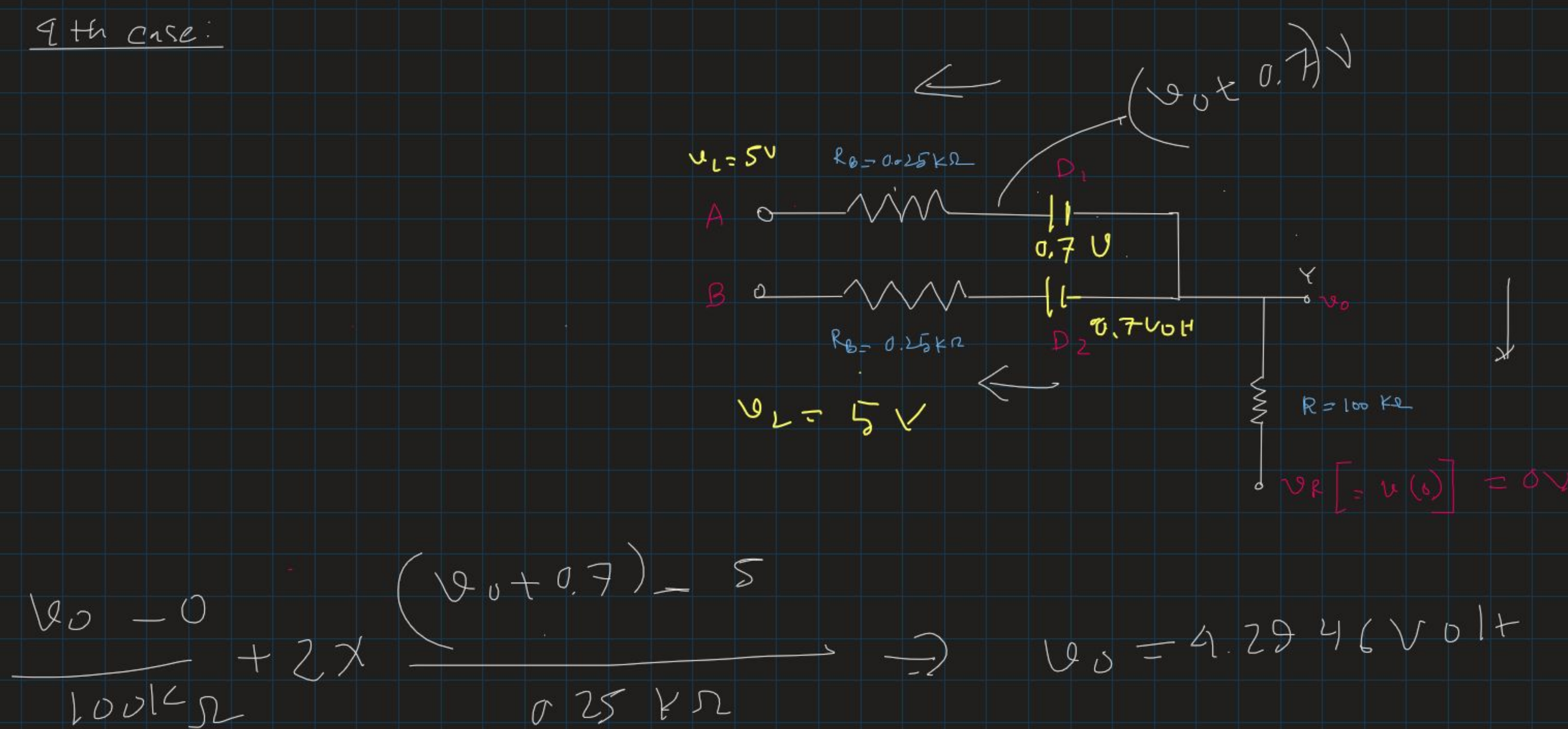
1st case:



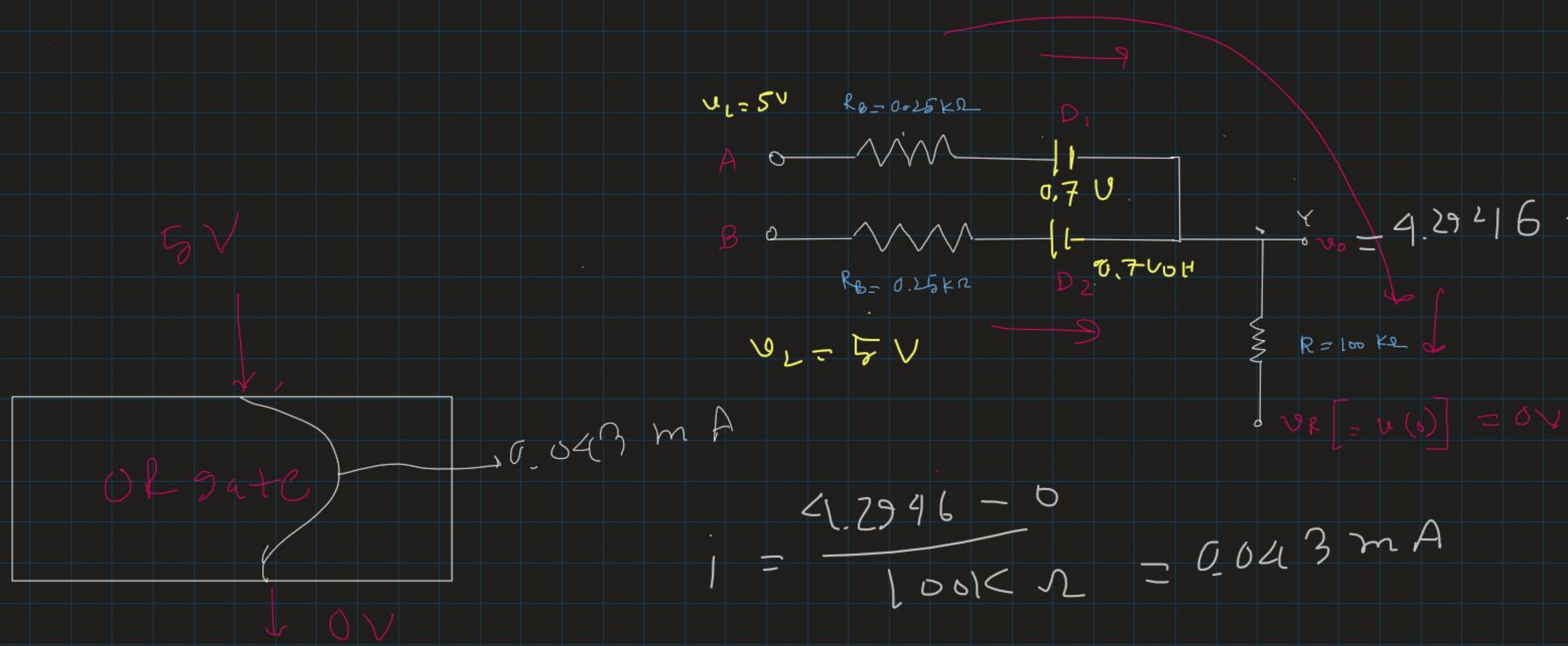
2nd case:



3rd case:



maximum power dissipation:

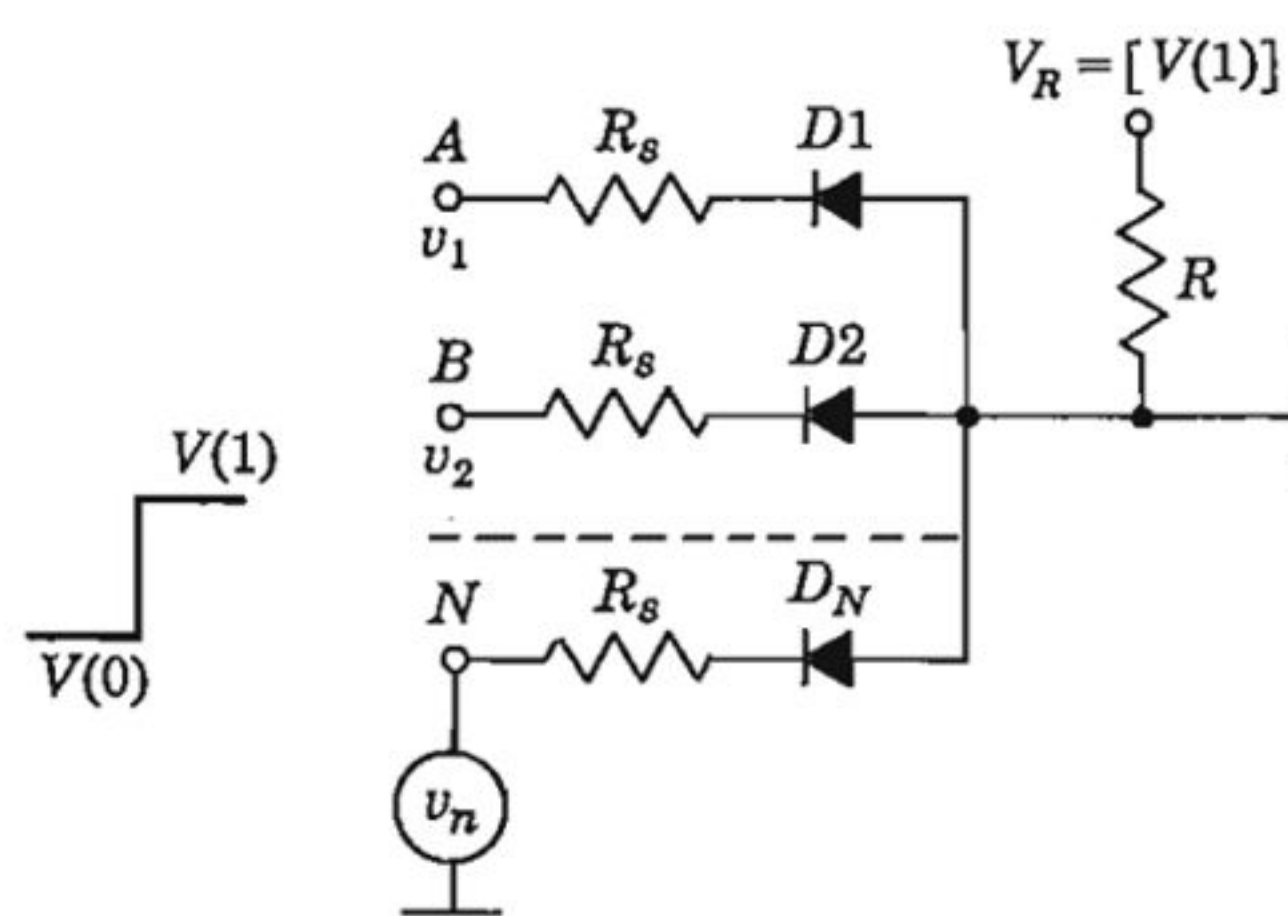


$$P = 1V \times I$$

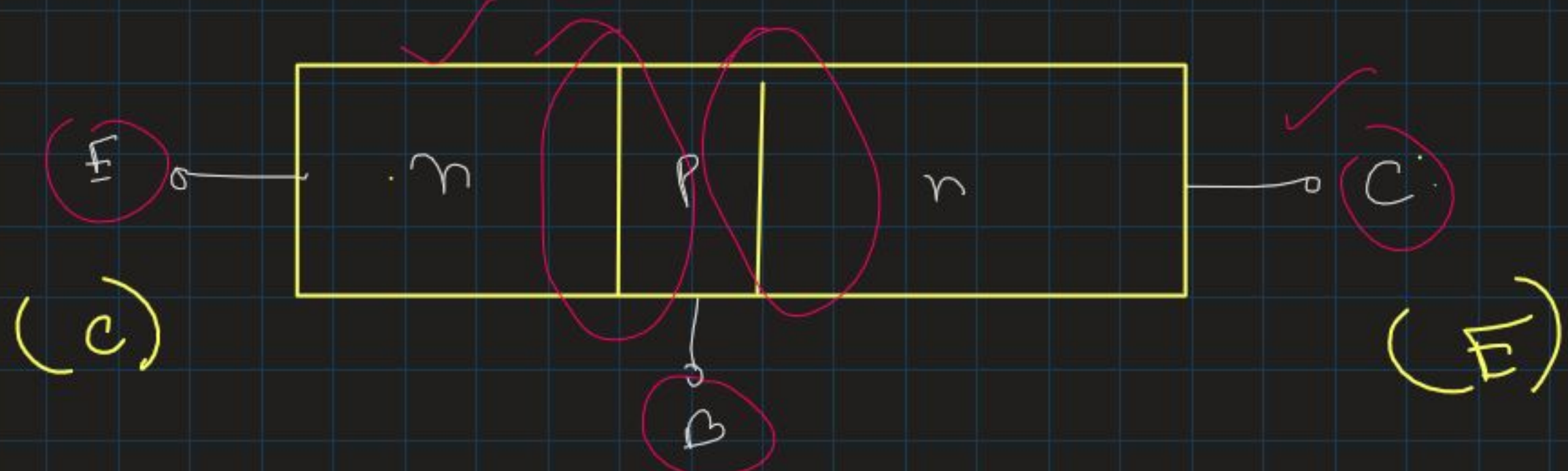
$$= (5 - 0)V \times 0.043mA = 0.215mW$$

AND Gate: If $V(0) = 0V$ and $V(1) = 5V$,
ans $R_S = 0.25k\Omega$, $R = 100k\Omega$. Fan In $N=2$

(a) Find out the output voltage levels.
(b) Find out the maximum power dissipation.



Operating Mode of BJT



- (a) Saturation region
- (b) Active region
- (c) Cutoff region
- (d) Reverse Active region

V_{BC}	
Reverse Active $V_C < V_B < V_E$	Saturation $V_E < V_B$ $V_C < V_B$
Cut-Off $V_E > V_B$ $V_C > V_B$	Forward Active $V_C > V_B > V_E$
V_{BE}	

cut in voltage

Region	$V_{BE} (V)$	$V_{CE} (V)$	Current Relationships	Test
Cutoff	< 0.5	$0.2 -$	$I_B = I_C = I_E = 0$	$V_{BE} < 0.5$
Forward active	0.7	> 0.2	$I_C = \beta_F I_B$ $I_E = I_B + I_C$	$V_{CE} > 0.2$
Saturation	0.8	$0.2/0.1$	$I_B > \frac{I_C}{\beta_F}$	$I_B \geq \frac{I_C}{\beta_F}$
Reverse active	$< -0.6V$ ($V_{BC} = 0.7V$)	< -0.2	$I_E = \beta_R I_B$	$V_C < V_B < V_E$

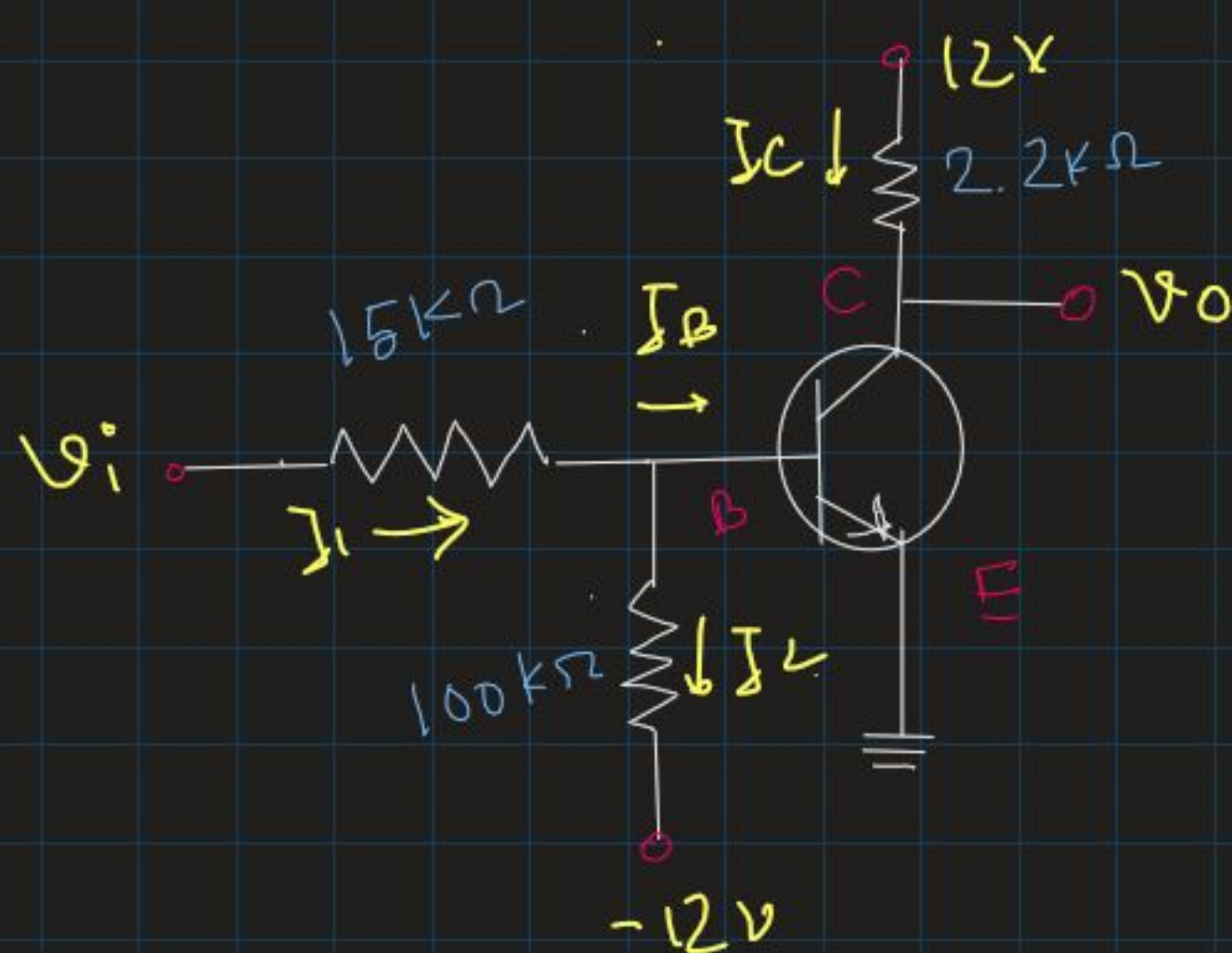
$V_{BE} > 0$
 $V_C > V_B$

β_F = Forward active current gain

β_R = Reverse active current gain

RTL Inverter : If the value of beta = 30 , Find the output voltage levels considering the input voltage levels to be 0 v and 12 v

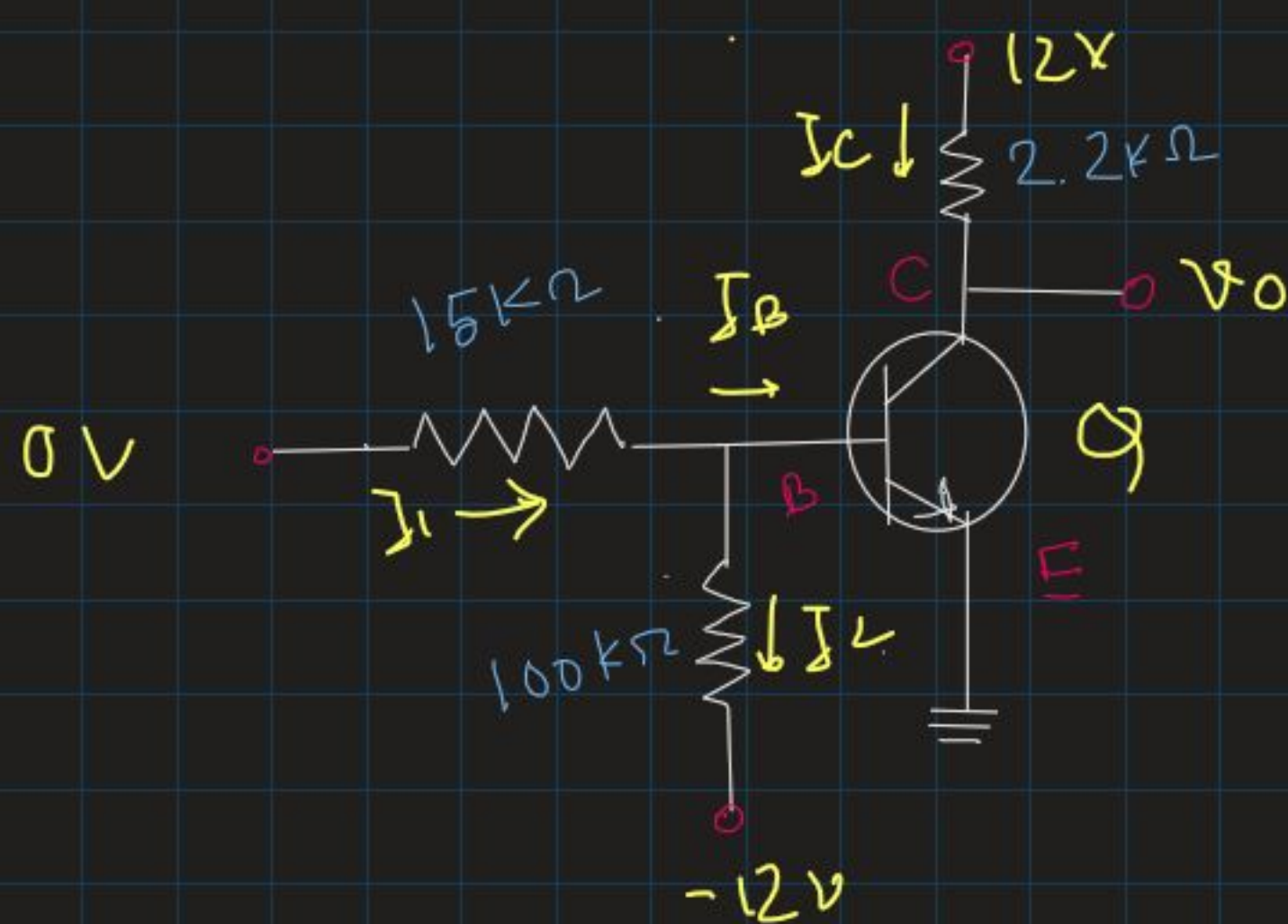
12V
0.2V



first case :-

$V_{in} > 0.5$

$\alpha \rightarrow$ cutoff



$$I_C = I_E = I_B = 0$$
$$V_o = 12V$$

$$I_1 = I_2 = \frac{0 - (-12)}{(100 + 15)k\Omega} = 0.1043mA$$

$$I_1 = \frac{0 - V_B}{15k\Omega} = 0.1043mA$$

$$V_B = -0.1043 \times 15 = -1.565V$$

$$V_B < 0.5V \text{ (cutoff)}$$

second case :-

$\alpha \rightarrow$ saturation

$$\left. \begin{array}{l} V_{BE} = 0.8V \\ V_{CE} = 0.2V \end{array} \right\} V_E = 0V$$
$$V_B = 0.8V$$

$$V_C = 0.2V$$

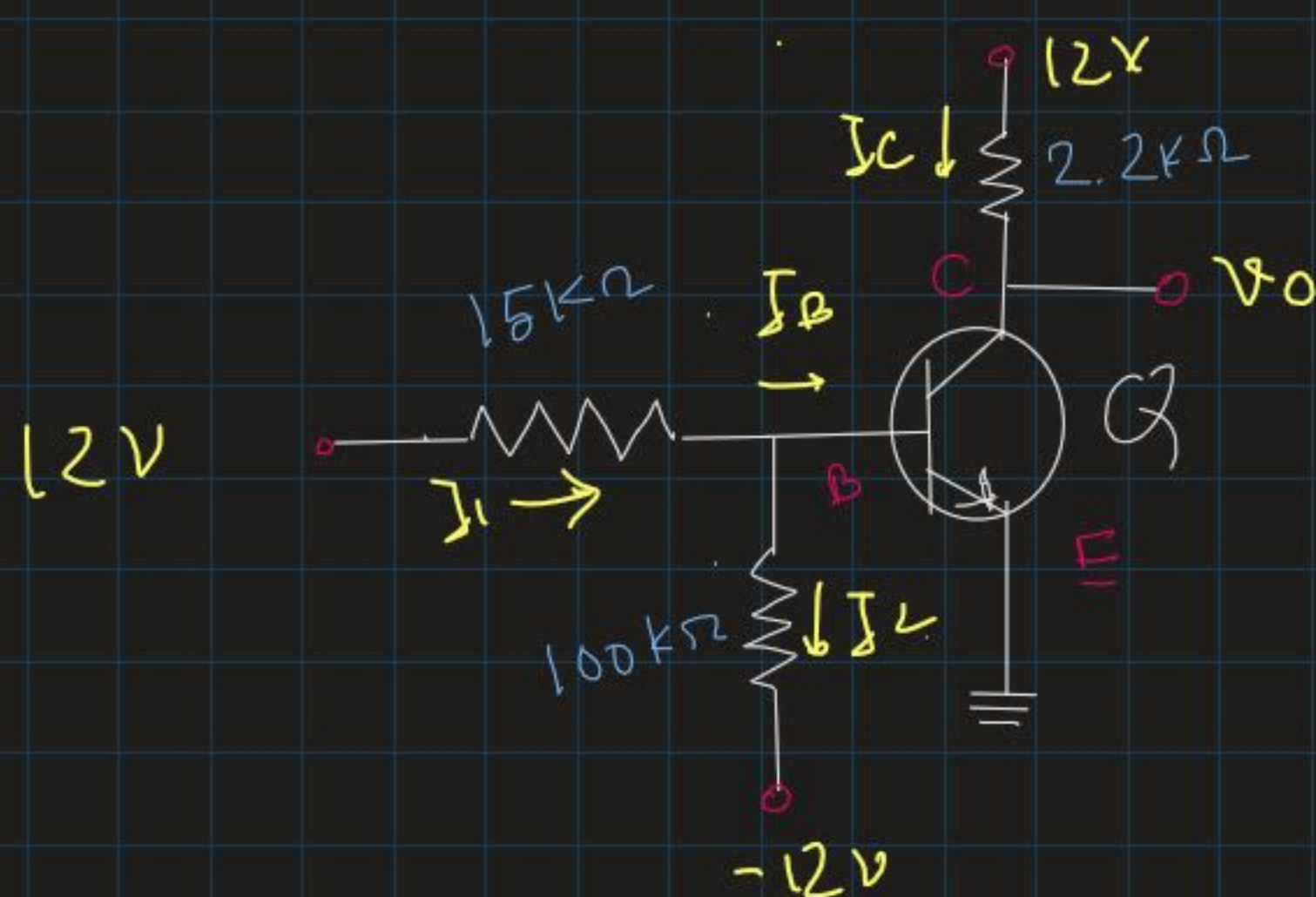
$$I_1 = \frac{12 - 0.8}{15k\Omega} = 0.746mA$$

$$I_2 = \frac{0.8 - (-12)}{100k\Omega} = 0.128mA$$

$$I_1 = I_2 + I_B$$

$$I_B = I_1 - I_2 = 0.746 - 0.128 = 0.617mA$$

$$\beta_{forced} = \frac{I_C}{I_B} = \frac{5.36}{0.617} = 8.69 < \beta(30)$$



$$I_C = \frac{12 - 0.2}{2.2k\Omega} = 5.36mA$$

RTL (Resistor - Transistor Logic) Family

1. High logic voltage level for circuit - 1 to 3.6 volt.
2. low logic voltage level for circuit - 0.2 volt.
3. power dissipation of the RTL gate = 12 mW
4. Propagation delay averages 25 ns

Problem : Calculate the output voltage level for different possible input levels

Truth table:

A	B	C	QA	QB	QC	Y
Low	Low	Low	off	off	off	3.6V
Low	Low	High	off	off	on	0.2V
Low	High	Low	off	on	off	0.2V
High	Low	Low	on	off	on	0.2V
Low	High	High	off	on	on	0.2V
High	Low	High	on	off	on	0.2V
High	High	Low	on	on	off	0.2V
High	High	High	on	on	on	0.2V

2nd case:

3 min calculation:

$$V_{BE} = 0.8V$$

$$B_1 + \sin \alpha \quad V_F = 0$$

$$V_B = 0.8V$$

$$I_B = \frac{3.6 - 0.8}{\leq 500 \Omega} = 6.22 \text{ mA}$$

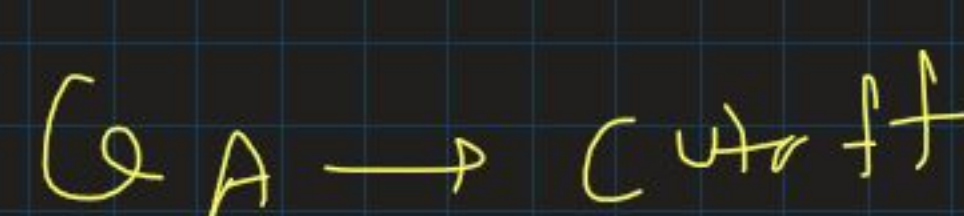
$$I_C = \frac{3.6 - 0.2}{r_{be}} = 5.3125 \text{ mA}$$

$$\beta_{\text{partikel}} = \frac{J_c}{J_\beta}$$

$$\begin{array}{r} 5.3125 \\ - 4.4595 \\ \hline 0.853 \end{array}$$

$$B_{min} = 0.853$$

5th case:


$$\begin{matrix} Q_B \rightarrow \\ G_C \rightarrow \end{matrix} \left\{ \begin{matrix} \text{saturation} \end{matrix} \right.$$

$V_{CE} \rightarrow$ same for all of them

$$i_{b40} = \frac{3.6 - 0.2}{r_{L10}} = 5.3125 \text{ mA}$$

$$I_{CB} = I_C = \frac{53125}{2} = 26562.5 \text{ mA}$$