Emitter Coupled Logic (ECL) / Current Mode Logic (CML)

- → Unsaturated Logic family (Transistors used in ECL circuit operate only in Forward Active and Cut off)
- → Fastest Logic family
- → Low propagation delay

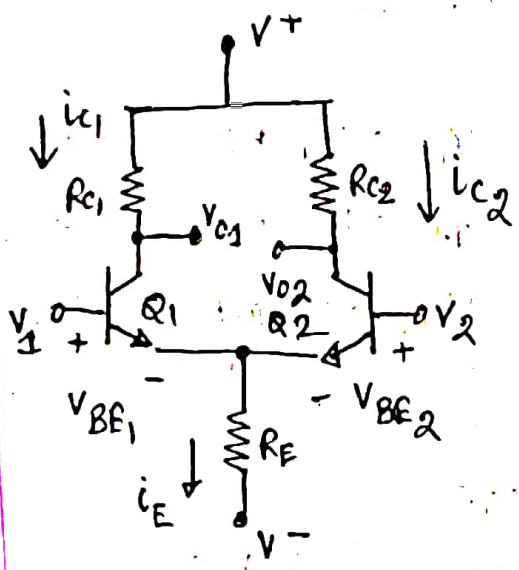


Fig: Basic Differential amplifier circuit.

Assumption

High β transistor $\Rightarrow \uparrow \beta = \frac{i_C}{i_B \downarrow}$

$\therefore i_B \approx 0$

KCL

$$i_E = i_{C_1} + i_{C_2}$$

$$V_d = V_{BE_1} - V_{BE_2}$$

$$= (V_{B_1} - V_{E_1}) - (V_{B_2} - V_{E_2})$$

$$= (V_1 - V_{E_1}) - (V_2 - V_{E_2})$$

$$\boxed{V_d = V_1 - V_2}$$

Case → $V_{BE_1} \gg V_{BE_2}$

Q_1 → Forward Active

Q_2 → cut off

Case → $V_{BE_2} \gg V_{BE_1}$

Q_1 → Cut off

Q_2 → Forward Active

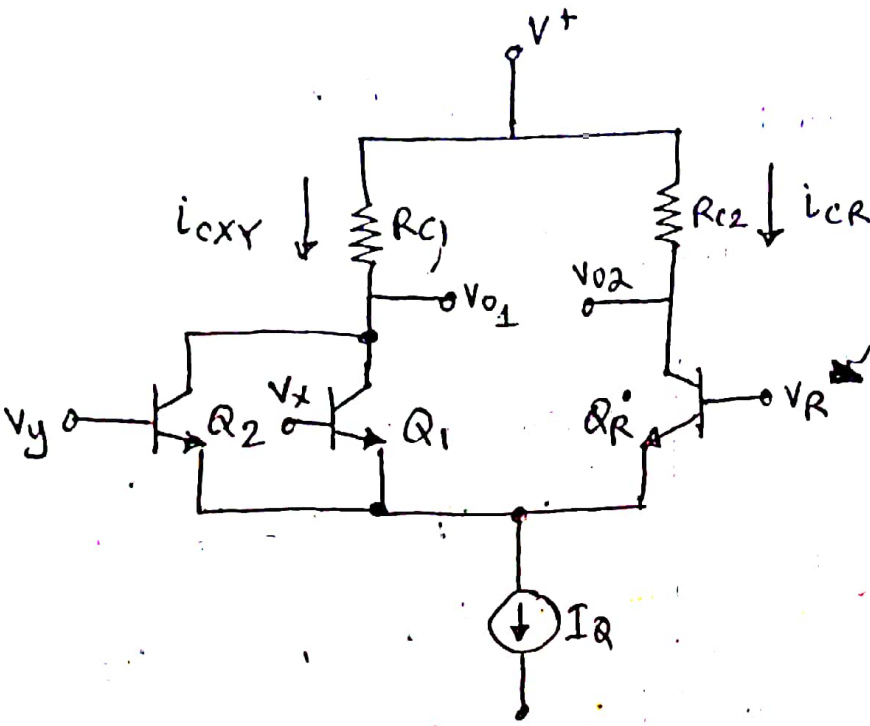
Diode current eqn

$$i_E = i_s e^{V_{BE}/V_T}$$

i_s → reverse saturation current

V_T → Thermal voltage = 25.9 mV

Basic ECL NOR Gate



V_{IL} → Input Low voltage

V_{IH} → Input high voltage

V_{OL} → output Low voltage

Truth Table

V_x	V_y	V_{O1}	V_{O2}
V_{IL}	V_{IL}	V^+	V_{OL_2}
V_{IH}	V_{IL}	V_{OL_1}	V^+
V_{IL}	V_{IH}	V_{OL_1}	V^+
V_{IH}	V_{IH}	V_{OL_1}	V^+

V_{O1} → NOR output

V_{O2} → OR output

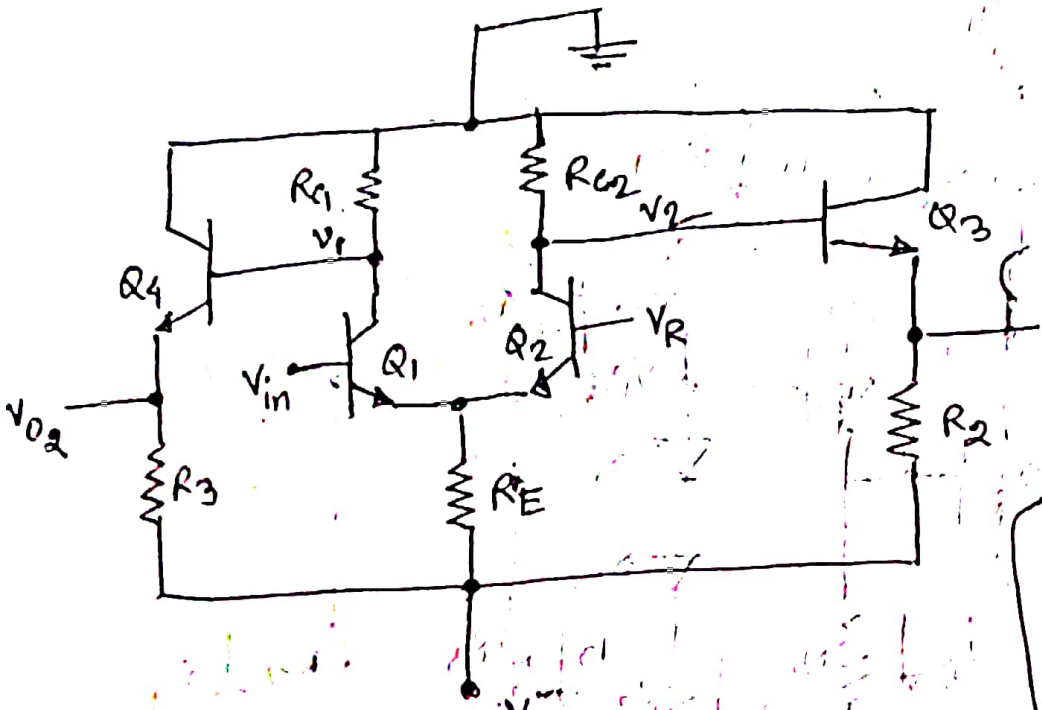
Advantage

Two different output Logic (OR, NOR) can be obtained from the same ECL gate

Logic "LOW" ↓ $V_{IL} < V_R$

Logic "HIGH" ↓ $V_{IH} \rightarrow V_R$

ECL NOT Gate



V_R → reference voltage
V_{in} → input

Base voltage ≤ Collector voltage
↓
Forward Active Mode

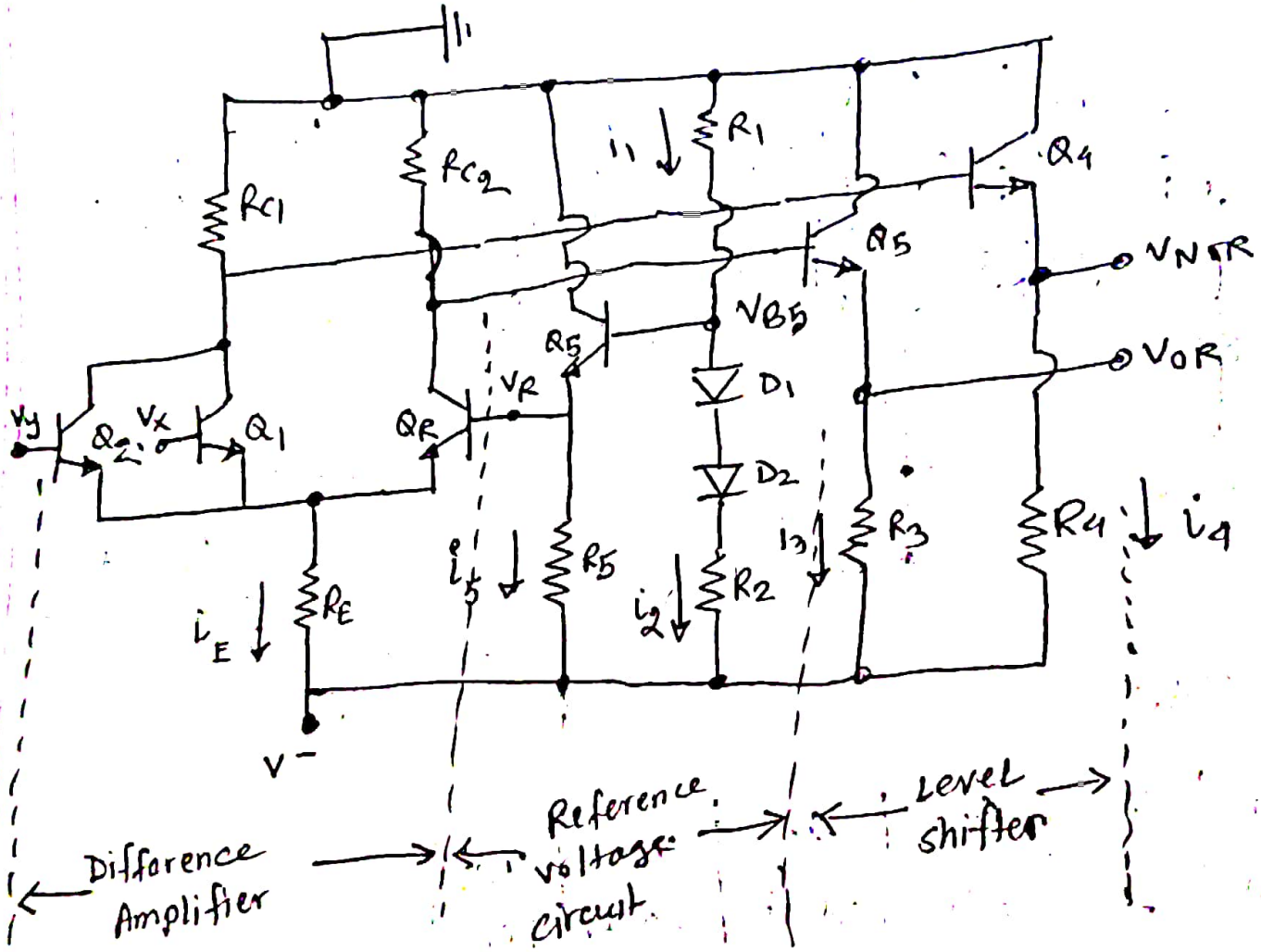
Truth Table

V_{in}	V_R	Q_1	Q_2	V_{O1}	V_{O2}
HIGH	–	Active	cut off	−0.7V	LOW
LOW	–	cut off	Active	LOW	HIGH

$$V_R = \frac{\text{Logic HIGH} + \text{Logic LOW}}{2}$$

Logic LOW → −1.7V
Logic HIGH → −0.7V

ECL NOR Gate with Reference circuit



Logic LOW → ~~-0.7~~ -1.4V

Logic HIGH → -0.7V

Q_5 → Forward Active

V_{OR} → OR output

V_{NOR} → NOR output

V_R → reference voltage

$$V_R = \frac{\text{Logic LOW} + \text{Logic HIGH}}{2}$$

$$= \frac{-1.4 - 0.7}{2} = -1.05V$$

$$\boxed{V_R = -1.05V}$$

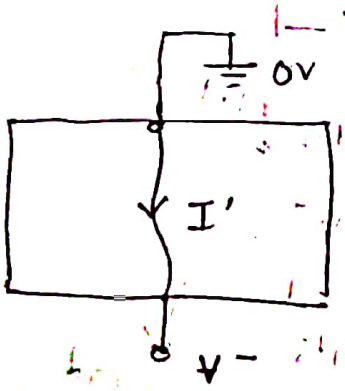
Diodes D_1, D_2 are used to reduce temperature variation in ECL circuit

Power Dissipation (max) in ECL NOR gate with reference circuit

$V_x = V_y = \text{HIGH} \rightarrow -0.7V$

$\therefore V_{OR} \rightarrow -0.7V$

$\therefore V_{NOR} \rightarrow -1.4V$



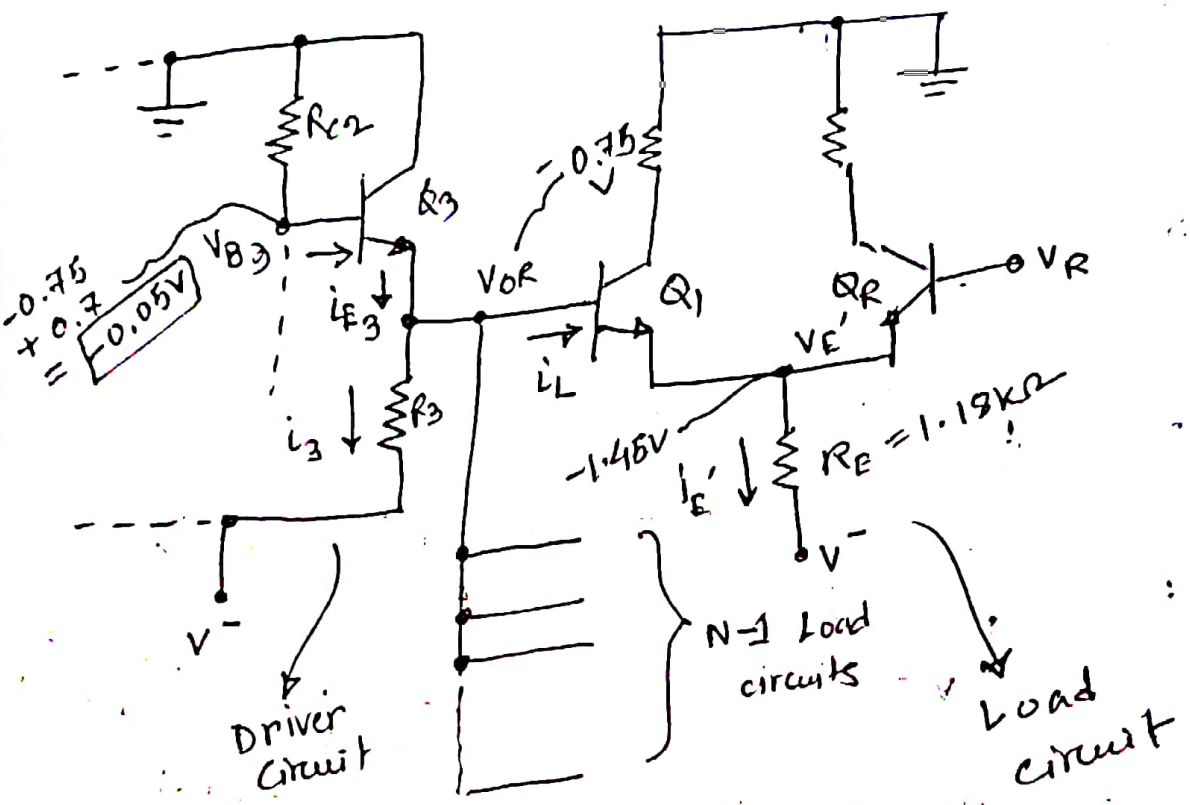
$$I' = i_E + i_5 + i_2 + i_3 + i_1$$

consider all the currents flowing from Ground to V^- terminal.

Power dissipation, $P = \Delta V \cdot I'$

$P = V^- \times I'$

Max. fanout of ECL Logic Gate



Loading effect → The change in output voltage due to adding Load circuit

V_{OR} → Logic HIGH = $-0.75V$

Q_1 → Forward Active

Q_R → cut off

$V_E' = -0.7 - 0.75$
$= -1.45V$

$i_E' = \frac{-1.45 + 5.2}{1.18}$
$= 3.48mA$

standard Load current

$i_L = i_B = \frac{i_E'}{(1+\beta)}$

Driver circuit

$i_{B3} = \frac{0 - V_{B3}}{R_{C2}}$

$i_{E3} = (1+\beta) i_{B3}$

KCL

$i_{E3} = i_3 + N i_L'$ ← fanout eqn