BRAC UNIVERSITY

Department of Electrical and Electronic Engineering

CSE350: Digital Electronics and Pulse Techniques

Experiment No: 1

Implementing Diode Logic (DL) gates

Objective:

1. Construction of DL gates.
2. Understanding the circuit operation

Circuit Diagram:

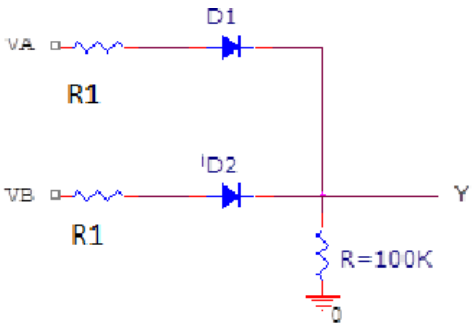


Fig 1: OR gate

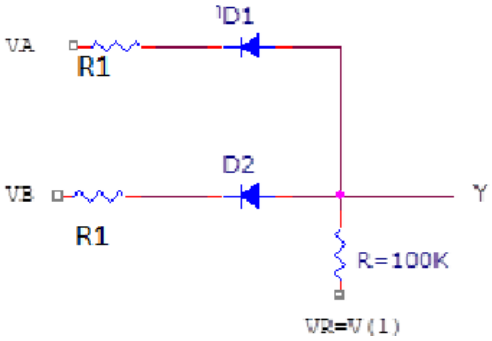


Fig 2: AND gate

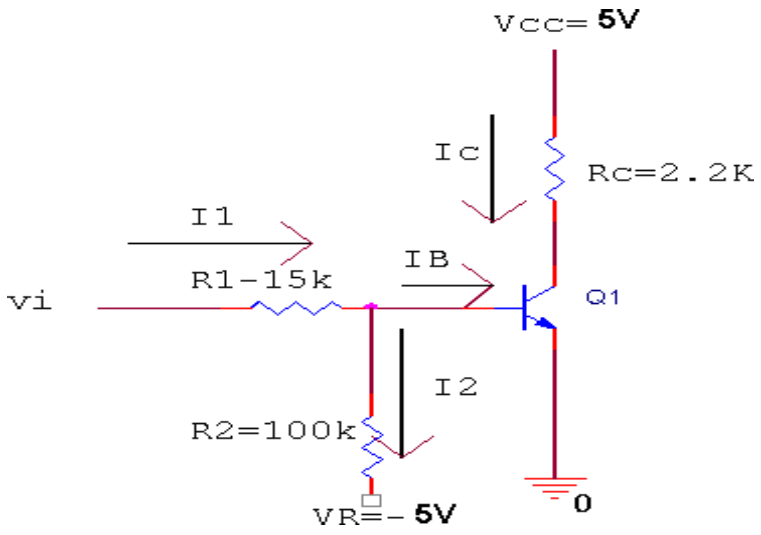


Fig 3: INVERTER for positive logic

Simulation tasks:

1. For DL OR and AND gate, assume the resistor value to be XXX where XXX is the last 3 digits of your student ID
1. Then draw the circuit as shown in Fig: 1,2 & 3 (In proteus)
2. Fill up the following table for OR gate, AND gate and inverter

V_A	V_B	V_{R1}	V_{R2}	I_{R1}	I_{R2}	V_R=Y

OR Gate

V_A	V_B	V_{R1}	V_{R2}	I_{R1}	I_{R2}	V_R=Y

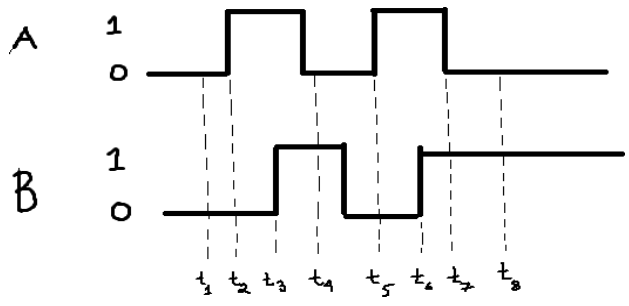
AND Gate

V_i	V_{R1}	V_{R2}	V_{RC}	I_1	I_2	I_B	I_C	Y

Inverter

Report:

1. Explain the operation of diode logic OR gate.
2. (For DL AND gate) If logic high voltage at the input (V_A ,V_B) is taken to be 6 V but V_R= 5V, then will the circuit still work as an AND gate? (use Proteus to change input voltage levels and observe the output)
3. Verify that the transistor will be operating in the saturation and cutoff region in two cases for the inverter circuit (Use Proteus Data for verification)
4. Can the inverter circuit function without the R2 = 100k resistor? Justify your answer using simulation data.
5. Assuming AND gate , draw the output timing diagram



Reference: Microelectronics: Digital and Analog Circuits and Systems by Jacob Millman. Page- 125-132