Kh. Jordan Zubair Nafis
19301007 { Sec:09, Lab:02, 350 } Last 4 digit of id is = 1007

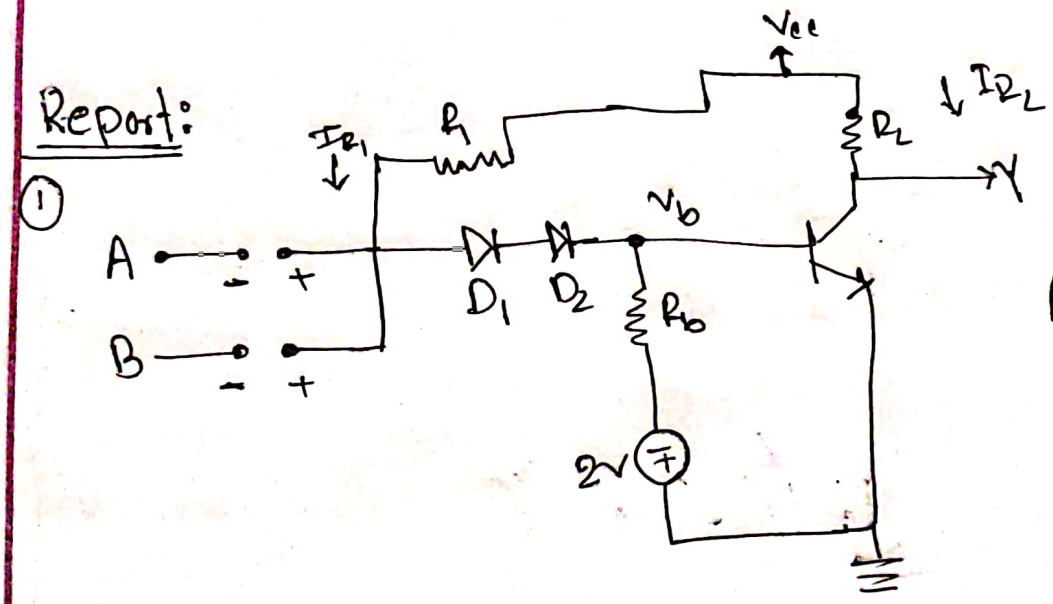
A	B	V_{DA}	V_{DB}	V_p	I_{R_1}	I_{R_2}	V_b	Output
0	0	0.67	0.67	0.67	4.3×10^{-3}	1.7×10^{-11}	0.50	5
0	1	0.69	-4.31	0.69	4.3×10^{-3}	1.7×10^{-11}	0.48	5
1	0	-4.31	0.69	0.69	4.3×10^{-3}	1.7×10^{-11}	0.48	5
1	1	-2.71	-2.71	2.29	2.69×10^{-3}	4.8×10^{-3}	0.92	0.1636

2nd

A	B	V_p	V_b	Output Y
1	0	0.69	0.48	5
1	1	2.29	0.92	0.1636

Report:

①



A,B = 5V

② In table-2, as 'A' is fixed (high), so, when V_B is low, output is high and when V_B is high, output is low. So, NOT gate Logical operation is used here.
As, V_A is high, so DA will be off. So, output depends only V_B. Output will be high, when input (only V_B) is Low and vice versa.

③ For two inputs, if either one will high or both will high, we will get high output. But for both high input, we will get Low output. In our lab circuit, input A,B and diode A,B are connected with AND gate and right side of circuit is connected with RTL inverter. In this way, AND operation is performed in DTL NAND and invert it by RTL inverter.

A	B	output
0	0	1
0	1	1
1	0	1
1	1	0

1930107.

④ If one input is high another one is low, the Q_1 will be in cutoff mode.

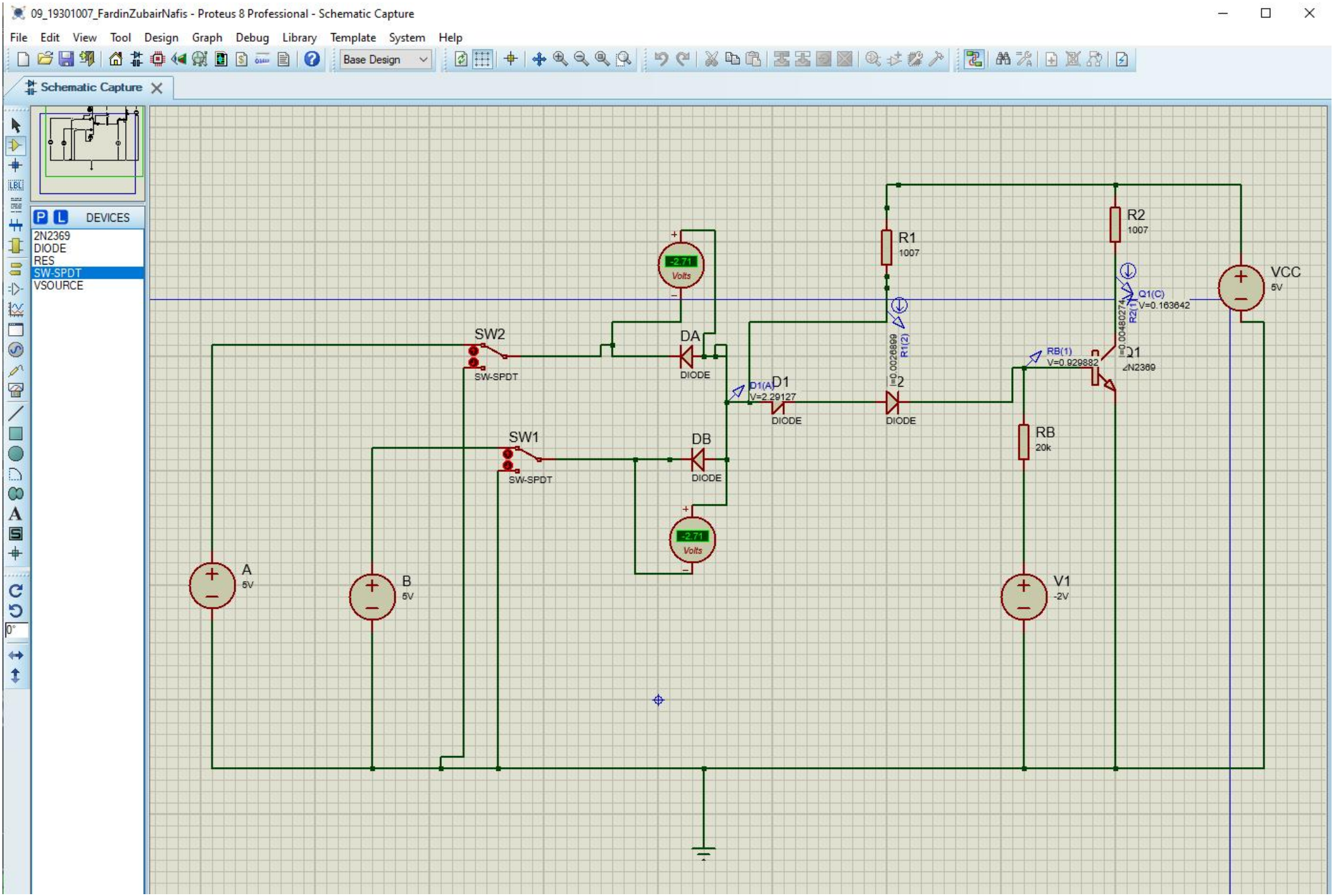
⑤ Either one of them have to high or both of them have to zero but not both of them high, will keep output high.

A	B	output
5V	0V	5V
0V	5V	5V
0V	0V	5V

⑤ From proteus, we saw that for V_A and V_B, if we put 1.2V, then output 3.87.

but A = 1.3V, B = 1.3V, then we will get low output.

So, max value of $V_A = V_B = 1.2V$.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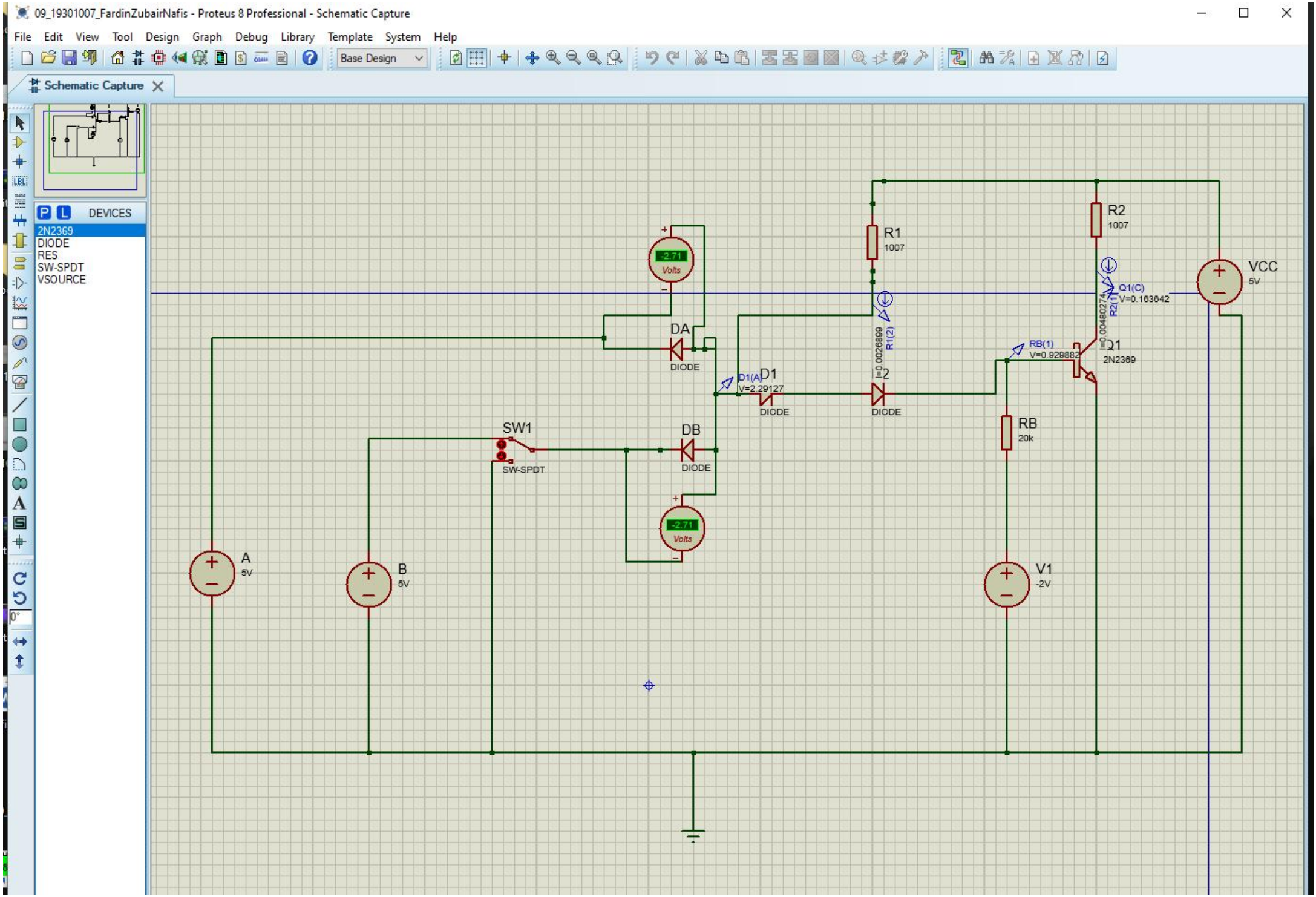
Base Design
Schematic Capture
DEVICES
2N2369
DIODE
RES
SW-SPDT
VSOURCE
SW2
SW-SPDT
SW1
SW-SPDT
DA
DIODE
DB
DIODE
-2.71
Volts
-2.71
Volts
D1(A)
V=2.29127
D1
DIODE
R1
1007
R1(2)
I=0.0026899
2
DIODE
R2
1007
Q1(C)
V=0.163642
R2(1)
I=0.00480274
RB(1)
V=0.929882
Q1
2N2369
RB
20k
VCC
5V
A
5V
B
5V
V1
-2V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B
5V
V1
-2V