Lab Assignment-4

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Section: 12
Course: CSE350

2d-17301042

circuit-1

Input configuration	D	C	B	A	Output Vo (V)
1	0	0	0	0	0.002
2	0	0	0	5	-0.497
3	0	0	5	0	-0.997
4	0	0	5	5	-1.497
5	0	5	0	0	-1.997
6	0	5	0	5	-2.497
7	0	5	5	0	-2.997
8	0	5	5	5	-3.497
9	5	0	0	0	-3.997
10	5	0	0	5	-4.497
11	5	0	5	0	-4.997
12	5	0	5	5	-5.497
13	5	5	0	0	-5.997
14	5	5	0	5	-6.497
15	5	5	5	0	-6.997
16	5	5	5	5	-7.497

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circuit-2

input configuration	D	C	B	A	output Vo (V)
1	0	0	0	0	.0049
2	0	0	0	5	-0.620
3	0	0	5	0	-1.245
4	0	0	5	5	-1.869
5	0	5	0	0	-2.495
6	0	5	0	5	-3.119
7	0	5	5	0	-3.744
8	0	5	5	5	-4.369
9	5	0	0	0	-4.994
10	5	0	0	5	-5.619
11	5	0	6	0	-6.244
12	5	0	5	5	-6.869
13	5	5	0	0	-7.494
14	5	5	0	5	-8.119
15	5	5	5	0	-8.744
16	5	5	5	5	-9.369

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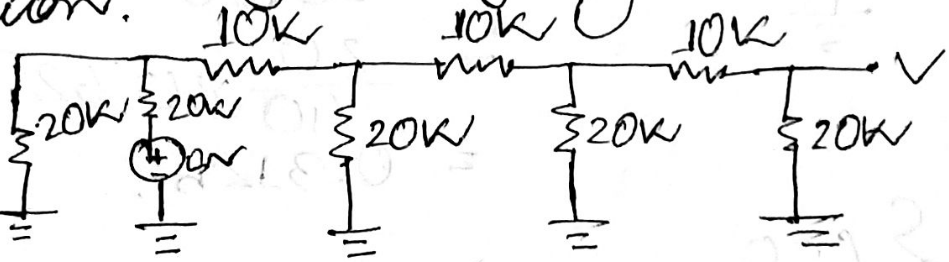
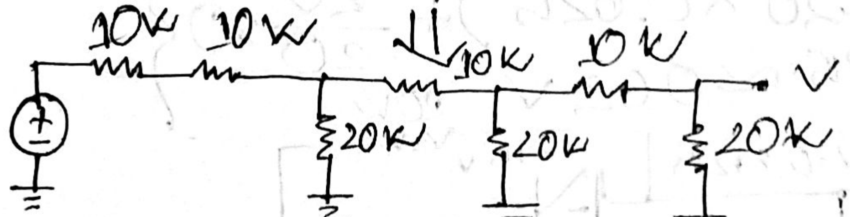
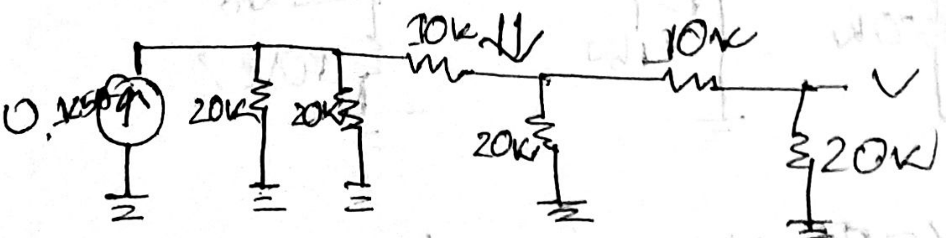
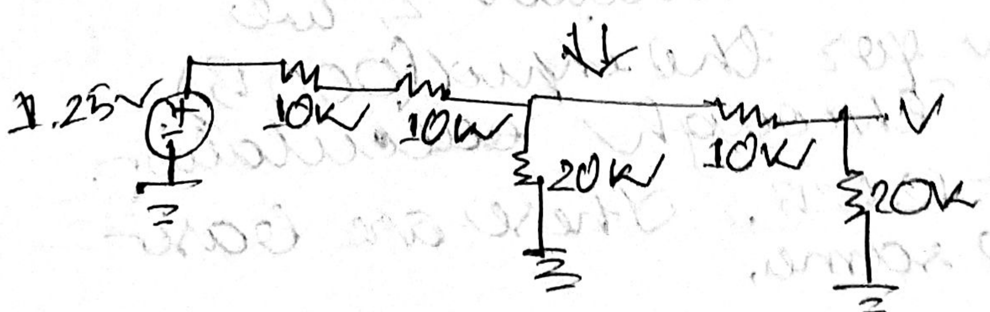
(1).

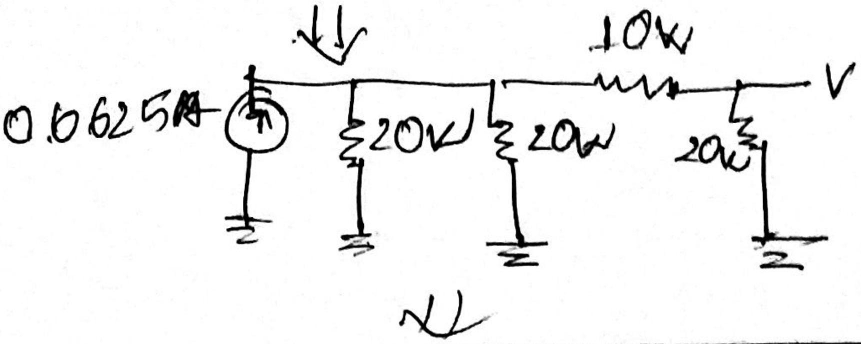
Let's take = 0001.
Here, A = 5V
B, C, D = 0V.
Now, By applying source transformation.



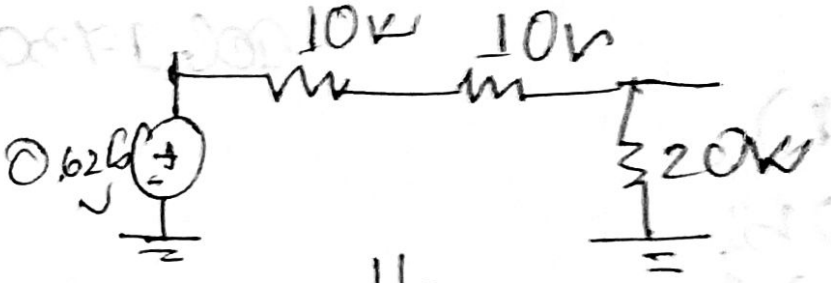


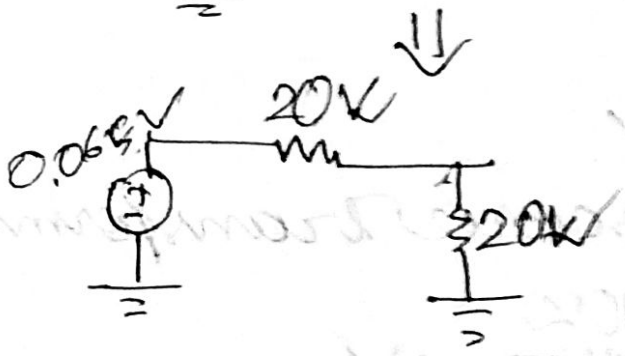






(P.T.O)





$$\therefore V = \frac{20}{20+20} \times 0.625$$

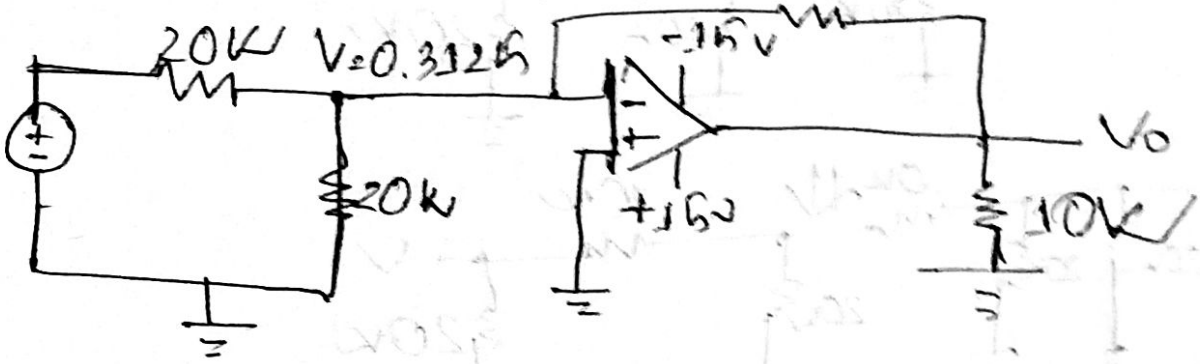
$$= \frac{20}{40} \times 0.625$$

$$= 0.3125.$$

Again,

$$V_0 - \left\{ \left(\frac{20}{20} \times 0.625 \right) + \frac{20}{20} \times 0 \right\}$$

$$= -0.625 \approx 0.62\,V$$



From proteus circuit 2, we get -0.620 v for the input (0005) and through calculation we get -0.625. These are basically the same.

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Id-1

(2)

The last two digits are 4 and 2.

∴ V0 high = 6, low = 0.

input configuration	D	C	B	A	output
1	0	0	0	0	0.002 V
2	0	0	0	6	-0.59 V
3	0	0	6	0	-1.19 V
4	0	0	6	6	-1.79 V
5	0	6	0	0	-2.39 V
6	0	6	0	6	-2.99 V
7	0	6	6	0	-3.59 V
8	0	6	6	6	-4.19 V
9	6	0	0	0	-4.49 V
10	6	0	0	6	-5.39 V
11	6	0	6	0	-5.99 V
12	6	0	6	6	-6.59 V
13	6	6	0	0	-7.19 V
14	6	6	0	6	-7.79 V
15	6	6	6	0	-8.39 V
16	6	6	6	6	-8.99 V

(P.T.O)

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(3)

For both the converters - here, input is 4 bits.

So. full step output $= 2^4 - 1$
$= 15$ step

Binary weighted resistors

step size $= -0.497$
full scale $= -7.497$

$\therefore$ resolution $= \frac{-0.497}{-7.497}$

$= 0.0662$

R and 2R

step size $= -0.620$
full scale $= -9.369$

$\therefore$ resolution $= \frac{-0.620}{-9.369} = 0.0661$

(4)

The step size corresponds to the RF.

if we increase RA step size will also increase proportionately.

Similarly decreasing the value of RA will also decrease step size proportionately.

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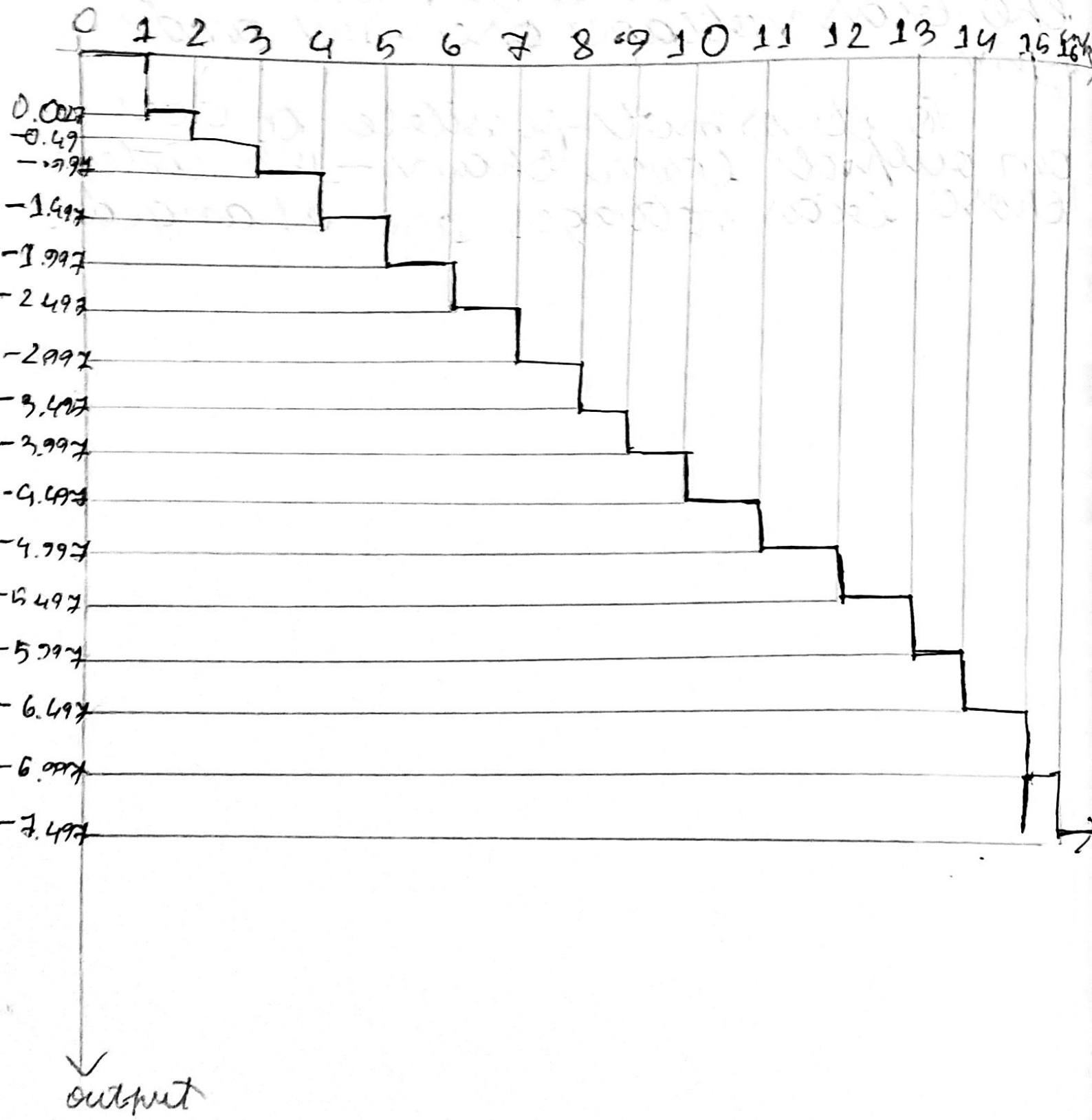
(5)

In the above D2A converters the bias voltages are -15V and +15V.

So it is not possible to get an output lower than -15V unless those bias voltages are changed.

(P.T.O)

circuit-1 (Binary weighted-resistors)



9 circuit-2 (R-2R)

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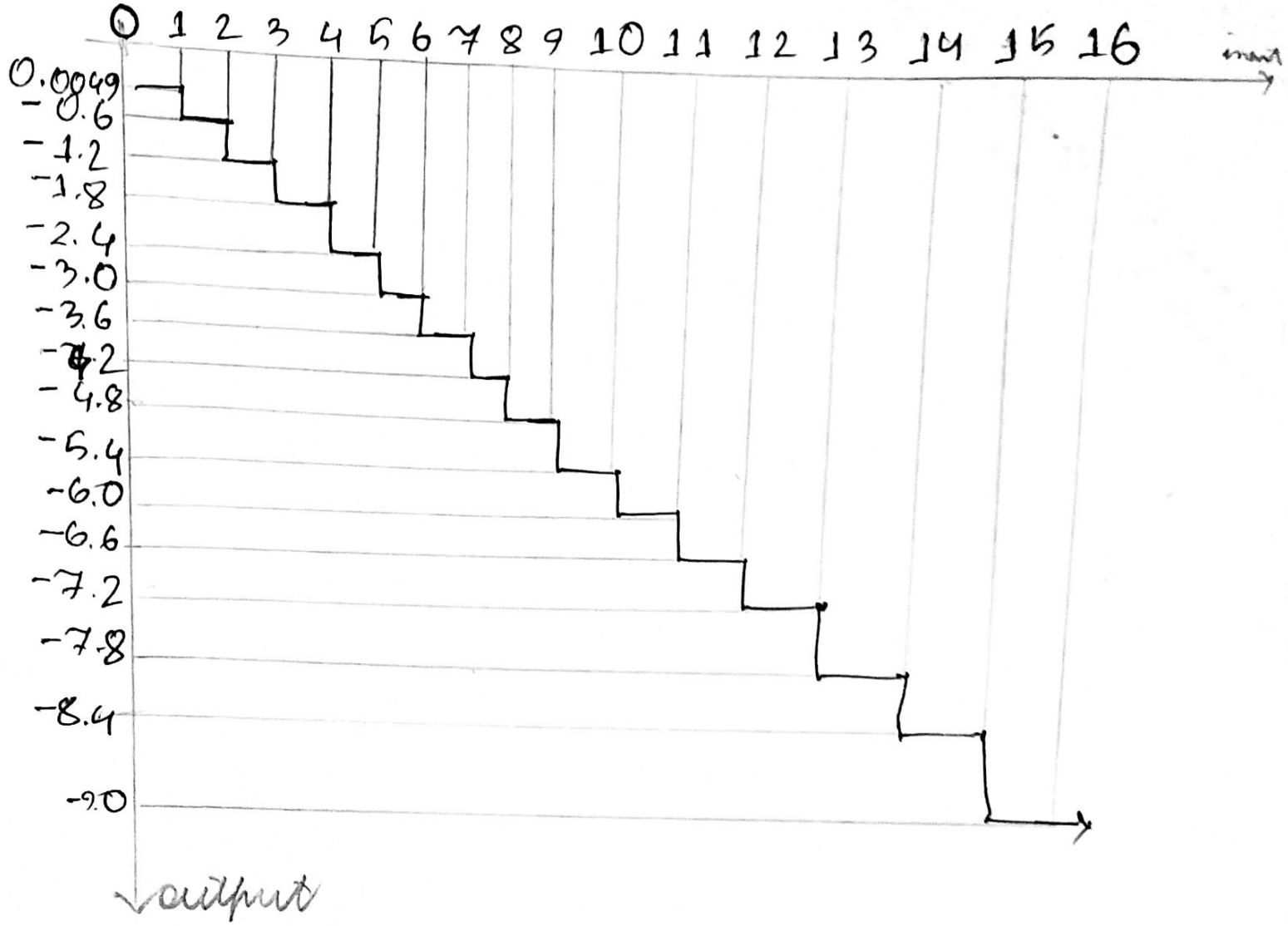

12_17301042_Rafsan Basher_circuit1 - Proteus 8 Professional - Schematic Capture

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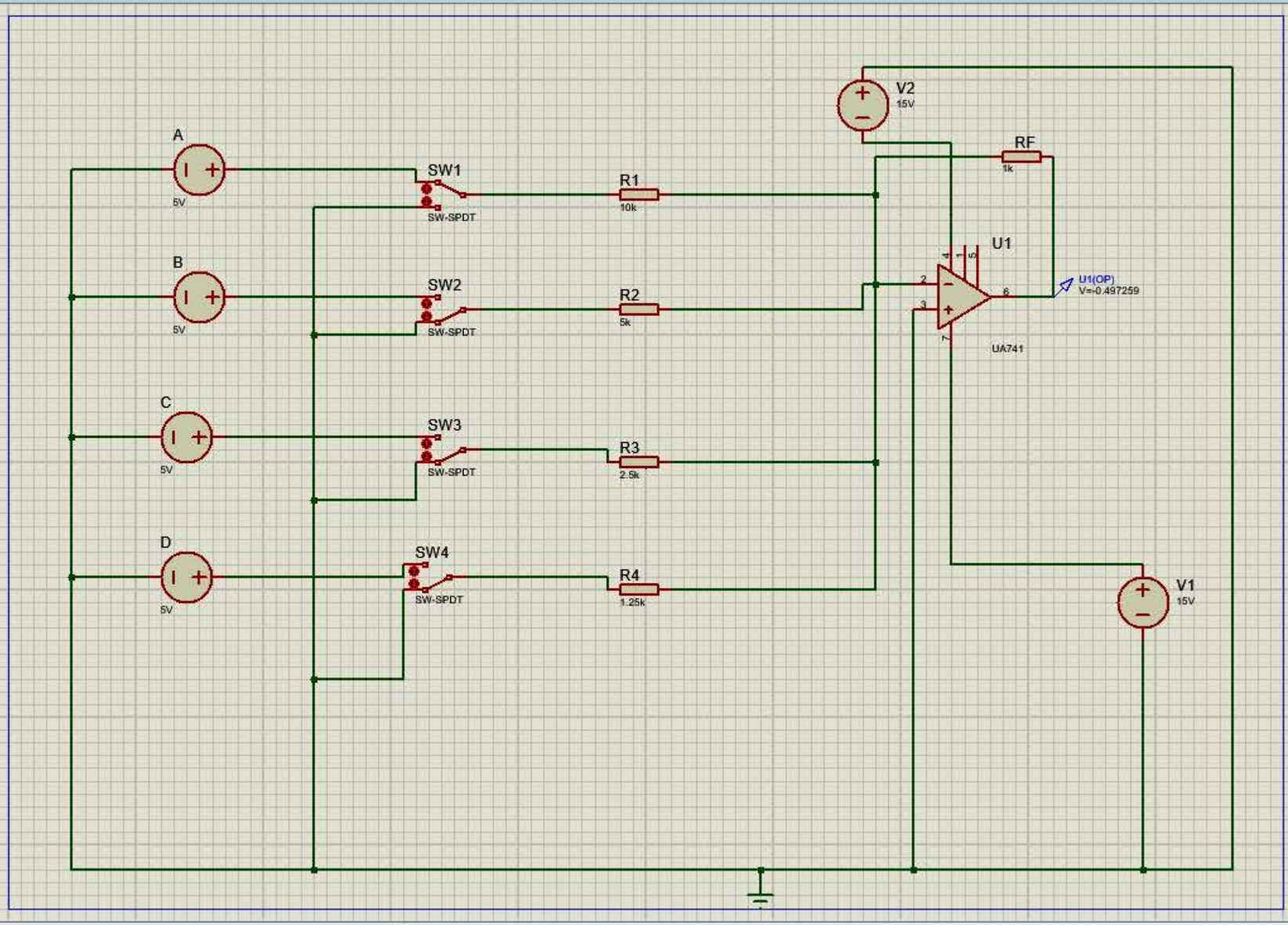
Base Design

Schematic Capture

DEVICES

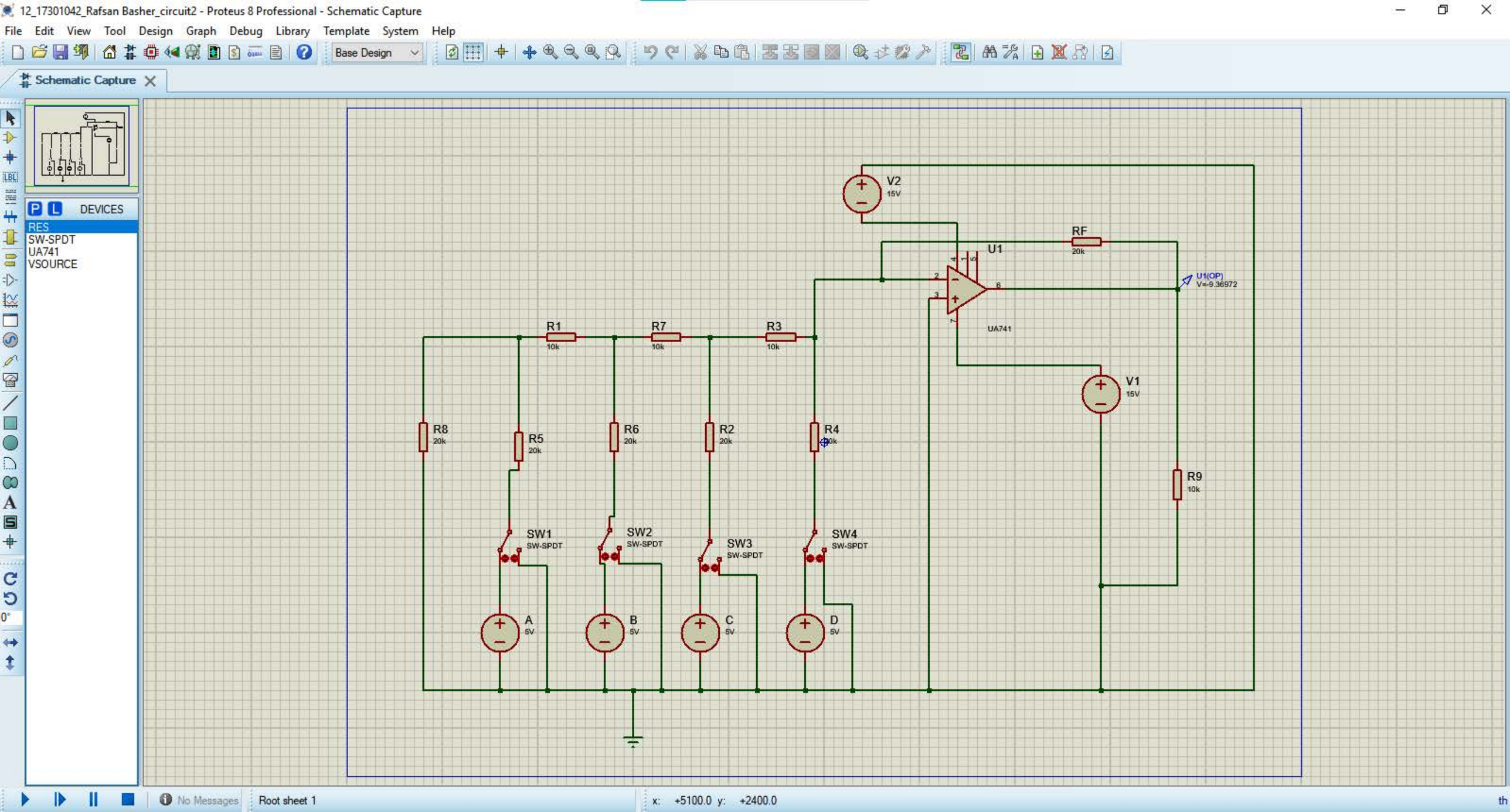
RES
SW-SPDT
UA741
VSOURCE



No Messages

Root sheet 1

x: +6500.0 y: -400.0


12_17301042_Rafsan Basher_circuit2 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
RES
SW-SPDT
UA741
VSOURCE
V2
15V
RF
20k
U1
UA741
U1(OP)
V=-9.36972
R1
10k
R7
10k
R3
10k
V1
15V
R8
20k
R5
20k
R6
20k
R2
20k
R4
20k
R9
10k
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT
SW4
SW-SPDT
A
5V
B
5V
C
5V
D
5V
No Messages
Root sheet 1
x: +5100.0 y: +2400.0