CSE 350
LAB-3

Name: Kazi Md. Al-Wakil

ID: 19301051

Section: 12

Group: 2

Table: 1

Input A	Input B	Input (VA)	Input (VB)	V_0 (V)	V_1 (V)	V_2 (V)	V_3 (V)	V_4 (V)	V_5 (V)	V_6 (V)
0	0	0	0	4.601	0.717	0.0077	7.24×10^{-09}	5	4.798	5
0	1	0	5	4.601	0.755	0.049	7.32×10^{-09}	5	4.798	5
1	0	5	0	4.601	0.755	0.049	7.32×10^{-09}	5	4.798	5
1	1	5	5	0.0093	2.656	1.9469	1.04003	~~1.31×10^{-07}~~ 1.13256	0.572	4.997

Report:

1. Totempole circuit is one kind of modified TTL circuit. This circuit has been designed specifically to decrease time when the output voltage is in transition period.

Also, totempole TTL circuit keeps the power dissipation in a moderate level.

In ~~tom~~. totempole TTL the total resistance of a extra resistor, a transistor and a diode is

less than the regular resistor Rc (which use is used in TTL). Totempole TTL can charge the capacitor faster and switching time speed also increases due to active pull up network.

② The ~~fi~~ circuit given in figure-1 is working as an NAND gate. When the input is low or mixture of high and low it is giving high output voltage.

When the input voltages are high, the output voltage is giving low voltage.

A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

This characteristic of totempole TTL is considered as a NAND gate.

Date: ...../...../.....

When any of the input is low then all the current goes through them and ahlen some operation modes the circuit gives high output voltage. When the inputs are high, no current passes through them and ahlen some operation modes, output voltage will be logically low.

Thus the figure-1 circuit is acting like a NAND Gate.

(3) We will be considering 4 cases.

When

both the inputs are logical ~~low~~ high, then

$T_3 \rightarrow$ Saturation mode

When,

One input is low, other is high and vice versa, then

$T_3 \rightarrow$ cut off

When,

Both the inputs are logical low, then

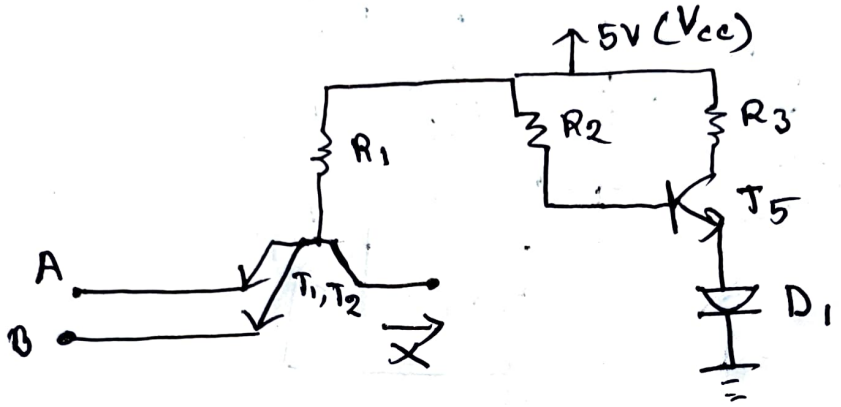
$T_3 \rightarrow$ cut off

4. Active portion when both inputs are low:

$T_1, T_2 \rightarrow$ Saturation mode

$T_3, T_4 \rightarrow$ Cutoff

$T_5 \rightarrow$ Forward Active



(5) If the D_1 diode is not used in the circuit then,

the T_5 transistor will be turned on whe both the inputs are ~~output~~ logical high.

As we know, when both the inputs are logical high then T_1, T_2 → Reverse Active

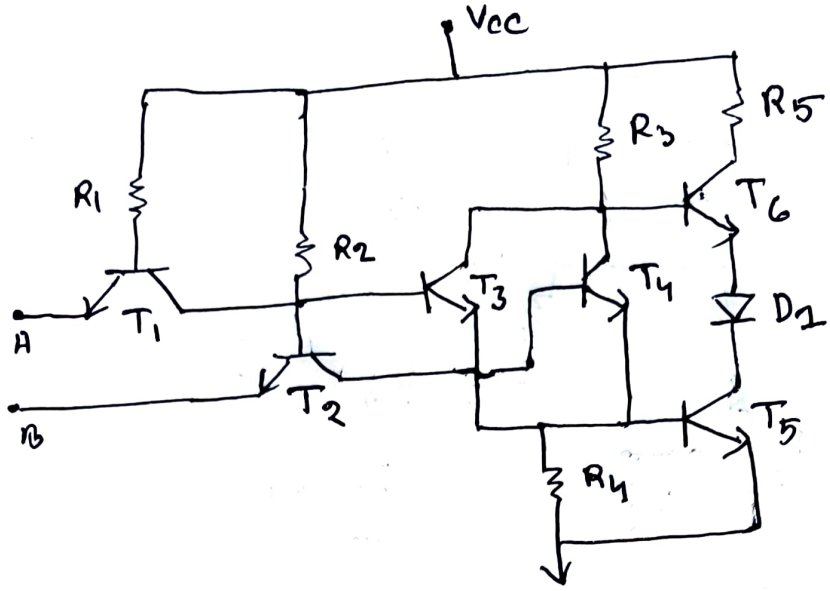
T_3, T_4 → Saturation

Q_3, D_1 → cutoff.

Q_3, D_1 is in cutoff because there is not enough voltage available to ~~th~~ turn both transistor and diode on. That's why they are in cutoff. But when the diode will be not ~~pres~~ present then the transistor will be turned on as it requires only 0.5 volt to turn on. For this reason the ~~out~~ output voltage will be logical ~~high~~ low but the value will be increased by a lot.

So, if we remove the D_1 diode, the outputs states will remain same but the values will be different.

6. A TTL NOR gate with Totem pole output stage:



7. Mode of operation of the T_5 transistor: (when at least one input is low): Forward Active.

Here,

we know, a transistor is in forward active mode

then,

$$V_{BC} \leq 0$$

Here, $V_B = 5V$, $V_C = 5V$

So, $V_{BC} = V_B - V_C$

$= 5 - 5$

$= 0$

Also,

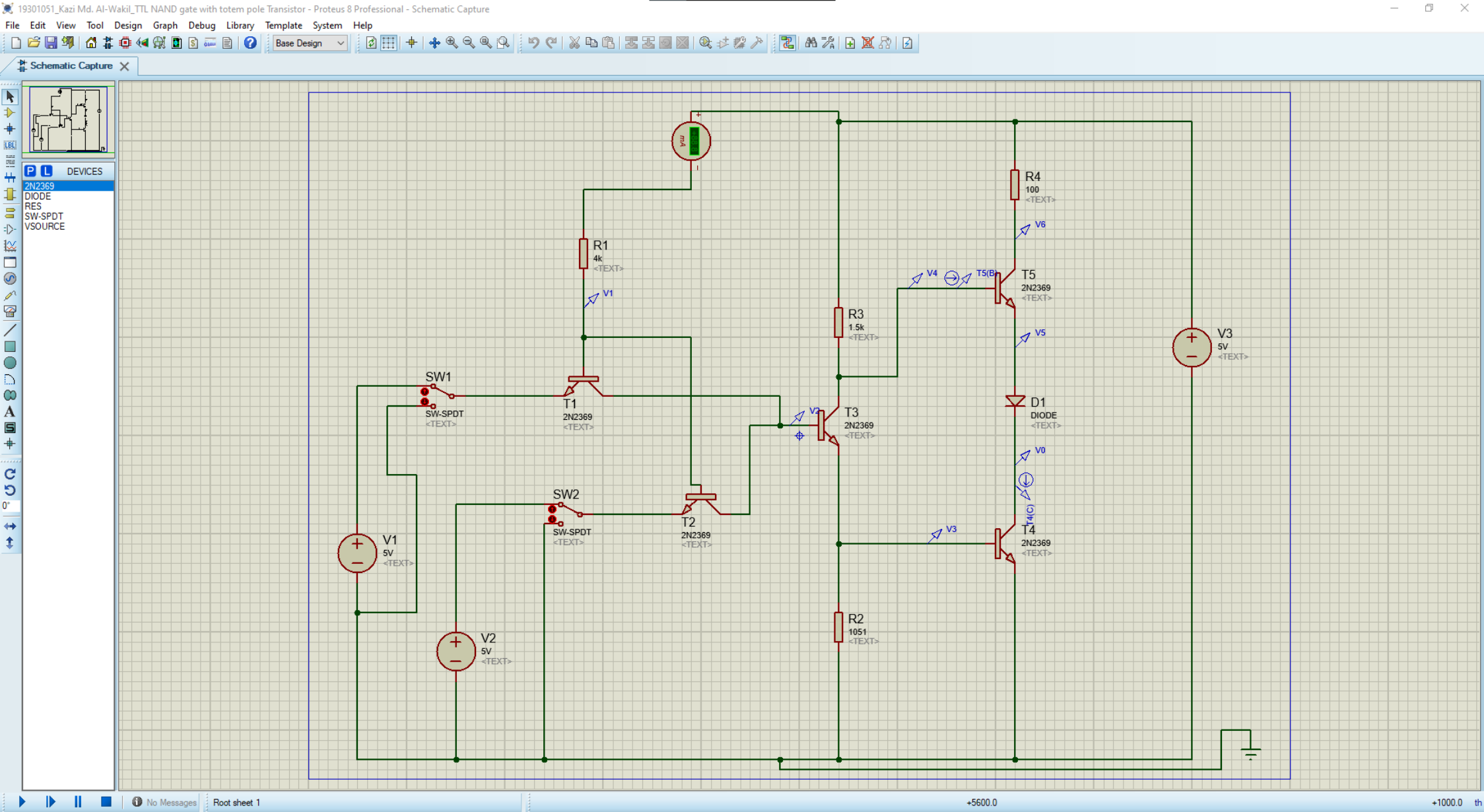
$V_C = 5V$, $V_E = 4.798$

So, $V_C - V_E$

$= 5 - 4.798$

$= 0.202 \geq 0.2$

So, T_5 is in forward Active.


19301051_Kazi Md. Al-Wakil_TTL NAND gate with totem pole Transistor - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
2N2369
DIODE
RES
SW-SPDT
VSOURCE
R1
4k
R2
1051
R3
1.5k
R4
100
SW1
SW-SPDT
SW2
SW-SPDT
T1
2N2369
T2
2N2369
T3
2N2369
T4
2N2369
T5
2N2369
D1
DIODE
V1
5V
V2
5V
V3
5V
V0
V1
V2
V3
V4
V5
V6
T4(C)
T5(B)
No Messages
Root sheet 1
+5600.0
+1000.0