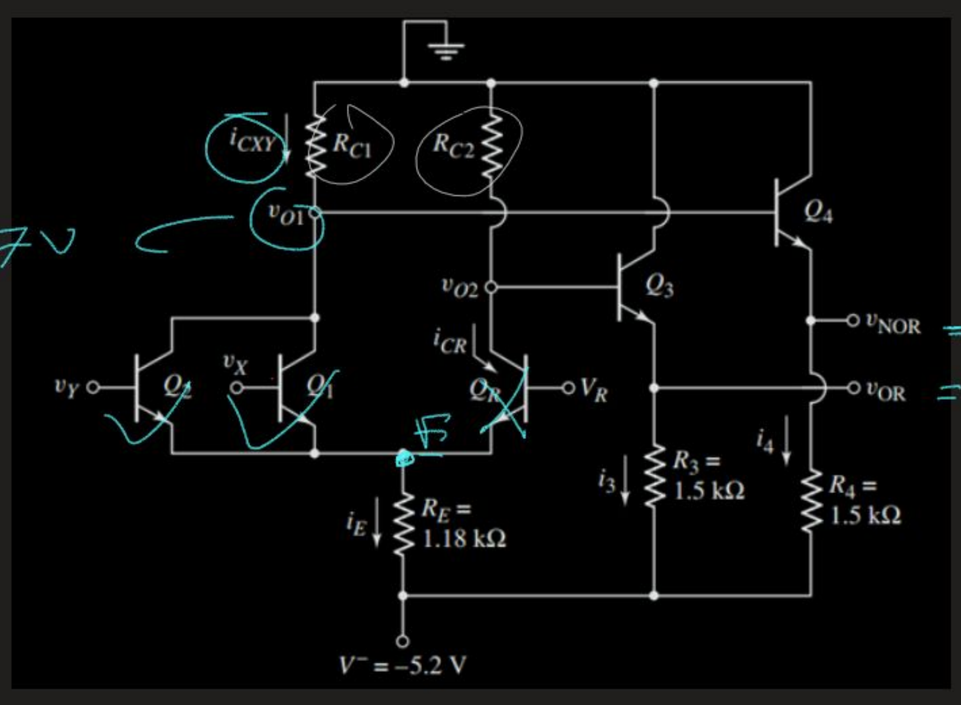
Lecture 10 part 1

Thursday, July 8, 2021 11:22 PM

EXAMPLE 17.2

Objective: Calculate current, resistor, and logic 0 values in the basic ECL logic gate.

Consider the circuit in Figure 17.4. Determine R_{C1} and R_{C2} such that when Q_1 and Q_2 are conducting, the B–C voltages are zero.



$-0.7V$

$v_{NOR} = -1.4V$

$v_{OR} = -0.7V$

$V_{BC} = 0$

$v_x = v_y = v_{High} = -0.7V$

$V_{BE} = 0.7\ V$

$V_E = (-0.7 - 0.7)\ V$

$= -1.4V$

$I_E = \dfrac{-1.4-(-5.2)}{1.18\ k\Omega}$

$= 3.22\ mA$

$v_{O2} = 0\ Volt$

$v_{O1} = -0.7\ Volt$

$i_{CXY} = i_E = 3.22\ mA$

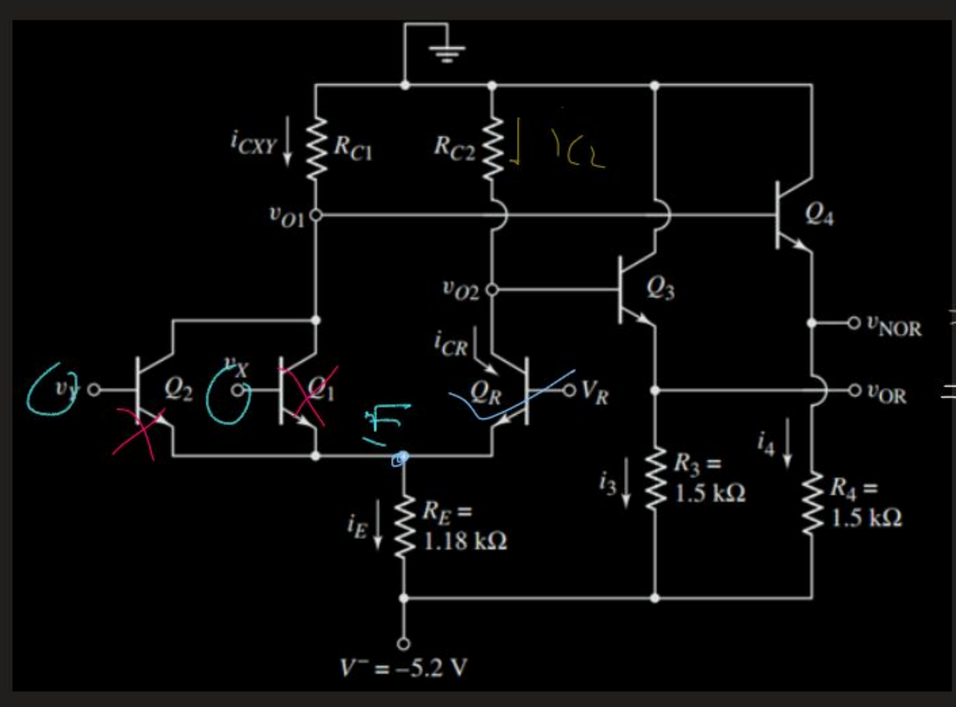
$i_{CXY} = \dfrac{0 - v_{O1}}{R_{C1}}$

$R_{C1} = 217\ ohm$

$i_4 = \dfrac{-1.4-(-5.2)}{1.5\ k\Omega} = 2.53\ mA$

$i_3 = \dfrac{-0.7-(-5.2)}{1.5\ k\Omega} = 3\ mA$

(ii) When both inputs are at logic low:



$v_{NOR} = -0.7V$

$v_{OR} = -1.4V$

$v_x = v_y = -1.4\ V \rightarrow$ Logic low

High ——— -0.7

——— V_R

Low ——— $-1.4V$

$V_R = \dfrac{-0.7-1.4}{2} = -1.05V$

$V_E = -1.75\ V.$

$I_E = \dfrac{-1.75-(-5.2)}{1.18k\Omega} = 2.92\ mA$

$v_{O2} = -1.05\ Volt$ ✗

$v_{O1} = -0.7\ volt$ ✓

$v_{OR} = -1.4V$

$I_{C2} = I_E = \dfrac{0 - v_{O2}}{R_{C2}}$

$R_{C2} = 240\ \Omega$

Lecture 10 part 2

Thursday, July 8, 2021 11:20 PM

Design the reference portion of the ECL circuit.

Consider the circuit in Figure 17.5. The reference voltage VR is to be –1.05 V.

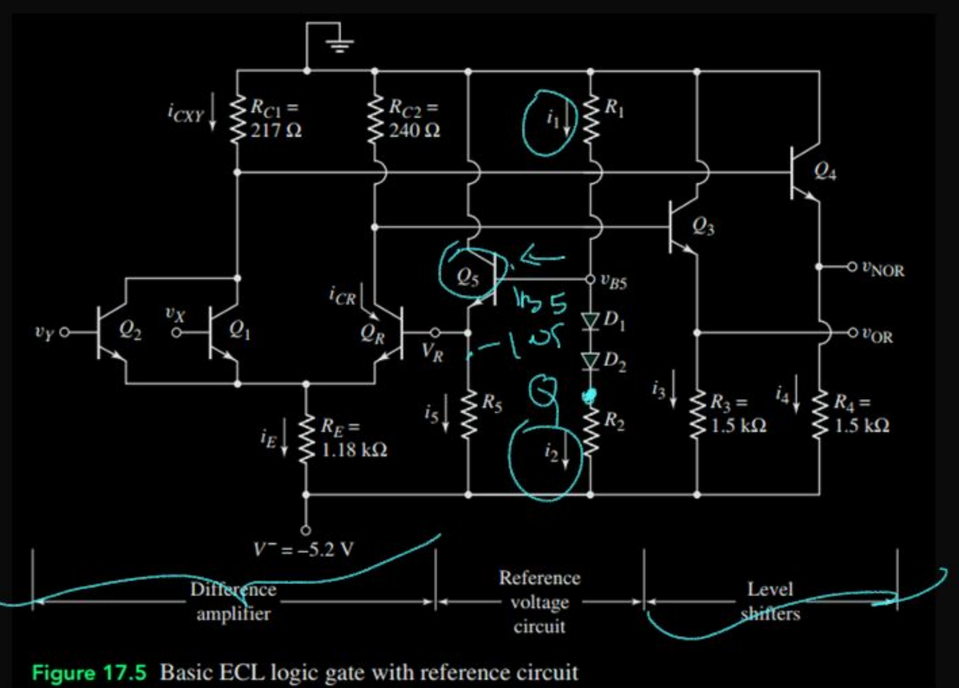


Figure 17.5 Basic ECL logic gate with reference circuit

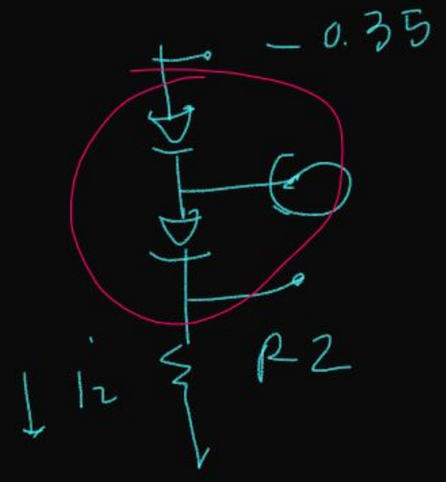
$v_{B5} = -0.35$ volt

$R_1 = 250\,\Omega$

$i_1 = \dfrac{0 - (-0.35)}{250\,\Omega} = 1.4$ mA

$i_{B5} \approx 0$

So, $i_1 = i_2$



$v_Q = -0.35 - (2 \times 0.7)$

$= -1.75$ volt

$i_2 = \dfrac{V_Q - (-5.2)}{R_2}$ $\Rightarrow 1.4$ mA $= \dfrac{-1.75 - (-5.2)}{R_2}$

$R_2 = 2.46\,k\Omega$

$i_{Q5} = i_1 = 1.4$ mA

$i_5 = i_{Q5} = i_1 = 1.4$ mA

$i_5 = \dfrac{-1.05 - (-5.2)}{R_5}$

$R_5 = 2.96\,k\Omega$

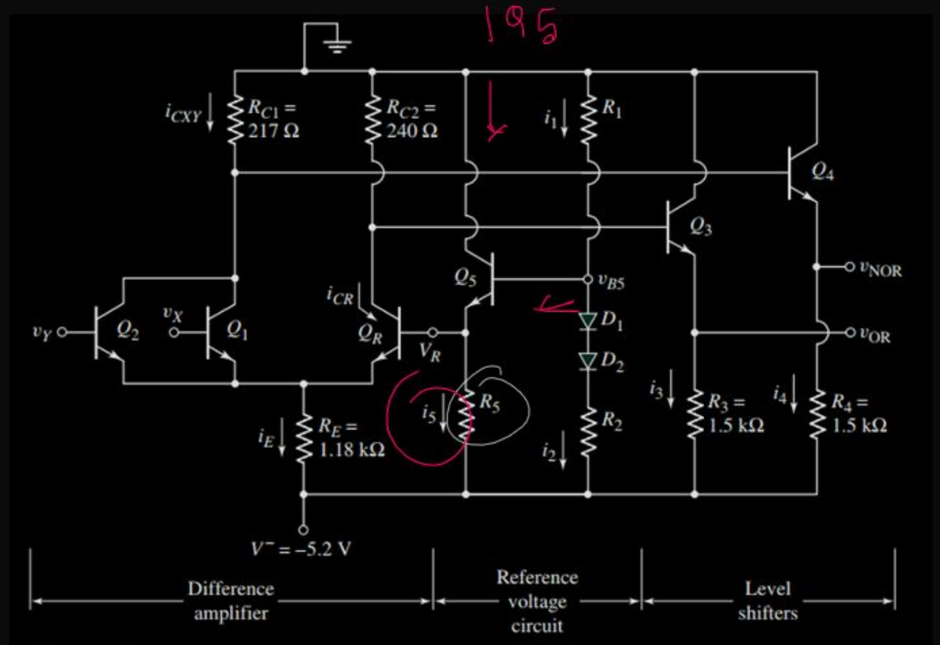


Figure 17.5 Basic ECL logic gate with reference circuit

Lecture 10 Part 3

Friday, July 9, 2021 2:11 AM

EXAMPLE 17.4

Objective: Calculate the power dissipated in the ECL logic circuit.

Consider the circuit in Figure 17.5. Let $v_X = v_Y = -0.7\,\text{V} = \text{logic 1}$.

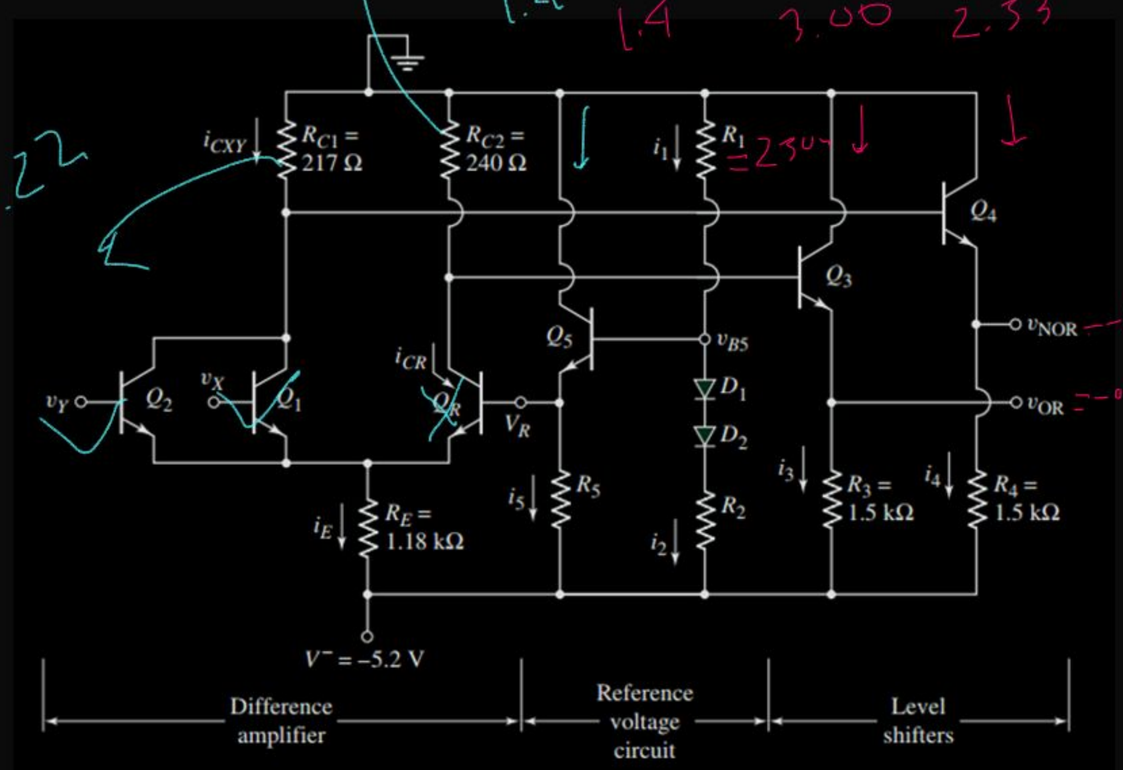


Figure 17.5 Basic ECL logic gate with reference circuit

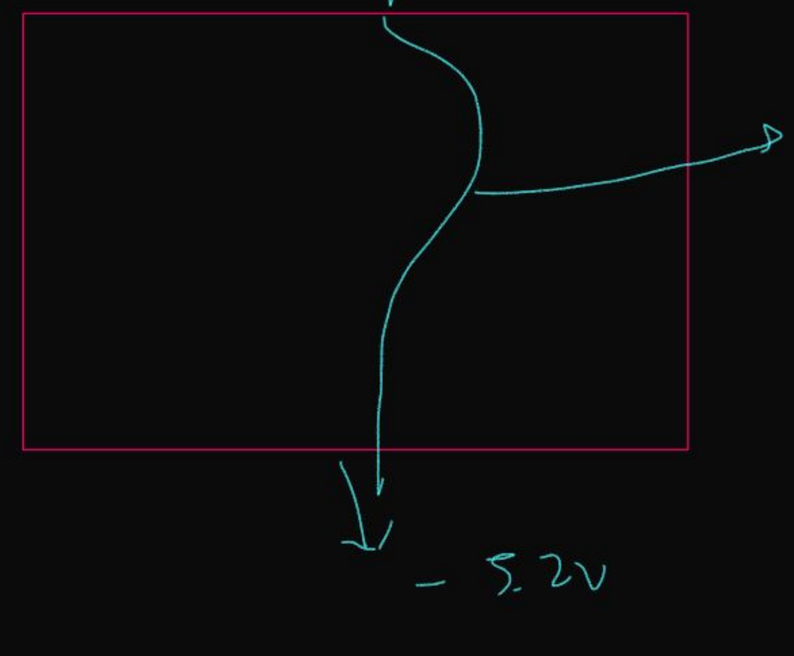
$v_{OR} = -0.7\,\text{V}$

$v_{NOR} = -1.4\,\text{V}$

$$i_4 = \frac{-1.4 - (-5.2)}{1.5\,\text{k}\Omega}$$

$$i_4 \cong 2.53\,\text{mA}$$

$$i_3 = \frac{-0.7 - (-5.2)}{1.5\,\text{k}\Omega} = 3\,\text{mA}$$



$P = \Delta V \times I$

$= [0 - (-5.2)] \times 11.53\,\text{mW}$

$= 60.06\,\text{mW}$

Lecture 10 Part 4

Friday, July 9, 2021 3:08 AM

17.5

Calculate the maximum fanout of an ECL logic gate, based on dc loading effects.

Consider the circuit in Figure 17.6. Assume the current gain of the transistors is β = 50, which represents a worst-case scenario. Assume that the logic 1 level at the

- **OR output is allowed to decrease by 50 mV at most from a value of −0.70 V to −0.75 V.**

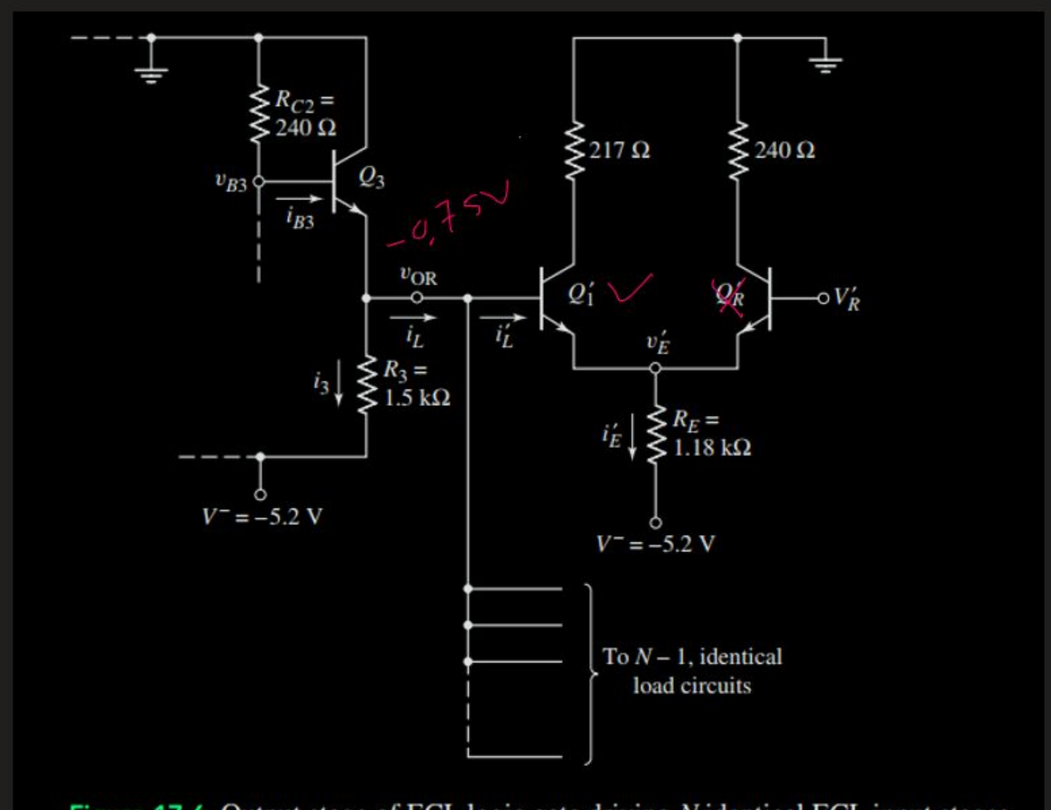


Figure 17.6 Output stage of ECL logic gate driving N identical ECL input stages

$v_{B1} = -0.75\ V$

$V_{E'} = (-0.75 - 0.7)\ V$

$= -1.45\ V$

$i_{E'} = \dfrac{-1.45 - (-5.2)}{1.18K} = 3.18\ mA$

$i_{B1}' = i_2' = \dfrac{i_E'}{(\beta+1)}$

Standard load current = $\Rightarrow i_2' = 62.35\ \mu A$

$v_{B3} = -0.05\ V$

$i_{B3} = \dfrac{0 - (-0.05)}{240\Omega} = 0.2083\ mA$

$i_{E3} = (\beta+1)\, i_{B3}$

$= \{51 \times 0.2083\}\ mA$

$= 10.625\ mA$

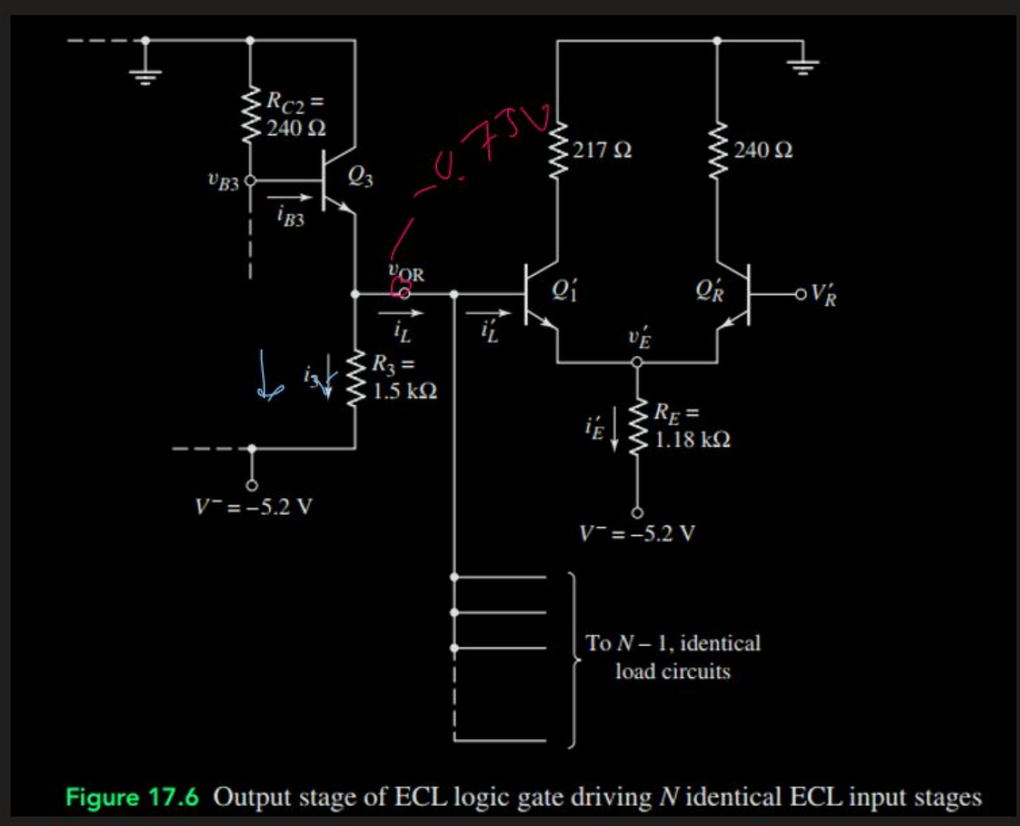


Figure 17.6 Output stage of ECL logic gate driving N identical ECL input stages

$i_{E3} = 13 + N \times i_L'$

$= \dfrac{-0.75 - (-5.2)}{1.5K} + N \times 62.35\ \mu A$

$10.625\ mA = 2.967\ mA + N \times 62.35\ \mu A$

$N = 122.82$

$\lfloor N \rfloor = 122$