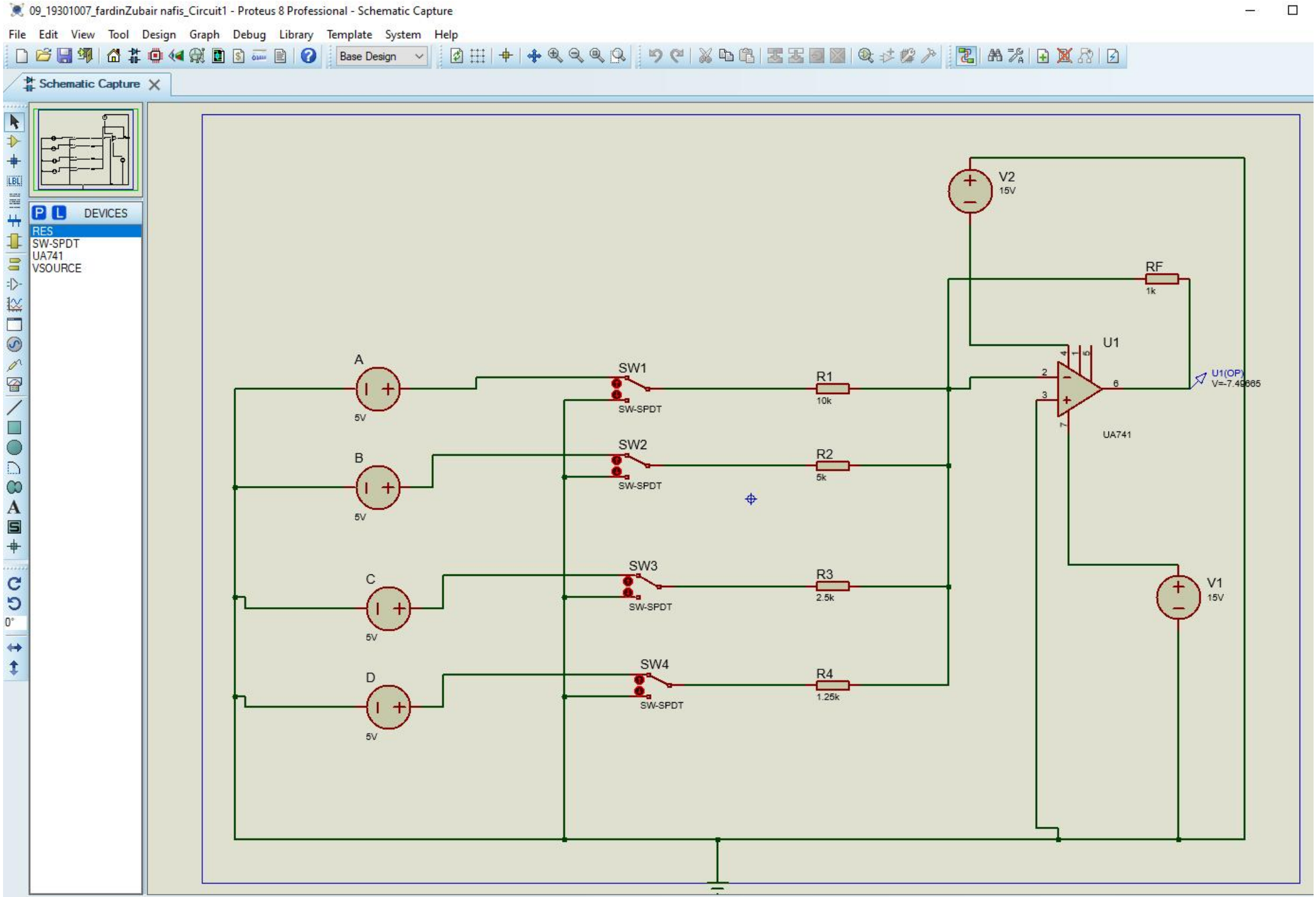
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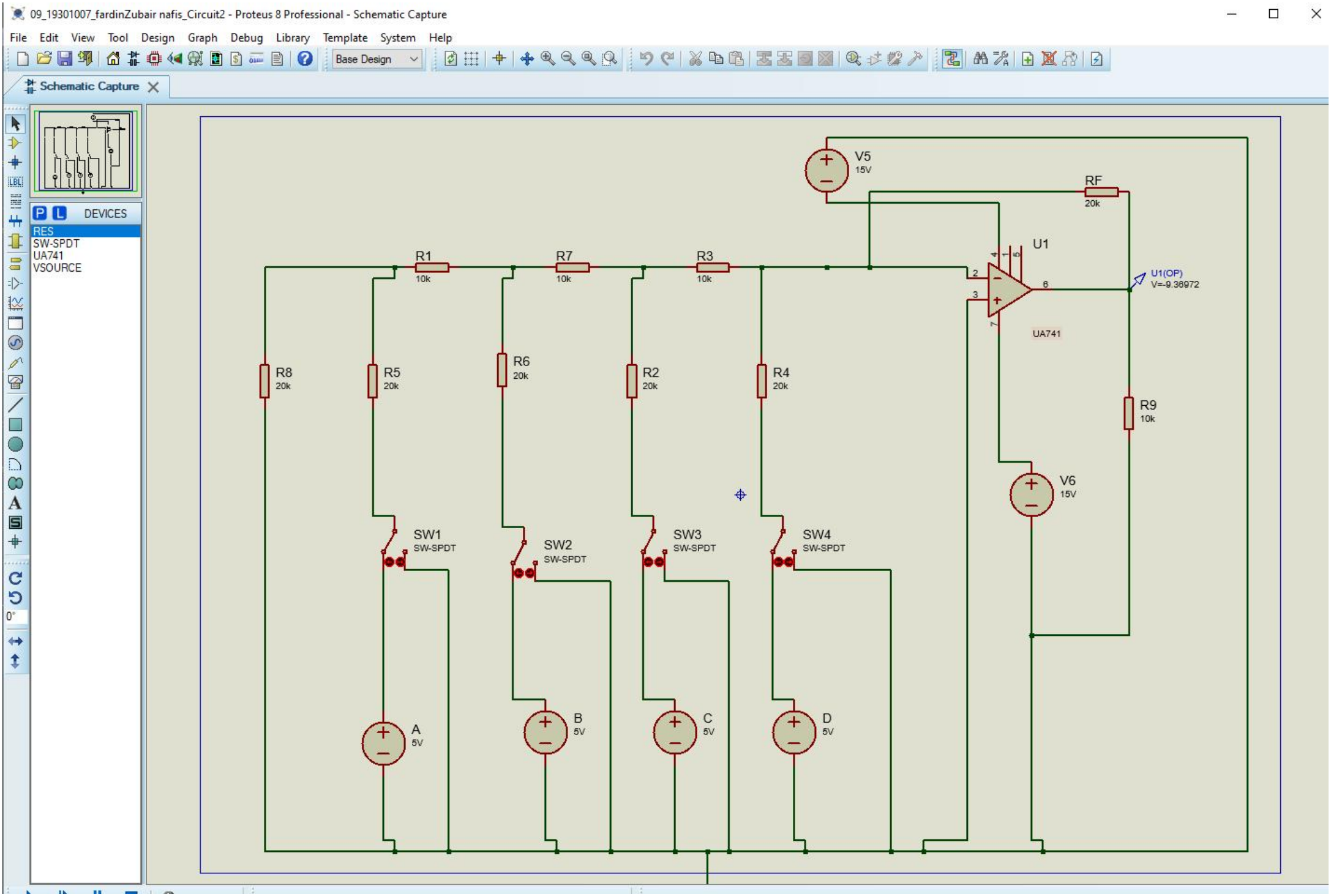
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
RES
SW-SPDT
UA741
VSOURCE
A
B
C
D
5V
SW1
SW2
SW3
SW4
SW-SPDT
R1
10k
R2
5k
R3
2.5k
R4
1.25k
RF
1k
U1
UA741
U1(OP)
V=-7.49665
V2
15V
V1
15V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Base Design
Schematic Capture
DEVICES
RES
SW-SPDT
UA741
VSOURCE
V5
15V
RF
20k
U1
UA741
U1(OP)
V=-9.36972
R1
10k
R7
10k
R3
10k
R8
20k
R5
20k
R6
20k
R2
20k
R4
20k
R9
10k
V6
15V
SW1
SW-SPDT
SW2
SW-SPDT
SW3
SW-SPDT
SW4
SW-SPDT
A
5V
B
5V
C
5V
D
5V

Kh. Fardin Zubaira Nafis
1930100 7 { Sec.: 09 } { Lab: 04 } CSE-330.

Circuit 01

Input Configuration	D	C	B	A	output (Vo)
1	0	0	0	0	= 0.0027
2	0	0	0	5	- = 0.497
3	0	0	5	0	- = 0.997
4	0	0	5	5	- = 1.497
5	0	5	0	0	- = 1.997
6	0	5	0	5	- = 2.497
7	0	5	5	0	- = 2.997
8	0	5	5	5	- = 3.497
9	5	0	0	0	- = 3.997
10	5	0	0	5	- = 4.497
11	5	0	5	0	- = 4.997
12	5	0	5	5	- = 5.497
13	5	5	0	0	- = 5.997
14	5	5	0	5	- = 6.497
15	5	5	5	0	- = 6.997
16	5	5	5	5	- = 7.497

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Circuit 02

Input voltage corresponding to the	D	C	B	A	Output voltage (V_o)
1	0	0	0	0	+0.0049
2	0	0	0	5	-0.620
3	0	0	5	0	-1.245
4	0	0	5	5	-1.869
5	0	5	0	0	-2.493
6	0	5	0	5	-3.119
7	0	5	5	0	-3.744
8	0	5	5	5	-4.369
9	5	0	0	0	-4.9948
10	5	0	0	5	-5.619
11	5	0	5	0	-6.244
12	5	0	5	5	-6.869
13	5	5	0	0	-7.494
14	5	5	0	5	-8.1198
15	5	5	5	0	-8.744
16	5	5	5	5	-9.369

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Report:

① In both circuit of D2A converter, we can not get the higher output less than 15V and a higher than 15V. Because, in both circuit of D2A converter, −15V and +15V are bias voltage and so output will be between them.

② for both D2A converter.

∵ input is 4 bits; ∴ full step output $= 2^4 - 1$

$= 15$ steps.

Binary weighted resistor:

Step size = −0.497
full scale = −7.497

$\therefore$ resolution $= \frac{-0.497}{-0.7.494}$

$= 0.0663$ V

R/2R D2A:

step size = −0.62
full scale = −9.369

resolution $= \frac{-0.62}{-9.369}$

$= 0.0661$ V

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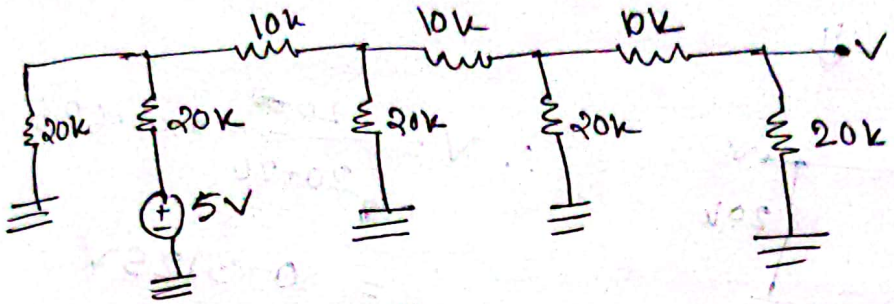
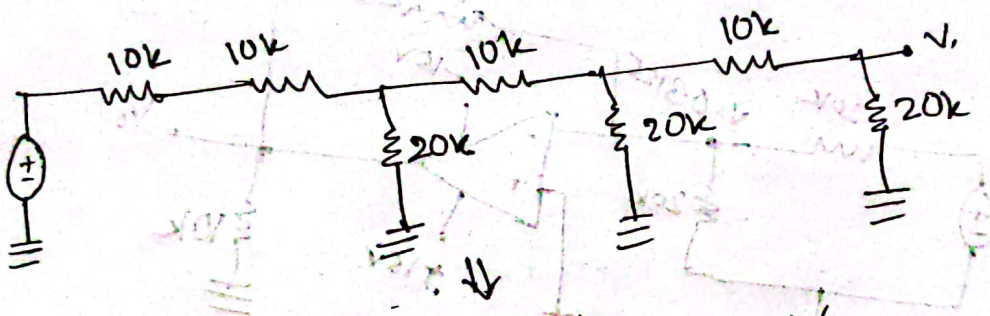
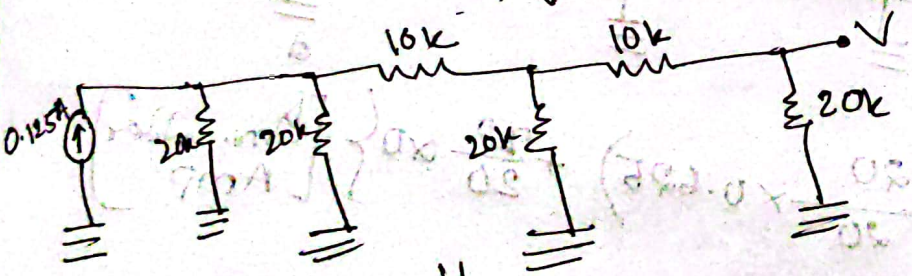
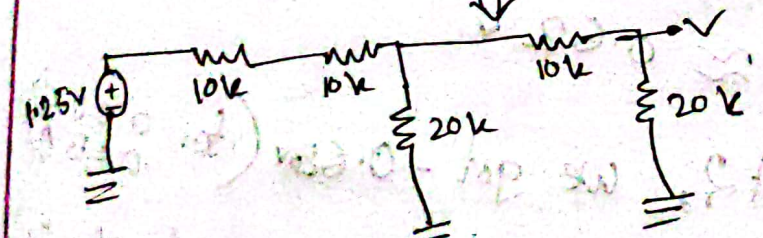
(3) if we choose, 0005 - ; where A is 5V (high)
DCBA
B, C, D is (low) 0V.

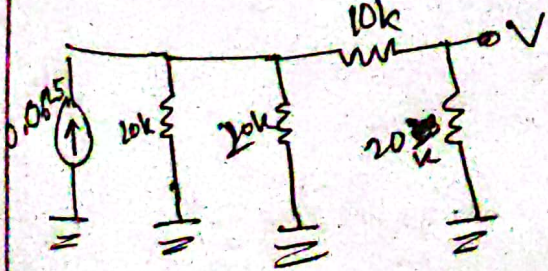
Applying source transformation in this circuit,











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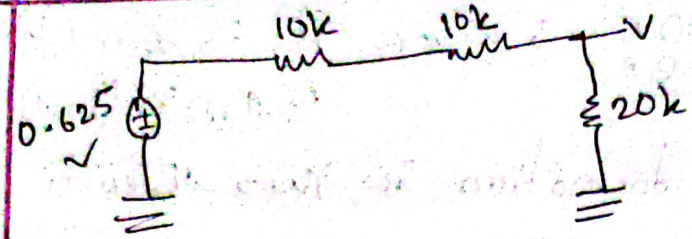
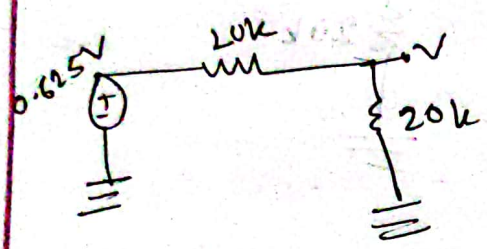
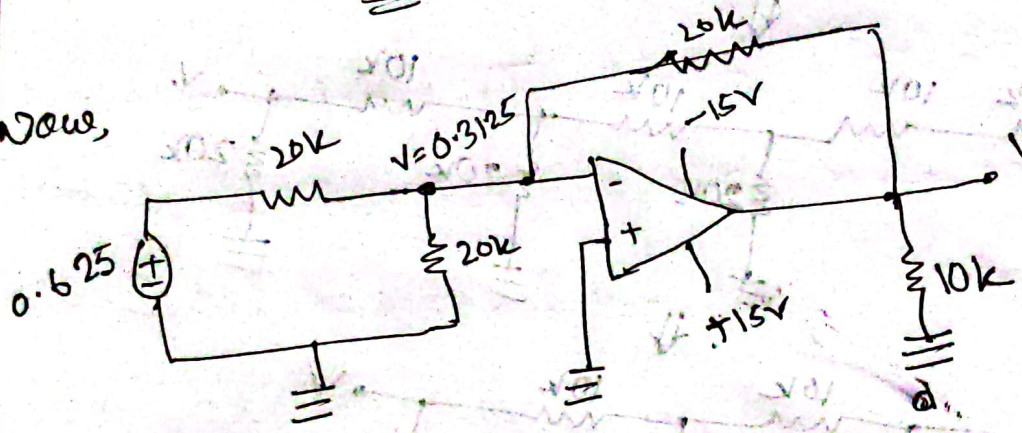




$$\therefore V = \frac{20}{20+20} \times 0.625$$

$$= 0.3125\,V$$

Now,



$$\therefore V_o = -\left\{\left(\frac{20}{20} \times 0.625\right) + \frac{20}{20} \times 0\right\}$$ [Inv. adder Amp]

$$= -0.625 \simeq 0.62\,V$$

from, proteus, circuit 2, we got -0.62V (for 0.005; 0 < B < A) and from calculation, we got -0.625 which is almost same.

for Circuit 01

19301007

④ Last 2 digit of ID = 07 = 0+7 = 7v = High

Low = 0V.

Input Configuration	D	C	B	A	Output V_o
1	0	0	0	0	0.002 7
2	0	0	0	1	−0.697
3	0	0	1	0	−1.397
4	0	0	1	1	−2.097
5	0	1	0	0	−2.797
6	0	1	0	1	−3.497
7	0	1	1	0	−4.197
8	0	1	1	1	−4.897
9	1	0	0	0	−5.596
10	1	0	0	1	−6.297
11	1	0	1	0	−6.997
12	1	0	1	1	−7.697
13	1	1	0	0	−8.397
14	1	1	0	1	−9.097
15	1	1	1	0	−9.796
16	1	1	1	1	−10.496

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⑤ when, RF = 1kΩ; Input for 0000 ⇒ $V_0 = 0.0027$ V

" " 0001 ⇒ $V_0 = -0.4097$ V

∴ step size = $-0.4097 \simeq 0.5$ V

when, RF = 3kΩ, input for 0000 ⇒ $V_0 = 0.006$ V

input " 0001 ⇒ $V_1 = -1.49$ V

∴ step size = $-1.49 \simeq 1.5$ V

So, if we increas RF 3 times, step size also increase 3 times. So, if RF increases, then step size also increases.

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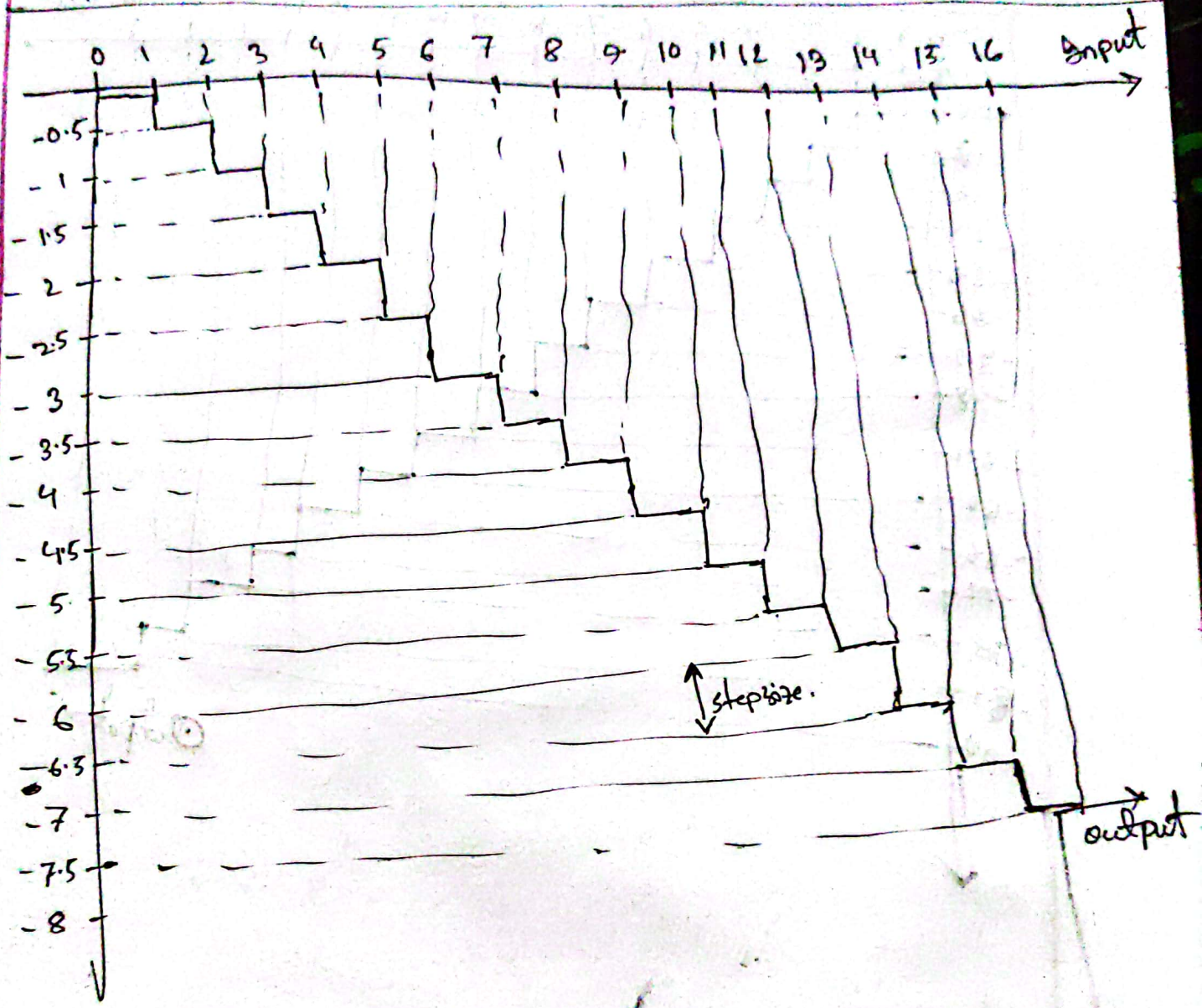
Input-output graph for Binary weighted Resistor D2A



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Input-output graph for R2R-D2A