CSE 350 Lab Report-2

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Sec : 12.

1.

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Experiment No.2:

Implementing a DTL logic gate.

Table-1

In A	In B	V_{DD}	V_{DD}	V_P	I_{R_1}	I_{R_2}	V_B	output Y
0	0	0.66	0.66	0.66	0.0025	1.723×10^{-11}	0.515	5
0	5	0.68	-4.32	0.678	0.0024	1.722×10^{-11}	0.498	5
5	0	-4.32	0.68	0.678	0.0024	1.722×10^{-11}	0.498	5
5	5	-2.83	-2.83	2.1674	0.001	0.002	0.891	0

Table-2

Input A	Input B	V_P	V_B	output Y
5	0	0.678	0.498	5
5	5	2.1674	0.891	0

Report

(1)

When one of the input is HIGH and other one is LOW, Q1 is in CUT OFF mode.

Lets assume input A is low and Input B is high,

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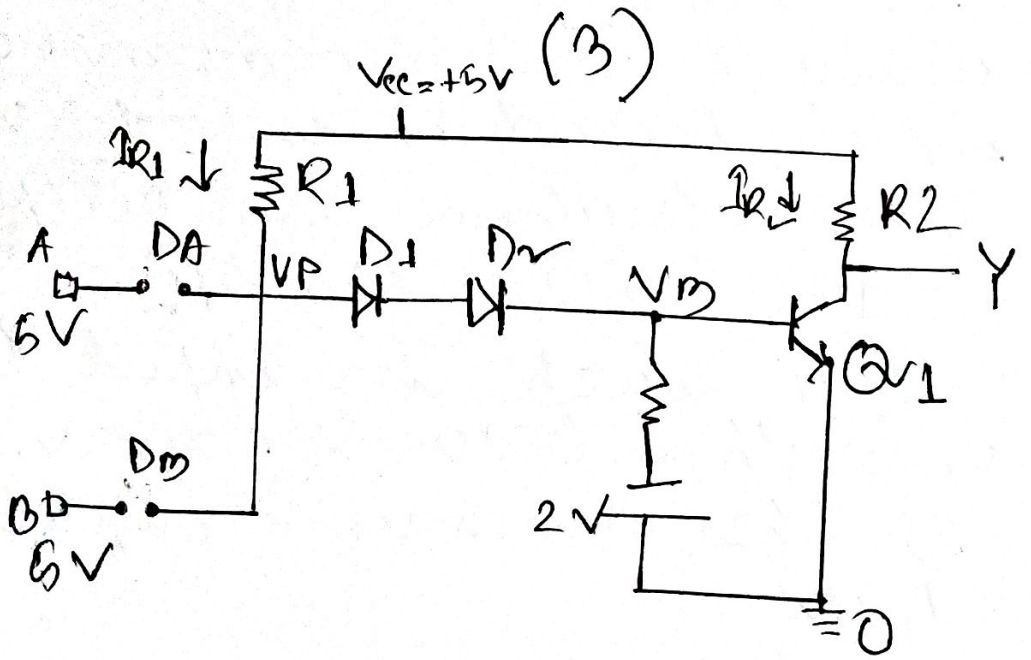
In this situation, D_A will be "on" and D_B will be "off."

(2).

In NAND operation when both the Inputs are high, we get a low output. On every other case, the output will be high.

In this circuit, input A and B are connected to reversed D_A and D_B which is acting as an ~~xx~~ AND gate. The ~~input~~ output of that AND gate is fed into the RTL inverter where it gets inverted, thus NAND is performed.

(3)



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(4)

Here we fixed A as logical high. when input B is low the output is high. And when B is high, the output is low. So here, a NOT operation is taking place.

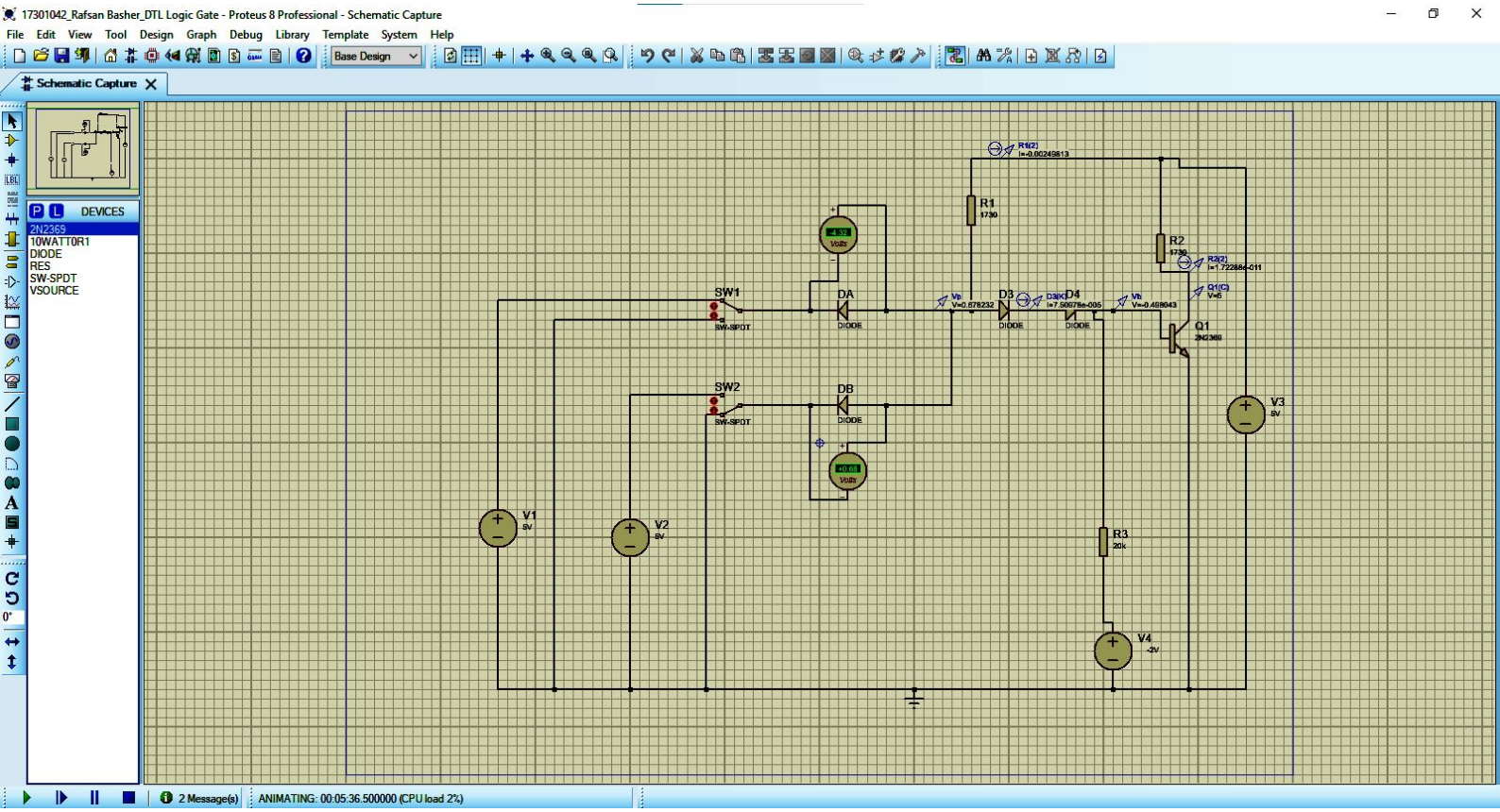
When A is high, in this circuit, A will be on cutoff mode. So. the output will depend on input B And because of that, when B is low output is high and B is high output is low.

(5)

According to my proteus simulation the minimum value of input A and B are 1.3 V. in this situation the output is = 0.138 which is low.

If I switch the input to 1.2 V, output becomes 3.842 V.

So, the minimum input is = 1.3 V.


17301042_Rafsan Basher_DTL Logic Gate - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
2N2369
10WATT0R1
DIODE
RES
SW-SPDT
VSOURCE
R1
1730
R2
1730
R3
20k
SW1
SW-SPDT
SW2
SW-SPDT
DA
DIODE
DB
DIODE
D3
DIODE
D4
DIODE
Q1
2N2369
V1
5V
V2
5V
V3
5V
V4
-2V
2 Message(s)
ANIMATING: 00:05:36.500000 (CPU load 2%)