BRAC UNIVERSITY

Department of Electrical and Electronic Engineering

CSE350: Digital Electronics and Pulse Techniques

Experiment No: 2

Implementing a DTL logic gate

Objective

1. Construct a DTL logic gate.
2. Understand the circuit operation.

Circuit Diagram

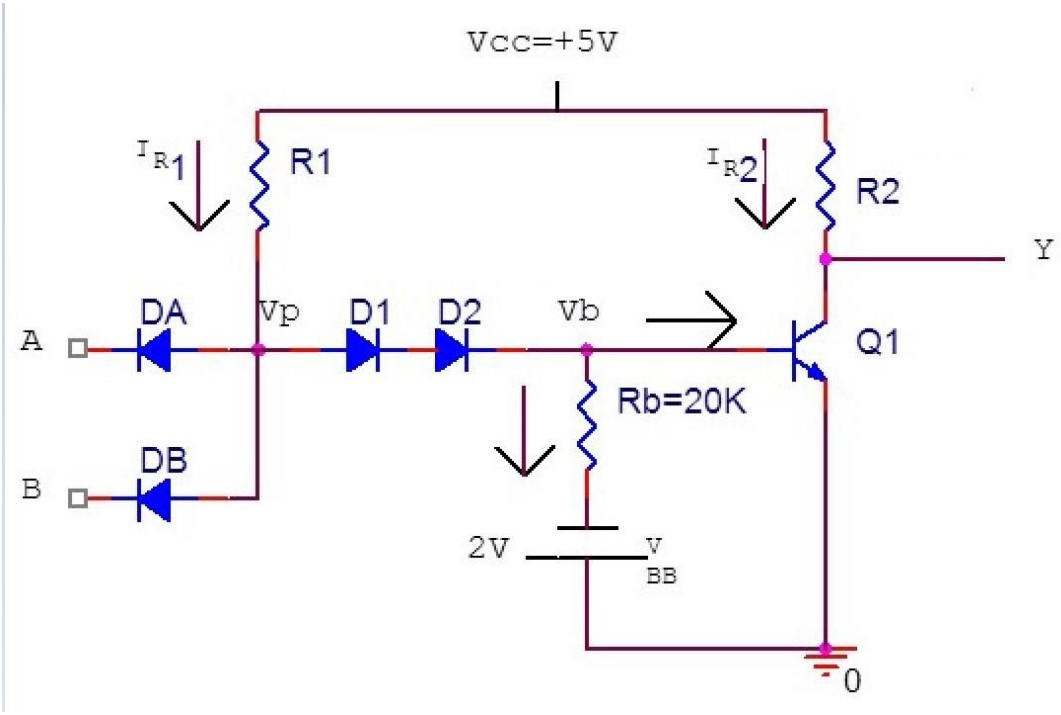

Fig: 1

Laboratory tasks

1. Connect the circuit as shown in Fig: 1 assuming that the values of R1 and R2 = XXXX where XXXX are the first 4 digits of your student ID (in ohms). 2.

   Observe the output for all possible inputs

3. Fill up the following table.

Input A	Input B	V_{DA}	V_{DB}	V_P	I_{R1}	Ir2	Vb	Output Y
0	0							
0	5							
5	0							
5	5							

4. Operate the gate in Fig 1 as an inverter by connecting either of the inputs to +5V and using the remaining one as input terminal. Fill up the following table.

Input A	Input B	V_P	Vb	Output Y
5	0			
5	5			

Report

1. Using proteus data Find the operation mode of Q1 when one of the inputs is **HIGH** and other one is **LOW**. Additionally, find whether diodes DA and DB are ON or OFF.
2. Explain briefly how NAND operation is performed in the circuit.
3. Assume that the output of the circuit shown in Fig: 1 is **LOW**. Draw the partial circuit consisting of only those components which remain active.
4. Explain the logic operation in the table 2 (Laboratory task step 4). How did you reach that logic operation from NAND operation of figure 1?
5. What is the minimum value of inputs A,B to keep the output LOW? (use simulation data) (assume any output value greater than 1v is not LOW)

General guidelines:

1. Submit the lab report of experiment 2 within due date.
2. Submit your own report.
3. cheating or unfair means may cause **0 in the lab report** and in the extreme case **expulsion from BRACU.**

What will Lab Assignment includes:

1. Lab assignments must be individual.
2. Lab assignments must be handwritten.
3. you need to upload the Doc/PDF of the lab assignment in the designated box in the google form.
4. you can convert the file to pdf using microsoft office or other software.
5. You also have to upload the simulation files **(.pdsprj)** files in designated box in the google form
6. Lab assignment will include screenshot of the circuits from Proteus software, data table taking the data from Proteus and the questions in the report section given in the lab sheet.
7. **You must attach the screenshot of the schematic from Proteus software that will include the components and project name used for that particular circuit. project name will be in this format: ID_name_circuit1 or ID_name_circuit2. you must follow this rule.**
8. Attach a cover page that will include your name and section.