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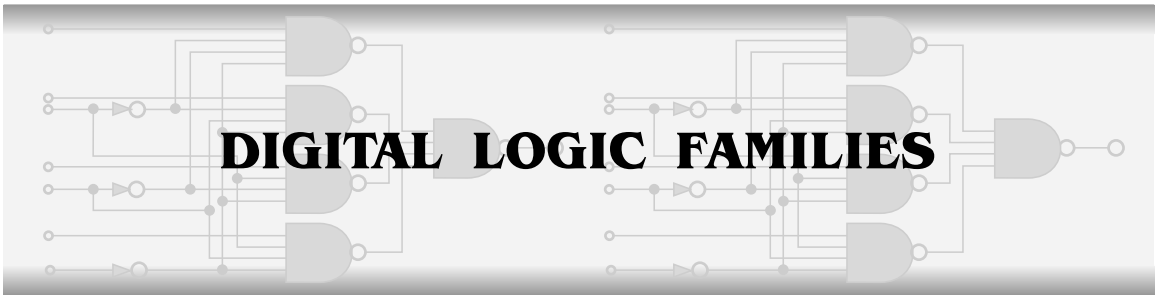

DIGITAL LOGIC FAMILIES

4.1 INTRODUCTION

The switching characteristics of semiconductor devices have been discussed in Chapter 3. Basically, there are two types of semiconductor devices: bipolar and unipolar. Based on these devices, digital integrated circuits have been made which are commercially available. Various digital functions are being fabricated in a variety of forms using bipolar and unipolar technologies. A group of compatible ICs with the same logic levels and supply voltages for performing various logic functions have been fabricated using a specific circuit configuration which is referred to as a *logic family*.

4.1.1 Bipolar Logic Families

The main elements of a bipolar IC are resistors, diodes (which are also capacitors) and transistors. Basically, there are two types of operations in bipolar ICs:

1. Saturated, and
2. Non-saturated.

In saturated logic, the transistors in the IC are driven to saturation, whereas in the case of non-saturated logic, the transistors are not driven into saturation.

The saturated bipolar logic families are:

1. Resistor–transistor logic (RTL),
2. Direct–coupled transistor logic (DCTL),
3. Integrated–injection logic (I^2L),
4. Diode–transistor logic (DTL),
5. High–threshold logic (HTL), and
6. Transistor-transistor logic (TTL).

The non-saturated bipolar logic families are:

1. Schottky TTL, and
2. Emitter-coupled logic (ECL).

4.1.2 Unipolar Logic Families

MOS devices are unipolar devices and only MOSFETs are employed in MOS logic circuits. The MOS logic families are:

1. PMOS,
2. NMOS, and
3. CMOS

While in PMOS only *p*-channel MOSFETs are used and in NMOS only *n*-channel MOSFETs are used, in complementary MOS (CMOS), both *p*- and *n*-channel MOSFETs are employed and are fabricated on the same silicon chip.

All the above logic families are discussed in this chapter.

4.2 CHARACTERISTICS OF DIGITAL ICs

With the widespread use of ICs in digital systems and with the development of various technologies for the fabrication of ICs, it has become necessary to be familiar with the characteristics of IC logic families and their relative advantages and disadvantages. Digital ICs are classified either according to the complexity of the circuit, as the relative number of individual basic gates (2-input NAND gates) it would require to build the circuit to accomplish the same logic function or the number of components fabricated on the chip. The classification of digital ICs is given in Table 4.1.

Table 4.1 Classification of digital ICs

IC Classification	*Equivalent individual basic gates*	*Number of components*
Small-scale integration (SSI)	Less than 12	Up to 99
Medium-scale integration (MSI)	12–99	100–999
Large-scale integration (LSI)	100–999	1,000–9,999
Very large-scale integration (VLSI)	Above 1,000	Above 10,000

The various characteristics of digital ICs used to compare their performances are:

1. Speed of operation,
2. Power dissipation,
3. Figure of merit,
4. Fan-out,
5. Current and voltage parameters,
6. Noise immunity,
7. Operating temperature range,
8. Power supply requirements, and
9. Flexibilities available.

4.2.1 Speed of Operation

The speed of a digital circuit is specified in terms of the propagation delay time. The input and output waveforms of a logic gate are shown in Fig. 4.1. The delay times are measured between the 50 per cent voltage levels of input and output waveforms. There are two delay times: $t_{p\text{HL}}$, when the output goes from the HIGH state to the LOW state and $t_{p\text{LH}}$, corresponding to the output making a transition from the LOW state to the HIGH state. The propagation delay time of the logic gate is taken as the average of these two delay times.

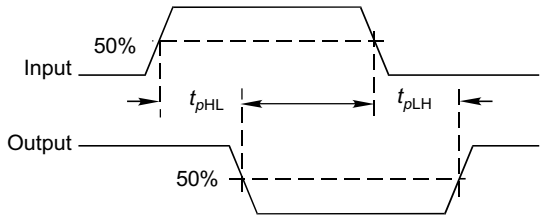

Fig. 4.1
Input and output voltage waveforms to define propagation delay times.

4.2.2 Power Dissipation

This is the amount of power dissipated in an IC. It is determined by the current, I_{CC}, that it draws from the V_{CC} supply, and is given by $V_{CC} \times I_{CC}$. I_{CC} is the average value of $I_{CC}(0)$ and $I_{CC}(1)$. This power is specified in milliwatts.

4.2.3 Figure of Merit

The figure of merit of a digital IC is defined as the product of speed and power. The speed is specified in terms of propagation delay time expressed in nanoseconds.

Figure of merit = propagation delay time (ns) × power (mW)

It is specified in pico joules ($ns \times \text{mW} = \text{pJ}$)

A low value of speed-power product is desirable. In a digital circuit, if it is desired to have high speed, i.e. low propagation delay, then there is a corresponding increase in the power dissipation and vice-versa.

4.2.4 Fan-Out

This is the number of similar gates which can be driven by a gate. High fan-out is advantageous because it reduces the need for additional drivers to drive more gates.

4.2.5 Current and Voltage Parameters

The following currents and voltages are specified which are very useful in the design of digital systems.

High-level input voltage, V_{IH}: This is the minimum input voltage which is recognized by the gate as logic 1.

Low-level input voltage, V_{IL}: This is the maximum input voltage which is recognized by the gate as logic 0.

High-level output voltage, V_{OH}: This is the minimum voltage available at the output corresponding to logic 1.

Low-level output voltage, V_{OL}: This is the maximum voltage available at the output corresponding to logic 0.

High-level input current, I_{IH}: This is the minimum current which must be supplied by a driving source corresponding to 1 level voltage.

Low-level input current, I_{IL}: This is the minimum current which must be supplied by a driving source corresponding to 0 level voltage.

High-level output current, I_{OH}: This is the maximum current which the gate can sink in 1 level.

Low-level output current, I_{OL}: This is the maximum current which the gate can sink in 0 level.

High-level supply current, I_{CC} (1): This is the supply current when the output of the gate is at logic 1.

Low-level supply current, I_{CC} (0): This is the supply current when the output of the gate is at logic (0).

The current directions are illustrated in Fig. 4.2.

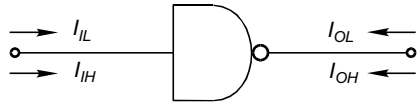

Fig. 4.2
A gate with current directions marked.

4.2.6 Noise Immunity

The input and output voltage levels defined above are shown in Fig. 4.3. Stray electric and magnetic fields may induce unwanted voltages, known as *noise*, on the connecting wires between logic circuits. This may cause the voltage at the input to a logic circuit to drop below V_{IH} or rise above V_{IL} and may produce undesired operation. The circuit's ability to tolerate noise signals is referred to as the *noise immunity*, a quantitative measure of which is called *noise margin*. Noise margins are illustrated in Fig. 4.3.

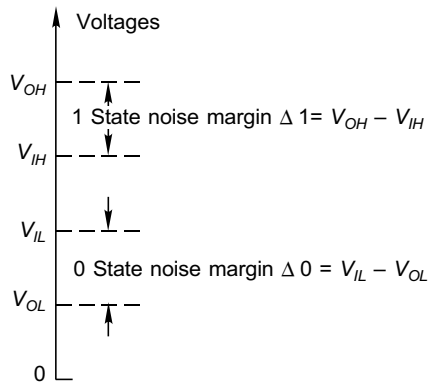

Fig. 4.3
Voltage levels and noise margins of ICs.

The noise margins defined above are referred to as *dc noise margins*. Strictly speaking, the noise is generally thought of as an a.c. signal with amplitude and pulse width. For high speed ICs, a pulse width of a few microseconds is extremely long in comparison to the propagation delay time of the circuit and therefore, may be treated as d.c. as far as the response of the logic circuit is concerned. As the noise pulse width decreases and approaches the propagation delay time of the circuit, the pulse duration is too short for the circuit to respond. Under this condition, a large pulse amplitude would be required to produce a change in the circuit output. This means that a logic circuit can effectively tolerate a large noise amplitude if the noise is of a very short duration. This is referred to as *ac noise margin* and is substantially greater than the dc noise margin. It is generally supplied by the manufacturers in the form of a curve between noise margin and noise pulse width.

4.2.7 Operating Temperature

The temperature range in which an IC functions properly must be known. The accepted temperature ranges are: 0 to + 70 °C for consumer and industrial applications and –55 °C to + 125 °C for military purposes.

4.2.8 Power Supply Requirements

The supply voltage(s) and the amount of power required by an IC are important characteristics required to choose the proper power supply.

4.2.9 Flexibilities Available

Various flexibilities are available in different IC logic families and these must be considered while selecting a logic family for a particular job. Some of the flexibilities available are:

1. *The breadth of the series:* Type of different logic functions available in the series.
2. *Popularity of the series:* The cost of manufacturing depends upon the number of ICs manufactured. When a large number of ICs of one type are manufactured, the cost per function will be very small and it will be easily available because of multiple sources.
3. *Wired-logic capability:* The outputs can be connected together to perform additional logic without any extra hardware.
4. *Availability of complement outputs:* This eliminates the need for additional inverters.
5. *Type of output:* Passive pull-up, active pull-up, open-collector/drain, and tristate. These will be explained in subsequent sections.

4.3 RESISTOR–TRANSISTOR LOGIC (RTL)

The resistor–transistor logic was the most popular form of logic in common use before the development of ICs. RTL circuits consist of resistors and transistors and was the earliest logic family to be integrated. Although RTL has become obsolete now, because of its simplicity and for historical reasons, it is proper to devote some attention to it and introduce some of the important concepts, useful for all types of gates, through this. The basic RTL gate is a NOR gate as shown in Fig. 4.4. For the sake of simplicity, a two-input NOR gate driving N similar gates is shown in the figure, which can be extended to accommodate a larger number of inputs. The number of input terminals is referred to as the *fan-in*.

4.3.1 Logic Operation

Inputs representing the logic levels are applied at A and B terminals. The voltage corresponding to LOW level should be low enough to drive the corresponding transistor to cut-off. Similarly, the input voltage corresponding to HIGH level should be high enough to drive the corresponding transistor to saturation.

If both the inputs are LOW, transistors T_1 and T_2 are cut-off and the output is HIGH. A HIGH level on any input will drive the corresponding transistor to saturation causing the output to go LOW. The LOW (0) level output voltage is $V_{CE,\text{sat}}$ of a transistor (~ 0.2 V) and the HIGH (1) level output voltage depends on the number of gates connected to the output. This causes the output voltage to be variable and is a deciding factor for the fan-out of the gate.

4.3.2 Loading Considerations

If all the inputs to the gate are LOW, the output is HIGH and if the gate is not driving any other gate, i.e. no load is connected, the output voltage will be slightly less than V_{CC} (there is voltage drop across the common collector resistor due to I_{CO} of T_1 and T_2).

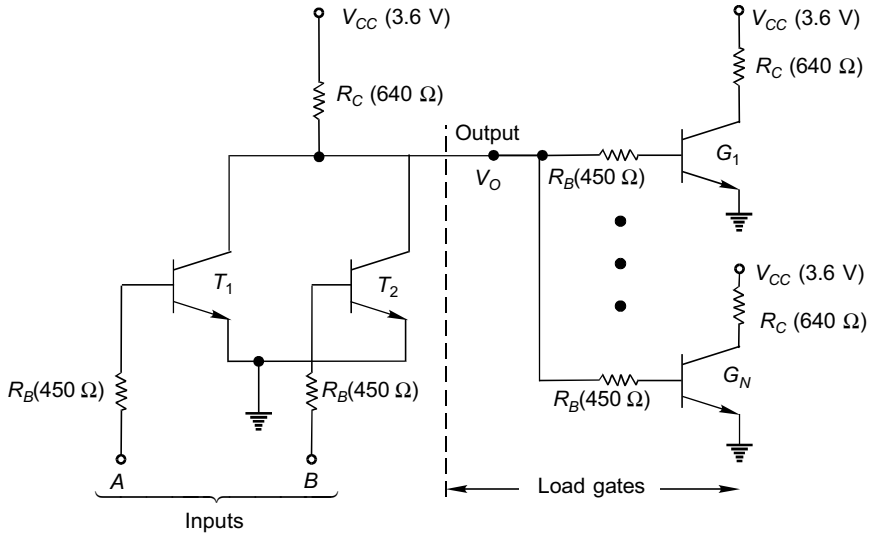

Fig. 4.4

A 2-input RTL NOR gate driving N similar gates.

When N similar gates are being driven, the load will be equivalent to a resistor of value $450/N$ ohms in series with a voltage source of 0.8 V (being the voltage between base and emitter of a transistor in saturation). The relevant portion of the circuit is shown in Fig. 4.5.
The base current for each load transistor is

$$I_B = \left(\frac{3.6 - 0.8}{640 + \frac{450}{N}} \right) \cdot \frac{1}{N} = \frac{2.8}{640N + 450} \qquad (4.1)$$

The collector current for the load transistor in saturation is

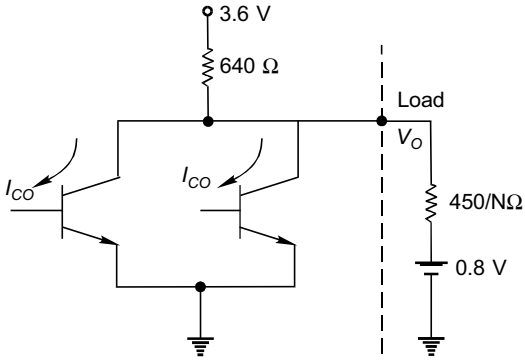

Fig. 4.5

A circuit illustrating the equivalent circuit at the input of the load gates.

$$I_{C,\text{sat}} = \frac{3.6 - 0.2}{640} = 5.31 \text{ mA} \qquad (4.2)$$

The value of N must satisfy the following relation,

$$h_{FE} \cdot I_B \geq I_{C,\text{sat}} \qquad (4.3)$$

For $N = 5$, $I_B = 0.767$ mA. Therefore, h_{FE} must be greater than 7.

4.3.3 Noise Margins

When the output is in 0 state $V_O = 0.2$ V. If this voltage becomes about 0.5 V (cut-in voltage of transistor), the load transistor comes to conduction which causes malfunction of the circuit. Hence, the logic 0 noise margin $\Delta 0 \approx 0.3$ V.

The logic 1 noise margin depends upon the number of gates being driven. For $N = 5$,

$$V_O = \frac{90}{90+640} \times (3.6) + \frac{640}{90+640} \times (0.8) = 1.14 \text{ V} \tag{4.4}$$

For $h_{FE} = 10$, the total base current required for load transistors to be driven into saturation will be $5 \times \left(\frac{5.31}{10}\right)$ mA and the corresponding V_O must be 1.04 V. Therefore, the noise margin for 1 level is $\Delta 1 = 1.14 - 1.04 = 0.1$ V.

4.3.4 Propagation Delay Time

The propagation delay time is also affected by the number of gates it drives. When the output of the gate is in LOW state all the load transistors are cut-off and the base–emitter junction of each of these transistors appears to be a capacitor, C. When the output has to change from LOW to HIGH level due to changes at the input, it will do so with a time constant given by

$$\left(640 + \frac{450}{N}\right) NC = (640N + 450)\ C \tag{4.5}$$

The resistance in the collector circuit pulls up the output voltage from LOW to HIGH level and hence is known as the *pull-up resistor*. It is passive pull-up in this case in contrast to an *active pull-up* which can be used to decrease the propagation delay time. Active pull-up will be discussed later.

4.3.5 Current Source Logic

The gate supplies current to the load transistors when in 1 level, whereas the leakage-current (reverse-saturation base current) of load transistors flow through T_1 or T_2 in 0 level. Since the source current is much greater than the sink current, it is known as *current source logic.*

4.3.6 Wired-Logic

If the outputs of the gates are connected together as shown in Fig. 4.6, the output Y is given by

$$\begin{aligned} Y &= Y_1 \cdot Y_2 \\ &= \overline{A+B} \cdot \overline{C+D} \\ &= \overline{A+B+C+D} \end{aligned}$$

This shows that fan-in can be increased by this connection which is referred to as *wired-*AND or *implied-*AND. The effect of this connection on fan-out, power dissipation and speed of operation can be seen in Prob. 4.3.

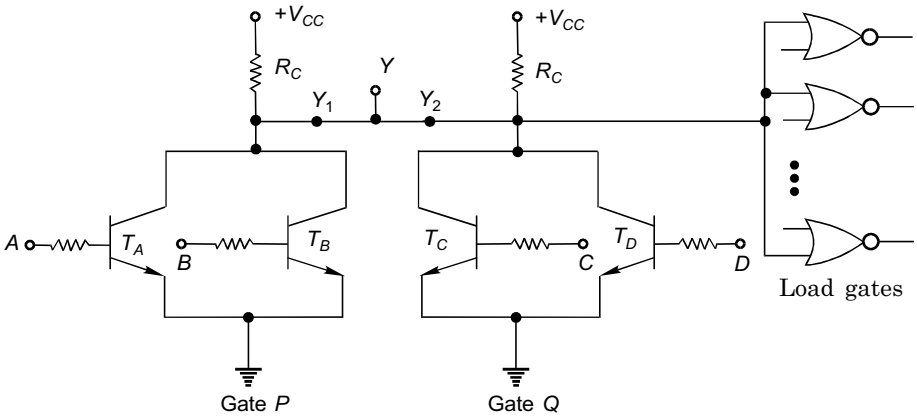

Fig. 4.6

Wired-AND connection of RTL gates driving similar gates

The characteristics of RTL can be summarized as: Poor noise margin, poor fan-out capabilities, low speed, and high power dissipation.

4.4 DIRECT-COUPLED TRANSISTOR LOGIC (DCTL)

In the RTL gate of Fig. 4.4, if the base resistors R_B are omitted, we obtain what is known as the direct-coupled transistor logic (DCTL) gate, in which the inputs are directly coupled to the bases. This circuit performs positive NOR logic and the voltages corresponding to logic 1 and 0 levels are $V_{BE,\text{sat}}$ (~ 0.8 V) and $V_{CE,\text{sat}}$ (~ 0.2 V) respectively. The separation between the logic 1 and 0 level voltages, which is referred to as the *logic swing*, is very small ($V_{BE,\text{sat}} - V_{CE,\text{sat}} =$ 0.6 V). Therefore, the noise margin of this circuit is very poor.

Although the DCTL is simpler than RTL, it never became popular because of the problem of *current hogging*. The gate should be able to drive the transistors of the load gates to saturation corresponding to logic level 1.

This does not pose any problem if all the transistors have same input characteristics but, unfortunately, the input characteristics differ due to the manufacturing tolerances of different IC packages operating at different temperatures. Owing to these differences, the saturation voltages of the load transistors may be different. Let the base–emitter voltages of the transistors corresponding to saturation be 0.78, 0.79, and 0.80 V. The transistor with the base–emitter voltage of 0.78 V, when it enters saturation, will not allow other transistors to enter saturation and will take whole of the current supplied from the driver gate. This is known as *current hogging*.

4.5 INTEGRATED-INJECTION LOGIC (I^2L)

As discussed above, the DCTL suffers from the difficulty of current hogging which makes it unsuitable. However, based on DCTL a new logic referred to as the integrated-injection logic

(I^2L), has been developed. I^2L has the simplicity of DCTL, uses very small silicon chip area, consumes very little power, and requires only four masks and two diffusions (compared to five masks and three diffusions for BJT) and hence, is easier and cheaper to fabricate. Due to these advantages it is eminently suited for medium- and large-scale integration. It is not used for small-scale integration and is the only saturated bipolar logic employed for large-scale integration. Texas Instruments SBP 9900 is a 16-bit microprocessor using I^2L technology.

The genesis of I^2L technology is the concept of merging the components, viz. one semiconductor region is part of two or more devices. Because of this type of merging it is also referred to as the *merged-transistor logic* (MTL). There is considerable saving in the silicon chip area in this process.

4.5.1 I^2L Inverter

The basic operation of I^2L is explained with the help of the inverter circuit shown in Fig. 4.7. If the input V_i is at LOW logic level ($V_i \approx 0$), T_1 is OFF so that $I_{B1} = 0$. The input source acts as a sink for the current I_1. Therefore, I_2 flows through the base of T_2 driving it to saturation. When T_1 is OFF and T_2 is ON, $V_{BE2} = V_{CE1} \approx 0.8$ V.

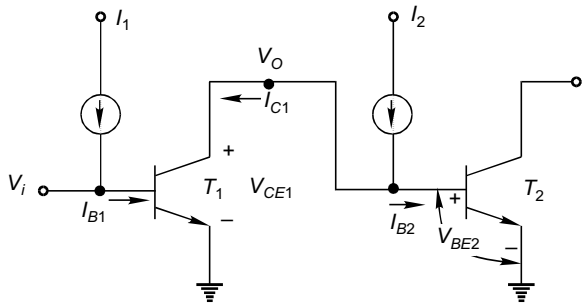

Fig. 4.7

An I^2L inverter directly coupled to the following stage.

On the other hand, if the input is at HIGH logic level ($V_1 \approx 0.8$ V), the base current I_{B1} will have two components, one of them being I_1 and the other is due to the source V_i, and consequently T_1 saturates. Therefore, $V_{CE1} = V_{CE,\text{sat}} \approx 0.2$ V, which drives T_2 to cut-off and T_1 acts as a sink for I_2. This shows that the logic level at V_O is complement to that of V_i, viz. T_1 acts as an inverter. The logic swing is about 0.6 V.

4.5.2 I^2L Configuration

Consider the DCTL gate structure shown in Fig. 4.8 in which there are two logical variables which are assumed to be outputs of similar DCTL gates and we need to generate the functions

$\overline{A+B}, \overline{A+\bar{B}}, \overline{\bar{A}+B}$, and $\overline{\bar{A}+\bar{B}}$.

We observe from the figure that the bases of transistors T_1, T_2, and T_4 are connected together, also their emitters are connected together (grounded). Therefore, the combination of T_1, T_2, and T_4 can be replaced with single transistor having one base, one emitter and three

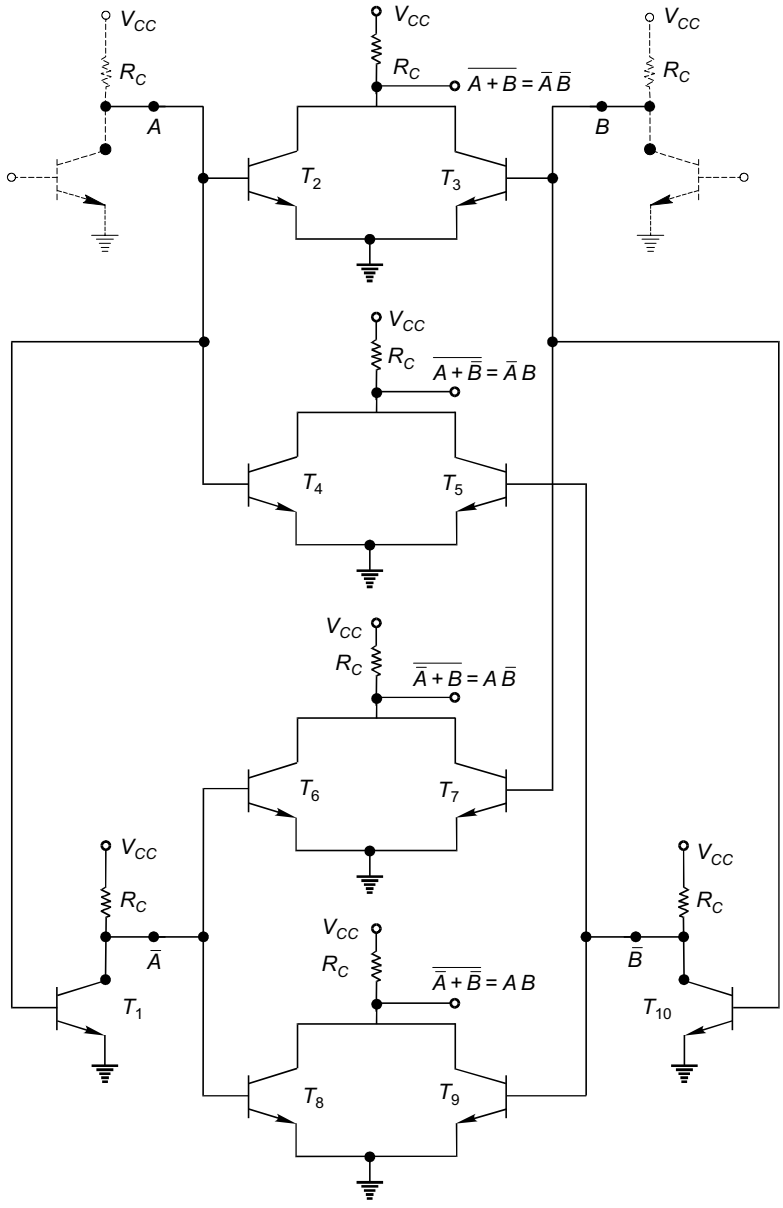

Fig. 4.8

A DCTL gate structure for generating functions of two logical variables.

collectors. Similarly, other transistors with common-bases are replaced with multiple-collector transistors. Using this concept, Fig. 4.8 is redrawn as shown in Fig. 4.9.

As shown in Fig. 4.7, a mechanism for supplying base currents is required. To achieve this, the collector resistors of driving gates (shown dotted in Fig. 4.8) are treated as the base resistors

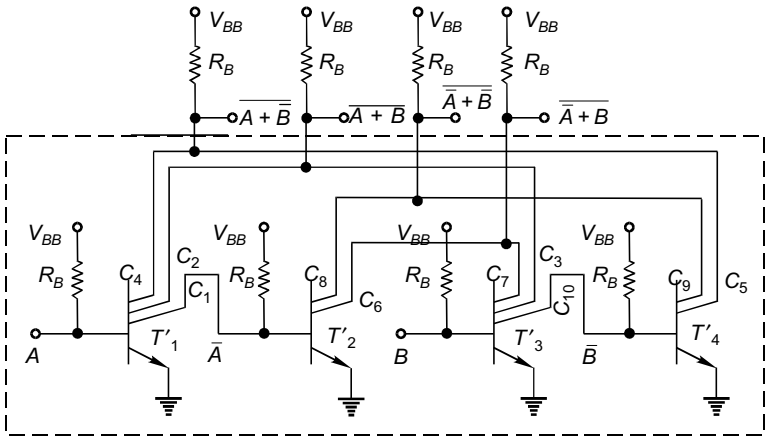

Fig. 4.9

Figure 4.8 redrawn with multiple-collector transistors.

of multiple-collector transistors (T'_1 and T'_3). Similarly, the collector resistors of T_1 and T_{10} are treated as the base resistors of T'_2 and T'_4, respectively. Correspondingly, the supply voltages are indicated as V_{BB}. The portion of the circuit shown outside the dotted box is either a part of other gates driven by the outputs shown or is omitted altogether. This means that an I^2L circuit has open-collector outputs, which either feed another I^2L circuit or are to be connected to the supply voltage through resistors. Suitable values of supply voltage and resistor are to be used for getting proper output voltage levels, for driving other gates such as TTL.

4.5.3 Fabrication of I^2L

The resistor R_B required to inject the base current would require a large silicon area if fabricated on the chip and thus, would render the circuit useless for LSI applications. It can be eliminated by replacing it with a current source. The grounded-base *p-n-p* transistor shown in Fig. 4.10 acts as a current source, which is referred to as a *current injector*. The resistor R_X is external to the chip and the current I_O is given by

$$I_O = \frac{V_{CC} - V_{EB}}{R_X} \tag{4.6}$$

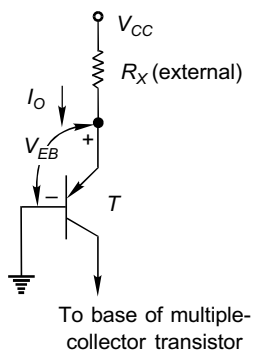

Fig. 4.10

A current injector for I^2L

The collector of the current injector transistor T of Fig. 4.10 and the base of the multiple-collector transistor are merged, viz. one *p* region serves both as collector of *p-n-p* transistor and base of *n-p-n* transistor. Similarly, the base of T is merged with the emitter of the multiple-collector transistor. A simplified physical structure of a portion of I^2L circuit is shown in Fig. 4.11. This shows the simplicity of I^2L structure.

The speed of operation of I^2L depends upon the charging current. The propagation delay time is inversely proportional to the charging current, also the power dissipation is proportional

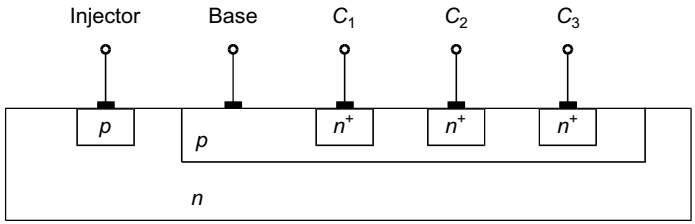

Fig. 4.11

The simplified physical structure of a portion of I^2L.

to the charging current, therefore we have to trade-off between power dissipation and speed. The figure of merit is independent of I_O and it is in the range of 0.1 to 0.7 p*J*. The silicon area required is very small and packing density in the range 120 to 200 gates per square millimetre have been realized.

4.6 DIODE–TRANSISTOR LOGIC (DTL)

The diode–transistor logic is somewhat more complex than RTL but because of its greater fan-out and improved noise margins it has replaced RTL. Its main disadvantage is slower speed and because of this it was modified and emerged as transistor– transistor logic (TTL) which is the most popular logic family today, as far as small- and medium-scale ICs are concerned. Although TTL has completely replaced DTL, for historical reasons as well as for better appreciation of TTL circuit, it is worthwhile discussing the details of DTL.

DTL circuit using discrete components was made using input diodes and a transistor inverter (NOT), which was modified for integrated circuit implementation as shown in Fig. 4.12.

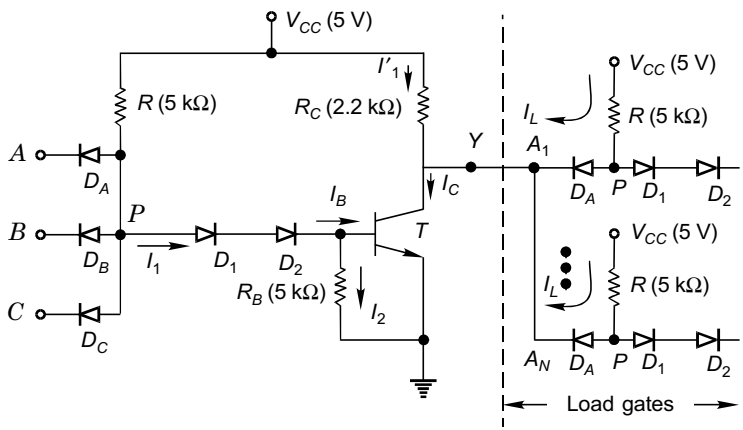

Fig. 4.12

A 3-input DTL NAND gate driving *N* similar gates.

4.6.1 Operation of DTL NAND Gate

The basic DTL gate is a NAND gate. A 3-input NAND gate driving N similar gates is shown in Fig. 4.12. The input diodes D_A, D_B, and D_C conduct through the resistor R, if the corresponding input is in the LOW state, while corresponding to HIGH state the diode is nonconducting. Therefore, if at least one of the inputs is LOW, the diode connected to this input conducts and the voltage V_P at point P is one diode drop above the low level voltage at the input. The voltage V_P should be such as to keep T in cut-off. Therefore, the output of T is V_{CC}. On the other hand, if all the three inputs are in HIGH state, the input diodes are cut-off and consequently current flowing from V_{CC} through R should be sufficient to drive T in saturation. Therefore, the output of T is $V_{CE,\text{sat}}$.

If we consider the voltages corresponding to logic 1 and 0 as V_{CC} and $V_{CE,\text{sat}}$ respectively, this circuit performs NAND operation. The following example illustrates the loading (fan-out) considerations and the noise-margins.

Example 4.1 For the DTL NAND gate of Fig. 4.12 calculate (*a*) fan-out (*b*) noise-margins, and (*c*) average power, *P*, dissipated by the gate. The diode and transistor parameters are:

Diode:	Voltage across a conducting diode	= 0.7 V
	Cut-in voltage V_γ	= 0.6 V
Transistor:	Cut-in voltage V_γ	= 0.5 V
	$V_{BE,\text{sat}}$	= 0.8 V
	$V_{CE,\text{sat}}$	= 0.2 V
	h_{FE}	= 30

Solution

(a) As discussed above, the logic levels are:

LOW level = $V(0) = V_{CE,\text{sat}} = 0.2$ V

HIGH level = $V(1) = V_{CC} = 5$ V

(*i*) If all the inputs are HIGH, the input diodes are reverse-biased. Assuming diodes D_1, D_2 to be conducting and T to be in saturation, the voltage $V_p = 0.7 + 0.7 + 0.8 = 2.2$ V.

Writing Kirchhoff's current law (KCL) equation at the base of T,

$$I_B = I_1 - I_2$$

where

$$I_1 = \frac{V_{CC} - V_P}{R} = \frac{5 - 2.2}{5} = 0.56 \text{ mA}$$

and

$$I_2 = \frac{V_{BE,\text{sat}}}{R_B} = \frac{0.8}{5} = 0.16 \text{ mA}$$

which gives a base current $I_B = 0.4$ mA. The collector current (without load gates connected) is

$$I_C = \frac{V_{CC} - V_{CE,\text{sat}}}{R_C} = \frac{5 - 0.2}{2.2} = 2.182 \text{ mA.}$$

Since $h_{FE} \times I_B = 30 \times 0.4 = 12$ mA is greater than I_C (2.182 mA), it is confirmed that the transistor is in saturation and the output is in LOW state. Now, if N load gates are fed from this gate, the input diodes of the driven gates will conduct through the output transistor T,

i.e. T acts as a sink for the current in the input to the gates it drives. Assuming that all the other inputs to each of the load gates are HIGH except the one driven by T, the current $I_L = \frac{V_{CC} - V_P}{R} = \frac{5 - 0.9}{5}$ = 0.82 mA. This current is referred to as *standard load*. The fan-out is given by I_C £ $h_{FE}\, I_B$, or 0.82 N + 2.182 ≤ 12 mA or N < 12 since N must be an integer. A conservative choice is N = 10. The Maximum collector current rating of T must be about 12 mA.

(ii) If at least one of the inputs is LOW, the corresponding input diode conducts and V_P = 0.2 + 0.7 = 0.9 V. The minimum voltage required for D_1, D_2, and T to be conducting is 0.6 + 0.6 + 0.5 = 1.7 V, which confirms that D_1, D_2 are nonconducting and hence T is cut-off. Consequently, the output voltage is V_{CC} (5 V) if the load gates are not connected.

If the load gates are connected, the input diodes of the load gates are nonconducting, which means the reverse-saturation current of these diodes must be supplied through the collector resistor R_C, which will produce a voltage drop across R_C and consequently the output voltage corresponding to HIGH state will be a little less than V_{CC}. The maximum current which can be supplied by the gate will depend upon V_{OH}. The fan-out is determined on the basis of maximum current.

(b) (*i*) If all the inputs are HIGH, the output is LOW. Since V_P = 2.2 V, the input diodes are reverse-biased by 5 – 2.2 = 2.8 V. Since the cut-in voltage of the diode is 0.6 V, a negative noise spike of at least 3.4 V present at the input will cause malfunction of the circuit, i.e. the 0 level noise margin Δ 0 = 3.4 V.

(*ii*) If at least one input is LOW, the output is HIGH. Since V_P = 0.9 V and a voltage of at least 1.7 V [part a (*ii*)] is required for D_1, D_2, and T to conduct, therefore a positive noise spike of at least 0.8 V will cause malfunction of the circuit, i.e. the 1 level noise margin Δ 1 = 0.8 V.

(c) The power $P(0)$ when the output is LOW is given by $P(0) = V_{CC}\,(I_1 + I'_1)$ = 5 (0.56 + 2.182) = 13.71 mW. When the output is in the HIGH state at least one of the input diodes conduct. Therefore, I_1 = 0.82 mA and I'_1 = 0. Hence $P(1)$ = (0.82) (5) = 4.1 mW.

If we assume that the occurrence of LOW and HIGH is equally likely then the average power is

$$P_{av} = \frac{P(0) + P(1)}{2} = \frac{13.71 + 4.1}{2} = 8.905 \text{ mW}$$

4.6.2 Propagation Delays

Delays are associated with the turning-on (*turn-on delay*) and the turning-off (*turn-off delay*) of the output transistor. While turning on, any capacitance shunting the output of the gate discharges rapidly through the low impedance of the output transistor in saturation. On the other hand, at turn-off the shunt capacitor must charge through the pull-up resistor R_C in addition to the storage time delay. The turn-off delay is considerably larger than the turn-on delay, often by a factor of 2 or 3. The propagation delay time of commercially available DTL gates are of the order of 30 to 80 ns.

4.6.3 Current Sink Logic

This gate supplies the reverse-saturation current of input diodes of the load gates in 1 state and sinks the current flowing through the forward-biased input diodes of the load gates in the

output transistor of the gate in 0 state. Since the sink current is much greater than the source current, this is known as *current sink logic.*

4.6.4 Wired-Logic

If the outputs of gates are connected together as shown in Fig. 4.13, additional logic is performed without additional hardware. This type of connection is referred to as *wired-logic*, *wired-*AND, or *implied-*AND.

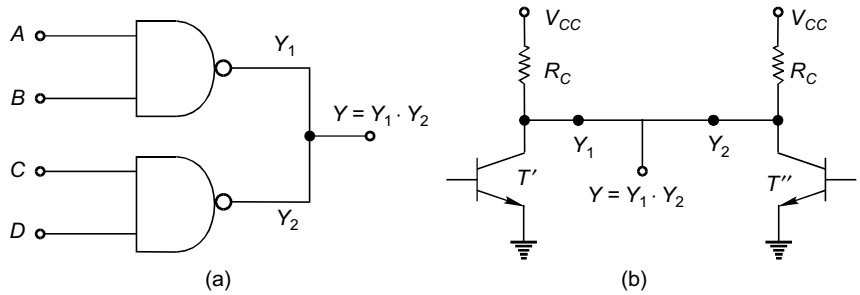

Fig. 4.13

The wired-AND connection of DTL gates

If $Y_1 = Y_2 = 1$, then $Y = 1$, whereas if any one (Y_1 or Y_2) or both are 0, then $Y = 0$. The output is

$$Y = Y_1\ Y_2 = (\overline{AB}) \cdot (\overline{CD}) = \overline{AB + CD} \tag{4.7}$$

Let us consider the effect of wired-AND connection on power dissipation, speed, and fan-out. The power dissipation in LOW output state $P(0)$ increases because of reduction in effective collector resistor ($R_C \parallel R_C = R_C/2$). Consequently, the speed of operation increases due to reduction in charging resistor ($R_C/2$).

There is an effective reduction in the fan-out of the gate in the wired-AND connection. If only one output transistor (say T') is conducting, then this transistor must not only sink the current of the load gates and the current due to its own pull-up resistor but must also sink the current in the pull-up resistor of the other output transistor T''. This situation makes it necessary to reduce the allowable fan-out of each gate in the wired-AND connection.

4.6.5 Modified Integrated DTL NAND Gate

From Ex. 4.1 we note that the fan-out may be increased by increasing the base current of the output transistor. This can be done by replacing D_1 by a transistor T_1, as illustrated in Fig. 4.14.

The circuit can be analysed in a similar way as in Ex. 4.1 (Prob. 4.9). Its fan-out is considerably higher than that of the circuit of Fig. 4.12.

4.7 HIGH-THRESHOLD LOGIC (HTL)

Due to the presence of electric motors, on–off control circuits, high voltage switches, etc. in an industrial environment, the noise level is quite high and the logic families discussed so far do

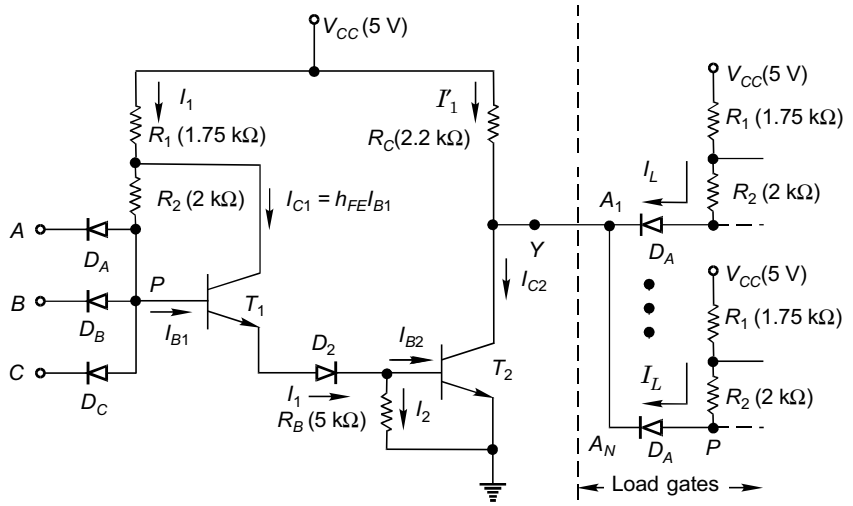

Fig. 4.14

A modified integrated 3-input DTL NAND gate driving N similar gates.

not perform the intended functions. For this purpose, the DTL gate of Fig. 4.14 has been redesigned with a higher supply voltage (15 V instead of 5 V). The diode D_2 has been replaced by a Zener diode with a Zener breakdown voltage of 6.9 V and the resistances have been modified so that approximately the same currents are obtained as in DTL. A 3-input HTL NAND gate with a fan-out of N is shown in Fig. 4.15. The circuit can be analysed to determine the noise-margins, fan-out and power dissipation (Prob. 4.10).

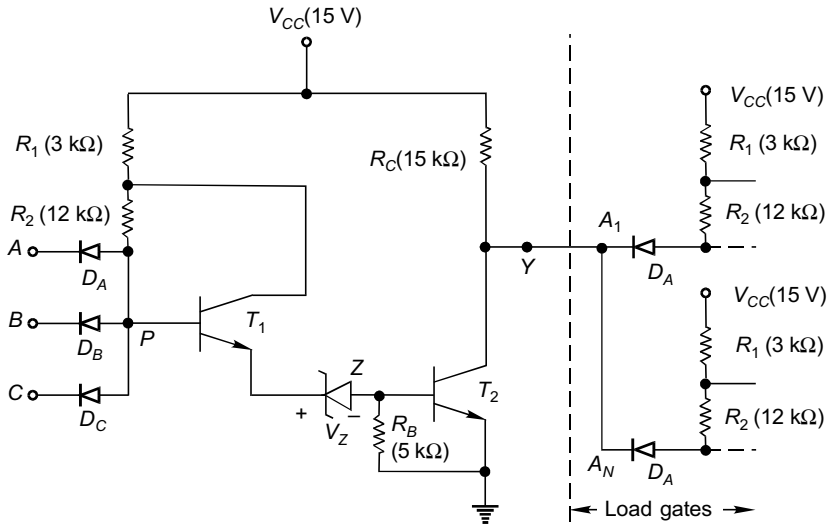

Fig. 4.15

A 3-input HTL NAND gate driving N similar gates.

The propagation delay time is adversely affected due to large resistance values. It is as high as hundreds of nano-seconds. The temperature sensitivity of the HTL gate is considerably less than that of DTL (Prob. 4.12).

4.8 TRANSISTOR–TRANSISTOR LOGIC (TTL)

Because of its speed limitations, DTL has become outdated and is completely replaced by another logic family referred to as transistor– transistor logic (TTL). The main cause for the speed limitation in DTL is the slow process of removal of stored base charge of the output transistor. For example, in the DTL gate of Fig. 4.12, when T goes from saturation to cut-off, the diodes D_1 and D_2 are nonconducting and hence, the base charge must leak-off through the resistor R_B, which is a relatively slow mechanism.

The DTL speed limitation is overcome by making the following modifications in the circuit of Fig. 4.12:

1. The input diodes D_A, D_B, and D_C are replaced by emitter–base junctions of multiple-emitter transistor (T_1), which is easily and economically fabricated in IC.
2. The collector–base junction of T_1 acts as the diode D_1.
3. The diode D_2 is replaced by emitter–base junction of another transistor (T_2).

The modified circuit is known as TTL and is shown in Fig. 4.16.

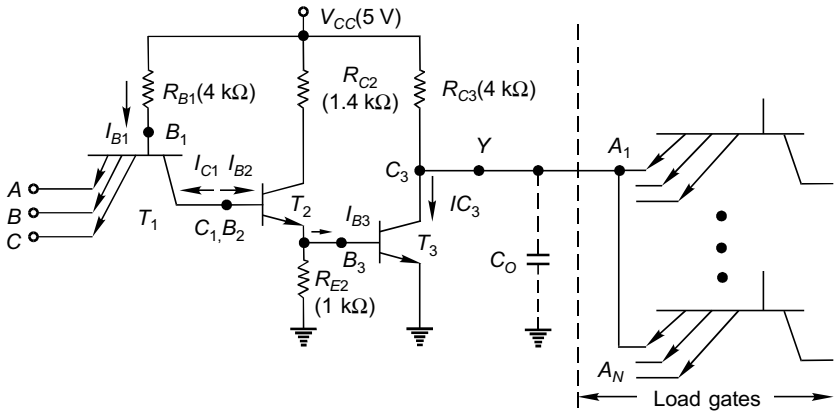

Fig. 4.16

A 3-input TTL NAND gate driving N similar gates.

4.8.1 Operation of TTL NAND Gate

The operation of the TTL gate of Fig. 4.16 is similar to the operation of the DTL gate of Fig. 4.12 as far as the steady-state operation is concerned, as is evident from conditions I and II discussed below. It is condition III that differentiates the operation of TTL from that of DTL and makes it the fastest of all saturating logic families.

For the operation discussed below, we assume that the load gates are not present and the voltages for logic 0 and 1 are $V_{CE,\,sat} \approx 0.2$ V and $V_{CC} = 5$ V respectively.

Condition I At least one input is LOW. The emitter–base junction of T_1 corresponding to the input in the LOW state is forward-biased making voltage at B_1, $V_{B1} = 0.2 + 0.7 = 0.9$ V. For base–collector junction of T_1 to be forward-biased, and for T_2 and T_3 to be conducting, V_{B1} is required to be at least $0.6 + 0.5 + 0.5 = 1.6$ V. Hence, T_2 and T_3 are OFF.

Since T_3 is OFF, therefore $Y = V(1) = V_{CC}$.

Condition II All inputs are HIGH. The emitter–base junctions of T_1 are reverse-biased. If we assume that T_2 and T_3 are ON, then $V_{B2} = V_{C1} = 0.8 + 0.8 = 1.6$ V. Since B_1 is connected to V_{CC} (5 V) through R_{B1}, the collector-base junction of T_1 is forward-biased. The transistor T_1 is operating in the active inverse mode, making I_{C1} flow in the reverse direction. This current flows into the base of T_2 driving T_2 and T_3 into saturation. Therefore, $Y = V(0) \approx 0.2$ V.

From conditions I and II, it appears that T_1 is acting as back-to-back diodes. The importance of T_1 will become clear from condition III.

Condition III Let the circuit be operating under condition II when one of the inputs suddenly goes to $V(0)$. The corresponding emitter–base junction of T_1 starts conducting and V_{B1} drops to 0.9 V. T_2 and T_3 will be turned off when the stored base charge is removed. Since $V_{C1} = V_{B2} = 1.6$ V, therefore the collector–base junction of T_1 is back-biased, making T_1 operate in the normal active region. This large collector current of T_1 is in a direction which helps in the removal of stored base charge in T_2 and T_3 and improves the speed of circuit.

The discussion in Sec. 4.6 regarding loading (fan-out) considerations, noise-margins, average power dissipation, propagation delays, and wired-AND connection, is equally valid for TTL gate of Fig. 4.16 with passive pull-up resistor.

The speed of the circuit can be improved by decreasing R_{C3} which decreases the time constant $(R_{C3} \cdot C_0)$ with which the output capacitance charges from 0 to 1 logic level. Such a reduction, however, would increase dissipation and would make it more difficult for T_3 to saturate.

4.8.2 Active Pull-up

It is possible in TTL gates to hasten the charging of output capacitance without corresponding increase in power dissipation with the help of an output circuit arrangement (Fig. 4.17) referred to as an *active pull-up* or *totem-pole* output.

The operation of the circuit can qualitatively be described as: For output Y to be in LOW state, transistor T_4 and diode D are cut-off. When the output makes a transition from LOW to HIGH corresponding to any input going to LOW, transistor T_4 enters saturation and supplies current for the charging of the output capacitor with a small time constant. This current decreases and eventually becomes zero under steady-state condition when $Y = V(1)$.

Diode D is used in the circuit to keep T_4 in cut-off when the output is at logic 0. Corresponding to this, T_2 and T_3 are in saturation, therefore,

$$V_{C2} = V_{B4} = V_{BE3,\,\text{sat}} + V_{CE2,\,\text{sat}} = 0.8 + 0.2 = 1.0 \text{ V} \tag{4.8}$$

Since $V_0 = V_{CE3,\,\text{sat}} \approx 0.2$ V, the voltage across the base-emitter junction of T_4 and diode D equals $1.0 - 0.2 = 0.8$ V, which means T_4 and D are cut-off.

If one of the inputs drops to LOW logic level, T_2 and T_3 go to cut-off. The output voltage cannot change instantaneously (being the voltage across C_0) and because of T_2 going to cut-off, the voltage at the base of T_4 rises driving it to saturation.

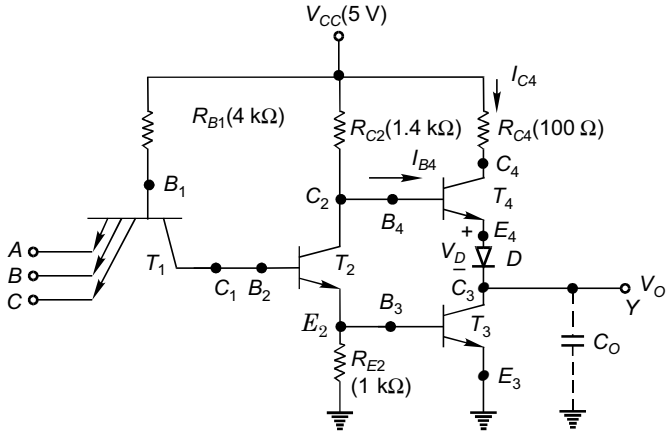

Fig. 4.17

A TTL gate with totem-pole output driver.

As soon as T_2 is cut-off,

$$V_{B4} = V_{BE4,\,sat} + V_D + V_O$$
$$= 0.8 + 0.7 + 0.2 = 1.7 \text{ V} \tag{4.9}$$

Therefore,
$$I_{B4} = \frac{V_{CC} - V_{B4}}{R_{C2}} = \frac{5 - 1.7}{1.4} = 2.36 \text{ mA} \tag{4.10}$$

and
$$I_{C4} = \frac{V_{CC} - V_{CE4,\,sat} - V_D - V_O}{R_{C4}}$$
$$= \frac{5 - 0.2 - 0.7 - 0.2}{0.1} = 39 \text{ mA} \tag{4.11}$$

Hence, T_4 is in saturation if h_{FE} exceeds $\frac{39}{2.36} = 16.5$.

The output voltage V_O rises exponentially towards V_{CC} with the time constant $= (R_{C4} + R_{CS4} + R_f)\ C_O$, where R_{CS4} is the saturation resistance of T_4 and R_f is the forward resistance of the diode.

As V_O increases, the base and collector currents of T_4 are decreased and eventually T_4 just comes out of conduction at steady-state. Therefore,

$$V(1) = V_{CC} - V_\gamma(T_4) - V_\gamma(\text{diode}) = 5 - 0.5 - 0.6 = 3.9 \text{ V}$$

Now, if the output is at $V(1)$ and all the inputs go to HIGH, T_2 goes ON. Consequently T_4 and D go OFF and T_3 conducts. The capacitor C_O discharges through T_3 and as V_O approaches $V(0)$, T_3 enters into saturation.

From the above discussion it is clear that the maximum current is drawn from the supply when the output makes a transition from $V(0)$ to $V(1)$ and equals $I_{C4} + I_{B4} = 39 + 2.4 = 41.4$ mA.

This current spike generates noise in the power supply distribution system and increases power dissipation in the gate, more so when it is operated at high frequencies.

4.8.3 Wired-AND

Wired-AND connection must not be used for totem-pole output circuits because of the current spike problem discussed above (Prob. 4.16). TTL circuits with open-collector outputs are available which can be used for wired-AND connections.

4.8.4 Open-Collector Output

A circuit with open-collector output is same as the circuit of Fig. 4.16 except for the collector–resistor R_{C3} of T_3 which is missing. The collector terminal C_3 is available outside the IC and the passive pull-up is to be connected externally. Naturally, the advantages of active pull-up are not available in this. Gates with open-collector output can be used for wired-AND operation (Prob. 4.18).

4.8.5 Unconnected Inputs

If any input of a TTL gate is left disconnected (open or floating) the corresponding E–B junction of T_1 will not be forward-biased. Hence, it acts exactly in the same way as if a logical 1 is applied to that input. Therefore, in TTL ICs, all unconnected inputs are treated as logical 1s. However, the unused inputs should either be connected to some used input(s) or returned to V_{CC} through a resistor.

4.8.6 Clamping Diodes

Clamping diodes are commonly used in all TTL gates to suppress the ringing caused from the fast voltage transitions found in TTL. These diodes shown in Fig. 4.18 clamp the negative undershoot at approximately – 0.7 V.

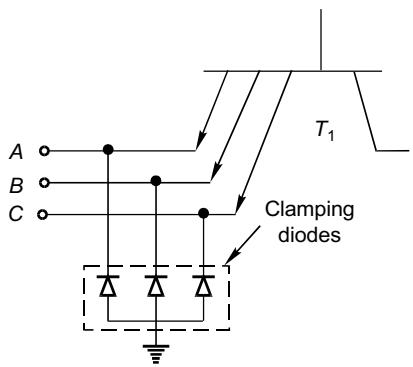

Fig. 4.18
A portion of a TTL gate showing the clamping diodes.

4.9 SCHOTTKY TTL

The speed limitation of TTL is mainly due to the turn-off time delays involved in transistors while making transitions from saturation to cut-off. This can be eliminated by replacing the transistors of TTL gate by Schottky transistors.

With this, the transistors are prevented from entering saturation and hence, there is saving in turn-off time. Schottky TTL gates have propagation delay time of the order of 2 ns which is very small in comparison with the propagation delay time of standard TTL which is of the order of 10 ns. It is a nonsaturating bipolar logic.

4.10 5400/7400 TTL SERIES

TTL 5400/7400 series is the most popular and commonly used series of digital ICs. 7400 devices are used for commercial applications whereas the 5400 devices are used for military

applications. The only difference in these two series are in the temperature and the power supply range. The temperature range is 0 °C to 70 °C for the 7400 series and –55 °C to 125 °C for the 5400 series. The supply voltage range is 5 ± 0.25 V for the 7400 series and 5 ± 0.5 V for the 5400 series.

There are seven different series of TTL 54-/74-logic family. These are given in Table 4.2.

Table 4.2 54-/74-TTL ICs with numbering scheme

Series	*Prefix*	*Examples*
Standard TTL	74-	7402, 74193
High Power TTL	74H-	74H02, 74H193
Low Power TTL	74L-	74L02, 74L193
Schottky TTL	74S-	74S02, 74S193
Low Power Schottky TTL	74LS-	74LS02, 74LS193
Advanced Schottky TTL	74AS-	74AS02, 74AS193
Advanced Low Power Schottky TTL	74ALS-	74ALS02, 74ALS193

Table 4.3 Specifications of TTL IC families

Parameter		*5400 7400*	*54H00 74H00*	*54L00 74L00*	*54S00 74S00*	*54LS00 74LS00*	*54AS00 74AS00*	*54ALS00 74ALS00*	*Units*
V_{IH}		2	2	2	2	2	2	2	Volts
V_{IL}	54 Series	0.8	0.8	0.7	0.8	0.7	0.8	0.8	Volts
	74 Series	0.8	0.8	0.7	0.8	0.8	0.8	0.8	
V_{OH}	54 Series	2.4	2.4	2.4	2.5	2.5	3	3	Volts
	74 Series	2.4	2.4	2.4	2.7	2.7	3	3	
V_{OL}	54 Series	0.4	0.4	0.3	0.5	0.4	0.5	0.4	Volts
	74 Series	0.4	0.4	0.4	0.5	0.5	0.5	0.5	
I_{IH}		40	50	10	50	20	20	20	μA
I_{IL}		–1.6	– 2.0	– 0.18	– 2.0	– 0.36	– 0.5	– 0.1	mA
I_{OH}		– 400	– 500	– 200	– 1000	– 400	– 2000	– 400	μA
I_{OL}	54 Series	16	20	2	20	4	20	4	mA
	74 Series	16	20	3.6	20	8	20	8	mA
$I_{CC}(1)$		8	16.8	0.8	16	1.6	3.2	0.85	mA
$I_{CC}(0)$		22	40	2.04	36	4.4	17.4	3	mA
t_{pHL}		15	10	60	5	15	4	8	ns
t_{pLH}		22	10	60	4.5	15	4.5	11	ns

Table 4.3 summarizes various specifications of 54/74 TTL logic families. Table 4.4 summerizes fan-out capabilities of each series when it drives ICs of the same series or of other series.

Table 4.4 Summary of TTL fan-out capabilities

Source TTL device / *Load TTL device* → ↓	*54/ 74*	*54H/ 74H*	*54L/ 74L*	*54S/ 74S*	*54LS/ 74LS*	*54AS/ 74AS*	*54ALS/ 74ALS*
54/74	10	8	40	8	20	20	20
54H/74H	12	10	50	10	25	25	25
54L/74L	2	1	20	1	10	7	10
54S/74S	12	10	100	10	50	40	50
54LS/74LS	5	4	40	4	20	16	26
54AS/74AS	12	10	110	10	55	40	100
54ALS/74ALS	5	4	40	4	20	16	20

From Table 4.3, we observe the following:

(i) The input and output voltage specifications are compatible for each of the TTL series, which makes it possible to use any mix of ICs of these series to achieve optimum design from the point of view of propagation delay and power dissipation.
(ii) The input and output current specifications are compatible and the number of gates of each of the series, which can be safely driven from any series can be determined as given in Table 4.4.
(iii) The low power dissipation series L, LS, and ALS have minimum power requirement and are suitable for battery operated circuits. Out of these series ALS series has the minimum propagation delay and therefore it is fast replacing other series.
(iv) H series has low propagation delay (high speed) but requires maximum power.
(v) S and AS series have very low propagation delay. The AS series is fast replacing S series because of its lower dissipation and propagation delay.

4.11 EMITTER-COUPLED LOGIC (ECL)

Emitter-coupled logic (ECL) is the fastest of all logic families and therefore is used in applications where very high speed is essential. High speeds have become possible in ECL because the transistors are used in difference amplifier configuration, in which they are never driven into saturation and thereby the storage time is eliminated. Here, rather than switching the transistors from ON to OFF and vice-versa, they are switched between cut-off and active regions. Propagation delays of less than 1 ns per gate have become possible in ECL.

Basically, ECL is realized using difference amplifier in which the emitters of the two transistors are connected and hence it is referred to as emitter-coupled logic. A 3-input ECL gate is shown in Fig. 4.19, which has three parts: The middle part is the difference amplifier which performs the logic operation.

Emitter follower are used for d.c. level shifting of the outputs, so that $V(0)$ and $V(1)$ are same for the inputs and the outputs. Note that two output Y_1 and Y_2 are available in this circuit which are complementary. Y_1 corresponds to OR logic and Y_2 to NOR logic and hence it is named as an OR/NOR gate.

Additional transistors are used in parallel to T_1 to get the required fan-in. There is a fundamental difference between all other logic families (including MOS logic) and ECL as far as the

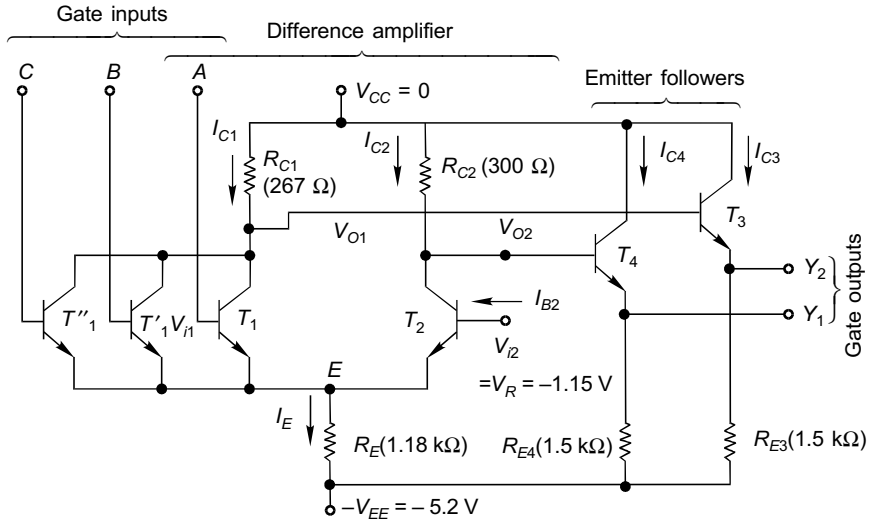

Fig. 4.19

A 3-input ECL OR/NOR gate.

supply voltage is concerned. In ECL, the positive end of the supply is connected to ground in contrast to other logic families in which negative end of the supply is grounded. This is done to minimize the effect of noise induced in the power supply (Prob. 4.22), and protection of the gate from an accidental short circuit developing between the output of a gate and ground (Prob. 4.23). The voltage corresponding to $V(0)$ and $V(1)$ are both negative due to positive end of the supply being connected to ground. The symbol of an ECL OR/NOR gate is shown in Fig. 4.20.

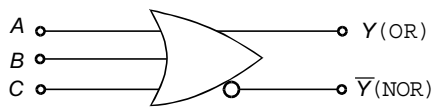

Fig. 4.20

The symbol for a 3-input OR/NOR gate.

Example 4.2 (a) Verify that the circuit of Fig. 4.19 performs OR/NOR operations. (b) Show that the transistors in this circuit operate in the active region and not in saturation. (c) Calculate the noise margins. (d) Find the average power dissipated by the gate.

Assume a base–emitter voltage of 0.7 V for a transistor conducting in active region.

Solution

(a) (i) Assume all inputs to be LOW.

Let us assume that the input transistors T_1, T'_1, T''_1 are cutt-off and T_2 is conducting in the active region. The voltage at the common emitter is $V_E = V_{i2} - V_{BE2} = -1.15 - 0.7 = -1.85$ V. The current

$$I_E = \frac{V_E - (-V_{EE})}{R_E} = \frac{-1.85 + 5.2}{1.18} = 2.84 \text{ mA}$$

Since $I_{B2} << I_{C2}$, therefore $I_{C2} \approx I_E$

$$V_{O2} = -0.3\ I_{C2} = -0.3\ (2.84) = -0.852 \text{ V}$$

Transistor T_4 will be conducting and the output at $Y_1 = V_{O2} - V_{BE4} = -0.852 - 0.7 = -1.55$ V which is assumed to be $V(0)$.

Therefore, if all the inputs are at $V(0) = -1.55$ V, then the base-to-emitter voltage of the input transistor is

$$V_{BE} = V_{i1} - V_E = -1.55 + 1.85 = 0.3 \text{ V}$$

which is less than the cut-in voltage (0.5 V) of the transistor and hence the input transistors are non-conducting, as was assumed above.

The base and collector of T_3 are effectively at the same potential, hence T_3 behaves as a diode. The current flowing through this diode is approximately 3 mA which corresponds to a voltage of about 0.75 V across the diode. Therefore, the voltage at $Y_2 = -0.75$ V which is assumed to be $V(1)$. This shows that Y_1 and Y_2 are complementary, i.e. $Y_2 = \overline{Y}_1$.

(ii) Assume at least one input to be HIGH. Corresponding to this the input transistor T_1 is assumed to be conducting and T_2 to be cut-off.

Then $V_E = V_{i1} - V_{BE1} = -0.75 - 0.7 = -1.45$ V

Hence, $V_{BE2} = V_{i2} - V_E = -1.15 + 1.45 = 0.3$ V which verifies the assumption that T_2 is cut-of.

The voltage $V_{O1} = -R_{C1} \times I_{C1}$

where $$I_{C1} = \frac{V_E - (-V_{EE})}{R_E}$$

$$= \frac{(-1.45 + 5.2)}{1.18} = 3.18 \text{ mA}$$

Since the collector current of T_1 is higher than the collector current of T_2 when it is conducting, hence $R_{C1} < R_{C2}$ to get the same voltage levels.

This gives voltage at $Y_2 = -1.55 = V(0)$. The voltage at $Y_1 = -0.75 = V(1)$. From (i) and (ii) above, we see that OR function is performed at Y_1 and NOR at Y_2. Hence it is an OR/NOR gate. Its voltages corresponding to logic 0 and 1 are –1.55 V and – 0.75 V respectively. The logic swing is 0.8 V.

(b) From part (a) (i), the voltage between collector and base of T_2 is $V_{CB2} = V_{O2} - V_{i2} = -0.85 + 1.15 = 0.30$ V which shows that the *C–B* junction is reverse-biased and hence T_2 is operating in its active region.

From part (a) (ii), the voltage between the collector and base of T_1 is

$$V_{CB1} = V_{O1} - V_{i1} = -0.85 + 0.75 = -0.1 \text{ V}$$

This shows that the *C–B* junction of T_1 is forward-biased but its magnitude is much less than the cut-in voltage and hence T_1 is operating in its active region.

(c) From part (a)(i), the base–emitter voltage of the input transistors is 0.3 V which is 0.2 V less than the cut-in voltage. Hence the noise margin $\Delta 0 = 0.2$ V.

From part (a) (ii) the base-emitter voltage of T_2 is 0.3 V which again gives a noise margin $\Delta 1 = 0.2$ V. The noise margins are equal and are quite small.

(d) From part (a) (i),

$$I_{C2} = 2.84 \text{ mA}$$

$$I_{C3} = \frac{5.2 - 0.75}{1.5} = 2.97 \text{ mA}$$

and $$I_{C4} = \frac{5.2 - 1.55}{1.5} = 2.43 \text{ mA}$$

From part (a) (ii),

$I_{C1} = 3.18$ mA
$I_{C3} = 2.43$ mA
$I_{C4} = 2.97$ mA

Therefore, average $I_E = \frac{2.84 + 3.18}{2} = 3.01$ mA. The total power supply current drain

$I_{EE} = 3.01 + 2.97 + 2.43 = 8.41$ mA

Therefore, the power dissipation = $V_{EE} \cdot I_{EE} = (5.2)\ (8.41)$
= 43.7 mW

4.11.1 Fan-Out

If all the inputs are LOW, the input transistors are cut-off. Therefore the input resistance is very high. On the other hand, if an input is HIGH, the input resistance is that of an emitter follower which is also high. Therefore, the input impedance is always high.

The output resistance is either that of an emitter follower or the forward resistance of a diode (T_3 or T_4 acts as a diode) which is always low. Because of the low output impedance and high input impedance, the fan-out is large.

4.11.2 Wired-OR Logic

The outputs of two or more ECL gates can be connected to obtain additional logic without using additional hardware. The wired-OR configurations are shown in Fig. 4.21.

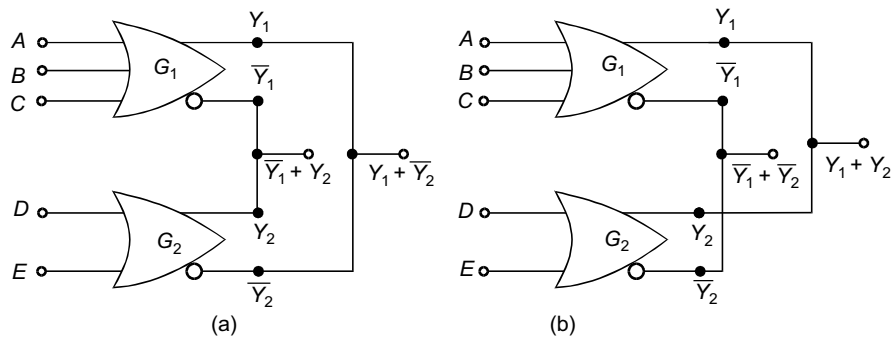

Fig. 4.21

Wired-OR connection of ECL gates.

4.11.3 Open-Emitter Outputs

Similar to open-collector output in TTL, open-emitter outputs are available in ECL which is useful for wired-OR applications.

4.11.4 Unconnected Inputs

If any input of an ECL gate is left unconnected, the corresponding E-B junction of the input transistor will not be conducting. Hence it acts as if a logical 0 level voltage is applied to that input. Therefore, in ECL ICs, all unconnected inputs are treated as logical 0s.

4.11.5 ECL Families

There are two popular ECL families:10xxx (or 10K) series and 100xxx (or 100K) series. The 100K series is the fastest of all logic families and has a propagation delay time less than 1 ns. Their voltage specifications are given in Table 4.5.

Table 4.5 Voltage specifications of ECL series

Series	*Supply voltage* V_{EE}, *V*	V_{OL} *V*	V_{OH} *V*	V_{IL} *V*	V_{IH} *V*
10K	5.2	–1.7	–0.9	–1.4	–1.2
100K	4.5	–1.7	–0.9	–1.4	–1.2

4.12 INTERFACING ECL AND TTL

It is often necessary to mix logic circuits of different families in the design of a digital system to realize the speed and power requirements by choosing the appropriate logic families for different parts of the system. Consider the interfacing between TTL and ECL gates. The logic levels in the two systems are entirely different and therefore level shifting circuits are required to be interposed between TTL and ECL gates. For TTL-to-ECL and ECL-to-TTL interfacing two level translator ICs are available. Interfacing using these ICs are described below.

4.12.1 TTL-to-ECL Translator

The MC10H124 is a quad TTL-to-ECL translator IC. It is a 16-pin IC and its logic diagram is shown in Fig. 4.22. It uses two power supplies; one positive and another negative for the generation of proper logic levels for ECL and TTL.

The logic levels of the translator circuit are:

$V_{IH} = 2\text{V},\ V_{IL} = 0.8\ \text{V}$

$V_{OH} = -0.98\text{V},\ V_{OL} = -1.63\text{V}$

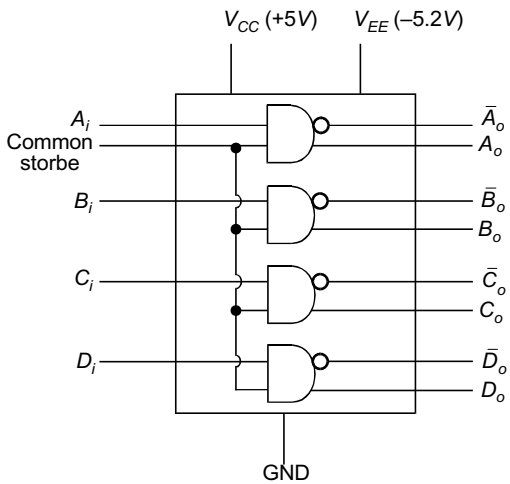

Fig. 4.22

Logic diagram of MC10H124 TTL-to-ECL translator

From Table 4.3, we have

$V_{OH} = 2.4$ V and $V_{OL} = 0.4$ V for TTL ICs. Comparing the output logic levels of TTL and the input logic levels of the translator IC, we observe,

$$V_{IH}\,(\text{Translator}) < V_{OH}\,(\text{TTL})$$

and

$$V_{IL}\,(\text{Translator}) > V_{OL}(\text{TTL})$$

which shows that the input logic levels of the translator are compatible with the output logic levels of TTL.

Similarly, comparing the output logic levels of the translator with the input logic levels of ECL (Table 4.5), we obtain

$$V_{IH}\,(\text{ECL}) < V_{OH}\,(\text{Translator})$$

and

$$V_{IL}\,(\text{ECL}) > V_{OL}\,(\text{Translator})$$

which demonstrates that the output logic levels of the translator are compatible with the input logic levels of ECL.

Figure 4.23 shows a TTL NAND gate driving an ECL NOR gate through a TTL-to-ECL translator gate.

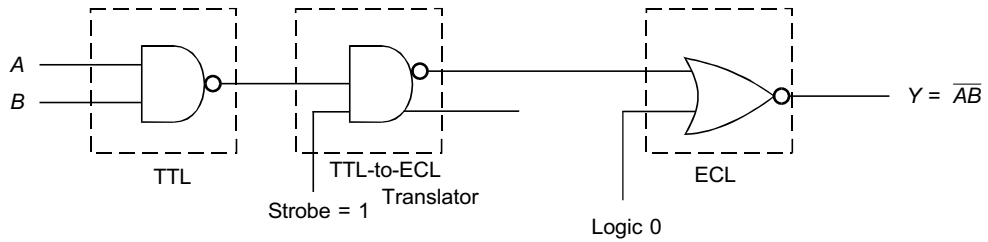

Fig. 4.23

A TTL NAND gate driving an ECL NOR gate through a TTL-to-ECL translator

4.12.2 ECL-to-TTL Translator

The MC10H125 is a quad ECL-to-TTL translator IC. It is a 16-pin IC and its logic diagram is shown in Fig. 4.24. It also uses two power supplies for the generation of proper logic levels for ECL and TTL. Its logic levels are:

$$V_{IH} = -1.13 \text{ V}, \quad V_{IL} = -1.48 \text{ V}$$

$$V_{OH} = 2.5 \text{ V}, \quad V_{OL} = 0.5 \text{ V}$$

Its input logic levels are compatible with ECL and the output logic levels are compatible with TTL (Prob. 4.26).

4.13 MOS LOGIC

MOSFETs have become very popular for logic circuits due to high density of fabrication and low power dissipation. When MOS devices are used in logic circuits, there can be circuits in which either only *p*– or only *n*-channel devices are used. Such circuits are referred to as PMOS and NMOS logic respectively. It is also possible to fabricate enhancement mode *p*-channel and *n*-channel MOS devices on the same chip. Such devices are referred to as complementary

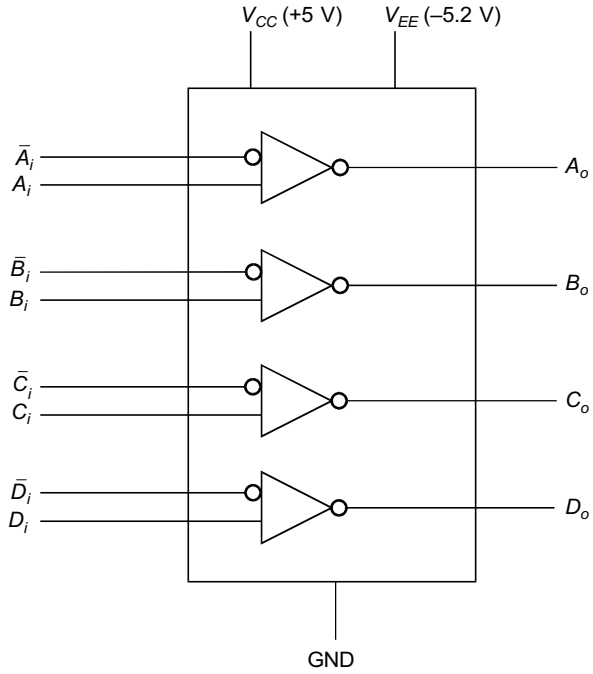

Fig. 4.24

Logic diagram of MC10H125 ECL-to-TTL translator

MOSFETs and logic based on these devices is known as CMOS logic. The power dissipation is extremely small for CMOS and hence CMOS logic has become very popular.

The basic MOS gate is an inverter as shown in Fig. 4.25, in which T_1 is an enhancement MOSFET which acts as driver and T_2 may be an enhancement (Fig. 4.25a) or depletion (Fig. 4.25b) MOSFET, which acts as load. Instead of fabricating diffusion resistor for load,

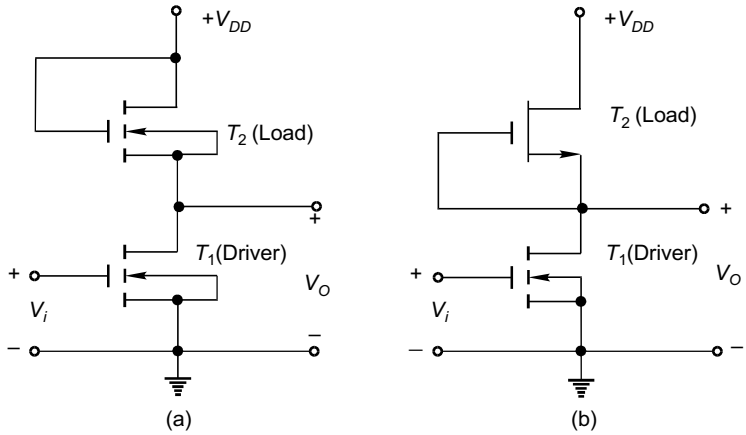

Fig. 4.25

A MOS inverter with (a) Enhancement load (b) Depletion load.

which usually occupies an area about 20 times that of a MOS device, MOSFET itself is used as the load. This makes possible high density of fabrication and therefore MOS logic made large scale integration possible.

The logic levels for the MOS circuits are

$$V(0) \approx 0$$
$$V(1) \approx V_{DD}$$

Although the MOS logic circuits are identical in configuration to bipolar DCTL, the problem of current hogging is not present. The operation of MOSFET switches is given in Section 3.7.

MOS logic is mainly used for LSI and VLSI ICs and not for SSI and MSI ICs. Most of the microprocessors, memories, and peripheral devices are available in NMOS.

4.13.1 MOSFET NAND and NOR Gates

NOR gates can be obtained by using multiple drivers in parallel, whereas for NAND gates the drivers are to be connected in series. A two-input NOR gate is shown in Fig. 4.26*a* and a two-input NAND gate in Fig. 4.26*b*.

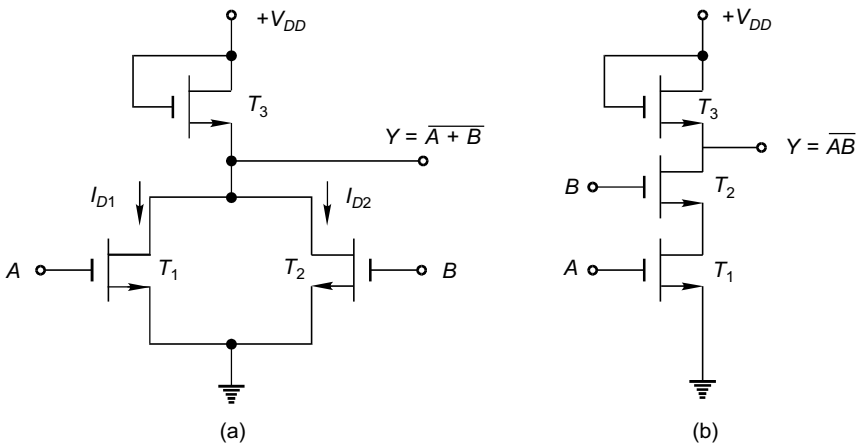

Fig. 4.26

2-input NMOS gates (a) NOR (b) NAND.

In the gate of Fig. 4.26*a*, if both inputs are 0, both transistors T_1 and T_2 are OFF ($I_{D1} = I_{D2} = 0$), hence the output is V_{DD}. If either one or both of the inputs are $V(1) = V_{DD}$, the corresponding FETs will be ON and the output is 0 V. Its truth table is given in Table 4.6, which obviously shows NOR operation.

In the gate of Fig. 4.26*b*, if either one or both the inputs are $V(0) = 0$, the corresponding FETs will be OFF, the voltage across the load FET will be 0, hence the output is V_{DD}. If both inputs are $V(1) = V_{DD}$, both T_1 and T_2 are ON and the output is 0. Its truth table is given in Table 4.7, which shows NAND operation.

Table 4.6 Truth table of Fig. 4.26*a*

Inputs		*Output*
A	*B*	*Y*
0	0	V_{DD}
0	V_{DD}	0
V_{DD}	0	0
V_{DD}	V_{DD}	0

Table 4.7 Truth table of Fig. 4.26*b*

Inputs		*Output*
A	*B*	*Y*
0	0	V_{DD}
0	V_{DD}	V_{DD}
V_{DD}	0	V_{DD}
V_{DD}	V_{DD}	0

4.13.2 Fan-Out

Since MOS devices have very high input impedance, therefore, the fan-out is large. But driving a large number of MOS gates increases the capacitance at the output of the driving gate which reduces, considerably, the speed of MOS gates.

The voltage and current parameters for 8085, 8086 microprocessors and other NMOS devices are:

$V_{CC} = 5$ V
$V_{IL} = 0.8$ V
$V_{IH} = 2$ V
$V_{OL} = 0.45$ V, $I_{OL} = 2$ mA
$V_{OH} = 2.4$ V, $I_{OH} = -400$ μA

The input and output leakage currents are $\pm$ 10 μA.

These voltages are directly compatible with TTL ICs. Usually, NMOS devices are available with higher sink currents which are directly compatible with TTL ICs. This helps in easy interfacing between NMOS devices and TTL devices.

4.13.3 Propagation Delay Time

The propagation delay time is large in MOS devices because of large capacitances present at the input and output of these devices. Also, the resistance through which these capacitors get charged and discharged is high.

In MOS devices, the phenomenon of minority charge storage is not present, and the speed of operation is mainly determined by the speed with which the capacitors get charged and discharged.

Due to the developments in the technology of MOS fabrication, it has become possible to obtain speeds which are comparable to TTL.

4.13.4 Power Dissipation

In the NAND gate of Fig. 4.26*b*, current is drawn from the power supply only during one of the four possible input conditions, whereas in the NOR gate of Fig. 4.23*a* power is drawn during three out of four input conditions. Therefore, the power consumption in MOS circuits is small which is very useful for large-scale integration.

4.13.5 Unconnected Inputs

MOS devices have very high input impedance and even a very small static charge flowing into this high impedance can develop a dangerously high voltage. This may cause damage to the device by rupturing the insulation layer and also to the persons handling such devices. Therefore, MOS ICs inputs must not be left unconnected. Even for storage of such devices, conductive foam or aluminium foil should be used which will ensure shorting of IC pins together so that no voltage can be developed between the pins. Necessary precautions must be taken while handling such devices.

4.14 CMOS LOGIC

A complementary MOSFET (CMOS) is obtained by connecting a *p*-channel and an *n*-channel MOSFET in series, with drains tied together and the output is taken at the common drain. Input is applied at the common gate formed by connecting the two gates together (Fig. 3.33). in a CMOS, *p*-channel and *n*-channel enhancement MOS devices are fabricated on the same chip, which makes its fabrication more complicated and reduces the packing density. But because of negligibly small power consumption, CMOS is ideally suited for battery operated systems.

Its speed is limited by substrate capacitances. To reduce the effect of these substrate capacitances, the latest technology known as silicon on sapphire (SOS) is used in microprocessor fabrication which employs an insulating substrate (sapphire). CMOS has become the most popular in MSI and LSI areas and is the only possible logic for the fabrication of VLSI devices.

4.14.1 CMOS Inverter

The basic CMOS logic circuit is an inverter shown in Fig. 3.33. For this circuit the logic levels are 0 V (logic 0) and V_{CC} (logic 1). When $V_i = V_{CC}$, T_1 turns ON and T_2 turns OFF. Therefore $V_0 \approx 0$ V, and since the transistors are connected in series the current I_D is very small. On the other hand, when $V_i = 0$ V, T_1 turns OFF and T_2 turns ON giving an output voltage $V_0 \approx V_{CC}$ and I_D is again very small. In either logic state, T_1 or T_2 is OFF and the quiscent power dissipation which is the product of the OFF leakage current and V_{CC} is very low. More complex functions can be realized by combinations of inverters.

4.14.2 CMOS NAND and NOR Gates

A 2-input CMOS NAND gate is shown in Fig. 4.27 and NOR gate in Fig. 4.28. In the NAND gate, the NMOS drivers are connected in series, where as the PMOS loads are connected in parallel. On the other hand, the CMOS NOR gate is obtained by connecting the NMOS drivers in parallel and PMOS loads in series. The operation of NAND gate can be understood from Table 4.8. The operation of the NOR gate can be verified in the similar manner (Prob. 4.29).

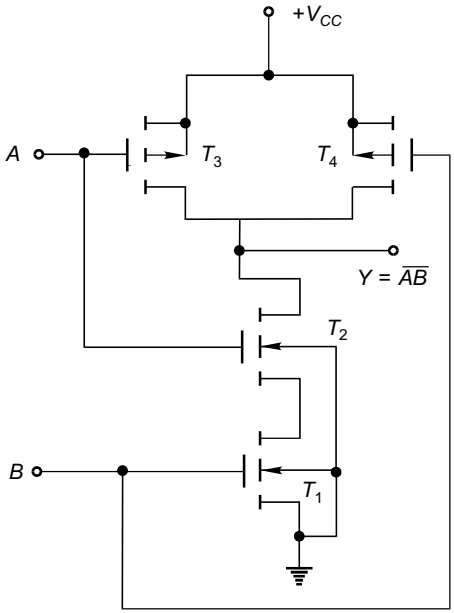

Fig. 4.27
A 2-input CMOS NAND gate.

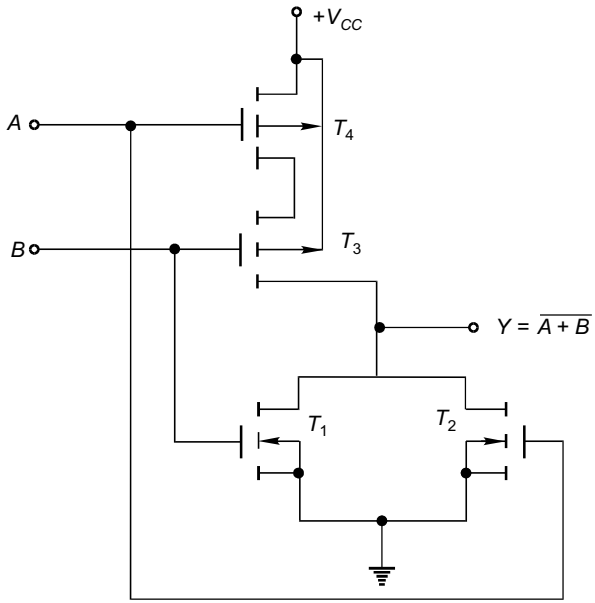

Fig. 4.28
A 2-input CMOS NOR gate.

Table 4.8 Operation of CMOS NAND gate

Inputs		*State of MOS devices*				*Output*
A	B	T_1	T_2	T_3	T_4	Y
0	0	OFF	OFF	ON	ON	V_{CC}
0	V_{CC}	ON	OFF	ON	OFF	V_{CC}
V_{CC}	0	OFF	ON	OFF	ON	V_{CC}
V_{CC}	V_{CC}	ON	ON	OFF	OFF	0

4.14.3 CMOS Transmission Gate

A CMOS transmission gate controlled by gate voltages C and $\overline{C}$ is shown in Fig. 4.29. Assume $C = 1$. If $A = V(1)$, then T_1 is OFF and T_2 conducts in the ohmic region because there is no voltage applied at the drain. Therefore, T_2 behaves as a small resistance connecting the output to the input and $B = A = V(1)$. Similarly, if $A = V(0)$, then T_2 is OFF and T_1 conducts, connecting the output to the input and $B = A = V(0)$. This means the signal is transmitted from A to B when $C = 1$.

In a similar manner, it can be shown that if $C = 0$, transmission is not possible.

In this gate the control C is binary, whereas the input at A may be either digital or analog [the instantaneous value must lie between $V(0)$ and $V(1)$].

4.14.4 Noise Margin

Noise margin of CMOS logic ICs is considerably higher than that of TTL ICs. CMOS devices

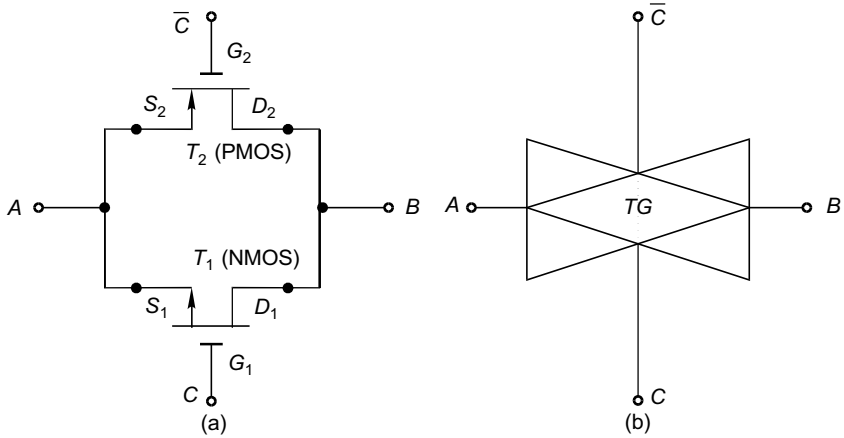

Fig. 4.29

(a) A CMOS transmission gate (b) Its symbol.

have wide supply voltage range and the noise margin increases with the supply voltage V_{CC}. Typically, it is 0.45 V_{CC}.

4.14.5 Unconnected Inputs

The unconnected CMOS ICs inputs behave in a way similar to MOS devices discussed in Section 4.13. Therefore, the unused inputs must be connected to either the supply voltage terminal or one of the used inputs provided that the fan-out of the signal source is not exceeded. This is highly unlikely for CMOS circuits because of their high fan-out.

Some CMOS ICs have Zener diodes connected at the inputs for protection against high input voltages.

4.14.6 Wired-Logic

Figure 4.30 shows two CMOS inverters with their outputs connected together. In this circuit,

(i) When $A = B = V(0)$
T_1 and T_1' are cut-off and $Y = V(1) = V_{CC}$

(ii) When $A = B = V(1)$
T_1 and T_1' are ON and $Y = V(0) = 0$

(iii) When $A = V(1)$ and $B = V(0)$
T_1 and T_2' are ON whereas
T_1' and T_2 are OFF

Therefore, a large current I will flow as shown in Fig. 4.30.
This will make voltage at Y equal to $V_{CC}/2$ which is neither in the range of logic 0 nor in the range of logic 1. Therefore, the circuit will not operate properly. Also because of large current I, the transistors will be damaged.

Similarly, corresponding to $A = V(0)$ and $B = V(1)$ the operation will not be proper.

Therefore, wired-logic must not be used for CMOS logic circuits.

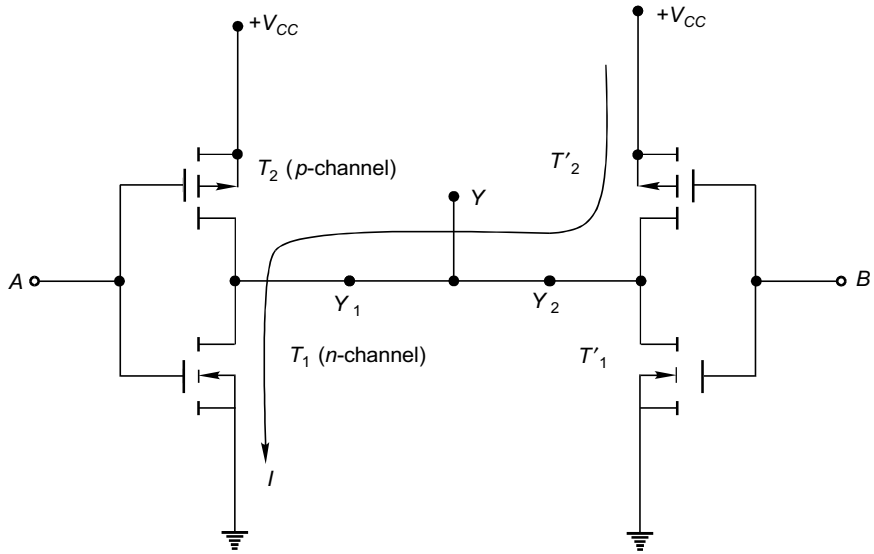

Fig. 4.30

CMOS inverters with outputs connected.

4.14.7 Open-Drain Outputs

CMOS gates with open-drain output are available which are useful for wired-AND operation. In this the drain terminal of the output transistor (*n*-channel) is available outside and the load resistor is to be connected externally since *p*-channel load does not exist.

4.14.8 54C00/74C00 CMOS Series

There are two commonly used CMOS series ICs. These are the 4000 series and 54C/74C series. 54C/74C CMOS series is pin-for-pin, function-for-function equivalent to the 54/74 TTL family and has, therefore, become very popular. The temperature range for 54C series is – 55 °C to + 125 °C and for 74C series is –40 °C to 85 °C. It has a wide supply voltage range, 3 V to 15 V. A person can take full advantage of his knowledge of the 54/74 TTL series for the effective use of 54C/74C series.

There have been significant improvements in 54C/74C series. The 74HC/74HCT have higher speed and better current capabilities. 74HC is known as *high-speed* CMOS and 74HCT is known as *high-speed, TTL compatible* CMOS series. 74AC/74ACT are very fast and have very high current sinking capabilities. These are known as *advanced* CMOS and *advanced, TTL compatible* CMOS, respectively. The 74 HC/74HCT/74AC/74ACT series can be operated at supply voltages in the range of 2–6 volts.

The voltage and current parameters of various 74 CMOS series with 5 V supply voltage are given in Table 4.9. From the table, we observe that the output currents and voltages for 74HC/74HCT/74AC/74ACT are different when gates of these series are driving CMOS circuits and TTL circuits. 74 HCT and 74 ACT series are compatible with TTL series for input as well as output and therefore, can easily be used along with TTL ICs for optimum system design from the point of view of speed, power dissipation, noise margins, cost, etc.

The fan-out of 74 HC/74HCT series is 20, whreas for 74AC/74ACT series it is 50 while driving these CMOS series. The fan-out of these gates while driving various TTL series gates can be determined using the specifications of TTL (Table 4.3) and CMOS (Table 4.9).

Table 4.9 Specifications of CMOS IC families

Parameter	*Load*	*74C*	*74HC*	*74HCT*	*74AC*	*74ACT*	*Units*
V_{IH}		3.5	3.85	2.0	3.85	2.0	volts
V_{IL}		1.5	1.35	0.8	1.35	0.8	volts
V_{OH}	CMOS	4.5	4.4	4.4	4.4	4.4	volts
	TTL		3.84	3.84	3.76	3.76	volts
V_{OL}	CMOS	0.5	0.1	0.1	0.1	0.1	volt
	TTL		0.33	0.33	0.37	0.37	volt
I_{IH}		1	1	1	1	1	μA
I_{IL}		– 1	– 1	– 1	– 1	– 1	μA
I_{OH}	CMOS	– 0.1	– 0.02	– 0.02	– 0.05	– 0.05	mA
	TTL		– 4.0	– 4.0	– 24.0	– 24.0	mA
I_{OL}	CMOS	0.36	0.02	0.02	0.05	0.05	mA
	TTL		4.0	4.0	24.0	24.0	mA

4.15 INTERFACING CMOS AND TTL

To achieve optimum performance in a digital system, devices from more than one logic family can be used, taking advantages of the superior characteristics of each family for different parts of the system. For example, CMOS logic ICs can be used in those parts of the system where low power dissipation is required, while TTL can be used in those portions of the system which requires high speed of operation. Also, some functions may be easily available in TTL and others may be available in CMOS. Therefore, it is necessary to examine the interface between TTL and CMOS devices.

The 74C series of CMOS ICs can be operated for any supply voltage in the range of 3 V to 15 V, whereas the 74HC/74HCT/74AC/74ACT series have the supply voltage range of 2 V to 6 V. Since the supply voltage used for all 74 series TTL ICs is 5 V, therefore, it is necessary to operate CMOS devices at + 5 V, to make it compatible with TTL devices.

4.15.1 CMOS Driving TTL

Figure 4.31 shows a CMOS gate driving N TTL gates. For such an arrangement to operate properly the following conditions are required to be satisfied,

$$V_{OH}\,(\text{CMOS}) \geq V_{IH}\,(\text{TTL}) \tag{4.12}$$

$$V_{OL}\,(\text{CMOS}) \leq V_{IL}\,(\text{TTL}) \tag{4.13}$$

$$-I_{OH}\,(\text{CMOS}) \geq NI_{IH}\,(\text{TTL}) \tag{4.14}$$

$$I_{OL}\,(\text{CMOS}) \geq -NI_{IL}\,(\text{TTL}) \tag{4.15}$$

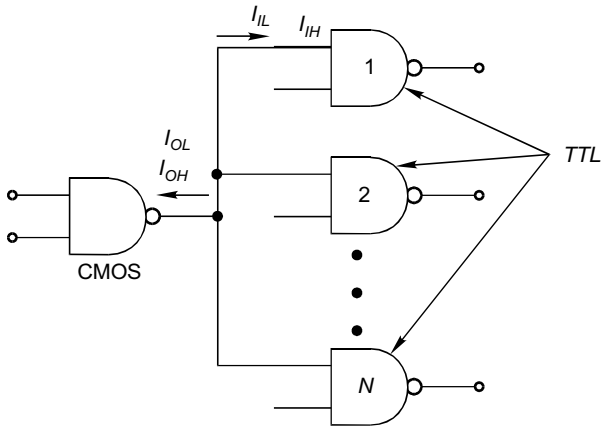

Fig. 4.31

A CMOS gate driving N TTL gates.

From the specifications given in Tables 4.3 and 4.9, we observe the following:

(i) The conditions of Eqs (4.12) and (4.13) are always satisfied. The noise margins when 74ACT is driving 74ALS gates are

$$\Delta\ 1 = 3.76 - 2.0 = 1.76 \text{ V}$$
$$\Delta\ 0 = 0.8 - 0.37 = 0.43 \text{ V}$$

(ii) The conditions of Eqs (4.14) and (4.15) are always satisfied for 74 HC/74 HCT/74 AC/ 74 ACT series. The value of N is different for different series. The value of N when 74 ACT is driving 74ALS gates is 240.

In case of 74 C series, the condition of Eq. (4.14) is satisfied for small values of N but the condition of Eq. (4.15) is not satisfied even for $N = 1$, except in case of 74L and 74ALS TTL series. This difficulty can be overcome by using CMOS buffers having an adequate available output current.

If 74C series gate is driving 74L series gates, the condition of Eq. (4.15) is satisfied for $N = 2$ and in case of 74ALS gates for $N = 3$.

4.15.2 TTL Driving CMOS

Figure 4.32 shows a TTL gate driving N CMOS gates. For such an arrangement to operate properly, the following conditions are required to be satisfied:

$$V_{OH}\ (\text{TTL}) \geq V_{IH}\ (\text{CMOS}) \tag{4.16}$$
$$V_{OL}\ (\text{TTL}) \leq V_{IL}\ (\text{CMOS}) \tag{4.17}$$
$$-I_{OH}\ (\text{TTL}) \geq NI_{IH}\ (\text{CMOS}) \tag{4.18}$$
$$I_{OL}\ (\text{TTL}) \geq -NI_{IL}\ (\text{CMOS}) \tag{4.19}$$

All the above conditions are always satisfied in case of 74 HCT and 74 ACT series for high values of N. This shows that these two CMOS series are TTL compatible. In the case of 74C/ 74HC/74AC series, the condition of Eq. (4.16) is not satisfied. A circuit modification used to

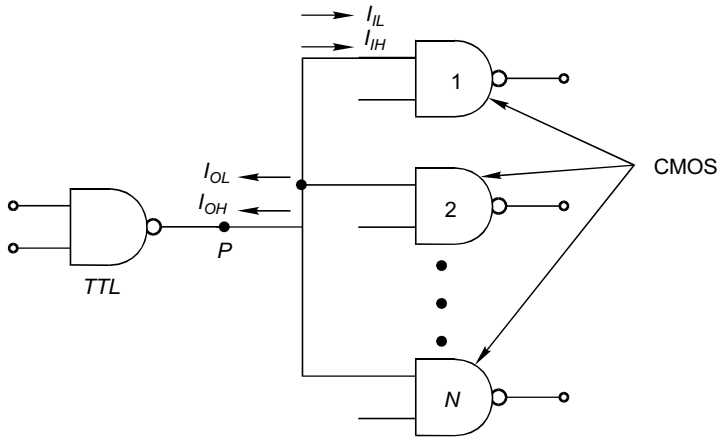

Fig. 4.32

A TTL gate driving *N* CMOS gates.

raise V_{OH} (TTL) above 3.5 V is obtained by connecting a resistance ($\approx$ 2 K Ω) between points *P* and V_{CC} as shown in Fig. 4.33. This acts as a passive pull-up, which pulls up the voltage at *P*, by charging the capacitor C_0 present between *P* and the ground terminal, to a higher value ($\approx V_{CC}$) after the transistor T_4 of the TTL becomes non-conducting.

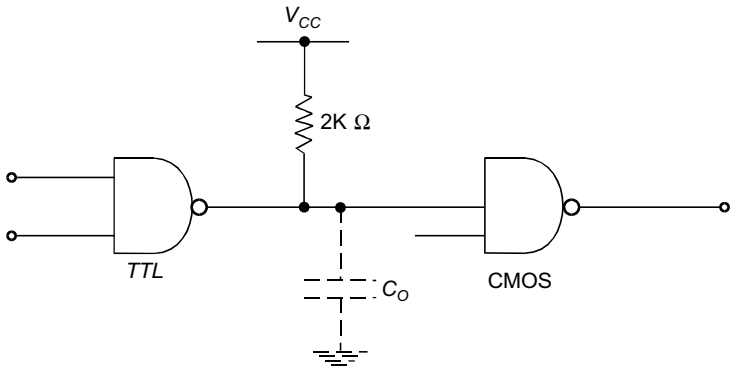

Fig. 4.33

Circuit to pull up the output voltage of TTL.

4.16 INTERFACING CMOS AND ECL

Using MC10H124 TTL-to-ECL translator and MC10H125 ECL-to-TTL translator ICs, it is possible to interface CMOS and ECL logic families. The input of MC10H124 translator is compatible to the output logic voltages of CMOS and therefore, this can be used for CMOs-to-ECL interfacing (Prob. 4.33). Similarly, the output of MC10H125 translator is compatible to the input logic voltages of CMOS (74 HCT and 74 ACT) families which makes it possible to be

used it for ECL-to-CMOS interfacing. Other CMOS logic families can also be interfaced using pull-up resistor similar to Fig. 4.33 (Prob. 4.34).

4.17 TRI-STATE LOGIC

In normal logic circuits there are two states of the output, LOW and HIGH. If the output is not in the LOW state, it is definitely in the other state (HIGH). Similarly, if the output is not in the HIGH state, it is definitely in the LOW state. In complex digital systems like microcomputers and microprocessors, a number of gate outputs may be required to be connected to a common line which is referred to as a *bus* which, in turn, may be required to drive a number of gate inputs. When a number of gate outputs are connected to the bus, we encounter some difficulties. These are:

1. Totem-pole outputs cannot be connected together because of very large current drain from the supply and consequent heating of the ICs which may get damaged.
2. Open-collector outputs can be connected together with a common collector-resistor connected externally. This causes the problems of loading and speed of operation.

To overcome these difficulties, special circuits have been developed in which there is one more state of the output, referred to as the *third state* or *high-impedance state*, in addition to the LOW and HIGH states. These circuits are known as *TRI-STATE, tri-state logic* (TSL) or *three-state logic*. TRI-STATE, is a registered trade mark of National Semiconductor Corporation of USA.

There is a basic functional difference between wired-OR and the TSL. For the wired-OR connection of two functions Y_1 and Y_2 is

$$Y = Y_1 + Y_2 \tag{4.20}$$

whereas for TSL, the result is not a Boolean function but an ability to multiplex many functions economically.

4.17.1 TSL Inverter

A TSL inverter circuit with tri-state output is shown in Fig. 4.34. When the control input is LOW, the drive is removed from T_3 and T_4. Hence, both T_3 and T_4 are cut-off and the output is in the third state. When the control input is HIGH, the output Y is logic 1 or 0 depending on the data input. The logic symbol of a TSL inverter is shown in Fig. 4.35 and its truth table is given in Table 4.10.

Table 4.10 Truth table of a TSL inverter

Data input	Control	Data output
0	0	HIGH – Z
1	0	HIGH – Z
0	1	1
1	1	0

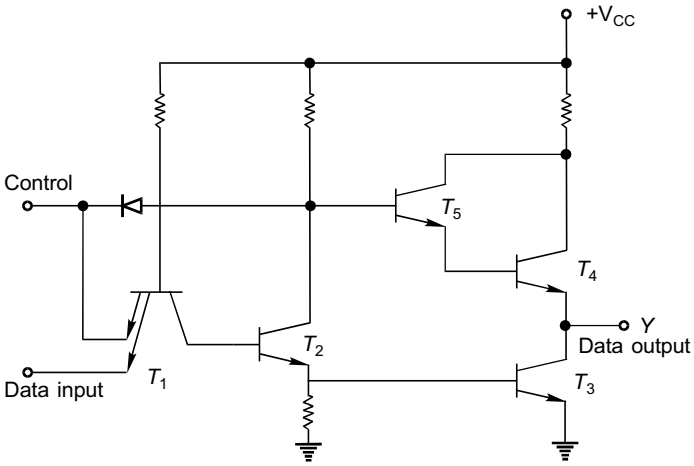

Fig. 4.34
A TSL inverter.

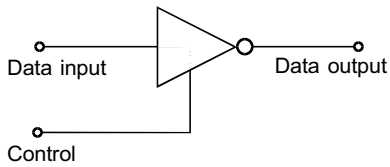

Fig. 4.35
Logic symbol of a TSL inverter.

The output and input current specifications of TSL family are given in Table 4.11.

Table 4.11 Current specifications of TSL family

Parameter	*Control input*	
	LOW (DISABLE)	*HIGH (ENABLE)*
I_{IH}	40 μA	40 μA
I_{IL}	– 1.6 mA	– 1.6 mA
I_{OH}	40 μA	– 5.2 mA
I_{OL}	– 40 μA	16 mA

Example 4.3 Consider the arrangement shown in Fig. 4.36. At any time one of the gates drives the bus line. Calculate the maximum possible value of N.

Solution

Let I_1 be driving the bus line. All other gates, I_2 through I_N must be tristated.

If the output of I_1 is in logic 1 state, it has to supply leakage current (40 μA) to each of the tri-stated gates and input current to G_1 and G_2 (40 μA). From Table 4.11, we have the maximum possible output current of TSL in logic 1 state as 5.2 mA. Therefore,

$$40(N - 1) + 40(2) \leq 5.2 \times 10^3$$

or

$$N \leq 129$$

which means 129 TSL outputs can be connected to the bus line.

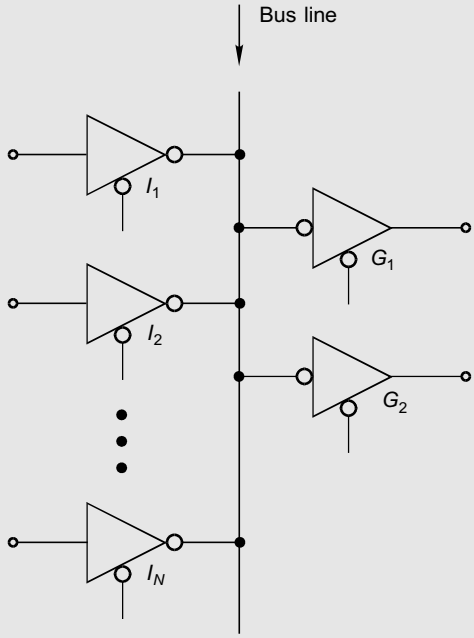

Fig. 4.36
N TSL gates driving a bus line.

4.18 SUMMARY

Essential features of all the major logic families have been discussed and the important conclusion are given below:

1. RTL and DTL families are no more used for new systems because of their low speed, high power dissipation, and low fan-out.
2. TTL is the most popular general purpose logic family. It is available in seven different series with a wide range of operating speed, power dissipation, and fan-out. There are a large number of functions in SSI and MSI available in TTL.

   TTL ICs are available with totem-pole output (which decreases speed-power product), open-collector output (which makes possible wired-AND connection and bus operation), and tri-state (TSL) outputs (which are ideally suited for bus operation).
3. HTL are best suited for an industrial environment where electrical noise level is high.
4. ECL is the fastest logic family. Its main disadvantages are low noise-margins and high power dissipation. For interfacing with other logic families, level-shifting networks are required.
5. I^2L is the only saturated bipolar logic suitable for LSI because of small silicon chip area required, and low power consumption. The supply voltage required is low hence it is highly suitable for battery operated systems.

I^2L circuits can drive TTL circuits if a resistive load is connected to the output stage of I^2L with a higher supply voltage (5 V).

6. MOS devices occupy a very small fraction of silicon chip area in comparison to bipolar devices and require very small power. Therefore, MOS logic is the most popular logic for LSI. The main drawback of MOS logic is slow speed, which is being improved upon by improvements in the technology of MOS fabrication. HMOS, a variety of NMOS has speeds comparable to bipolar logic families.
7. CMOS has the lowest speed power product and requires very small power.
   It is the most popular logic family and has led to the VLSI chips.
8. Corresponding to TTL 54/74 series, 54C/74C, 54HC/74HC, 54HCT/74HCT, 54AC/74AC and 54ACT/74ACT series have been developed which are directly compatible with various 54/74TTL series and have the same numbering scheme and pinouts.

A comparison of various digital IC logic families is given in Table 4.12.

Glossary

Active pull-up A circuit with active devices used to pull up the output voltage of a logic circuit from LOW to HIGH in response to the appropriate inputs.

Bipolar logic Logic circuits using bipolar junction semiconductor devices.

Breadth of logic family The number of different types of gates and other functions available in an IC logic family.

Buffer A circuit or gate that can drive a substantially higher number of gates or other loads. Also known as Buffer driver.

Bus A group of conductors carrying a related set of signals.

CMOS (Complementary metal-oxide semiconductor) A MOS device that uses one *p*-channel one *n*-channel device to make an inverter circuit.

Current sink logic A logic circuit in which the output sink current corresponding to logic 0 state is appreciably higher than the output source current corresponding to logic 1 state.

Current source logic A logic circuit in which the output source current corresponding to logic 1 state is appreciably higher than the output sink current corresponding to logic 0 state.

DCTL (Direct-coupled transistor logic) A form of bipolar logic that uses direct coupling.

Depletion mode MOSFET A MOS device in which channel width gets depleted when the voltage of proper polarity is applied at the gate.

DTL (Diode transistor logic) A form of bipolar logic circuit that uses diodes and bipolar junction transistors to realize a logic operation.

ECL (Emitter-coupled logic) A form of bipolar logic circuit that uses emitter-coupled configuration.

Enhancement mode MOSFET A MOS device in which the channel is formed only when a proper voltage is applied at the gate. The channel width enhances with the increased voltage at the gate.

Fan-in The number of inputs of a logic gate.

Table 4.12 Comparison of digital IC logic families

Parameter \ *Logic family*	*RTL*	*I^2L*	*DTL*	*HTL*	*TTL*				
					Standard	*High-Power high-speed H*	*Low-power low-speed L*	*Schottky low-power LS*	*Schottky S*
Basic gate	NOR	NOR	NAND	NAND	NAND	NAND	NAND	NAND	NAND
Fan-out	5	Depends on injector current	8	10	10	10	20	20	10
Power dissipation in mW per gate	12	6nW-70 μW	8-12	55	10	22	1	2	19
Noise immunity	Nominal	Poor	Good	Excel-lent	Very good	Very good	Very good	Very good	Very good
Propagation delay in ns per gate	12	25-250	30	90	10	6	33	9.5	3
Speed-power product (pJ)	144	<1	300	4950	100	132	33	19	57
Clock rate (MHz) for FFs	8	–	72	4	35	50	3	45	125
Available functions	High	LSI only	Fairly high	Nomi-nal	Very high	Very high	Very high	Very high	Very high

(*Contd.*)

Table 4.12 (*Contd.*)

Advanced Schottky AS	*Advanced low-power Schottky ALS*	*ECL*		*MOS*	*CMOS*				
		10K	*100K*		*74C*	*74HC*	*74HCT*	*74AC*	*74ACT*
NAND	NAND	OR–NOR	OR–NOR	NAND	NOR or NAND	NOR or NAND	NOR or NAND	NOR or NAND	NOR or NAND
40	20	25		20	50	20	20	50	50
10	1	40-55	40-55	0.2-10	Static 0.01	0.0025	0.0025	0.005	0.005
					Dynamic				
					1 MHz 1	0.6	0.6	0.75	0.75
					Total 1.01	0.6025	0.6025	0.755	0.755
Very good	Very good	Poor	Poor	Good	Very good	Very good	Very good	Very good	Very good
1.5	4	2	0.75	300	70.0	18	18	5.25	4.75
15	4	100	40	60	d.c. 0.7	0.045	0.045	0.026	0.024
					dynamic				
					(at 1 MHz)70.7	10.8	10.8	4.0	3.6
175	50	>60	600 MHz	2	10	60	60	100	100
Very high	Very high	High	High	Low	High	High	High	High	High

Fan-out The maximum number of similar logic gates which can be driven by a logic gate.

Field-effect transistor (FET) A three terminal semiconductor device in which the current flow is due to the flow of one type of charge carriers only. The current in the channel is controlled by the field produced due to the applied voltage at the gate.

Figure of merit (of digital ICs) It is the product of speed expressed as propagation delay time and power dissipation. It is also known as the speed power product.

High-impedance state The third state of a tristate logic (TSL) in which the device is inactive and is effectively disconnected from the circuit.

HTL (High-threshold logic) A form of bipolar logic circuit which is identical to DTL but has appreciably higher noise margins.

I^2L (Integrated-injection logic) A form of bipolar logic circuit that uses only bipolar transistors. It is an alternative form of DCTL.

Logic Swing The difference between the voltages corresponding to HIGH and LOW levels.

LSI (Large-scale integration) An IC chip containing logic circuits equivalent of 100 to 1000 gates or containing 1000 –10,000 transistors.

MOSFET (Metal-oxide-semiconductor field-effect transistor) A field-effect transistor consisting of a semiconductor substrate over which an oxide layer is grown and above the oxide layer a metalic layer is deposited which acts as the gate. If is also known as the insulated-gate FET (IGFET).

Merged-transistor logic (MTL) Same as the I^2L.

MSI (Medium-scale integration) An IC chip containing logic circuits equivalent of 13 to 99 gates or containing 100–1000 transistors.

Noise immunity A circuits ability to tolerate noise.

Noise margin A measure of the noise which can be tolerated by a logic circuit.

Noise-margin, high-level For a logic circuit, the difference between the minimum voltage that is produced at the output corresponding to logic 1 and the minimum voltage that is recognised as logic 1 of the input.

Noise-margin, low-level For a logic circuit the difference between the maximum voltage that is recognised as logic 0 at the input and the maximum voltage that is produced corresponding to logic 0 at the output.

Non-saturated logic A logic circuit in which the BJTs are not driven to saturation corresponding to ON state.

Open-collector output An output of a digital IC which is the collector terminal of a BJT not connected to any other point inside the IC.

Open-drain output An output of a MOS IC which is the drain terminal of a MOS device not connected to any other point in the IC.

Open-emitter output An output of an ECL IC which is the emitter terminal of a BJT not connected to any other point in the IC.

Passive pull-up A resistance used to pull-up the output voltage of a logic circuit from LOW to HIGH in response to appropriate inputs.

Pull-up resistor A resistor connected between the output (collector or drain of a transistor) and the supply voltage (V_{CC} or V_{DD}).
Saturated logic A logic circuit in which the BJTs are driven to saturation corresponding to ON state.
Schottky TTL The TTL circuit in which each BJT is replaced by a Schottky transistor.
SSI (small-scale integration) An IC chip containing circuits equivalent of upto 12 gates or 100 transistors.
Three-state gate (tristate gate) A gate having a 1, 0, or high-impedance output states.
Tristate output An output of a logic circuit having 1, 0, or high-impedance states.
Totem-pole output Same as the active pull-up.
TSL (Tristate logic) Same as tristate output.
TTL (Transistor-transistor logic) A form of bipolar logic circuit that uses transistors to realize the logic operations.
Unipolar logic Logic circuits using only MOS devices.
VLSI (Very large-scale integration) An IC chip containing logic circuits equivalent of above 1000 gates or above 10,000 transistors.
Wire-ANDing Tying the outputs of two or more gates together to perform additional logic. Also known as Wired-Logic.

Review Questions

4.1 A logic family using BJTs is known as _____ logic family.
4.2 A unipolar logic family uses only _____ devices.
4.3 Figure of merit of a digital IC is given by _____.
4.4 The number of similar gates which a gate can drive is known as its _____ .
4.5 Fan-in signifies the _____ of a gate.
4.6 A TTL gate is driving another TTL gate. The output transistor of the driver gate is driven _____ into saturation when its output is at low level.
4.7 For interfacing logic gates V_{OH} must be _____ than V_{IH}.
4.8 Outputs of TTL gates with active pull-up must _____ connected together.
4.9 Unconnected input terminal of a TTL gate behaves as _____ .
4.10 The input terminal of a CMOS circuit must _____ .
4.11 Schottky TTL has _____ propagation delay time than TTL.
4.12 The temperature range for 74-series ICs is _____ .
4.13 The states of a TSL are _____ .
4.14 TTL gates with _____ output can be used for wired-logic operation.
4.15 _____ is the fastest logic family.

Problems

4.1 In the RTL NOR gate of Fig. 4.4, calculate the average power supplied by V_{CC} to the driver gate when it is driving 5 gates. Assume $V_{BE,\,sat} \approx 0.8$ V, $V_{CE,\,sat} \approx 0.2$ V, $h_{FE} = 10$. Neglect leakage currents.

4.2 In the circuit of Fig. 4.4, calculate
- (a) Output voltage V_O and noise margin $\Delta 1$ for $N = 5, 6, 7, 8, 9, 10$. Assume $h_{FE} = 10$.
- (b) Repeat (a) for $h_{FE} = 20$.
- (c) Comment on the effect of h_{FE} on the fan-out and noise margin of circuit.
- (d) Comment on the effect of N on the noise margin for a given h_{FE}.

4.3 In the circuit of Fig. 4.6, the fan-out of RTL NOR gates P and Q is 5 each.
- (a) Calculate the fan-out of the combined gate.
- (b) Evaluate the propagation delay time constant and power dissipation, and comment on the effect of wired-logic on these.

4.4 A buffer is used to increase the output drive capability of a logic circuit. An RTL buffer inverter is shown in Fig. 4.37.
- (a) Explain the operation of this circuit.
- (b) Calculate the fan-out. Assume $h_{FE} = 30$.
- (c) Consider outputs of two such buffers A and B connected in parallel. Let the input to buffer A be logic 1 and the input to buffer B be logic 0. Calculate the current flowing in T_3 of buffer A.

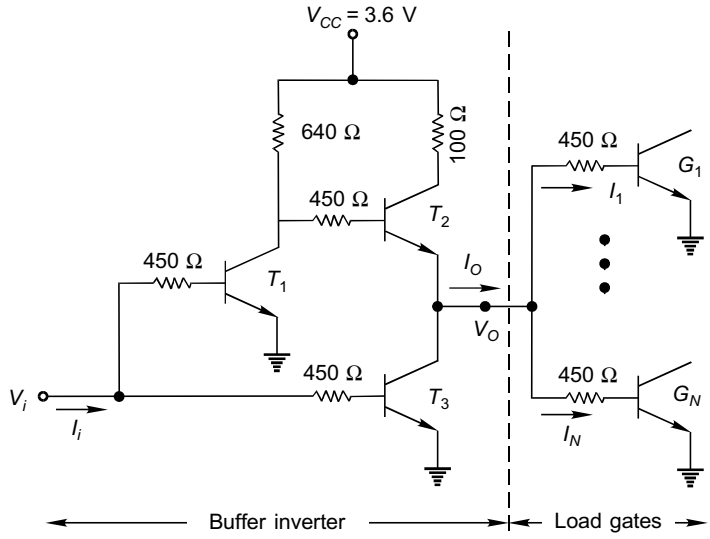

Fig. 4.37

An RTL buffer inverter driving N RTL gates.

4.5 What will happen in the DTL circuit of Fig. 4.12 if
- (a) one of the diodes D_1 or D_2 is removed,
- (b) one more diode D_3 is inserted in series with D_1 and D_2.

4.6 Calculate the value of h_{FE} required for a fan-out of 10 in the DTL gate of Fig. 4.12.

4.7 M DTL gates (Fig 4.12) each with a fan-out of N are connected in a wired-AND connection. Determine the fan-out of this combination as a function of number M.

4.8 In the modified DTL NAND gate of Fig. 4.14, show that when T_1 is conducting it is in its active region and not in the saturation region.

4.9 Explain the operation of the modified DTL gate of Fig. 4.14 and calculate its (a) fan-out (b) noise-margins, and (c) average power dissipation. Assume $h_{FE} = 30$.

4.10 Calculate (a) noise-margins, (b) fan-out, and (c) power dissipation of HTL gate of Fig. 4.15. Assume $h_{FE} = 40$.

4.11 Repeat Problem 4.7 for the HTL gate shown in Fig. 4.15.

4.12 Explain why the temperature sensitivity of HTL is significantly better than that of DTL.

4.13 In the TTL NAND gate of Fig. 4.17 determine the current drawn from the supply, when the output
(a) is LOW
(b) is HIGH
(c) makes a transition from LOW to HIGH.

4.14 Consider the circuit shown in Fig. 4.38 which uses TTL gates. The current I is 1.6 mA when terminal B is left unconnected. Find the value of I when B is connected to A. Comment on the effect of this connection on the fan-out of gate G_1.

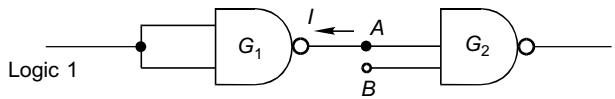

Fig. 4.38
Circuit for Problem 4.14.

4.15 In the TTL gate of Fig. 4.17, what happens if
(a) $R_{C4} = 0$,
(b) diode D is not present,
(c) the output accidently gets shorted to ground?

4.16 The outputs of two totem-pole TTL gates (Fig. 4.17) are connected as shown in Fig. 4.39. Obtain the current drawn from the supply for all the possible combinations of the inputs to the two gates.

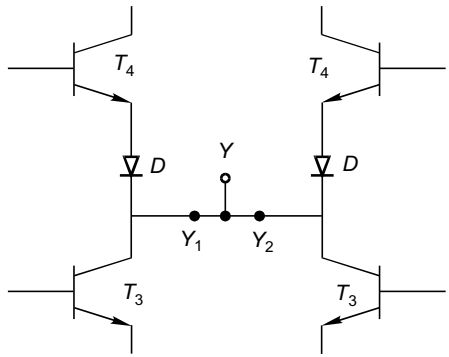

Fig. 4.39
Circuit for Problem 4.16.

4.17 For an open-collector TTL gate, the specifications are:

$$V_{OH} = 2.4 \text{ V}$$
$$V_{OL} = 0.4 \text{ V}$$
$$I_{OH} = 250\ \mu\text{A}$$
$$I_{OL} = 16 \text{ mA}$$
$$I_{IH} = 40\ \mu\text{A}$$
$$I_{IL} = -1.6 \text{ mA}$$

Calculate the value of R_C required for the open-collector gate. Assume $V_{CC} = 5$ V and a fan-out of 8.

4.18 If 5 open-collector gates of Problem 4.17 are wire-ANDed, and are loaded by similar 6 gates, calculate the value of collector resistor R_C required.

4.19 For an open-collector TTL, non-inverting buffer (7407) the specifications are:

$V_{OH} = 30$ V (maximum), $V_{IH} = 2.0$ V
$V_{OL} = 0.4$ V, $V_{IL} = 0.8$ V
$I_{OH} = 250\ \mu$A, $I_{IH} = 40\ \mu$A
$I_{OL} = 40$ mA, $I_{IL} = -1.6$ mA

If 7 such gates are wire-ANDed and drive 7 standard TTL gates of 74-series, determine the value of supply voltage V_{CC} and the collector resistor R_C to be used.

4.20 If it is desired to use a 10 V, 30 mA lamp as load in a digital circuit, can you use a 74-series TTL gate with (a) totem-pole output (b) with passive pull-up (c) open-collector output (specifications given in Problem 4.17), (d) open-collector buffer 7407?
In case your answer is yes, give the circuit arrangement and explain its operation.

4.21 Verify Table 4.4 using the specifications given in Table 4.3.

4.22 Consider the ECL circuit shown in Fig. 4.40. Here, V_n represents the noise. Calculate the noise component in the output taken between.
(a) Y and P terminals (b) Y and Q terminals
Hence justify the grounding of positive end of the supply voltage. Assume $h_{FE} = 100$.

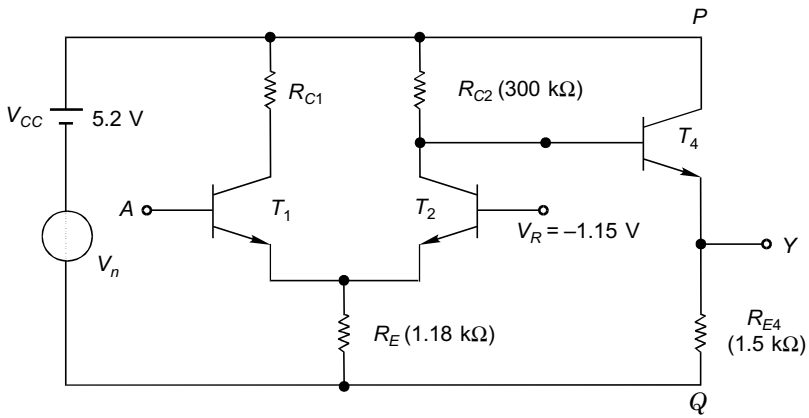

Fig. 4.40
Circuit for Problem 4.22.

4.23 (a) What will happen in the ECL gate of Fig. 4.19 if Y_1 or Y_2 accidently gets shorted to ground.
(b) Repeat part (a) if negative end of the supply is grounded.

4.24 Compare the current spikes in ECL and TTL gates.

4.25 Verify the operation of wired-OR connections of ECL gates shown in Fig. 4.21.

4.26 Prove that the input of MC10H125 IC is ECL compatible and its output is TTL compatible.

4.27 Design a circuit for interfacing an ECL 2-input NOR gate with a TTL inverter to obtain NOR function of the combined circuit.

4.28 What happens if output accidently gets shorted to ground in
(i) NMOS? (ii) CMOS?

4.29 Explain the operation of CMOS NOR gate of Fig. 4.28.

4.30 Find the fan-out of each of the 74 TTL series driving 74 HC/74 HCT/74 AC/74 ACT gates using the specifications given in Tables 4.3 and 4.9.

4.31 Consider a CMOS gate driving TTL gates. Find the fan-out when
(a) 74HC/74HCT gate is driving each of TTL series gates.
(b) 74AC/74ACT gate is driving each of TTL series gates.

4.32 A 74AC/74ACT gate is driving twenty 74AS gates. It is desired to drive some 74ALS gates in addition to this. Find the maximum possible number of 74ALS gates which can be connected.

4.33 Is it possible to use TTL-to-ECL translator for CMOS-to-ECL interfacing? Justify your answer.

4.34 Is it possible to use ECL-to-TTL translator for ECL-to-CMOS interfacing? Justify your answer.