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BRAC UNIVERSITY
Department of Computer Science and Engineering

Examination: Quiz
Duration: 35 minutes

Semester :Summer 2022
Full Marks: 15

CSE 360: Computer Interfacing

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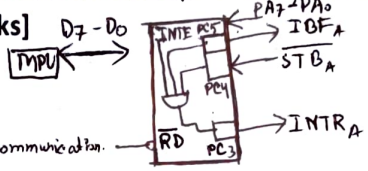
1. **(CO3)** Suppose, the interfacing IC is configured with the control bits "1011X01X". If the device connected to **Port A** is having data communication with Microprocessor, **explain** the step by step process using the timing diagram. **[5 Marks]**



Port A: mode 1, input device
Port B: mode 0, input device

Data communication with port-A will be input communication. Input will come ~~to port~~ from port A to CPU.

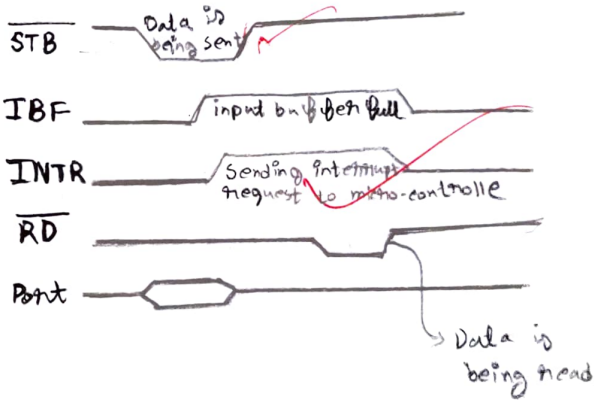
PA7 - PA0 ⇒ Data is coming from input through this pins

IBF = Input buffer full

$\overline{STB}$ = Strobing signal,

INTR = Interrupt request

1. Device will give input to 82C55: $\overline{STB}$ = 0, meaning data is being sent through PA7 - PA0.
2. When input buffer full, IBF = 1 to the device meaning that input buffer is full. then, $\overline{STB}$ = 1, disableing it; halting data communication.
3. 82C55, interrupt CPU through $INTR_A$, letting it know that input buffer is full, can it be read? INTR = 1.
4. CPU's free time, A_0 = 0, A_1 = 0, activating port A the $\overline{RD}$ = 0, $\overline{WR}$ = 1, Read the data stored.
5. After reading the data, $INTR_A$ = 0, IBF = 0, And if there is new data then the whole process repeat, $\overline{STB_A}$ = 0 data is being sent.



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2. **(CO3)** For which **mode** the outputs are latched and inputs are buffered of the I/O devices? **Explain** the reason briefly. **[3 Marks]**

When the device is in mode0 (Low level device is connected to the 82C55) then the outputs are latched and inputs are buffered.

When a low level I/O device, suppose led, buzzer, switch is connected to 82C55, then it is mode0. In this mode outputs are latched, it means that when cpu gives it output or try to write on the device connected to port, then outputs are being latched to maintain the output as it is. Latch is a digital IC whic holds data put into it. 1's remain 1's

until cleared. Thus, when a output of cpu arrives at the device, that is being stored at the latch. Thus, ~~cpu~~ latch regulates the output. CPU can clear the data through clear wire or can give opposite input. This is how, a output is being stored and showed to us.

Inputs are buffered, because, when input arrives it stays in the buffer of 82C55. CPU is not always free. So in the meantime the data needs to be stored. When low level device give analog input, buffer makes that input noise less or cancels some noise, also modify the input as the cpu wants. This way input and cpu's data communication is being synchronized.

So, we can say that, inputs are buffered to maintain synchronization of the data communication and outputs are latched so that it can show output continuosly (until cleared) in low level device (mode 0).

3. (CO3) Suppose, the interfacing IC is configured with the control bits "0xxx1011". **Explain** the ports mode and type of device connected to the IC. **[3 Marks]**

0	x	x	x	1	0	1	1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

$D_7 = 0$, so the ic is in bit set/reset mode.

$D_6 = x$, $D_5 = x$ } Port A has no device connected to it

$D_4 = x$ } Port A " " " " " "
Hence, port A's device has no input/output type

$D_3 = 1$, $D_2 = 0$, $D_1 = 1$ } A low level device is connected to Port-C's 5 No. Pin

$D_0 = 1$, Set mode

Port A, B does not work in bit set reset mode. Only port-C (low level device) can work in bit set-reset mode

(Ans)

4. Suppose, the Port A of 82C55 is connected with a hard drive. Now, which of the following statement is true?

a) Port B can be configured for Mode 1 or Mode 0
b) Port C pins 6 and 7 can work as I/O
c) Port B can only be configured for Mode 1
d) Port C pins 4 and 5 can work as I/O

5. Suppose you have connected an Ipad to port-A and a printer to port-B. How many pins from port-C can you use for I/O?

a) 2 b) 0 c) 3 d) 5

6. Suppose, a printer is connected to Port A and a scanner is connected to Port B of 82c55. What is the control bit that has configured the 82C55?

a) 1010X11X b) 0011010X
c) 100110101 d) 1101X10X

7. Which pins are used to transfer data from the Data Bus Buffer to the Microprocessor?

a) PA0 - PA7 b) WR0 - WR7
c) D0 - D7 d) PC0 - PC7