

## CSE360 ASSIGNMENT

(2)

Name: Kazi Md. Al-Wakil

ID: 19301051

Section: 2

## Answer to the gues No. -1

(a)

A keyboard is connected to post-A. So, Post-A is in mode-1 as keyboard is high level unidinectional device, input device.

Similarly, a monitor is connected to Pont-B. So, pont-B is in mode-1 as moniton is a high level output (wildirectional) device.

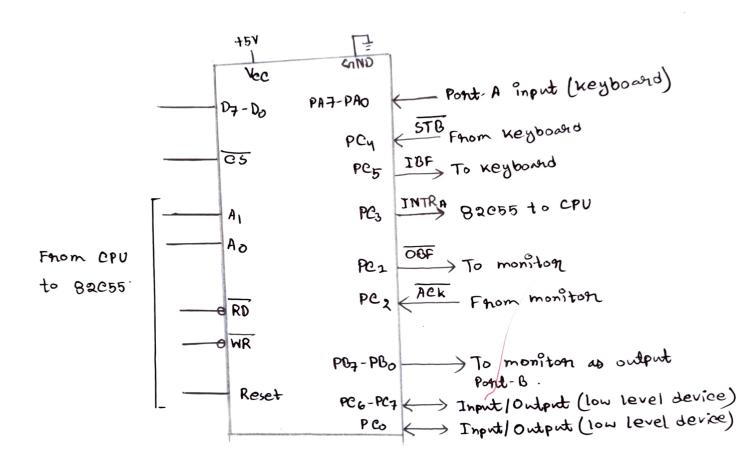
Now control bits to configure 82055 IC are:

D7	Do	05	Dy	D3	D2	D2	Do
1	O	1	1	110	1	O	2/0
Ilo mode	Pont-Ain Pont input of the second sec		Pont-A input	PCG, PC7,  1=input  0:0ulput  PCG, PC7,  ore  Gen conn  with lov  level de	in mode	Pont-B 1 Oudput	PCO is sow free. Can connect with low level device input=1 output=0

This is the control bits to configure the

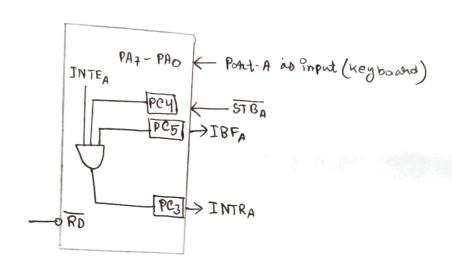
82C55 IC.

Diagnam of configured 82C55 IC:



Here, we can see the block diagram of give

Scenasio.



When we prossed (B) on keyboard,

O'B' key's ASCII value came as imput to PAZ-PAO.

DAt the same, the STBA will have 'O' (active low). This means that, with this stander signal, keyboard is letting the IC know that it's sending data. PCH pin does the work.

3 The data sent if nom keyboard is now at the builder, waiting to be processed by CPV

DAs, the 8-bit data bus builten gets full, it sends a signal to 8205 keyboard. It's a acknowledgement signal. By this signal keyboard knows that the IC necesives the signal and the data bus builten is that, also, we can not give any input now. The data stoned in builten has to be processed before getting any new data. Ic gives the signal through DC5, it's a IBFA signal. It states that input builten full'. As it is active high, to be enable, '1' will be passed.

- (5) At the same time, when IBF signal is '1', STB must cause when the builden is thul, input device can not give any input so STB will '1' (active low)
- © IC communicates with the micho-controller through PC3 pin.

  An Inter Interrupt signal is being sent to the micho-controller;

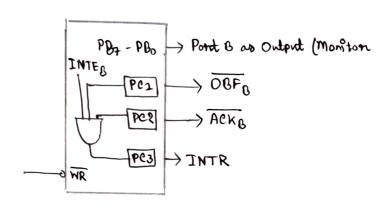
  This interrupt signal checks of the micho-controller is

  there to head the data. A high value (1) is sent to the micho-controller.
- Then, micho-controller is shee, he wit understands by looking at the Internupt signal that, a data is heady to be nead. Then sets A170, A070, it selects port A.
- (B) RD = 0, enables nead pin, WR = 1, disables write pin.
- O once micho-controller reads the data. IBF signal to disabled. And the whole process starts again.

Timing d	Jagham:
ङाष्ठ	(Data strobed Pato pont)
IBF	(Buffen Bull)
INTR	(Internupt neguest)
RD	Data nead by michophocesyn
٥.,	

9

To see (B) in the monitor, the ne steps are given below:



Hene, PC3 pin used to send interrupt signal to moniton, the same pin also used by post A. When we have opposite types (Input and output) on post A and in post B, then we can use I pin to send interrupt signal. It's ensures that there is no enrose. Only inputs will be on only sulput interrupt signals can pads.

DINTR signal will be high. INTR => 1. this signal is sent microphs to check in any data is available to show.

Description acknowledging that an output derice is connected to the IC, CPV enables when o and Ao = 1,A1 = 0, selects part B'. Sends data from Do-D7. Thus, enabling white pin allows the microphocesson to white to the output device which is connected to the post B.

The data sont by the cpu stones in the bullen. And Hat the sometime INTR ⇒0. Cause data bus bullen is thall and no new data is needed from cpu.

- (9) 82055 sends 'Ordpid buffer that' signal to the monitor
- 6) When the moniton is free, it sends an acknowledgement signal to the 82055. ACKB =>0
- © Stoned data from data bus builden is now sent point B and to moniton. Then,  $\overline{OBFB} \Rightarrow 1$ , as output builden is empty aften whiting the data to the output device. Also,  $\overline{ACKB} \Rightarrow 1$ .

INTR >1.

Thus we can see B' In the moniton.

## Timing diagram: NR OBFO (Buffer cfull) INTR (Internupt Respuest) ACKB Data nemoved from port/buffer

## Ans. to the gues. No. 2

(0)

Criven that,

An Ipad to post A of 82c55 PPI, So, post-A is operating in mode 2 as Ipad is a high level di-dissectional device:

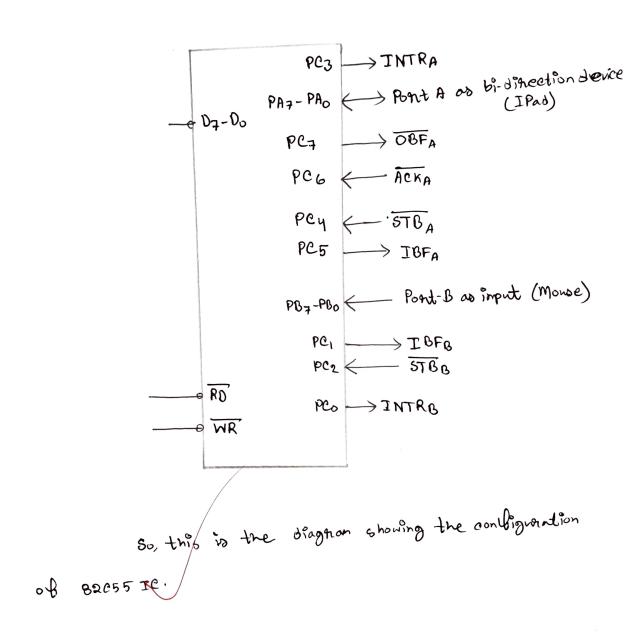
A mouse to post B. Post B is operating in mode 1.

As mouse is a high level input device (unidirectional)

Now, control world by which 82055 should be configured.

Day	De	05	Dy	03	D2	D1	Do
1	1	X	×	×	1	1	X
I/O mode	Pont in mo		SCPU can not determine input/output type orb bi-digrection device	handshaki	Pont-B in mode 1	Pont-B input	Buoy with handshaking

So, this is the control word in which 82055 should be programmed.



Segnences and process that takes place between the 82055 and I pad is given below:

For initial configuration: A1>1, A0>1, RD>1, WR>0, Control bits>11×1×11×

- ① Alten tapping on scheen to send data to michaphocesson, 8 bit data will be passed through PAT-PAO. At the same 8 time  $\overline{518}_{A} \Rightarrow 0$ , enabling it means that data is being sent.
  - 2) When the builder is full, It waits for the CPV to process the data. Then, IBFA => 1, Indicating that builder is full, all data has been necesived and can not send more data. At the same time 5TBA => 1, disablar disabling the signal so that Ipad can not give more data.
    - 3) Then, INTRA  $\Rightarrow$  1, Indicating and asking the micro processon 9% it can take any data.
    - When CPU is Gree, it knows the device by looking at the intermupt signal, and gets neady to head data from the ipad. Sets  $A_1=>0$ ,  $A_0=>0$ , RD=>0, RD=>0.
    - 5) Once the cpu neads the data, IDFA => 0, disabling cause bullen is empty now. Fo

For a new data whole process repeats.

- Now, the device will show output:

  For initial configuration:  $A_1 \Rightarrow 1$ ,  $A_0 \Rightarrow 1$ ,  $R\overline{D} \Rightarrow 1$ ,  $W\overline{R} \Rightarrow 0$ , control bits  $A_1 \Rightarrow 1$ . Author processing the data, when the device is neady to show output,  $INTRA \Rightarrow 1$ . Checking if the cpu is heady to deliver output.  $PC_3$  pin is sending the signal.
- ② CPV, a liter acknowledgeing that ipad is connected and gready to show output. CPV stands to write data to the bubblest.  $\overline{WR} \Rightarrow 0$ ,  $\overline{RD} \Rightarrow 1 \cdot A_1 \Rightarrow 0$ ,  $A_0 \Rightarrow 0$ , thus selects post A. At the same time INTRA  $\Rightarrow 0$ , course data bus bubblest is full and no new data is needed.
- 3 OBFA => 0, 'ordered builten bull' signal to the Ipad. So, that Ipad knows that builten is bull and it can strong only ordered.
- 9 When Ipad is free, it sends an acknowledgement signal to the 82055. ACKA =>0
- 5) Storned data now being sent to the post A. And the output will be shown at the device. In the meantime,  $\overline{OBF_A} \Rightarrow 1$ , disablence disabling output bulben as it's empty. Also,  $\overline{ACK_A} \Rightarrow 1$ ,  $\overline{INTR_A} \Rightarrow 1$ .

For a new output to show, the whole process will be repeated.

Timing Diagnam:	
STBA (Dala strobed Parto post)	
IBFA Bullen Vull	7
INTRA (intennupt	1
RD	ead y CPU)
WR	(Data sent to point)
OBF <sub>A</sub>	(Carller)
ACKA	
Pont	
	(Data nomoved from ports)