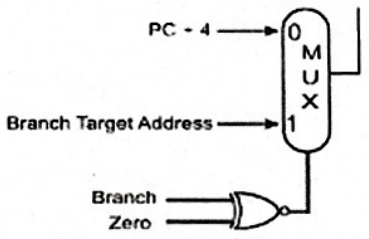
BRAC UNIVERSITY
Department of Computer Science and Engineering

Examination: ##
Duration: 90 minutes

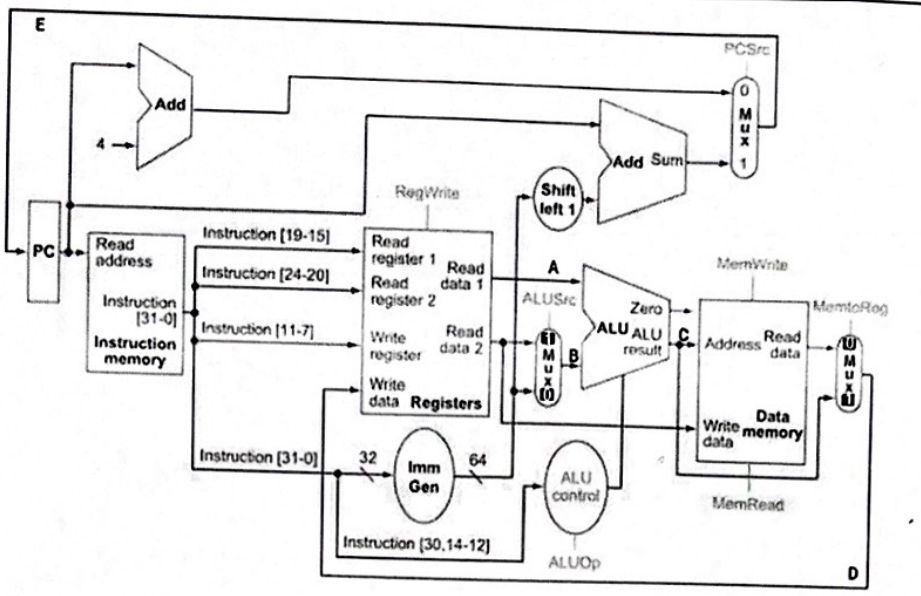
Semester: Summer24
Full Marks: ##

CSE 340: Computer Architecture

Name:	ID:	Section:

1	CO1	a.	**Convert** -111011.11011 x 2^{12} in 26-bit IEEE-754 format where, i. Size of the fraction field is 13 bits. ii. Size of the fraction field is 17 bits. **Show** the equivalent Hex representation of your conversions. iii. Suppose you plan to use the converted number in a subsequent calculation where precision is crucial. Given the choice between the two IEEE formats (with 13-bit and 17-bit fraction fields), which format would provide a more accurate conversion for your calculation?	3 3 2
		b.	i. **Multiply** 0.082 and 0.198 using IEEE-754 single precision floating point representation. ii. **Show** the status of the result (overflow or underflow or none). **Consider** 7 decimal digits when you are converting from decimal to binary.	3 1
		c.	**Subtract** -6.55 from 15.21 using IEEE-754 single-precision floating-point representation. **Consider** 5 decimal digits when you are converting from decimal to binary.	3
2	CO3	a.	Suppose that in a buggy implementation of the RISC V datapath, the AND gate for the branching decision was replaced with an **XNOR** gate. Describe how this error would affect the execution of the following instruction. i. **OR** x1, x2, x3 [3 points] ii. **BNE** x1, x2, target [3 points] 	3+3
		b.	**Design** a single cycle datapath with a control unit and control signals for the below instruction. BNE X_{10}, X_{21}, Label1	5

c.



5

Determine the values of the following control bits when executing the instruction "**Add** X21, X22, X23" and "BNE X23, X21, End" in the provided single-cycle datapath.

	Branch	ALUSrc	RegWrite	MemToReg	PcSrc
i.					
ii.					

d. The instructions provided below are executed sequentially within a **pipelined** datapath that is divided into five stages. **4**

Add X5, X6, X8
Sub X6, X5, X7
SD X6, 20(X5)
BEQ X6, X5, Loop
BNE X21, X5, END

Will any data hazards occur during the execution of this instruction set? If so, identify the number of data hazards and clearly circle them.