課題10-2

プログラム

function.v

```
module kadai10_2(
    input a,b,c,
    output z
);

    function MDC;
        input a,b,c;
        MDC = (a & b) | (b & c) | (c & a);
    endfunction

    assign z = MDC(a, b, c);
endmodule
```

実行結果

```
VCD info: dumpfile gate3_test.vcd opened for output.
a = 0, b = 0, c = 0, z = 0
a = 0, b = 0, c = 1, z = 0
a = 0, b = 1, c = 0, z = 0
a = 0, b = 1, c = 1, z = 1
a = 1, b = 0, c = 0, z = 0
a = 1, b = 0, c = 1, z = 1
a = 1, b = 1, c = 0, z = 1
a = 1, b = 1, c = 1, z = 1
```

課題10-4(1)

プログラム

mux4.v

```
module kadai10_4_1 (
    input [1:0] s,
    input [7:0] a,b,c,d,
    output [7:0] z
);

    function [7:0] mux4;
        input [1:0] s;
        input [7:0] a,b,c,d;
        if (s == 2'b00)      mux4 = a;
        else if (s == 2'b01) mux4 = b;
        else if (s == 2'b10) mux4 = c;
        else if (s == 2'b11) mux4 = d;
    endfunction

    assign z = mux4(s, a, b, c, d);
endmodule
```

実行結果

```
a: 00000000
b: 00001111
c: 11110000
d: 11111111
s: 00 z: 00000000
s: 01 z: 00001111
s: 10 z: 11110000
s: 11 z: 11111111
```

課題10-4(2)

プログラム

mux4.v

```
module kadai10_4_2 (
    input [1:0] s,
    input [7:0] a,b,c,d,
    output [7:0] z
);

    function [7:0] mux4;
        input [1:0] s;
        input [7:0] a,b,c,d;
        case (s)
            2'b00: mux4 = a;
            2'b01: mux4 = b;
            2'b10: mux4 = c;
            2'b11: mux4 = d;
        endcase
    endfunction

    assign z = mux4(s, a, b, c, d);
endmodule
```

実行結果

```
a: 00000000
b: 00001111
c: 11110000
d: 11111111
s: 00 z: 00000000
s: 01 z: 00001111
s: 10 z: 11110000
s: 11 z: 11111111
```

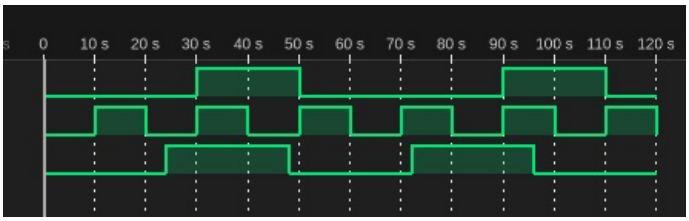
課題10-6

プログラム

dff.v

```
module DFF (
    input CK, D,
    output Q
);
    reg Q;
    always @(posedge CK) begin
        Q <= D;
    end
endmodule
```

波形



波形