

## 課題9-1

### 実行予想

```
1100
0010
0101
0010
1
1110
1000
0
0
01110101
0101
```

### 実行結果

```
1) 1100
2) 0010
3) 0101
4) 0010
5) 1
6) 1110
7) 1000
8) 0
9) 0
10) 01110101
11) 0101
```

## 課題9-5(1)

### プログラム

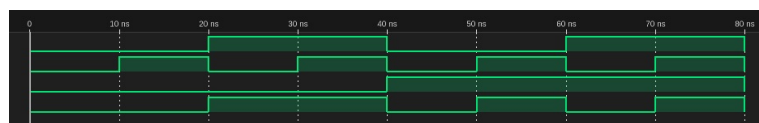
#### mux.v

```
module mux (  
    input a, b, s,  
    output y  
);  
assign y = s ? b : a;  
endmodule
```

#### main.v

```
`timescale 1ns/1ns  
module mux_test;  
    reg a, b, s;  
    wire y;  
    mux f(a, b, s, y);  
  
    initial begin  
        a = 0; b = 0; s = 0;  
        $dumpfile("main.vcd");  
        $dumpvars(0, mux_test);  
        $monitor("a=%b b=%b s=%b y=%b", a, b, s, y);  
  
        // Test cases  
        a = 0; b = 0; s = 0; #10;  
        a = 0; b = 1; s = 0; #10;  
        a = 1; b = 0; s = 0; #10;  
        a = 1; b = 1; s = 0; #10;  
        a = 0; b = 0; s = 1; #10;  
        a = 0; b = 1; s = 1; #10;  
        a = 1; b = 0; s = 1; #10;  
        a = 1; b = 1; s = 1; #10;  
        $finish;  
    end  
endmodule
```

### タイムチャート



波形

## 課題9-5(2)

### プログラム

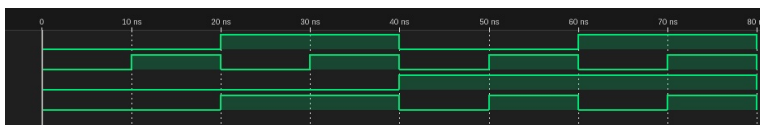
#### circuit.v

```
module my_mux (  
    input a, b, s,  
    output y  
);  
    wire sel_bar;  
    wire a_and, b_and;  
  
    not (sel_bar, s);  
    and (a_and, a, sel_bar);  
    and (b_and, b, s);  
    or (y, a_and, b_and);  
endmodule
```

#### main.v

```
`timescale 1ns/1ns  
module my_mux_test;  
    reg a, b, s;  
    wire y;  
    my_mux f(a, b, s, y);  
  
    initial begin  
        a = 0; b = 0; s = 0;  
        $dumpfile("main.vcd");  
        $dumpvars(0, my_mux_test);  
        $monitor("a=%b b=%b s=%b y=%b", a, b, s, y);  
  
        // Test cases  
        a = 0; b = 0; s = 0; #10;  
        a = 0; b = 1; s = 0; #10;  
        a = 1; b = 0; s = 0; #10;  
        a = 1; b = 1; s = 0; #10;  
        a = 0; b = 0; s = 1; #10;  
        a = 0; b = 1; s = 1; #10;  
        a = 1; b = 0; s = 1; #10;  
        a = 1; b = 1; s = 1; #10;  
        $finish;  
    end  
endmodule
```

### タイムチャート



波形

## 課題9-6(1)

### プログラム

#### circuit.v

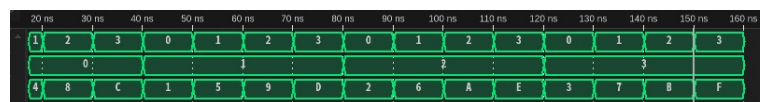
```
module kadai09_6 (  
    input [1:0] a,  
    input [1:0] b,  
    output [3:0] z  
);  
  
    assign z = {a, b};  
  
endmodule
```

### 実行結果

VCD info: dumpfile kadai09\_6\_test.vcd opened for output.

```
0: a = 00, b = 00, z = 0000  
10: a = 01, b = 00, z = 0100  
20: a = 10, b = 00, z = 1000  
30: a = 11, b = 00, z = 1100  
40: a = 00, b = 01, z = 0001  
50: a = 01, b = 01, z = 0101  
60: a = 10, b = 01, z = 1001  
70: a = 11, b = 01, z = 1101  
80: a = 00, b = 10, z = 0010  
90: a = 01, b = 10, z = 0110  
100: a = 10, b = 10, z = 1010  
110: a = 11, b = 10, z = 1110  
120: a = 00, b = 11, z = 0011  
130: a = 01, b = 11, z = 0111  
140: a = 10, b = 11, z = 1011  
150: a = 11, b = 11, z = 1111
```

### タイムチャート



波形

## 課題9-6(2)

### プログラム

#### circuit.v

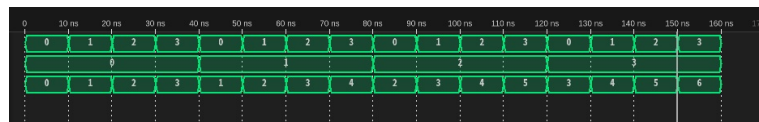
```
module kadai09_6 (  
    input [1:0] a,  
    input [1:0] b,  
    output [3:0] z  
);  
  
    assign z = {2'b00, a} + {2'b00, b};  
  
endmodule
```

### 実行結果

VCD info: dumpfile kadai09\_6\_test.vcd opened for output.

0:	a = 00, b = 00, z = 0000
10:	a = 01, b = 00, z = 0100
20:	a = 10, b = 00, z = 1000
30:	a = 11, b = 00, z = 1100
40:	a = 00, b = 01, z = 0001
50:	a = 01, b = 01, z = 0101
60:	a = 10, b = 01, z = 1001
70:	a = 11, b = 01, z = 1101
80:	a = 00, b = 10, z = 0010
90:	a = 01, b = 10, z = 0110
100:	a = 10, b = 10, z = 1010
110:	a = 11, b = 10, z = 1110
120:	a = 00, b = 11, z = 0011
130:	a = 01, b = 11, z = 0111
140:	a = 10, b = 11, z = 1011
150:	a = 11, b = 11, z = 1111

### タイムチャート



波形