課題10-2

プログラム

function.v

```verilog
module kadai10_2(
    input a,b,c,
    output z
);

    function MDC;
        input a,b,c;
        MDC = (a & b) | (b & c) | (c & a);
    endfunction

    assign z = MDC(a, b, c);
endmodule
```

実行結果

```
VCD info: dumpfile gate3_test.vcd opened for output.
a = 0, b = 0, c = 0, z = 0
a = 0, b = 0, c = 1, z = 0
a = 0, b = 1, c = 0, z = 0
a = 0, b = 1, c = 1, z = 1
a = 1, b = 0, c = 0, z = 0
a = 1, b = 0, c = 1, z = 1
a = 1, b = 1, c = 0, z = 1
a = 1, b = 1, c = 1, z = 1
```