Exp No.	Title	Date
S5	**Design of Half Adder and Full Adder circuits**	**9 Oct 2019**

Objective:

- To design and study the Half Adder and Full Adder circuits

Apparatus/Tool required:

ORCAD / Capture CIS → 7400 Library: 7486, 7408, 7432
Digclock

Simulation Settings:

Analysis Type – Time Domain
Run to time: 4ms (Half Adder)
8ms (Full Adder)

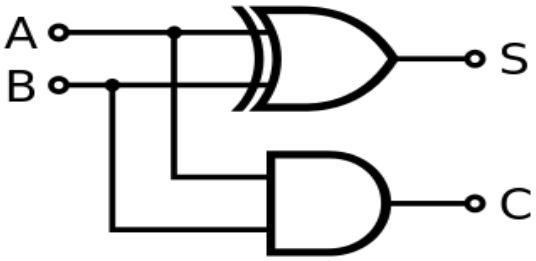
Theory:

A half adder is a type of adder, an electronic circuit that performs the addition of numbers. The half adder is able to add two single binary digits and provide the output plus a carry value. It has two inputs, called A and B, and two outputs S (sum) and C (carry). The common representation uses a XOR logic gate and an AND logic gate.

$$\mathbf{S = A \oplus B}$$

$$\mathbf{C = A \,.\, B}$$

A (Inp)	**B (Inp)**	**C (Out)**	**S (Out)**
0	**0**	**0**	**0**
0	**1**	**0**	**1**
1	**0**	**0**	**1**
1	**1**	**1**	**1**

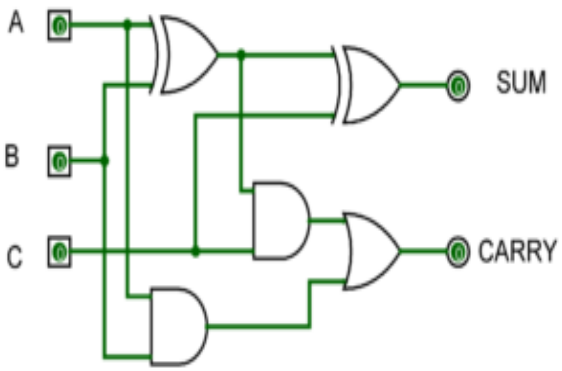


A full adder adds three one-bit binary numbers, two operands and a carry bit. The adder outputs two numbers, a sum and a carry bit. The term is contrasted with a half adder, which adds two binary digits. A full adder is effectively two half adders, an XOR and an AND gate, connected by an OR gate.

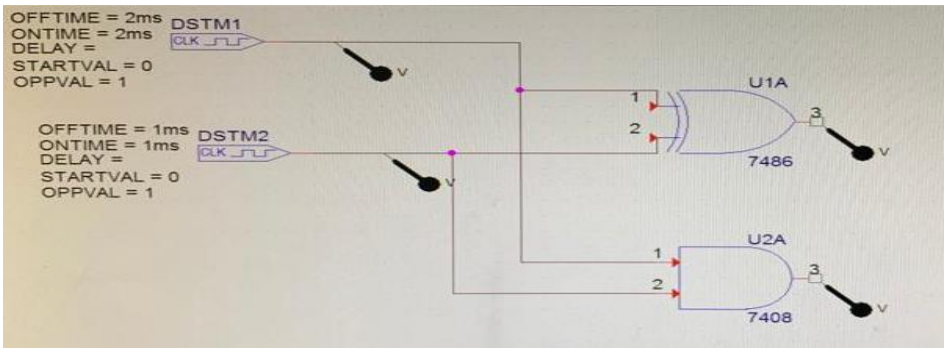
$$S = A \oplus B \oplus C$$

$$C = (A \oplus B).C + A.B$$

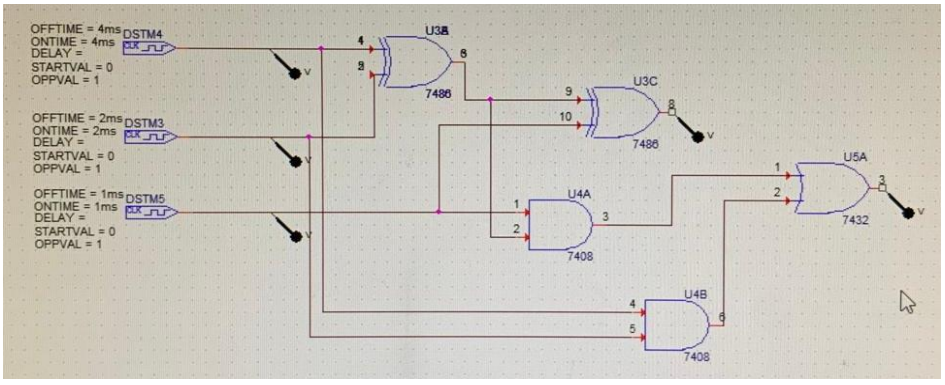
A (Inp)	B (Inp)	C (Inp)	C (Out)	S (Out)
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Circuit Diagram:



Half Adder

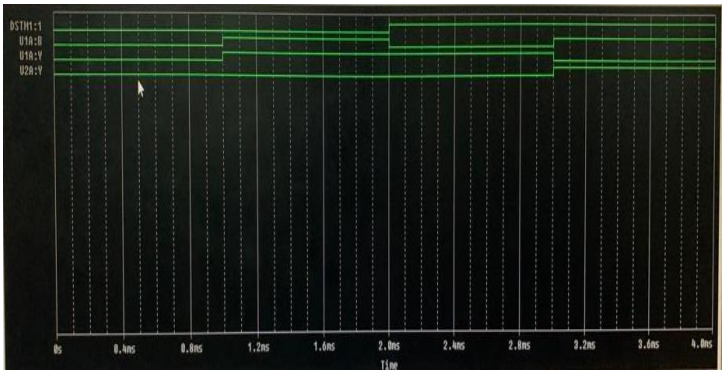


Full Adder

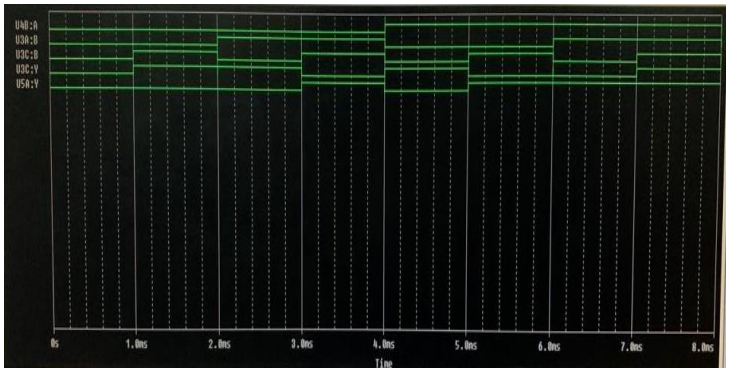
Procedure:

1. Create the given circuit diagram in new project file using the general procedure.
2. Replace the default component value and source value as per given circuit diagram.
3. Create the New simulation profile and set analysis type as Time Domain.
4. Run the simulation and observe the graphs.

Simulation Results:



Half Adder



Full Adder

Conclusion & Inference:

(i) Half Adder

When both inputs are low then Sum and Carry will be logic low (0), If any one of the inputs is high then Sum will be logic high (1) and Carry will be logic low (0). When both inputs are high then Sum becomes logic low (0) and Carry becomes logic high (1).

(ii) Full Adder

When all three inputs are low then Sum and Carry will be logic low (0), If any one input is high then Sum will be logic high (1) and Carry will be logic low (0). When two of the three inputs are high then Sum becomes logic low (0) and Carry becomes logic high (1). When all three inputs are high then, both Sum and Carry becomes logic high (1).

Reg. No.	Name	Marks
19BCE0811	AKSHAT SRIVASTAV	