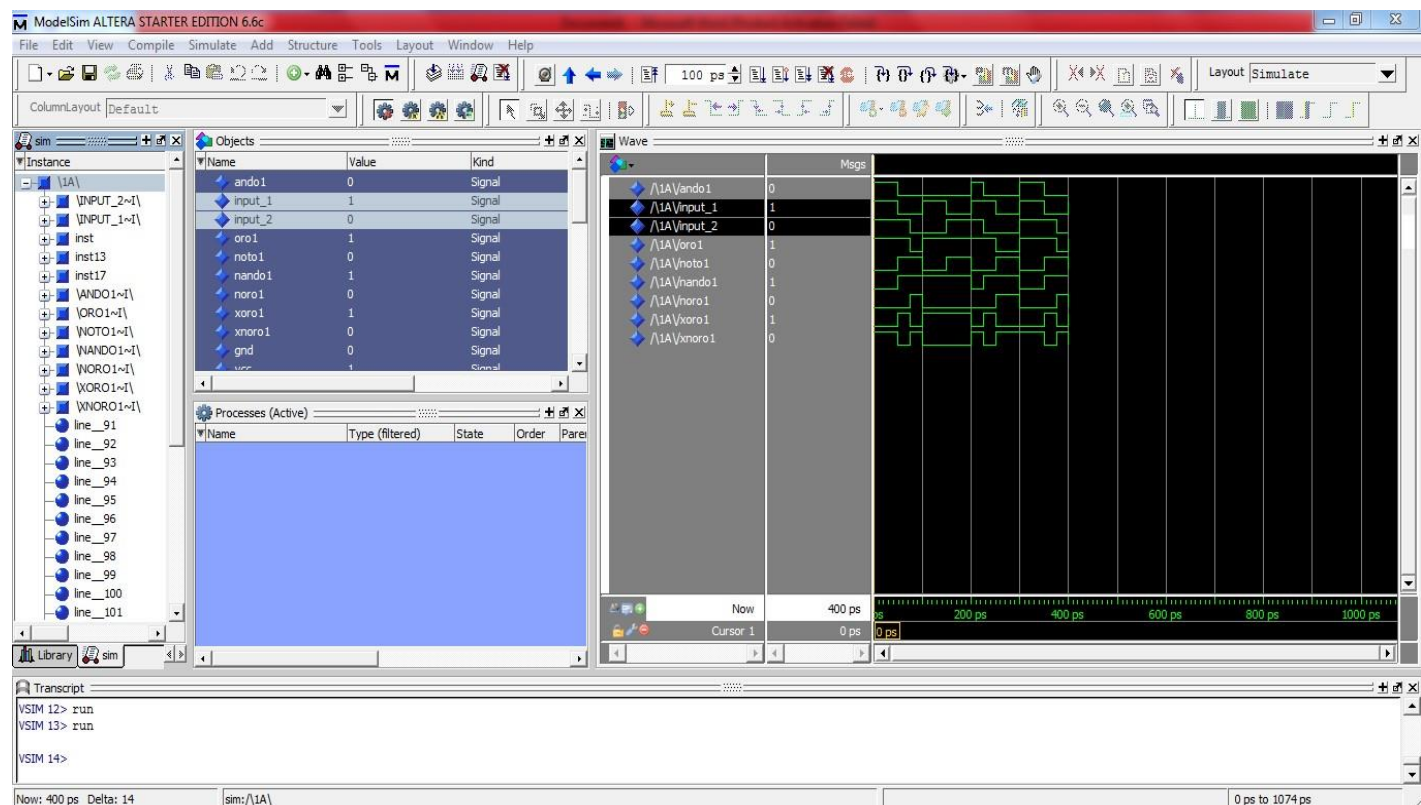
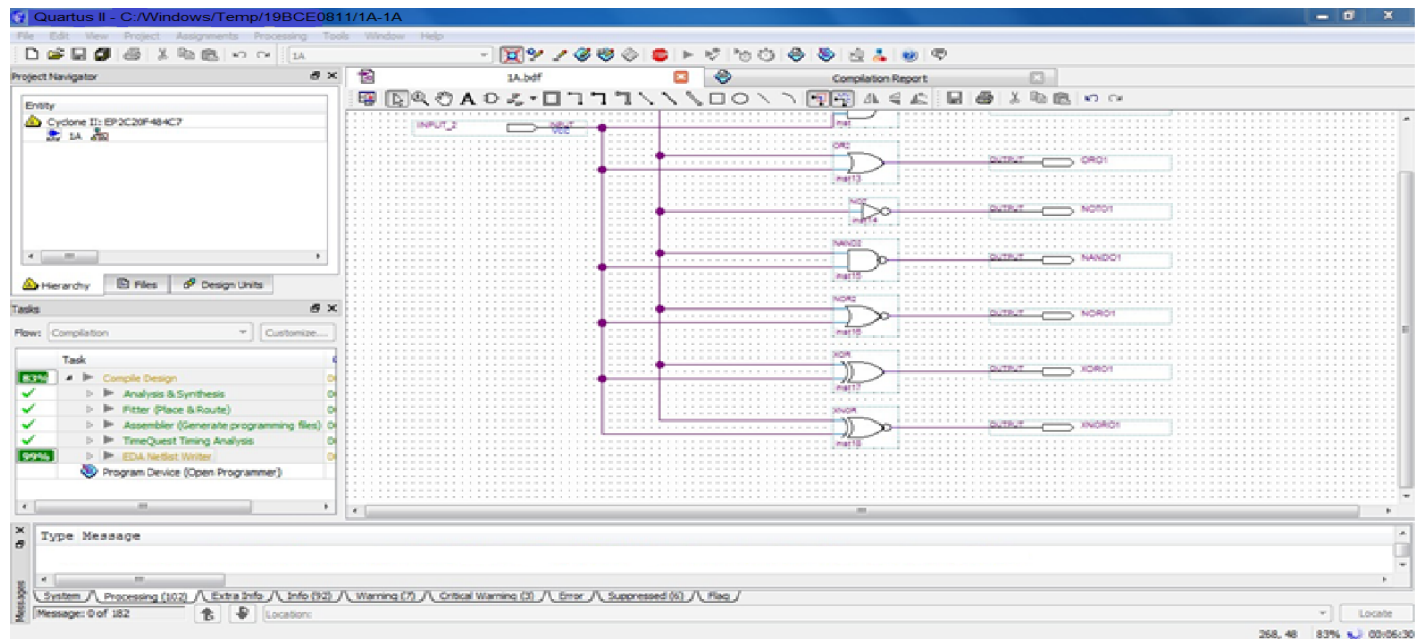
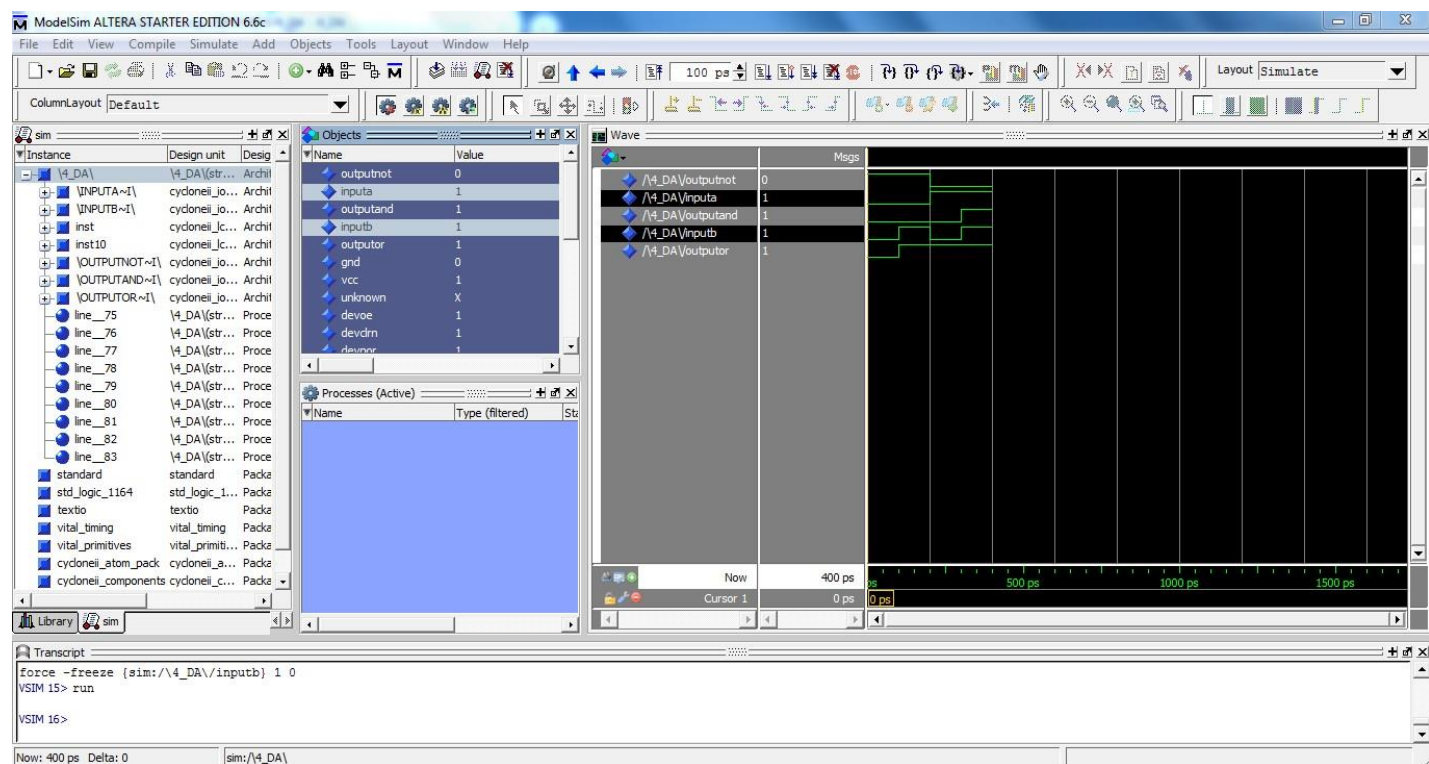
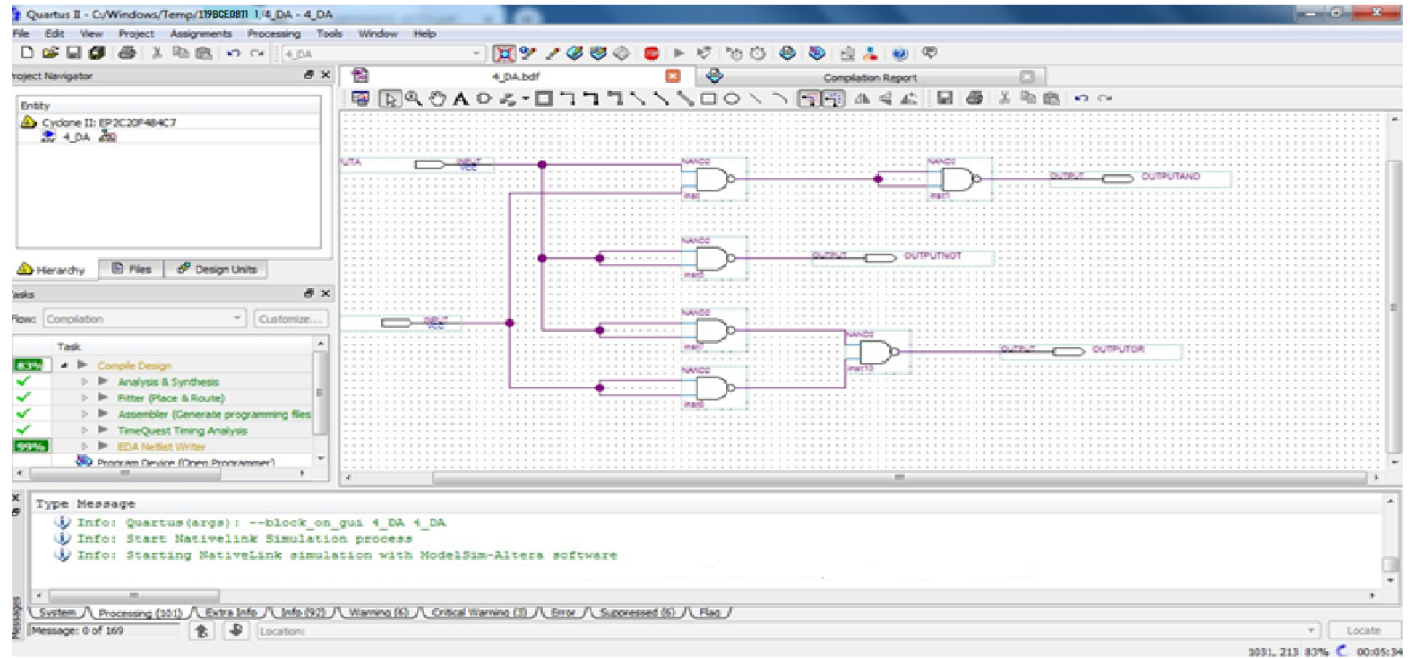


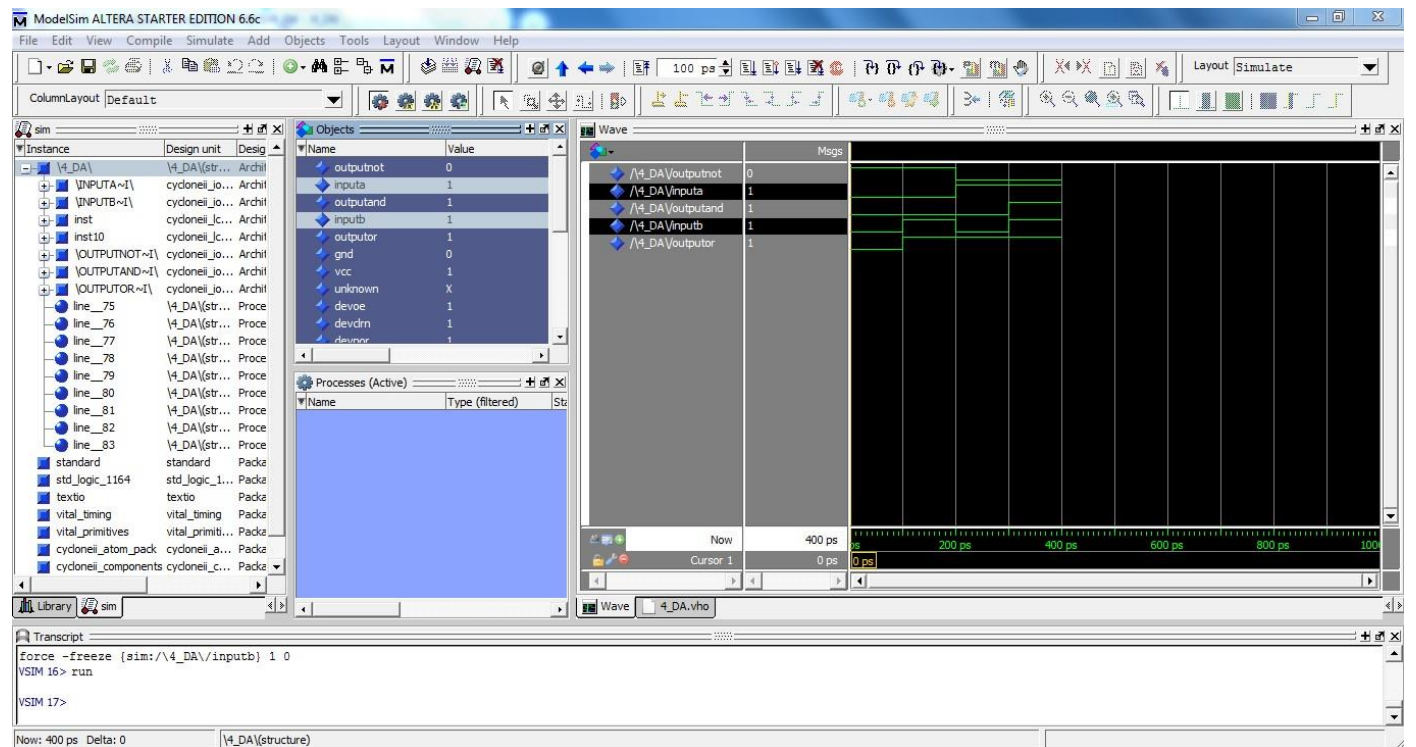
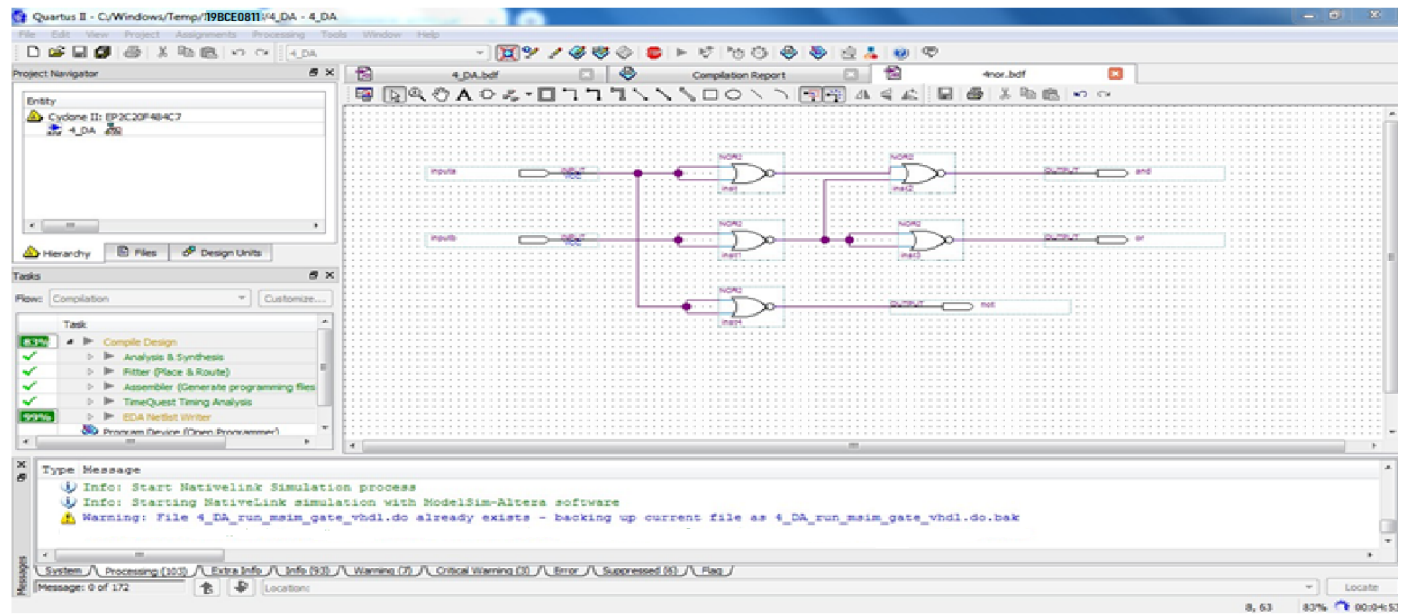
Q1,2,3) Displaying output for all types of basic gates



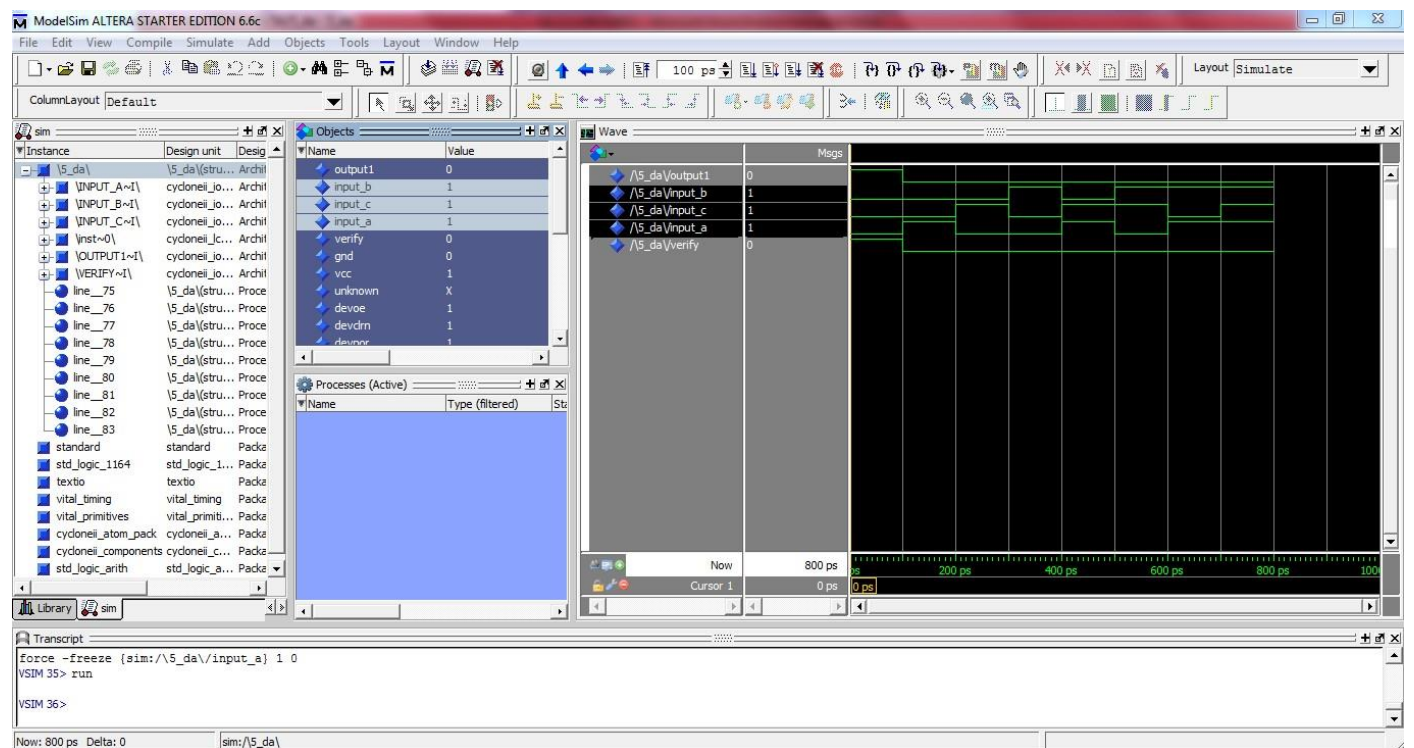
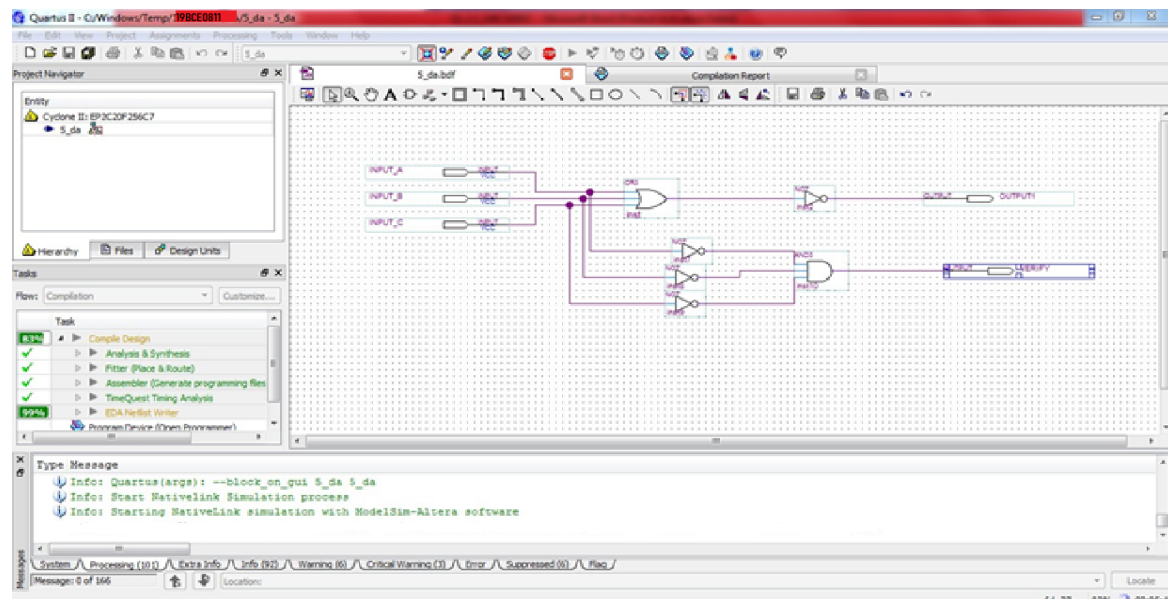
Q4) NAND as a universal gate to represent other gates



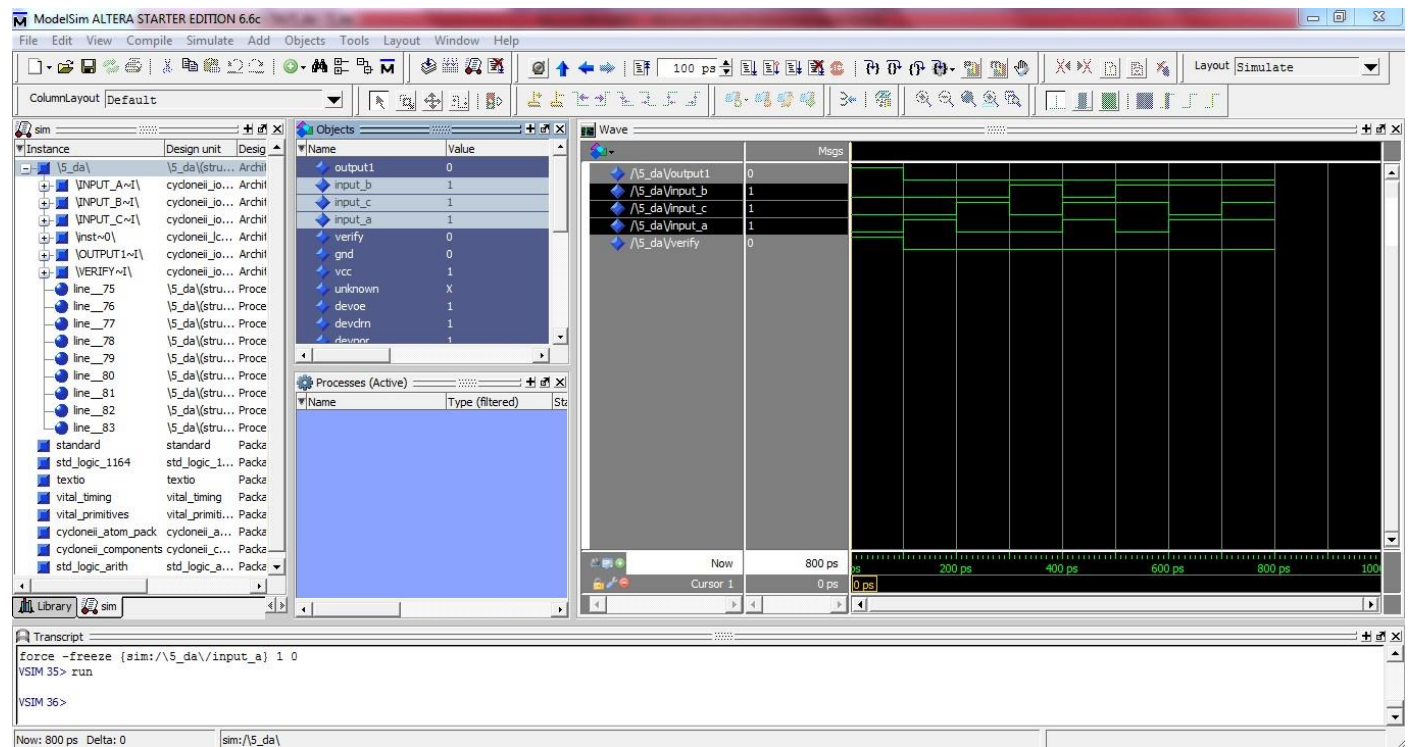
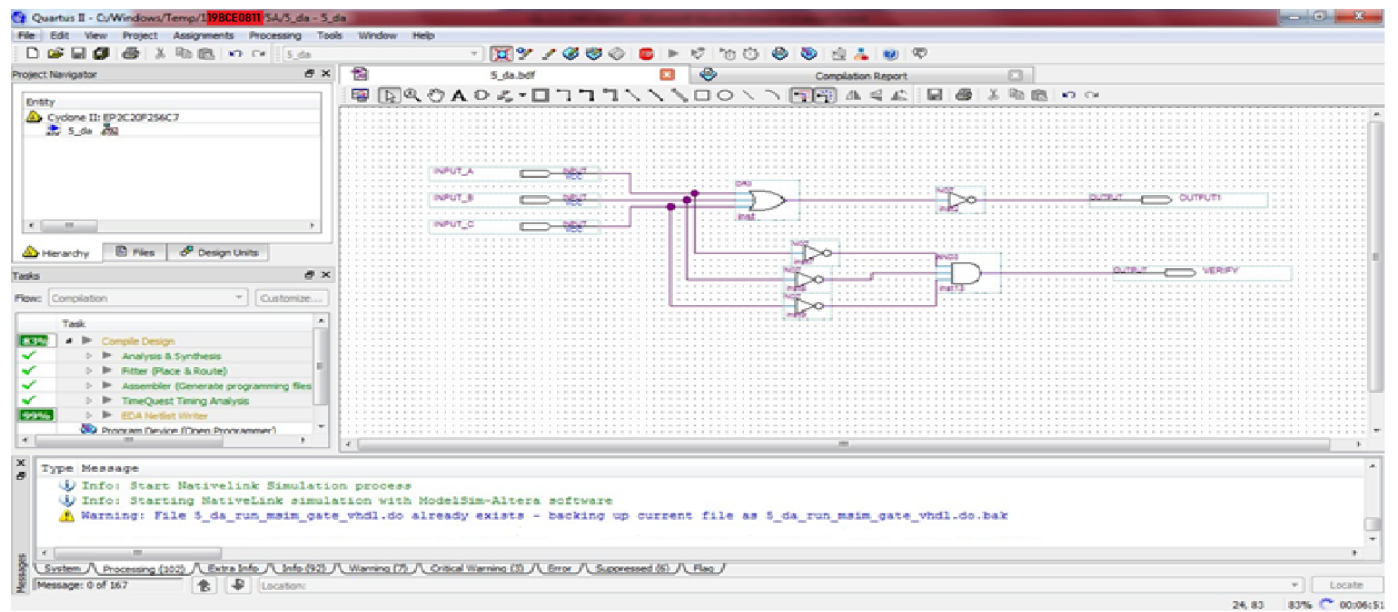
NOR as a universal gate to represent other gates



Q5) Displaying $(A+B+C)' = A'.B'.C'$ by gates



$$(A.B.C)' = A' + B' + C'$$



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