



McKelvey School of Engineering

Spring Semester 2023

CSE463M: Digital Integrated Circuit Design and Architecture

Final Assign #3 - Layout

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- * There are many parts to complete the Simplified DES.
- * Below is the list of all parts.

For basic operation

INVERTOR
NAND
XOR2
XOR4

For bit control

P10
P8
P4
SHIFT 1
SHIFT 3
EP
SWITCH
IP
IP Invert

For selection

2:1 mux
16:1 mux

For Enable

ENABLE

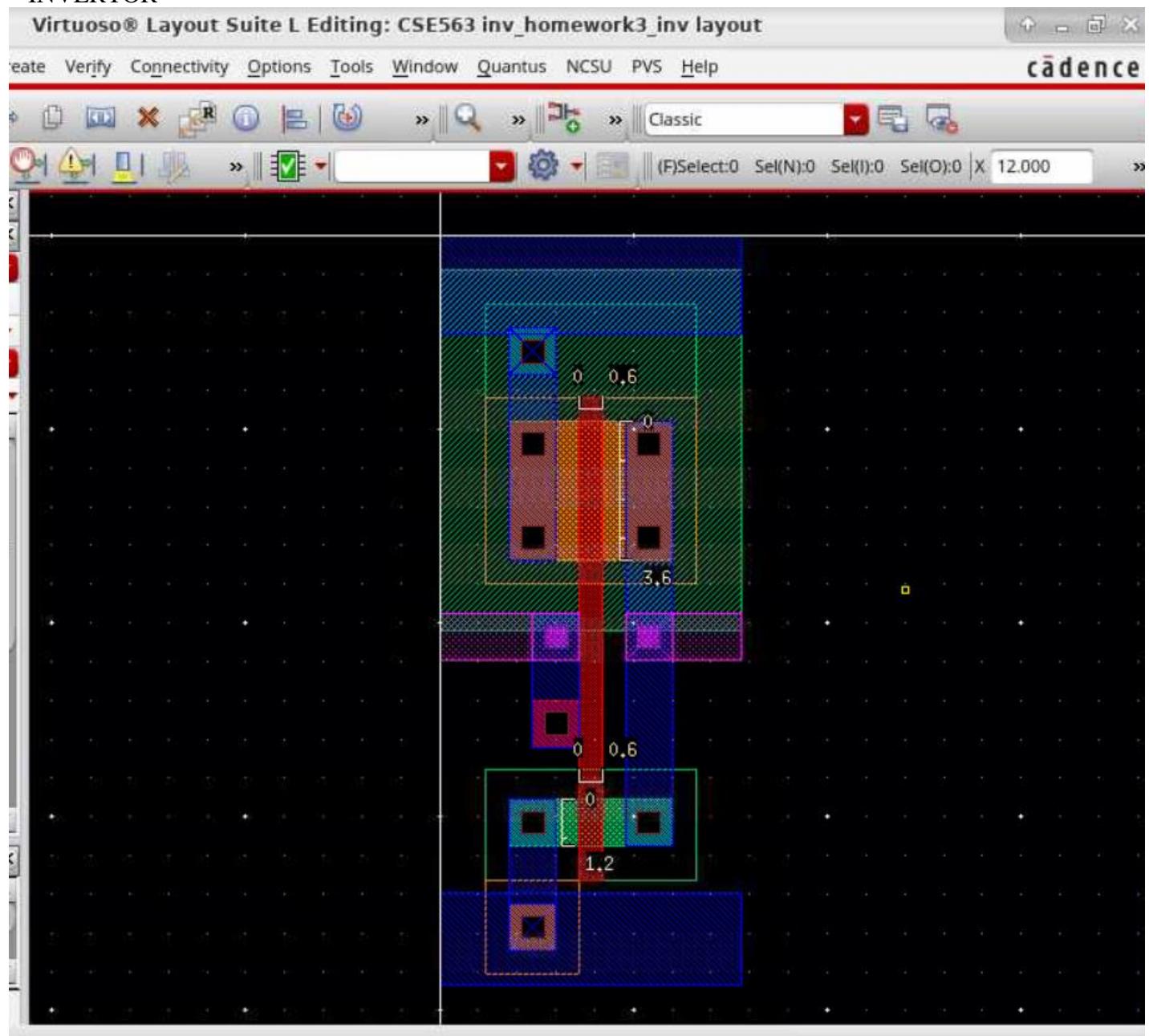
For CLK

D-LATCH
D Flip flop

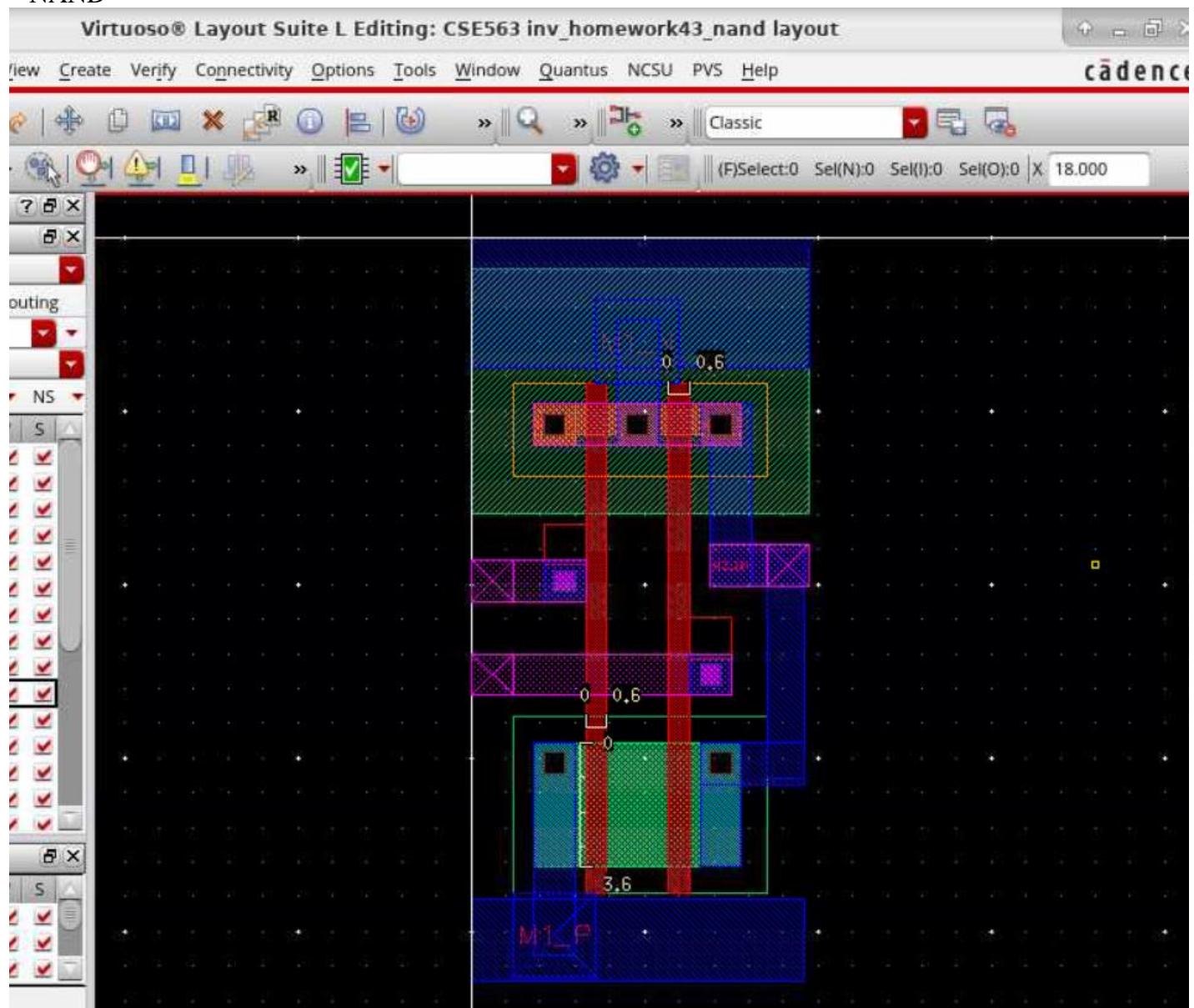
For SBox

SBox Red
SBox Green

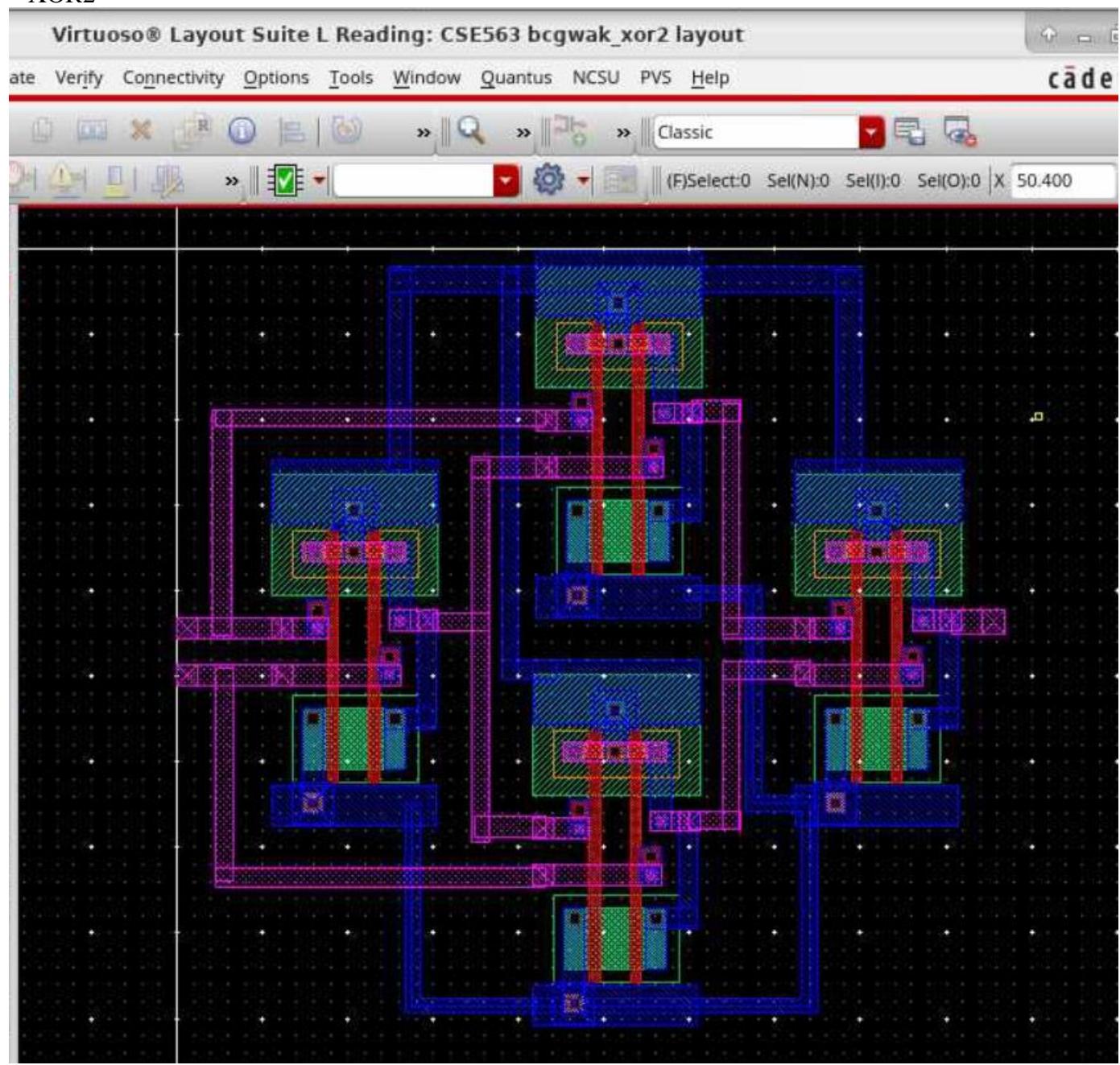
* INVERTOR



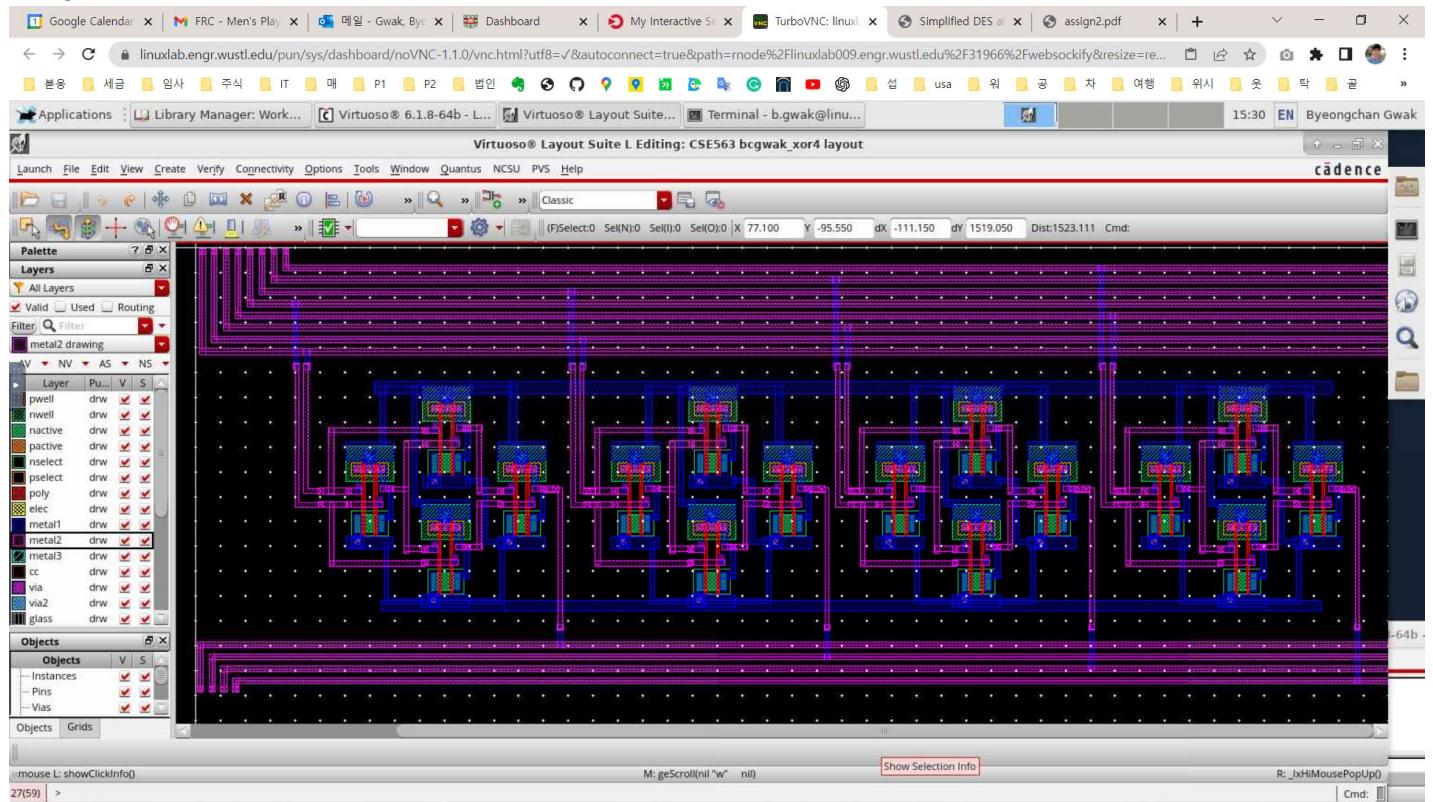
* NAND



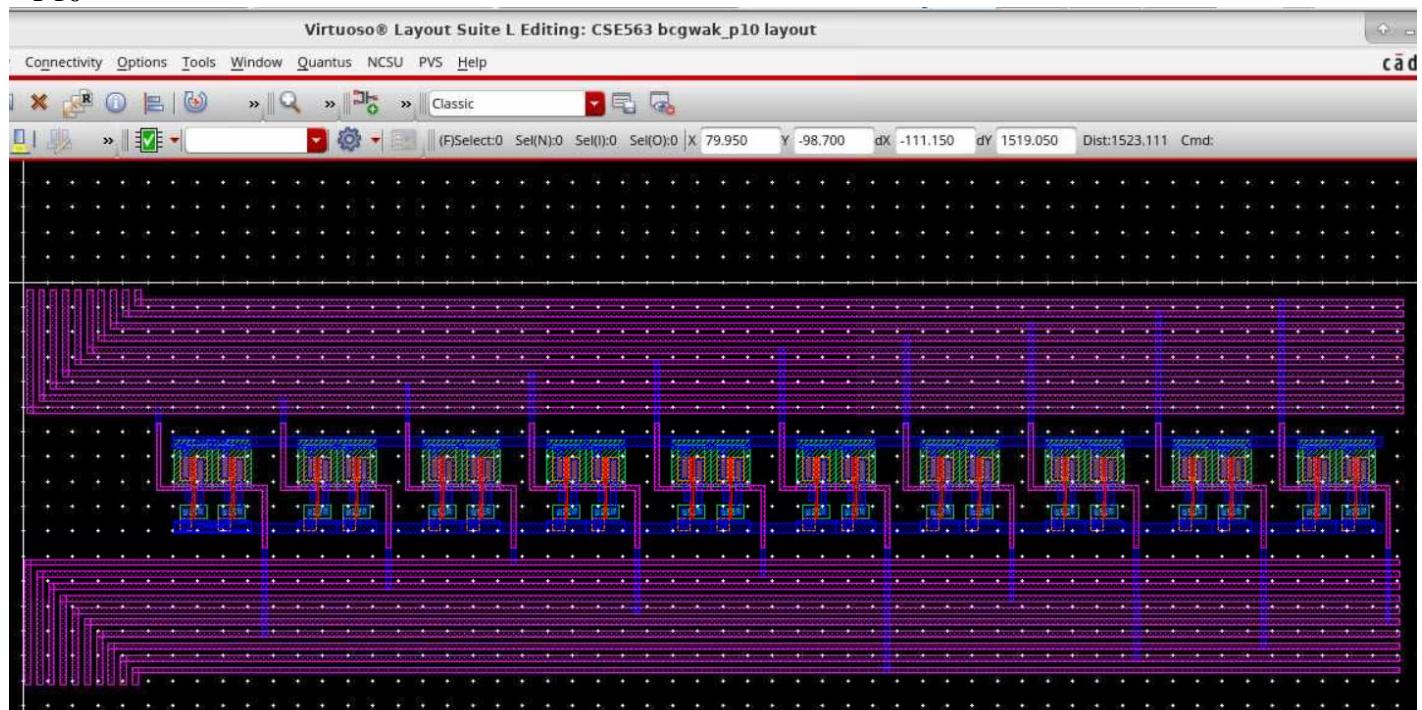
* XOR2



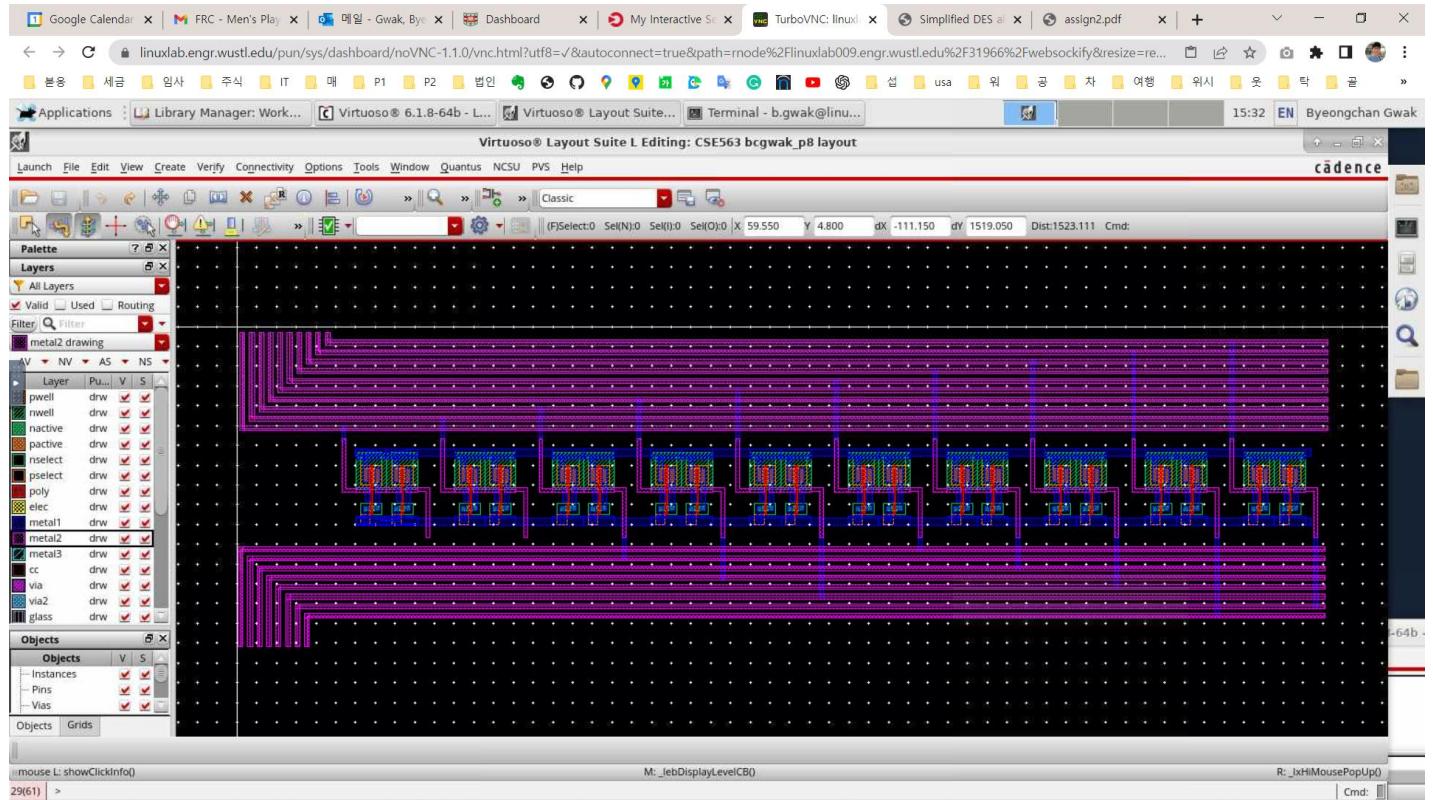
* XOR4



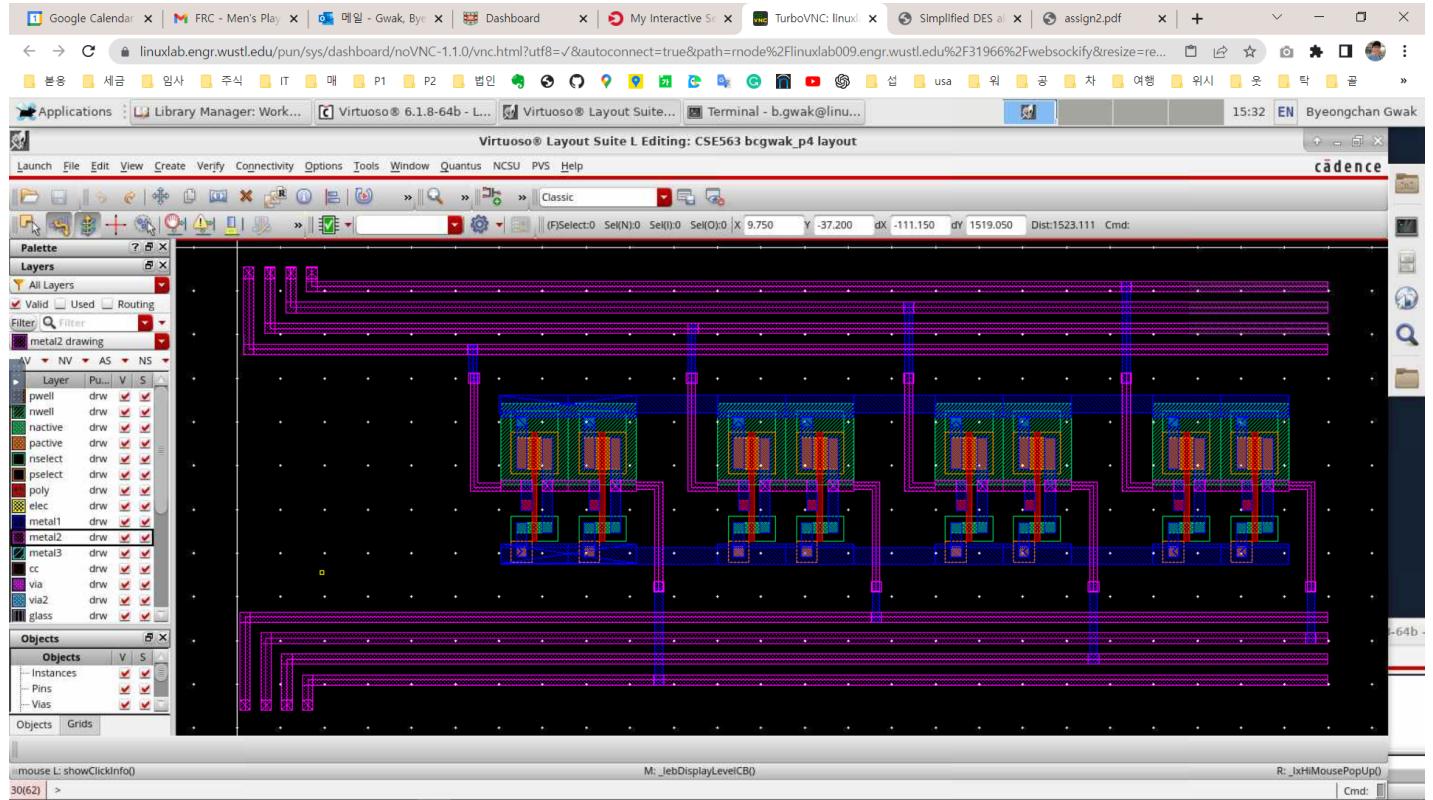
* P10



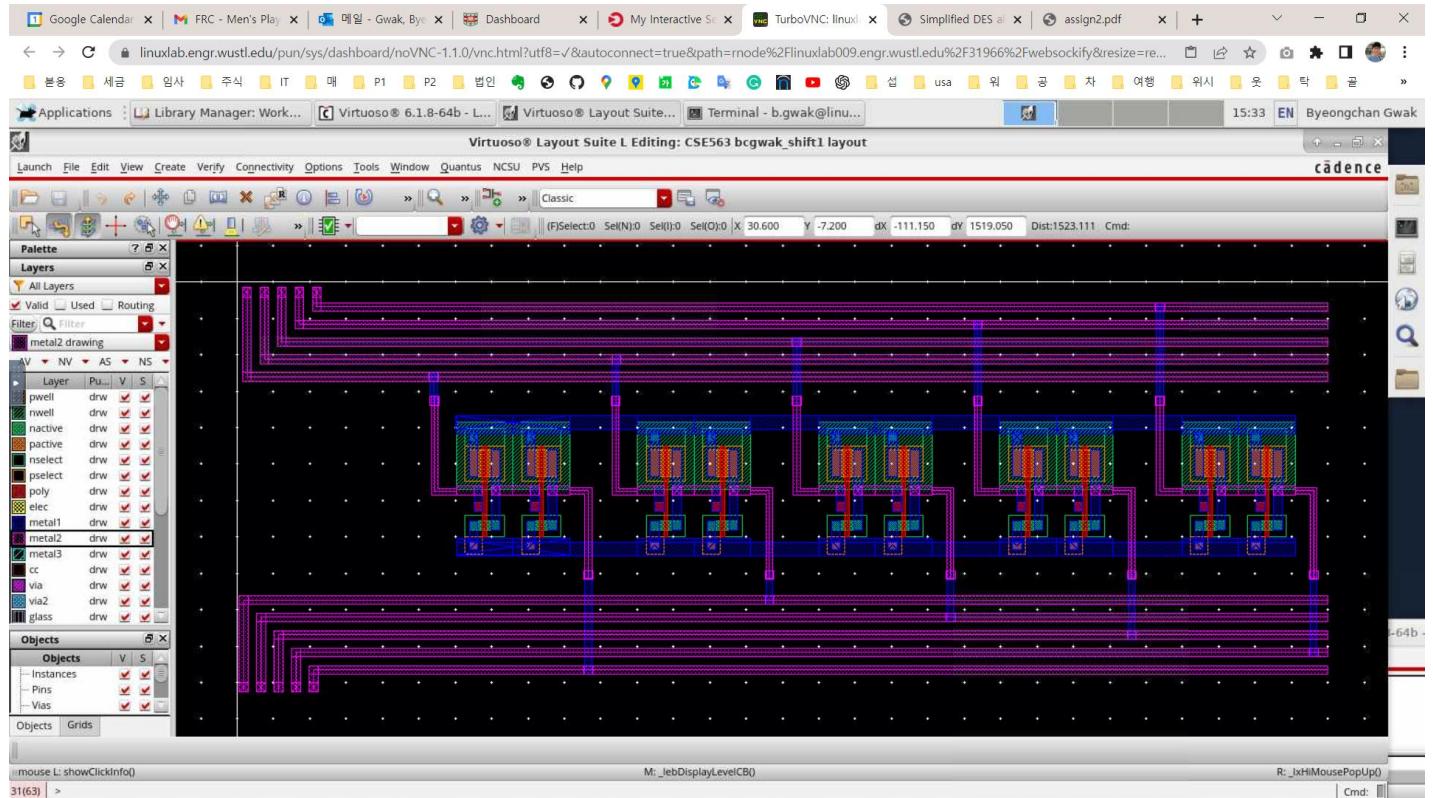
* P8



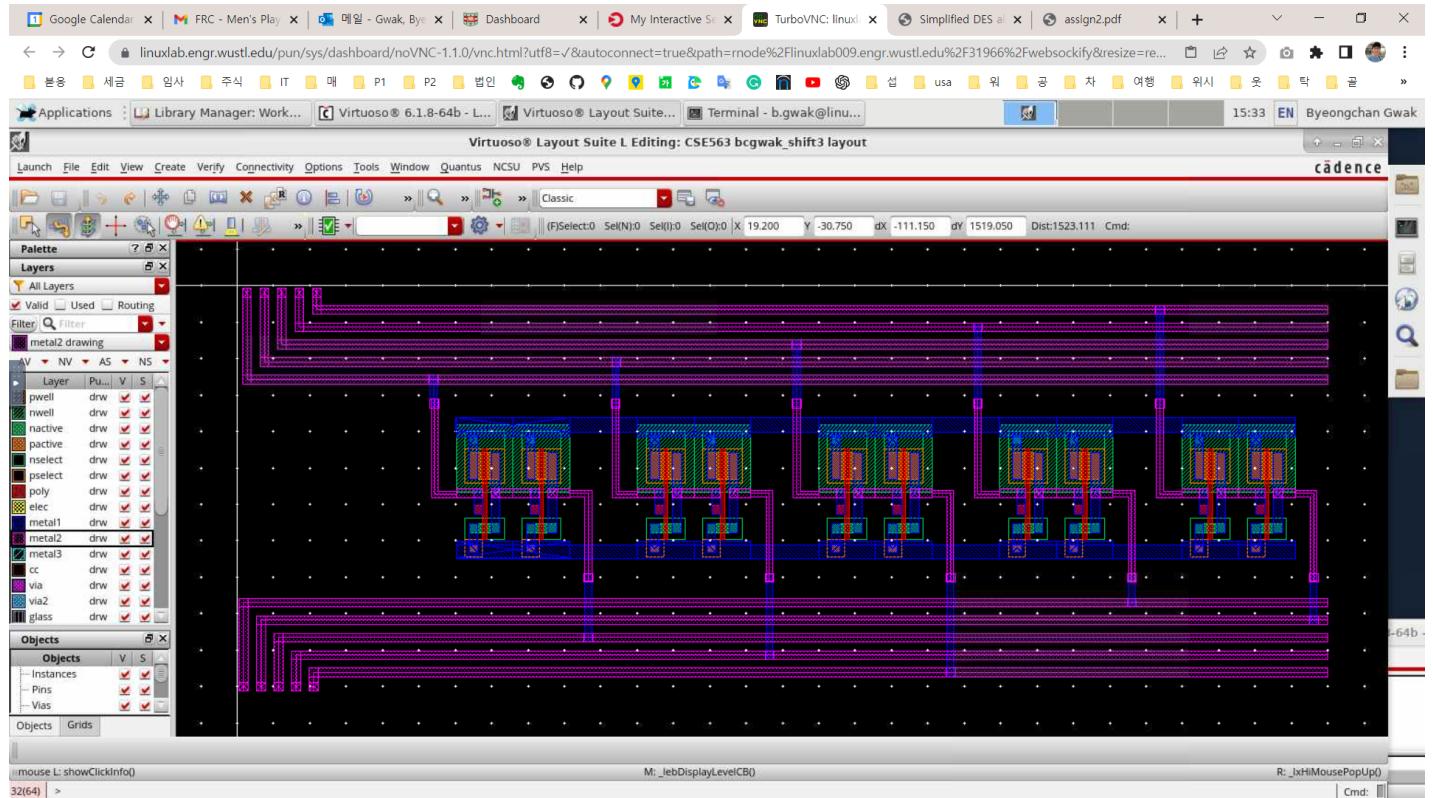
* P4



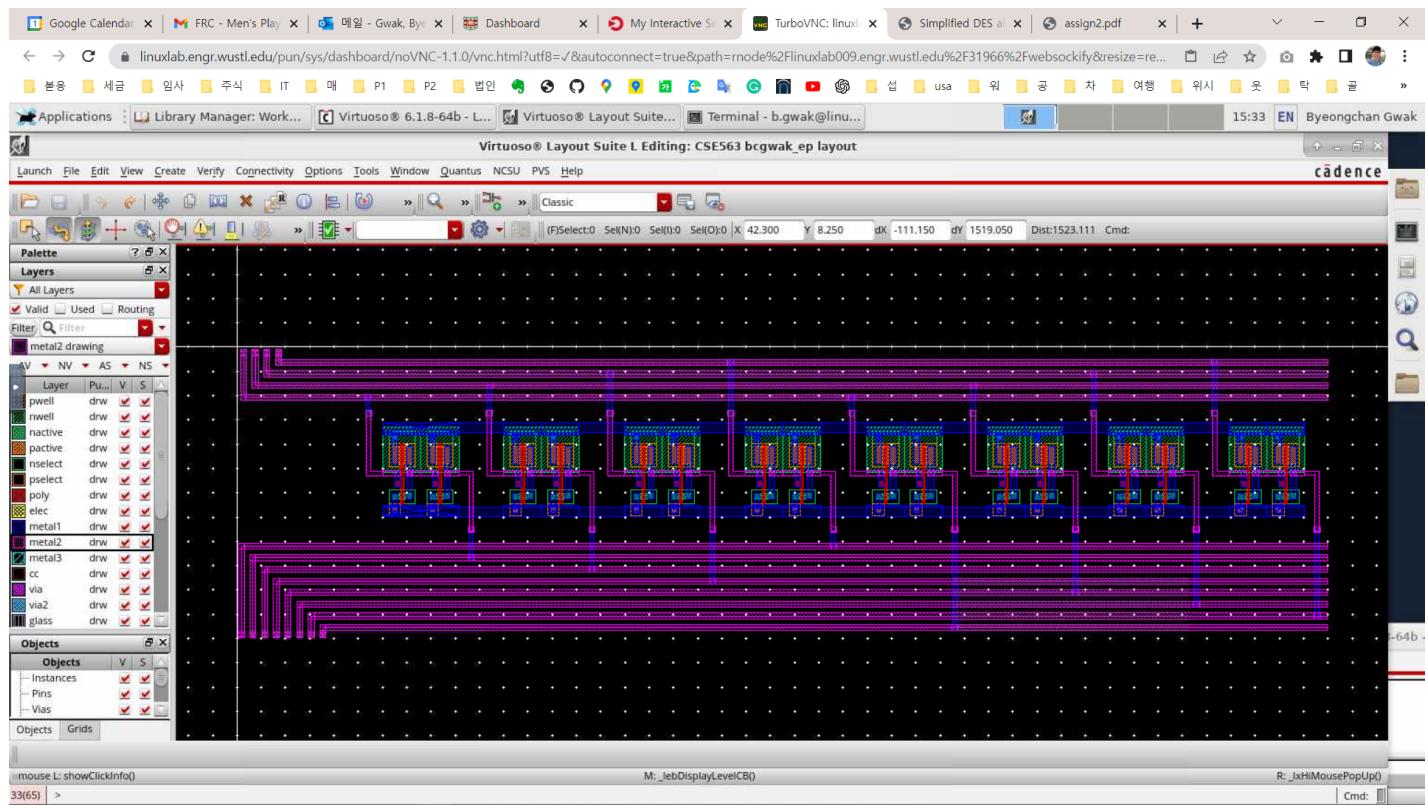
* SHIFT 1



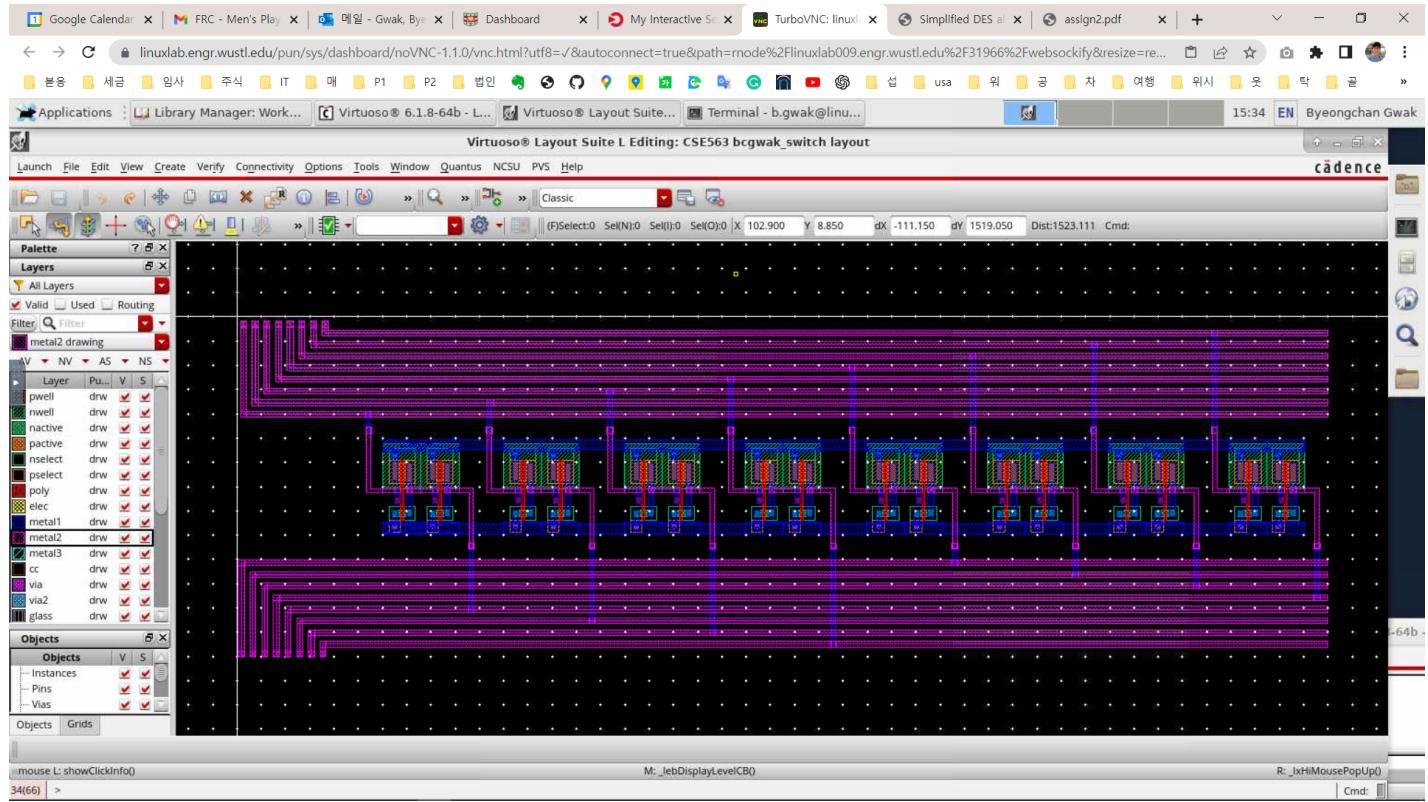
* SHIFT 3



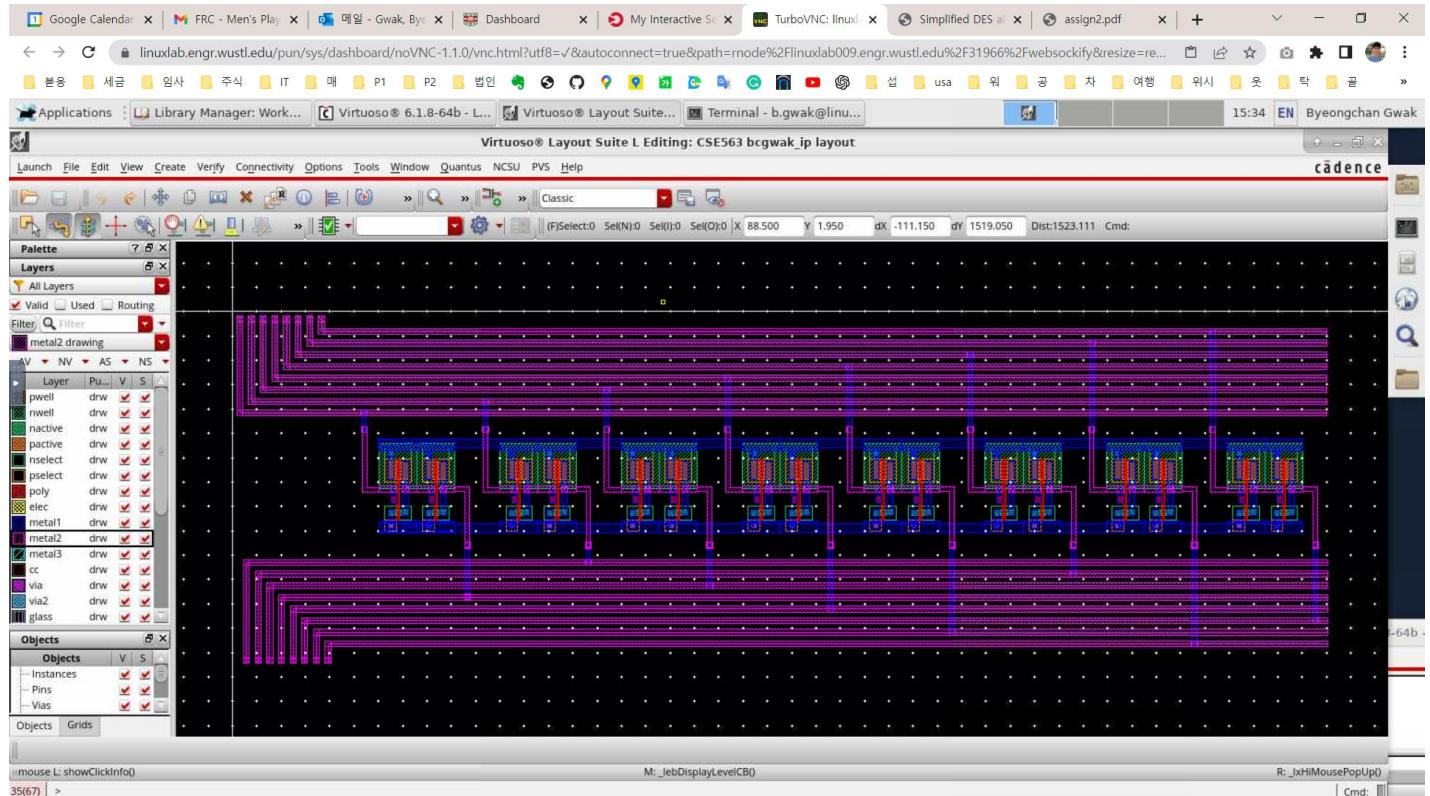
* EP



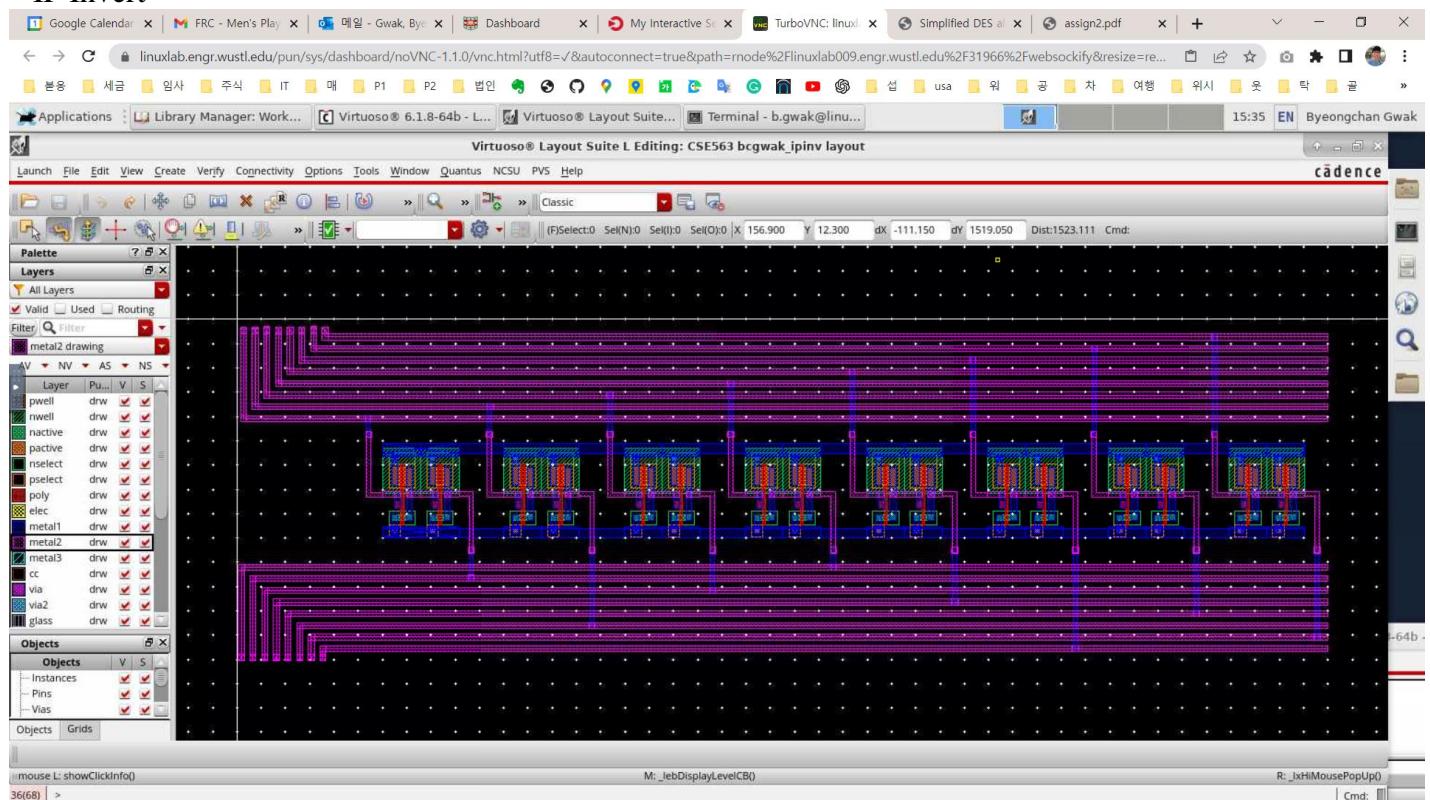
* SWITCH



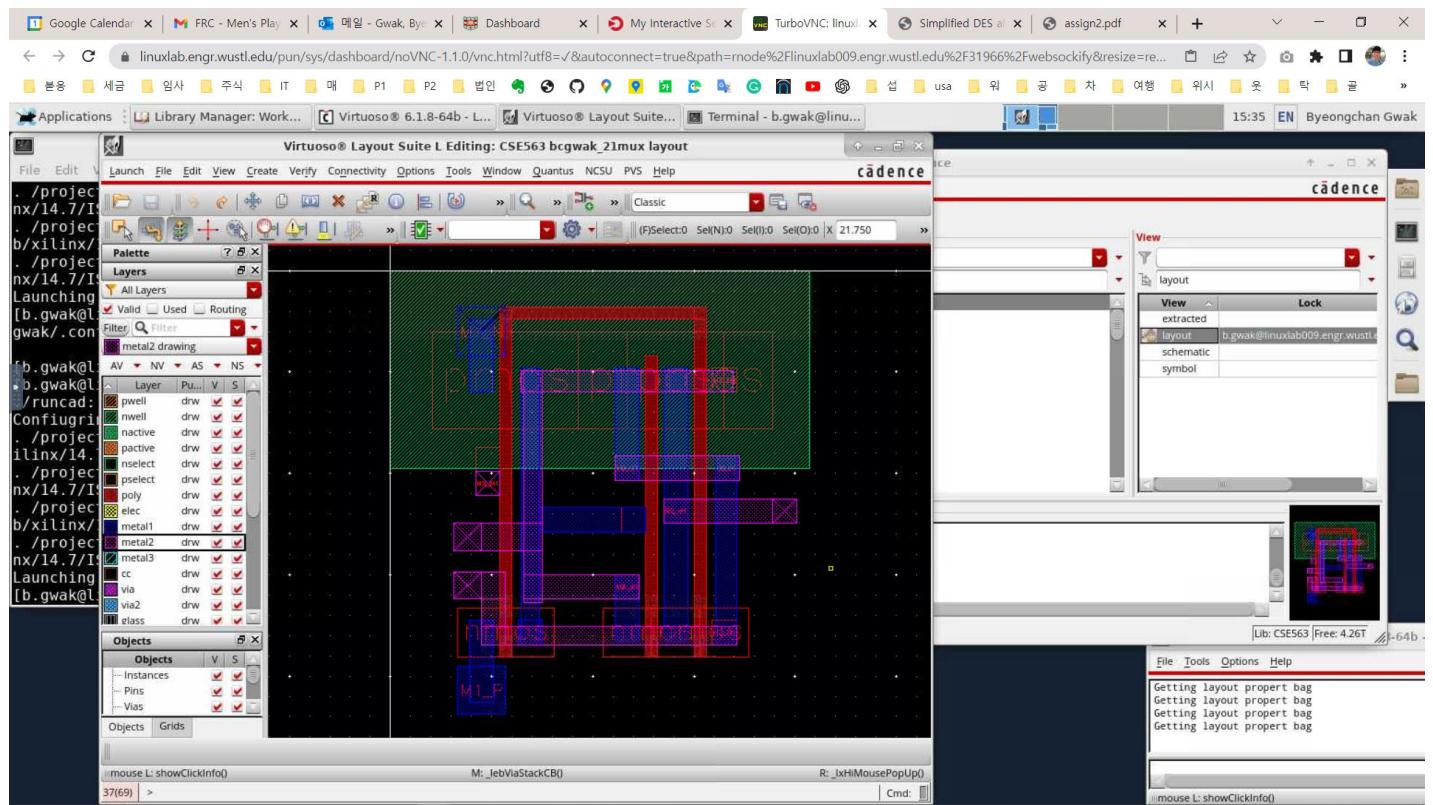
* IP



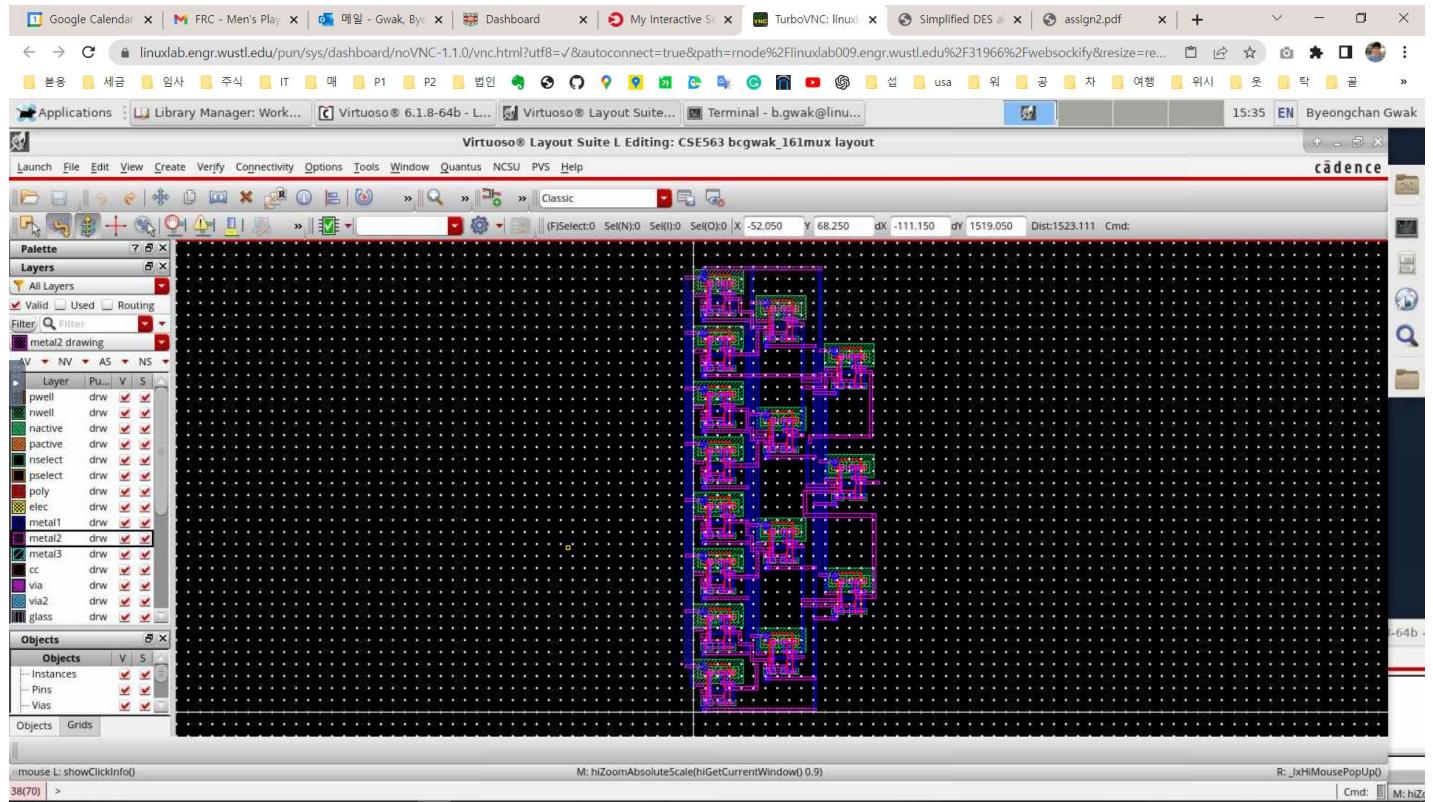
* IP Invert



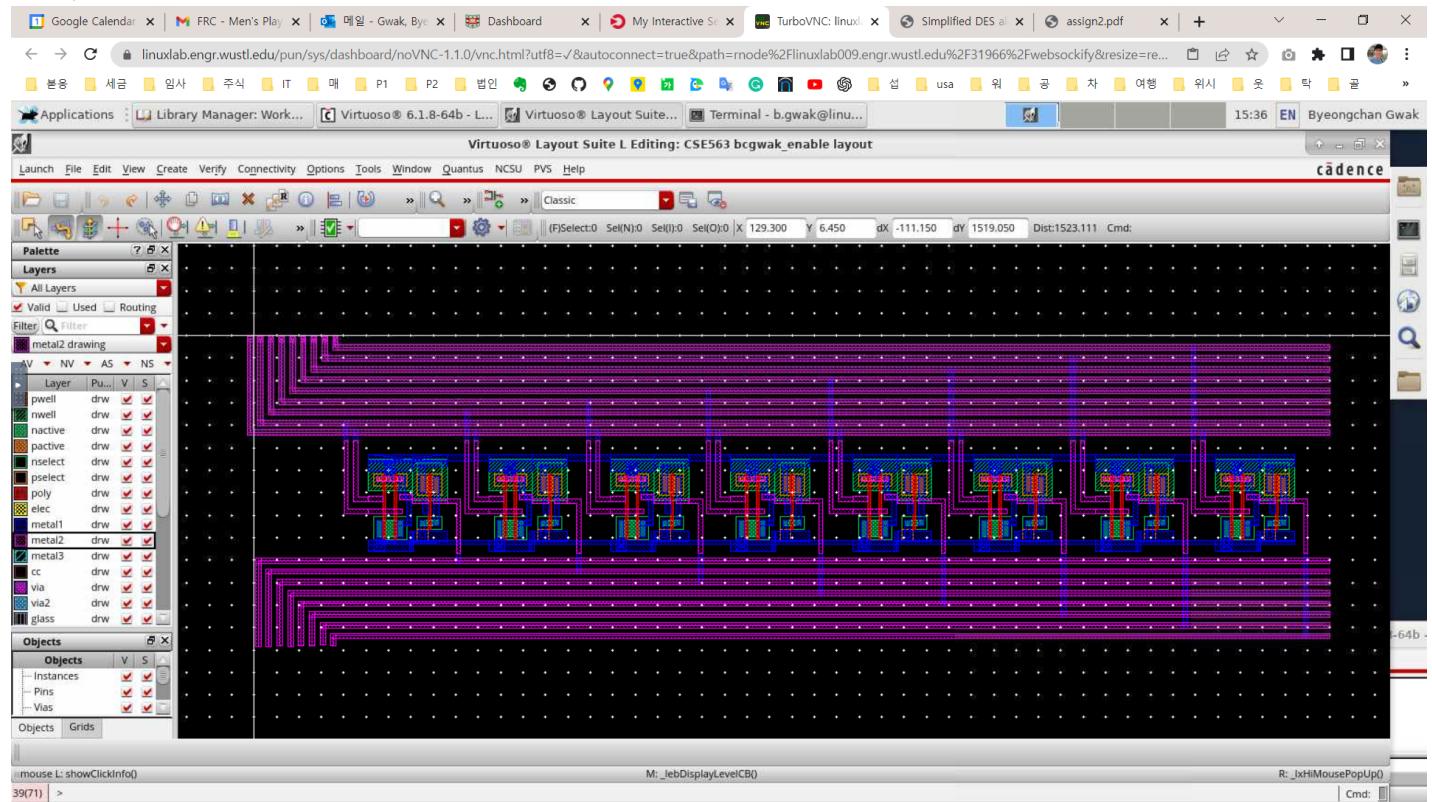
* 2:1 mux



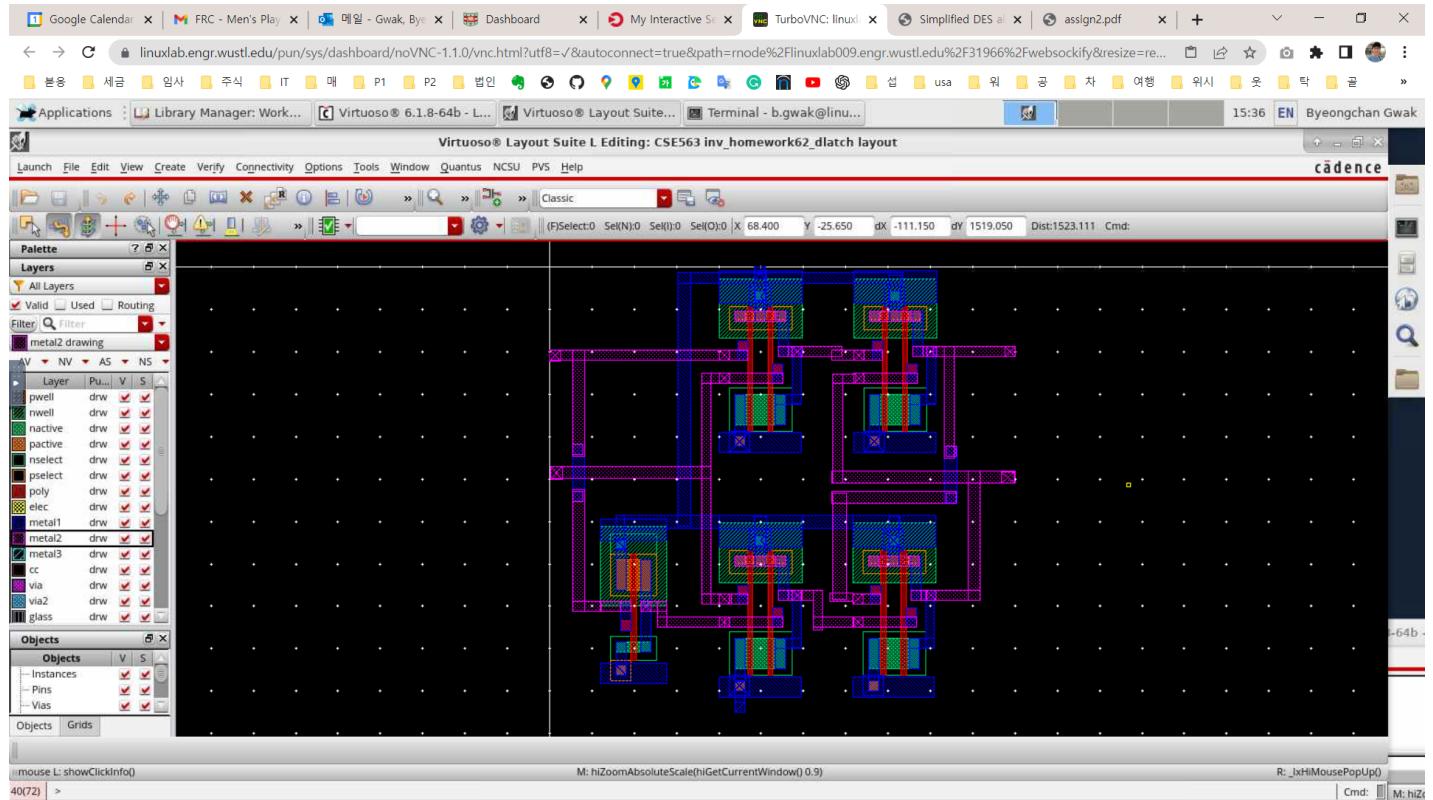
* 16:1 mux



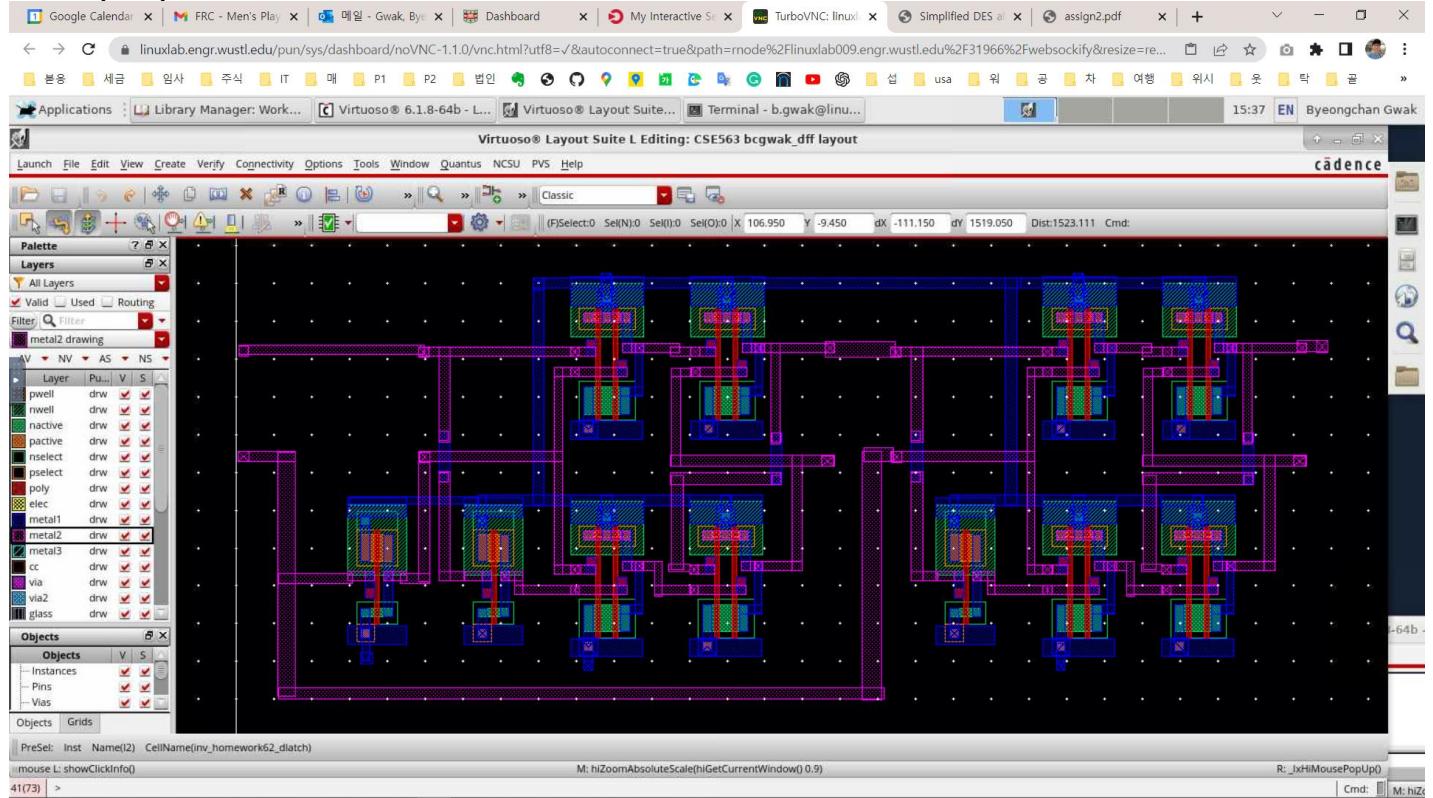
* ENABLE



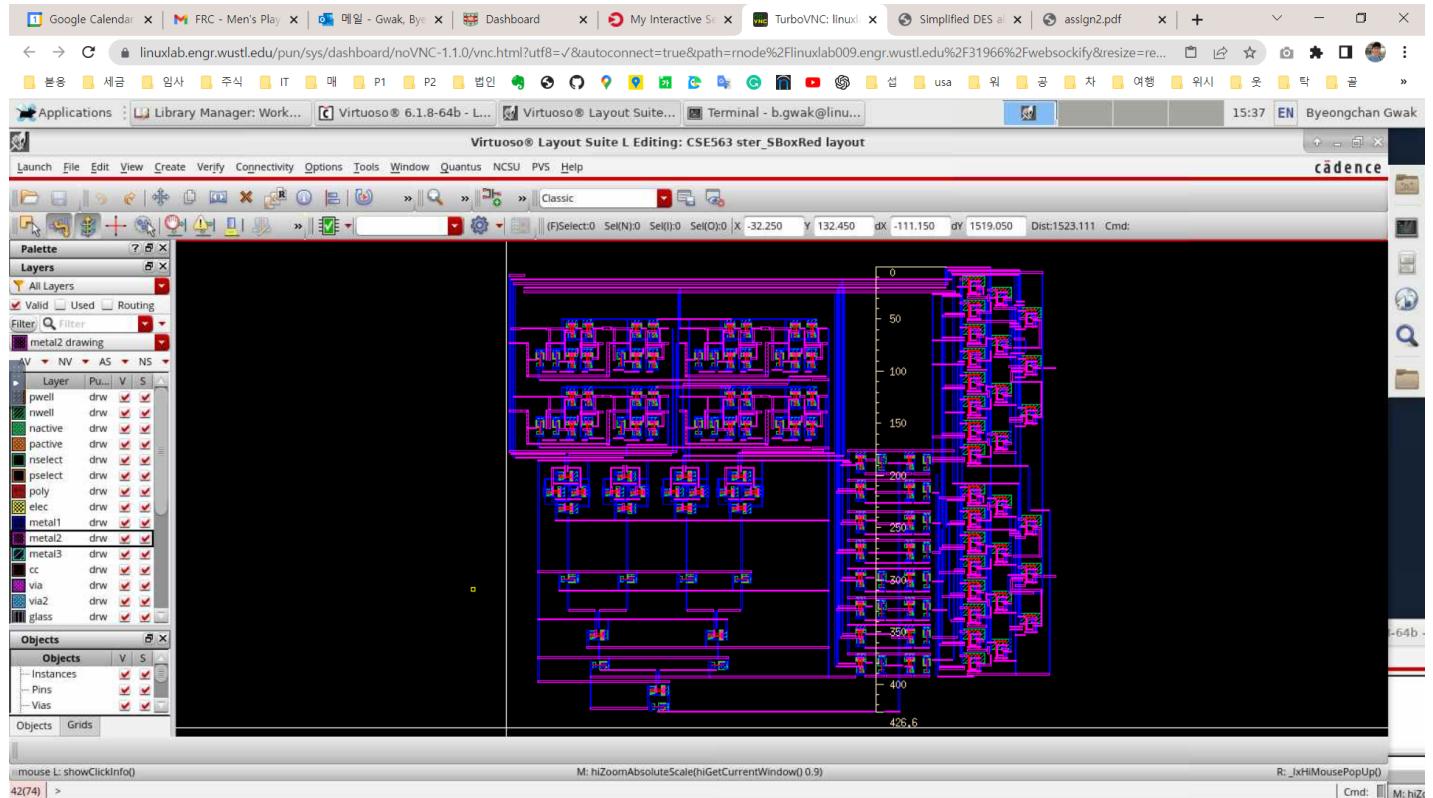
* D-LATCH



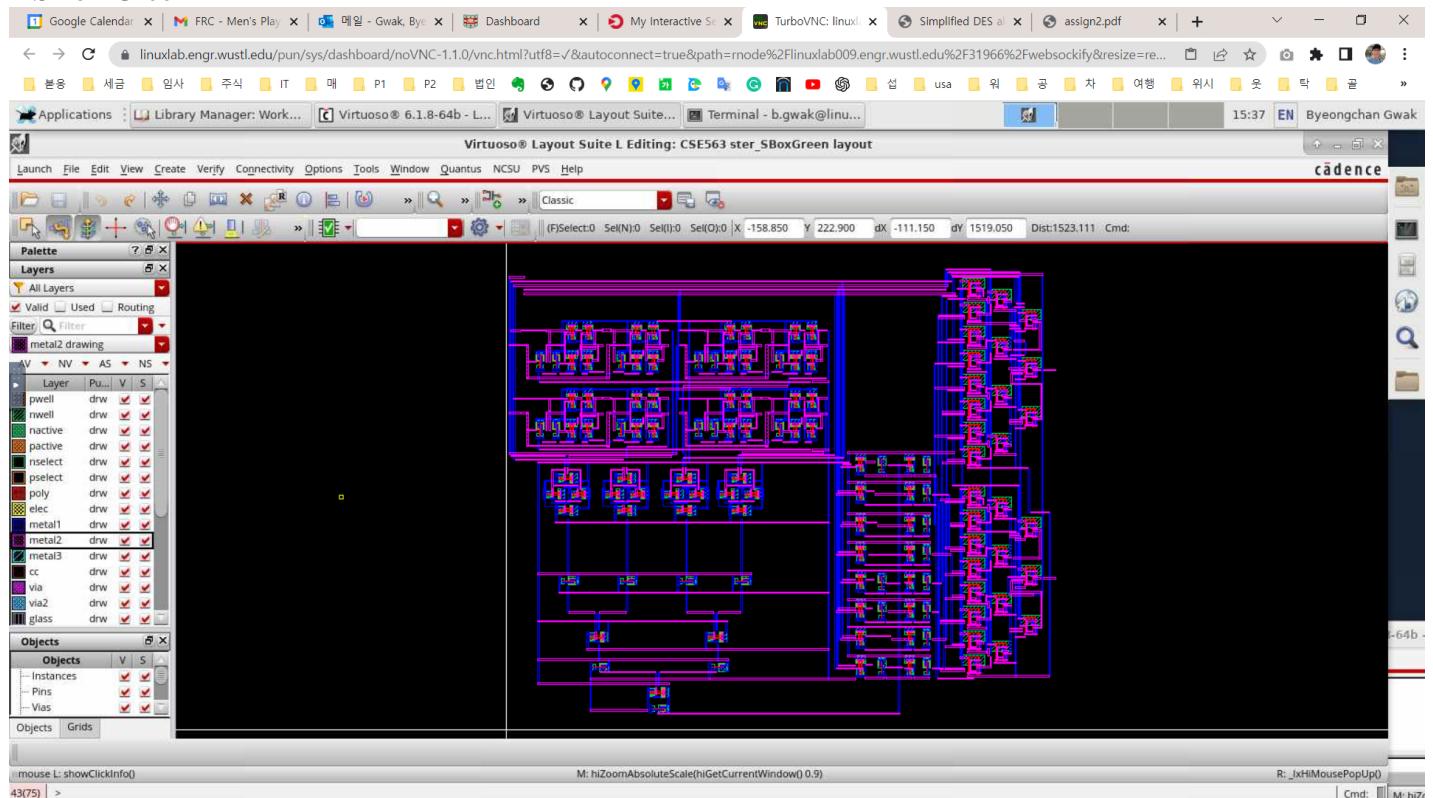
* D Flip flop



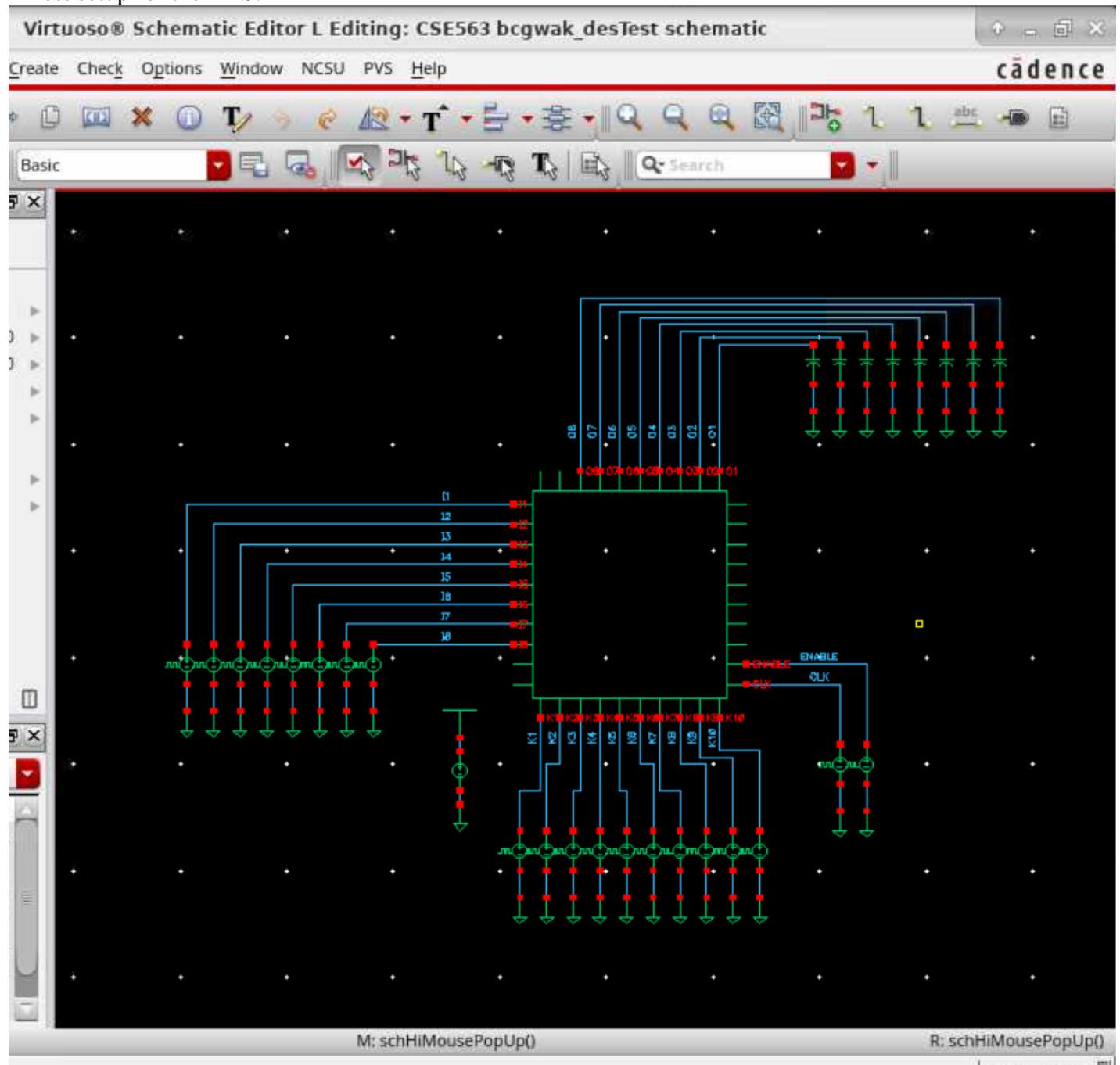
* SBox Red



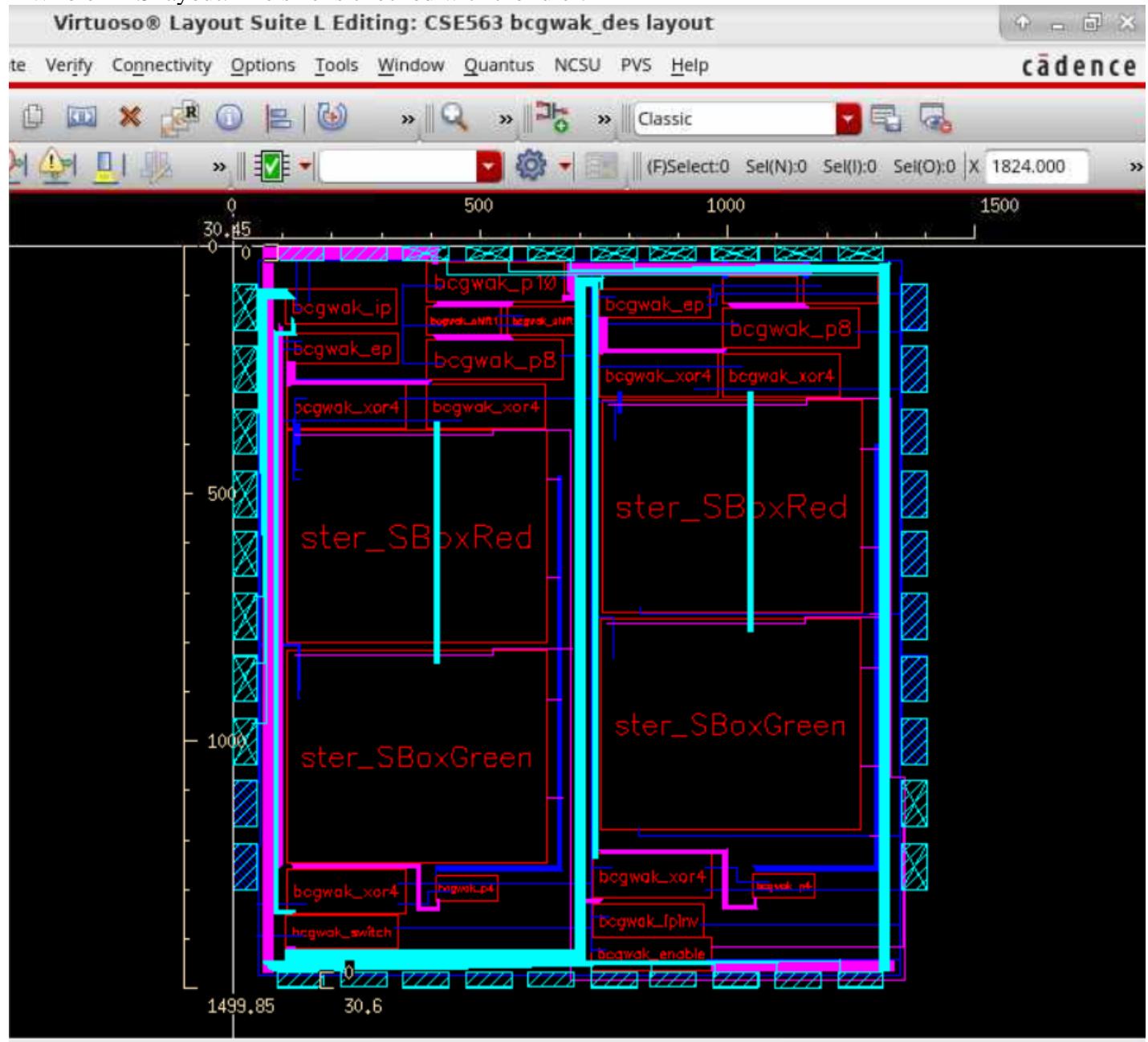
* SBox Green

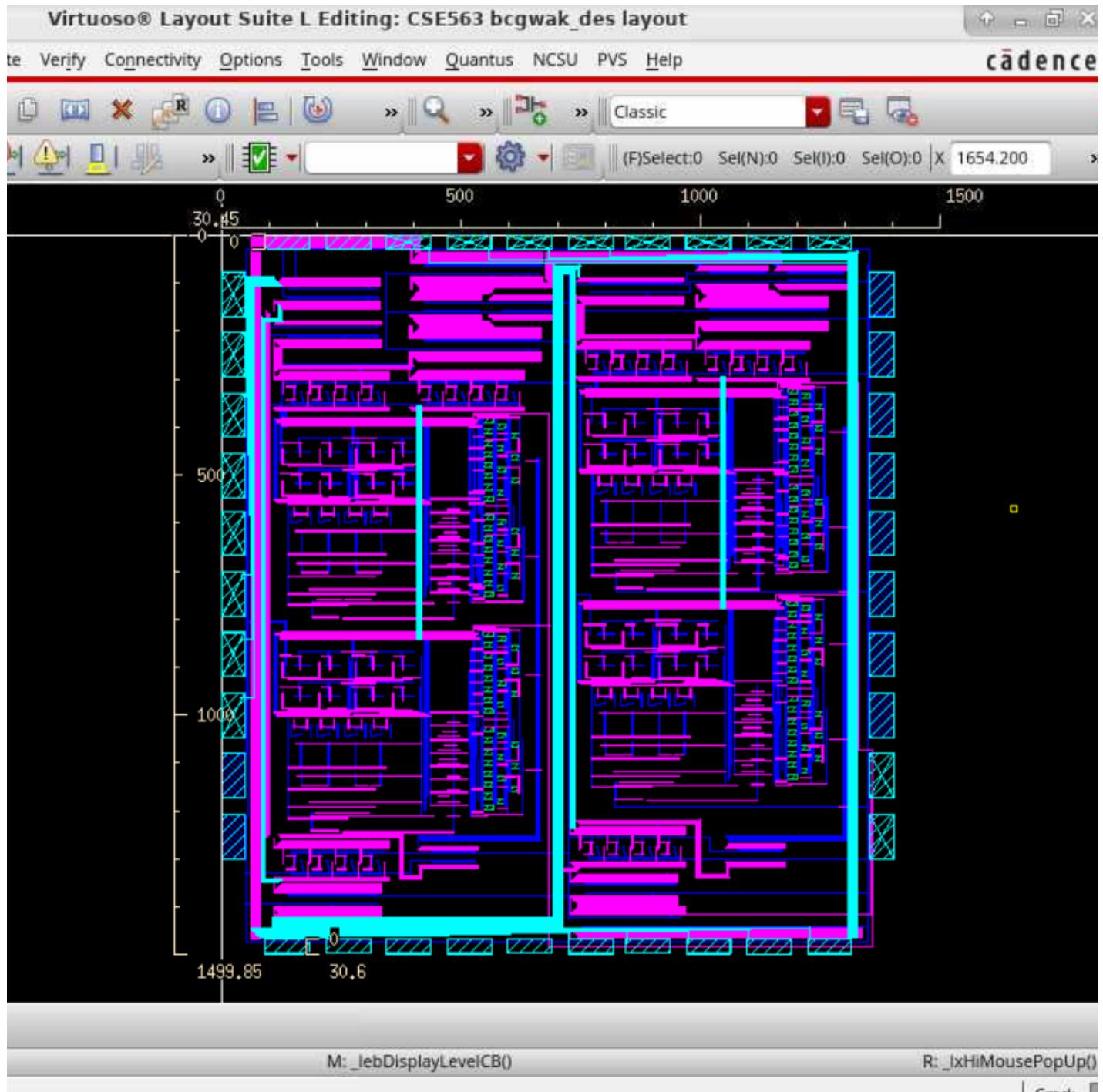


* Test setup for the DES.



* Whole DES layout. The size is checked with the ruler.





* Test result: CLK, ENABLE, Input(I1, I2, ..., I8), Key(K1, K2, ..., K10), Output(O1, O2, ..., O8)

