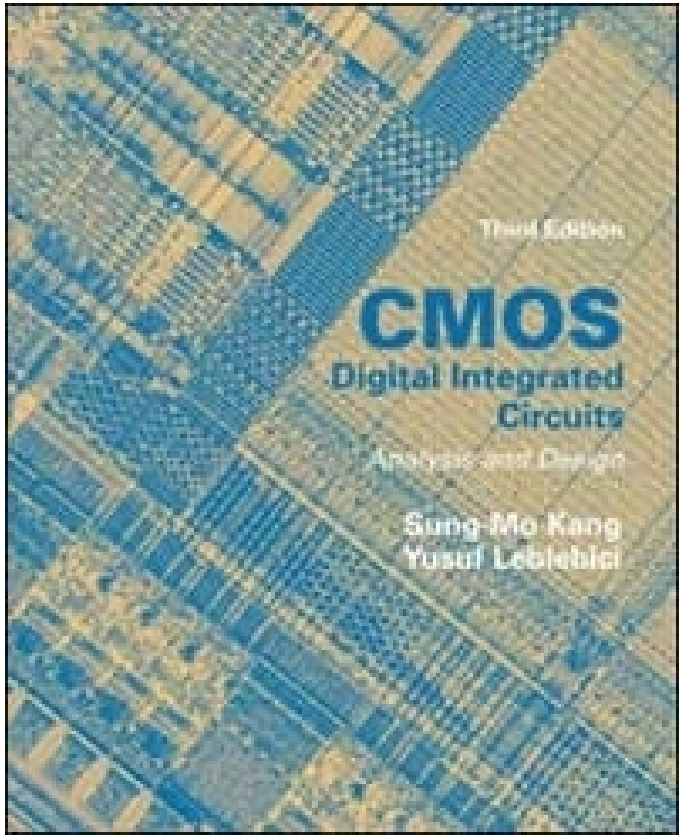
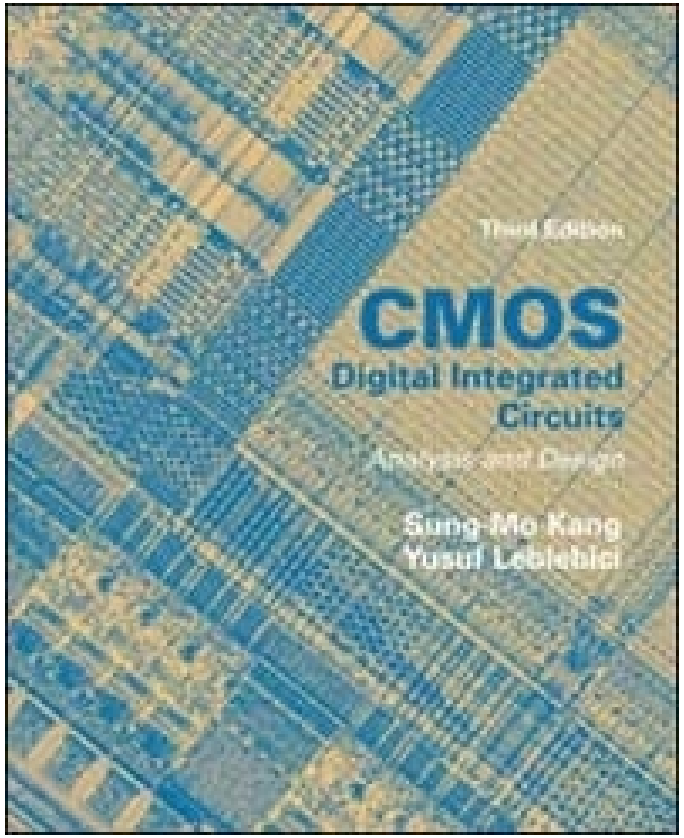
Digital IC Design and Architecture



MOS Transistor

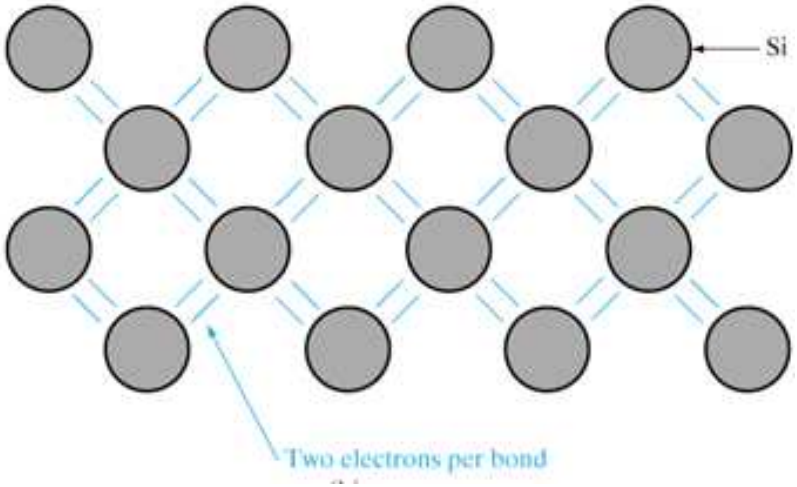
Goal of this chapter

- Present intuitive understanding of device operation
- Introduction of basic device equations of PN junction
- Introduction of basic device equations of FET
- Analysis of secondary and deep-sub-micron effects

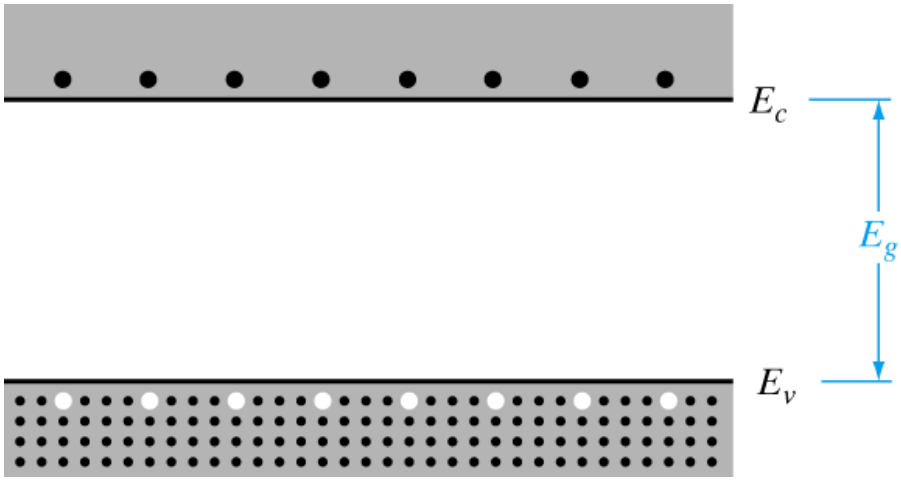


Properties of Si

Properties of Si

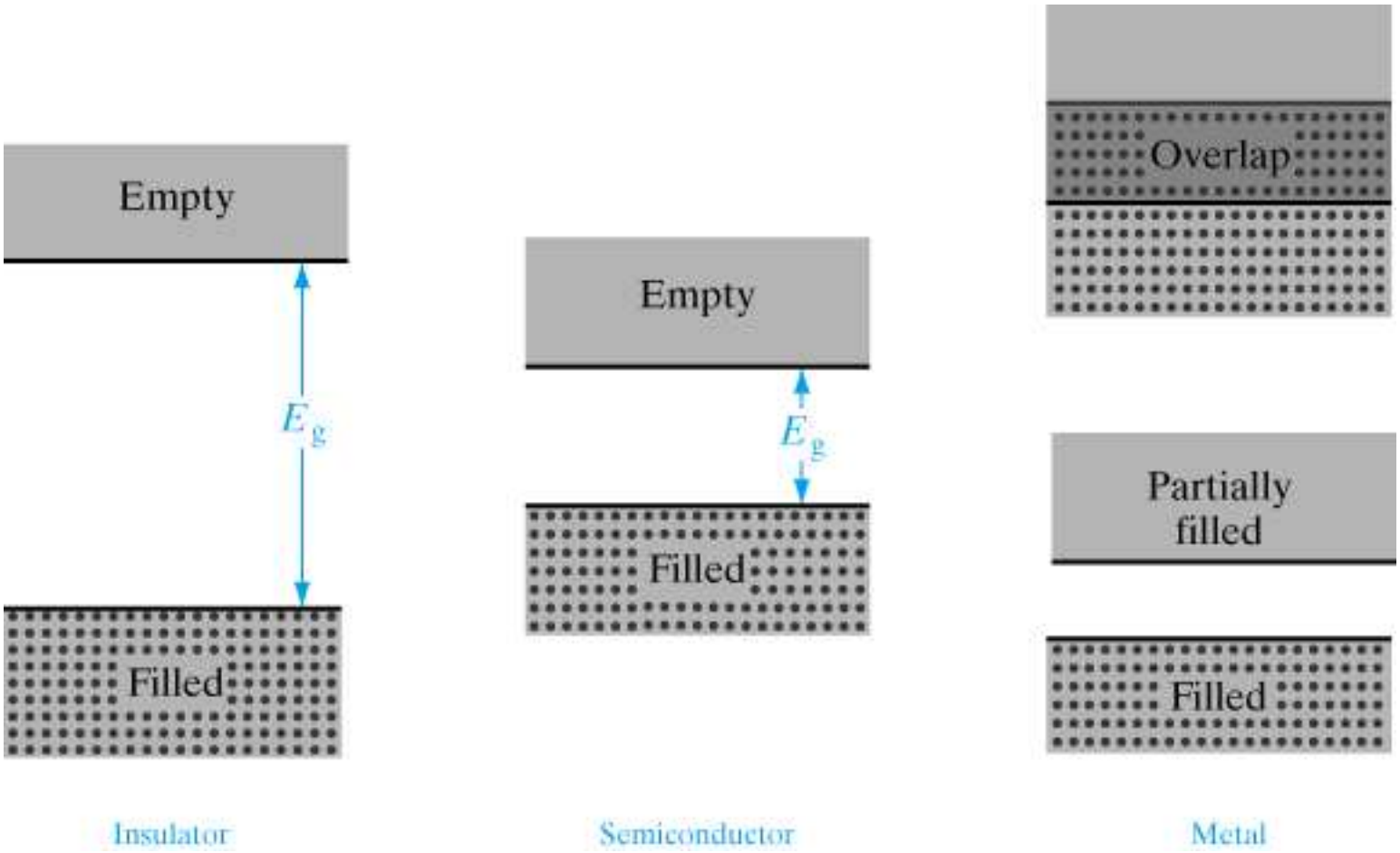


- covalent bonding in the Si crystal, veiwed along a <100> direction



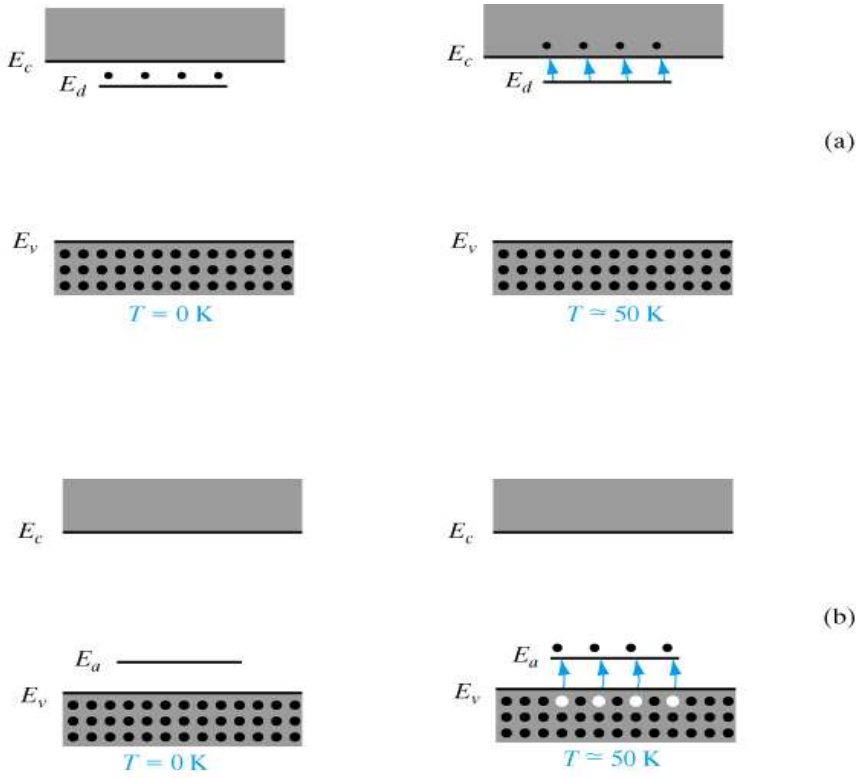
Energy band diagram of Si:
Eg=1.1eV

Typical band structures at 0 K



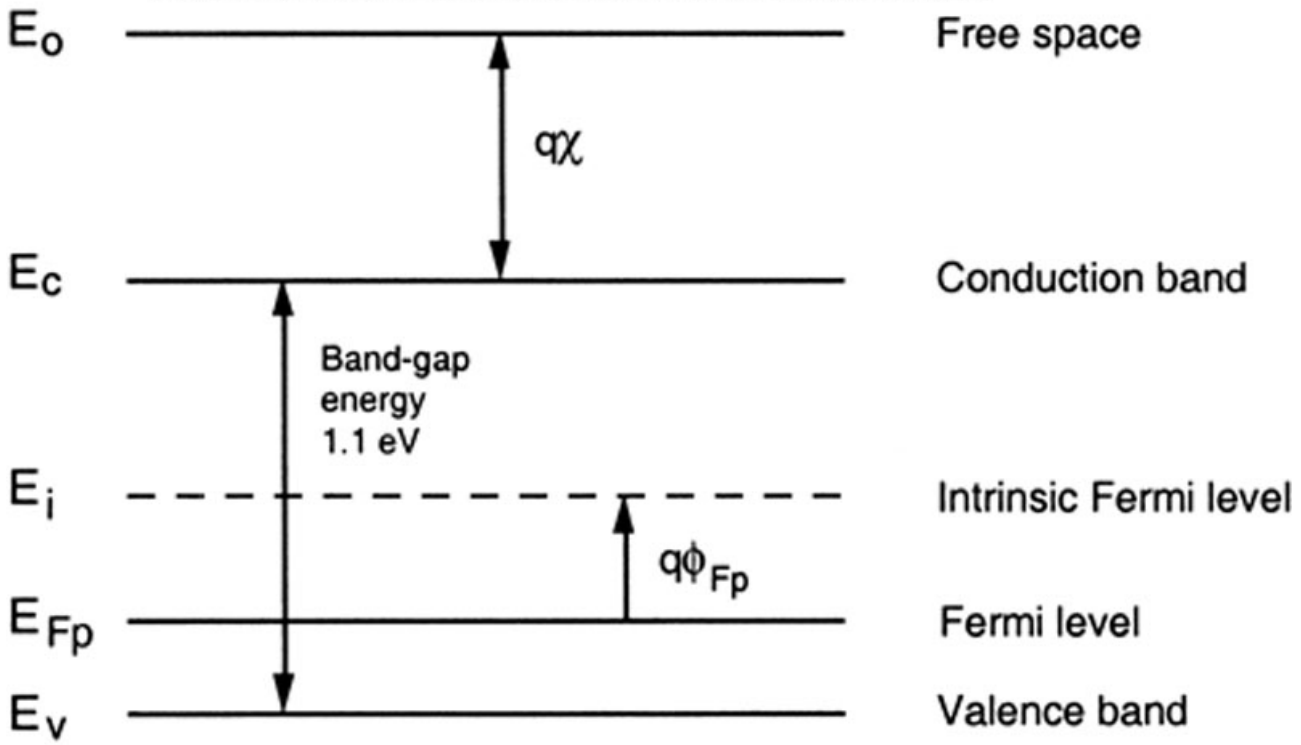
A. Insulators have large band gaps which prevents electrons to “jump” from valence to conduction band. B. Semiconductors have smaller band gaps such that electrons can be thermally excited to the conduction band C. In metals, large number of electrons exist in the valence band.

Doping of Silicon



Energy band model and chemical bond model of dopants in semiconductors: (a) donation of electrons from donor level to conduction band; (b) acceptance of valence band electrons by an acceptor level, and the resulting creation of holes; (c) donor and acceptor atoms in the covalent bonding model of a Si crystal.

Energy Band Diagram of p-type Silicon

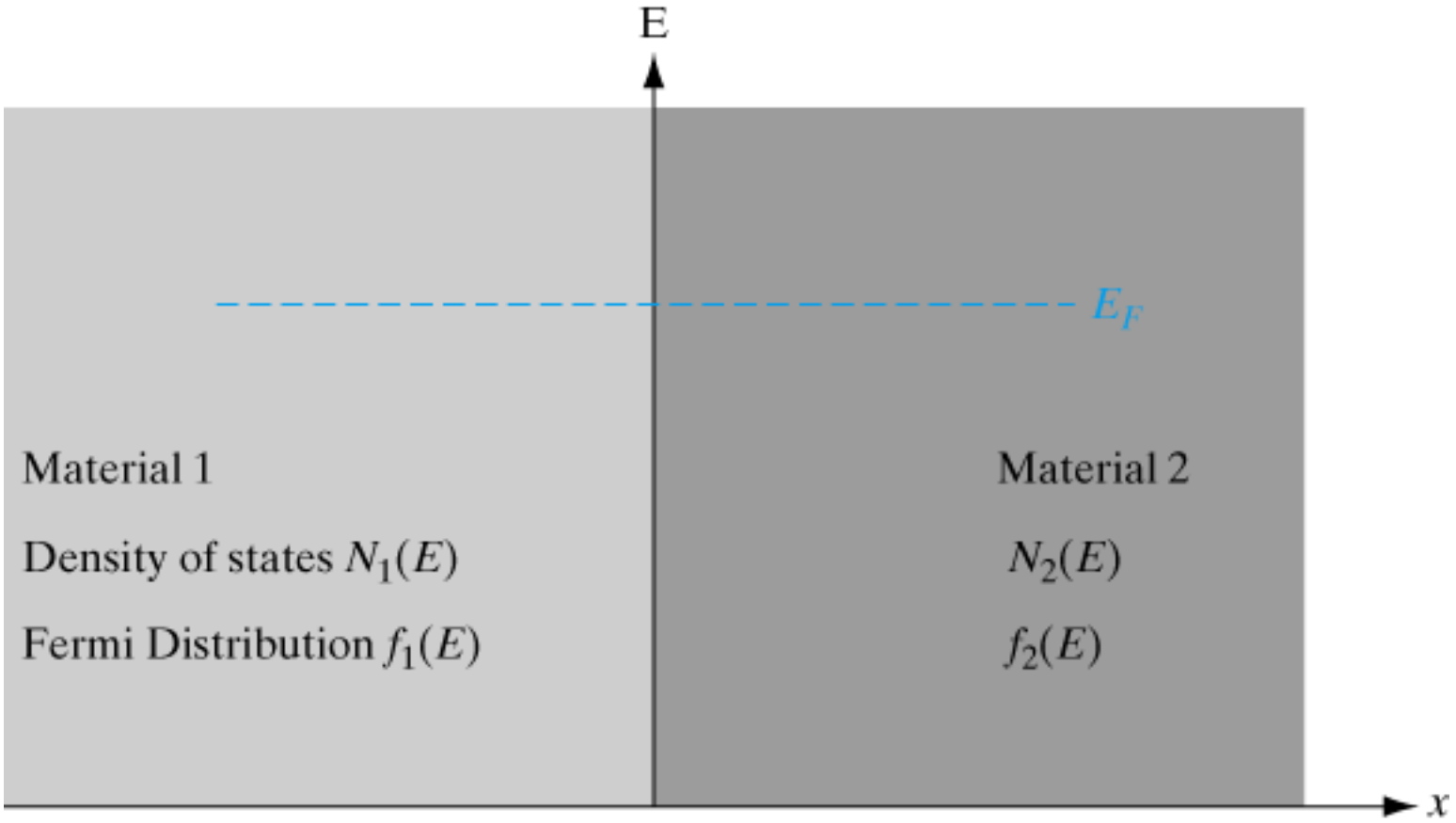


The Fermi potential for p-type semiconductor:

$$\phi_{F_P} = \frac{kT}{q} \ln \frac{n_i}{N_A}$$

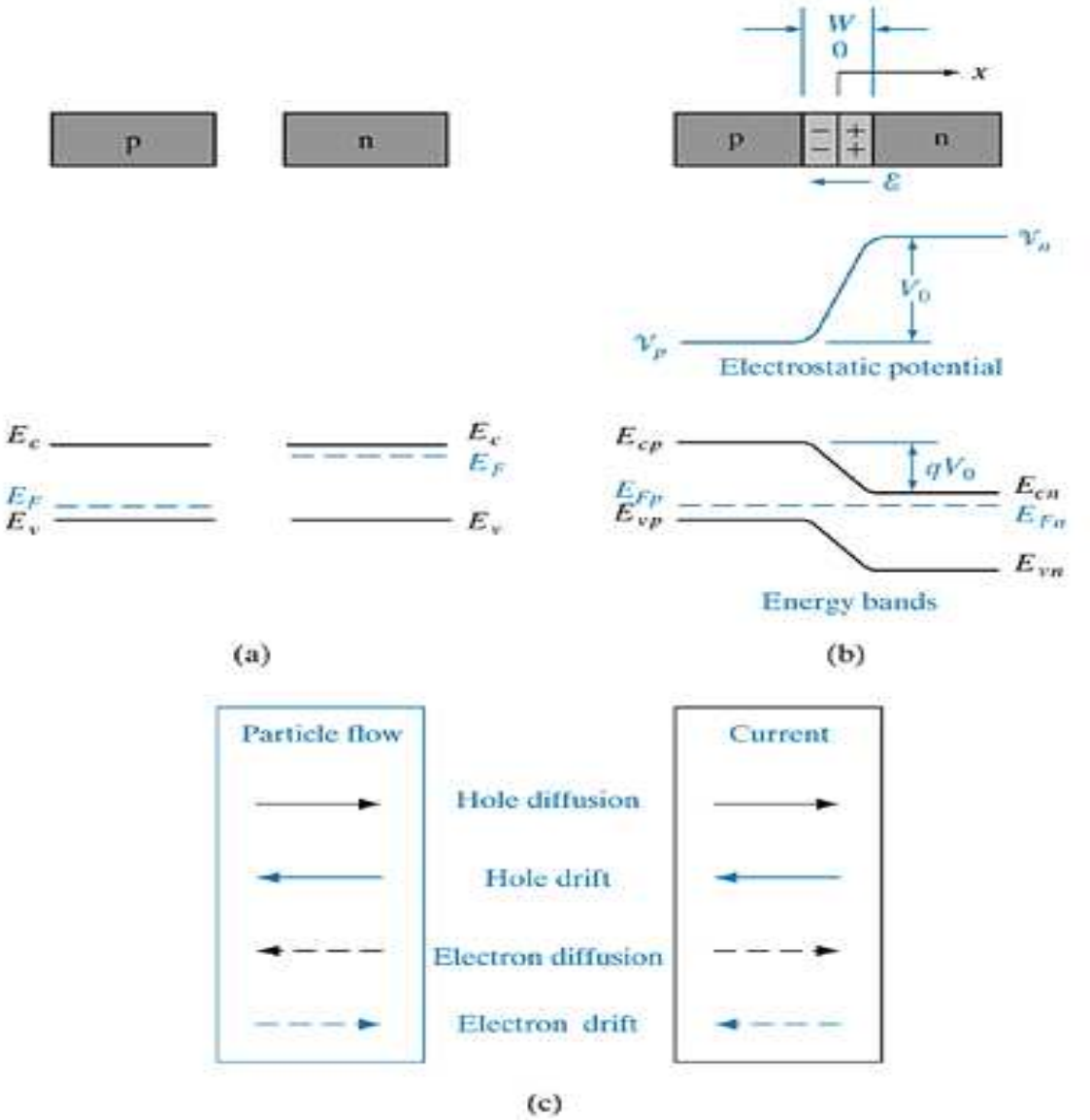
$$\phi_F = \frac{E_F - E_i}{q}$$ The Fermi potential

Junction between two materials



Two materials in intimate contact at equilibrium.
Note: Since the net motion of electrons is zero, the equilibrium Fermi level must be constant throughout.

PN Junction: Energy Band



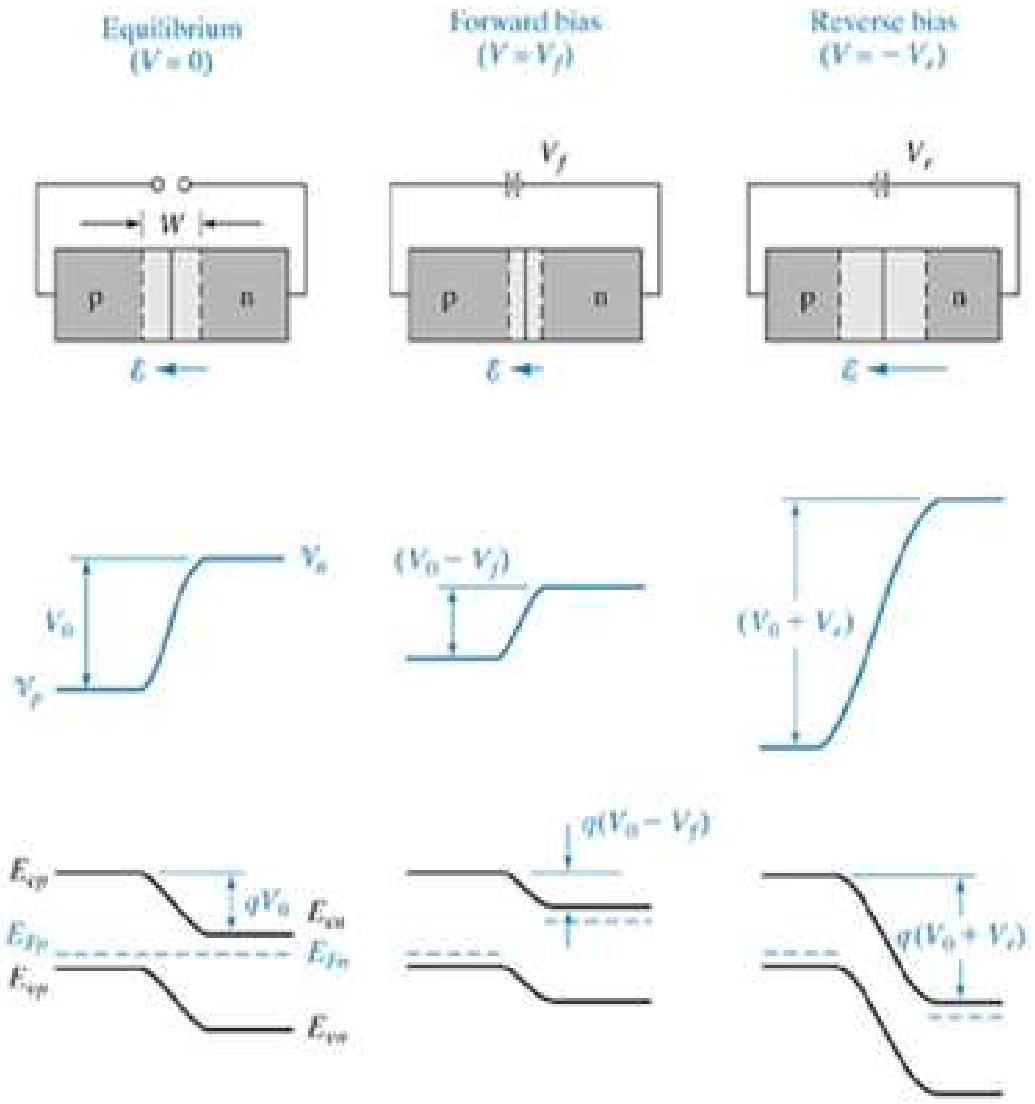
Built-in potential:

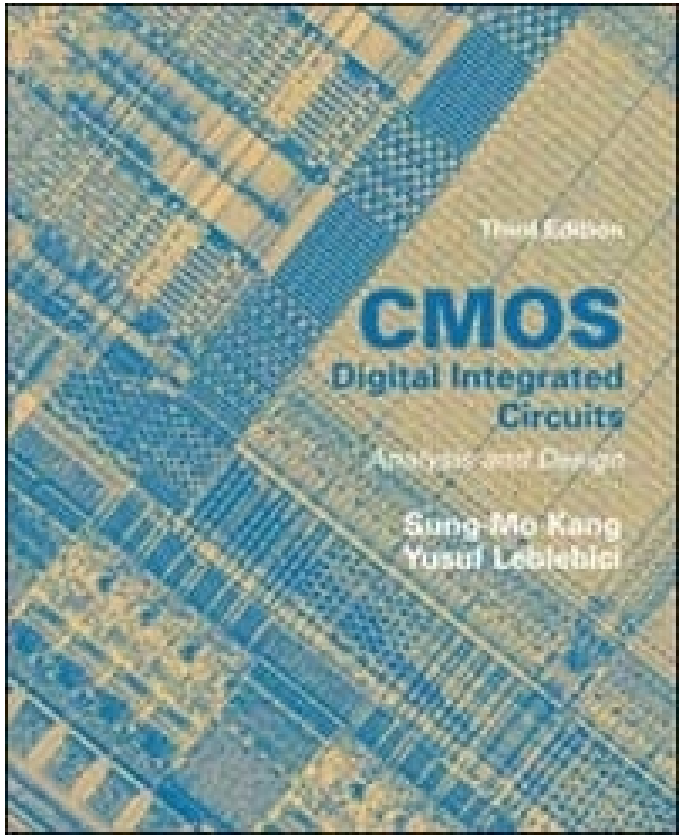
$$V_0 = \frac{kT}{q} \ln \frac{N_a N_d}{n_i^2}$$

Depletion region:

$$W = \left[\frac{2\varepsilon V_o}{q} \left(\frac{N_a + N_d}{N_a N_d} \right) \right]^{1/2}$$

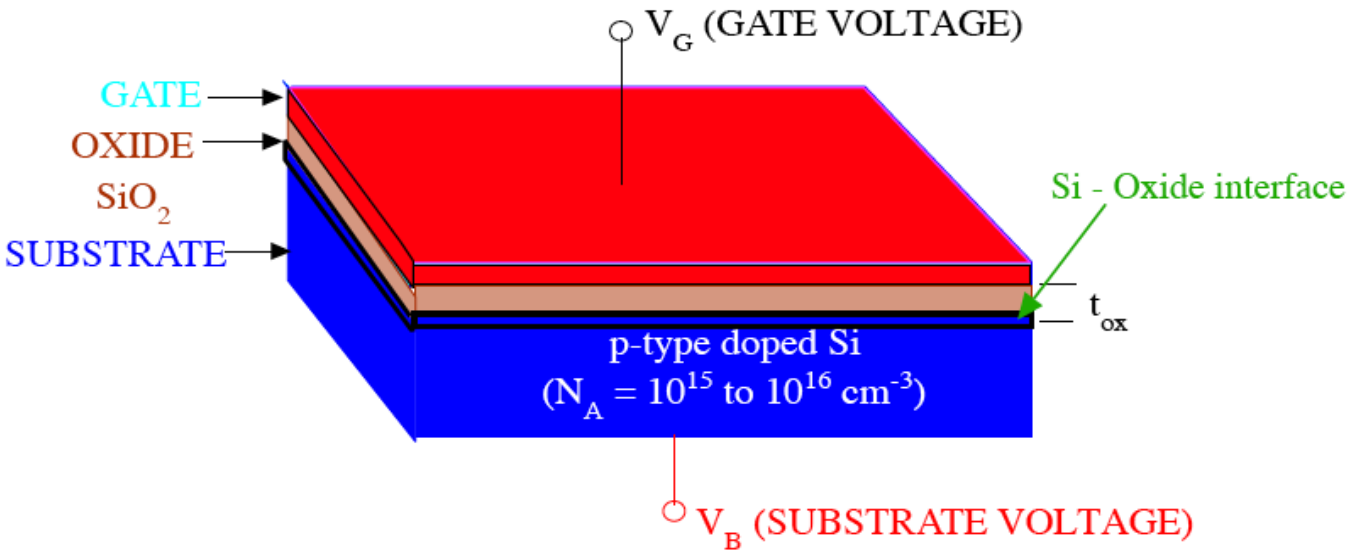
PN Junction Under External Bias





MOSFET Energy Band Diagram

Two terminal MOS Structure



EQUILIBRIUM: $n\,p = n_i^2$ ($n_i \approx 1.45 \times 10^{10}$ cm^{-3}) Intrinsic carrier concentration

Let SUBSTRATE be uniformy doped @ N_A

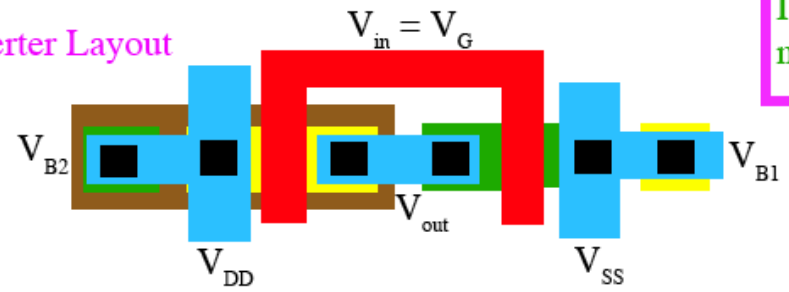
$$n_{p0} \approx \frac{n_i^2}{N_A} \quad \text{and} \quad p_{p0} = N_A$$

MASS ACTION LAW

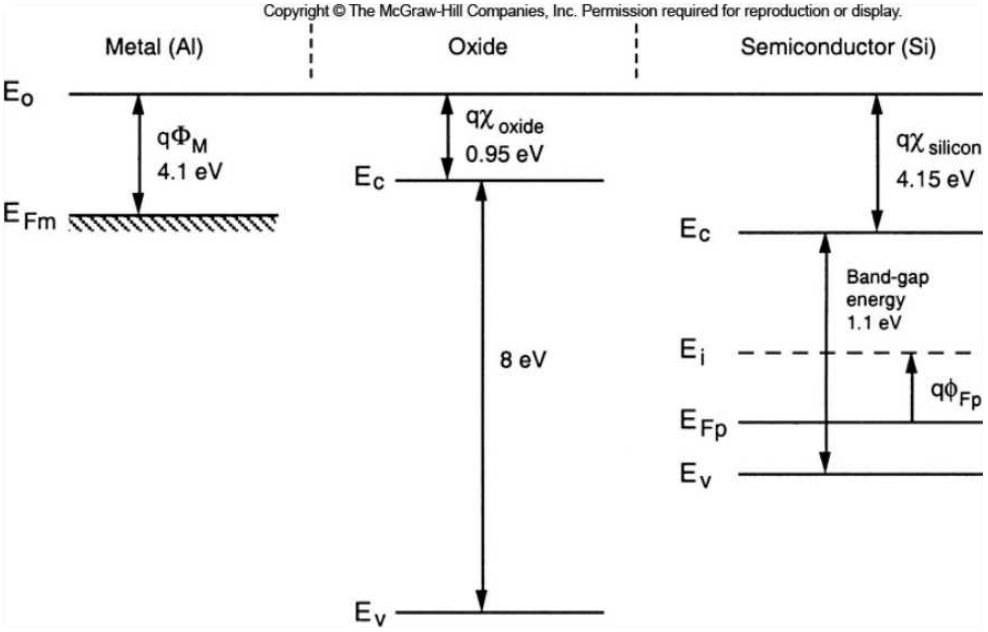
(BULK carrier concentrations)

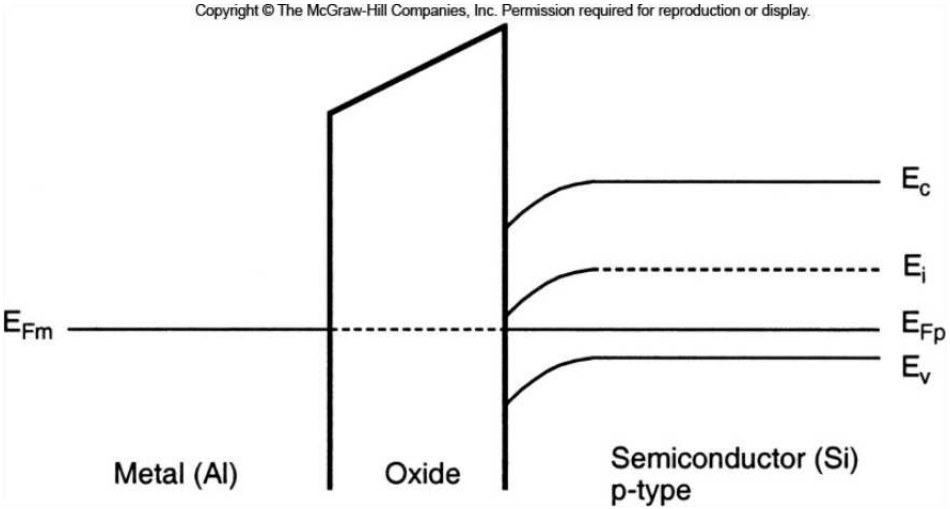
If n-type doped Si:
$n_{n0} = N_D$ and $p_{n0} = n_i^2/N_D$

N-well CMOS Inverter Layout



Energy Band Diagram of FET





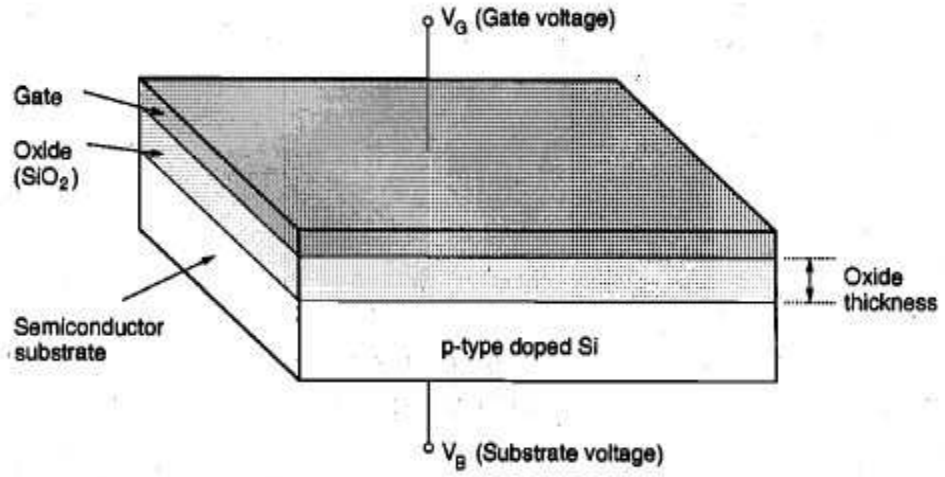
The energy required to move an electron from the Fermi level into free space is called Work function:

$$q\Phi_S = q\chi + (E_C - E_F)$$

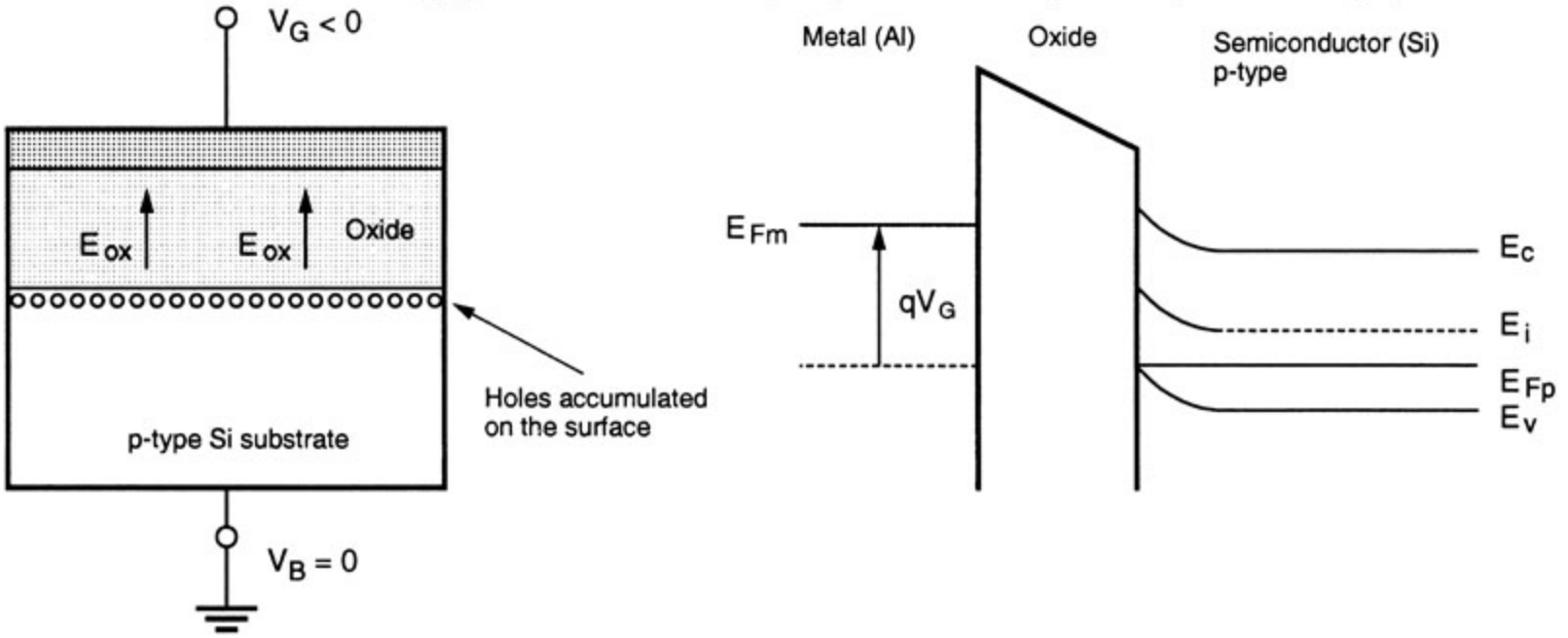
Two-Terminal MOS Structure with External Bias

Three Regions of Operation:

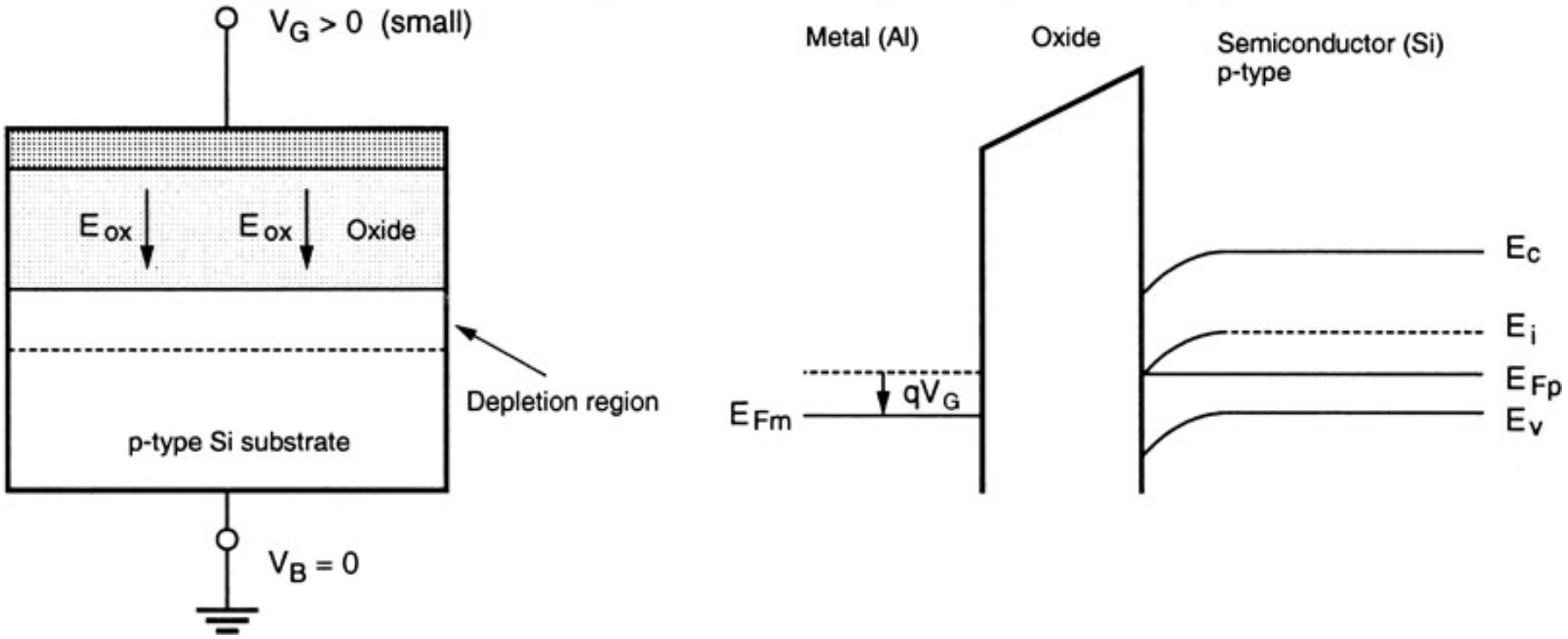
1. Accumulation Region: VG < 0
2. Depletion Region: VG > 0, small
3. Inversion Region: VG > 0, large



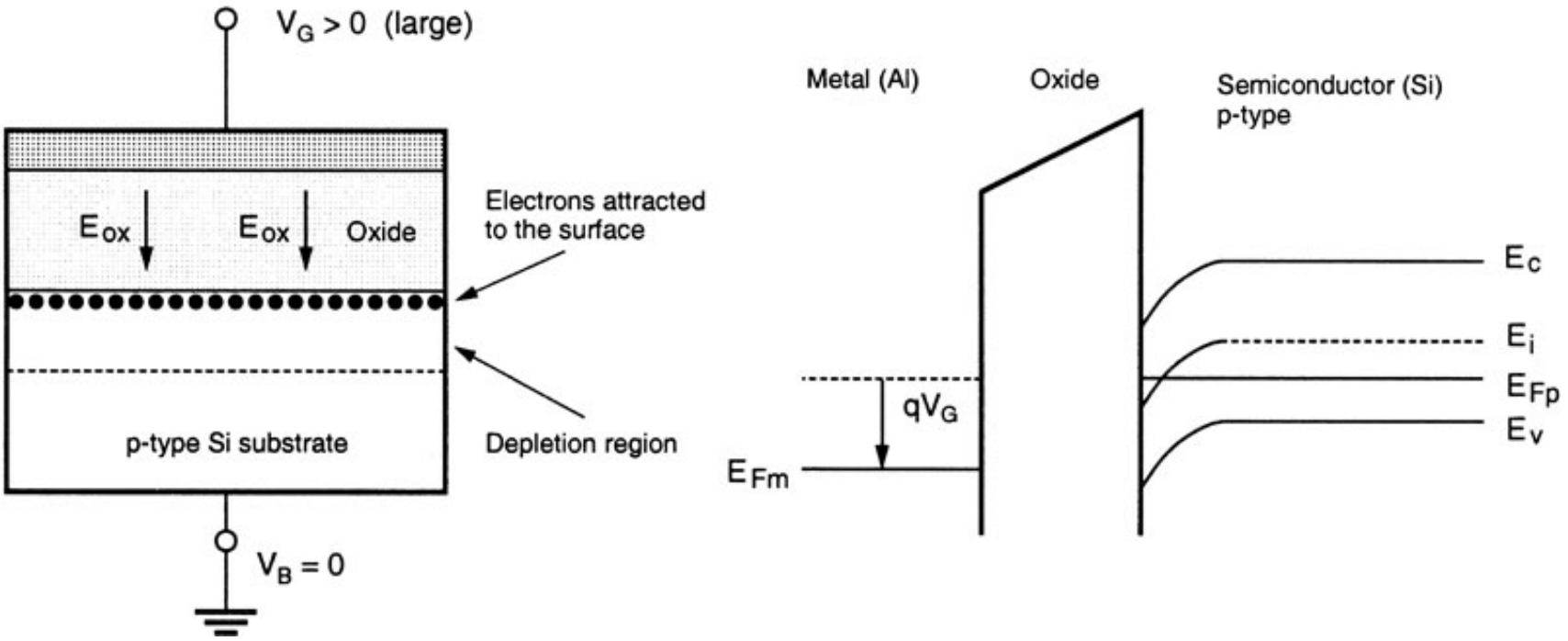
Two-Terminal MOS Structure Accumulation Region



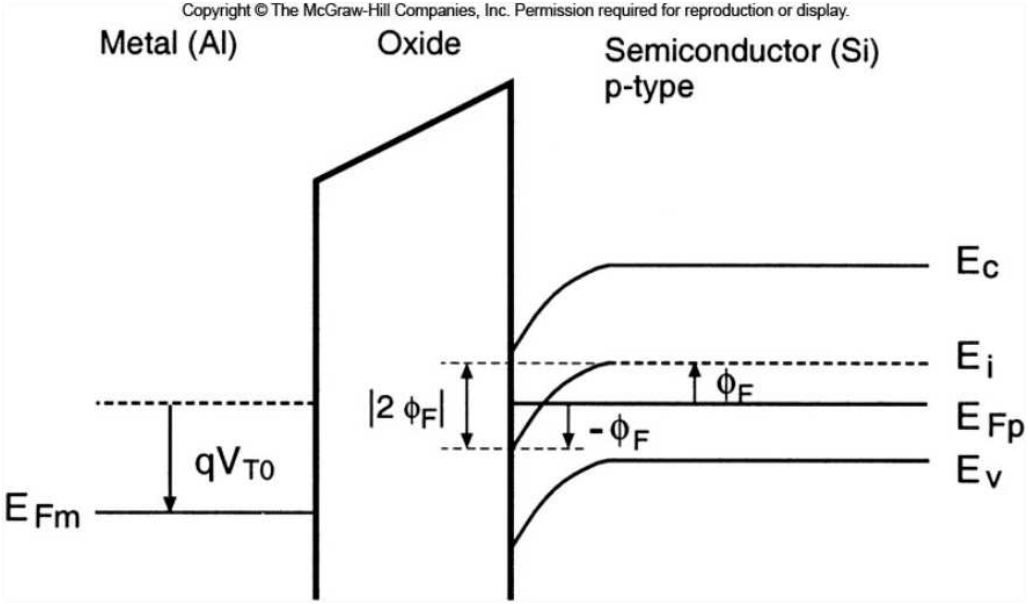
Two-Terminal MOS Structure Depletion Region



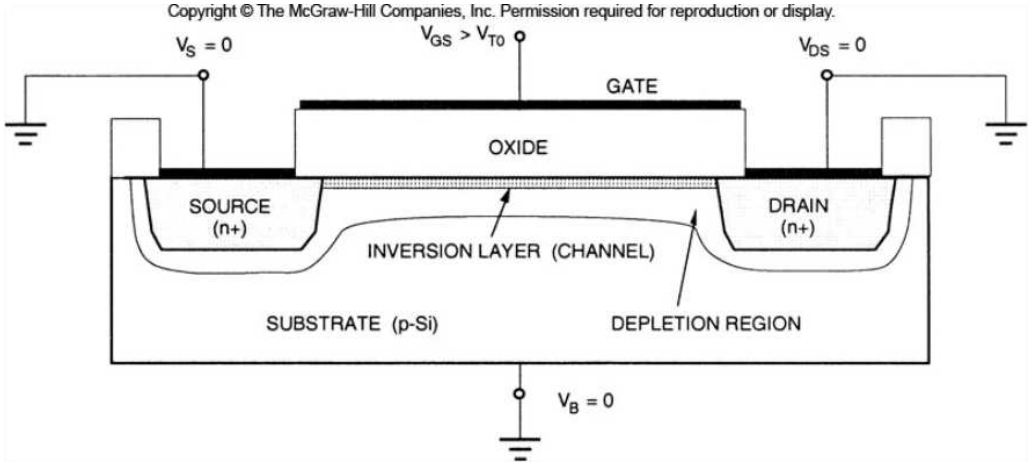
Two-Terminal MOS Structure Inversion Region



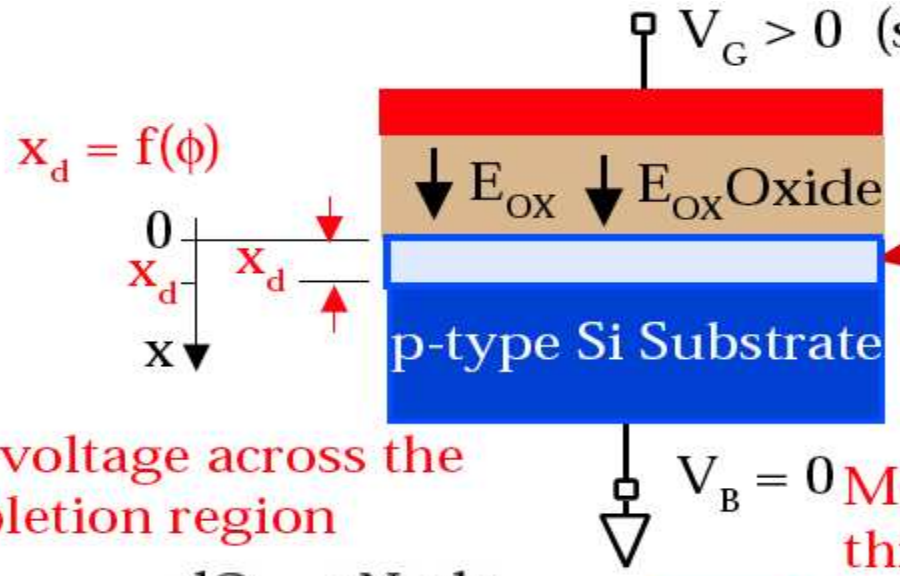
Two-Terminal MOS Structure Energy Band Diagram



Bending of the semiconductor bands at the onset of strong inversion: *the surface potential ϕ_s is twice the value of ϕ_F in the neutral p material.*



Two-Terminal MOS Structure Depletion Region



ϕ = voltage across the depletion region

$$dQ = -qN_A dx$$

Mobile hole charge density in thin layer parallel to Si-Oxide interface

(dV=dQ/C) $$d\phi = \frac{-x}{\varepsilon_{Si}} dQ = x \frac{qN_A}{\varepsilon_{Si}} dx$$

Change in surface potential to displace dQ by distance x into bulk (Poisson eq)

$$\int_{\phi_F}^{\phi_s} d\phi = \int_0^{x_d} x \frac{qN_A}{\varepsilon_{Si}} dx$$

$$\phi_s - \phi_F = \frac{qN_A}{2\varepsilon_{Si}} x_d^2$$

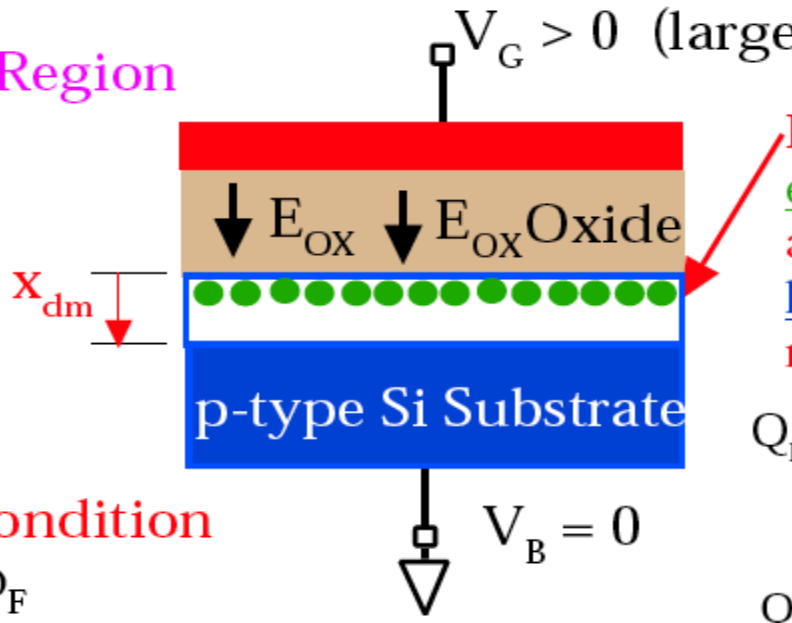
$$x_d = \sqrt{\frac{2\varepsilon_{Si}|\phi_s - \phi_F|}{qN_A}}$$

Depletion Region Charge Density

$$Q = -qN_A x_d = -\sqrt{qN_A \varepsilon_{Si} |\phi_s - \phi_F|}$$

Two-Terminal MOS Structure Inversion Region

Inversion Region



INVERSION Region
electrons
attracted to Si-Oxide interface
holes
repelled deeper into Si bulk

$$Q_{B0} = Q|_{x_d = x_{dm}} = -qN_A x_{dm}$$
$$= -\sqrt{qN_A \varepsilon_{Si} |-2\phi_F|}$$

Q_{B0} -> depletion charge density at surface inversion ($\phi = -\phi_F$)

Inversion Condition

$$\phi_s = -\phi_F$$

$$x_{dm} = x_d|_{\phi_s = -\phi_F} = \sqrt{\frac{2\varepsilon_{Si}|-2\phi_F|}{qN_A}}$$

$$\phi_{Fp} = \frac{kT}{q} \ln \frac{n_i}{N_A} \quad (N_A >> n_i)$$

$$\phi_{Fn} = \frac{kT}{q} \ln \frac{N_D}{n_i} \quad (N_D >> n_i)$$

$n_i = 1.45 \times 10^{10}$ cm^{-3} @ room temp,
$k = 1.38 \times 10^{-23}$ J/°K,
$q = 1.6 \times 10^{-19}$ C

=> $kT/q = 26$ mV @ room temp

Threshold Voltage for MOS Transistors

n-channel enhancement

For $V_{SB} = 0$, the threshold voltage is denoted as V_{T0} or $V_{T0n,p}$ [V_{T0} -> VT0 in SPICE]

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{B0}}{C_{ox}}$$

+ for nMOS
- for pMOS

V_{FB} -> Flat Band Voltage [V_{FB} = VFB in SPICE]

[$2\phi_F$ = PHI in SPICE]

$$Q_{B0} = -\sqrt{2qN_A\varepsilon_{Si}|-2\phi_F|}\ C/cm^2$$ [N_A = NSUB in SPICE]

Q_{B0} -> depletion charge density at surface inversion ($\phi_s = -\phi_F$)

Threshold Voltage factors:

-> Gate conductor material;

-> Gate oxide material & thickness;

-> Substrate doping;

-> Impurities in Si-oxide interface;

-> Source-bulk voltage V_{SB};

-> Temperature.

$$\Phi_{GC} = \phi_F(\text{substrate}) - \phi_M$$ metal gate

$$\Phi_{GC} = \phi_F(\text{substrate}) - \phi_F(\text{gate})$$ polysilicon gate

$\Phi_{GC} = \phi_{F(sub)} - \phi_{F(gate)}$ -> work funtion between gate and channe

$$Q_{ox} = qN_{ox}\ C/cm^2$$ [Q_{ox} = qNSS in SPICE]

Q_{ox} -> charge density at gate Si-oxide interface due to impurities and lattice imperfections at the interface.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$ - Gate oxide capacitance per unit area

Adjusting V_{T0} using an added Channel Implant

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{B0}}{C_{ox}}$$

Intrinsic V_{T0} - no channel implant adjustment

$$V'_{T0} = V_{T0} + \Delta V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{B0}}{C_{ox}} \pm \frac{qN_I}{C_{ox}}$$

Adjusted V'_{T0} – due to channel implant adjustment with carrier concentration N_I

$$\Delta V_{T0} = \pm \frac{qN_I}{C_{ox}}$$

$+\frac{qN_I}{C_{ox}}$ for p-type implant

$-\frac{qN_I}{C_{ox}}$ for n-type implant

NOTE: When channel implant adjustment N_I is done as a step in the CMOS process, the SPICE parameter VT0 refers to the adjusted threshold voltage V'_{T0}.

Threshold Voltage for MOS Transistors

n-channel enhancement $V_{T0} = V_{FB} - 2\phi_F - \frac{Q_{B0}}{C_{ox}}$ for $V_{SB} = 0$

For $V_{SB} \neq 0$: the threshold voltage is denoted as V_T or $V_{Tn,p}$

$$Q_B = -\sqrt{2qN_A\varepsilon_{Si}|-2\phi_F + V_{SB}|}\ , \quad Q_{B0} = -\sqrt{2qN_A\varepsilon_{Si}|-2\phi_F|}$$

$$V_T = V_{FB} - 2\phi_F - \frac{Q_{ox}}{C_{ox}} - \frac{Q_B}{C_{ox}}$$

$$= \underbrace{V_{FB} - 2\phi_F - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{B0}}{C_{ox}}}_{V_{T0}} - \frac{Q_B - Q_{B0}}{C_{ox}}$$

where

$$\frac{Q_B - Q_{B0}}{C_{ox}} = \underbrace{\sqrt{\frac{2qN_A\varepsilon_{Si}}{C_{ox}}}}\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

(γ = Body-effect coefficient) [γ = GAMMA in SPICE]

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

$$\gamma = \frac{\sqrt{2q \cdot N_A \cdot \varepsilon_{Si}}}{C_{ox}}$$ - Body-effect coefficient or substrate bias

Threshold Voltage for MOS Transistors

n-channel -> p-channel

****BE CAREFULL*** WITH SIGNS

- V_{FB} is negative in nMOS, positive in pMOS
- ϕ_F is negative in nMOS, positive in pMOS
- Q_{B0}, Q_B are negtive in nMOS, positive in pMOS
- γ is positive in nMOS, negative in pMOS
- V_{SB} is positive in nMOS, negative in pMOS

NOTE: $\gamma \propto \frac{C_{BC}}{C_{GC}}$

EXAMPLE 3.2 Calculate the threshold voltage V_{T0n} at $V_{BS} = 0$, for a polysilicon gate n-channel MOS transistor with the following parameters:

substrate doping density $N_A = 10^{16}\ cm^{-3}$,
gate oxide thickness $t_{ox} = 500$ Angstroms,
flat band voltage $V_{FB} = -1.04\ V$,
oxide-sub interface charge $N_{ox} = 0\ cm^{-2} \Rightarrow Q_{ox} = 0$

dielectric permativities: $\varepsilon_{ox} = 0.34 \times 10^{-12} Fcm^{-1}$, $\varepsilon_{Si} = 1.06 \times 10^{-12} Fcm^{-1}$

$$V_{T0n} = V_{FB} - 2\phi_{F(sub)} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{B0}}{C_{ox}}$$

$\phi_{F(sub)}$:

$$\phi_{F(sub)} = \frac{kT}{q} \ln \frac{n_i}{N_A} = 0.026V \ln\left(\frac{1.45 \times 10^{10}}{10^{16}}\right) = -0.35V$$

C_{ox}:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{0.34 \times 10^{-12}\ Fcm^{-1}}{500 \times 10^{-8}\ cm} = 6.8 \times 10^{-8}\ F/cm^2$$

EXAMPLE 3-2 CONT.

$$V_{T0n} = V_{FB} - 2\phi_{F(sub)} - \frac{Q_{B0}}{C_{ox}}$$

$\varepsilon_{ox} = 0.34 \times 10^{-12} \text{Fcm}^{-1}$,
$\varepsilon_{Si} = 1.06 \times 10^{-12} \text{Fcm}^{-1}$

Q_{B0}:

$$Q_{B0} = -\sqrt{2qN_A\varepsilon_{Si}\left|-2\phi_{F(sub)}\right|}$$

$$= -\sqrt{2(1.6\text{x}10^{-19}\,\text{C})(10^{16}\,\text{cm}^{-3})(1.06\text{x}10^{-12}\,\text{Fcm}^{-1})\,|2\text{x}0.35\,\text{V}|}$$

F = C/V

$$= -4.87 \times 10^{-8}\ \text{C/cm}^2$$

$$\frac{Q_{B0}}{C_{ox}} = \frac{-4.87\text{x}10^{-8}\,\text{C/cm}^2}{6.8\text{x}10^{-8}\,\text{F/cm}^2} = -0.72\ \text{V}$$

$$V_{T0n} = -1.04\,\text{V} - 2(-0.35\,\text{V}) - (-0.72\,\text{V}) = 0.38\,\text{V}$$

EXAMPLE 3.3 Consider the n-channel MOS transistor in Example 3.2:

substrate doping density $N_A = 10^{16}\ cm^{-3}$,
gate oxide thickness $t_{ox} = 500$ Angstroms,
substrate Fermi potential $\Phi_{F(sub)} = -0.35\ V$
zero subtrate bias threshold voltage $V_{T0n} = 0.38\ V$
dielectric permativities: $\varepsilon_{ox} = 0.34 \times 10^{-12} Fcm^{-1}$, $\varepsilon_{Si} = 1.06 \times 10^{-12} Fcm^{-1}$.

In digital circuit design, the condition $V_{SB} = 0$ can not always be quaranteed for all transistors. Plot the threshold voltage V_T as a function of V_{SB}.

$$V_{Tn} = V_{T0n} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

γ - Body-effect coefficient:

F = C/V

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{ox}} = \frac{\sqrt{2(1.6\times10^{-19}\,C)(10^{16}\,cm^{-3})(1.06\times10^{-12}\,Fcm^{-1})}}{6.8\times10^{-8}\,F/cm^2}$$

$$= \frac{5.824\times10^{-8}\,C/V^{-1/2}cm^2}{6.8\times10^{-8}\,C/Vcm^2} = 0.85\,V^{1/2}$$

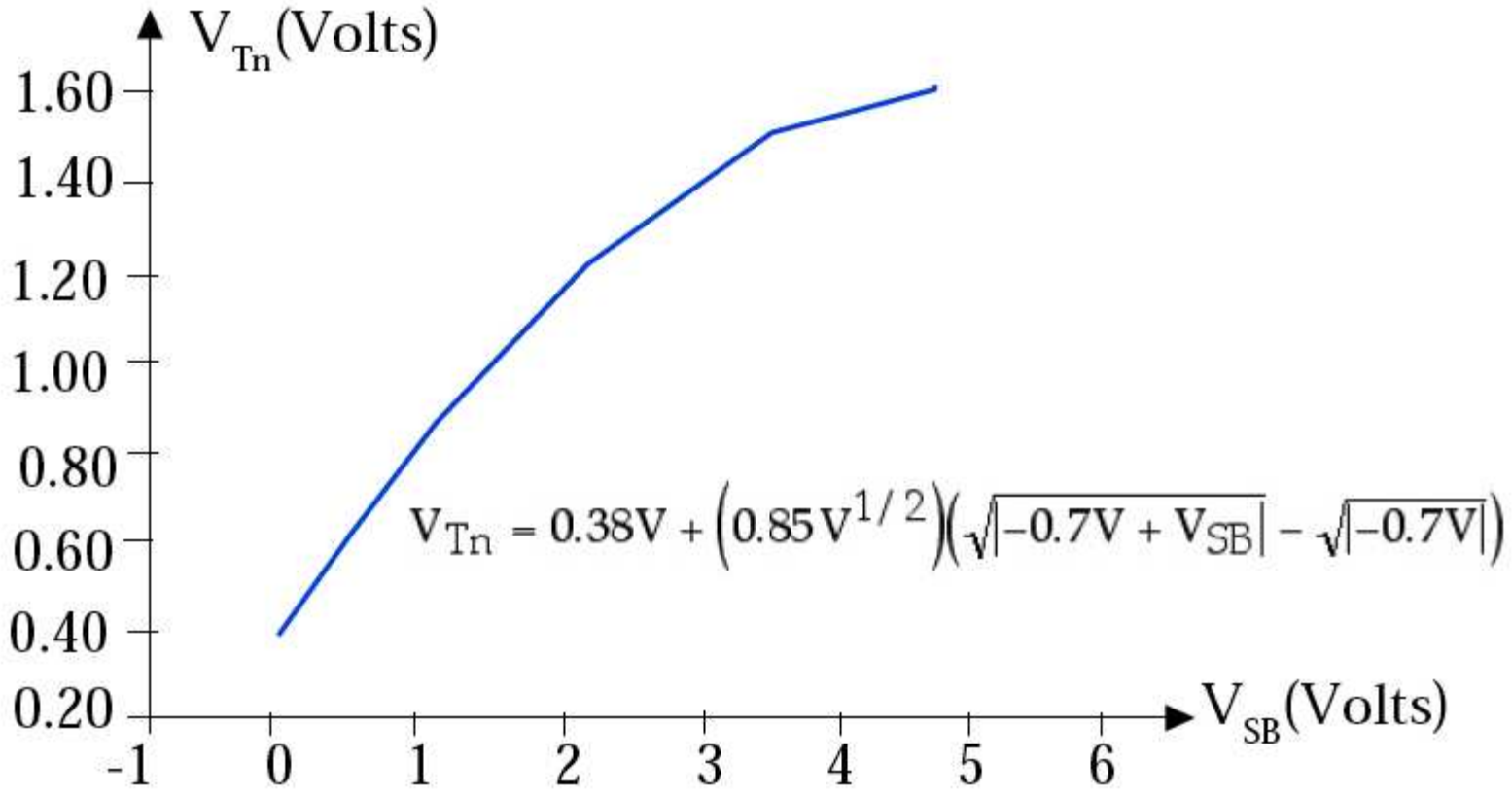
EXAMPLE 3-3 CONT.

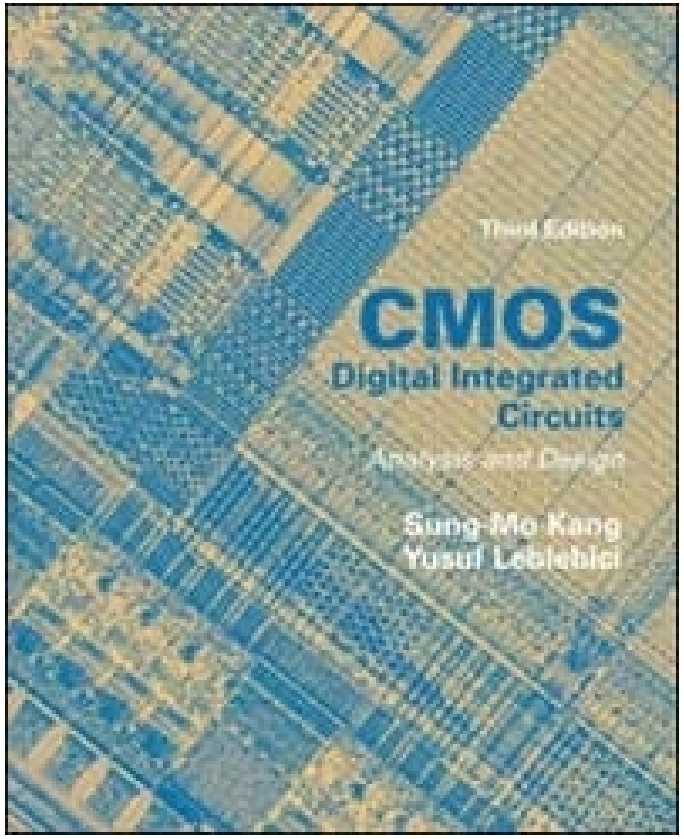
$$V_{Tn} = V_{T0n} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

where

$V_{T0n} = 0.38V$ (from EX 3-2)

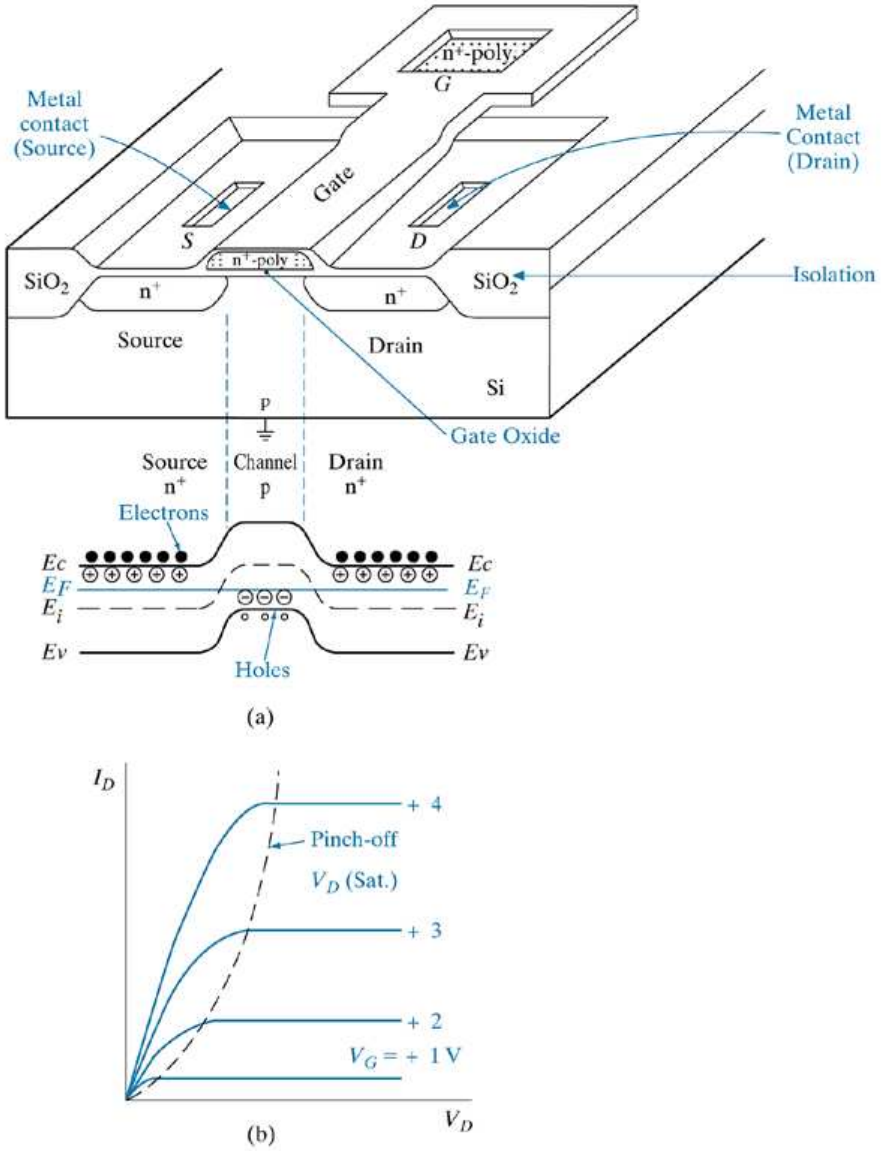
$\gamma = 0.85V^{1/2}$



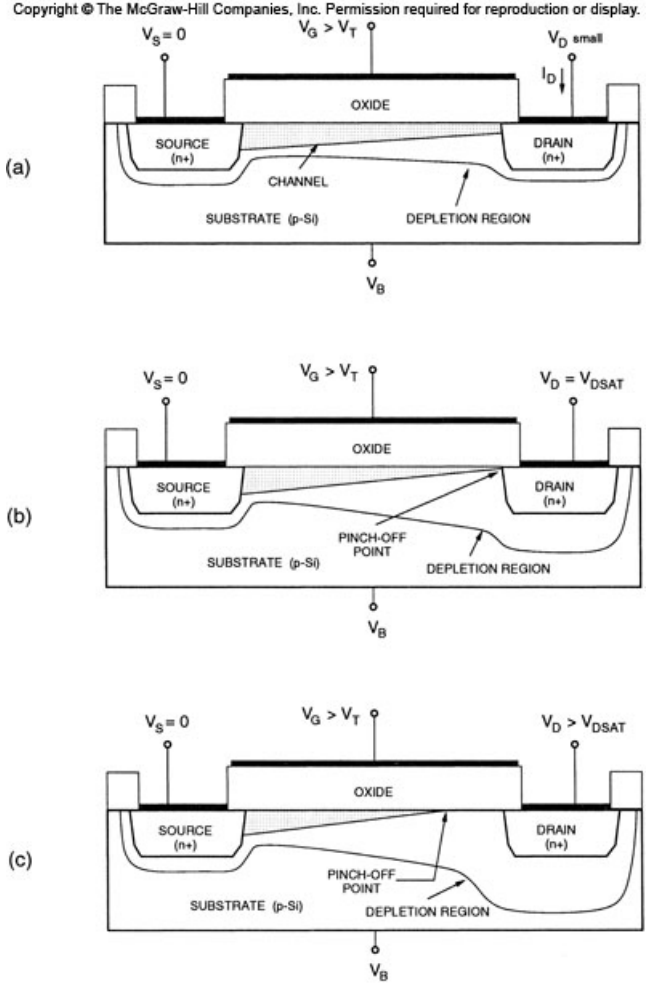


MOSFET I-V Characteristics

FET Band Diagram at Equilibrium



MOS Operation: A Qualitative View



n-channel MOSFET cross-sections under different operating conditions: (a) linear region for $V_G > V_T$ and $V_D < (V_G - V_T)$; (b) onset of saturation at pinch-off, $V_G > V_T$ and $V_D = (V_G - V_T)$; (c) strong saturation, $V_G > V_T$ and $V_D > (V_G - V_T)$.

I-V Equations of NFET

MOSFET CURRENT - VOLTAGE CHARACTERISTICS

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS} - V_{T0})V_{DS} - V_{DS}^2]$$

$$= \frac{k'}{2}\frac{W}{L}[2(V_{GS} - V_{T0})V_{DS} - V_{DS}^2] \qquad k' = \mu_n C_{ox}$$

[k' -> KP in SPICE]

$$= \frac{k}{2}[2(V_{GS} - V_{T0})V_{DS} - V_{DS}^2] \qquad k = k'\frac{W}{L}$$

NFET in saturation region

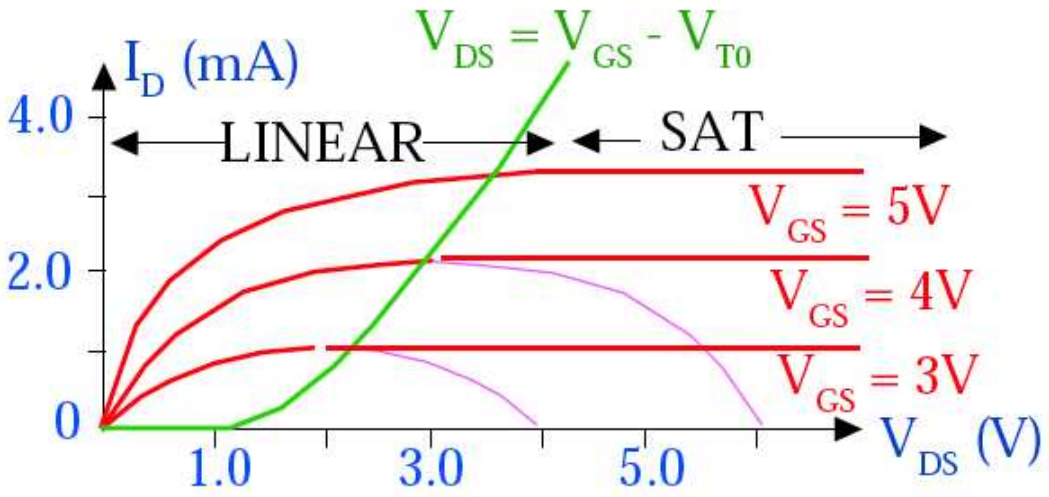
MOSFET CURRENT - VOLTAGE CHARACTERISTICS

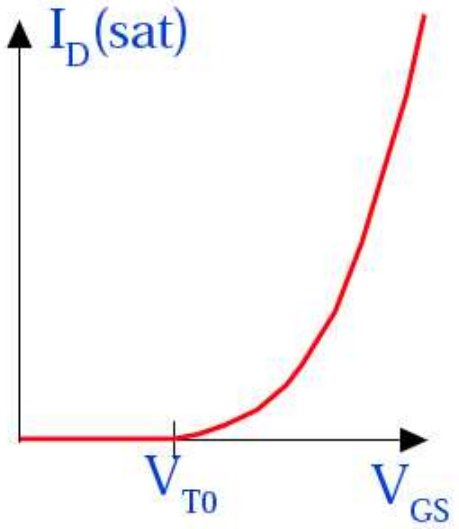
$V_{DS} \geq V_{GS} - V_{T0} = V_{DSAT}$ SATURATION REGION

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS}-V_{T0})V_{DS}-V_{DS}^2] \quad @V_{DS} = V_{DSAT} = V_{GS} - V_{T0}$$

$$= \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS}-V_{T0})(V_{GS}-V_{T0})-(V_{GS}-V_{T0})^2]$$

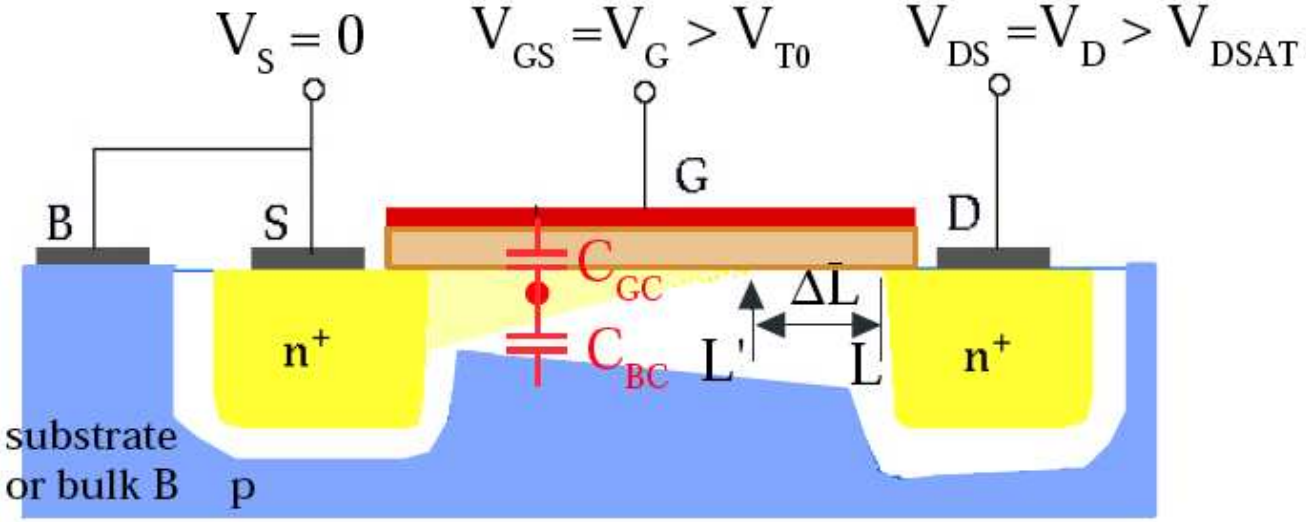
$$I_D(sat) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{T0})^2$$





NFET in saturation region: 2nd order effects

MOSFET CURRENT - VOLTAGE CHARACTERISTICS



$$I_D(sat) = \frac{\mu_n C_{ox}}{2}\frac{W}{L'}(V_{GS} - V_{T0})^2 = \frac{\mu_n C_{ox}}{2}\frac{W}{L(1-\frac{\Delta L}{L})}(V_{GS} - V_{T0})^2$$

where $\Delta L \propto \sqrt{V_{DS} - V_{DSAT}}$

emperical relation: $\frac{1}{1-\frac{\Delta L}{L}} = 1 + \lambda V_{DS}$ [λ -> LAMBDA in SPICE]

λ = channel length modulation coefficent (V^{-1})

NFET in saturation region: complete

MOSFET CURRENT - VOLTAGE CHARACTERISTICS

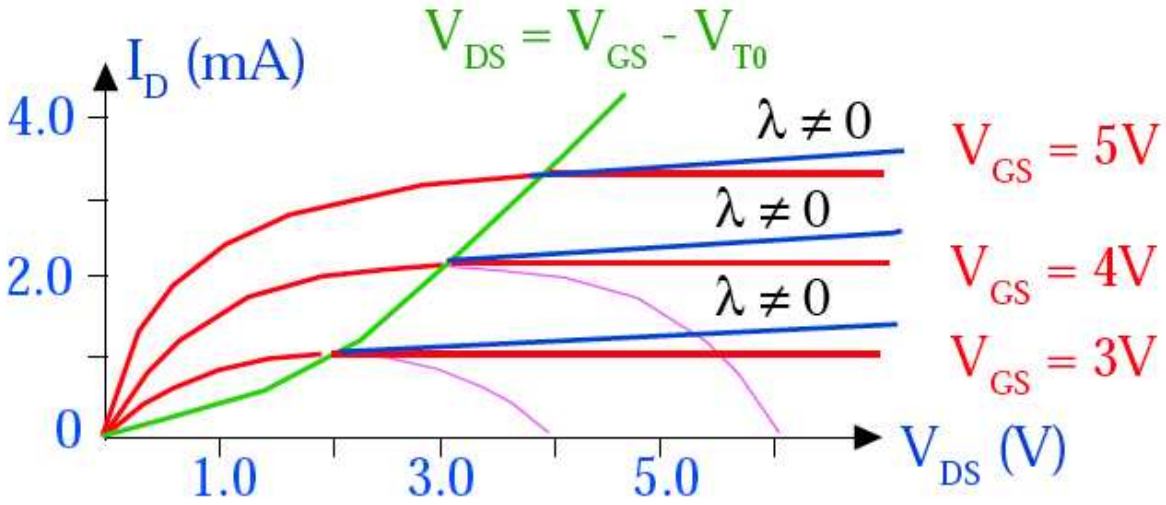
$$I_D(\text{sat}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L'}(V_{GS}-V_{T0})^2 = \frac{\mu_n C_{ox}}{2}\frac{W}{L(1-\frac{\Delta L}{L})}(V_{GS}-V_{T0})^2$$

$$\frac{1}{1-\frac{\Delta L}{L}} = 1+\lambda V_{DS} \qquad \text{assume } \lambda V_{DS} << 1$$

$$I_D(\text{sat}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{T0})^2(1+\lambda V_{DS})$$

$$I_D(\text{lin}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2(V_{GS}-V_{T0})V_{DS}-V_{DS}^2\right](1+\lambda V_{DS})$$

LEVEL 1 Model



Current-Voltage equation of the nMOS

$$I_D = 0 \qquad \text{for} \qquad V_{GS} < V_T \qquad (3.54)$$

$$I_D(lin) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2] \quad \text{for} \quad V_{GS} \geq V_T$$

$$\text{and} \quad V_{DS} < V_{GS} - V_T \qquad (3.55)$$

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad \text{for} \quad V_{GS} \geq V_T$$

$$\text{and} \quad V_{DS} \geq V_{GS} - V_T \qquad (3.56)$$

Current-Voltage equation of the pMOS

$$I_D = 0 \qquad \text{for} \qquad V_{GS} > V_T \qquad (3.57)$$

$$I_D(lin) = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2] \quad \text{for} \quad V_{GS} \le V_T$$

$$\text{and} \quad V_{DS} > V_{GS} - V_T \qquad (3.58)$$

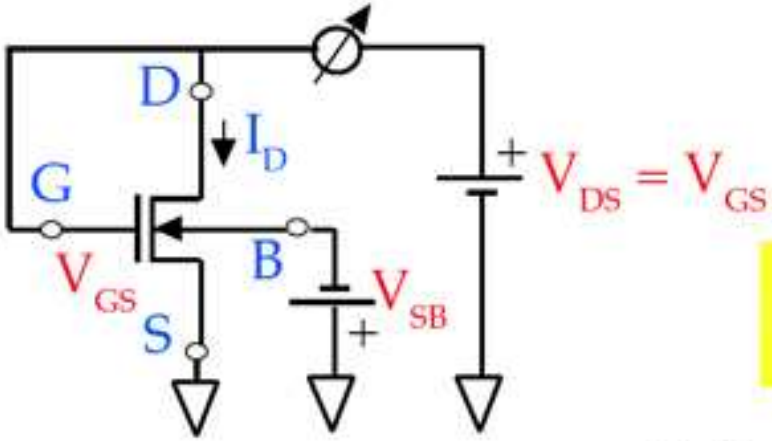
$$I_D(sat) = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad \text{for} \quad V_{GS} \le V_T$$

$$\text{and} \quad V_{DS} \le V_{GS} - V_T \qquad (3.59)$$

MOSFET CURRENT - VOLTAGE CHARACTERISTICS

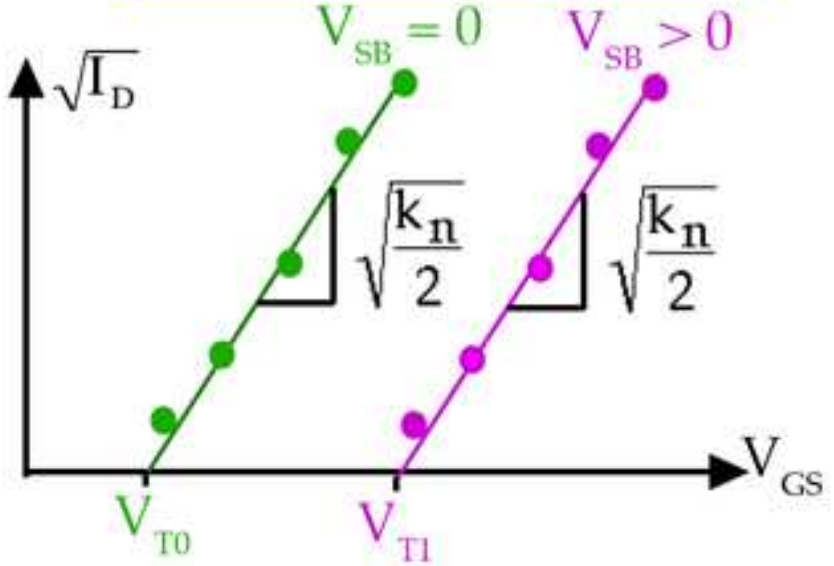
MEASUREMENT OF PARAMETERS (V_{T0}, γ, λ, k_n, k_p)

$$k_n = \mu_n C_{ox} \frac{W}{L} \qquad k_p = \mu_p C_{ox} \frac{W}{L}$$



$$I_D(sat) = \frac{k_n}{2}(V_{GS} - V_{T0})^2$$

$$\sqrt{I_D(sat)} = \sqrt{\frac{k_n}{2}}(V_{GS} - V_{T0})$$



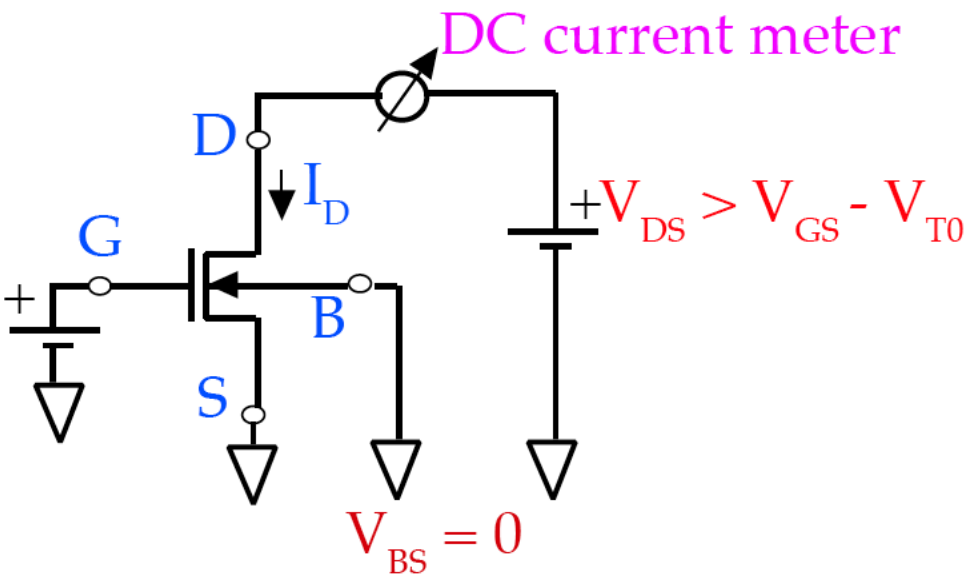
Gamma

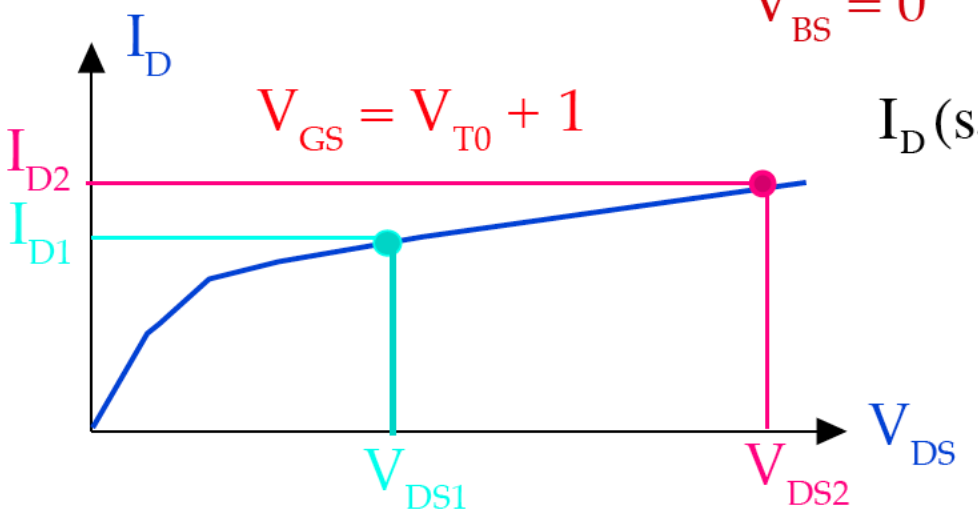
$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

$$\gamma = \frac{V_T(V_{SB}) - V_{T0}}{\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{-2\phi_F}}$$

MOSFET CURRENT - VOLTAGE CHARACTERISTICS

Lambda





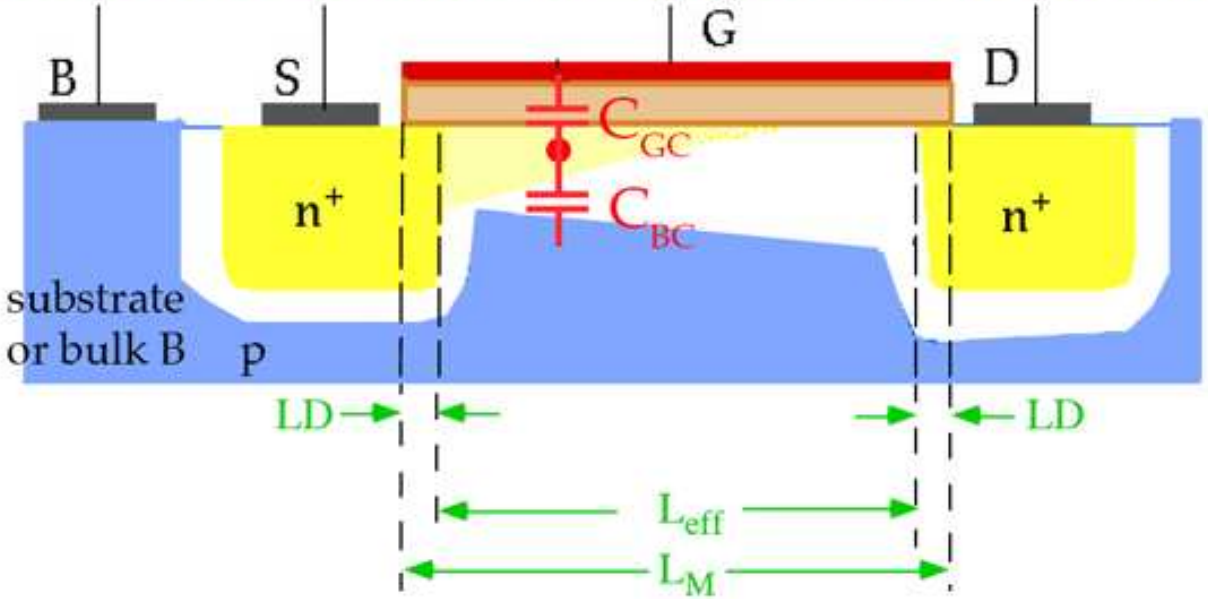
$$I_D(sat) = k_n(V_{GS} - V_{T0})^2(1 + \lambda V_{DS})$$

$$V_{GS} = V_{T0} + 1\ V$$

$$\frac{I_{D2}}{I_{D1}} = \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

$$\lambda = \frac{I_{D1} - I_{D2}}{V_{DS1}I_{D2} - V_{DS2}I_{D1}}$$

EFFECTIVE CHANNEL LENGTH AND WIDTH



SPICE Parameters

$L_{eff} = L_M - 2LD - DL$

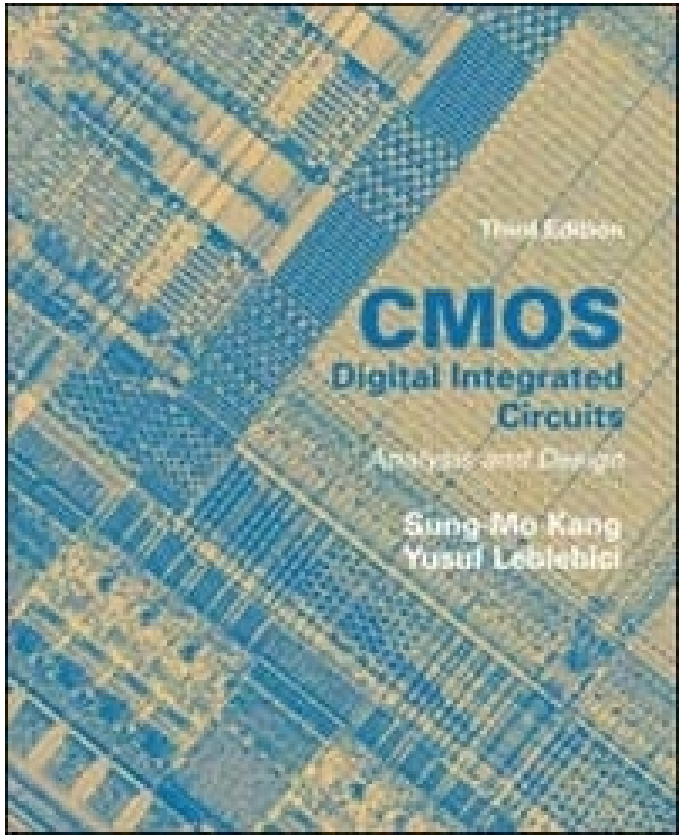
LD -> under diffusion

DL -> error in photolith and etch

$W_{eff} = W_M - DW$

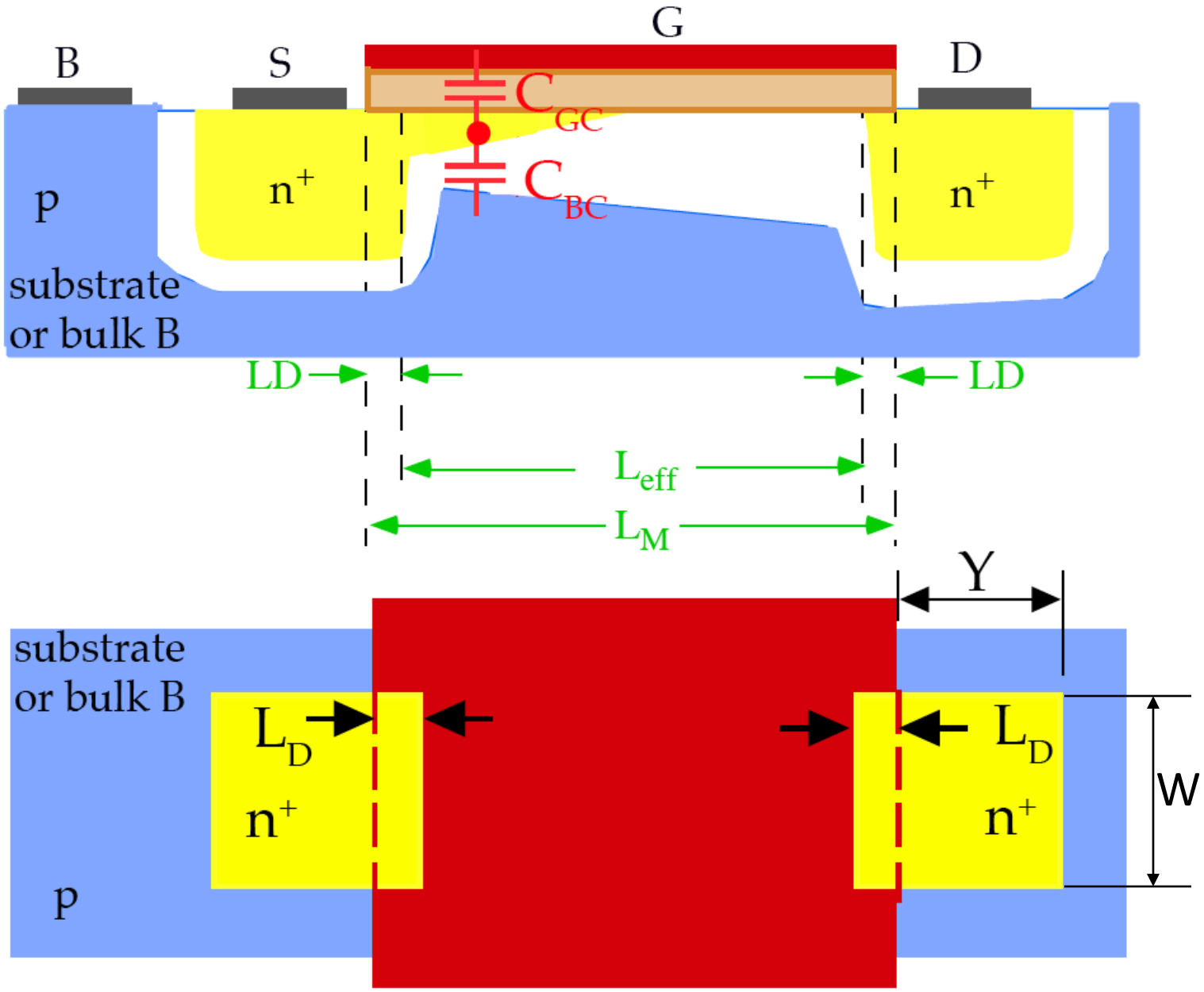
SPICE Parameters

DW -> error in photolith and etch

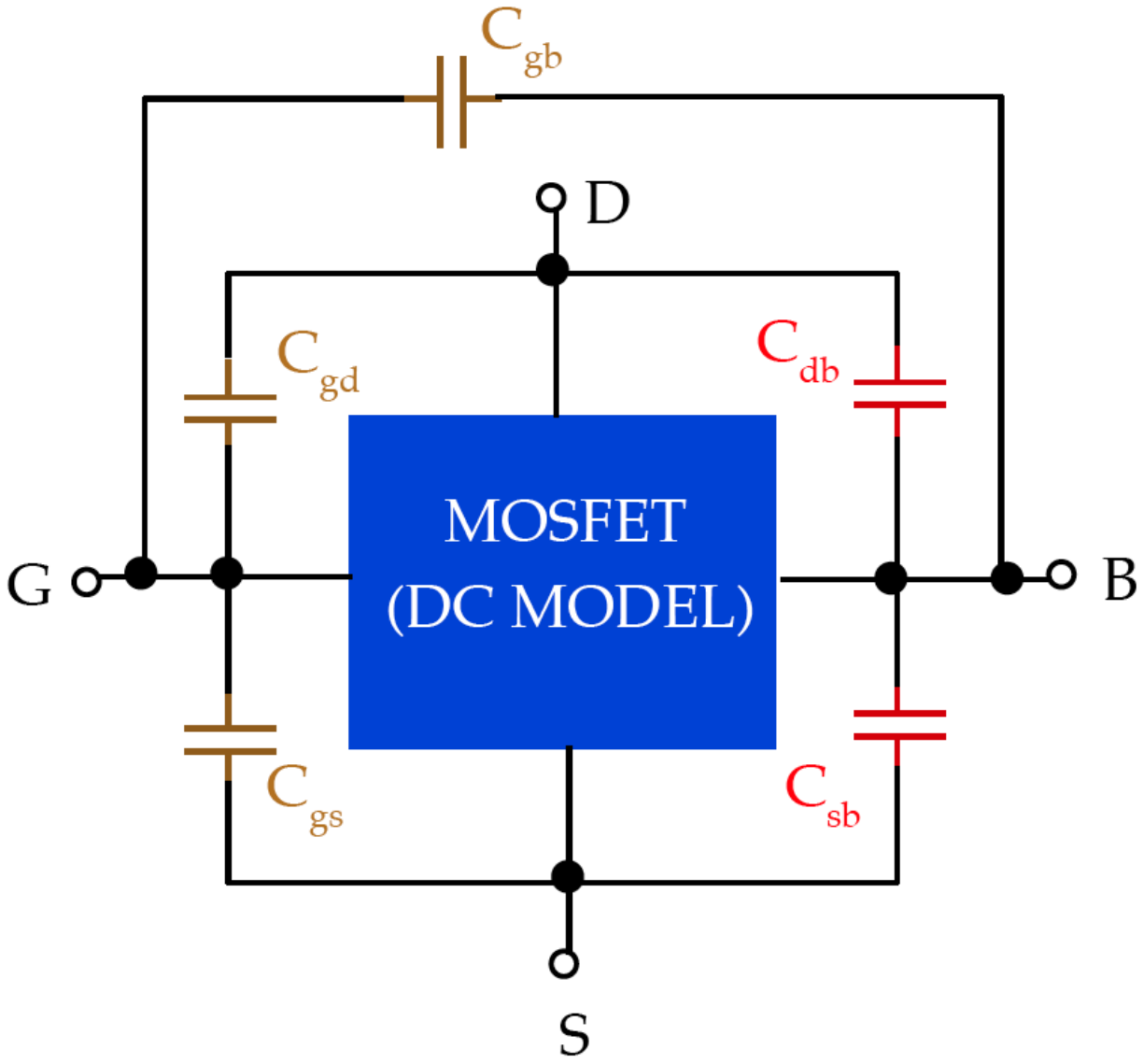


MOSFET Capacitance Models

MOSFET CAPACITANCES



MOSFET CAPACITANCES

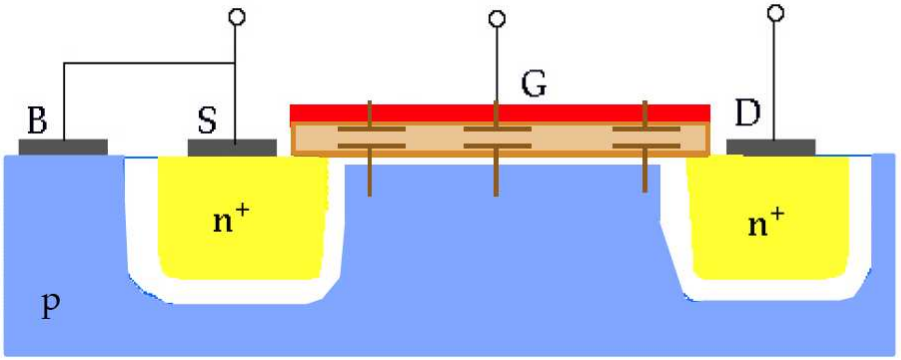


C_{gd}, C_{gs}, C_{gb} -> Oxide Capacitances

C_{db}, C_{sb} -> Junction Capacitances

b. Gate - Channel C_{gb}, C_{gb} and C_{gb}

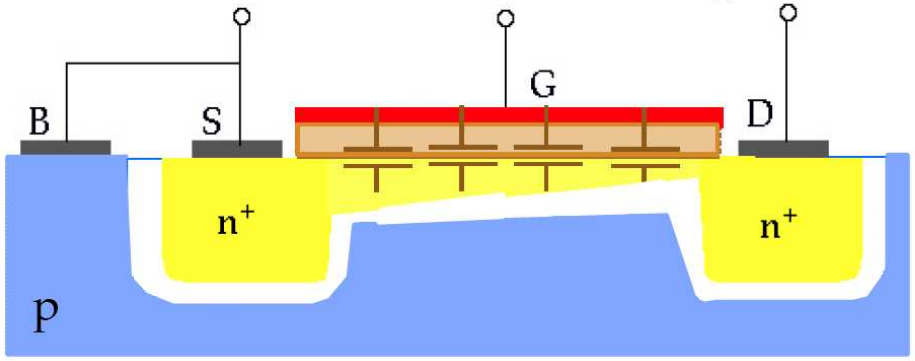
MOSFET - Cut-off Region



$C_{gb} = C_{ox} W L_{eff}$

$C_{gs} = C_{gd} = 0$ (no conducting channel in cut-off)

MOSFET - Linear Region

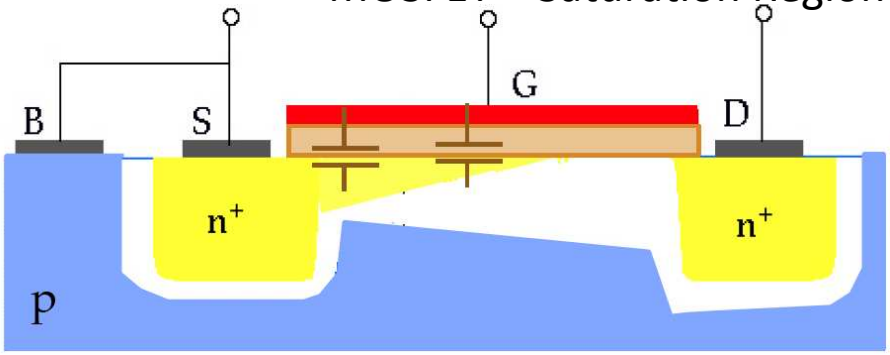


$C_{gb} = 0$

$C_{gs} = (1/2) C_{ox} W L_{eff}$

$C_{gd} = (1/2) C_{ox} W L_{eff}$

MOSFET – Saturation Region



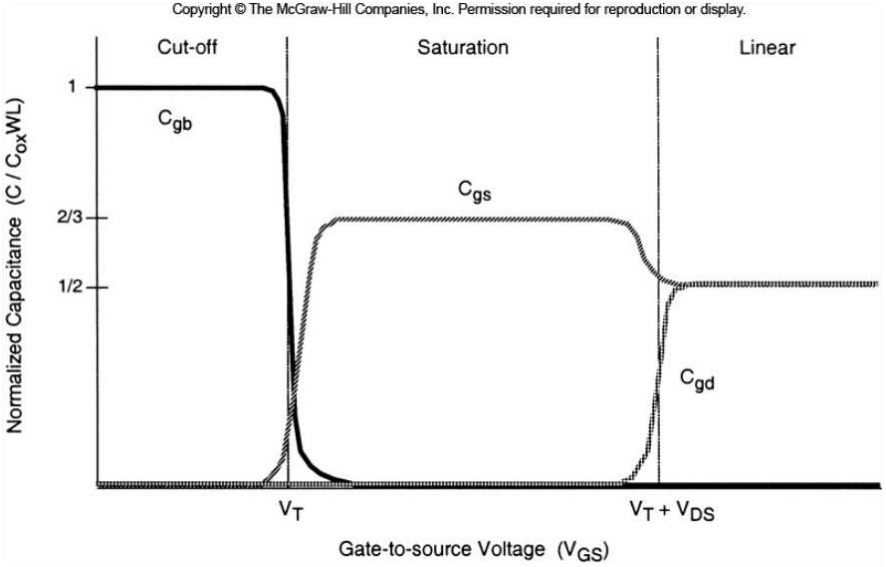
$C_{gb} = 0$

$C_{gs} = (2/3) C_{ox} W L_{eff}$

$C_{gd} = 0$

Capacitance Summary

Capacitance	Cut-off	Linear	Saturation
$C_{gb}(total)$	$C_{ox}WL_{eff} + C_{GB0}$	$0 + C_{GB0}$	$0 + C_{GB0}$
$C_{gd}(total)$	$0 + C_{GD0}$	$0.5C_{ox}WL_{eff} + C_{GD0}$	$0 + C_{GD0}$
$C_{gs}(total)$	$0 + C_{GS0}$	$0.5C_{ox}WL_{eff} + C_{GS0}$	$(2/3)C_{ox}WL_{eff} + C_{GS0}$



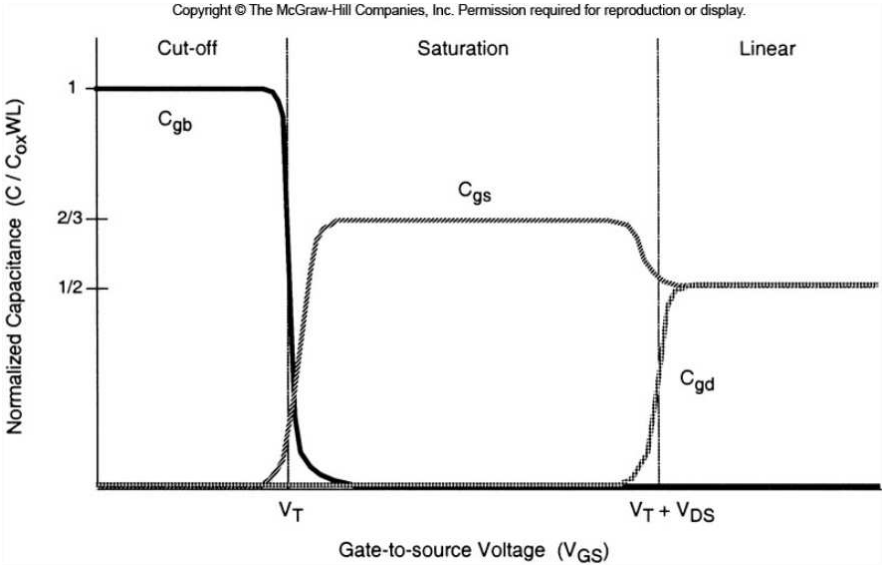
Capacitance Summary

Capacitance	Cut-off	Linear	Saturation
$C_{gb}(total)$	$C_{ox}WL_{eff} + C_{GB0}$	$0 + C_{GB0}$	$0 + C_{GB0}$
$C_{gd}(total)$	$0 + C_{GD0}$	$0.5C_{ox}WL_{eff} + C_{GD0}$	$0 + C_{GD0}$
$C_{gs}(total)$	$0 + C_{GS0}$	$0.5C_{ox}WL_{eff} + C_{GS0}$	$(2/3)C_{ox}WL_{eff} + C_{GS0}$

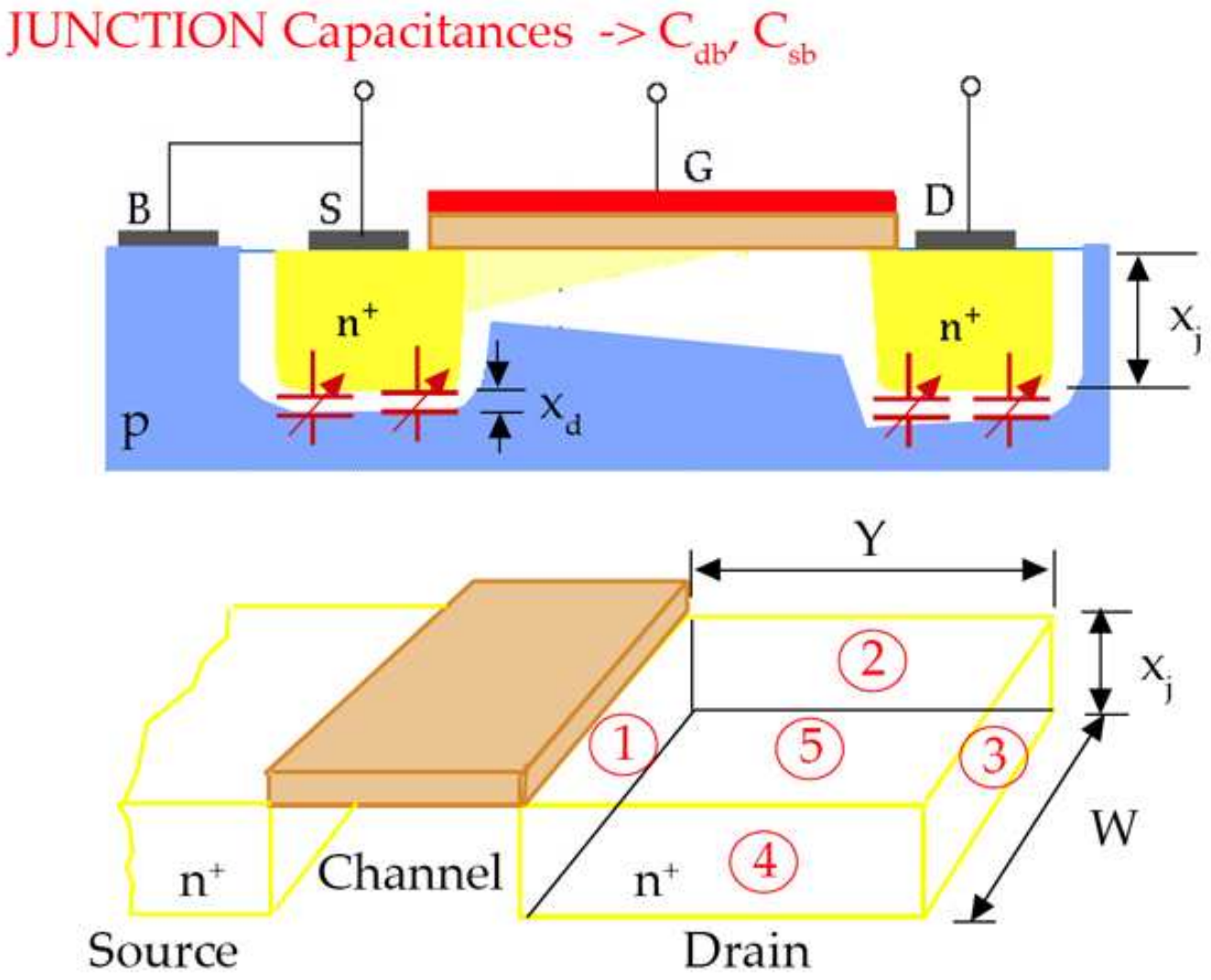
$C_{GS0} = C_{OX}WL_D$

$C_{GD0} = C_{OX}WL_D$

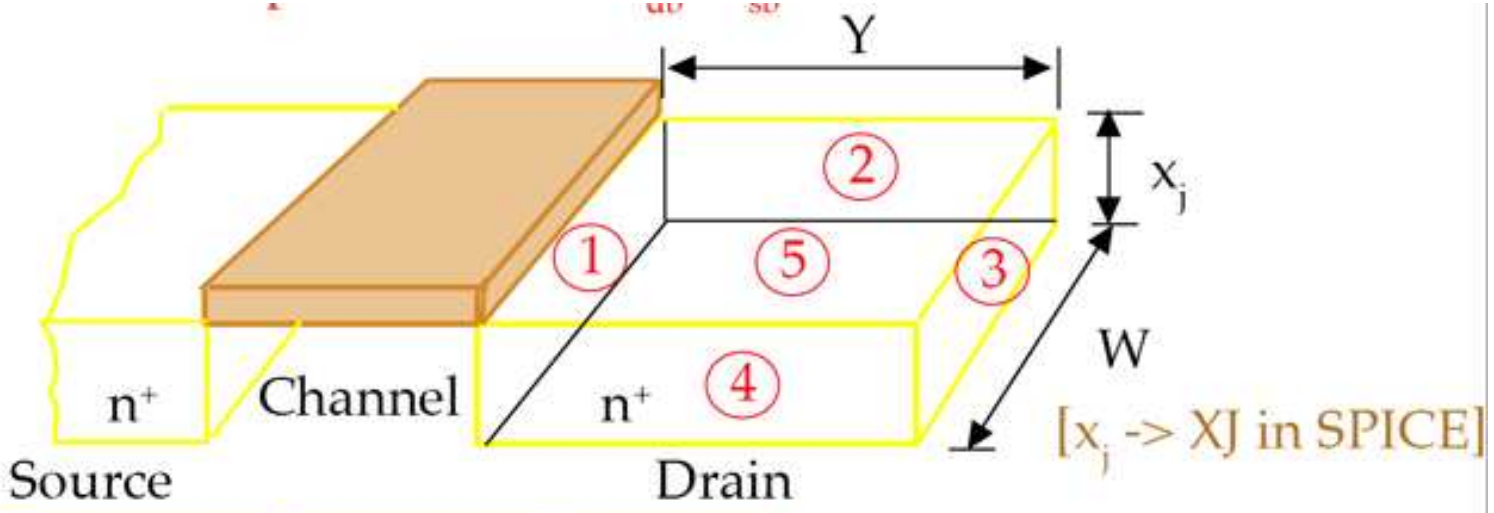
$C_{GB0} \sim 0$ (small)



Drain/Source Capacitance



Drain/Source Capacitance

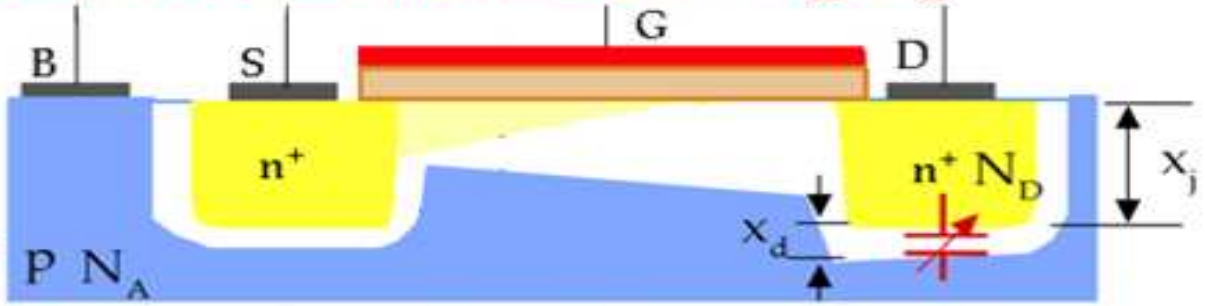


Junction	Area	Type
①	$W x_j$	n^+/p
②	$Y x_j$	n^+/p^+
③	$W x_j$	n^+/p^+
④	$Y x_j$	n^+/p^+
⑤	WY	n^+/p

p - Substrate -> N_A
p^+ - Channel-stop -> $10N_A$

Depletion Region Capacitance

Depletion Region Capacitances -> C_{db}, C_{sb}



n+, p junctions

$$x_d = \sqrt{\frac{2\varepsilon_{Si}}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(\phi_0 - V)}$$ ↔ V = Ext Bias --> V_{SB}, V_{DB}

$$\phi_0 = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)$$ built-in junction potential

Q_j = depletion-region charge

A = junction area

m = grading coefficient
m = ½ for abrupt junction

$$C_j(V) = \left|\frac{dQ_j}{dV}\right| = \frac{AC_{j0}}{\left(1-\frac{V}{\phi_0}\right)^m} = \frac{(AS, D)\cdot CJ}{\left(1-\frac{V}{PB}\right)^m} \quad (F)$$

[AS, AD -> Source, Drain Areas in SPICE]

[CJ -> C_{j0} in SPICE]

[PB -> ϕ_0 in SPICE]

[MJ -> m in SPICE]

where

$$CJ = C_{j0} = \sqrt{\frac{q\epsilon_{Si}}{2}\left(\frac{N_A N_D}{N_A + N_D}\right)\frac{1}{\phi_0}} \quad (F/cm^2)$$

Zero-bias junction capacitance per unit area

Depletion Region Capacitance

- Notice that external bias voltages V which can be V_{SB} or V_{DB} will be assigned as positive values but they should be used in all equations as negative numbers because source and drain are n^+ materials and bulk is p material.
- In all equations where we use V if voltage is given as positive value in the problem statement use it as negative value
- Please see Examples 3.8 and 3.9 from the textbook on pages 159 thru 162

Depletion Region Capacitance

n^+, p Junctions

$$C_j(V) = \left|\frac{dQ_j}{dV}\right| = \frac{AC_{j0}}{\left(1-\frac{V}{\phi_0}\right)^m} = \frac{(AS, D)\cdot CJ}{\left(1-\frac{V}{PB}\right)^{MJ}} \quad \text{(F)}$$

[AS, AD -> Source, Drain Areas in SPICE]

[CJ -> C_{j0} in SPICE]

[PB -> ϕ_0 in SPICE]

[MJ -> m in SPICE]

$$CJ = C_{j0} = \sqrt{\frac{q\epsilon_{Si}}{2}\left(\frac{N_A N_D}{N_A + N_D}\right)\frac{1}{\phi_0}} \quad \text{(F/cm}^2\text{)}$$

$C_j(V) = A\,C_{j0}$ when $V = 0$

EQUIVALENT LINEAR LARGE SIGNAL CAPACITANCE

$$C_j(V) \approx AC_{j0}\cdot\frac{-\phi_0}{(V_2 - V_1)(1-m)}\left[\left(1-\frac{V_2}{\phi_0}\right)^{1-m} - \left(1-\frac{V_1}{\phi_0}\right)^{1-m}\right]$$

$0 < K_{eq} < 1$ --> Voltage Equivalence Factor

where $V_1 \le V \le V_2$

V = Ext Bias --> V_{SB}, V_{DB}

$$C_j(V) = AC_{j0}K_{eq} = (AS, D)\cdot CJ\cdot K_{eq}$$

Depletion Region Capacitance

n^+, p^+ junctions (Sidewalls)

$$C_{j0sw} = \sqrt{\frac{\varepsilon_{Si}\, q}{2}\left(\frac{N_A(sw)N_D}{N_A(sw)+N_D}\right)\frac{1}{\phi_{0sw}}} \quad (F/cm^2)$$

[PS, PD -> Source, Drain Perimeters in SPICE]

[CJSW -> C_{jsw} in SPICE]

[PBSW -> ϕ_{0SW} in SPICE]

[MJSW -> m(sw) in SPICE]

[XJ -> x_j in SPICE]

Since all sidewalls have depth = x_j:

$$C_{jsw} = C_{j0sw}\, x_j \qquad (F/cm)$$

EQUIVALENT LARGE SIGNAL CAPACTIANCE

$$C_{jsw}(V) \approx PC_{jsw}K_{eq}(sw)$$

P = sidewall perimeter

$$K_{eq}(sw) = \frac{-\phi_{0sw}}{(V_2 - V_1)(1-m(sw))}\left[\left(1-\frac{V_2}{\phi_{0sw}}\right)^{1-m(sw)} - \left(1-\frac{V_1}{\phi_{0sw}}\right)^{1-m(sw)}\right]$$

m(sw) = ½ for an abrupt junction

EXAMPLE 4

Determine the total junction capacitance at the drain, i.e. C_{db}, for the n-channel enhancement MOSFET in Fig. 1. The process parameters are

$CJ = 1.35 \times 10^{-8}$ F/cm^2
$CJSW = 5.83 \times 10^{-12}$ F/cm
$PB = 0.896$ V
$PBSW = 0.975$ V
$XJ = 1 \times 10^{-4}$ cm
$MJ = MJSW = ½$

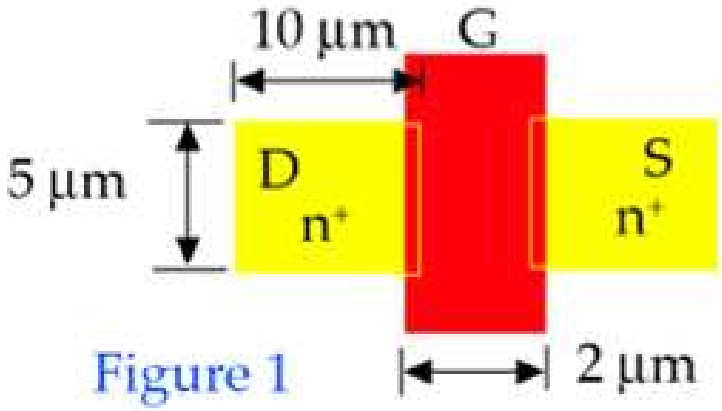


Figure 1

Source, Drain are surrounded by p^+ channel-stop. The substrate is biased at 0V. Assume the drain voltage range is 0.5 V to 5.0 V.

CJ = 1.35 x 10^{-8} F/cm^2
CJSW = 5.83 x 10^{-12} F/cm
PB = 0.896 V
PBSW = 0.975 V
XJ = 1 x 10^{-4} cm
MJ = MJSW = 1/2

$$C_j(V) = AC_{j0}K_{eq} = AD \cdot CJ \cdot K_{eq}$$

V2 = -5V and V1 = -0.5V

$$K_{eq} = \frac{-PB}{(V_2 - V_1)(1-MJ)}\left[\left(1-\frac{V_2}{PB}\right)^{1-MJ} - \left(1-\frac{V_1}{PB}\right)^{1-MJ}\right]$$

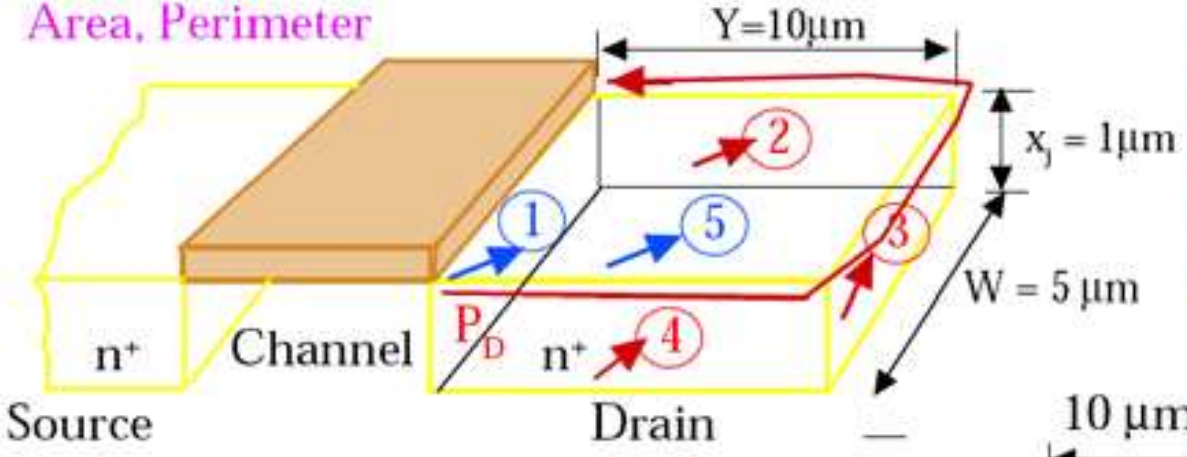
$$= \frac{2 \cdot 0.896\,V}{(5\,V - 0.5\,V)}\left[\left(1+\frac{5\,V}{0.896\,V}\right)^{1/2} - \left(1+\frac{0.5\,V}{0.896\,v}\right)^{1/2}\right] = 0.52$$

$$C_{jsw}(V) = PC_{jsw}K_{eq}(sw) = PD \cdot CJSW \cdot K_{eq}(sw)$$

$$K_{eq}(sw) = \frac{-PBSW}{(V_2 - V_1)(1-MJSW)}\left[\left(1-\frac{V_2}{PBSW}\right)^{1-MJSW} - \left(1-\frac{V_1}{PBSW}\right)^{1-MJSW}\right]$$

$$= \frac{2 \cdot 0.975\,V}{(5\,V - 0.5\,V)}\left[\left(1+\frac{5\,V}{0.975\,V}\right)^{1/2} - \left(1+\frac{0.5\,V}{0.975\,v}\right)^{1/2}\right] = 0.53 \approx K_{eq}$$

Area, Perimeter



CJ = 1.35 x 10^{-8} F/cm^2
CJSW = 5.83 x 10^{-12} F/cm
PB = 0.896 V
PBSW = 0.975 V
XJ = 1 x 10^{-4} cm
MJ = MJSW = 1/2

A_D: n+/p junctions:

A_D = (5 x 1) μm^2 + (10 x 5) μm^2
= 55 μm^2

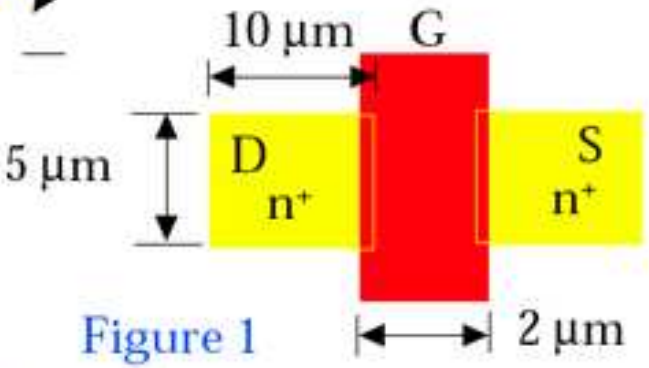


Figure 1

P_D: n+/p+ junctions:

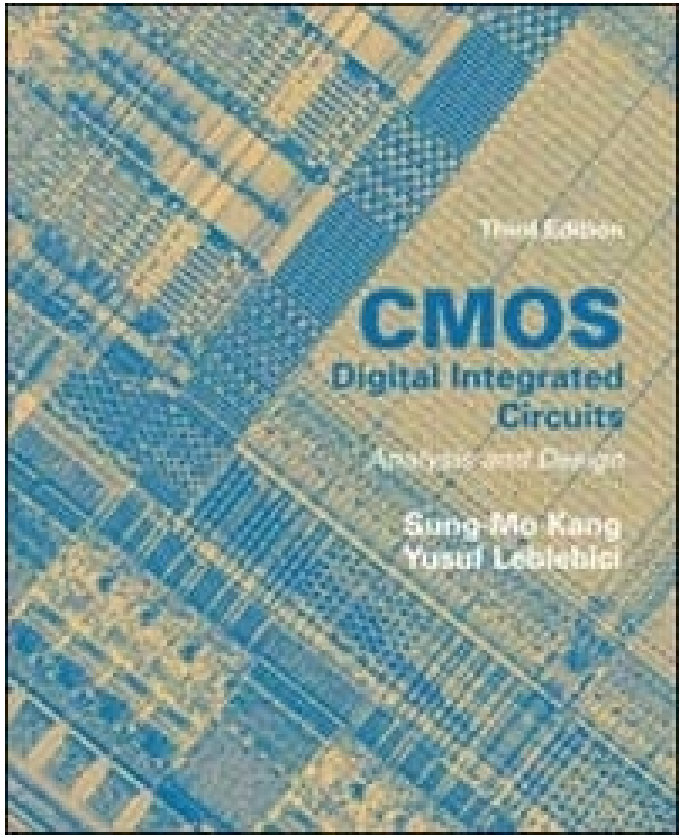
P_D = 2Y + W = 20 μm + 5 μm = 25 μm

$$C_j(V) = AC_{j0}K_{eq} = AD \cdot CJ \cdot K_{eq} = (55 \times 10^{-8}\, cm^2) \cdot (1.35 \times 10^{-8}\, F/cm^2) \cdot 0.52 = 3.86\, fF$$

$$C_{jsw}(V) = PC_{jsw}K_{eq}(sw) = PD \cdot CJSW \cdot K_{eq}(sw)$$

$$= (2.5 \times 10^{-3}\, cm) \cdot (5.83 \times 10^{-12}\, F/cm) \cdot 0.53 = 7.72\, fF$$

$$C_{db} = AD \cdot CJ \cdot K_{eq} + PD \cdot CJSW \cdot K_{eq}(sw) = 11.58\, fF$$



MOSFET Scaling

MOSFET - SCALING

SCALING -> refers to ordered reduction in dimensions of the MOSFET and other VLSI features

- Reduce Size of VLSI chips.
- Change operational charateristics of MOSFETs and parasitics.
- Phyiscal limits restrict degree of scaling that can be achieved.

SCALING FACTOR = $\alpha > 1$ --> S

First-order "constant field" MOS scaling theory:

The electric field E is kept constant, and the scaled device is obtained by applying a dimensionless scale-factor α to reduce dimensions by $(1/\alpha)$ and maintain E unchanged:

a. All dimensions, including those vertical to the surface $(1/\alpha)$

b. device voltages $(1/\alpha)$

c. the concentration densities (α).

$(1/\alpha)/(1/\alpha) = 1$ $\qquad$ $\alpha(1/\alpha) = 1$

$E_{ox} = V_{GS} / t_{ox}$ <=> $E = \frac{q}{\varepsilon} N_A x$

MOSFET - SCALING

Alternative Scaling Rules:

Constant Voltage Scaling, i.e. V_{DD} is kept constant, while the process dimensions are scaled by $(1/\alpha)$.

a. All dimensions, including those vertical to the surface $(1/\alpha)$

b. device voltages (1)

c. the concentration densities (α^2) to preserve charge-field relations.

$1/(1/\alpha) = \alpha$ $\qquad$ $\alpha^2(1/\alpha) = \alpha$

$E_{ox} = V_{GS} / t_{ox}$ $\quad <=> \quad$ $E = \frac{q}{\varepsilon} N_A x$

Lateral Scaling: only the gate length is scaled $L = 1/\alpha$ (gate-shrink).

Scaling Effects

Influence of Scaling on MOS Device Performance

PARAMETER	SCALING MODEL		
	Constant Field	Constant Voltage	Lateral
Length (L)	$1/\alpha$	$1/\alpha$	$1/\alpha$
Width (W)	$1/\alpha$	$1/\alpha$	1
Supply Voltage (V)	$1/\alpha$	1	1
Gate Oxide thickness (t_{ox})	$1/\alpha$	$1/\alpha$	1
Junction depth (X_j)	$1/\alpha$	$1/\alpha$	1
Substrate Doping (N_A)	α	α^2	1
Current (I) - (W/L) $(1/t_{ox})V^2$	$1/\alpha$	α	α
Power Dissipation (P) - IV	$1/\alpha^2$	α	α
Power Density (P/Area)	1	**(α^3)**	α^2
Electric Field Across Gate Oxide - V/t_{ox}	1	α	1
Load Capacitance (C) - WL $(1/t_{ox})$	$1/\alpha$	$1/\alpha$	$1/\alpha$
Gate Delay (T) - VC/I	$1/\alpha$	$1/\alpha^2$	$1/\alpha^2$

Important 2nd Order Effects

Short Channel Effects - L_{eff} --> x_j

Narrow Channel Effects - W --> x_{dm}

Subthreshold Current - $V_{GS} < V_{T0}$

Short Channel Effect - L_{eff} --> x_j (source, drain diffusion depth)

V_{T0} (short channel) = V_{T0}(long channel) - ΔV_{T0}

$$\Delta V_{T0} \approx 8.15 \times 10^{-20} \eta \frac{v_{DS}}{L_{eff}^3 C_{ox}} \qquad \text{(Lvl 3)}$$

[SPICE Parameter: ETA -> η = imperical parameter]

Narrow Channel Effect - W --> x_{dm} (depletion region depth)

V_{T0} (narrow channel) = V_{T0}(long channel) + ΔV_{T0}

$$\Delta V_{T0} \approx \frac{\delta(\pi \epsilon_{Si} |2\Phi_F|)}{4 W C_{ox}} \qquad \text{(Lvl 2 \& 3)}$$

[SPICE Parameter: DELTA -> δ = imperical parameter]

Subthreshold Current - $V_{GS} < V_{T0}$

$$I_D(weak\ inversion) = I_{on} e^{(V_{GS} - V_{on})/(q/nkT)} \qquad \text{(Spice Model)}$$

$I_{on} = I_D$ in strong inversion and $V_{GS} = V_{on}$ is the boundary weak and strong inversion