CSE 463-563: Digital Integrated Circuits Design and Architecture

Prof. Darko Ivanovich

Exam 2: Inverters and Combinational Logic Circuits

(Take home exam, Open book, Open notes, Internet search, Calculator or Wolfram-Alpha app are allowed)

Due April 18th, 2023

Attempt all questions. Show all calculations to obtain partial credits. If you run out of time, outline how you would approach the problem.

Total possible points: 200 for CSE463 students (Problems 1, 2, and 3)
270 for CSE563 students (Problems 1, 2, 3, and 4)

My phone number for any question you have is 314-537-4124.
Please text me and I will answer quickly.

Student name: Byeongchan Gwak

CSE463 students will work on Problems P1, P2 and P3

CSE563 students will work on Problems P1, P2, P3 and P4

Problem P1. (50pts)

Design a 3-input CMOS NOR gate with logic threshold voltage of $V_{DD}/3$.

(a) Find ratio k_p/k_n for $V_{TH} = V_{DD}/3$. (10pts)

(b) The 3-input CMOS NOR gate should have a maximum fall time τ_{fall} of 1ns for 100fF load capacitance. Use this fall time requirement to determine proper size of nMOS transistors $(W/L)_n$. (15pts)

(c) From (a) and (b) determine proper size of pMOS transistors $(W/L)_p$. (15pts)

(d) Select W_n, L_n, W_p and L_p using calculations from (b) and (c). (10pts)

Assume $k_n' = 100\mu A/V^2$, $k_p' = 100\mu A/V^2$, $V_{DD}=5V$, $V_{T0n} = 1V$, $|V_{T0p}| = 1V$, $\gamma=0$ and $\lambda=0\ V^{-1}$.

1. (a)

Since $V_{th} = \frac{V_{DD}}{3}$,

we have $k_{p,eq} = \frac{k_p}{3}$

$k_{n,eq} = 3k_n$

$$V_{th} = \frac{V_{TO,n} + \sqrt{\frac{k_{p,eq}}{k_{n,eq}}}\left(V_{DD} + V_{TO,p}\right)}{1 + \sqrt{\frac{k_{p,eq}}{k_{n,eq}}}}$$

$$V_{th} = \frac{V_{DD}}{3} = \frac{5}{3} = \frac{1 + \sqrt{\frac{1}{9}\cdot\frac{k_p}{k_n}}\ (5-1)}{1 + \sqrt{\frac{1}{9}\frac{k_p}{k_n}}}$$

And we have $k_n' = k_p'$,

$$\frac{5}{3} = \frac{1 + \frac{4}{3}\sqrt{\frac{k_p}{k_n}}}{1 + \frac{1}{3}\sqrt{\frac{k_p}{k_n}}}$$

$$\boxed{\frac{k_p}{k_n} = 0.73469}$$

(b) $$1ns > \tau_{fall} = \frac{C_{load}}{3k_n(V_{DD} - V_{TO,n})}\left[\frac{2(V_{TO,n} - 0.1V_{DD})}{V_{DD} - V_{TO,n}} + \ln\left(\frac{2(V_{DD} - V_{TO,n})}{0.1V_{DD}} - 1\right)\right]$$

$$1ns > \frac{100\times10^{-15}}{3\times100\times10^{-6}\left(\frac{W}{L}\right)_n(5-1)}\left[\frac{2(1-0.5)}{5-1} + \ln\left(\frac{2(5-1)}{0.5} - 1\right)\right]$$

$$1ns > \frac{10^{-9}}{3\times4\times\left(\frac{W}{L}\right)_n}\left[\frac{1}{4} + \ln(15)\right]$$

$$\boxed{\left(\frac{W}{L}\right)_n > 0.2465}$$

(c) From the answers above.

$k_p = 0.73469 k_n$, $\left(\frac{W}{L}\right)_n > 0.2465$

I will choose $L_n = 600$ nm $W_n = 1800$ nm.

$$\boxed{k_p = \left(\frac{W}{L}\right)_p = 0.73469 \times \frac{1800}{600} = 2.204}$$

(d) $L_n = 600$ nm , $W_n = 1800$nm , $L_p = 600$ nm

$$k_p = \left(\frac{W}{L}\right)_p = 2.204$$

$$\frac{W_p}{600} = 2.204$$

$$W_p = 1322$$

so, $W_p = 1322$ nm

Hence.

$$\boxed{L_n = 600\text{nm}, \ W_n = 1800\text{nm}, \ L_p = 600\text{nm}, \ W_p = 1322\text{nm}.}$$

Problem P2. (70pts)

Consider the following function: $Z = (A + B + C)(D + E)F$.

(a) Draw the pMOS and nMOS CMOS transistors schematic of the function Z. Assume that all signals and their respective inverse signals are available for the design. (10 pts)

(b) If all transistors are implemented with $W/L = 1$, $k_p' = k_n' = 100\mu A/V^2$, $V_{DD} = 5V$, $V_{T0n} = 1V$ and $|V_{T0p}| = 1V$, what is the value of the logic threshold, V_{TH}, when all inputs are connected to V_{TH}? (10 pts)

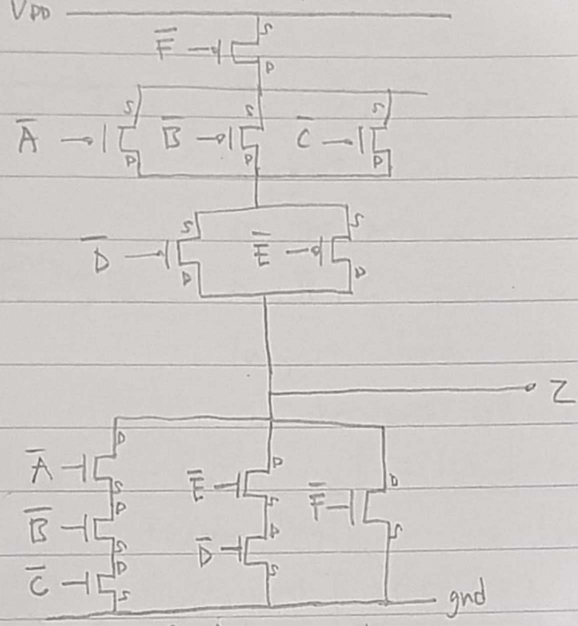
(c) Which transitions will have the longest rise and fall times? (10 pts)

(d) Calculate the longest rise time for C_{load} of 100fF. (20 pts)

(e) What is the common Euler path for the pMOS and nMOS network of transistors? Draw the optimized stick-diagram layout. (20 pts)

2 (a) $Z = (A+B+C)(D+E)F$

$\bar{Z} = \overline{\bar{A}\bar{B}\bar{C} + \bar{D}\bar{E} + \bar{F}}$



(b) $$\left(\frac{W}{L}\right)_{n,eq} = \left(\frac{W}{L}\right)_{\bar{F}} + \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_{\bar{E}}} + \frac{1}{\left(\frac{W}{L}\right)_{\bar{D}}}} + \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_{\bar{A}}} + \frac{1}{\left(\frac{W}{L}\right)_{\bar{B}}} + \frac{1}{\left(\frac{W}{L}\right)_{\bar{C}}}}$$

$$= 1 + \frac{1}{1+1} + \frac{1}{1+1+1} = 1 + \frac{1}{2} + \frac{1}{3} = \frac{6+3+2}{6} = \frac{11}{6}$$

$$\left(\frac{W}{L}\right)_{p,eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_{\bar{F}}} + \frac{1}{\left(\frac{W}{L}\right)_{\bar{E}} + \left(\frac{W}{L}\right)_{\bar{D}}} + \frac{1}{\left(\frac{W}{L}\right)_{\bar{A}} + \left(\frac{W}{L}\right)_{\bar{B}} + \left(\frac{W}{L}\right)_{\bar{C}}}}$$

$$= \frac{1}{1 + \frac{1}{2} + \frac{1}{3}} = \frac{1}{\frac{11}{6}} = \frac{6}{11}$$

$$V_{th} = \frac{V_{T0,n} + \sqrt{\frac{k_{p,eq}}{k_{n,eq}}}\left(V_{DD} + V_{T0,p}\right)}{1 + \sqrt{\frac{k_{p,eq}}{k_{n,eq}}}}$$

$$= \frac{1 + \sqrt{\frac{6/11}{11/6}}\,(5-1)}{1 + \sqrt{\frac{6/11}{11/6}}} = \frac{1 + 4\sqrt{\frac{6^2}{11^2}}}{1 + \sqrt{\frac{6^2}{11^2}}} = \boxed{2.0588\ V}$$

(c) In order to have largest rise, fall time, largest load capacitance is needed.

For T_{rise}, $\bar{B}$, $\bar{D}$, $\bar{F}$ path will have the largest load capacitance.
so the path will have longest rise time

For T_{fall}, $\bar{A}$, $\bar{B}$, $\bar{C}$ path will have the largest load capacitance.
so the path will have longest fall time.

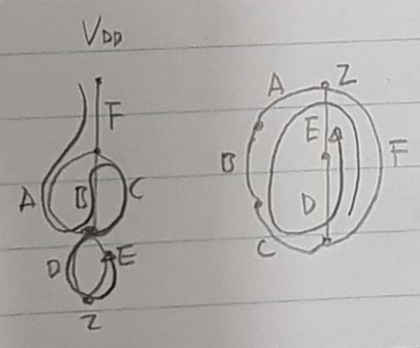
(d) $$T_{rise} = \frac{C_{load}}{K_{P,eff}(V_{DD} - |V_{Top}|)}\left[\frac{2(|V_{Top}| - 0.1V_{DD})}{V_{DD} - |V_{Top}|} + \ln\left(\frac{2(V_{DD} - |V_{Top}|)}{0.1V_{DD}} - 1\right)\right]$$

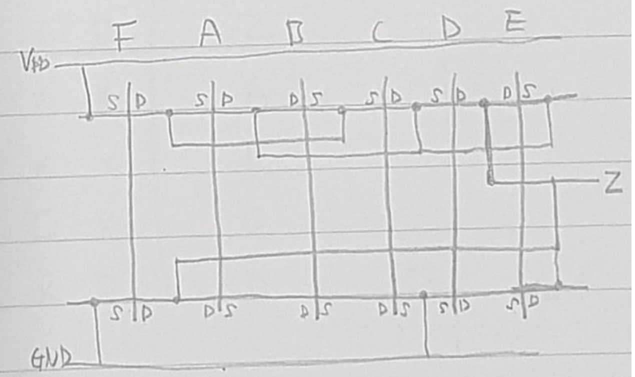
$$= \frac{100\times10^{-15}}{100\times10^{-6}\times\frac{6}{11}\times4}\left[\frac{2(1-0.5)}{(5-1)} + \ln\left(\frac{2(5-1)}{0.5} - 1\right)\right]$$

$$= \frac{11}{24}\times10^{-9}\times\left(\frac{1}{4} + \ln(15)\right) = 1.355\times10^{-9}$$

$$\boxed{= 1.355\ ns}$$

(e)





$\boxed{\text{Euler Path} = F \to A \to B \to C \to D \to E}$

Problem P3. (80 pts)

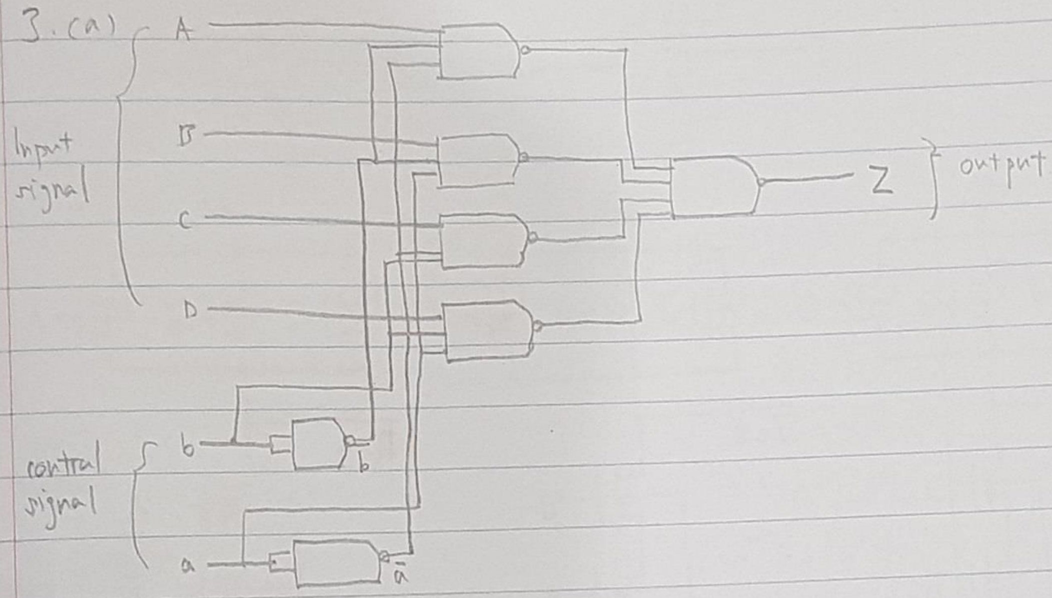
You need to design a 4-to-1 multiplexer.

(a) Draw a logic gate design of your 4-to-1 multiplexer design. Specify all logic gates, input signals, control signals and output signal connections in your gate level design. (20pts)

(b) Define Truth Table and Logic Equation of your 4-to-1 multiplexer design using input signals, control signals and output signal. (20pts)

(c) Draw your detailed pMOS and nMOS transistor level design. You need to show how you would connect all pMOS and nMOS transistors' drains, sources, gates and bulks inside your detailed design. Show the multiplexer's input signals, control signals and output signal connected in your transistor level design. You should use your logic gate design from the part (a) to design your transistor level design. (40pts)

3. (a)

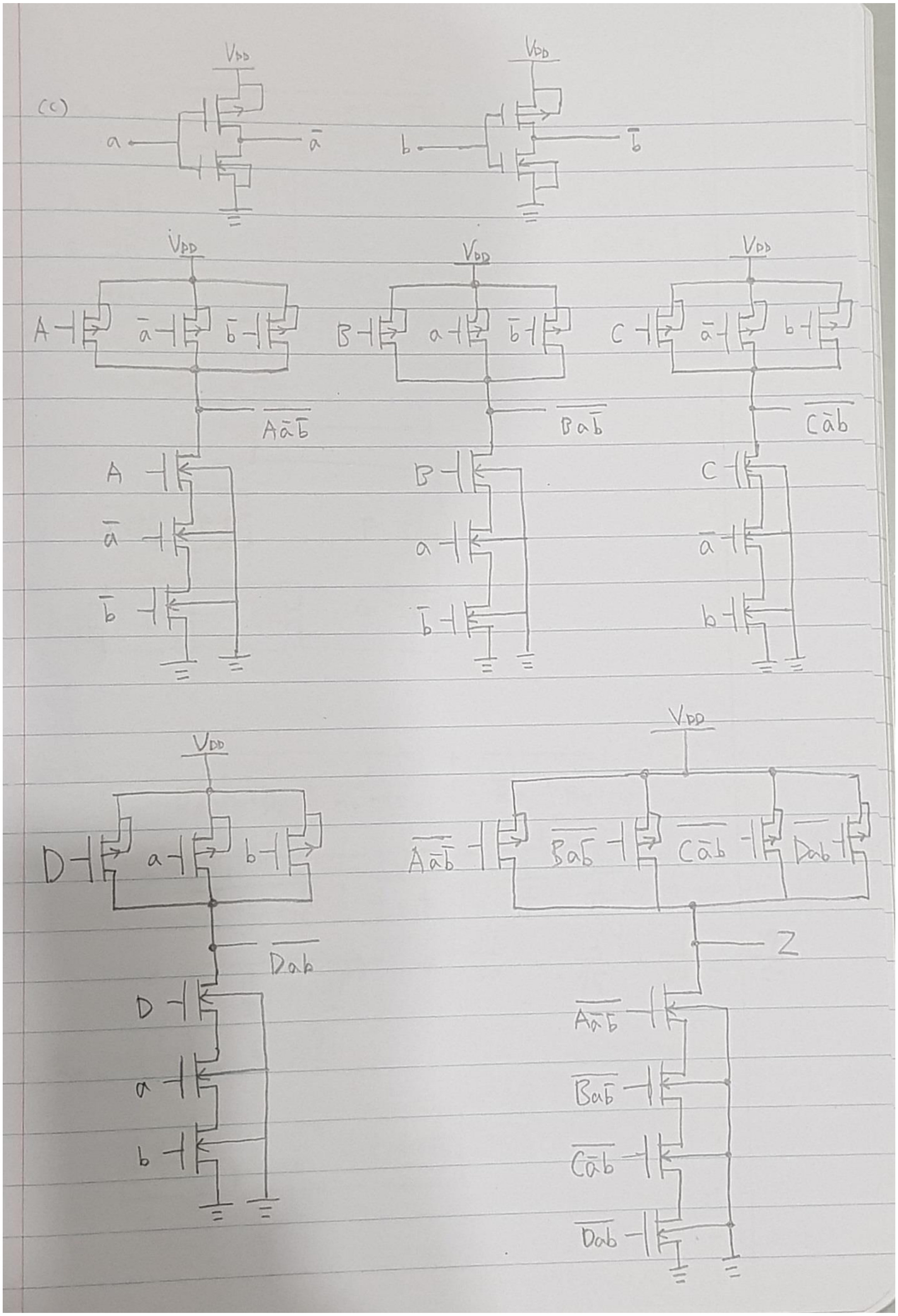


(b) $Q = \overline{(\overline{A\bar{a}\bar{b}})(\overline{Ba\bar{b}})(\overline{C\bar{a}b})(\overline{Dab})}$

$= \overline{(\bar{A}+a+b)(\bar{B}+\bar{a}+b)(\bar{C}+a+\bar{b})(\bar{D}+\bar{a}+\bar{b})}$

$= \bar{a}\bar{b}A + a\bar{b}B + \bar{a}bC + abD$

control signals		data signals				Output
a	b	A	B	C	D	Z
0	0	A	x	x	x	A
1	0	x	B	x	x	B
0	1	x	x	C	x	C
1	1	x	x	x	D	D


(c)
VDD
a
$\bar{a}$
b
$\bar{b}$
A
B
C
D
$\overline{A\bar{a}\bar{b}}$
$\overline{Ba\bar{b}}$
$\overline{C\bar{a}b}$
$\overline{Dab}$
Z

Problem P4. (70 pts)

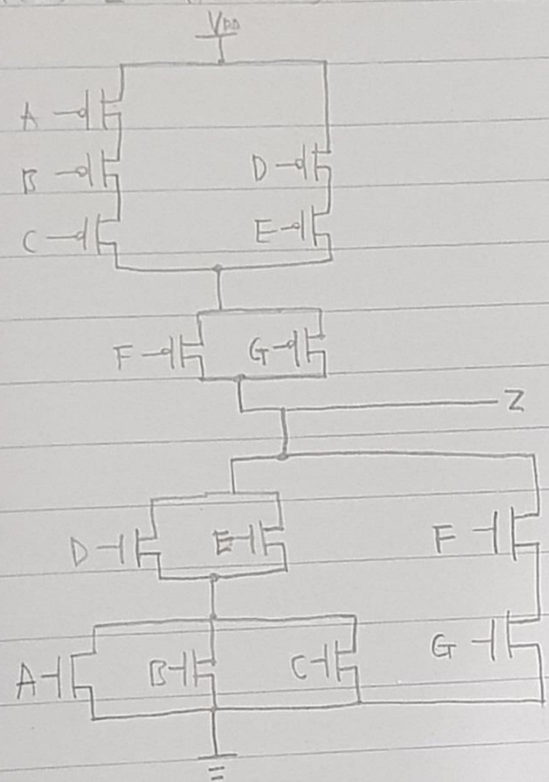
Consider the following function: $Z = \overline{(A + B + C)(D + E) + FG}$.

(a) Draw the pMOS and nMOS CMOS transistors schematic of the function Z. Assume that all signals and their respective inverse signals are available for the design. (10 pts)

(b) If $(W/L)_p = 15$ determine $(W/L)_{p.eq}$ for the design. (30 pts)

(c) If $(W/L)_n = 10$ determine $(W/L)_{n.eq}$ for the design. (30 pts)

4(a) $Z = \overline{(A+B+C)(D+E) + FG}$



(b) $$R_{eq,p} = \frac{1}{\frac{1}{R_A+R_B+R_C} + \frac{1}{R_D+R_E}} + \frac{1}{\frac{1}{R_F} + \frac{1}{R_G}}$$

$$= \frac{1}{\frac{1}{\frac{1}{15}+\frac{1}{15}+\frac{1}{15}} + \frac{1}{\frac{1}{15}+\frac{1}{15}}} + \frac{1}{\frac{1}{\frac{1}{15}} + \frac{1}{\frac{1}{15}}} =$$

$$= \frac{1}{\frac{15}{3} + \frac{15}{2}} + \frac{1}{30} = \frac{6}{75} + \frac{1}{30} = \frac{17}{150}$$

$$R_{eq,p} = \left(\frac{L}{W}\right)_{p,eq} = \frac{17}{150}$$

$$\boxed{\left(\frac{W}{L}\right)_{p,eq} = \frac{150}{17} = 8.8235}$$

(c) $$\frac{1}{R_{eq,n}} = \frac{1}{\frac{1}{\frac{1}{R_A}+\frac{1}{R_B}+\frac{1}{R_C}} + \frac{1}{\frac{1}{R_D}+\frac{1}{R_E}}} + \frac{1}{R_F + R_G}$$

$$= \frac{1}{\frac{1}{10+10+10} + \frac{1}{10+10}} + \frac{1}{\frac{1}{10}+\frac{1}{10}}$$

$$= \frac{1}{\frac{1}{30}+\frac{1}{20}} + \frac{10}{2}$$

$$= 12 + 5 = 17$$

$$\frac{1}{R_{eq,n}} = \boxed{\left(\frac{W}{L}\right)_{n,eq} = 17}$$