Washington University in St. Louis

McKelvey School of Engineering

Spring Semester 2023

CSE463M: Digital Integrated Circuit Design and Architecture

Final Assign #4 – Final Report

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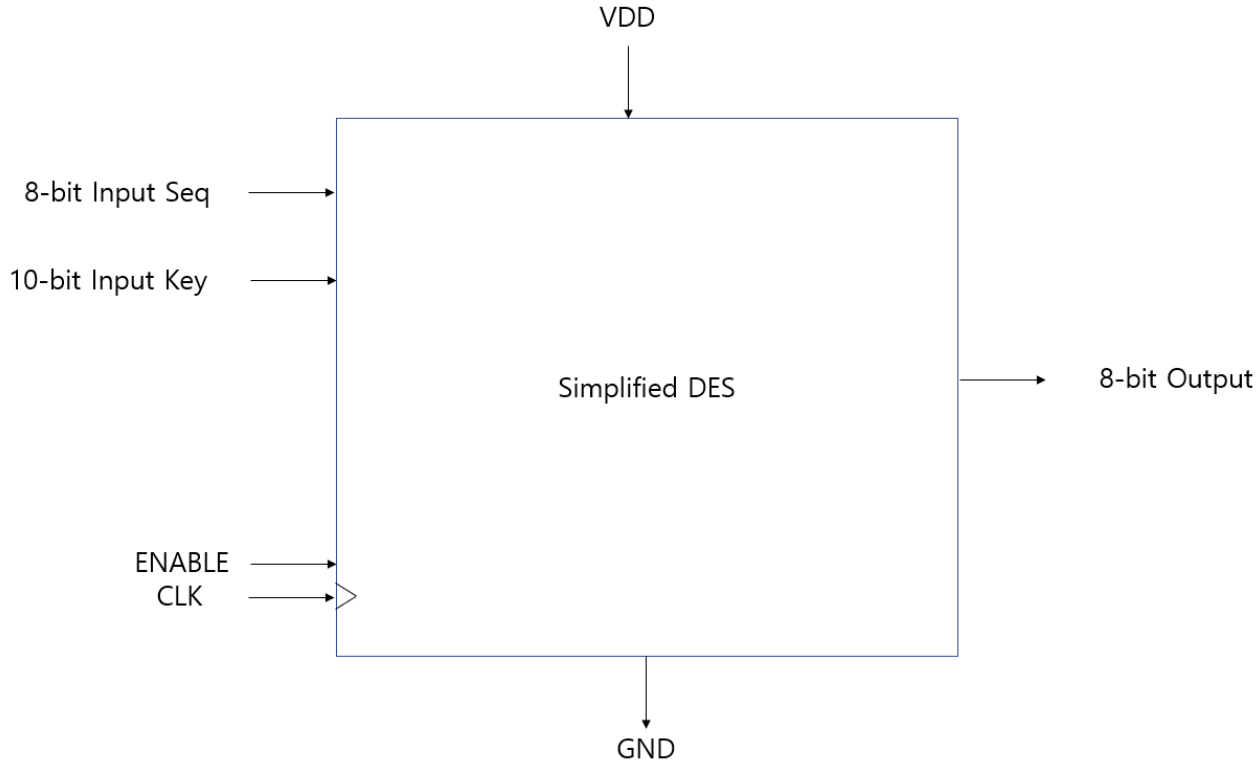
Byeongchan Gwak

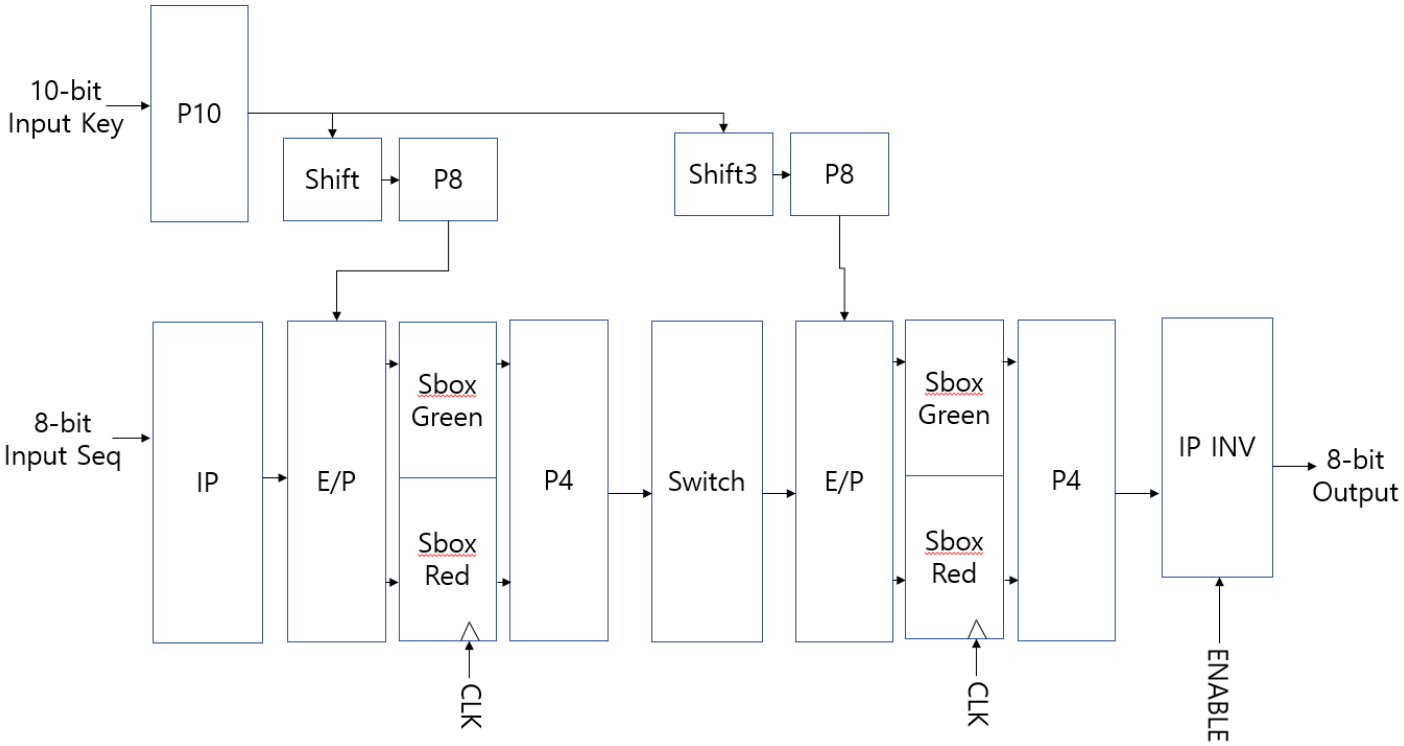
Table of Contents

1. Objective of this project

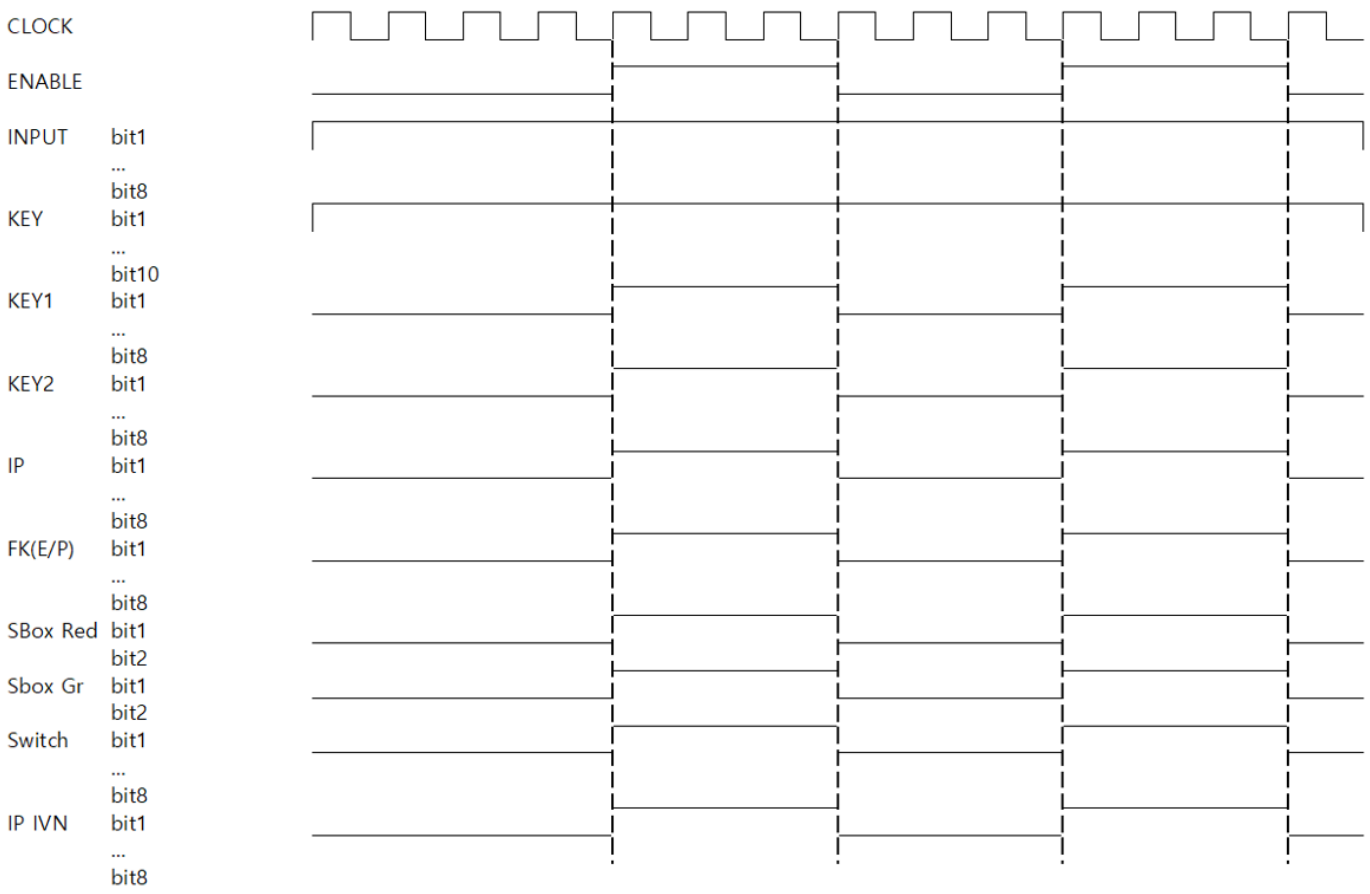
- My team will design a CMOS chip that will perform simplified DES in hardware on 8-bit Input = 11101100 using 10-bit Input key k = 1100010110.

2. Block diagram





3. Anticipated timing diagram



4. List of all parts used in this project

* There are many parts to complete the Simplified DES.
* Below is the list of all parts.

 # For basic operation
INVERTOR
NAND
XOR2
XOR4

 # For bit control
P10
P8
P4
SHIFT 1
SHIFT 3
EP
SWITCH
IP
IP Invert

 # For selection
2:1 mux
16:1 mux

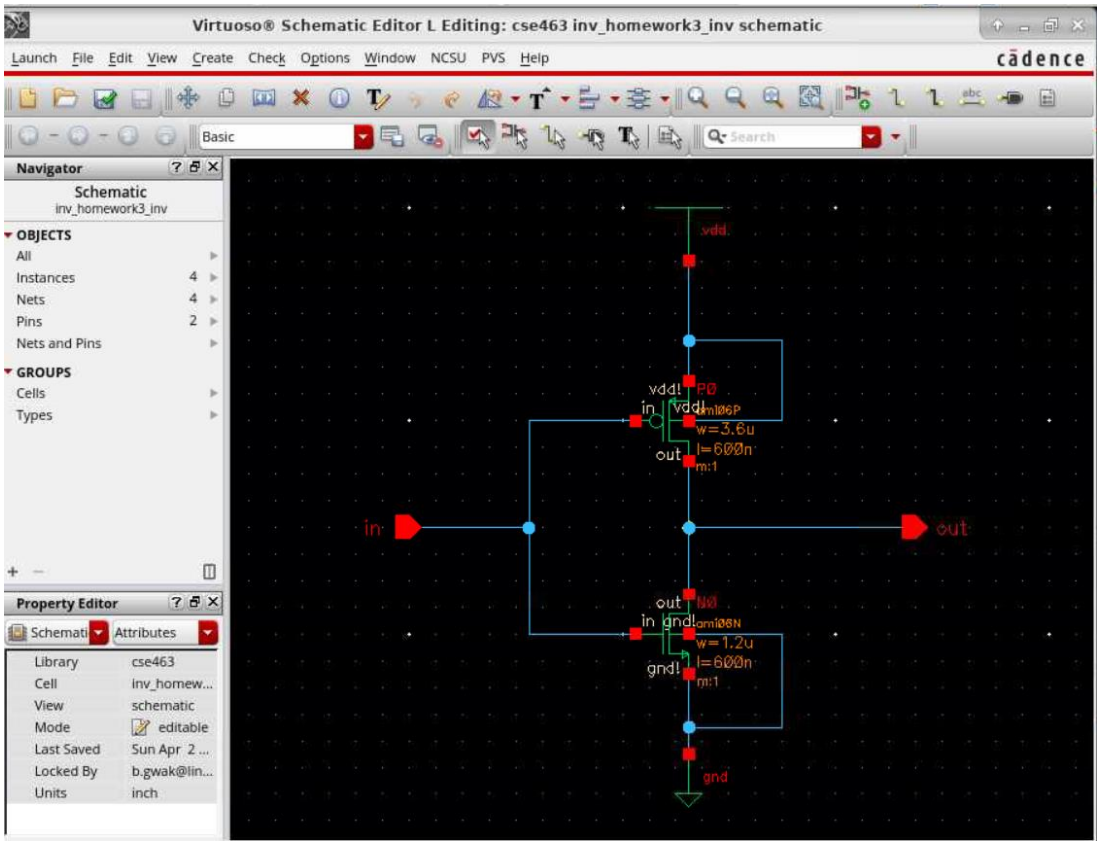
 # For Enable
ENABLE

 # For CLK
D-LATCH
D Flip flop

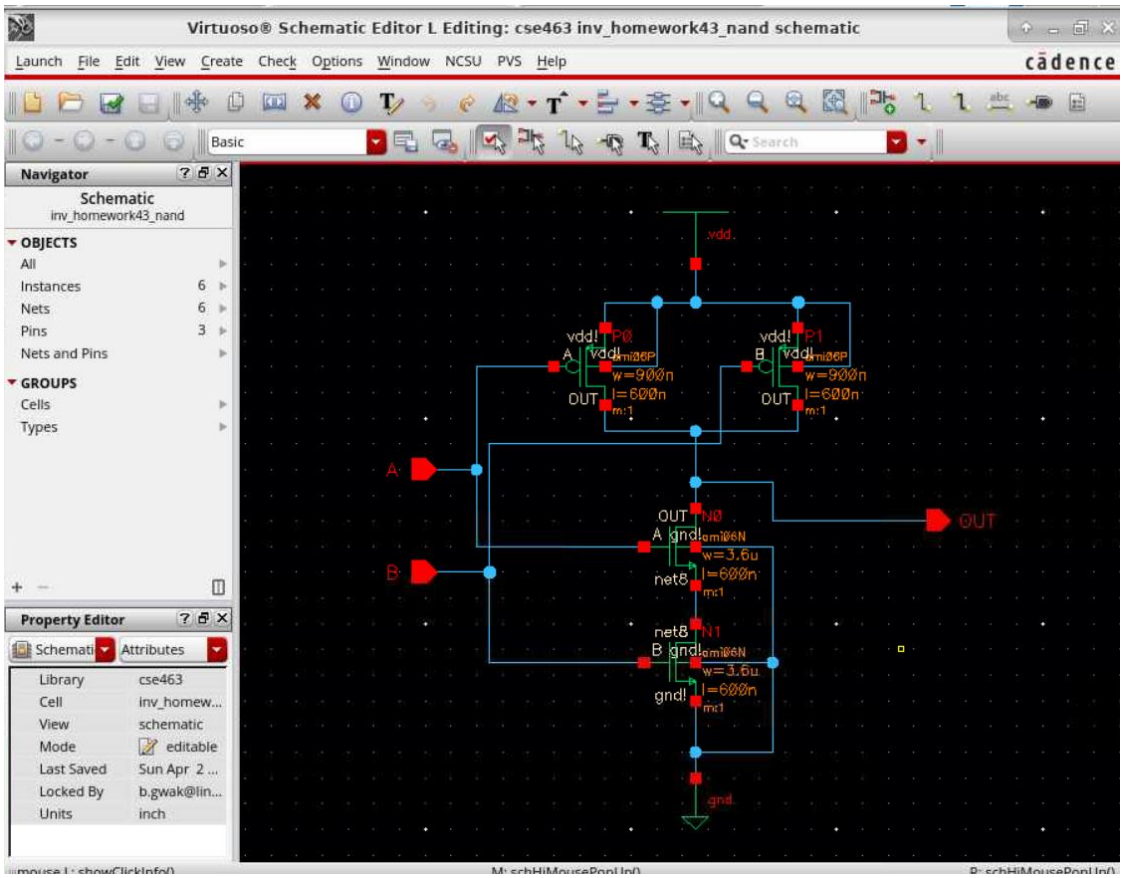
 # For SBox
SBox Red
SBox Green

5. Schematic

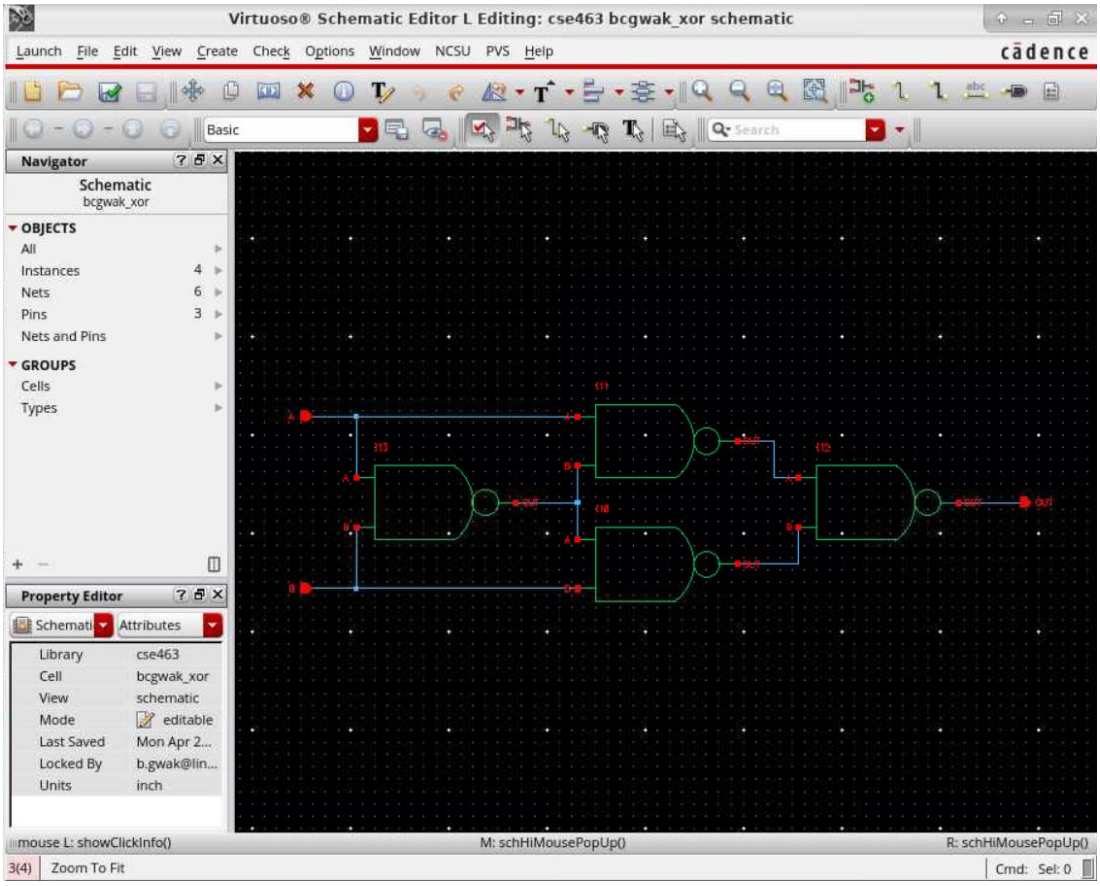
* INVERTOR



* NAND



* XOR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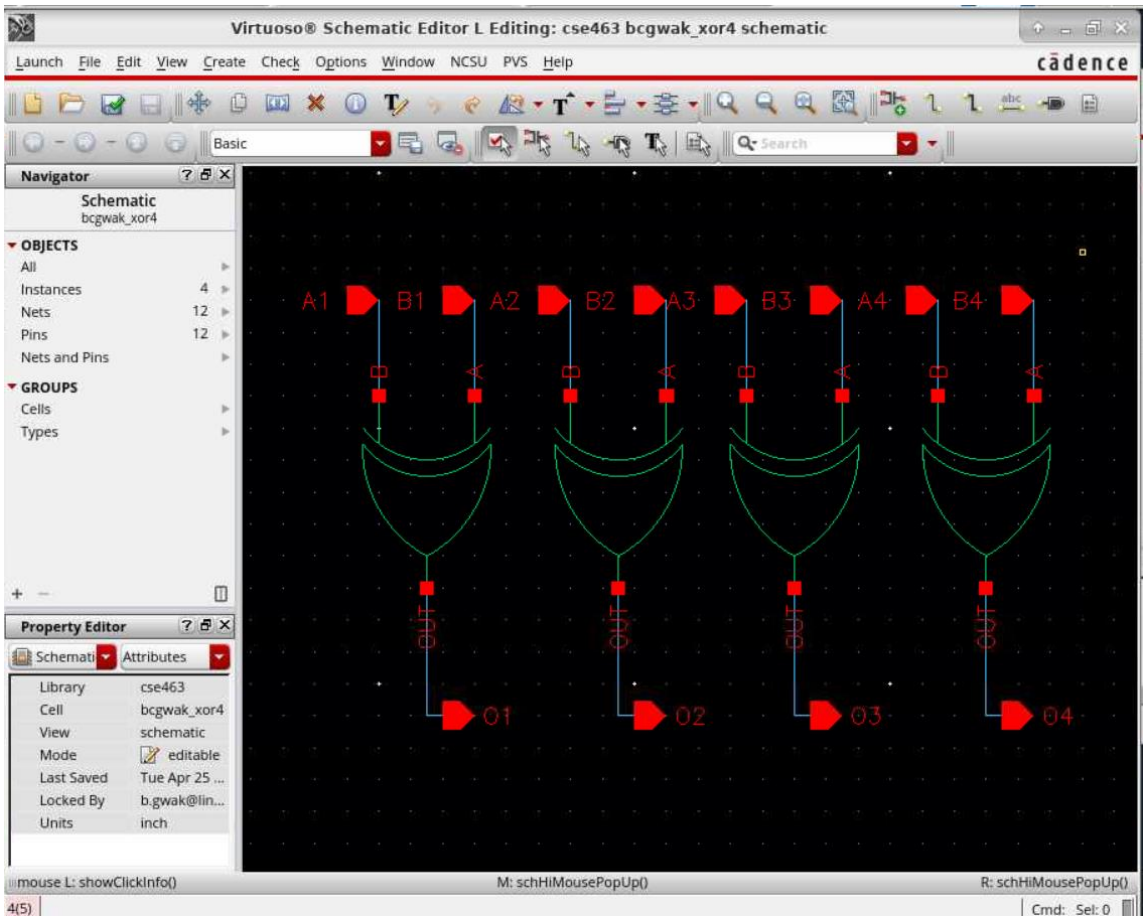
cadence
Basic
Navigator
Schematic
bcgwak_xor
OBJECTS
All
Instances 4
Nets 6
Pins 3
Nets and Pins
GROUPS
Cells
Types
Property Editor
Schemati
Attributes
Library cse463
Cell bcgwak_xor
View schematic
Mode editable
Last Saved Mon Apr 2...
Locked By b.gwak@lin...
Units inch
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()
3(4)
Zoom To Fit
Cmd: Sel: 0

* XOR4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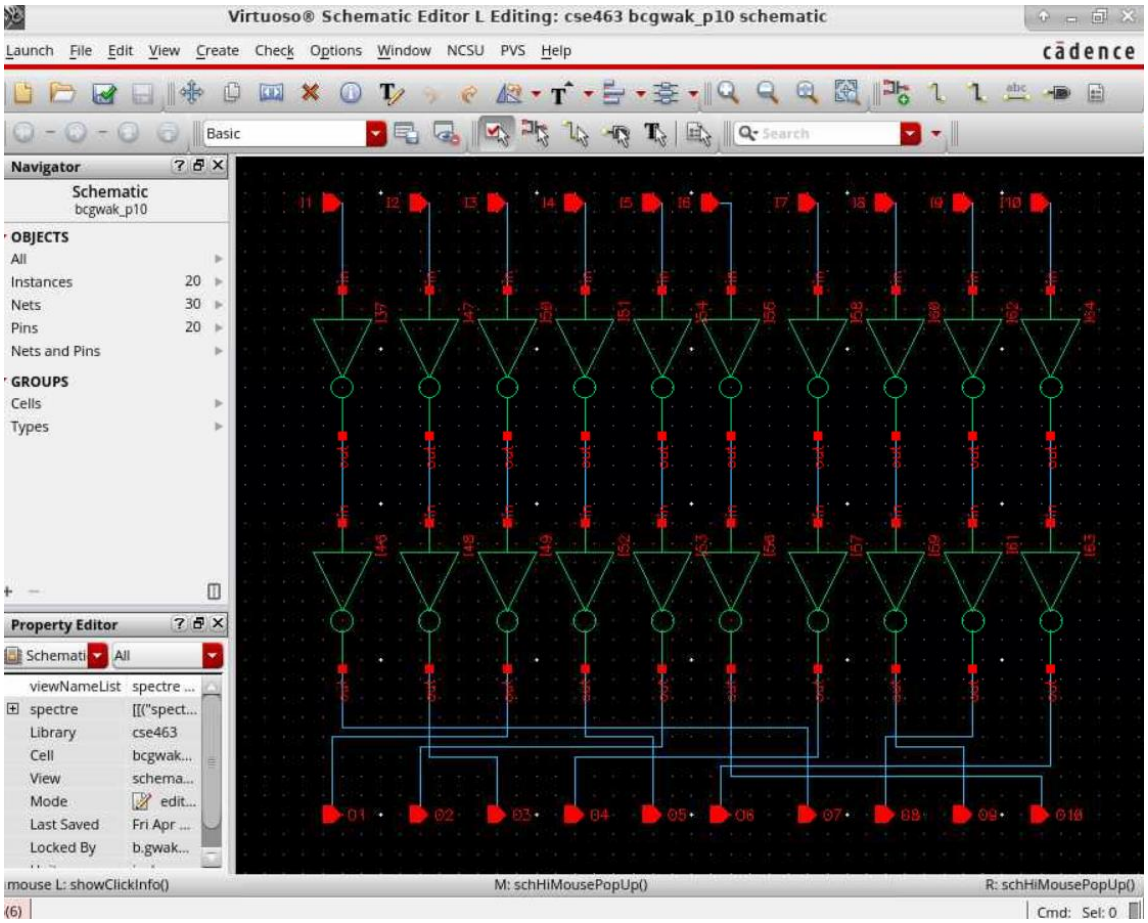
Basic
Navigator
Schematic
bcgwak_xor4
OBJECTS
All
Instances 4
Nets 12
Pins 12
Nets and Pins
GROUPS
Cells
Types
Property Editor
Schemati
Attributes
Library cse463
Cell bcgwak_xor4
View schematic
Mode editable
Last Saved Tue Apr 25 ...
Locked By b.gwak@lin...
Units inch
A1
B1
A2
B2
A3
B3
A4
B4
OUT
O1
O2
O3
O4
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()
4(5)
Cmd: Sel: 0

* P10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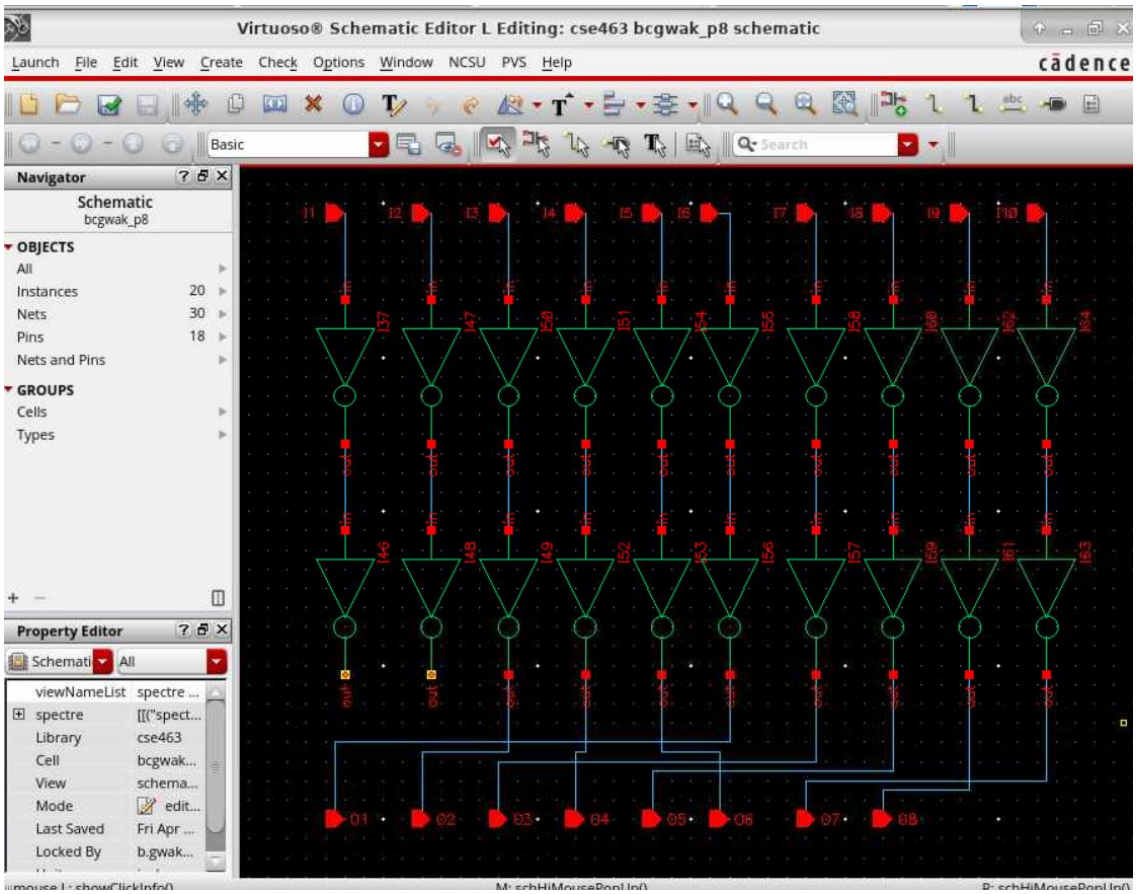
Launch File Edit View Create Check Options Window NCSU PVS Help
cadence
Basic
Navigator
Schematic
bcgwak_p10
OBJECTS
All
Instances 20
Nets 30
Pins 20
Nets and Pins
GROUPS
Cells
Types
Property Editor
Schemati All
viewNameList spectre ...
spectre [[("spect...
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()
(6)
Cmd: Sel: 0

* P8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Basic
Navigator
Schematic
bcgwak_p8
OBJECTS
All
Instances 20
Nets 30
Pins 18
Nets and Pins
GROUPS
Cells
Types
Property Editor
Schemati All
viewNameList spectre ...
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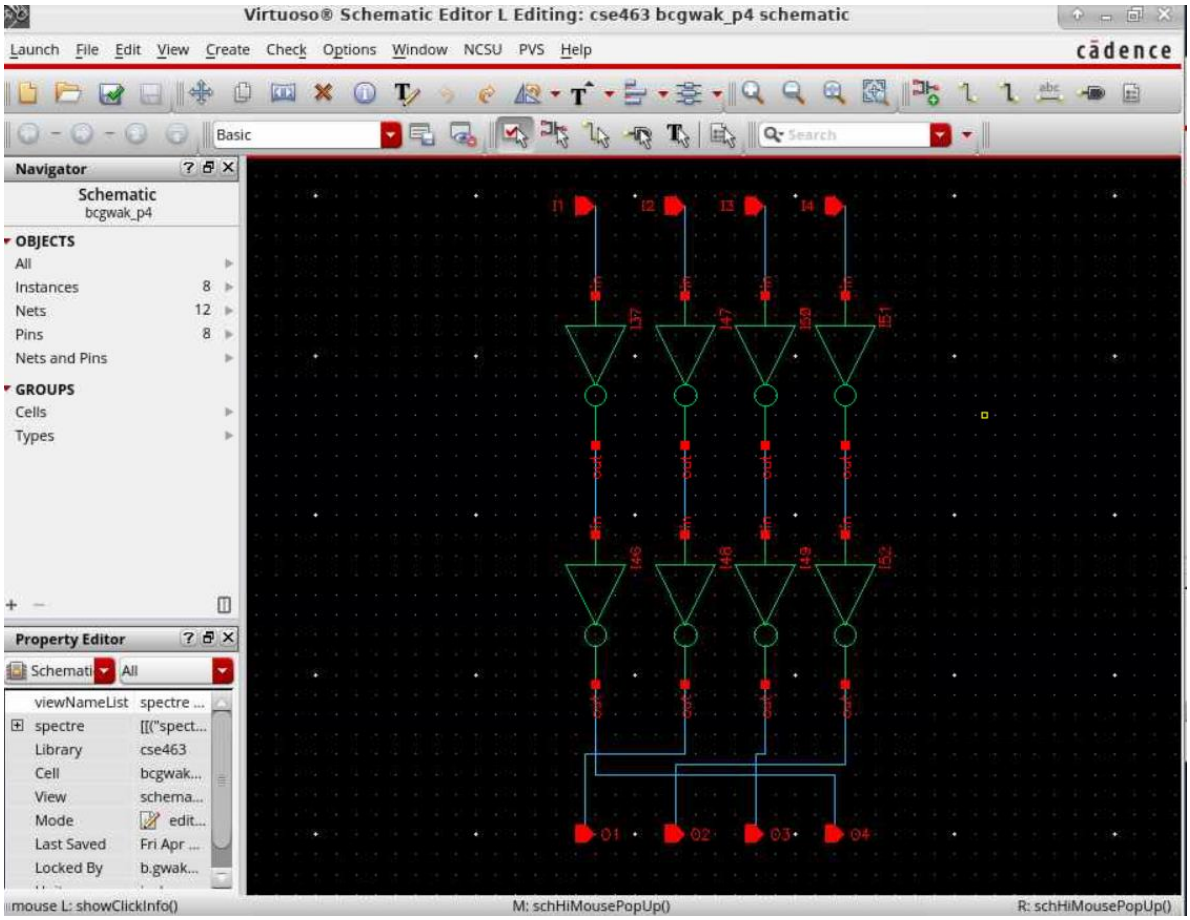
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...

* P4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Navigator
Schematic
bcgwak_p4
OBJECTS
All
Instances 8
Nets 12
Pins 8
Nets and Pins
GROUPS
Cells
Types
Property Editor
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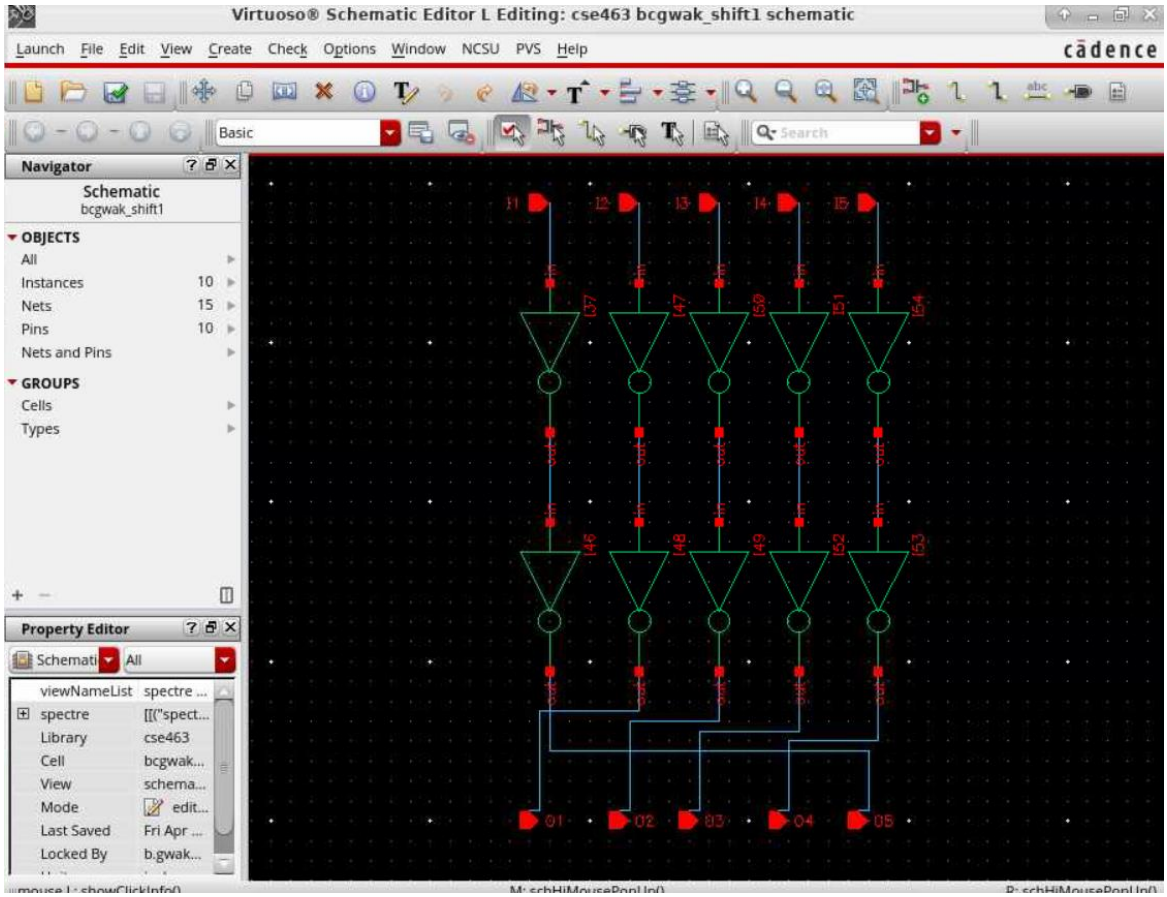
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...
I1
I2
I3
I4
I37
I47
I50
I51
I46
I48
I49
I52
O1
O2
O3
O4
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()

* SHIFT 1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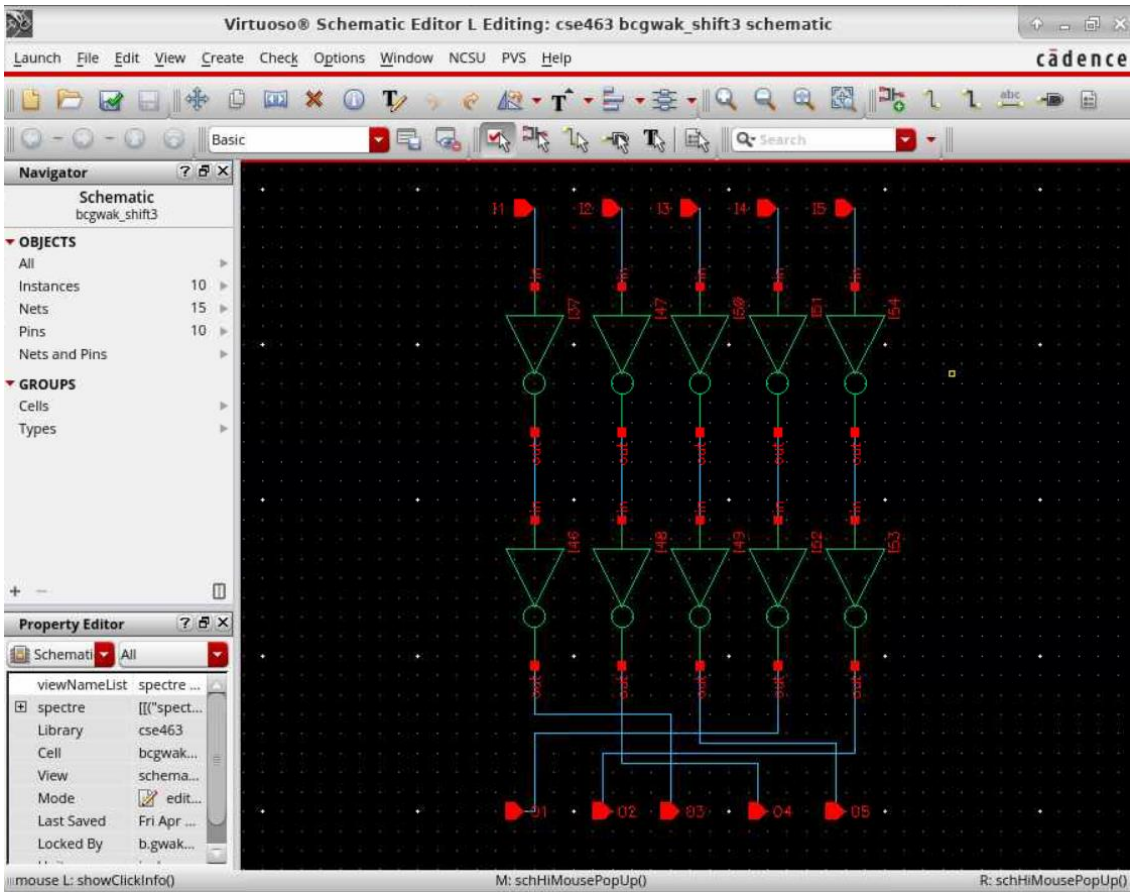
Navigator
Schematic
bcgwak_shift1
OBJECTS
All
Instances 10
Nets 15
Pins 10
Nets and Pins
GROUPS
Cells
Types
Property Editor
viewNameList spectre ...
spectre [[("spect...
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...
I1
I2
I3
I4
I5
I37
I47
I50
I51
I54
I46
I48
I49
I52
I53
O1
O2
O3
O4
O5

* SHIFT 3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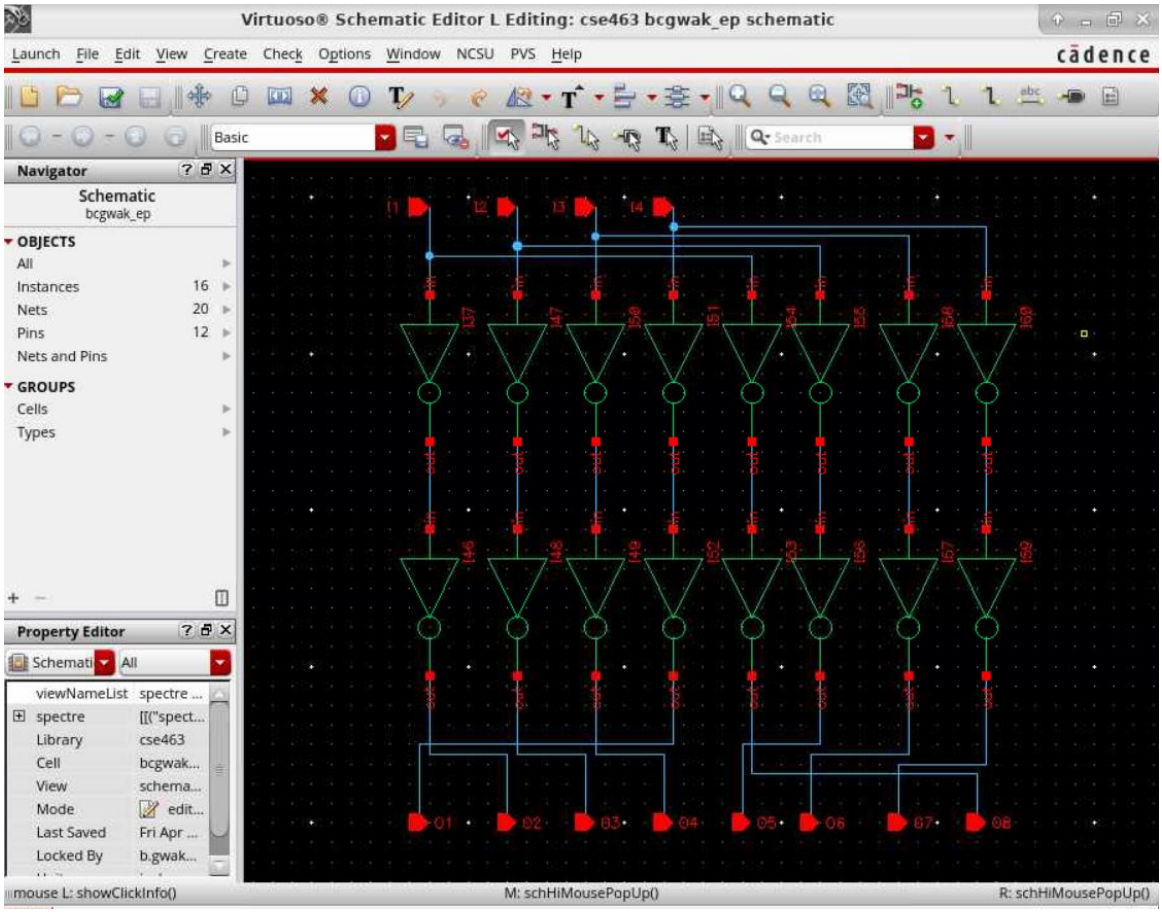
Navigator
Schematic
bcgwak_shift3
OBJECTS
All
Instances 10
Nets 15
Pins 10
Nets and Pins
GROUPS
Cells
Types
Property Editor
viewNameList spectre ...
spectre [("spect...
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()

* EP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Navigator
Schematic
bcgwak_ep
OBJECTS
All
Instances 16
Nets 20
Pins 12
Nets and Pins
GROUPS
Cells
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Cell bcgwak...
View schema...
Mode edit...
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Locked By b.gwak...
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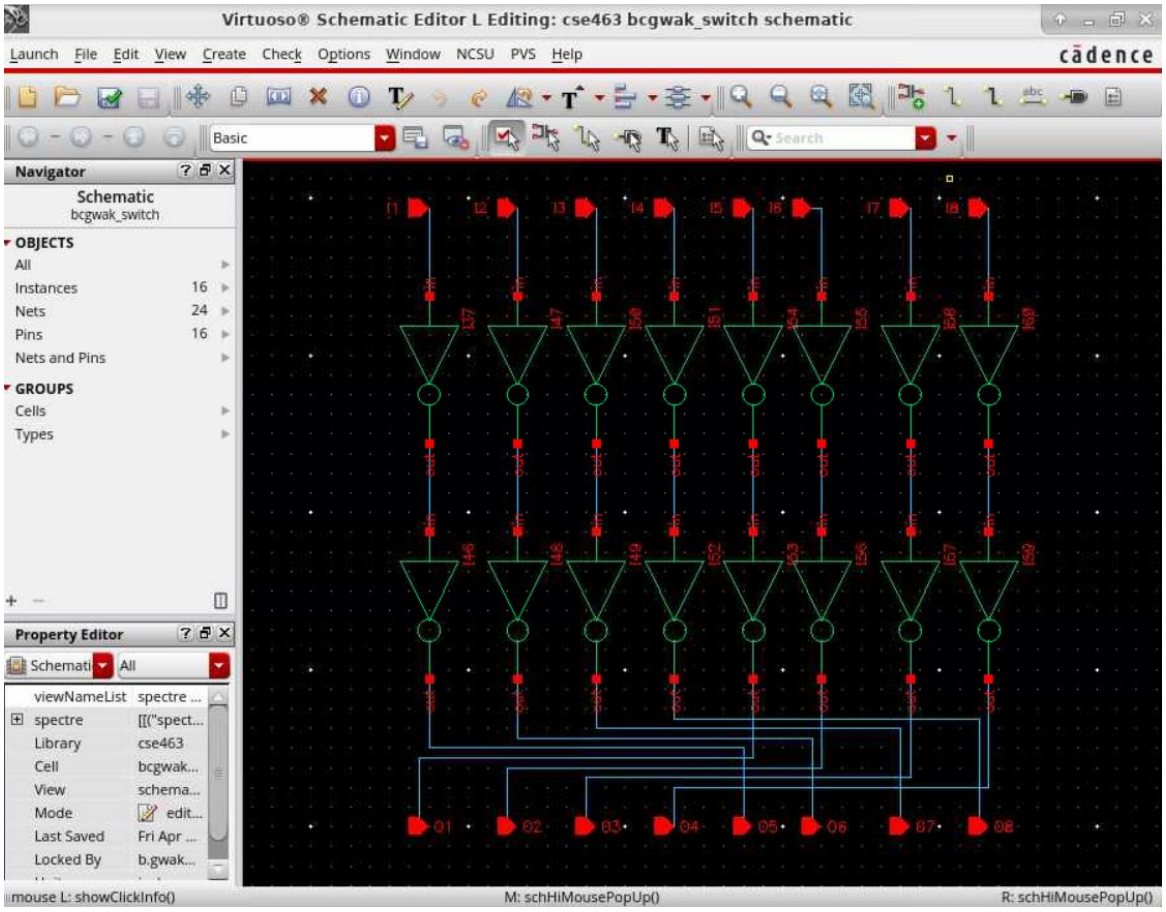
M: schHiMousePopUp()
R: schHiMousePopUp()

* SWITCH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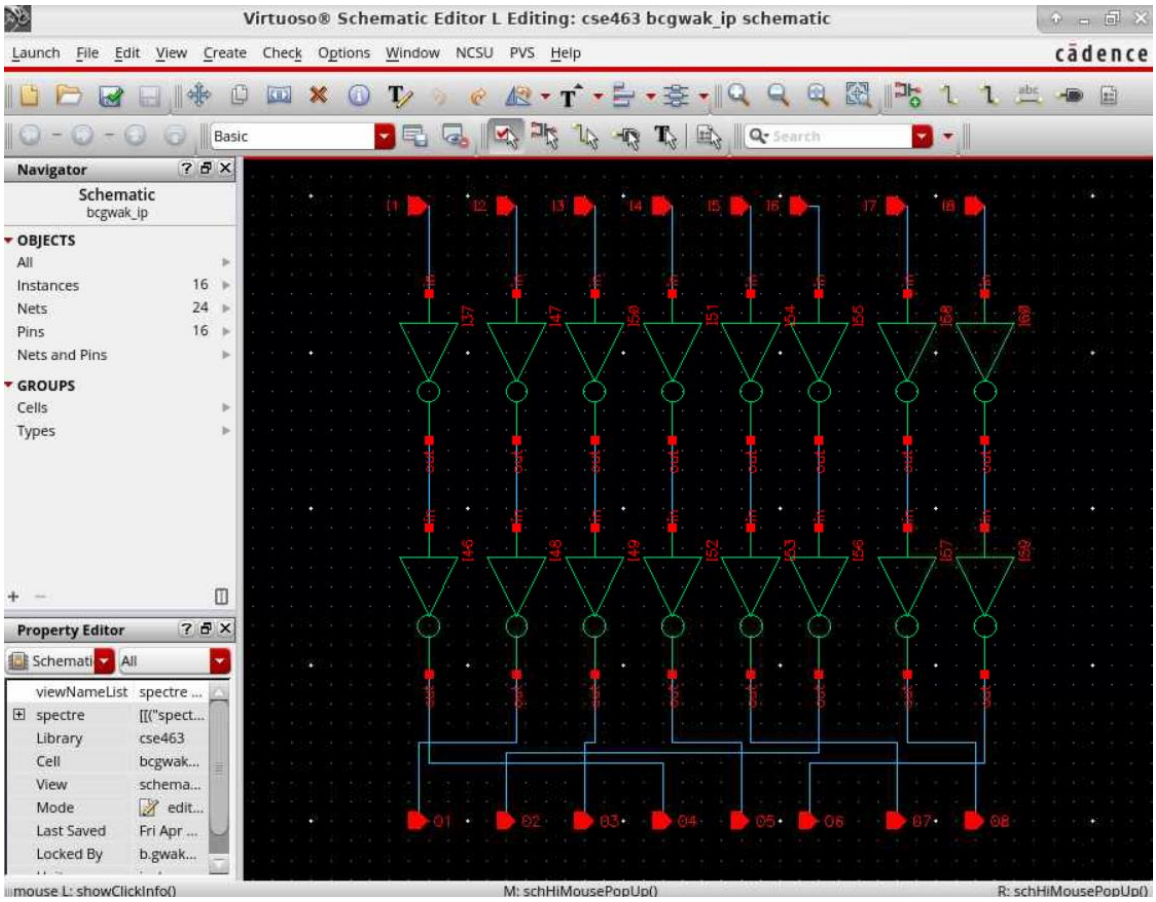
Basic
Search
Navigator
Schematic
bcgwak_switch
OBJECTS
All
Instances 16
Nets 24
Pins 16
Nets and Pins
GROUPS
Cells
Types
Property Editor
Schemati
All
viewNameList spectre ...
spectre [("spect...
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()

* IP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Basic
Search
Navigator
Schematic
bcgwak_ip
OBJECTS
All
Instances 16
Nets 24
Pins 16
Nets and Pins
GROUPS
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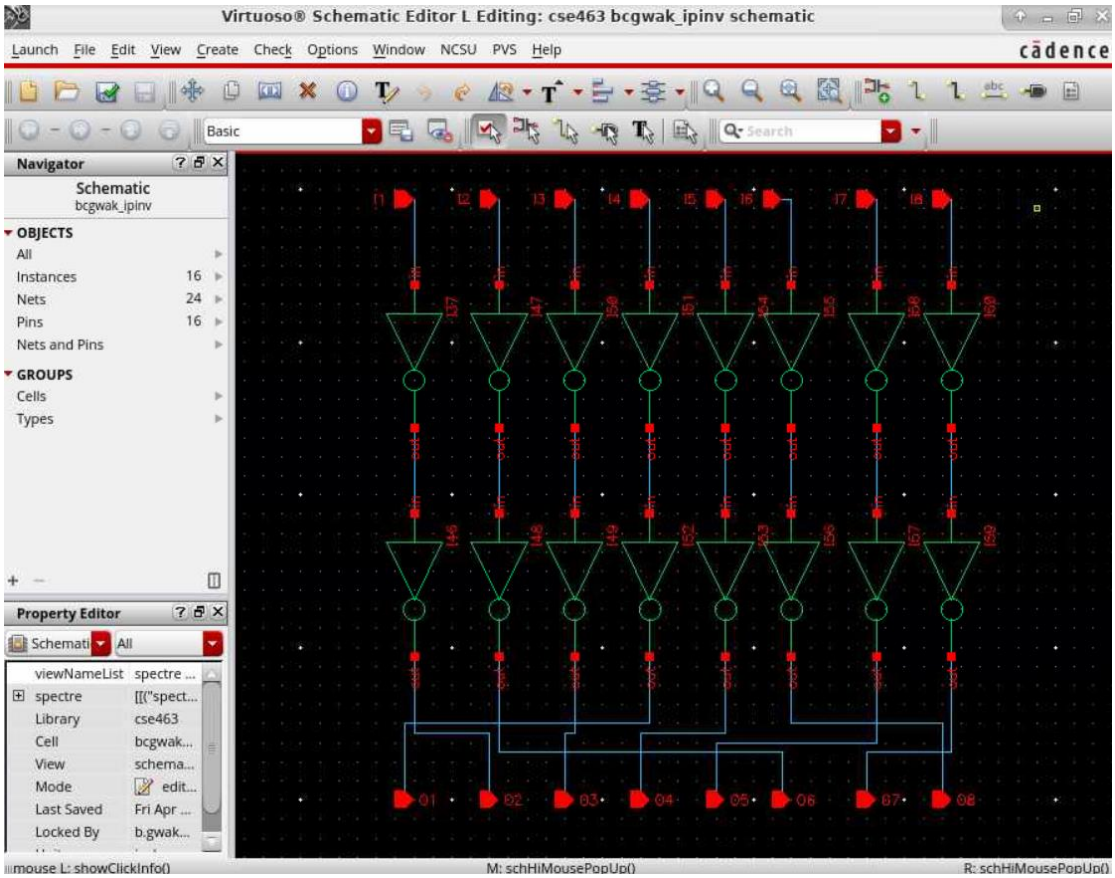
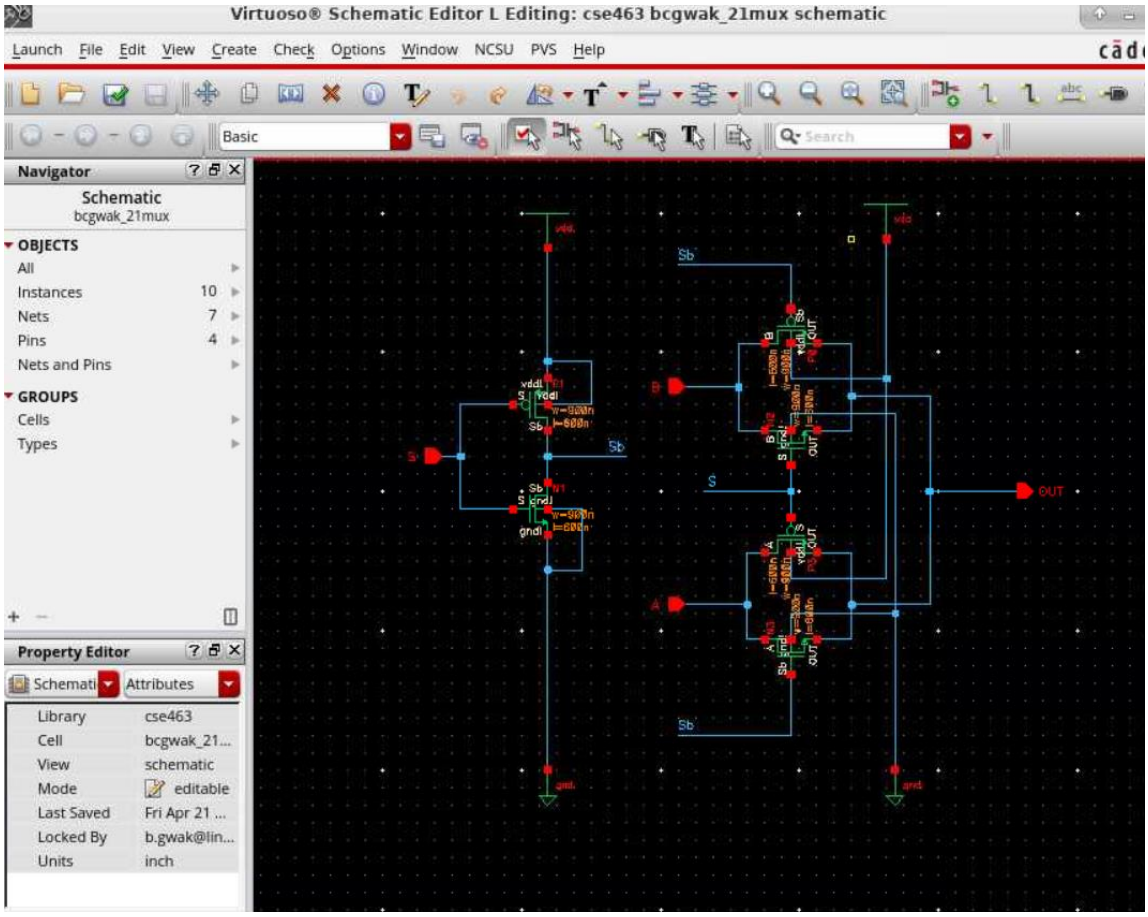
viewNameList spectre ...
spectre [("spect...
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()

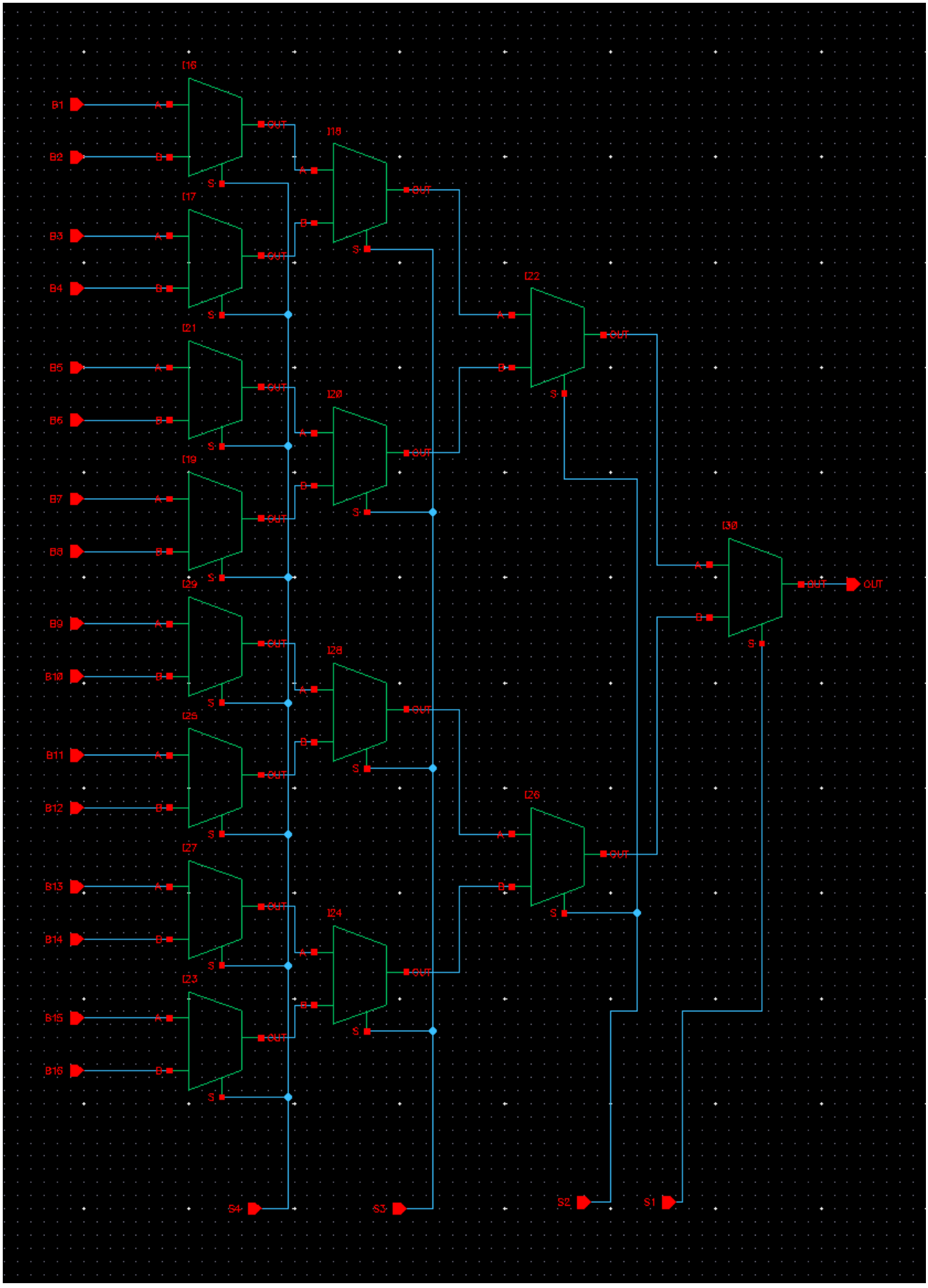
* IP Invert



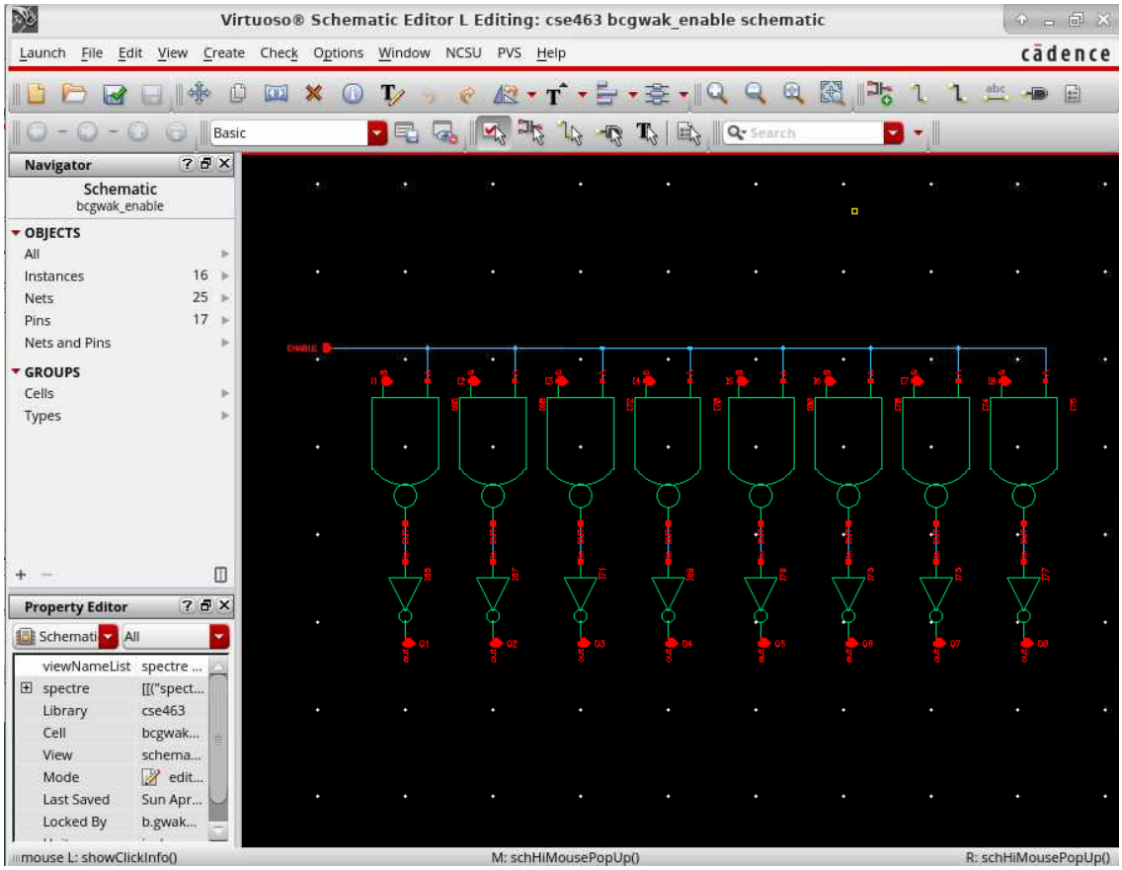
* 2:1 mux



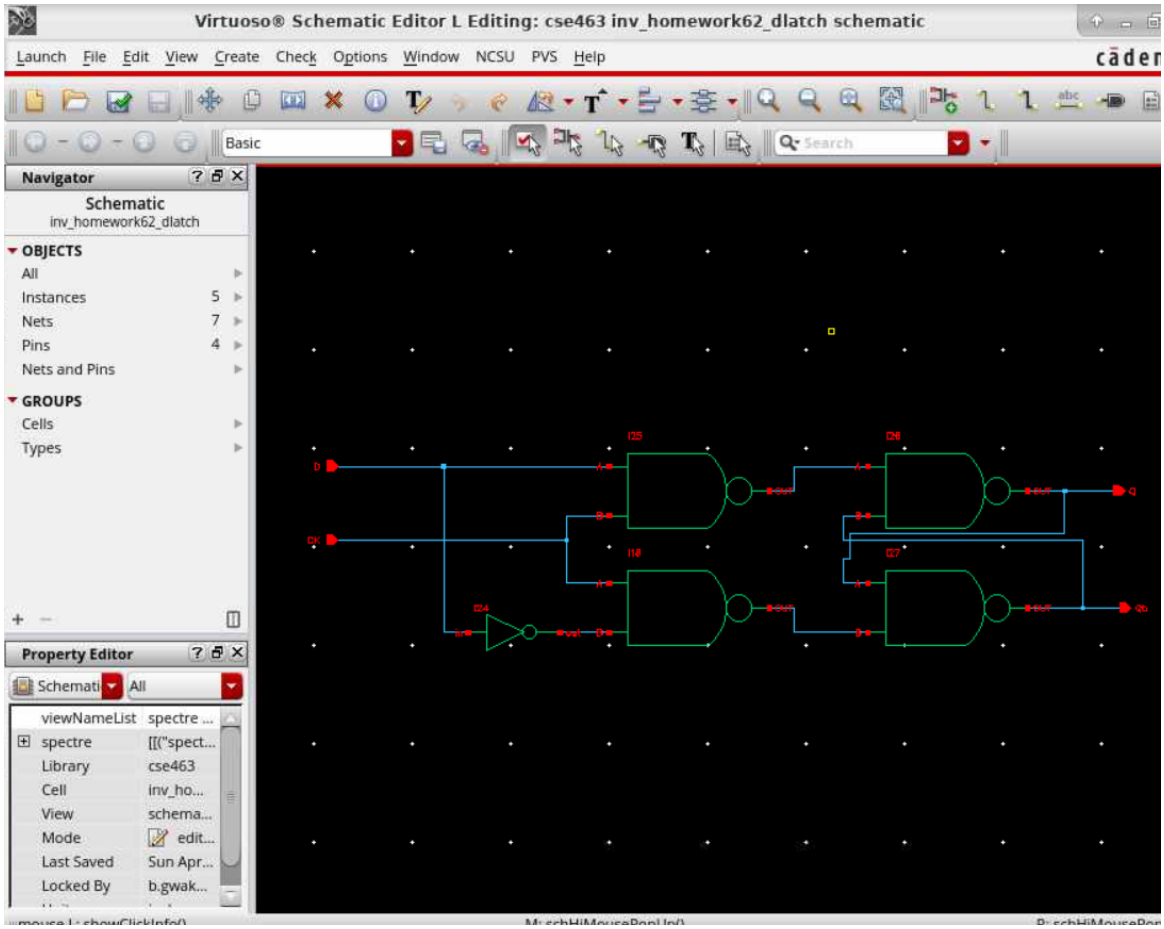
* 16:1 mux


I16
I18
I17
I22
I21
I20
I19
I30
I29
I28
I25
I26
I27
I24
I23
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
B13
B14
B15
B16
A
B
S
OUT
S4
S3
S2
S1

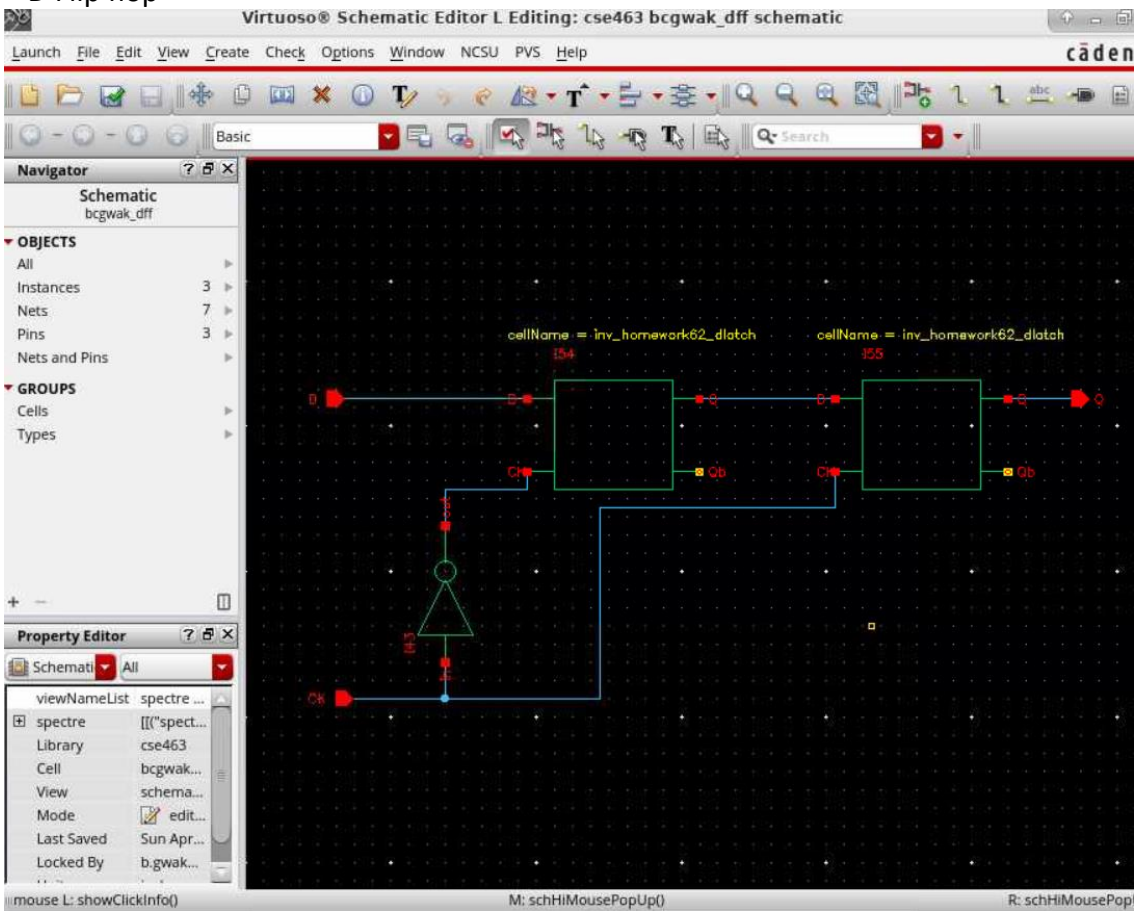
* ENABLE



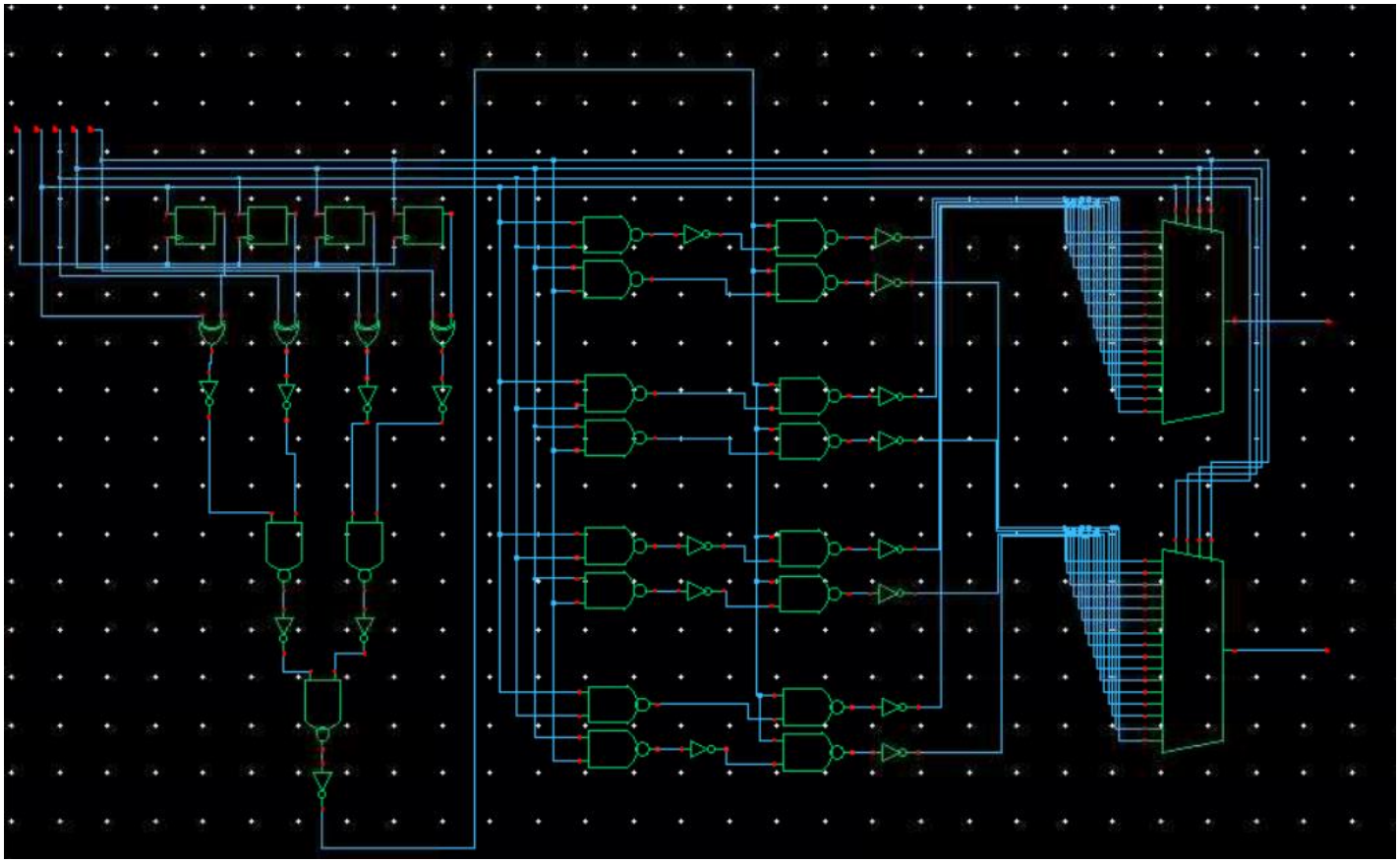
* D-LATCH



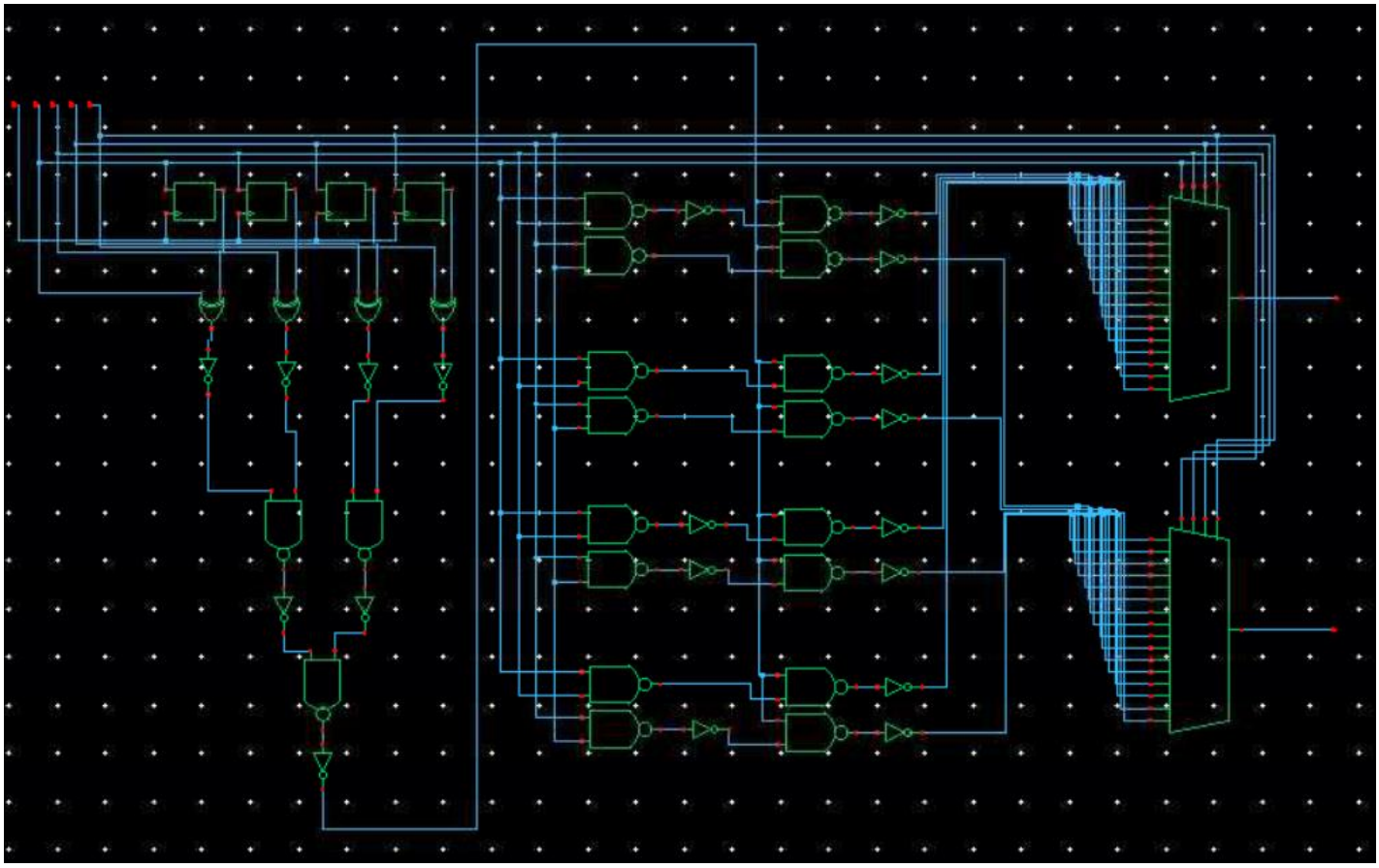
* D Flip flop



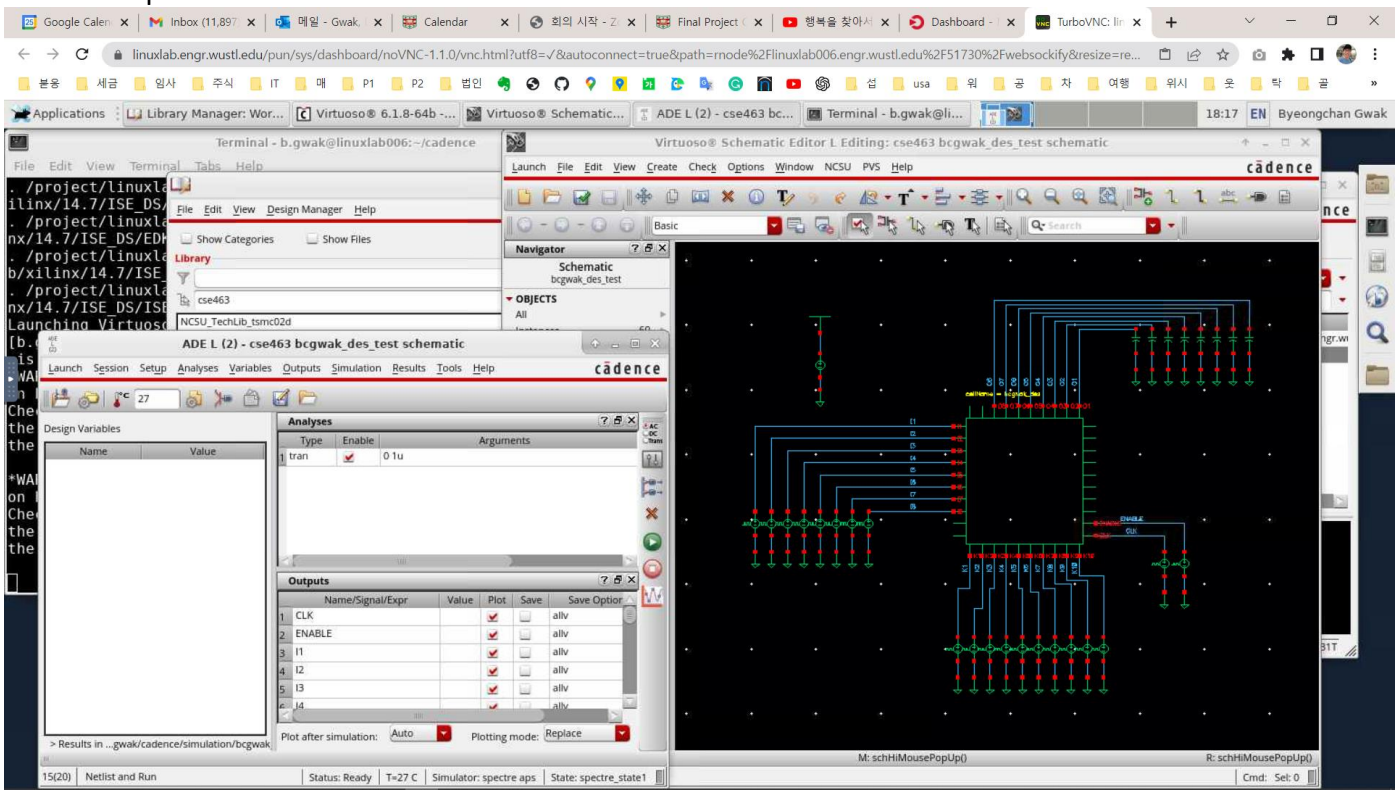
* SBox Red



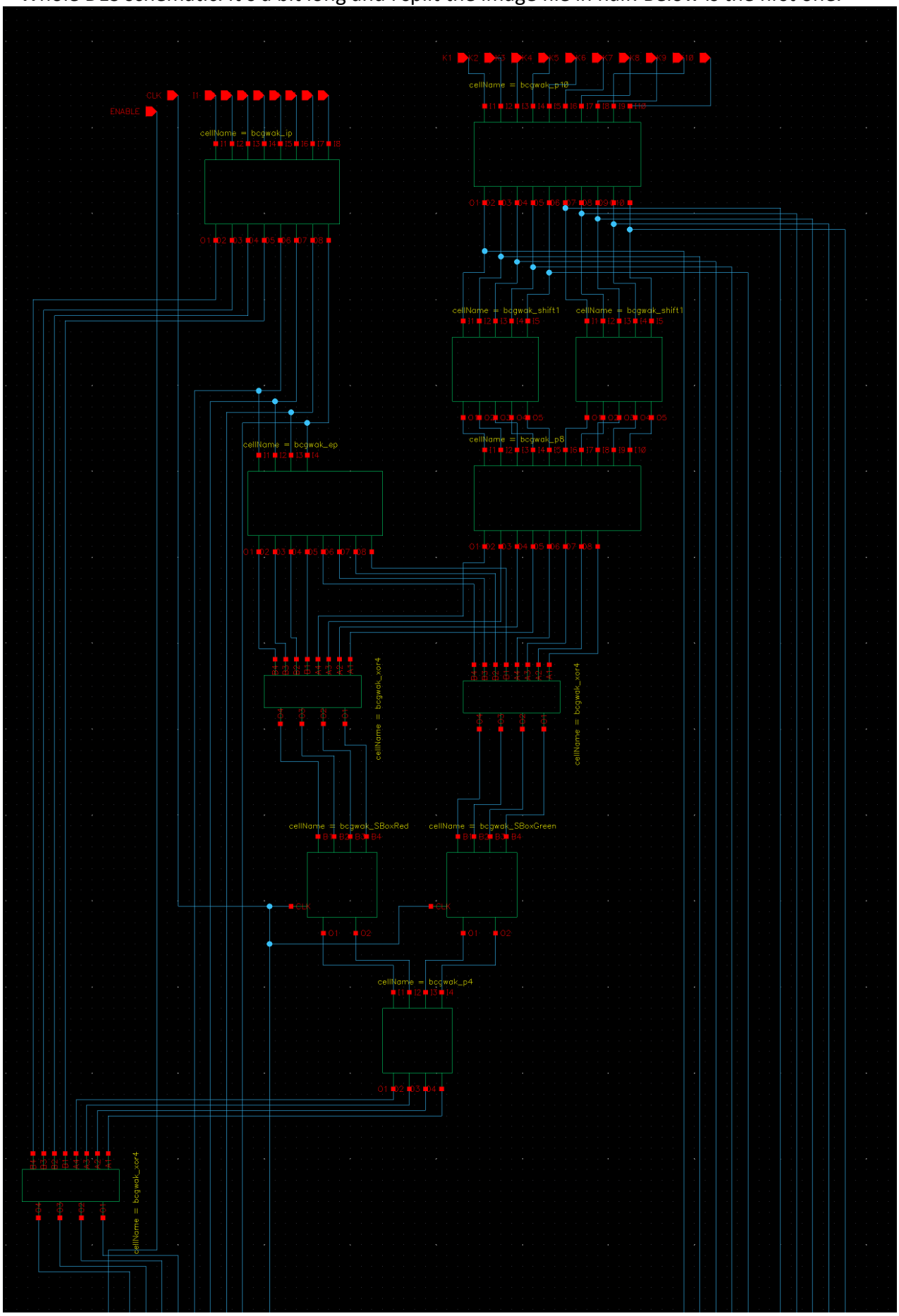
* SBox Green



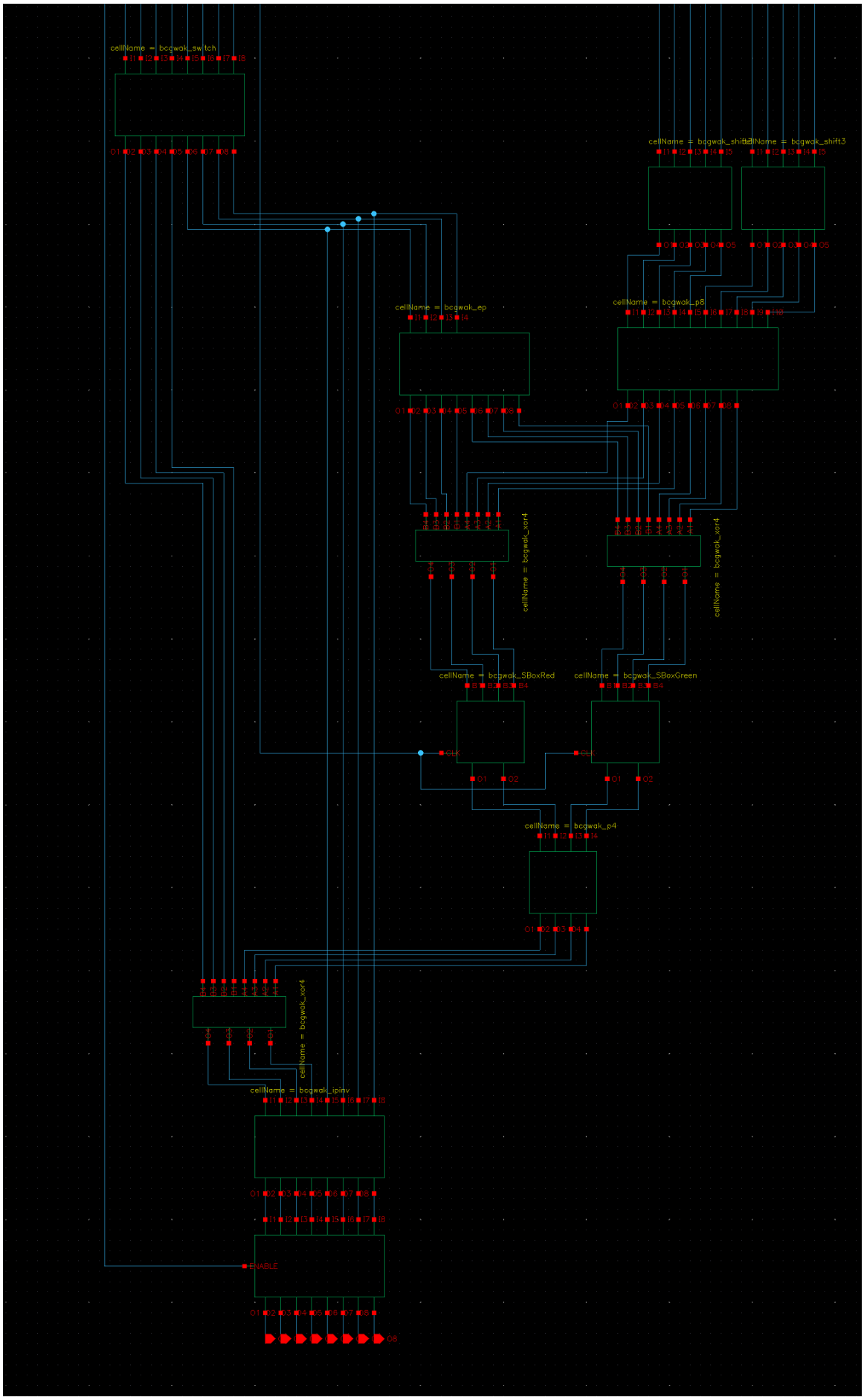
* Test setup for the DES.



* Whole DES schematic. It’s a bit long and I split the image file in half. Below is the first one.

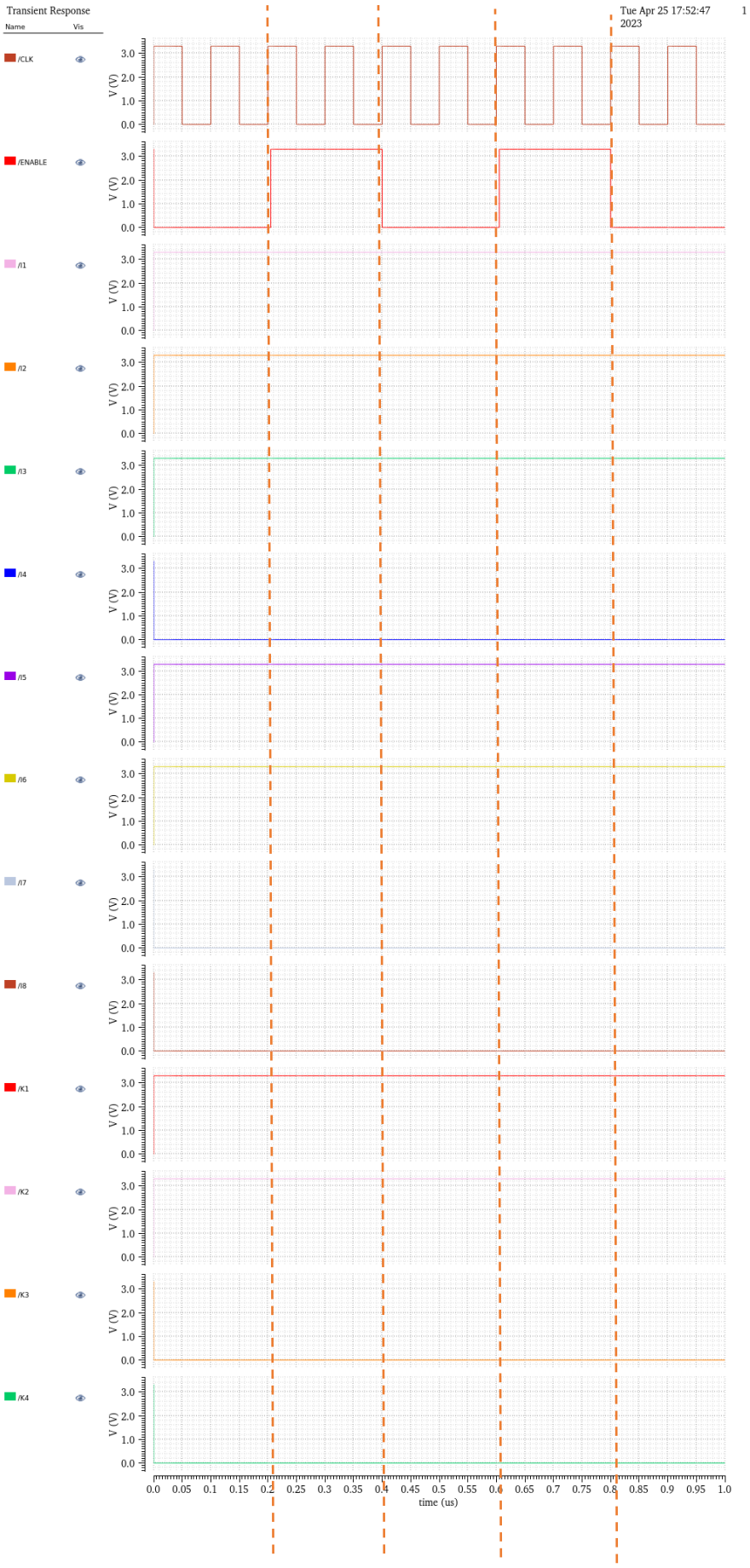


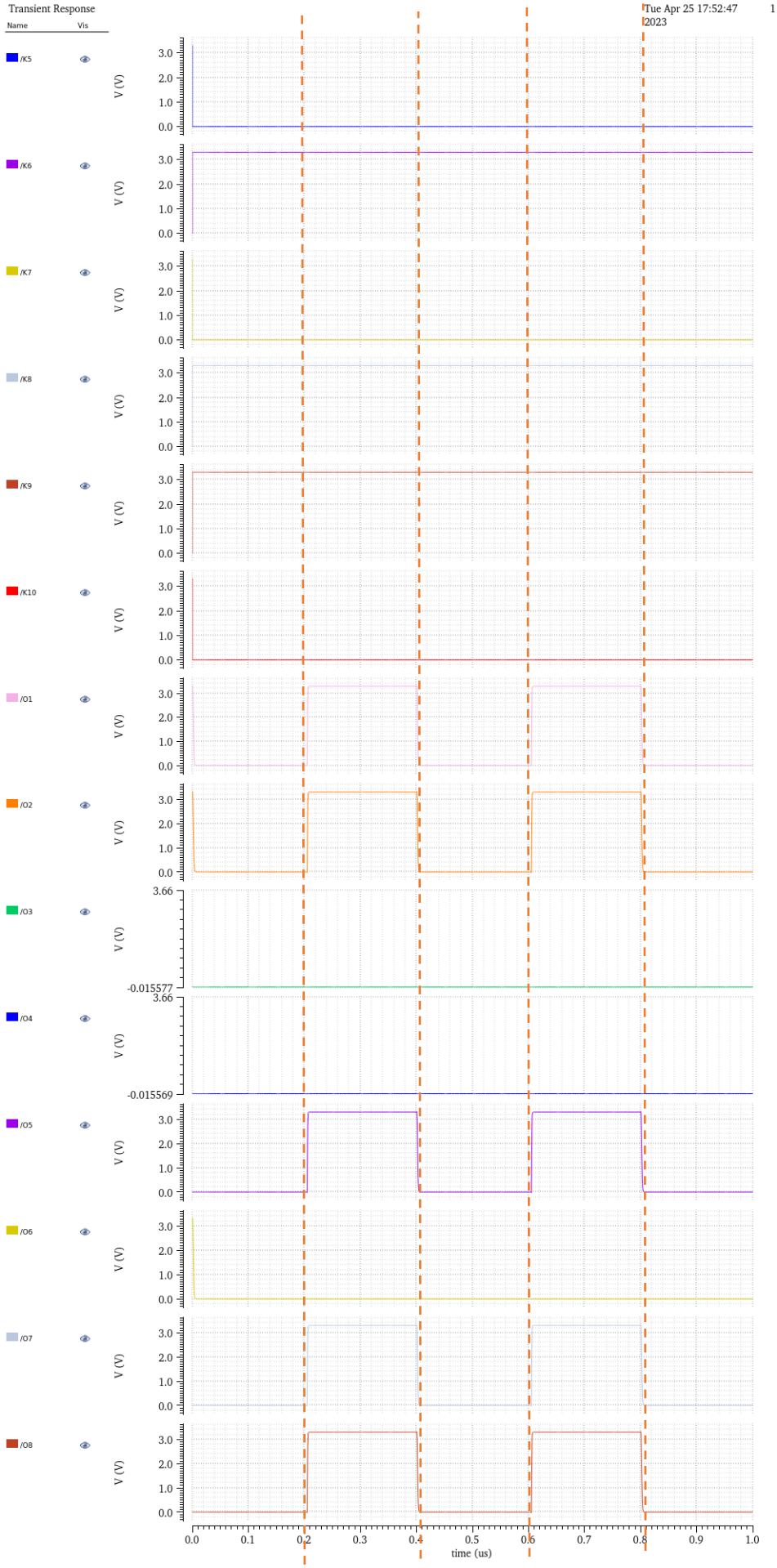
* Below is the second half.



6. Schematic timing diagram result

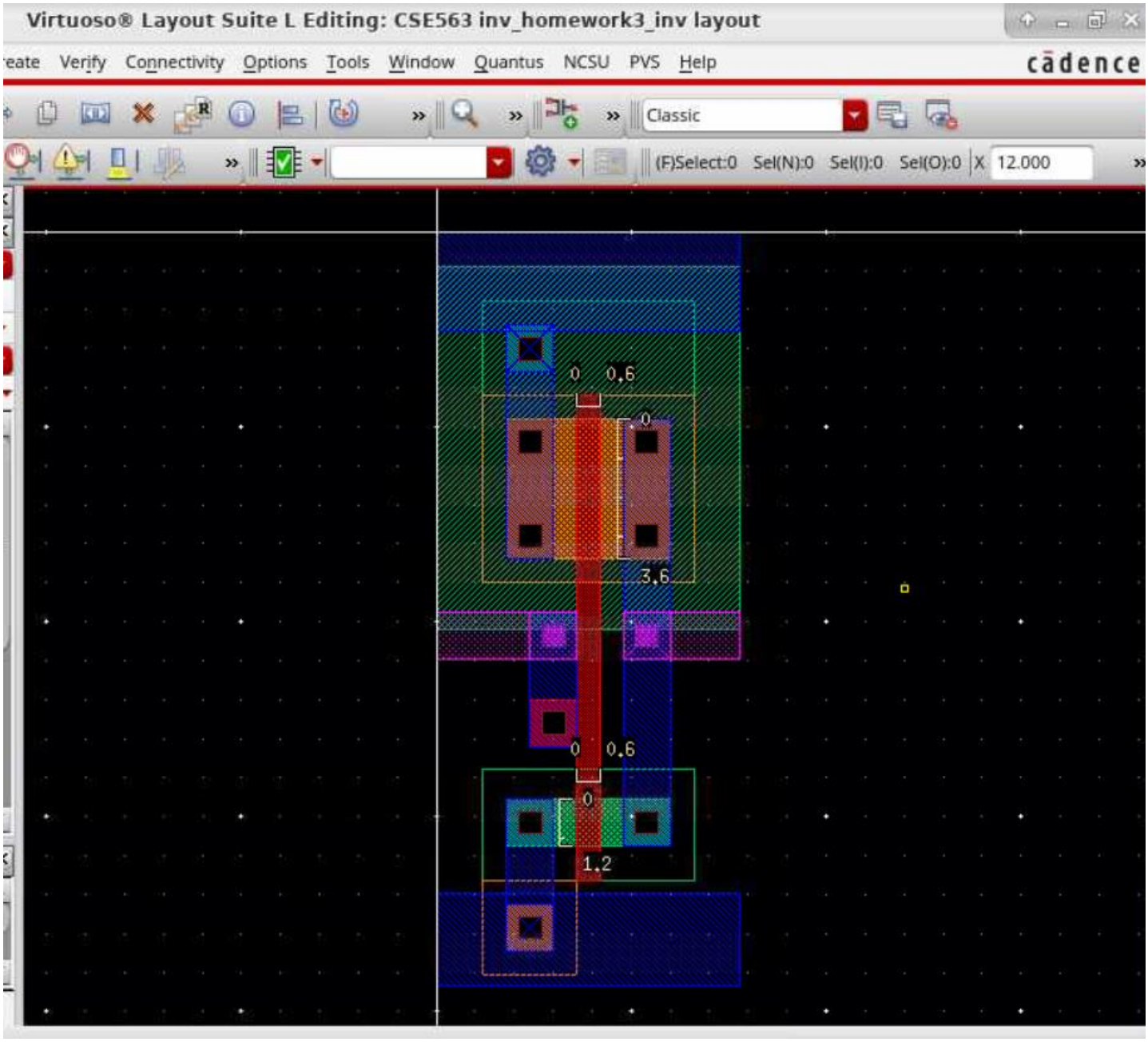
* Test result: CLK, ENABLE, Input(I1, I2, …, I8), Key(K1, K2, …, K10), Output(O1, O2, …, O8)



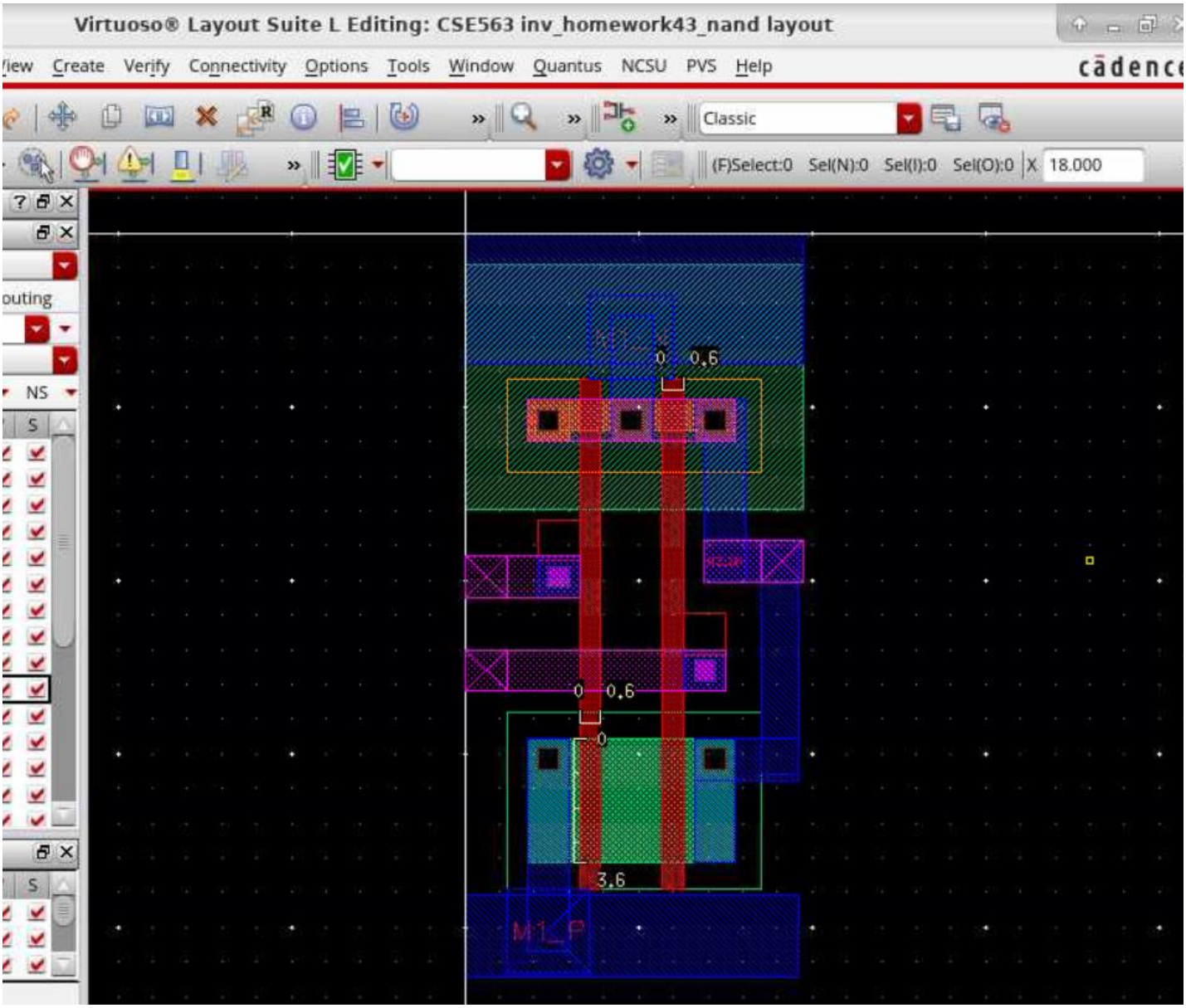

Transient Response
Tue Apr 25 17:52:47 2023
1
Name
Vis
/K5
/K6
/K7
/K8
/K9
/K10
/O1
/O2
/O3
/O4
/O5
/O6
/O7
/O8
V (V)
3.0
2.0
1.0
0.0
3.66
-0.015577
-0.015569
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
time (us)

7. Layout

* INVERTOR



* NAND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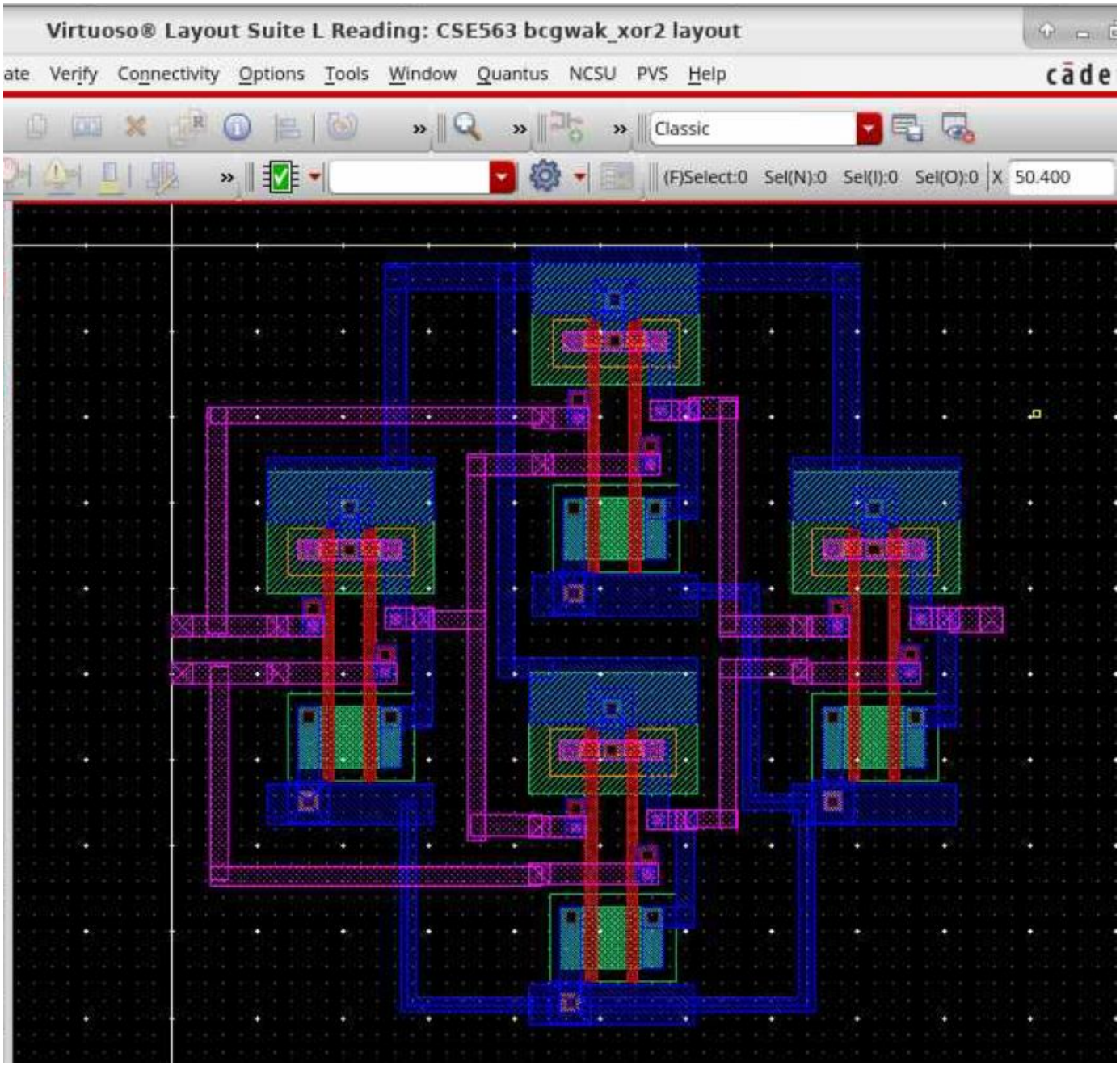
Create
Verify
Connectivity
Options
Tools
Window
Quantus
NCSU
PVS
Help
cadence
Classic
(F)Select:0
Sel(N):0
Sel(I):0
Sel(O):0
X
18.000
0
0.6
0
0.6
0
3.6
M1_P

* XOR2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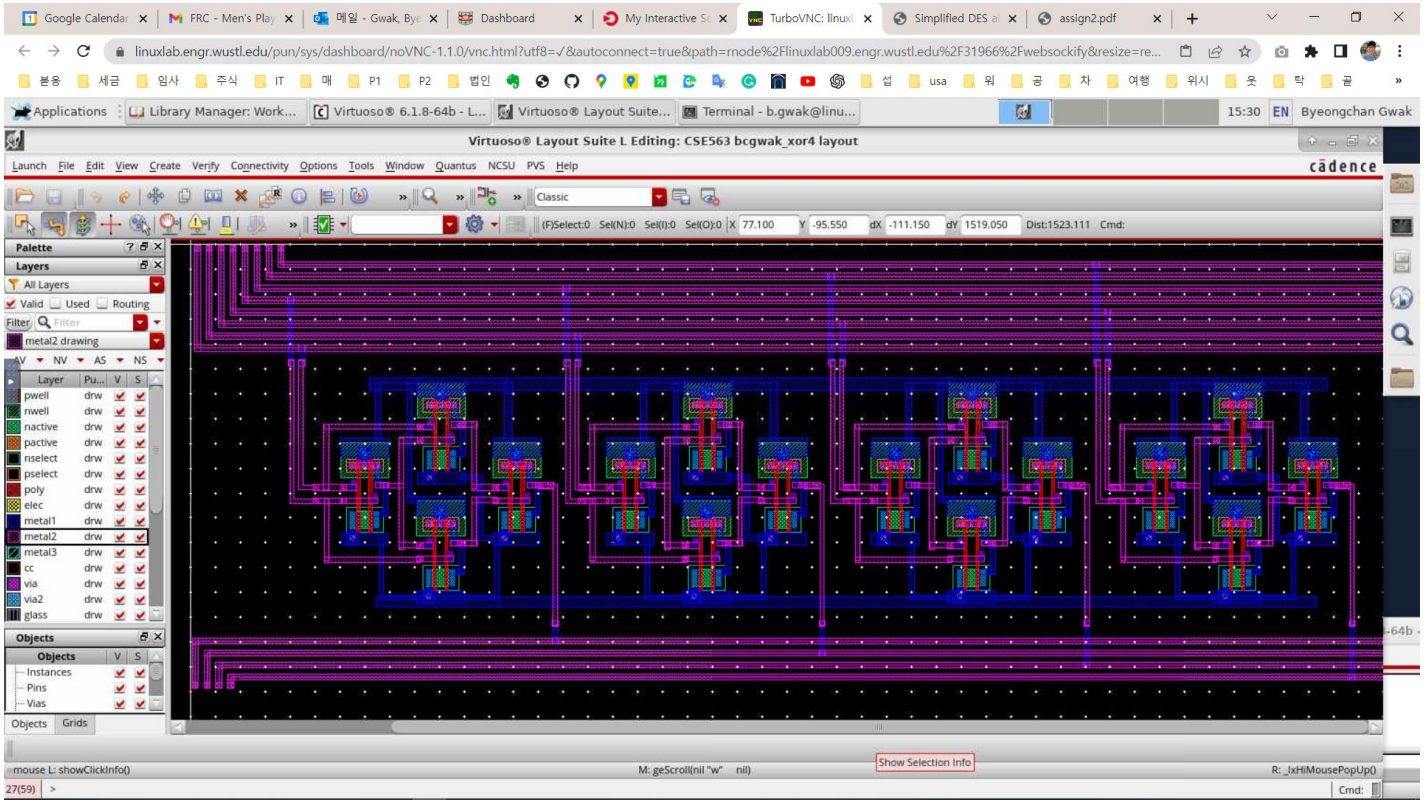
ate Verify Connectivity Options Tools Window Quantus NCSU PVS Help
cāde
Classic
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X 50.400

* XOR4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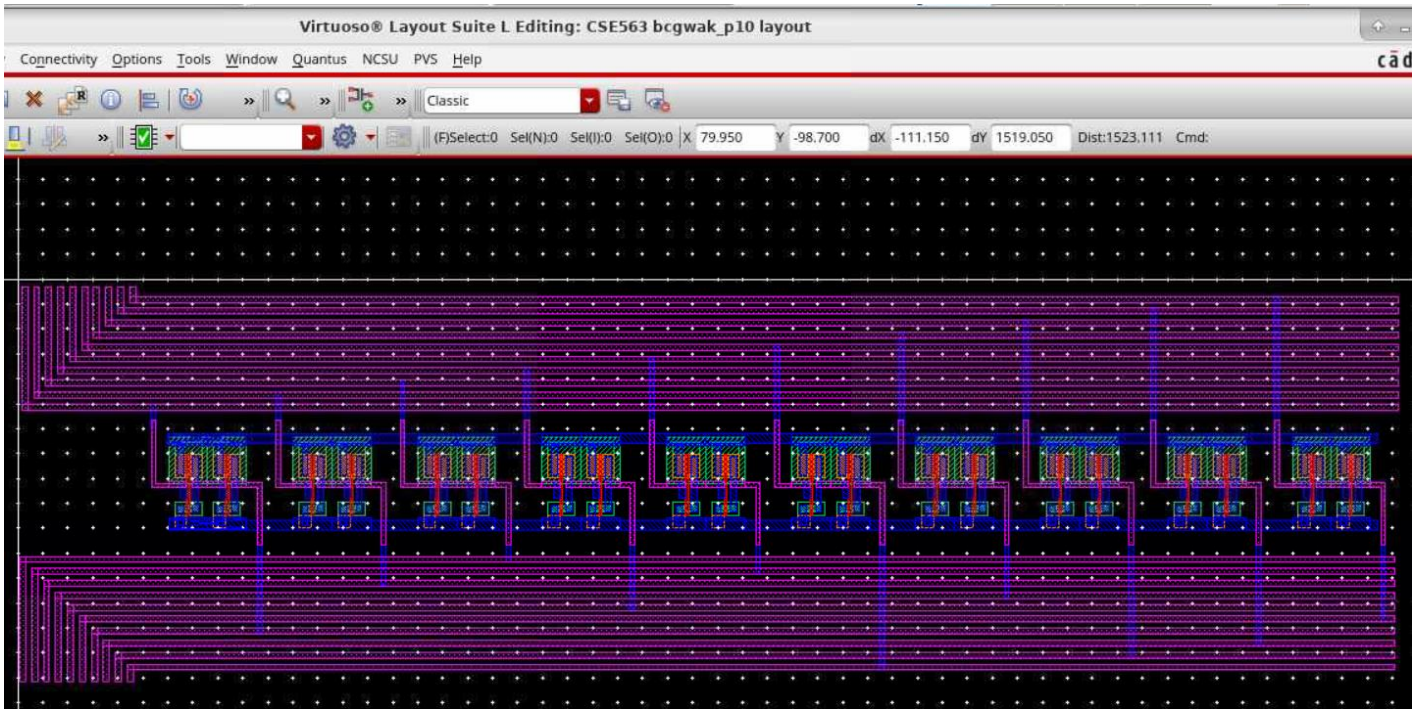
Launch File Edit View Create Verify Connectivity Options Tools Window Quantus NCSU PVS Help
cadence
Palette
Layers
All Layers
Valid Used Routing
metal2 drawing
Objects
Instances
Pins
Vias
Show Selection Info

* P10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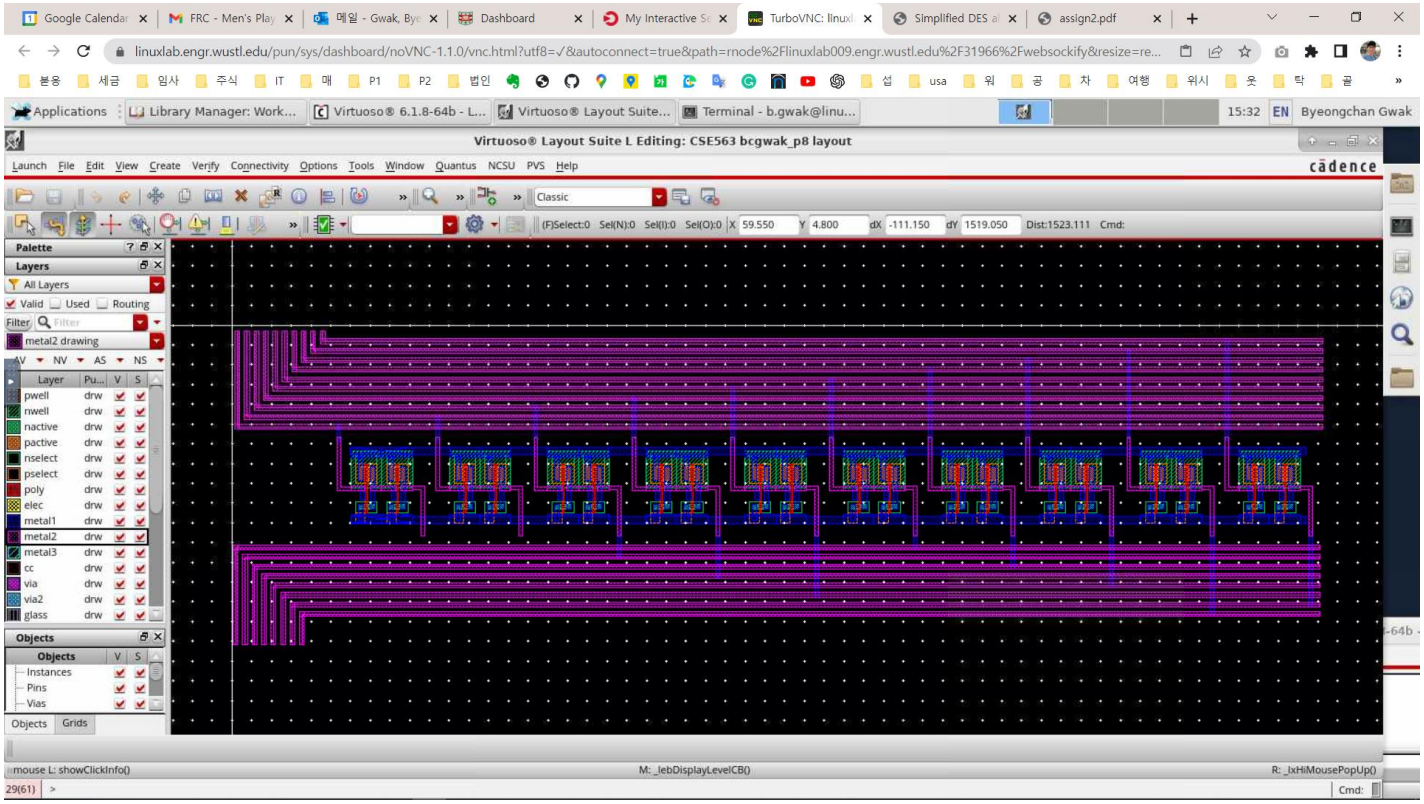
Connectivity Options Tools Window Quantus NCSU PVS Help
Classic
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X 79.950 Y -98.700 dX -111.150 dY 1519.050 Dist:1523.111 Cmd:

* P8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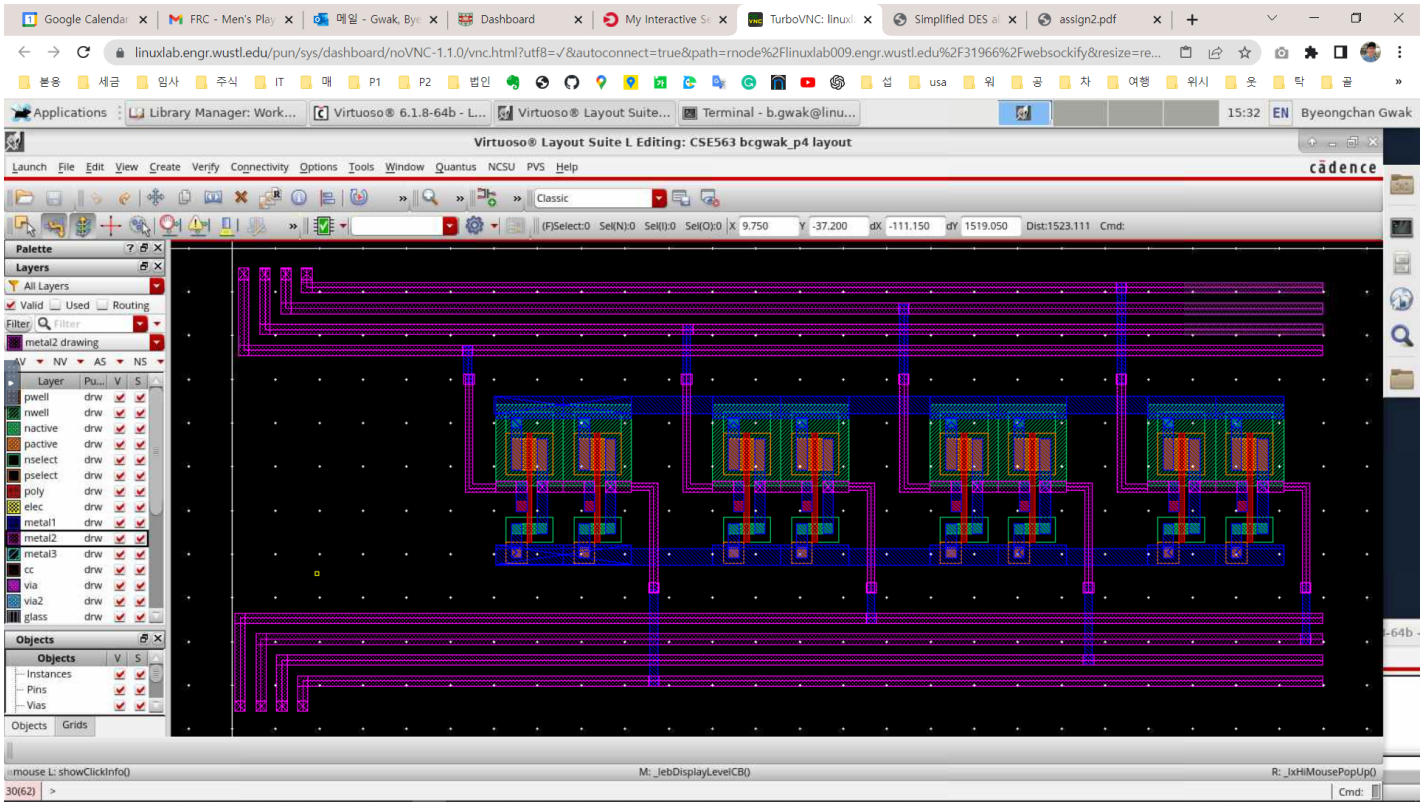
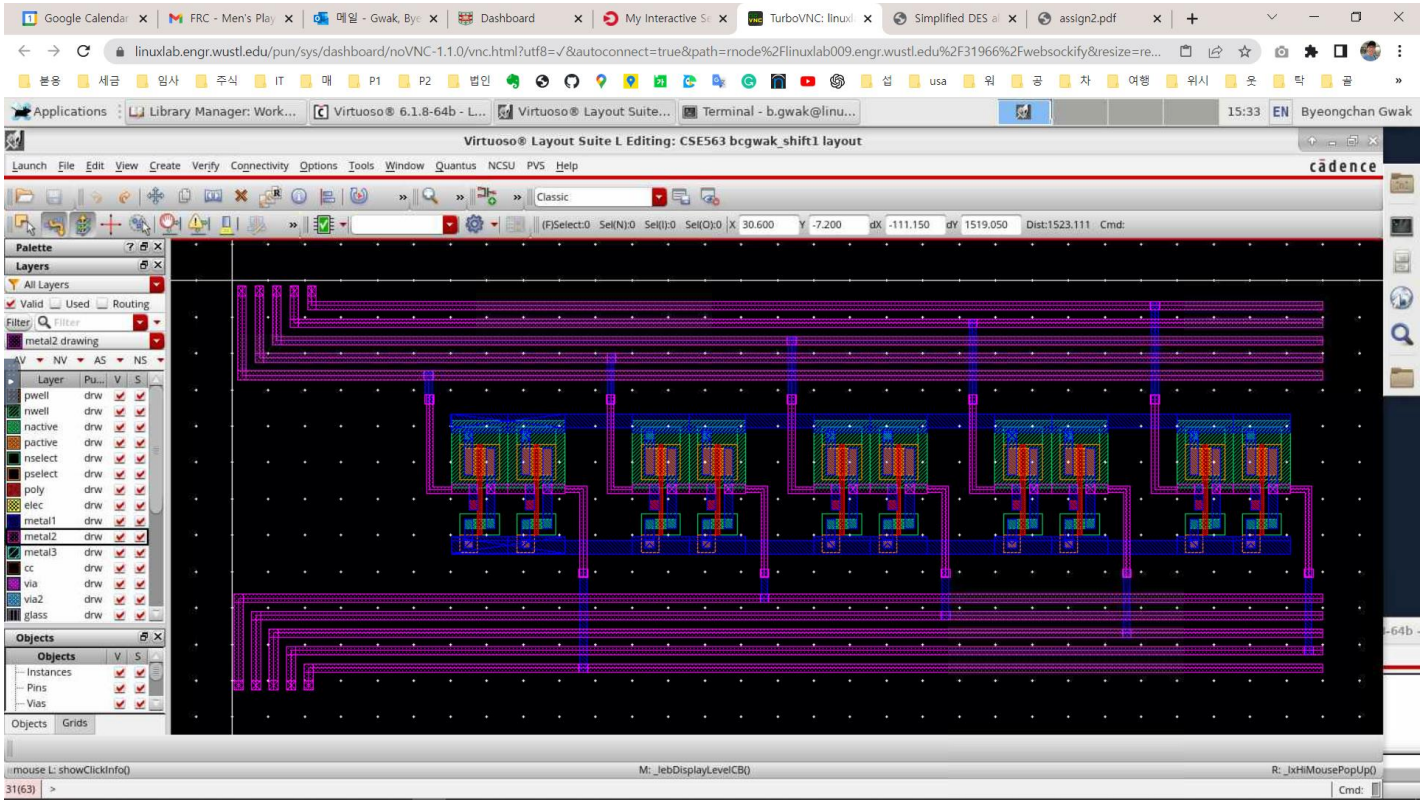
cadence

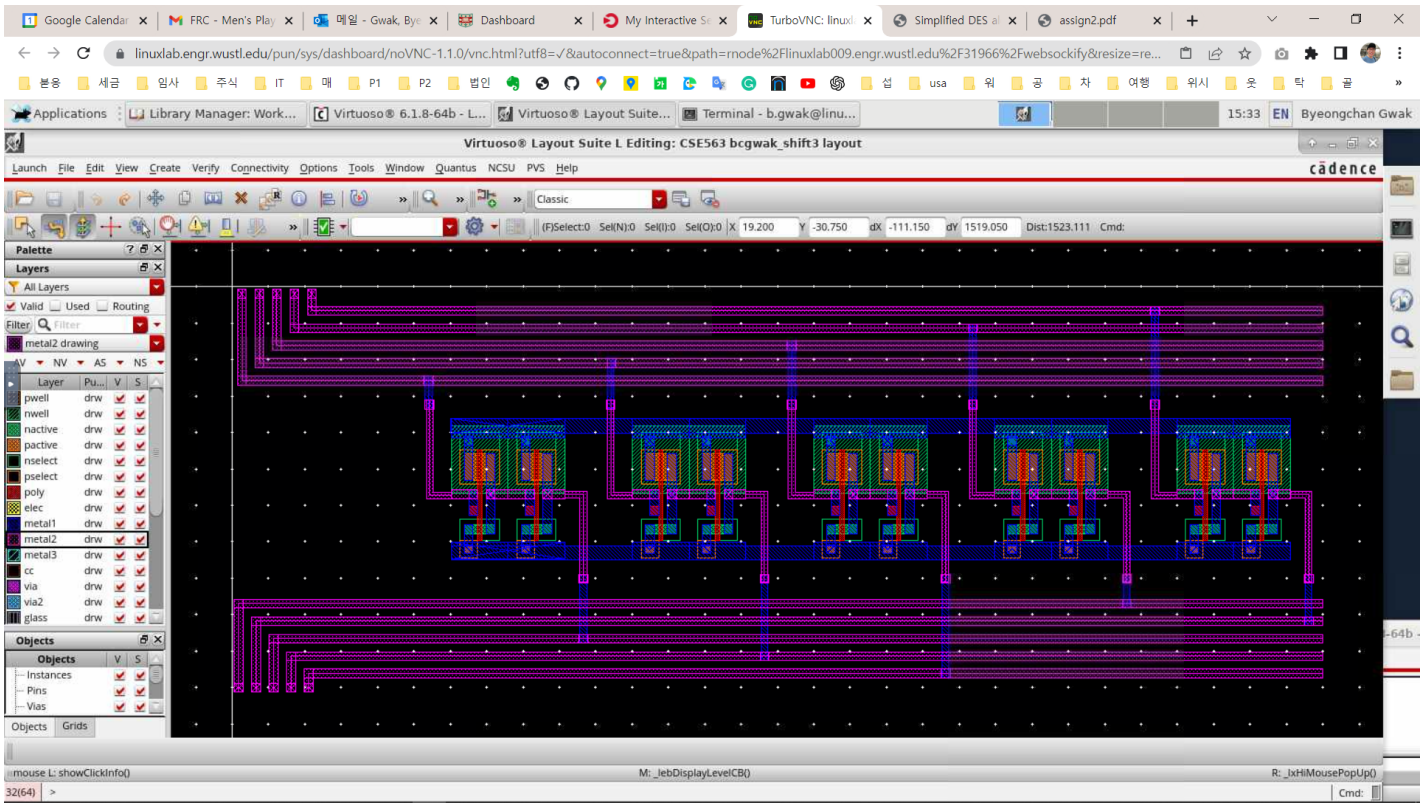
* P4


Virtuoso® Layout Suite L Editing: CSE563 bcgwak_p4 layout
cadence

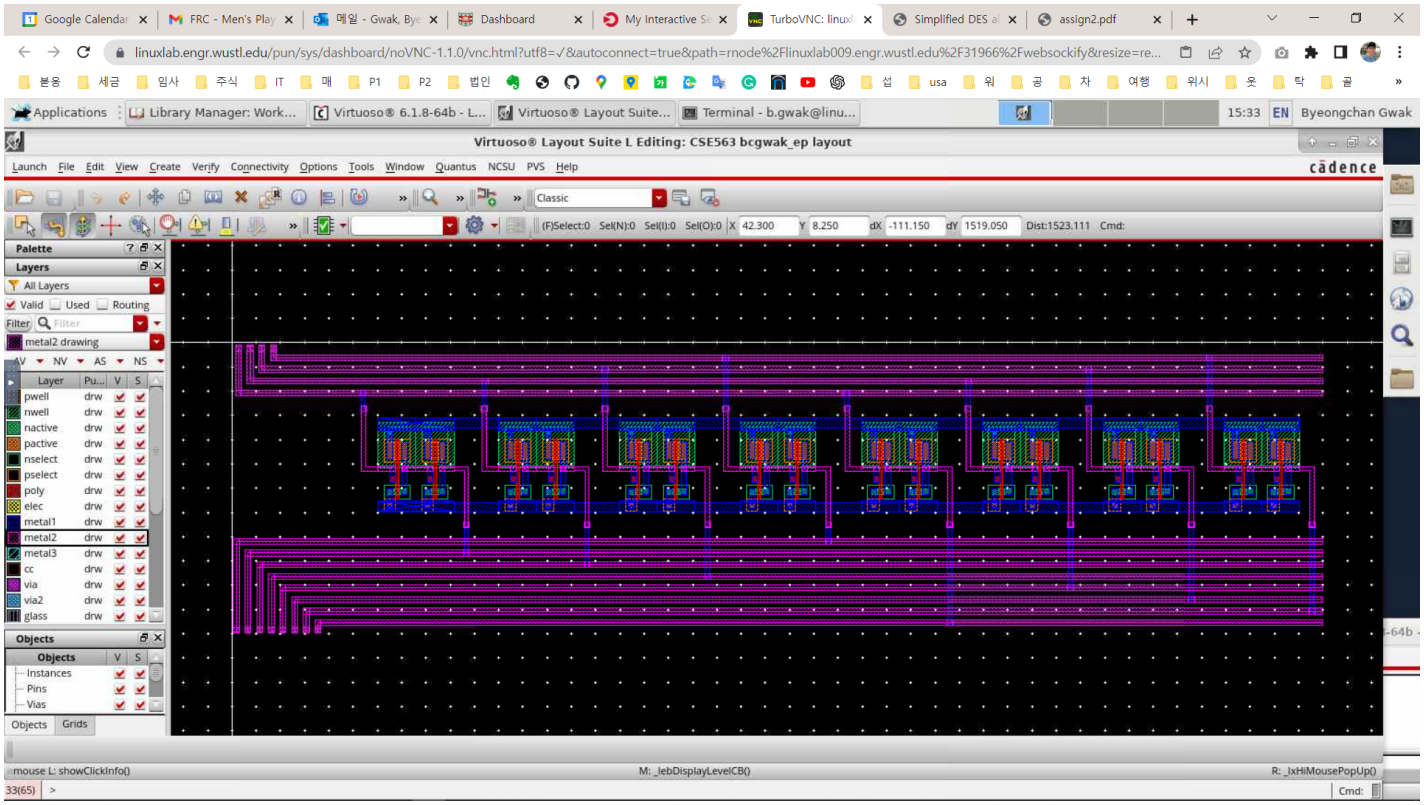
* SHIFT 1



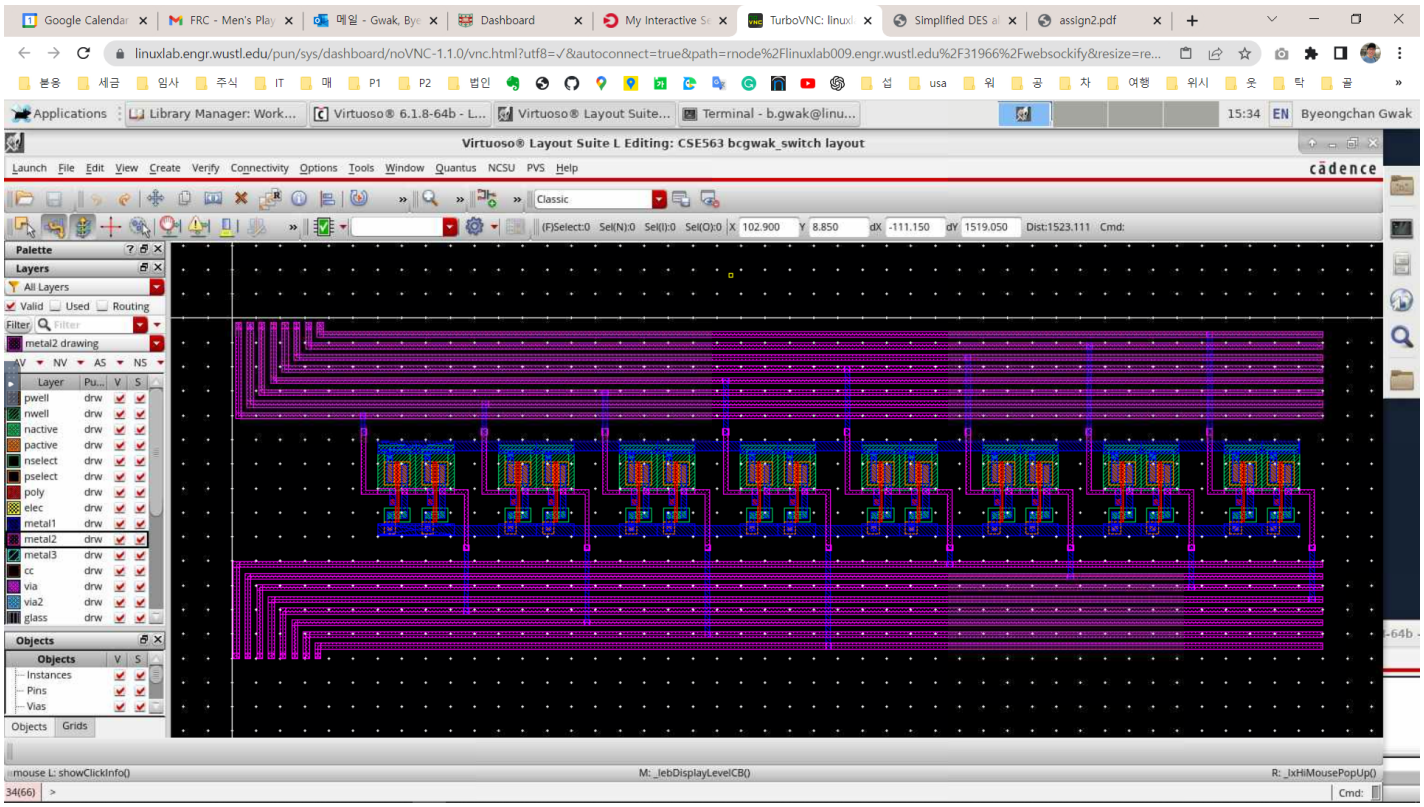
* SHIFT 3



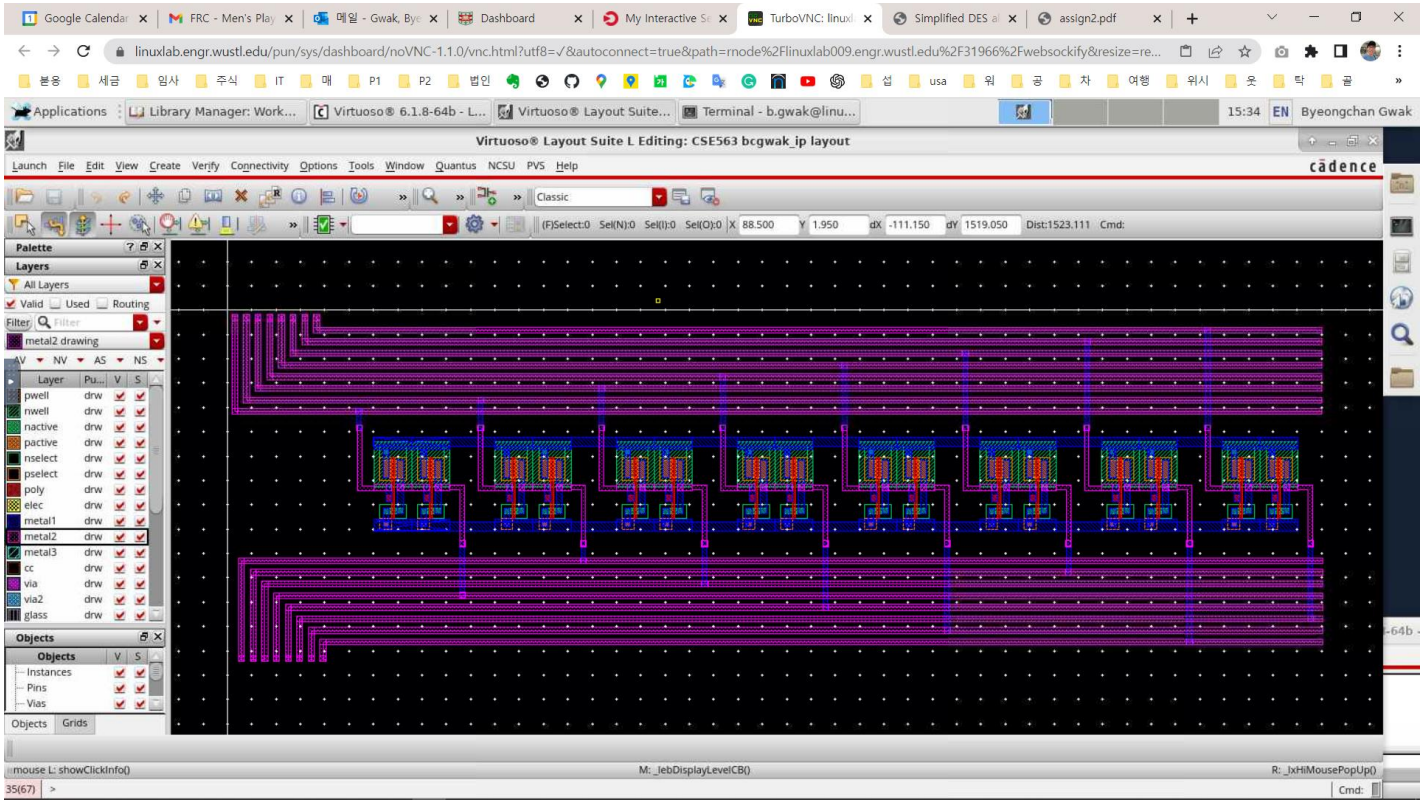
* EP


Virtuoso® Layout Suite L Editing: CSE563 bcgwak_ep layout
cadence

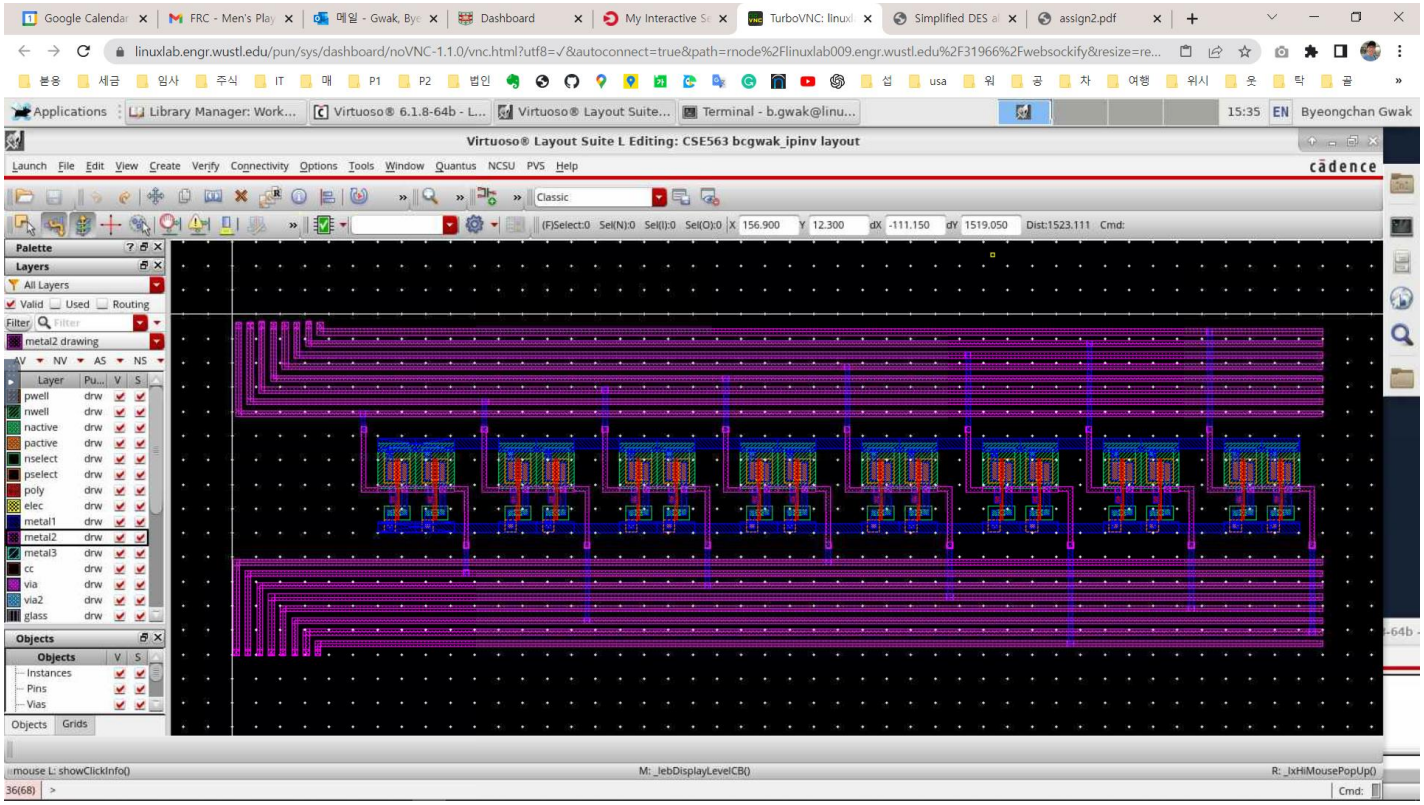
* SWITCH


Virtuoso® Layout Suite L Editing: CSE563 bcgwak_switch layout
cadence

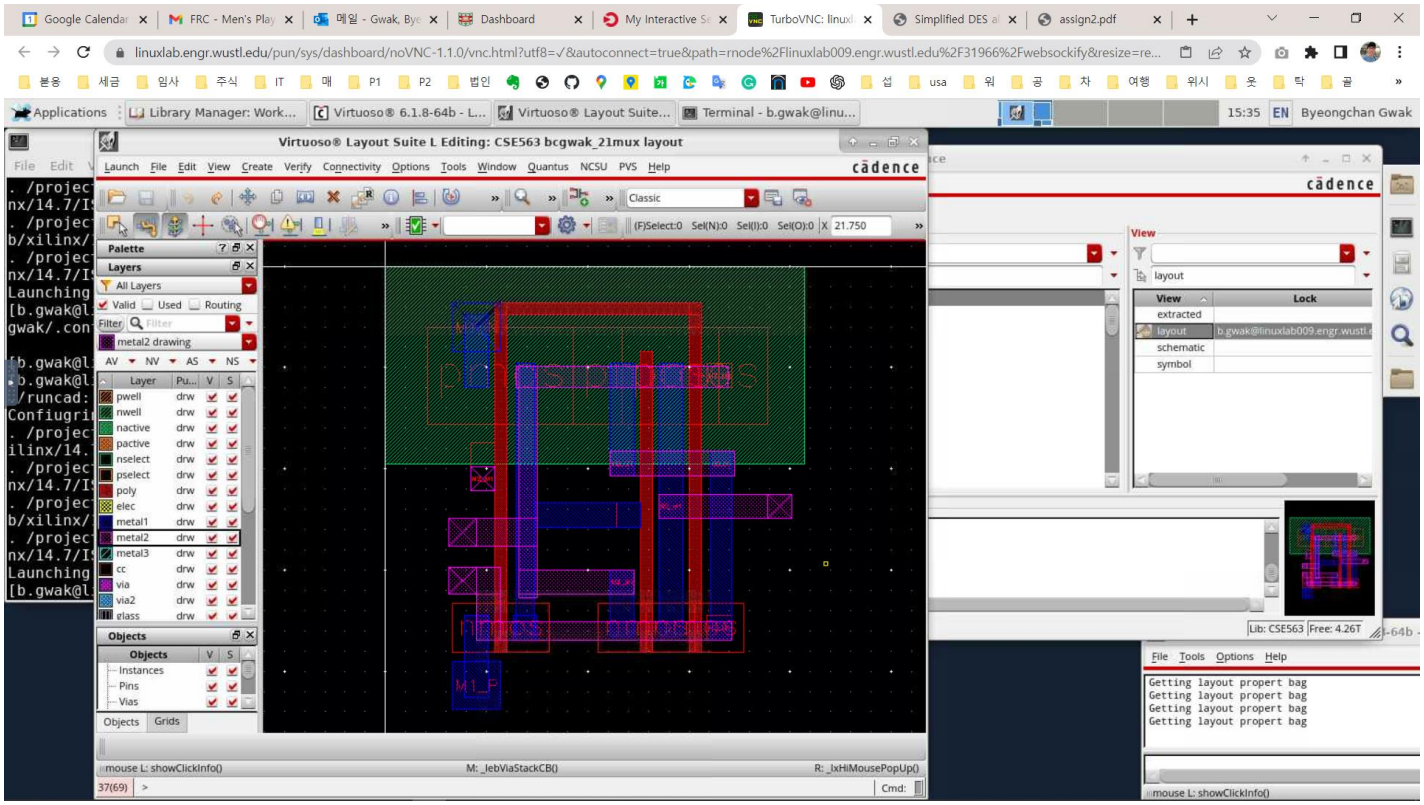
* IP


Virtuoso® Layout Suite L Editing: CSE563 bcgwak_ip layout
cadence

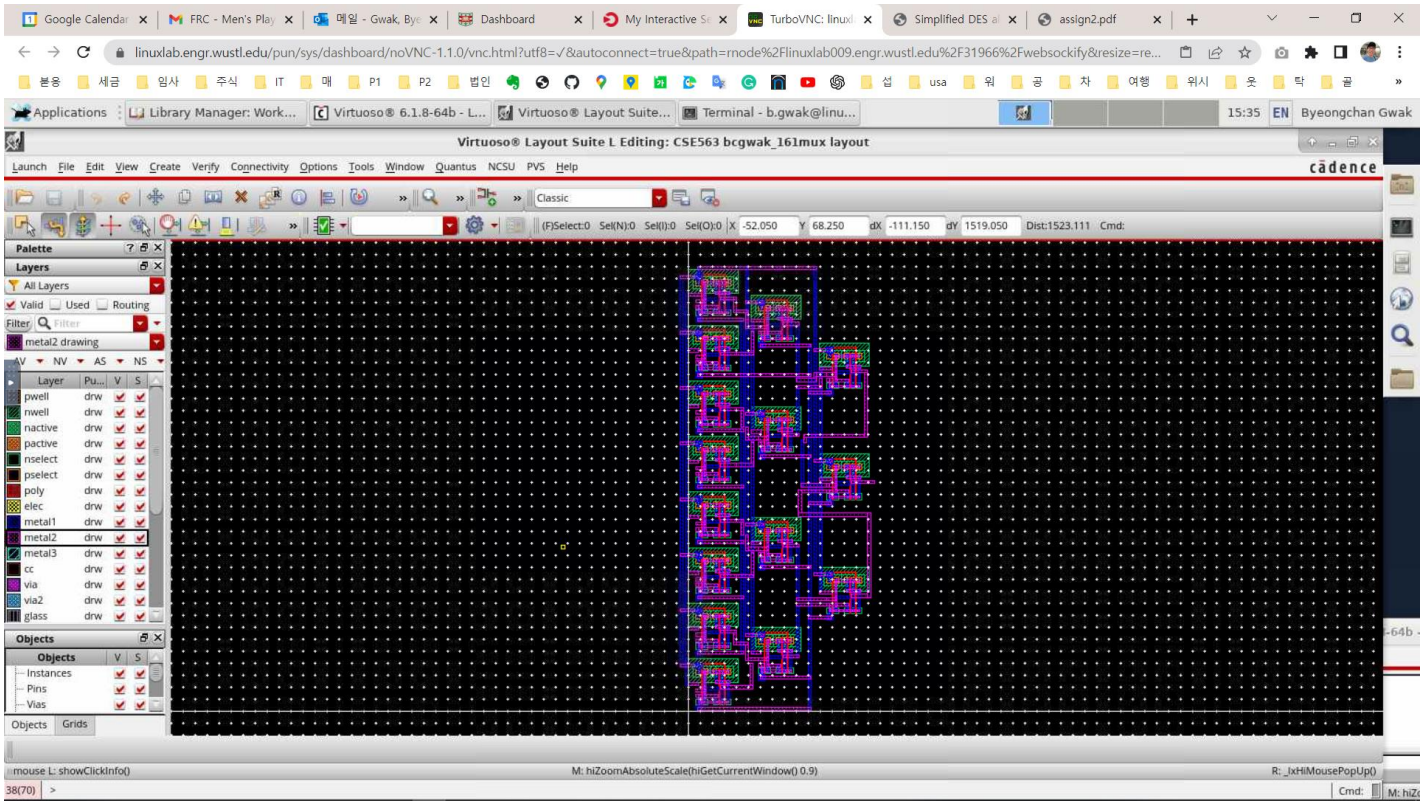
* IP Invert


Virtuoso® Layout Suite L Editing: CSE563 bcgwak_ipinv layout
cadence

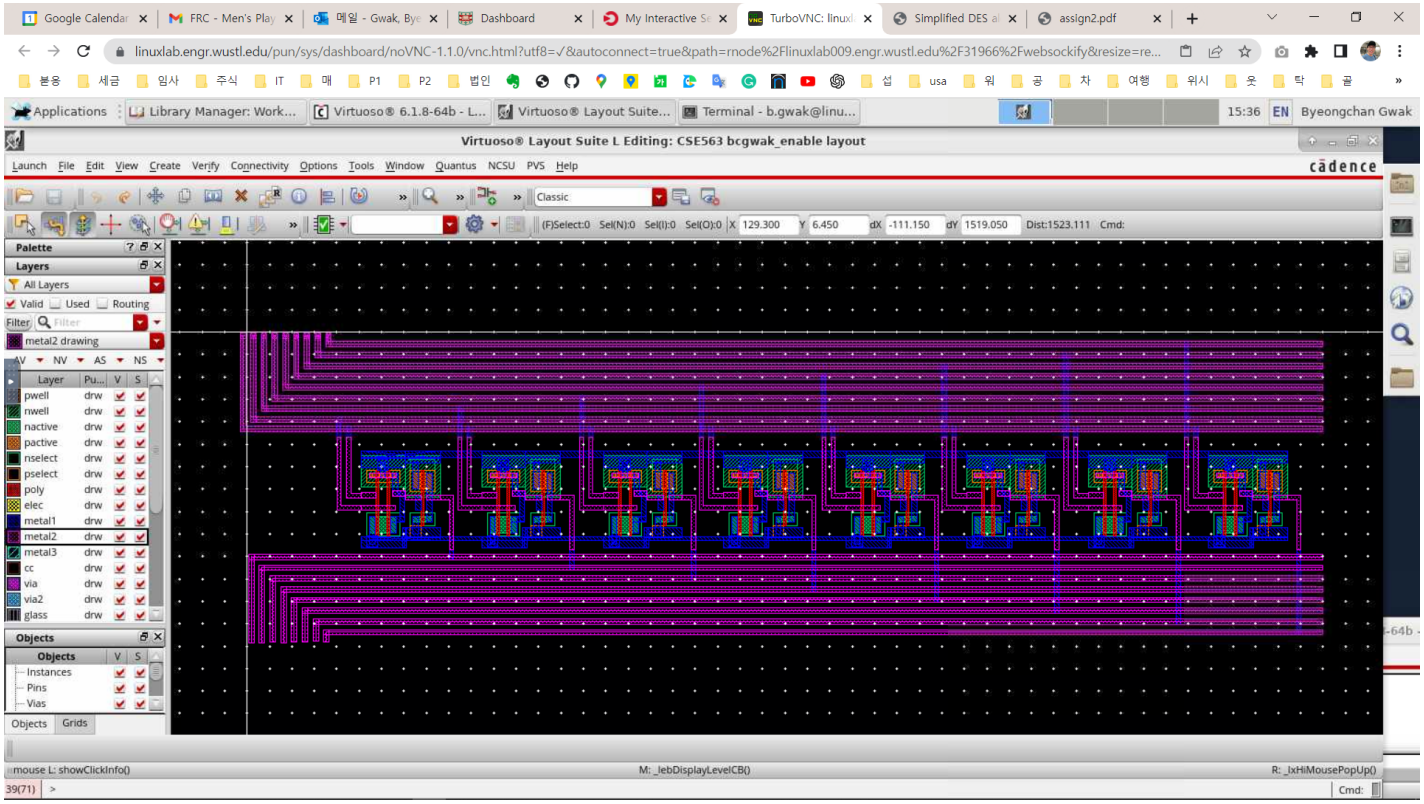
* 2:1 mux



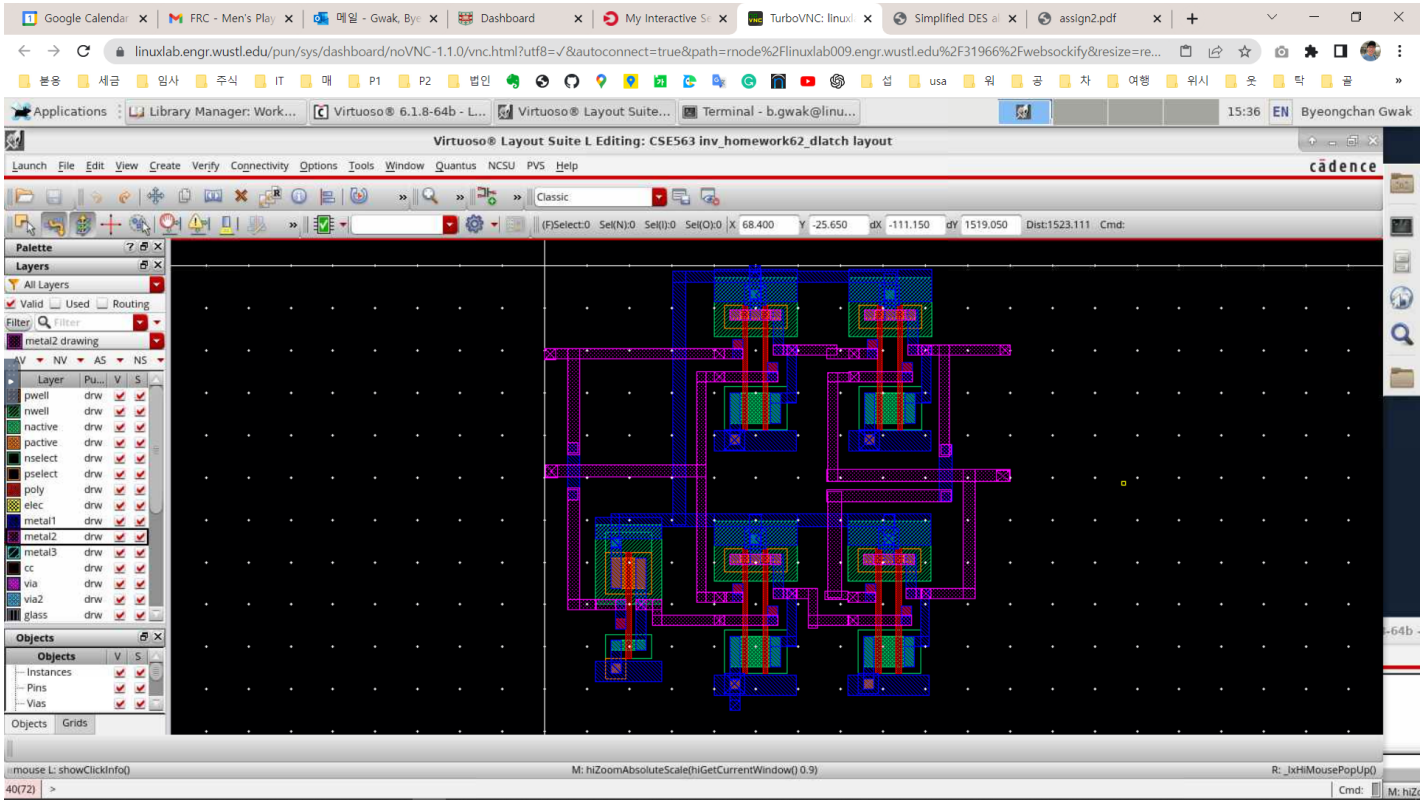
* 16:1 mux



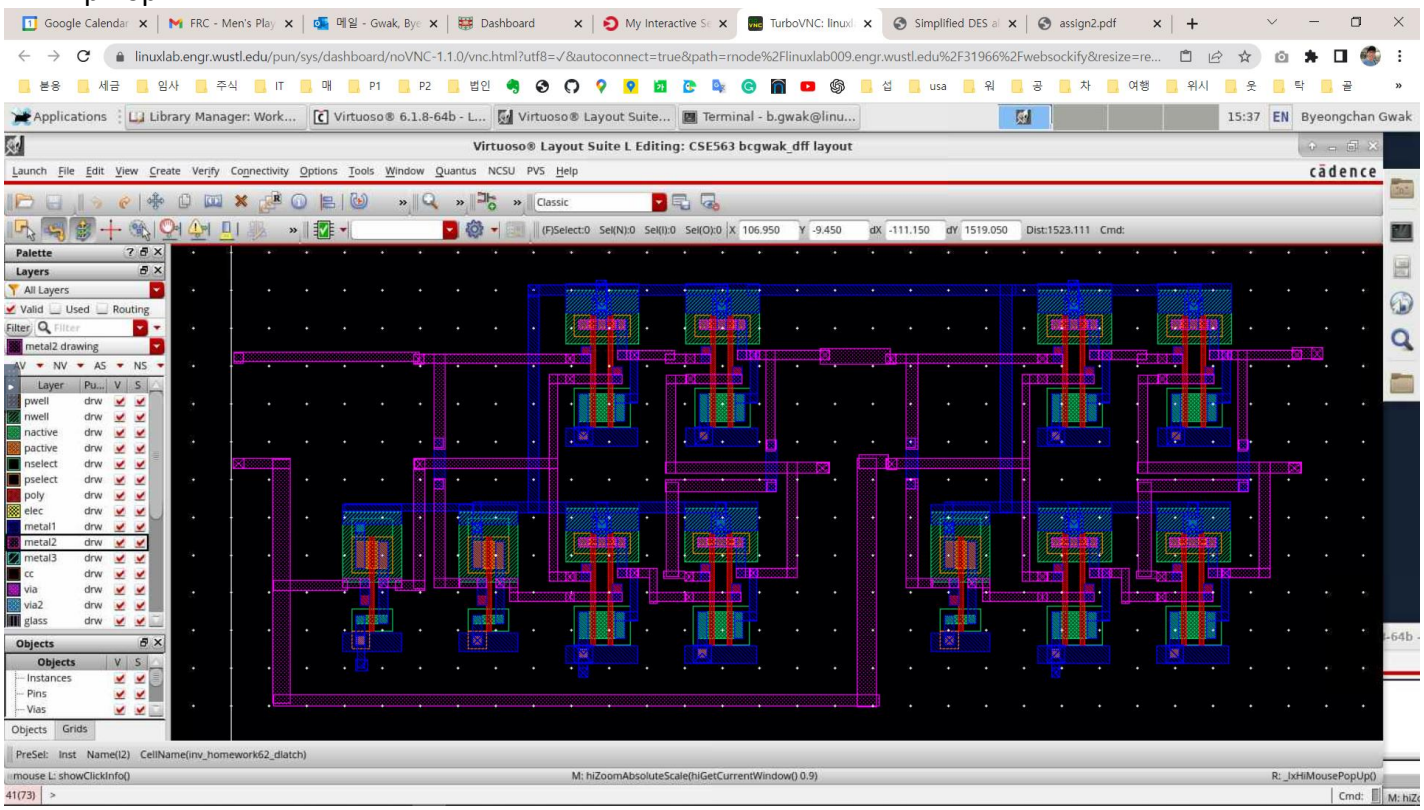
* ENABLE


Virtuoso® Layout Suite L Editing: CSE563 bcgwak_enable layout
cadence
Palette
Layers
All Layers
metal2 drawing
Objects
Instances
Pins
Vias

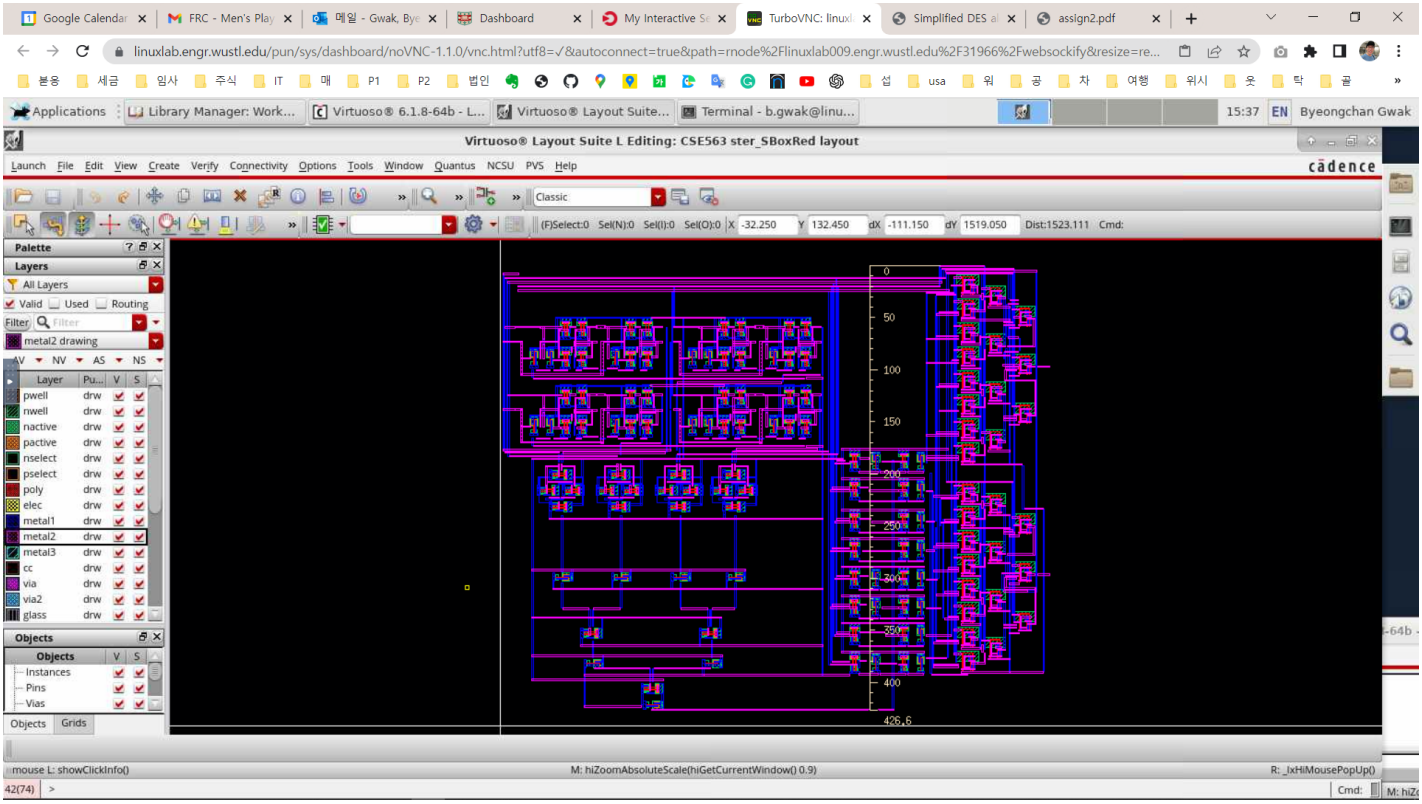
* D-LATCH



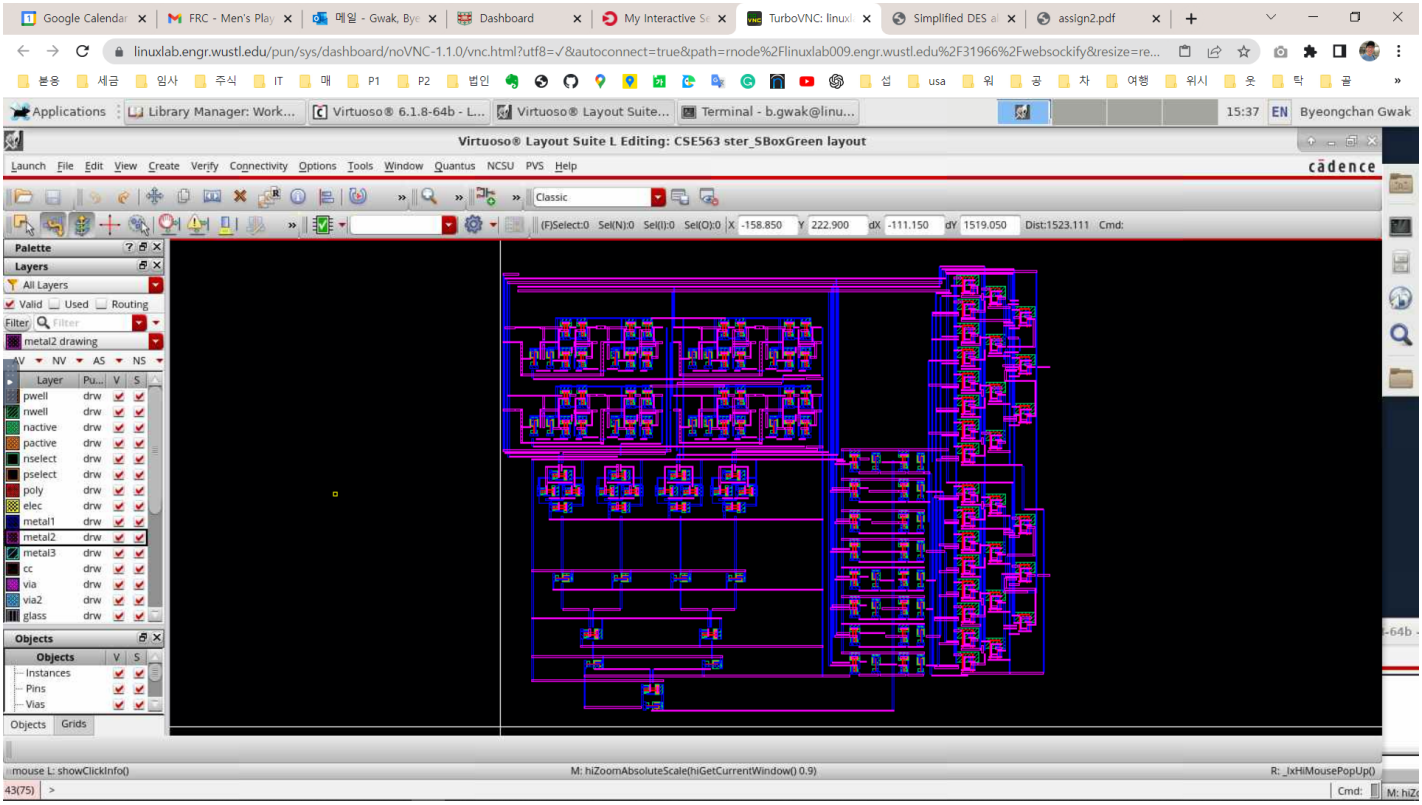
* D Flip flop



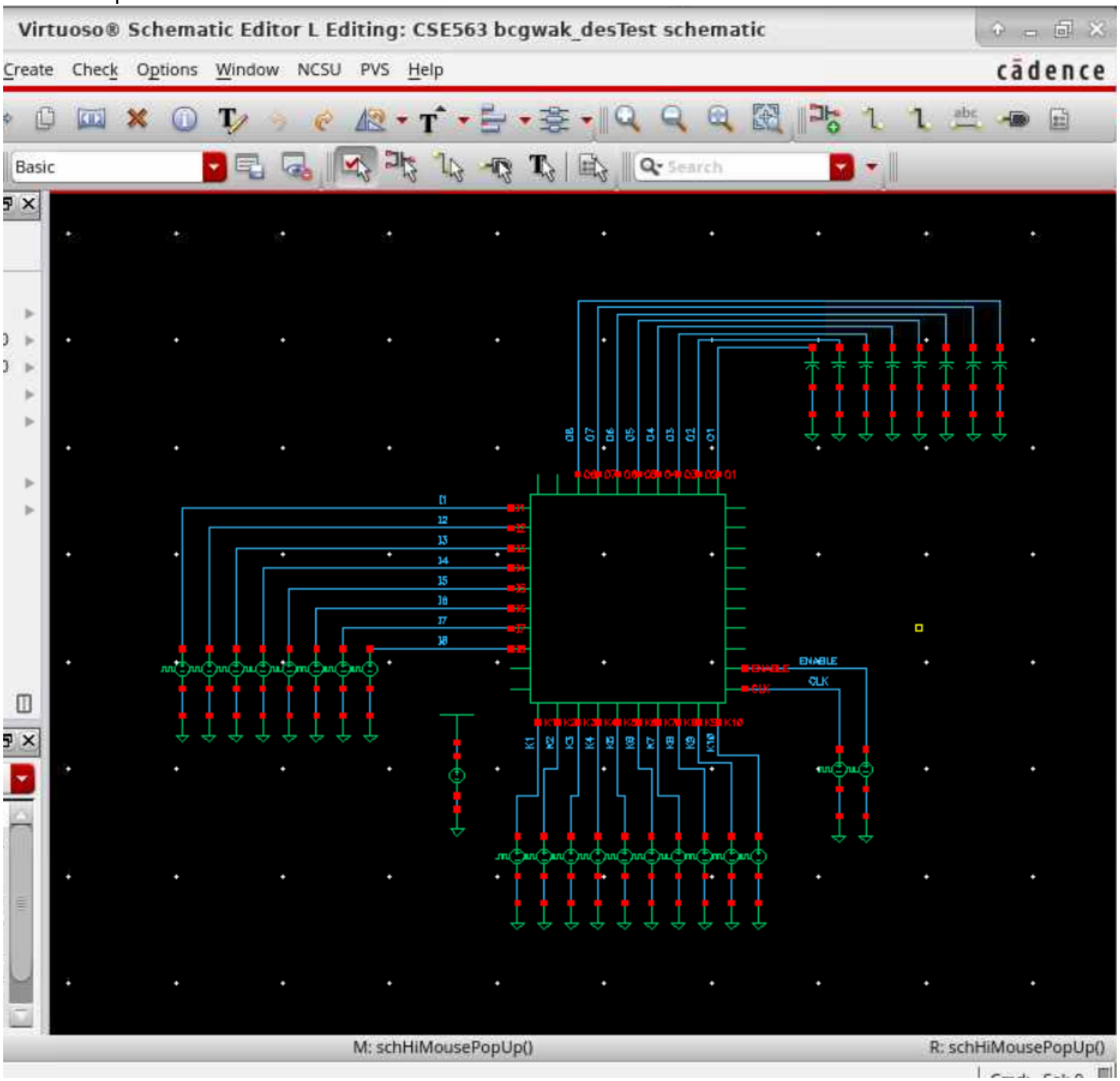
* SBox Red



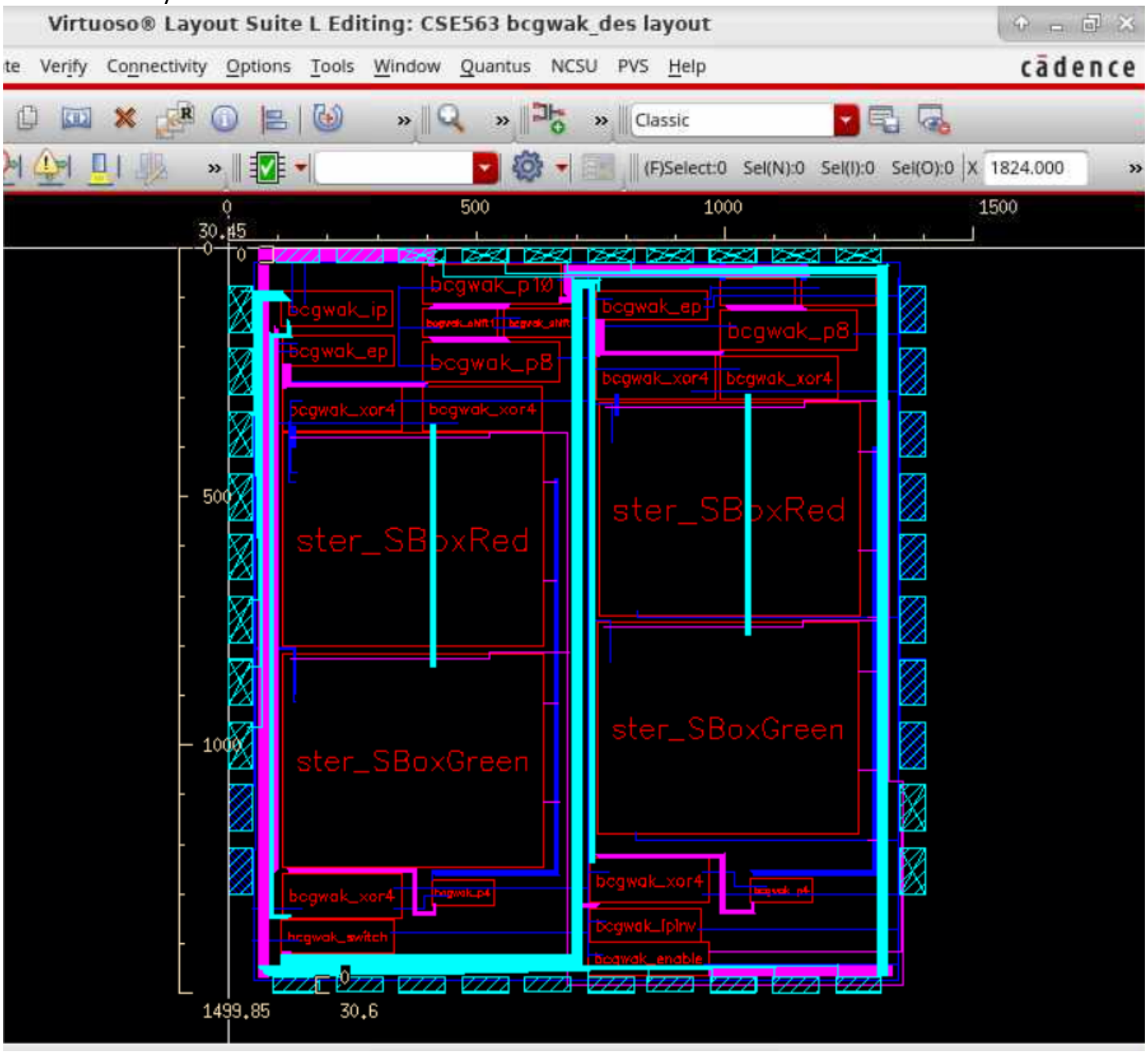
* SBox Green

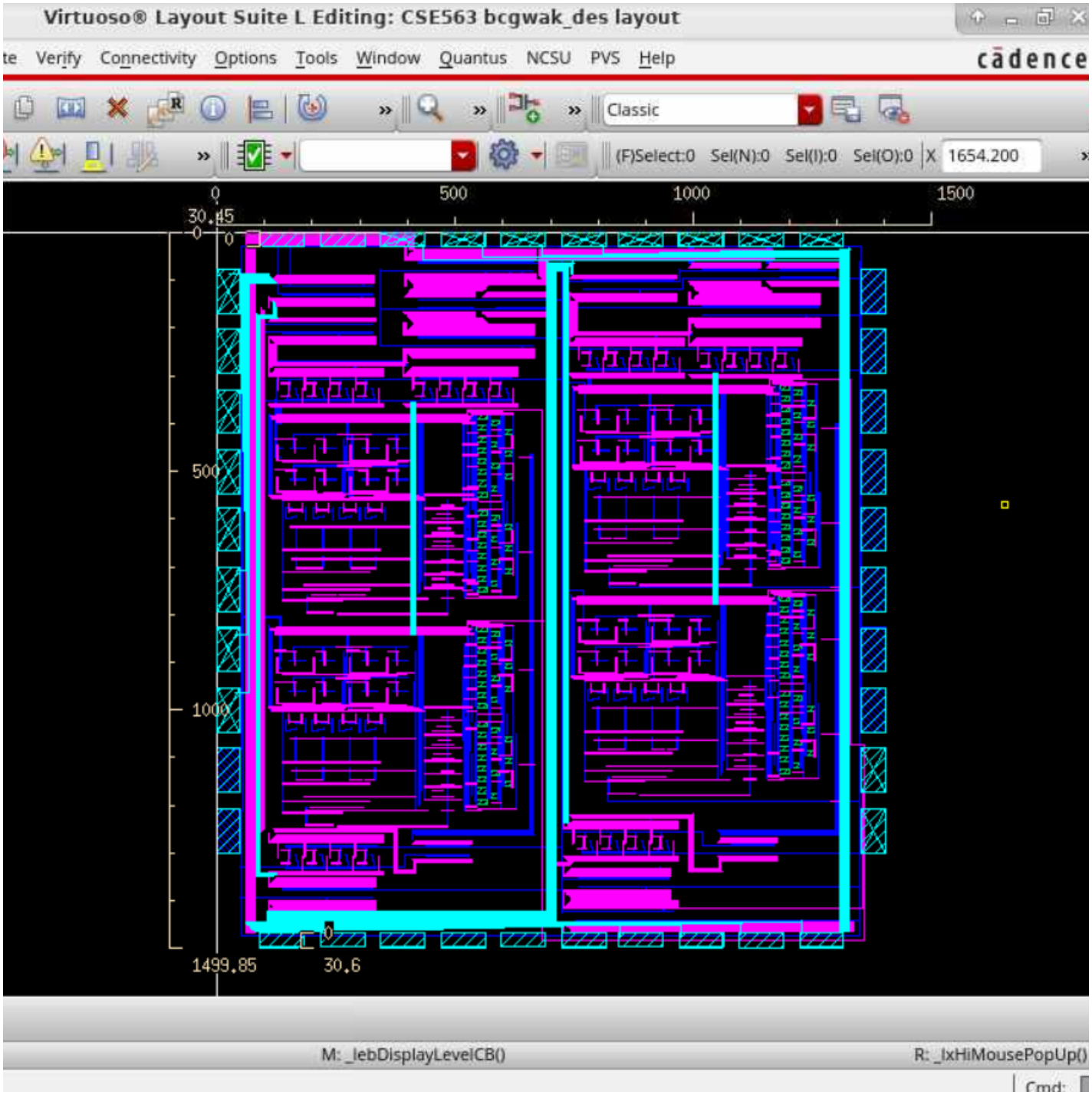


* Test setup for the DES.



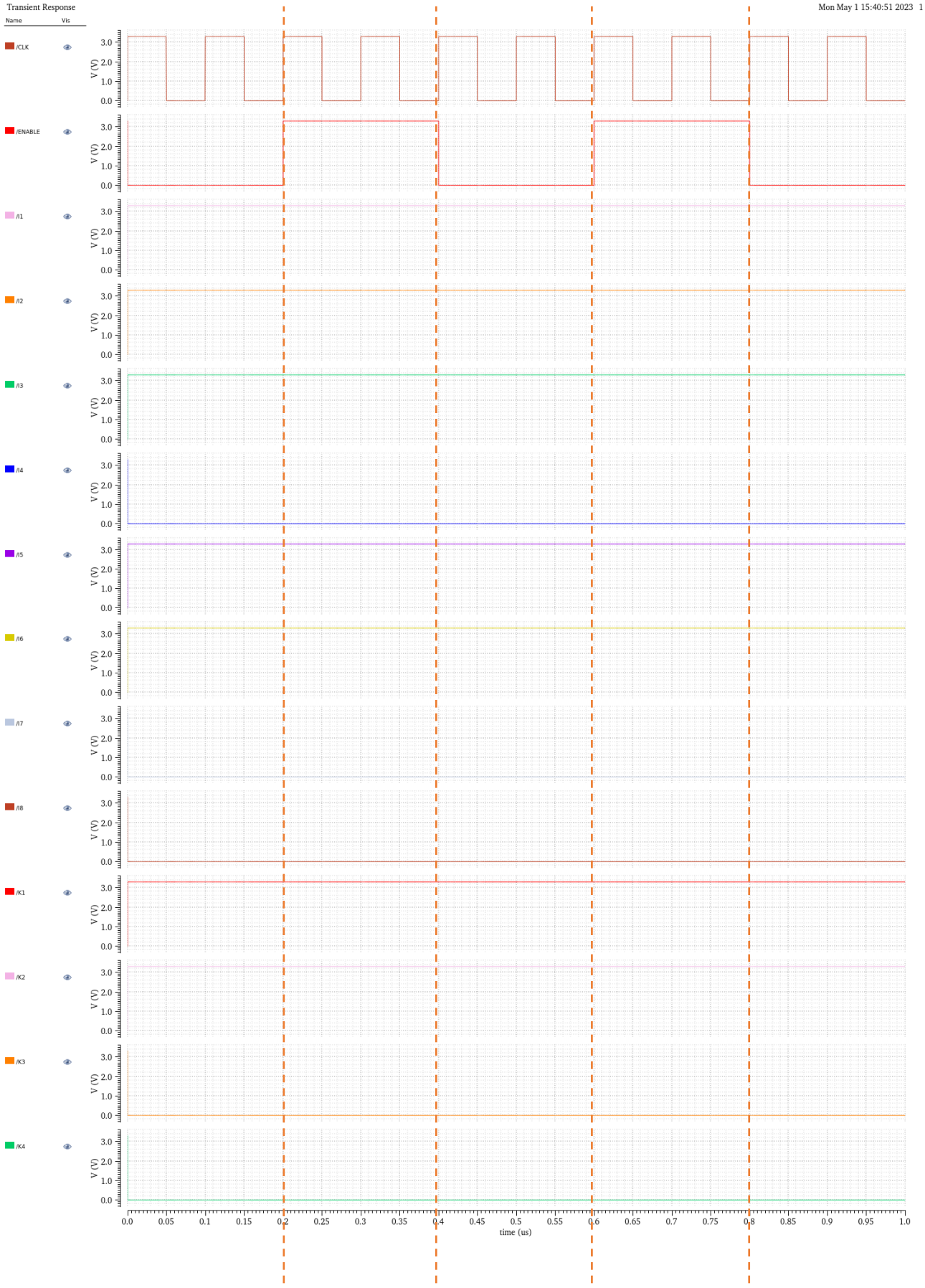
* Whole DES layout. The size is checked with the ruler.

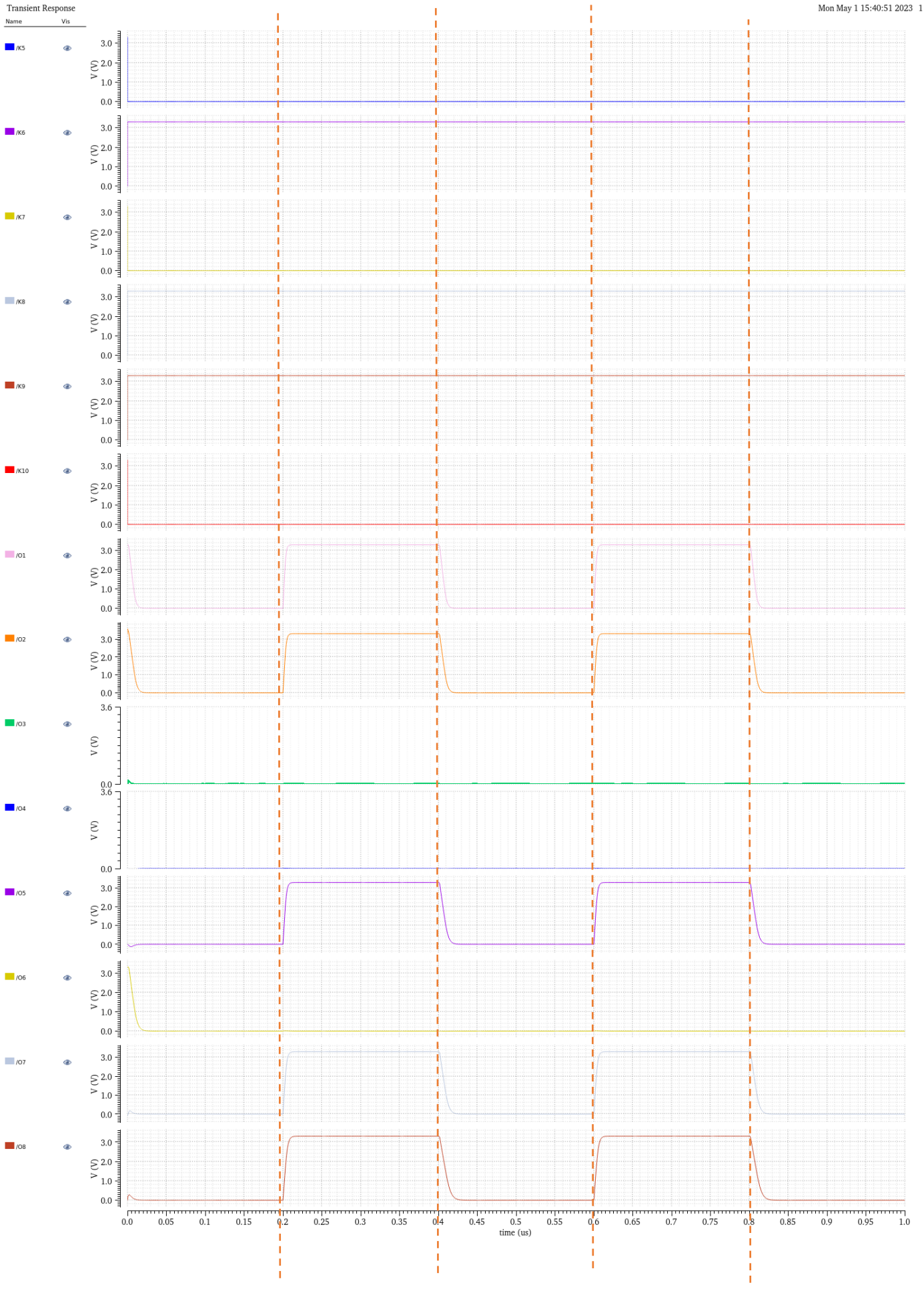



Virtuoso® Layout Suite L Editing: CSE563 bcgwak_des layout
te Verify Connectivity Options Tools Window Quantus NCSU PVS Help
cadence
Classic
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X 1654.200
0
500
1000
1500
30.45
0
500
1000
1499.85
30.6
M: _lebDisplayLevelCB()
R: _lxHiMousePopUp()
Cmd:

8. Layout timing diagram result

* Test result: CLK, ENABLE, Input(I1, I2, …, I8), Key(K1, K2, …, K10), Output(O1, O2, …, O8)




Transient Response
Mon May 1 15:40:51 2023 1
Name
Vis
/K5
/K6
/K7
/K8
/K9
/K10
/O1
/O2
/O3
/O4
/O5
/O6
/O7
/O8
V (V)
3.0
2.0
1.0
0.0
3.6
0.0 0.05 0.1 0.15 0.2 0.25 0.3 0.35 0.4 0.45 0.5 0.55 0.6 0.65 0.7 0.75 0.8 0.85 0.9 0.95 1.0
time (us)

9. Investigation of how fast CLOCK signal can be(CSE563)

- The current clock rate is 10 MHz, or 100 ns. What needs to be considered to increase the clock speed is the parasitic capacitance. Looking at the graph above, the delay due to parasitic capacitance is about 10 ns. In the end, it is concluded that even if CLOCK is increased as much as possible, it is difficult to reduce it to less than 10 ns.