CSE 463-563: Digital Integrated Circuits Design and Architecture

Exam 1: MOS Transistor Theory and Inverter

(Open book, Open Notes, Calculator or Wolfram-Alpha app are allowed)

March 23th, 2023

Attempt all questions. Show all calculations to obtain partial credits. If you run out of time, outline how you would approach the problem.

Total possible points: 200 for CSE463 students (Problems 1, 2, and 3)
270 for CSE563 students (Problems 1, 2, 3, and 4)

My phone number for any question you have is 314-537-4124.
Please text me and I will answer quickly.

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CSE463 students will work on Problems P1, P2 and P3

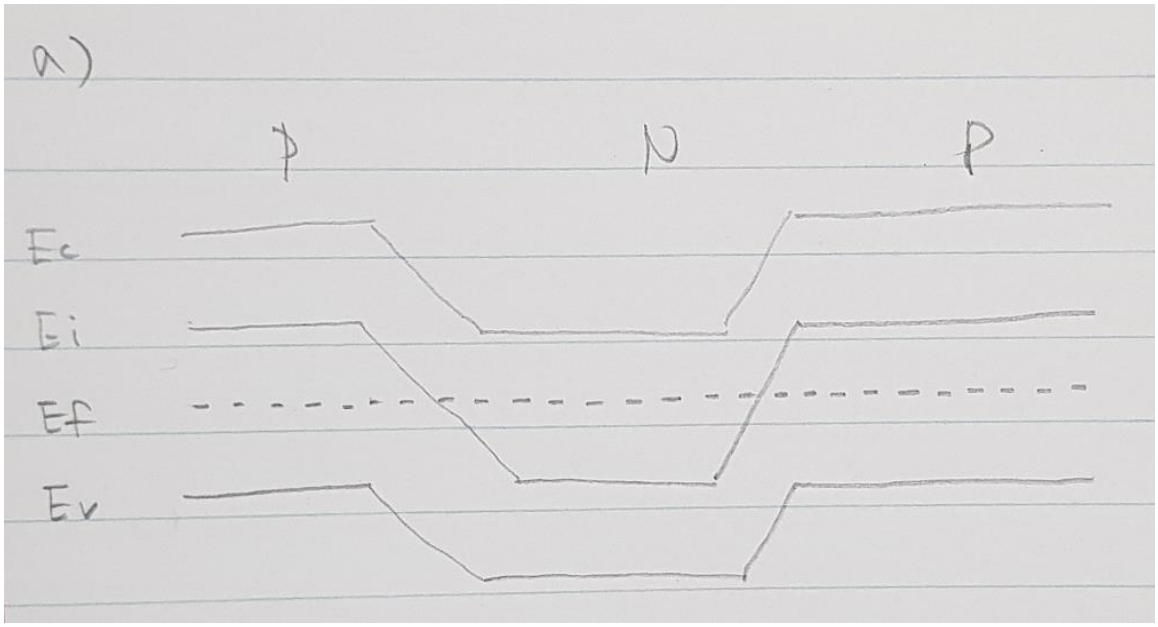
CSE563 students will work on Problems P1, P2, P3 and P4

P1. Three pieces of Si with acceptor concentration 10^{18} cm^{-3}, donor concentration 10^{15} cm^{-3} and acceptor concentration of 10^{18} cm^{-3}, respectively, are abutted. The sample temperature is T=300K (60 points)

(a) Draw the energy band diagrams before and after they are abutted. (10 points)
(b) Compute the built in potential for each junction. (20 points)
(c) Sketch and compute the depletion width for both junctions. (20 points)
(d) Draw the cross-section of an implementation of this device in 0.5um CMOS process. In CMOS process, you cannot simply join these three junctions with different doping. You will have to use p+ active, n+ active, n-well and p-substrate to formulate this device. (10 points)

+ My solution starts.

a)



b)

$$V_0 = \frac{kT}{q} \ln\left(\frac{N_A N_D}{{n_i}^2}\right)$$

$$\frac{kT}{q} = 0.026V$$

$$N_A = 10^{18}$$
$$N_D = 10^{15}$$
$$n_i = 1.45 \cdot 10^{10}$$

$$V_0 = 0.026 \cdot \ln\left(\frac{10^{18} \cdot 10^{15}}{(1.45 \cdot 10^{10})^2}\right)$$

$$\boxed{V_0 = 0.7589\ V}$$

c)

$$\varepsilon = 8.85 \cdot 10^{-14} \cdot 11.7 = 1.035 \cdot 10^{-12}$$
$$q = 1.6 \cdot 10^{-19} C$$

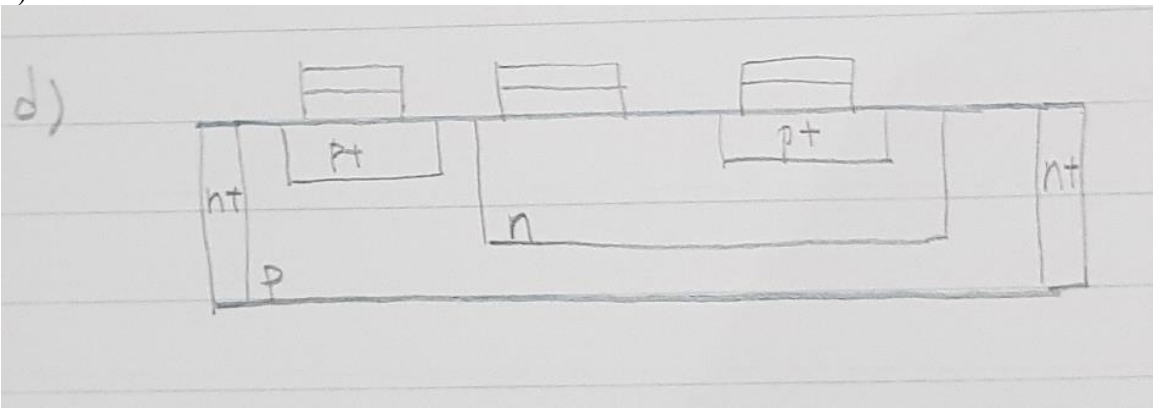
$$W = \sqrt{\frac{2\varepsilon V_0}{q}\left(\frac{N_A + N_D}{N_A \cdot N_D}\right)}$$

$$W = \sqrt{\frac{2 \cdot 1.035 \cdot 10^{-12} \cdot 0.7589}{1.6 \cdot 10^{-19}}\left(\frac{10^{18} + 10^{15}}{10^{18} \cdot 10^{15}}\right)}$$

$$W = 0.00009913$$

$$\boxed{W = 0.9913 \mu m}$$

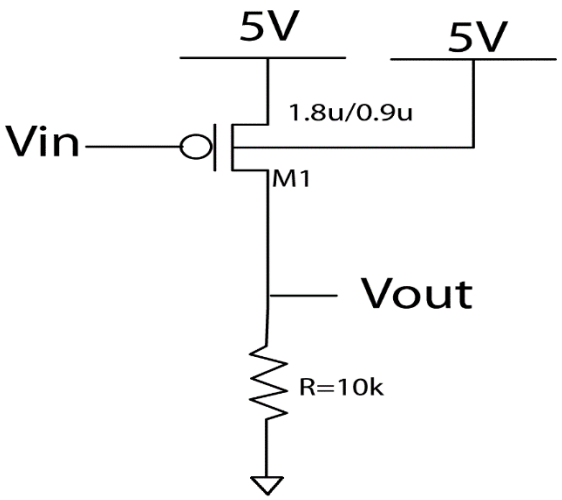
d)



+ My solution ends.

P2. Consider the inverter circuit in figure P2. Assume k_p' =10uA/V^2, |Vtop| = 1V and λ=0 V^{-1}. (60 pts)

(a) Compute V_{out} if Vin = 5V. Assume that γ=0 (10 pts)
(b) Compute V_{out} if Vin = 0V. Assume that γ=0 (10 pts)
(c) Compute the logic threshold of the inverter, i.e. compute V_{th}. Assume that γ=0 (10 pts)
(d) Draw the Vin vs. Vout curves for this circuit and clearly label V_{oh}, V_{ol} and V_{th}. (10 pts)
(e) How would you expect the value of V_{out} to change in (a) and (b) if γ=0.1? (10pts)
(f) Assume the circuit has a logic threshold of V_{th}. Specify *two circuit modifications* that will help you increase the logic threshold value V_{th}. (10pts)



P.2

+ My solution starts.

a)

$V_{in} = 5 - V_{out}$

$5 = 5 - V_{out}$

$V_{out} = 0$

b) $V_{in} = 5 - V_{out}$, $V_{in} = 0$

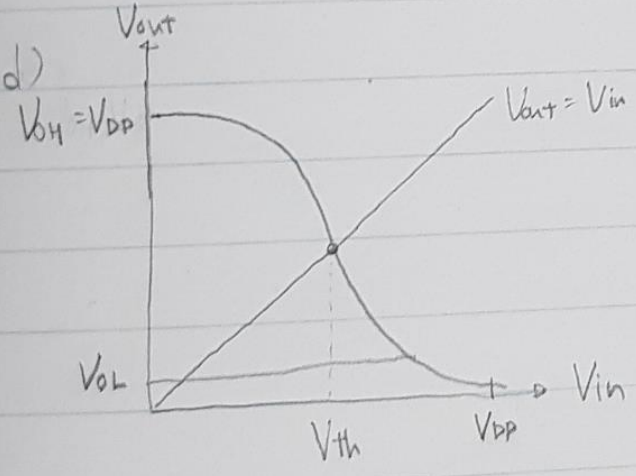
$V_{out} = 5\,V$

c) $V_{th} = V_{TO_p} + r\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$

since $r = 0$,

$V_{th} = V_{TO_p} = 1V$

d)



e) When r grows, Vout would increase ... (a)

When r grows, Vout would decrease ... (b)

f) increase the size of pMOS

decrease the size of resistor

+ My solution ends.

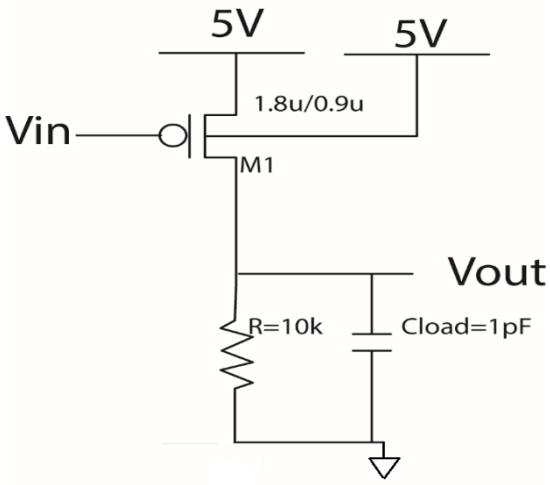
P3. Consider the following circuit. The load capacitance at the output node is C_{load}=1pF. Use voltage values from P2 in this problem. (80 pts)

(a) Derive a close form solution for the propagation delay high to low, i.e. τ_{PHL}. (20 pts)

(b) Solve the integrals for propagation delay high to low and compute the propagation delay τ_{PHL}. Note: $\int 1/x\, dx = \ln(x)$ (20 pts).

(c) Derive a close form solution for the propagation delay low to high, i.e. τ_{PLH}. (20 pts)

(d) Compute the propagation delay τ_{PLH}. Again note: $\int 1/x\, dx = \ln(x)$ (20 pts).



P.3

+ My solution starts.

a) $i_C = C_{load}\frac{dV_{out}}{dt} = i_{D,p} - i_{D,n}$

When H → L, pMos is switched off thus,

$i_{D,p} = 0$.

$$C_{load}\frac{dV_{out}}{dt} = -i_{D,n}$$

$$dt = -\frac{C_{load}}{i_{D,n}}dV_{out}$$

$$\int_{t_0}^{t_1} dt = \int_{V_{OH}}^{V_{50\%}} -C_{load}\cdot\frac{1}{i_{D,n}}dV_{out}$$

$$= \int_{V_{OH}}^{V_{50\%}} -C_{load}\cdot R\cdot\frac{1}{V_{out}}dV_{out}$$

b) $$\int_5^{2.5} -C_{load}\cdot R\cdot\frac{1}{V_{out}}dV_{out}$$

$$= -C_{load}\cdot R\cdot\int_5^{2.5}\frac{1}{V_{out}}dV_{out}$$

$$= -1\cdot10^{-12}\cdot 10000\cdot(\ln(2.5)-\ln(5))$$

$$= 6.9314\cdot10^{-9}$$

$$= 6.9314\ ns$$

c) $i_C = C_{load}\frac{dV_{out}}{dt} = i_{D,p} - i_{D,n}$

$$dt = \frac{C_{load}}{i_{D,p} - i_{D,n}} dV_{out}$$

$$\int dt = C_{load} \int \frac{1}{i_{D,p} - i_{D,n}} dV_{out}$$

$$= C_{load} \int \left(-\frac{V_{out}}{R} + i_{D,p}\right)^{-1} dV_{out}$$

- since pMOS is sat.

$$i_{D,p} = \frac{K'_n}{2}\left(\frac{W}{L}\right)_n \left[2(V_{GSn} - V_{TOn})V_{DSn} - V_{DSn}^2\right]$$

$$= \frac{10\cdot 10^{-6}}{2}\cdot\frac{1.8}{0.9}\left[2(0-1)5 - 5^2\right]$$

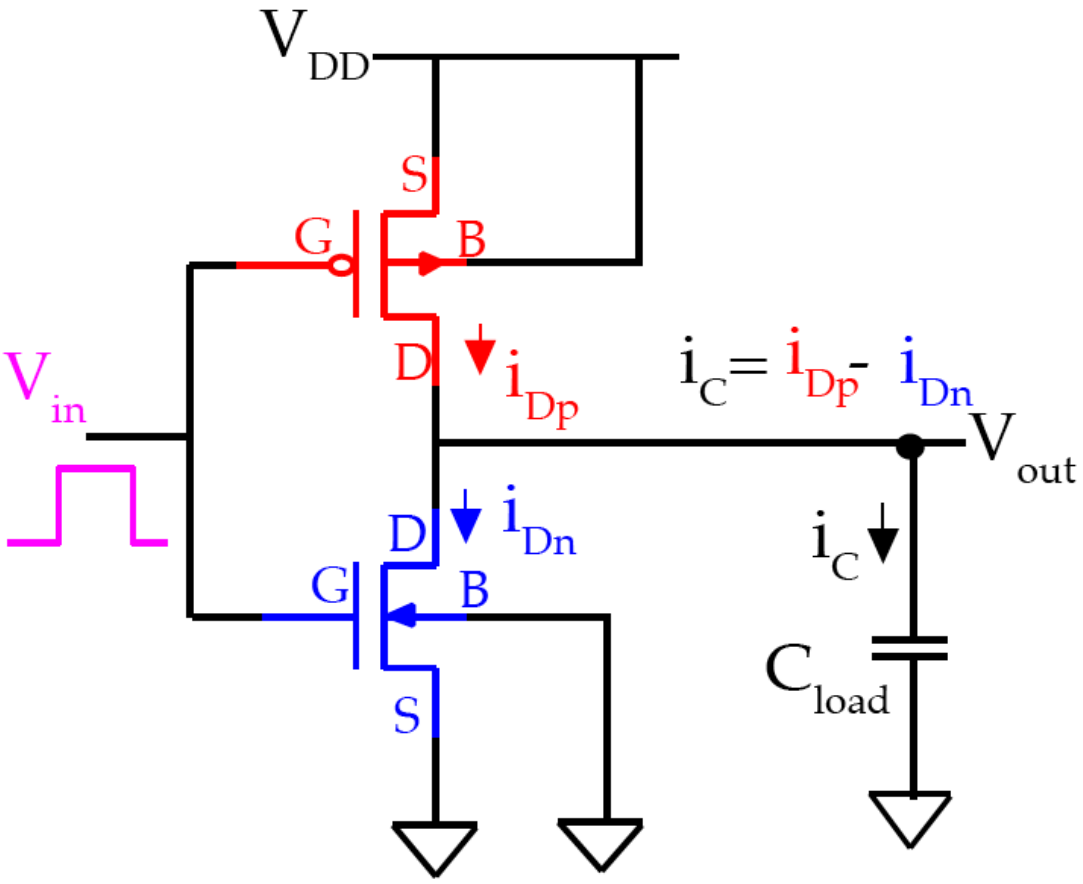
$$= 10\cdot 10^{-6}\cdot(-35)$$

$$\int dt = -1\cdot 10^{-12}\int \left(-\frac{V_{out}}{10000} + 10\cdot 10^{-6}(-35)\right)^{-1} dV_{out}$$

d)

+ My solution ends.

P4. Consider the following inverter circuit: (70 pts)



P.4

Transistors parameters are defined as

for nMOS transistor:

$V_{T0n} = 0.5V$; $\mu_n C_{ox} = 98\ \mu A/V^2$; Ln = 40nm;

for pMOS transistor:

$V_{T0p} = -0.48V$; $\mu_p C_{ox} = 46\ \mu A/V^2$; Ln = 40nm;

This inverter is designed for $V_{TH} = 0.68V$. Also $V_{DD} = 1.2V$

(a) (30pts)

A simplified expression of the total output load capacitance is given as:

$C_{load} = 5fF + Cdb,n + Cdb,p.$

The drain-substrate parasitic capacitance of the nMOS and pMOS transistors are the functions of the channel width that are defined with a set of simplified capacitance expressions:

Cdb,n = 0.16fF + (1.7Wn)fF

Cdb,p = 0.13fF + (1.4Wp)fF

where Wn and Wp are expressed in μm.

Determine the channel width Wn and Wp of both transistors such that the propagation delay HIGH-to-LOW is defined as:

$\tau_{PHL} \leq 35ps$.

+ My solution starts.

$$V_{th} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}}(V_{DD} - |V_{T0,p}|)}{1 + \sqrt{\frac{1}{k_R}}}$$

$$0.68 = \frac{0.5 + \sqrt{\frac{1}{k_R}}(1.2 - 0.48)}{1 + \sqrt{\frac{1}{k_R}}}$$

$$k_R = 0.049$$

$$k_R = \frac{k_n}{k_p} = \frac{k'_n(\frac{W}{L})_n}{k'_p(\frac{W}{L})_p} = \frac{98(\frac{W}{L})_n}{46(\frac{W}{L})_p}$$

$$0.049 = \frac{98(\frac{W}{L})_n}{46(\frac{W}{L})_p}$$

$$(\frac{W}{L})_p = 42.953(\frac{W}{L})_n$$

+ Since Ln and Lp is the same, we can get equation below.

$\boxed{W_p = 43.478W_n}$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PHL} = \frac{C_{load}}{\mu_n C_{ox}(V_{DD} - V_{T0n})}\left(\frac{L_n}{W_n}\right)\left[\frac{2V_{T0n}}{V_{DD} - V_{T0n}} + \ln\left(\frac{4(V_{DD} - V_{T0n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PHL} = \frac{C_{load}}{98 \cdot 10^{-6} \cdot (1.2 - 0.5)}\left(\frac{L_n}{W_n}\right)\left[\frac{2 \cdot 0.5}{1.2 - 0.5} + \ln\left(\frac{4(1.2 - 0.5)}{1.2} - 1\right)\right]$$

$$\tau_{PHL} = \frac{C_{load}}{98 \cdot 10^{-6} \cdot (1.2 - 0.5)}\left(\frac{40 \cdot 10^{-9}}{W_n}\right) \cdot 1.716$$

$$C_{load} = 5fF + 0.16fF + 1.7W_n fF + 0.13fF + 1.4W_p fF$$
$$C_{load} = (5.29 + 1.7W_n + 1.4W_p)fF$$
$$C_{load} = (5.29 + 1.7W_n + 1.4W_p) \cdot 10^{-15}$$

$$\tau_{PHL} = \frac{(5.29 + 1.7W_n + 1.4W_p) \cdot 10^{-15}}{98 \cdot 10^{-6} \cdot (1.2 - 0.5)}\left(\frac{40 \cdot 10^{-9}}{W_n}\right) \cdot 1.716$$

+ Since, $W_p = 43.478W_n$ and $\tau_{PHL} \leq 35ps$.

$$35 \cdot 10^{-12} \geq \frac{(5.29 + 1.7W_n + 1.4 \cdot 43.478W_n) \cdot 10^{-15}}{98 \cdot 10^{-6} \cdot (1.2 - 0.5)}\left(\frac{40 \cdot 10^{-9}}{W_n}\right) \cdot 1.716$$

$$W_n = 1.512 \cdot 10^{-7}$$
$$W_n = 0.1512 \cdot 10^{-6}$$
$$W_n = 0.1512\ \mu m$$

+ Since, $W_p = 43.478W_n$
$$W_p = 43.478W_n$$

$$W_p = 43.478 \cdot 0.1512\ \mu m$$
$$W_p = 6.573\ \mu m$$

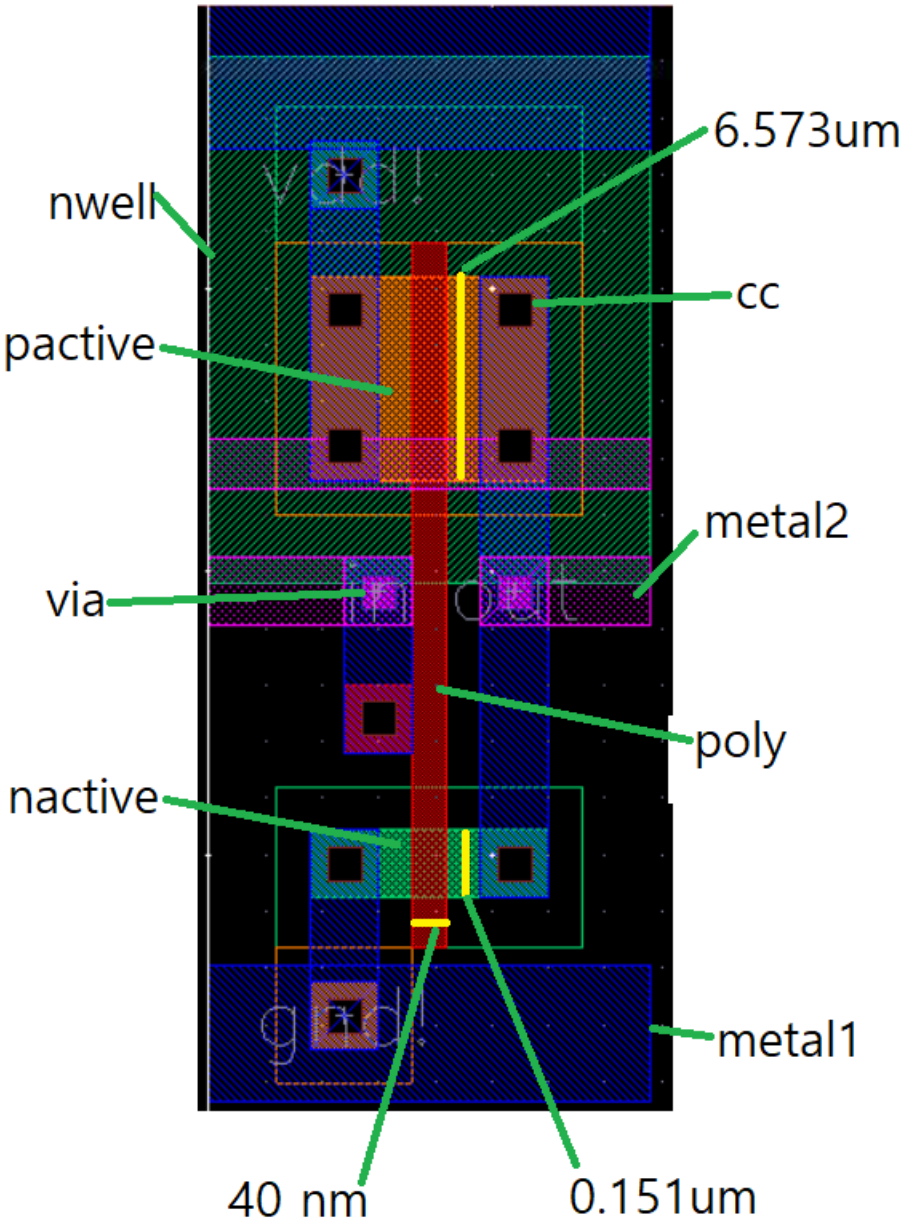
$\boxed{W_p = 6.573\ \mu m}$
$\boxed{W_n = 0.1512\ \mu m}$

+ My solution ends.

(b) (20pts)

Sketch layout of the inverter from part (a). Include bulk for both transistors. Mark Wn, Ln, Wp and Lp on the sketch of the layout. Specify all regions (n+ active, p+ active, nwell, metal1, metal2, via, contact, and polysilicon). Mark V_{DD}, GND, Vin and Vout on the sketch of the layout.

+ My solution starts.



+ My solution ends.

(c) (20pts)

Assume now that the CMOS inverter shown in figure P.4 has been designed with $(W/L)_n = 10$ and $(W/L)_p = 15$ and that the total output load capacitance is 5fF. Calculate the output rise time τ_{rise} and fall time τ_{fall} using proper equations from the lectures.

+ My solution starts.

$$\tau_{rise} = \frac{C_{load}}{\mu_p C_{ox} \frac{W_p}{L_p}(V_{DD} - |V_{T0p}|)}\left[\frac{2(|V_{T0p}| - 0.1V_{DD})}{V_{DD} - |V_{T0p}|} + \ln\left(\frac{2(V_{DD} - |V_{T0p}|)}{0.1V_{DD}} - 1\right)\right]$$

$$\tau_{rise} = \frac{5 \cdot 10^{-15}}{46 \cdot 10^{-6} \cdot 15 \cdot (1.2 - 0.48)}\left[\frac{2(0.48 - 0.1 \cdot 1.2)}{1.2 - 0.48} + \ln\left(\frac{2(1.2 - 0.48)}{0.1 \cdot 1.2} - 1\right)\right]$$

$$\tau_{rise} = 3.419 \cdot 10^{-11}$$

$$\boxed{\tau_{rise} = 34.19\, ps}$$

$$\tau_{fall} = \frac{C_{load}}{\mu_n C_{ox} \frac{W_n}{L_n}(V_{DD} - V_{T0n})}\left[\frac{2(V_{T0n} - 0.1V_{DD})}{V_{DD} - V_{T0n}} + \ln\left(\frac{2(V_{DD} - V_{T0n})}{0.1V_{DD}} - 1\right)\right]$$

$$\tau_{fall} = \frac{5 \cdot 10^{-15}}{98 \cdot 10^{-6} \cdot 10 \cdot (1.2 - 0.5)}\left[\frac{2(0.5 - 0.1 \cdot 1.2)}{1.2 - 0.5} + \ln\left(\frac{2(1.2 - 0.5)}{0.1 \cdot 1.2} - 1\right)\right]$$

$$\tau_{fall} = 2.516 \cdot 10^{-11}$$

$$\boxed{\tau_{fall} = 25.16\, ps}$$

+ My solution ends.