CSE463/563: Digital Integrated Circuits Design and Architecture

Instructor: Dr. Darko Ivanovich
Email: darkoivanovich@msn.com
Class Time: TuTh, 5:30 - 7.00PM, Crow Hall 205
Office Hours: Tuesday and Thursday, 7:00PM -

Course Description:

This course is an introduction to VLSI digital design. The material will focus on bottom up design of digital integrated circuits, starting from CMOS transistor properties and manufacturing technology to CMOS inverters, combinational and sequential logic designs and more complex digital blocks. Important design aspect of digital integrated circuits such as propagation delay, noise margins and power dissipation will be covered in the class, as well as design challenges in submicron technology will be addressed. The students will design combinational and sequential circuits at various levels of abstraction using state-of-the-art CAD environment provided by Cadence Design Systems. The goal of the class is to design transistor level digital integrated circuits in 0.5micron technology that can be fabricated by a semiconductor foundry.

Course Objectives:

The course will start with an overview of the intrinsic properties of CMOS transistors and an overview of fabrication methodologies for integrated circuits. Combinational circuits will be introduced with the design of the inverter circuit. The static and dynamic properties of the inverter will be studies in detail using hand calculations and SPICE simulations. The state-of-the-art tool for designing ICs, Cadence, will be introduced and will be used to design and verify the physical layout of the inverter. Using parameters extracted from Cadence layout simulations, a Verilog model will be constructed. Other CMOS combinational and sequential digital circuits, such as NAND, NOR, SR latch, flip flop and others, will be constructed and simulated at transistor, layout and behavioral level using Cadence. The final project will include a design of a complex digital system. The entire digital IC will be simulated and the final layout of the chip will be presented. The layout of the chip can be submitted for fabrication in a 0.5micron CMOS process.

Prerequisites:

ESE 232: *Introduction to Electronic Circuits*
CSE 362M: *Computer Architecture* (recommended)

Textbook:

- *CMOS Digital Integrated Circuits Analysis and Design*, 4th Edition S. M. Kang, Y. Leblebici and C. Kim, 2015.
- Online Cadence Tutorial

Other References:

- *Verilog HDL: A guide to digital design and synthesis*, S. Palnikar, 1996.
- *Basic VLSI Design*, D. Pucknell and K. Eshraghian 1988.
- *Fundamentals of CMOS VLSI Design*, J. Uyemura, 1988
- *Analysis and Design of Analog integrated Circuits*, P. Gray and R. Meyer, 1994

Course Grading:

Weekly Homework: 30%
Exam1: 20%
Exam2: 20%
Project: 30%

Grading Policy:

88% or above A
78% to 88% B
66% to 78% C
50% to 66% D
50% or below F

Spring 2023 Syllabus

Week	Topics	Chapter
Week 1 – Jan 15 thru Jan 21 (First day of class is January 17th)	Course Introduction, Fabrication of MOSFETs, MOS Transistor Theory	1, 2, 3
Week 2 – Jan 22 thru Jan 28	MOS Transistor Theory	3
Week 3 – Jan 29 thru Feb 4	MOS Transistor Theory Intro to Cadence Design	3
Week 4 – Feb 5 thru Feb 11	Inverter: Static Characteristics	5
Week 5 – Feb 12 thru Feb 18	Inverter: Static Characteristics Introduction to Cadence Layout	5
Week 6 – Feb 19 thru Feb 25	Inverter: Switching Characteristics	6
Week 7 – Feb 26 thru Mar 4	Inverter: Switching Characteristics	6
Week 8 – Mar 5 thru Mar 11	Combinational Logic Circuits	7
Week 9 – Mar 12 thru Mar 18	Spring Break	
Week 10 – Mar 19 thru Mar 25	Combinational Logic Circuits	7
Week 11 – Mar 26 thru Apr 1	Sequential Logic Circuits	8
Week 12 – Apr 2 thru Apr 8	Sequential Logic Circuits and Final Project	8
Week 13 – Apr 9 thru Apr 15	Semiconductor Memories and Final Project	10
Week 14 – Apr 16 thru Apr 22	Final Project Part 1	
Week 15 – Apr 23 thru Apr 29	Final Project Part 2	
Week 16 – Apr 30 thru May 6	Final Project Part 3	
Week 17 – May 12th	Final Project Deadline	