

McKelvey School of Engineering

Spring Semester 2023

CSE463M: Digital Integrated Circuit Design and Architecture

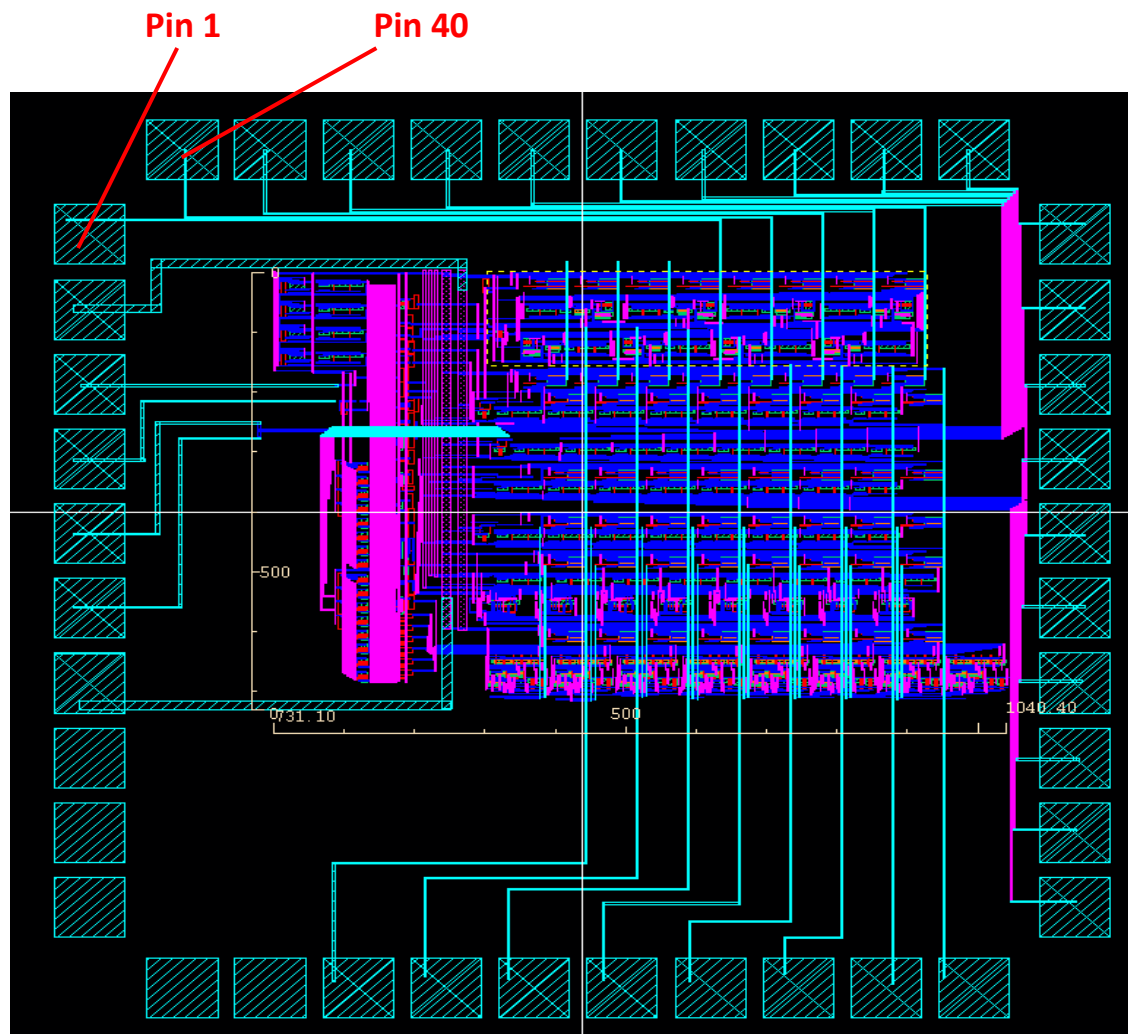
Final Project: Simplified DES CMOS chip design specifications

For all CSE463 and CSE563 students:

Your team needs to design a CMOS chip that will perform simplified DES in hardware on 8-bit Input = 11101100 using 10-bit Input key $k = 1100010110$.

Your chip will need to satisfy the following requirements:

1. Your CMOS chip will have 40 external pins as shown in the example below:



Therefore your design will have CMOS layout as it is shown in the previous figure. Your chip external pins should be used as this:

Pins 1 thru 8 – should be used for the 8-bit Input Sequence
(in your case this is Input = 01001010).

Pin 9 – should be V_{DD} which is 3.3V for this design.

Pin 10 – should be GND.

Pins 11 thru 20 – should be used for the 10-bit Input key k
(in your case this is k = 1110111001).

Pin 21 – should be input CLOCK which is 10MHz for this design.

Pin 22 – should be ENABLE input for this design.

When ENABLE is binary 0 then the chip 8-bit Output sequence = 00000000, and when ENABLE is binary 1 then the chip 8-bit Output sequence should be equal to a Simplified DES algorithm encrypted 8-bit value triggered by the chip CLOCK input. The Output sequence should stay equal to the Simplified DES algorithm encrypted 8-bit value as long as ENABLE = 1.

Pins 23 thru 26 – should be VDD.

Pins 27 thru 30 – should be GND.

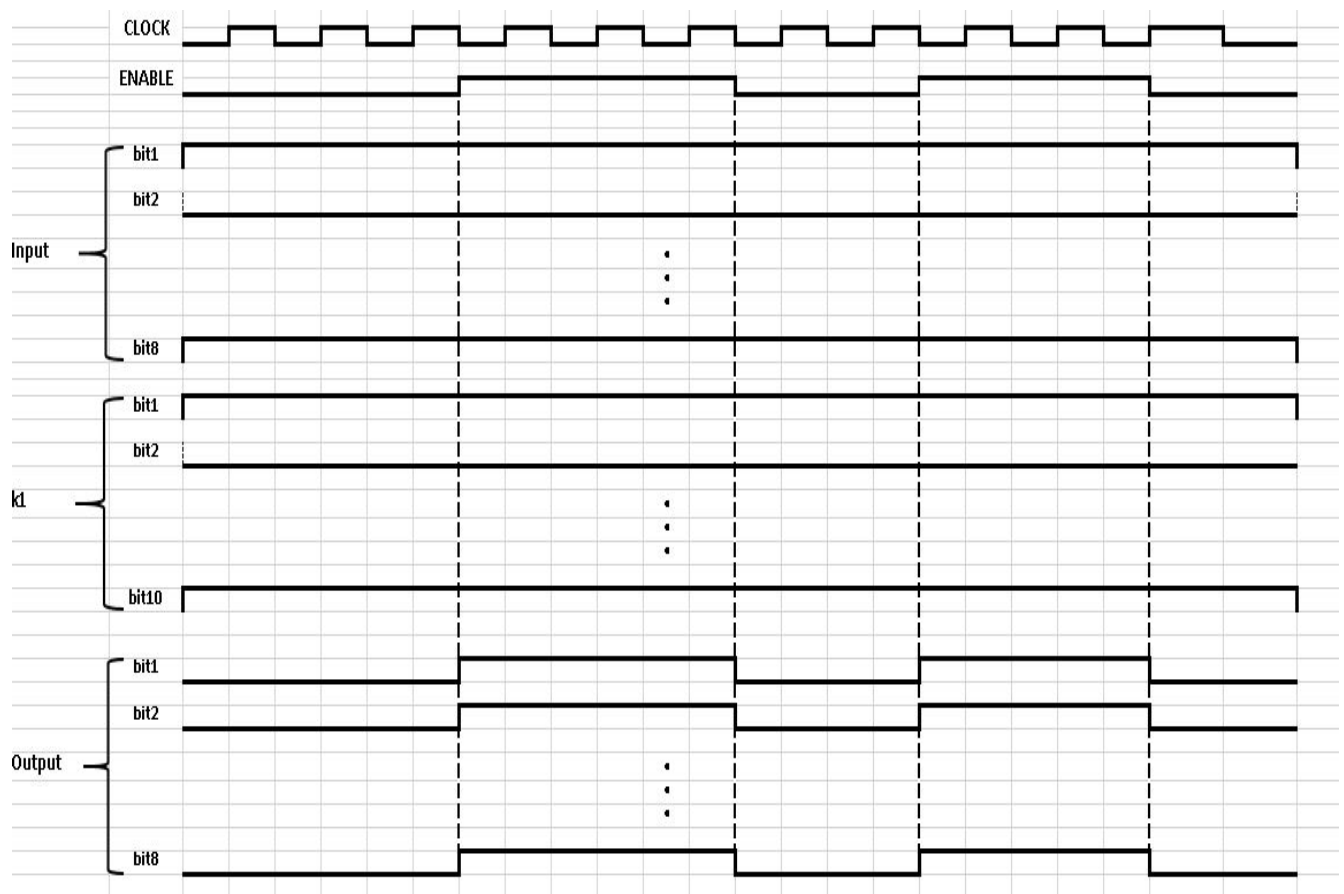
Pins 31 thru 38 – should be used for 8-bit Output Sequence.

Pin 39 – should be VDD.

Pin 40 – should be GND.

2. Your chip layout has to fit within 1.5mm by 1.5mm of silicon area. You can see in the previous figure what layout area is used for that example with the ruler included in the figure.
3. 8-bit input sequence, 10-bit input key k, ENABLE input, CLOCK input and 8-bit output sequence need to go thru buffer (two serially connected inverters) when they enter the chip layout or before they exit the chip layout. Also ENABLE input should control 8-bit input sequence and 10-bit input key k and allow (ENABLE = 1) or do not allow (ENABLE = 0) entering the buffers for the 8-bit input sequence and 10-bit input key k.

4. For Simplified DES algorithm key generation k_1 and k_2 you don't need to do anything special other than make sure that all your signals are valid square wave pulses and correct values. This part of design has lots of binary bits permutations and circular shifting of lower 5-bits and higher 5-bits.
5. Functions f_{k1} and f_{k2} are parts of the chip design where you will have to use one-bit XOR functions, various binary bits permutations and then two SBoxes will have to be designed as well.
6. The SBox_1 and SBox_2 designs should have 16 4-bit D flip-flop registers that use CLOCK input. Each 4-bit register represents one $b_1b_2b_3b_4$ combination out of 16 possible SBox combinations. Based on each of these 16 registers 4-bit outputs and your calculated 4-bit values $E/P(R) \text{ xor } k_1$ and $E/P(R) \text{ xor } k_2$ you will obtain proper two-bit value as output of this part of design. This is the most complex part of the design.
7. Your timing diagram in simulation for both schematic and layout should look like this:



You will work in a team of two students. Below are the target dates for each part of the design. For each completed task, submit a written report with the appropriate simulations, layouts and LVS/DRC reports. At the end these parts will be your final report.

For CSE563 students only:

Investigate how fast CLOCK signal can be utilized in your chip design and report this analysis

The project will be graded out of 100 points. You will receive points for each milestone as specified below.

Part 1: Due Friday (April 21, 2023)

Present an overview of your chip architecture. This should include a block diagram of your architecture, including all enable logic, buffers, combinational logic and registers. Present the timing sequence that includes all input and output signals. (10 points)

Part 2: Due Friday (April 28, 2023)

Present your Schematic Design of the entire chip and simulation that matches timing diagram from the part 7. (20 points)

Part 3: Due Friday (May 5, 2023)

Present layout of the entire chip and indicate successful DRC/LVS execution and simulation that matches timing diagram from the part 7. Try to optimize your layout area and present measurements of the area (use Shift-K to add a ruler for measurement). (20 points)

Part 4: Final Report due Friday (May 12, 2023):

Submit a final report describing your architecture and details of your circuits. In the final report, you are to outline your design, show simulation results, predict operation specifications, indicate what, if anything, is required to complete the design. (50 points)

Example of the Final Project Report is shown here:

Example of Final Project – Fall 2009

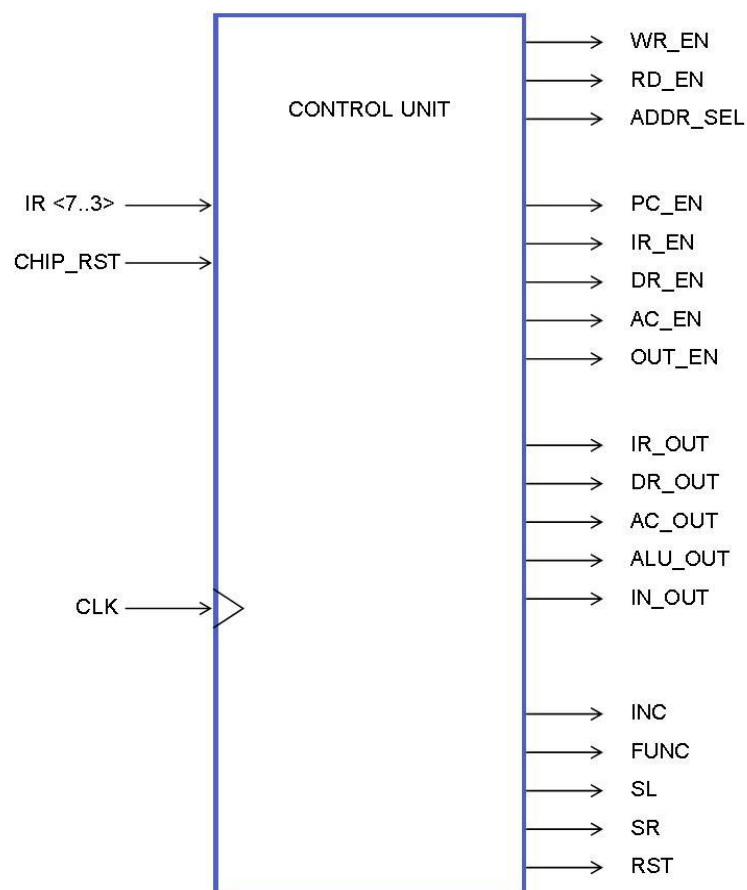
Toyland uProcessor

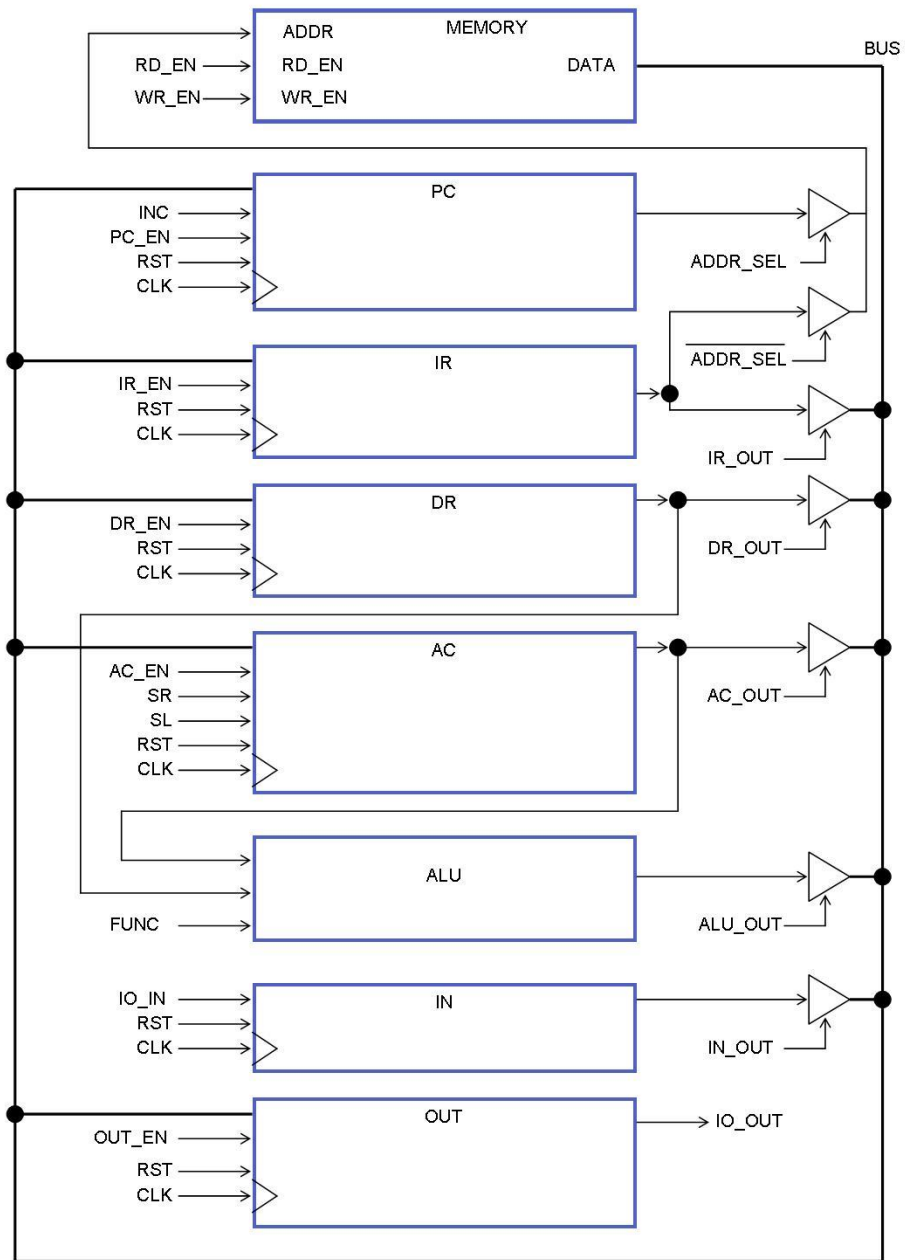
Stu Mesnier

Subharthi Paul

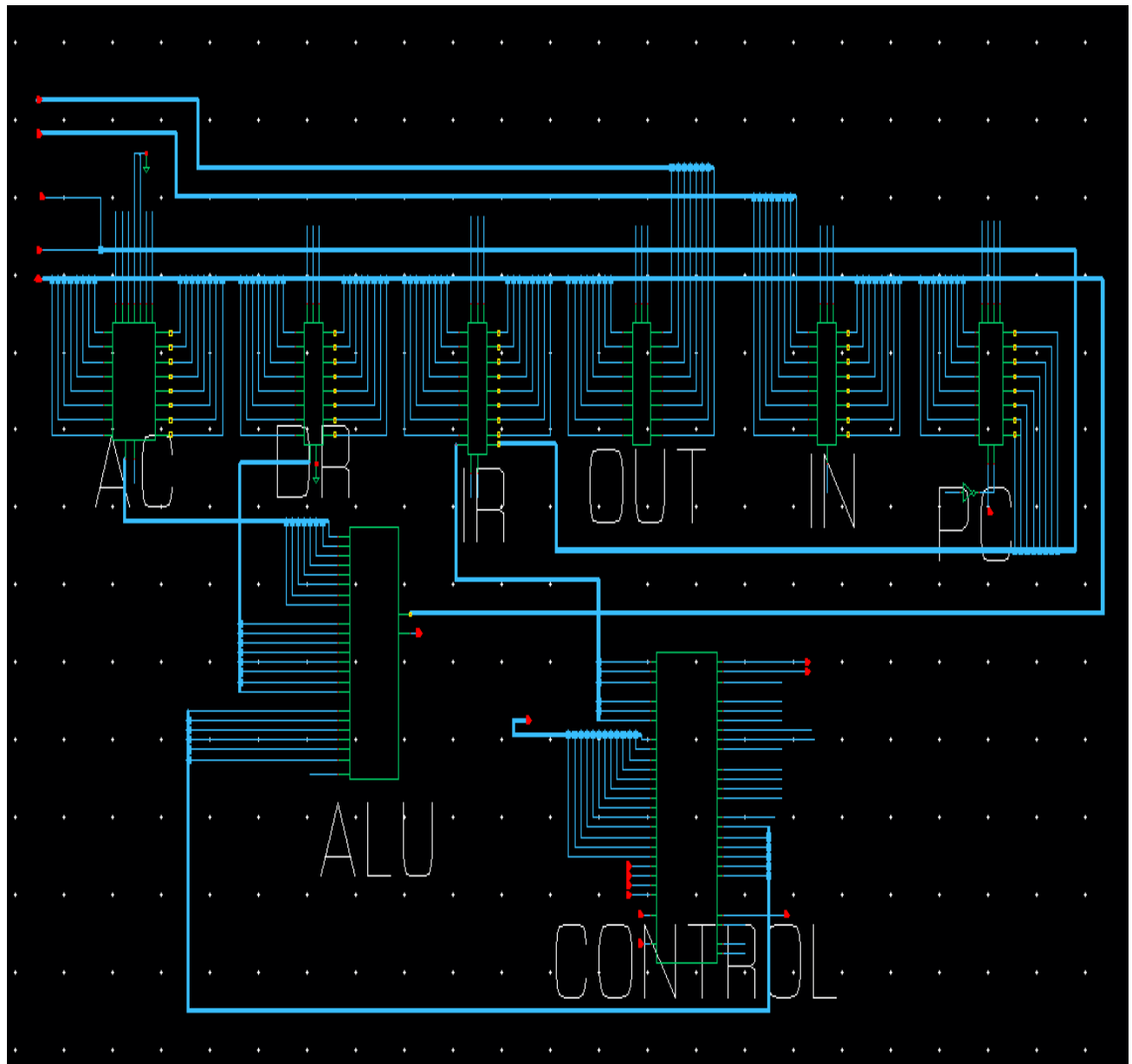
Will Steelman

Block Diagram:

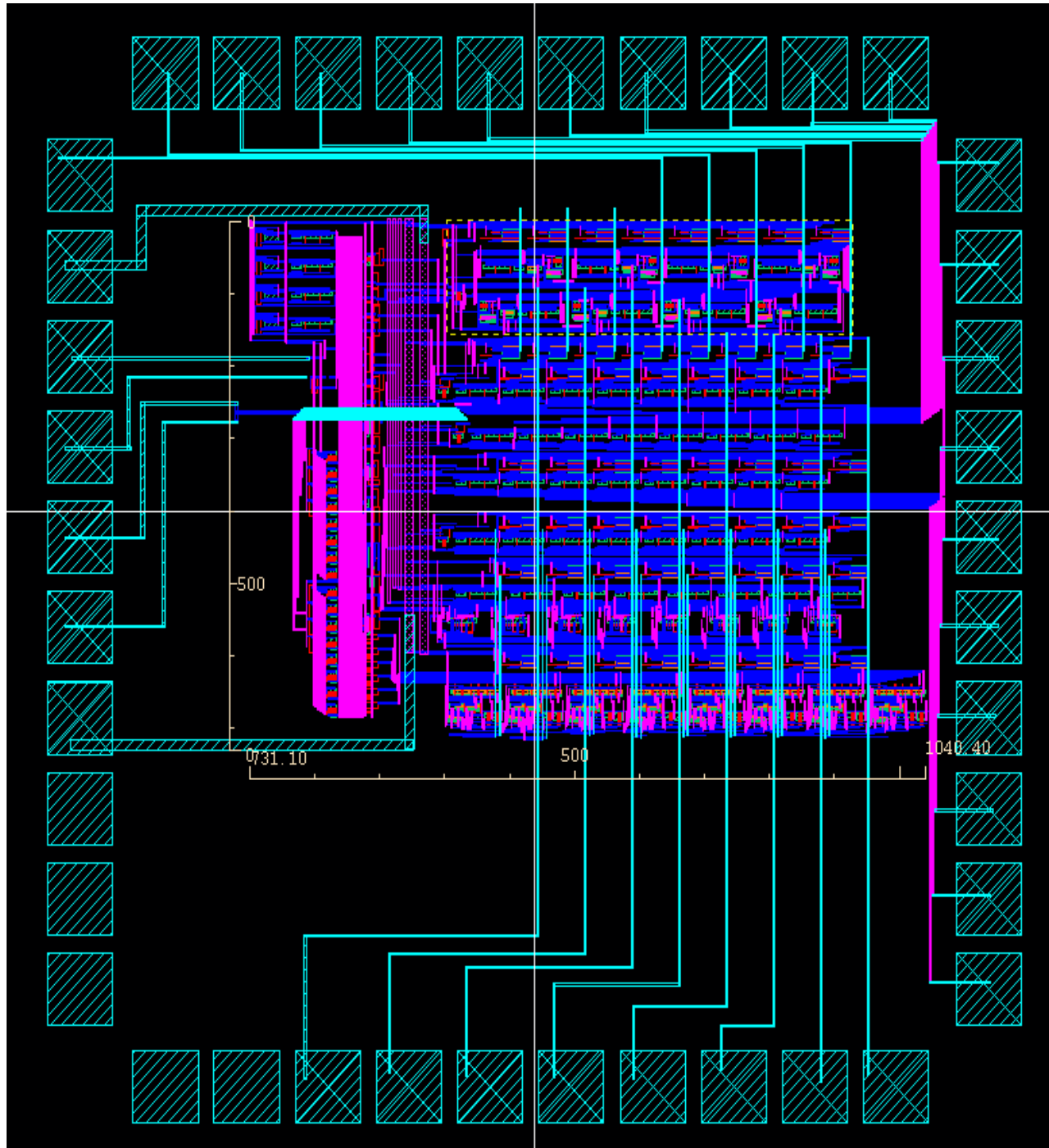




Chip Schematic:



Chip Layout:



Chip Simulation (similar to the Timing Diagram from the part 7):

