Washington University in St. Louis

McKelvey School of Engineering

Spring Semester 2023

CSE463M: Digital Integrated Circuit Design and Architecture

Final Assign #2 - Schematic

Sterling Lech

Byeongchan Gwak

* There are many parts to complete the Simplified DES.
* Below is the list of all parts.

 # For basic operation
INVERTOR
NAND
XOR
XOR4

 # For bit control
P10
P8
P4
SHIFT 1
SHIFT 3
EP
SWITCH
IP
IP Invert

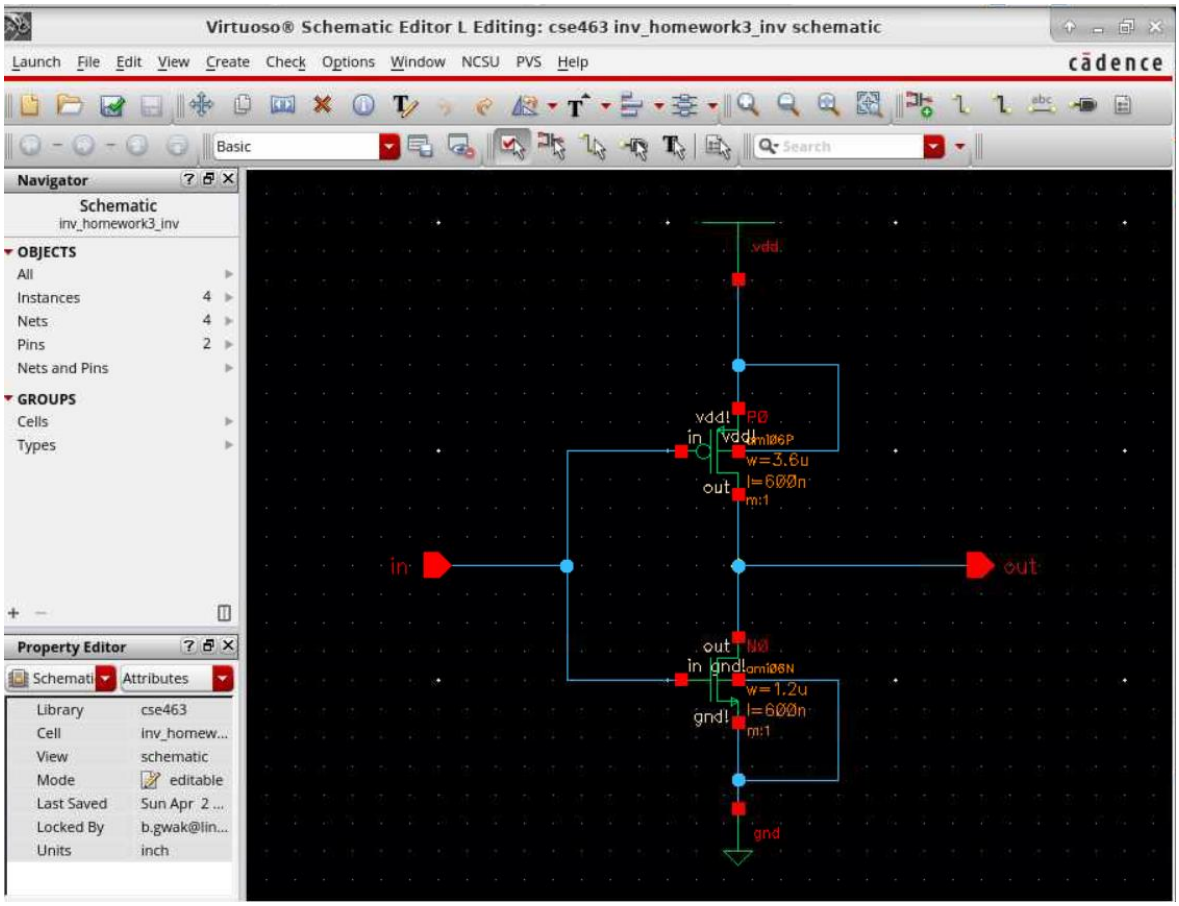
 # For selection
2:1 mux
16:1 mux

 # For Enable
ENABLE

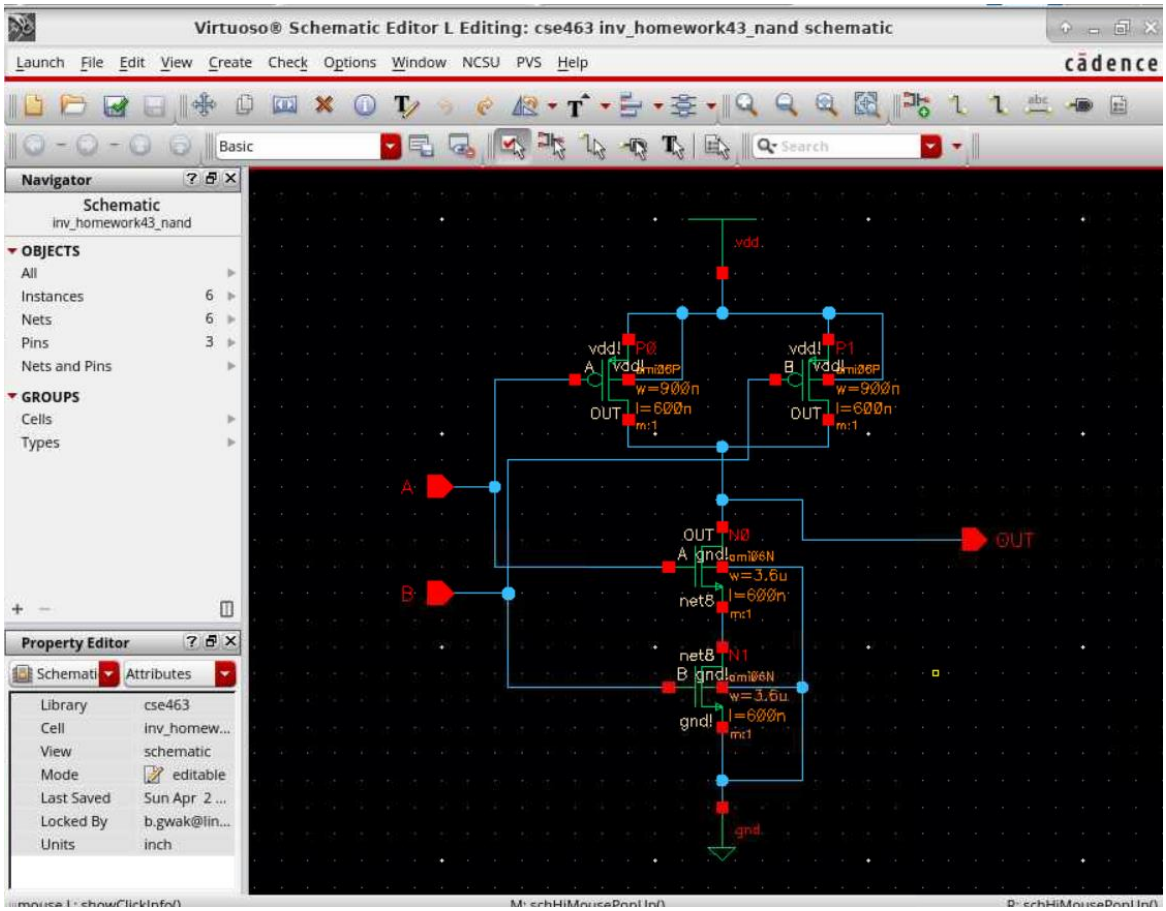
 # For CLK
D-LATCH
D Flip flop

 # For SBox
SBox Red
SBox Green

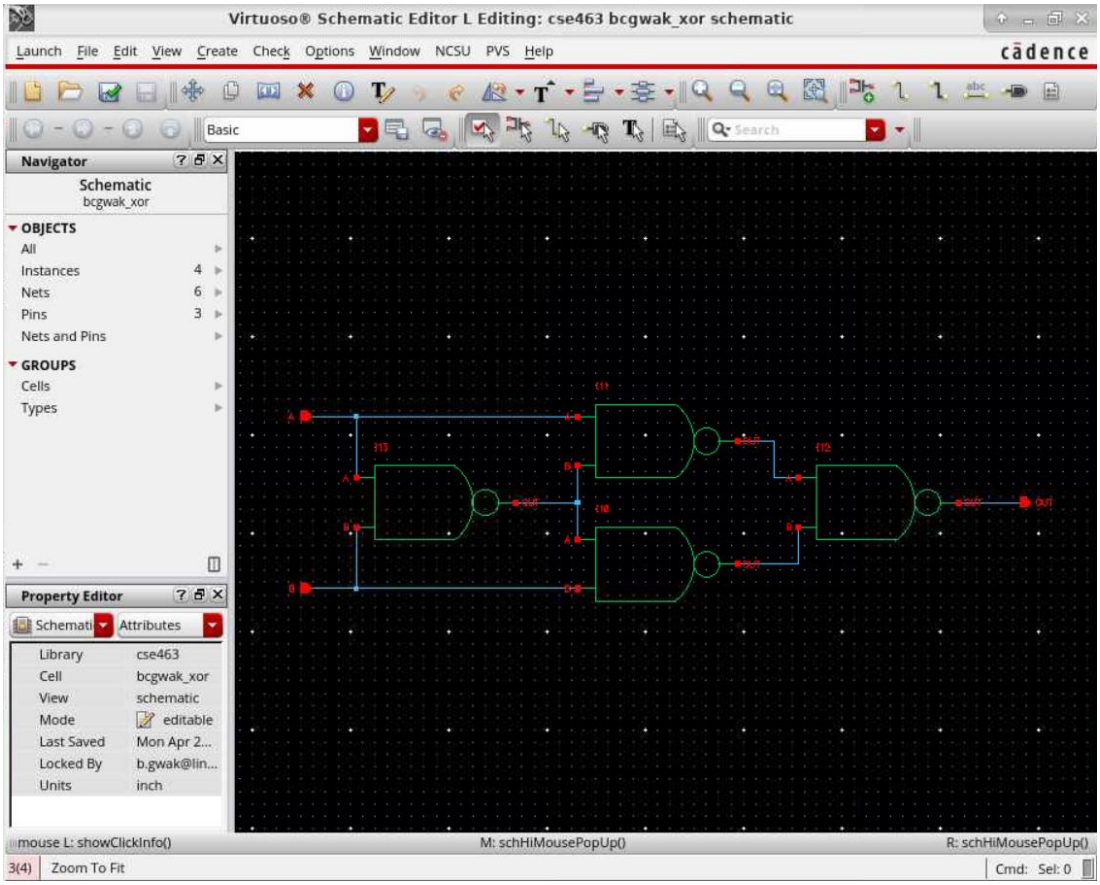
* INVERTOR



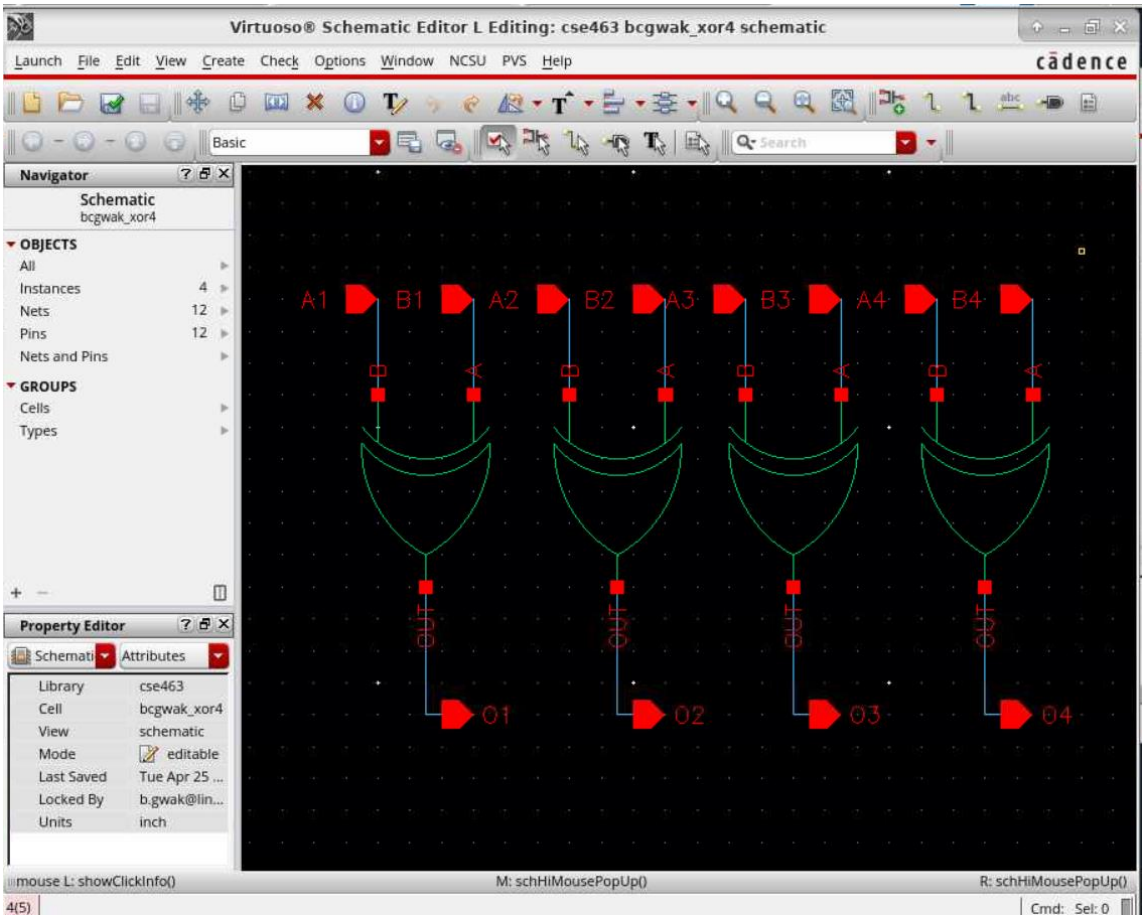
* NAND



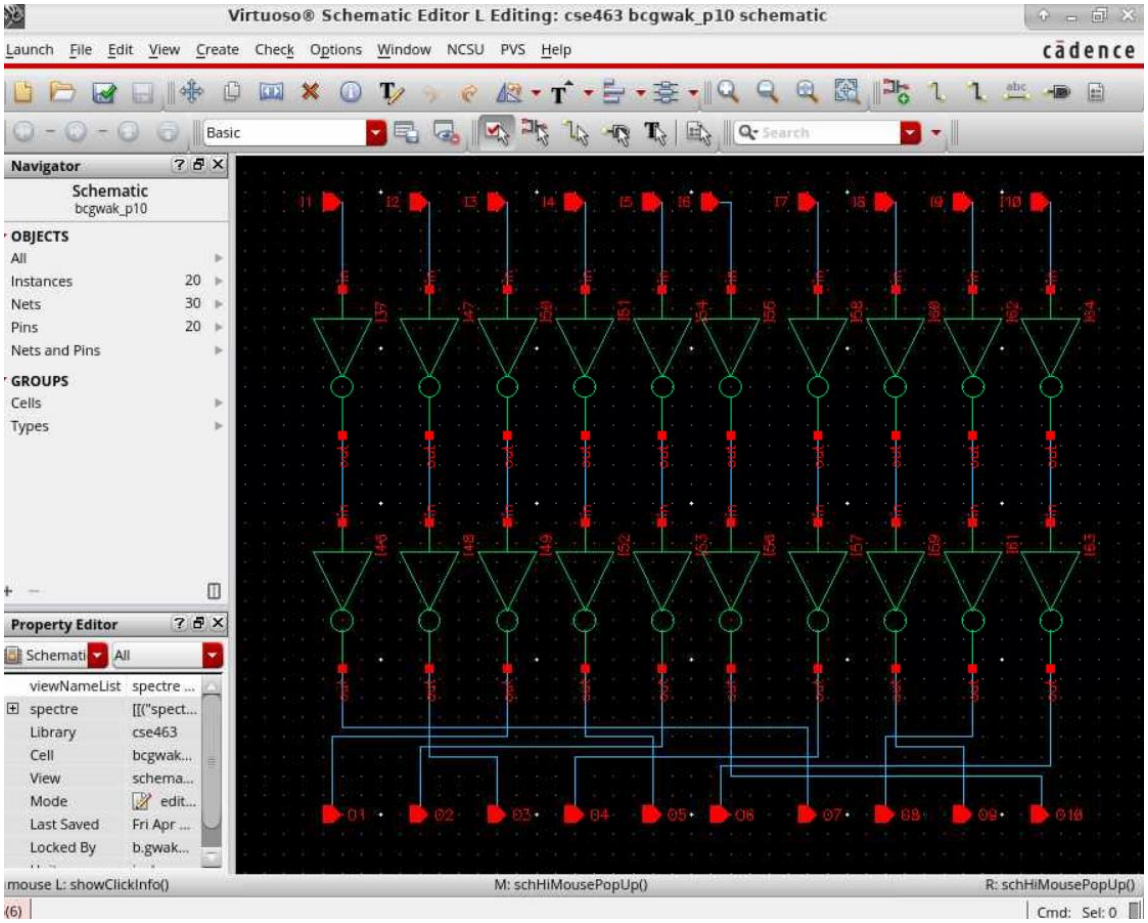
* XOR


Virtuoso® Schematic Editor L Editing: cse463 bcgwak_xor schematic
Launch File Edit View Create Check Options Window NCSU PVS Help
cadence
Navigator
Schematic
bcgwak_xor
OBJECTS
All
Instances 4
Nets 6
Pins 3
Nets and Pins
GROUPS
Cells
Types
Property Editor
Schemati Attributes
Library cse463
Cell bcgwak_xor
View schematic
Mode editable
Last Saved Mon Apr 2...
Locked By b.gwak@lin...
Units inch
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()
3(4)
Zoom To Fit
Cmd: Sel: 0

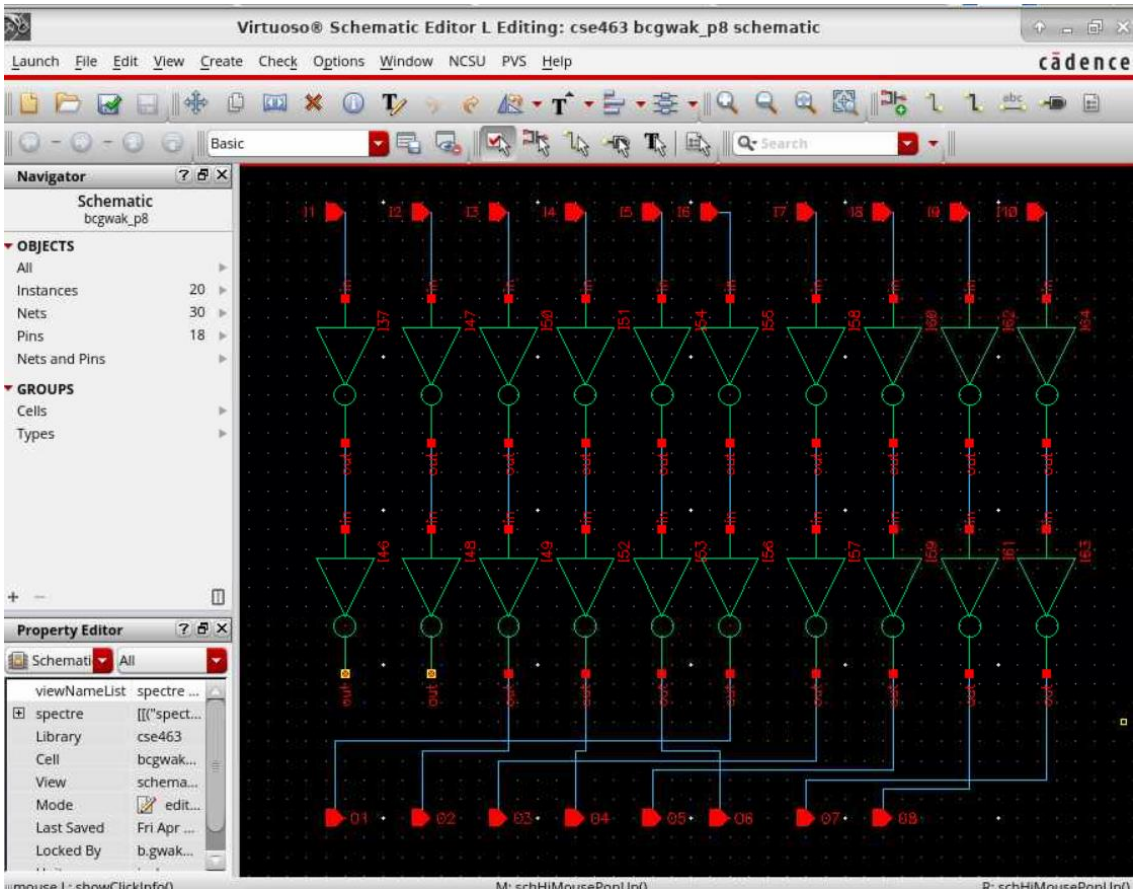
* XOR4


Virtuoso® Schematic Editor L Editing: cse463 bcgwak_xor4 schematic
Launch File Edit View Create Check Options Window NCSU PVS Help
cadence
Navigator
Schematic
bcgwak_xor4
OBJECTS
All
Instances 4
Nets 12
Pins 12
Nets and Pins
GROUPS
Cells
Types
Property Editor
Schemati Attributes
Library cse463
Cell bcgwak_xor4
View schematic
Mode editable
Last Saved Tue Apr 25 ...
Locked By b.gwak@lin...
Units inch
A1 B1 A2 B2 A3 B3 A4 B4
OUT
O1 O2 O3 O4
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()
4(5)
Cmd: Sel: 0

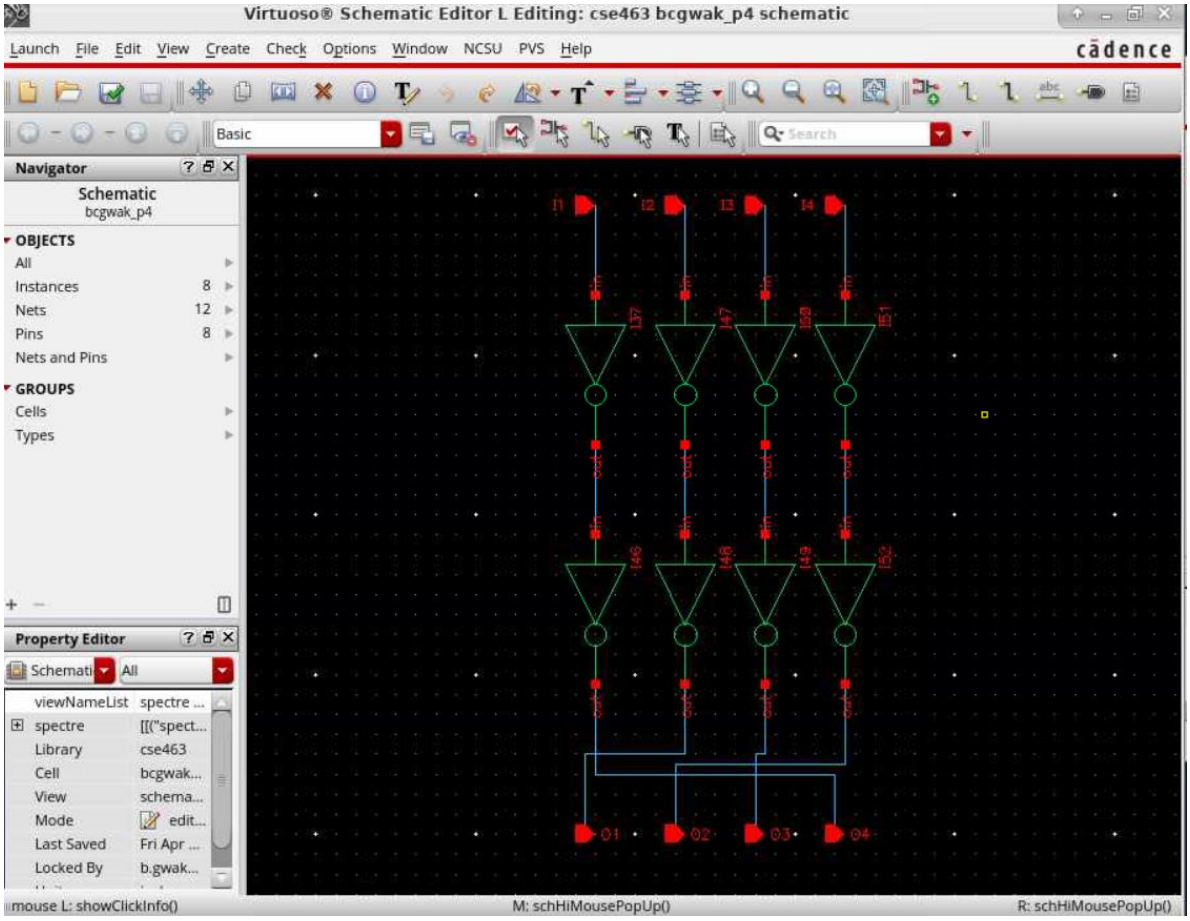
* P10


Virtuoso® Schematic Editor L Editing: cse463 bcgwak_p10 schematic
Launch File Edit View Create Check Options Window NCSU PVS Help
cadence
Basic
Navigator
Schematic
bcgwak_p10
OBJECTS
All
Instances 20
Nets 30
Pins 20
Nets and Pins
GROUPS
Cells
Types
Property Editor
Schemati All
viewNameList spectre ...
spectre [[("spect...
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()
Cmd: Sel: 0

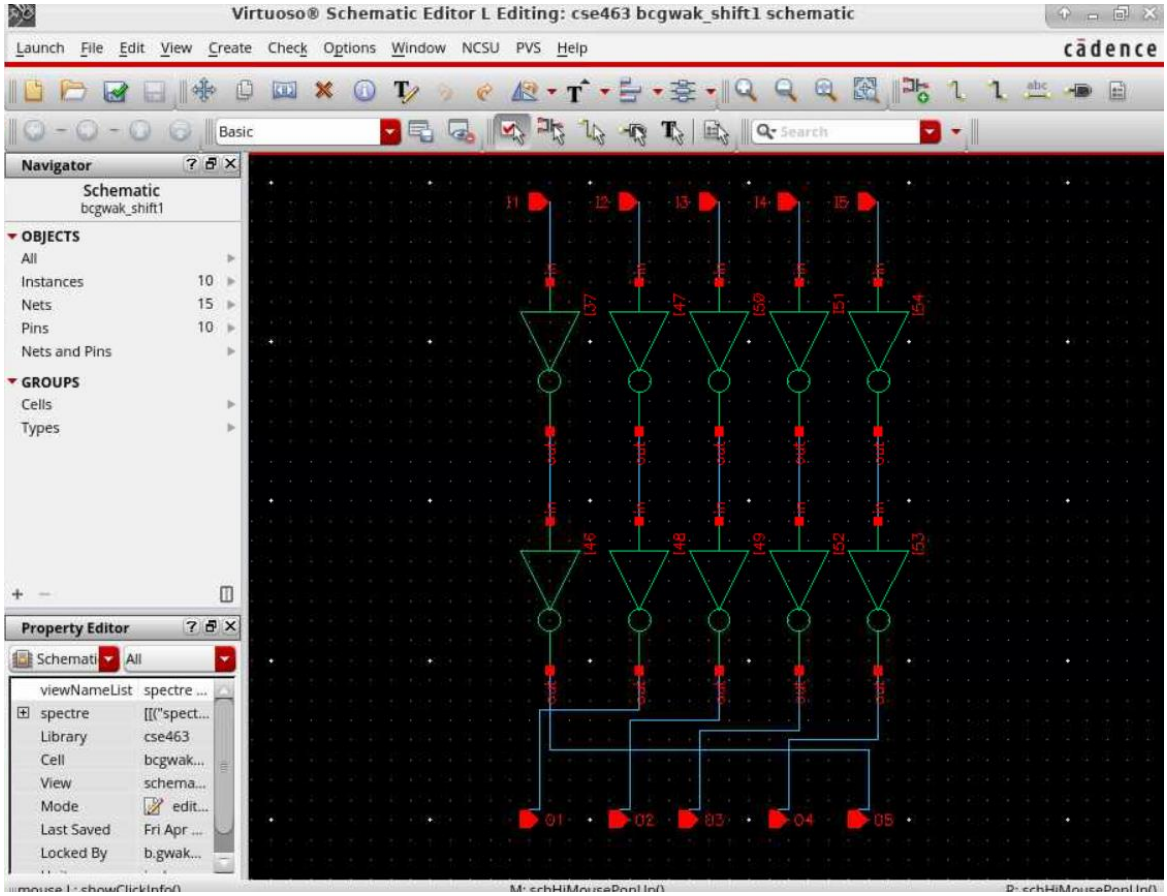
* P8


Virtuoso® Schematic Editor L Editing: cse463 bcgwak_p8 schematic
Launch File Edit View Create Check Options Window NCSU PVS Help
cadence
Basic
Navigator
Schematic
bcgwak_p8
OBJECTS
All
Instances 20
Nets 30
Pins 18
Nets and Pins
GROUPS
Cells
Types
Property Editor
Schemati All
viewNameList spectre ...
spectre [[("spect...
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...

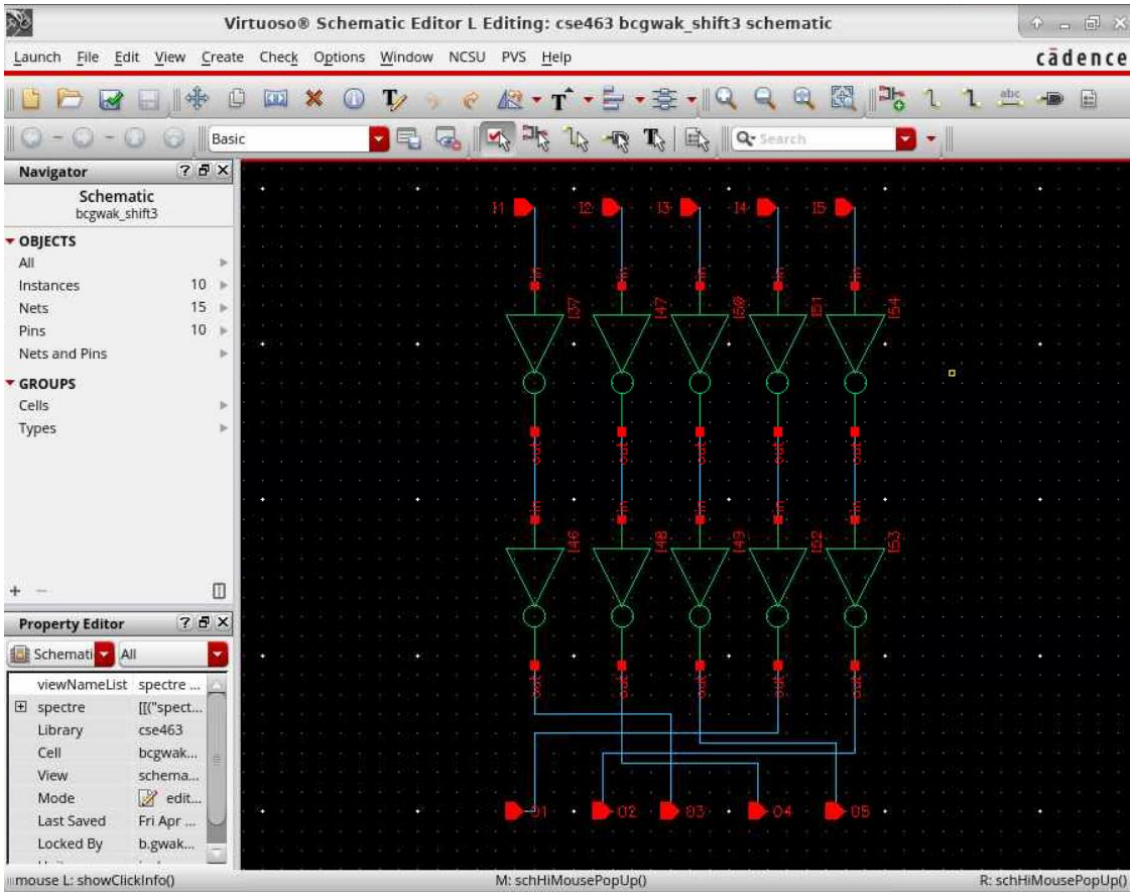
* P4


Virtuoso® Schematic Editor L Editing: cse463 bcgwak_p4 schematic
Launch File Edit View Create Check Options Window NCSU PVS Help
cadence
Navigator
Schematic
bcgwak_p4
OBJECTS
All
Instances 8
Nets 12
Pins 8
Nets and Pins
GROUPS
Cells
Types
Property Editor
viewNameList spectre ...
spectre [[("spect...
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...
I1
I2
I3
I4
I37
I47
I50
I51
I46
I48
I49
I52
O1
O2
O3
O4
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()

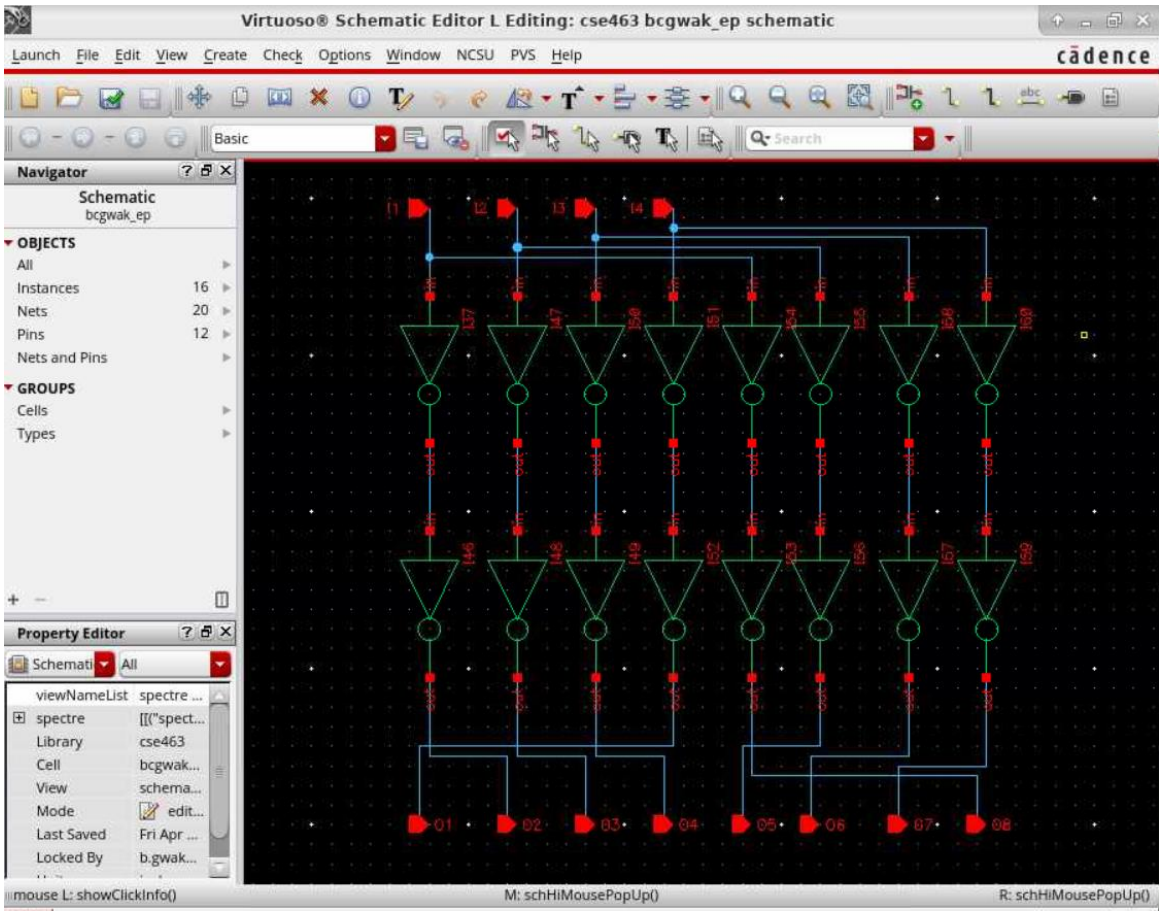
* SHIFT 1


Virtuoso® Schematic Editor L Editing: cse463 bcgwak_shift1 schematic
Launch File Edit View Create Check Options Window NCSU PVS Help
cadence
Navigator
Schematic
bcgwak_shift1
OBJECTS
All
Instances 10
Nets 15
Pins 10
Nets and Pins
GROUPS
Cells
Types
Property Editor
viewNameList spectre ...
spectre [[("spect...
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...
I1
I2
I3
I4
I5
I37
I47
I50
I51
I54
I46
I48
I49
I52
I53
O1
O2
O3
O4
O5

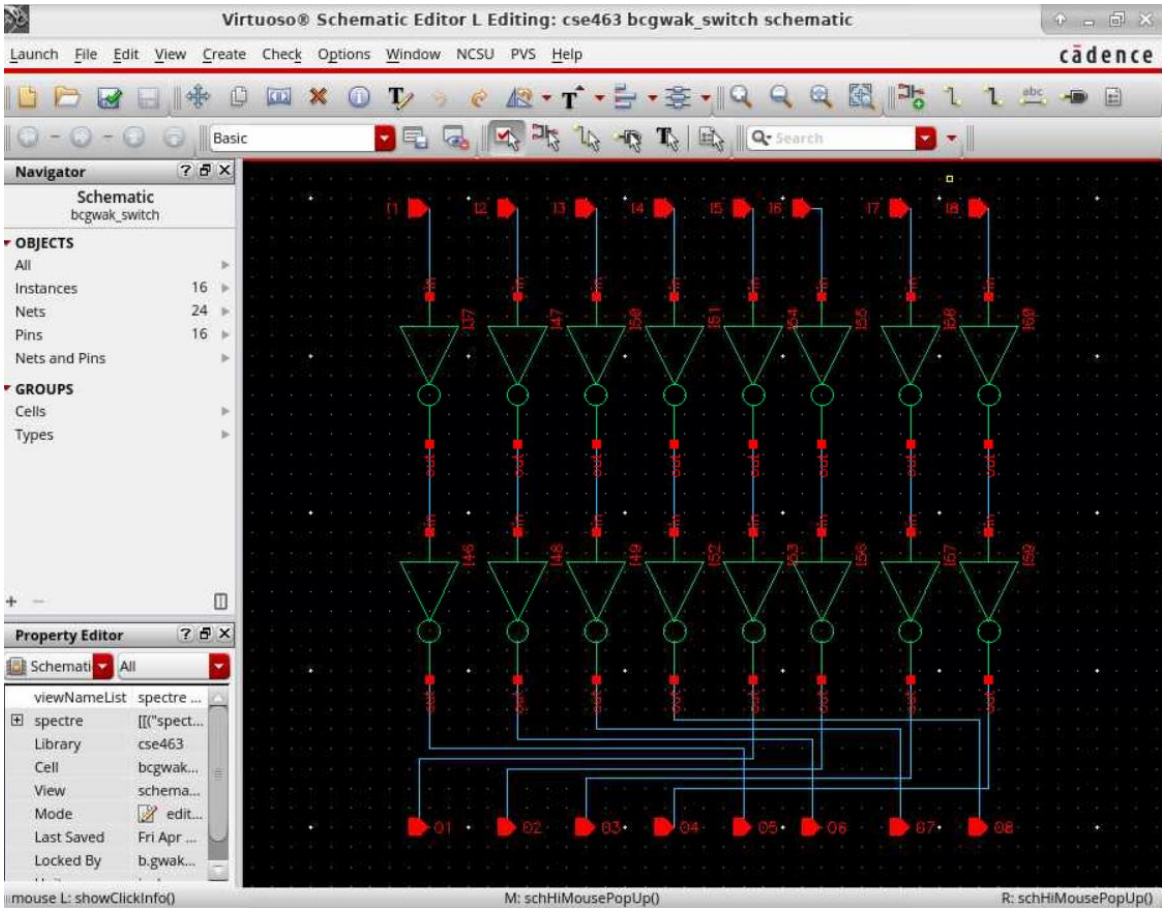
* SHIFT 3


Virtuoso® Schematic Editor L Editing: cse463 bcgwak_shift3 schematic
Launch File Edit View Create Check Options Window NCSU PVS Help
cadence
Navigator
Schematic
bcgwak_shift3
OBJECTS
All
Instances 10
Nets 15
Pins 10
Nets and Pins
GROUPS
Cells
Types
Property Editor
viewNameList spectre ...
spectre [[("spect...
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()

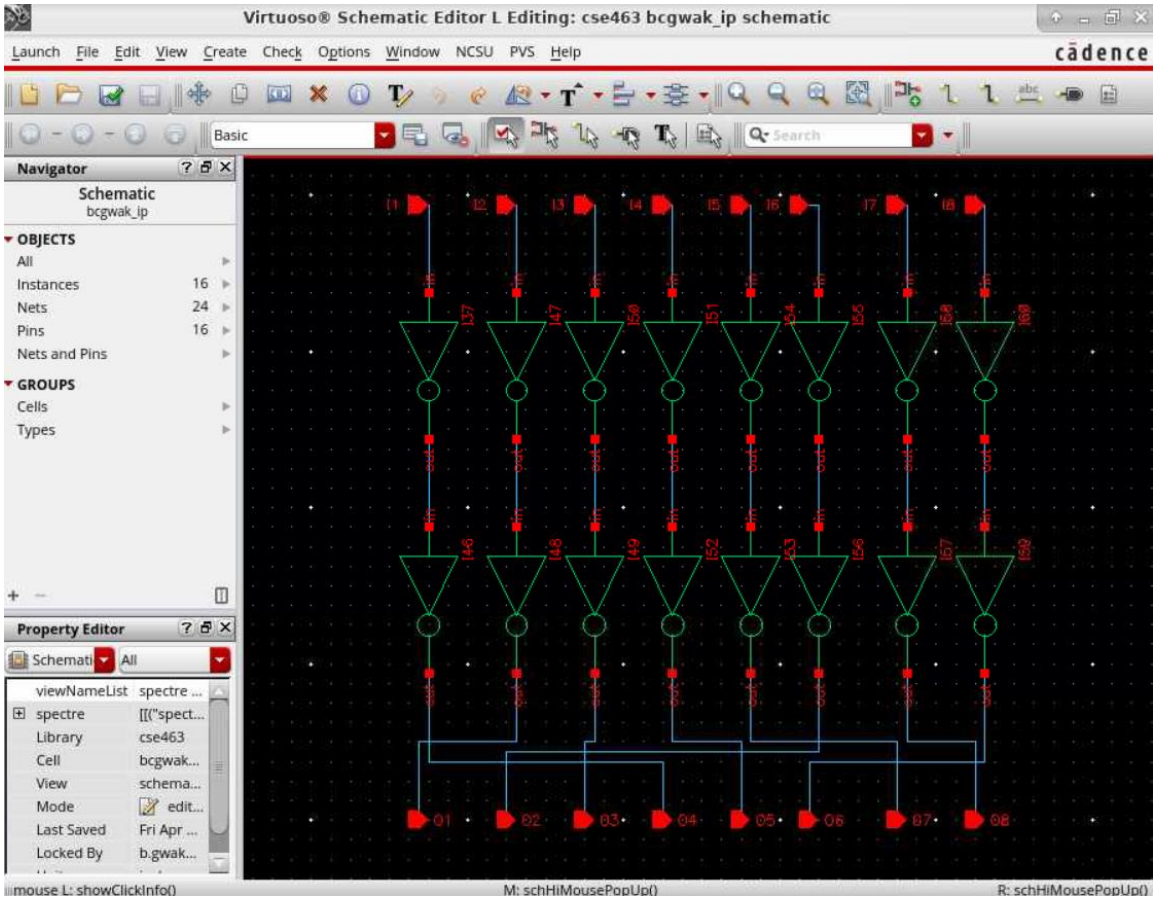
* EP


Virtuoso® Schematic Editor L Editing: cse463 bcgwak_ep schematic
Launch File Edit View Create Check Options Window NCSU PVS Help
cadence
Navigator
Schematic
bcgwak_ep
OBJECTS
All
Instances 16
Nets 20
Pins 12
Nets and Pins
GROUPS
Cells
Types
Property Editor
viewNameList spectre ...
spectre [[("spect...
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()

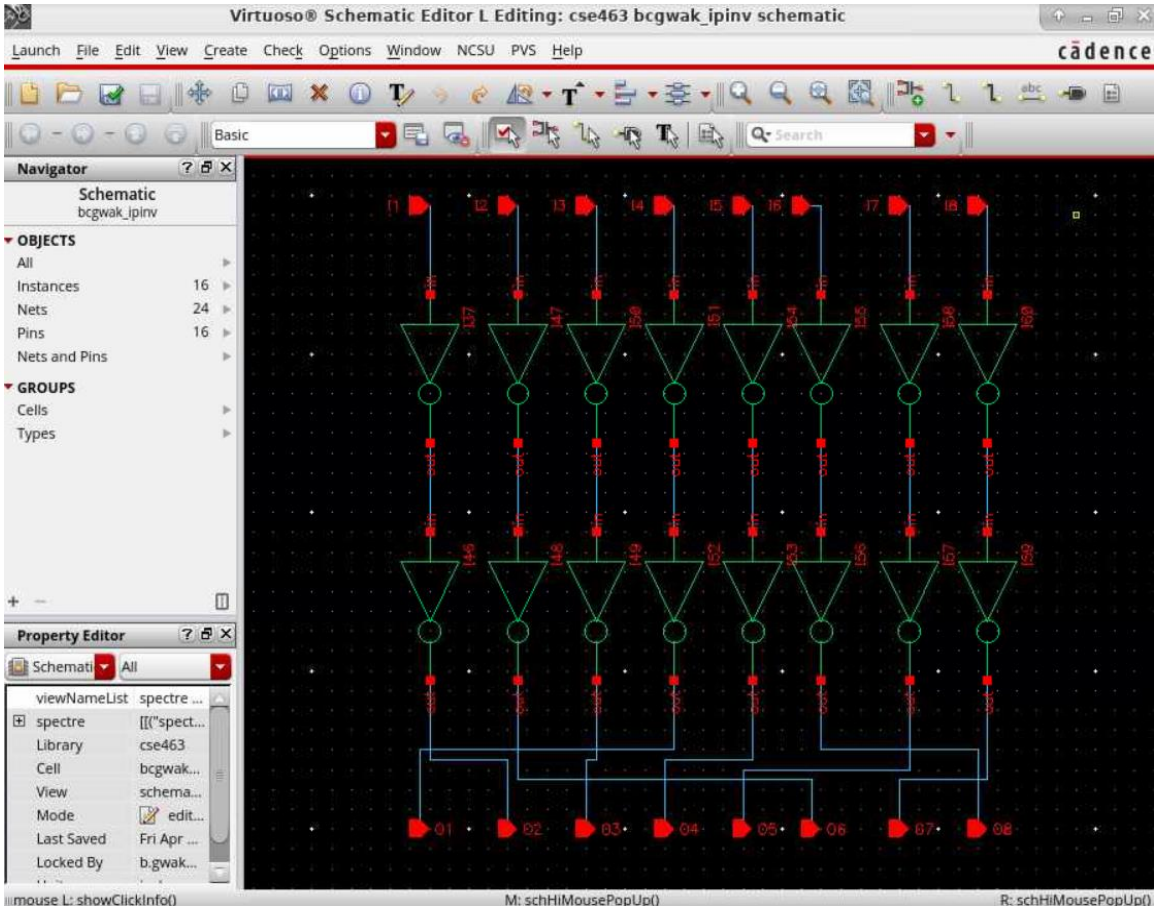
* SWITCH


Virtuoso® Schematic Editor L Editing: cse463 bcgwak_switch schematic
Launch File Edit View Create Check Options Window NCSU PVS Help
cadence
Basic
Search
Navigator
Schematic
bcgwak_switch
OBJECTS
All
Instances 16
Nets 24
Pins 16
Nets and Pins
GROUPS
Cells
Types
Property Editor
Schemati
All
viewNameList spectre ...
spectre [("spect...
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()

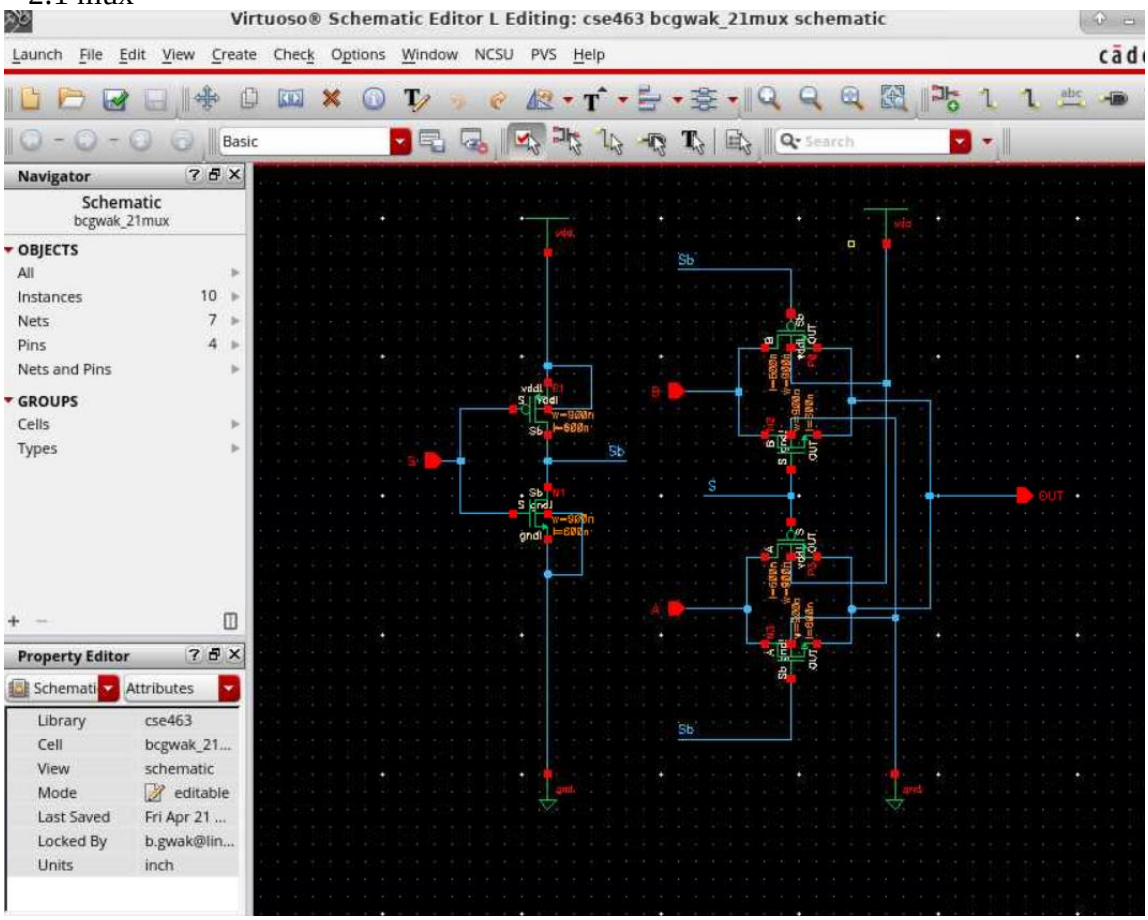
* IP


Virtuoso® Schematic Editor L Editing: cse463 bcgwak_ip schematic
Launch File Edit View Create Check Options Window NCSU PVS Help
cadence
Basic
Search
Navigator
Schematic
bcgwak_ip
OBJECTS
All
Instances 16
Nets 24
Pins 16
Nets and Pins
GROUPS
Cells
Types
Property Editor
Schemati
All
viewNameList spectre ...
spectre [("spect...
Library cse463
Cell bcgwak...
View schema...
Mode edit...
Last Saved Fri Apr ...
Locked By b.gwak...
mouse L: showClickInfo()
M: schHiMousePopUp()
R: schHiMousePopUp()

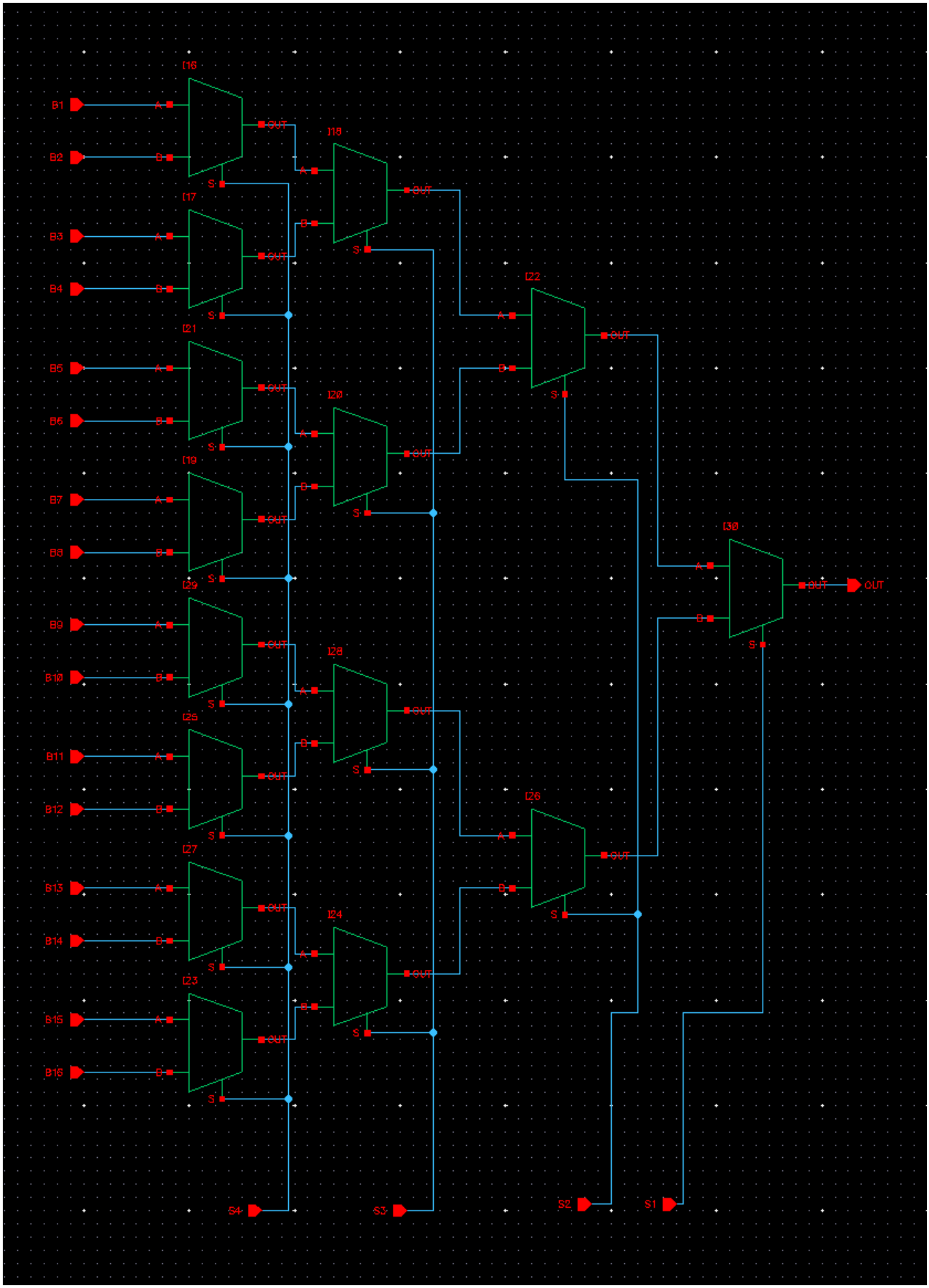
* IP Invert



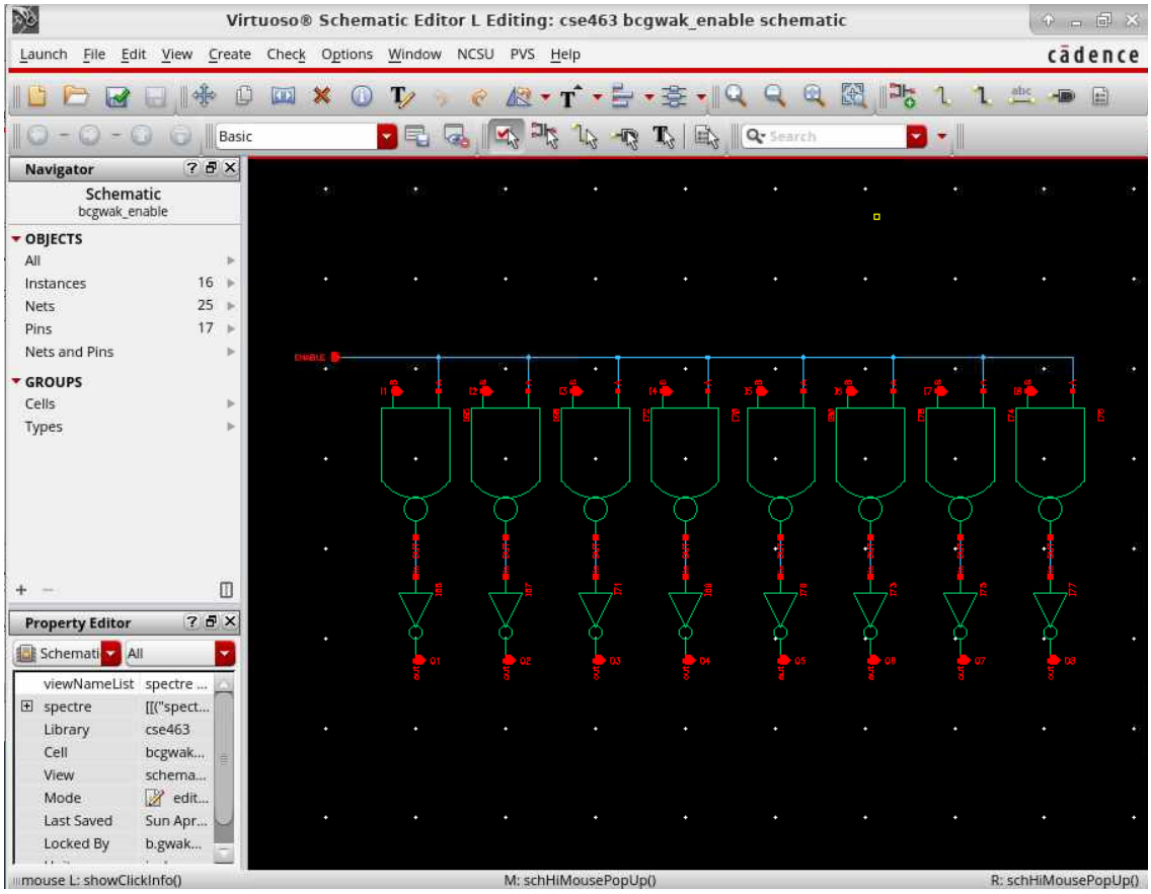
* 2:1 mux



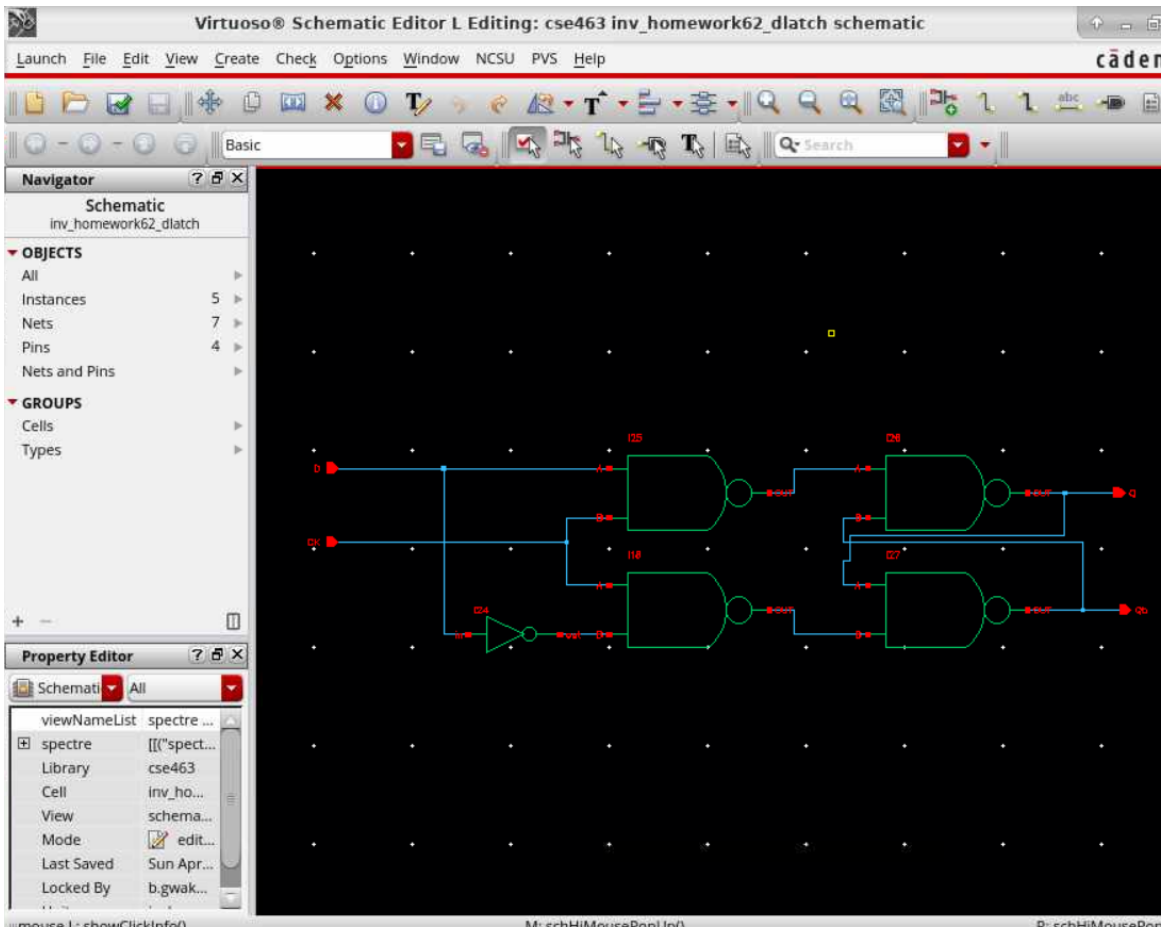
* 16:1 mux


I16
I18
I17
I22
I21
I20
I19
I30
I29
I28
I25
I26
I27
I24
I23
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
B13
B14
B15
B16
A
B
S
OUT
S4
S3
S2
S1

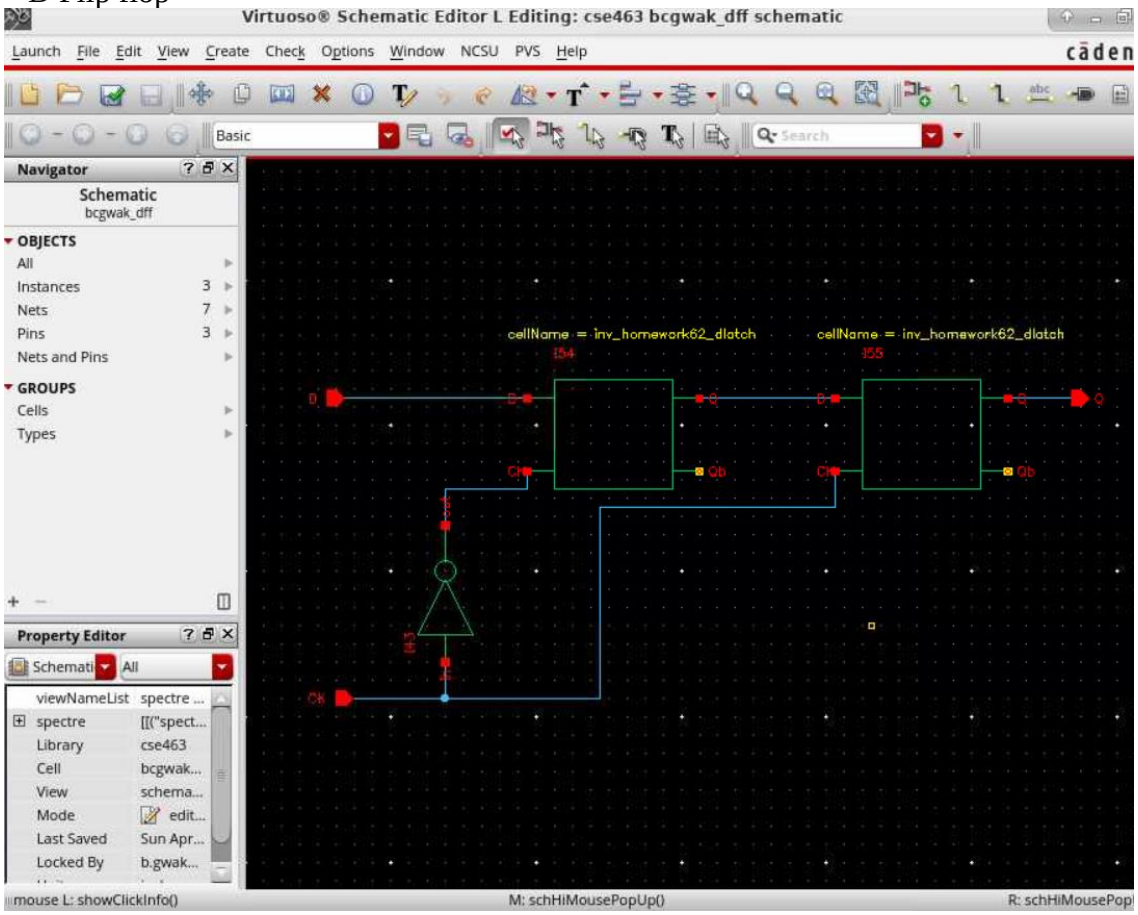
* ENABLE



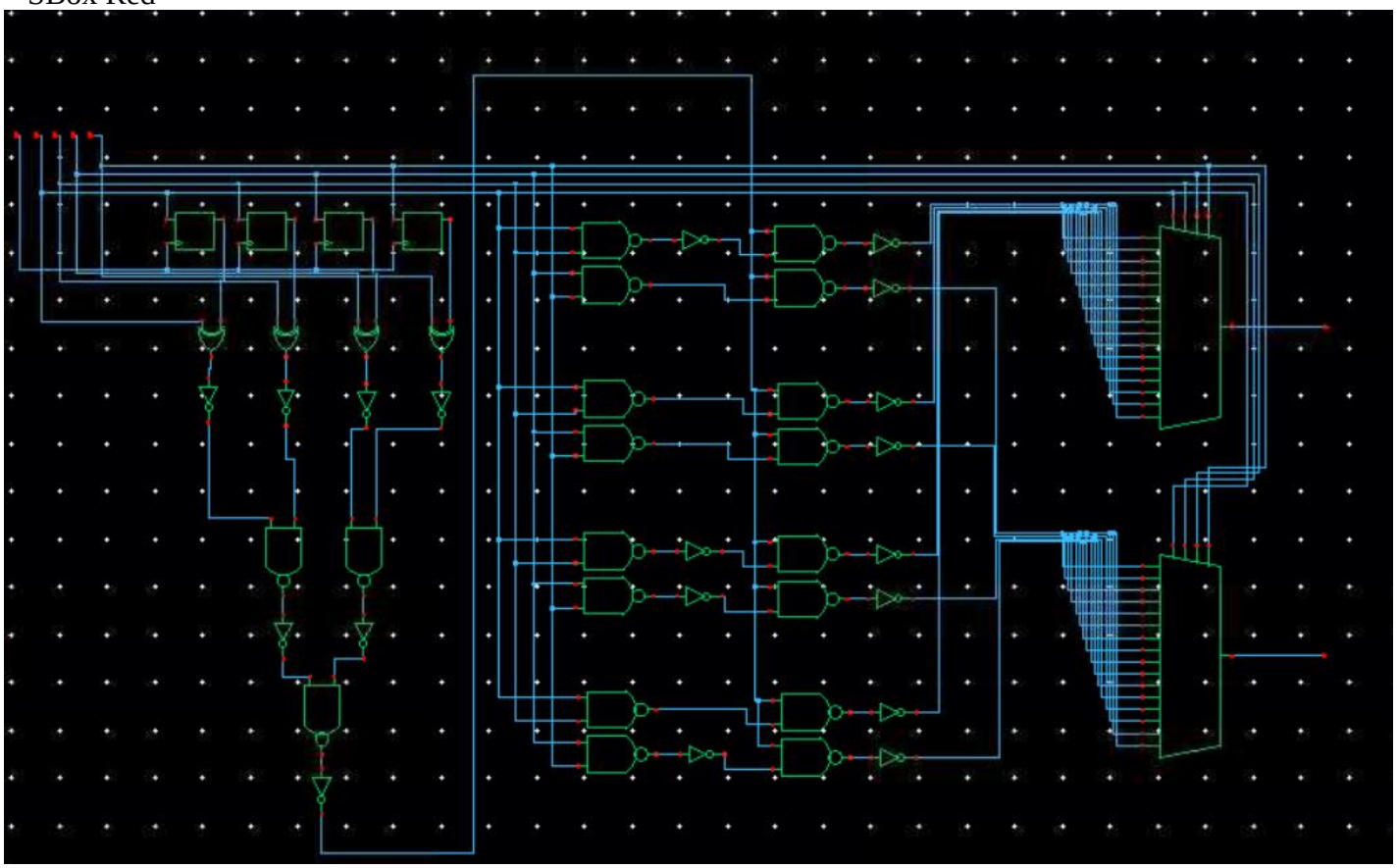
* D-LATCH



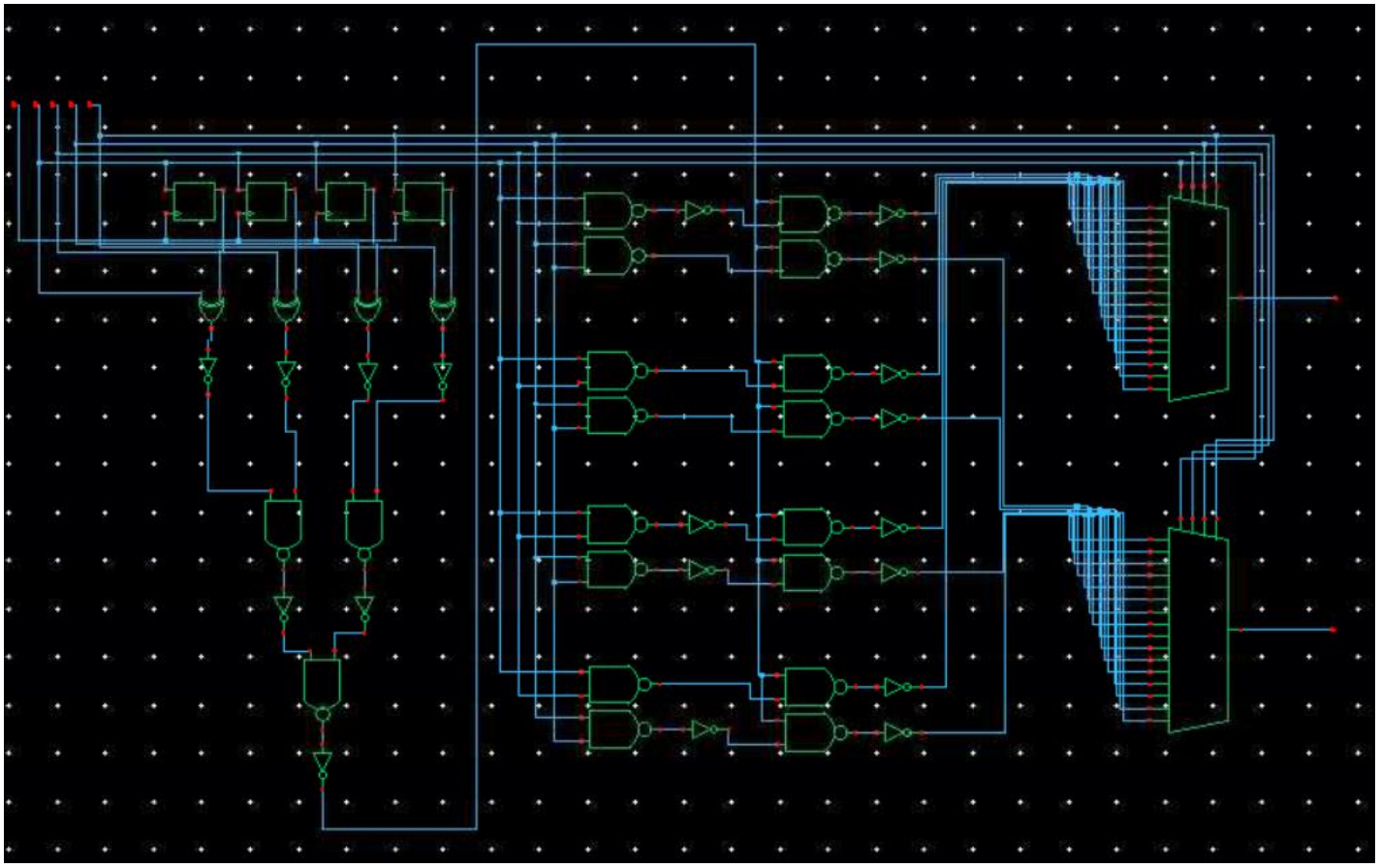
* D Flip flop



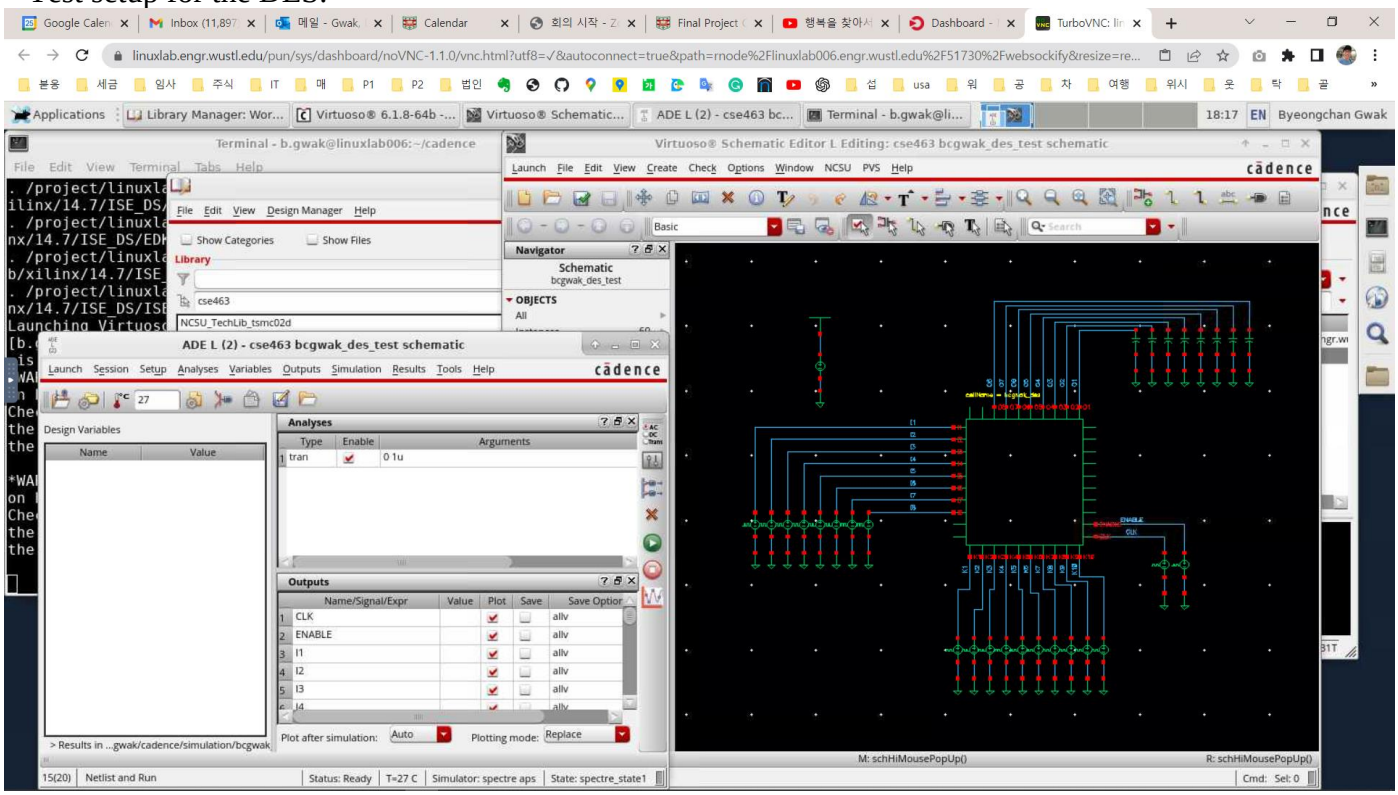
* SBox Red



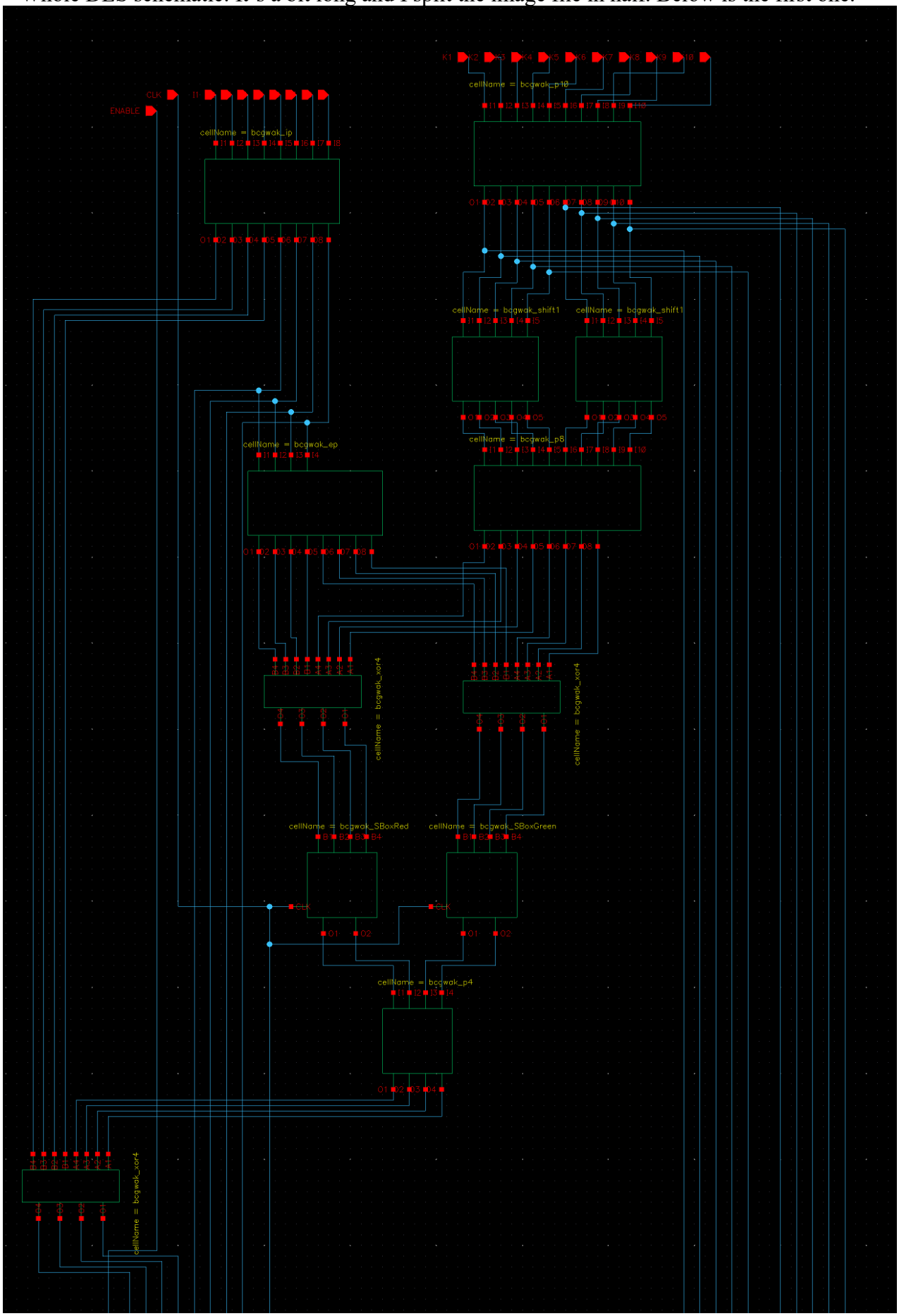
* SBox Green



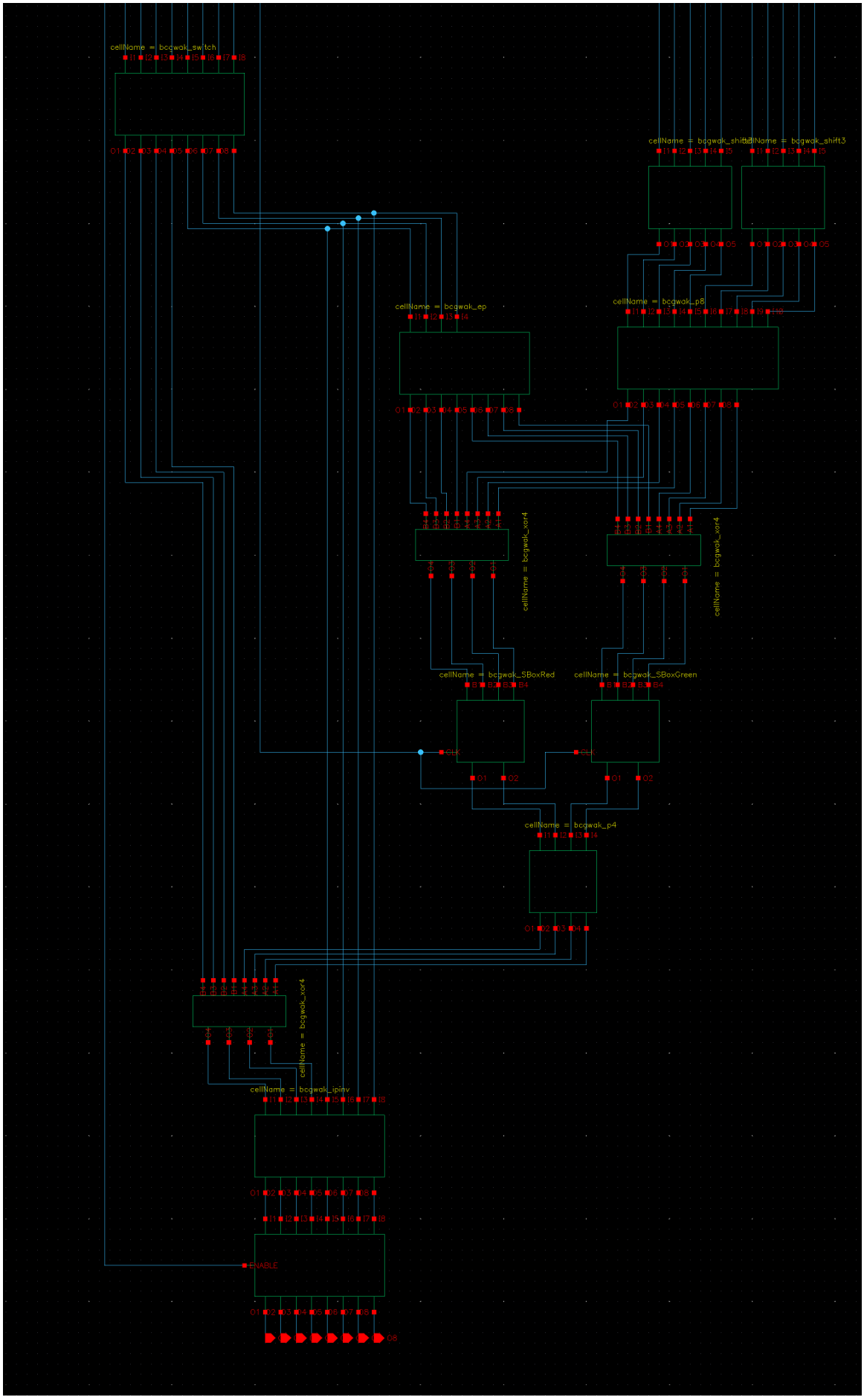
* Test setup for the DES.



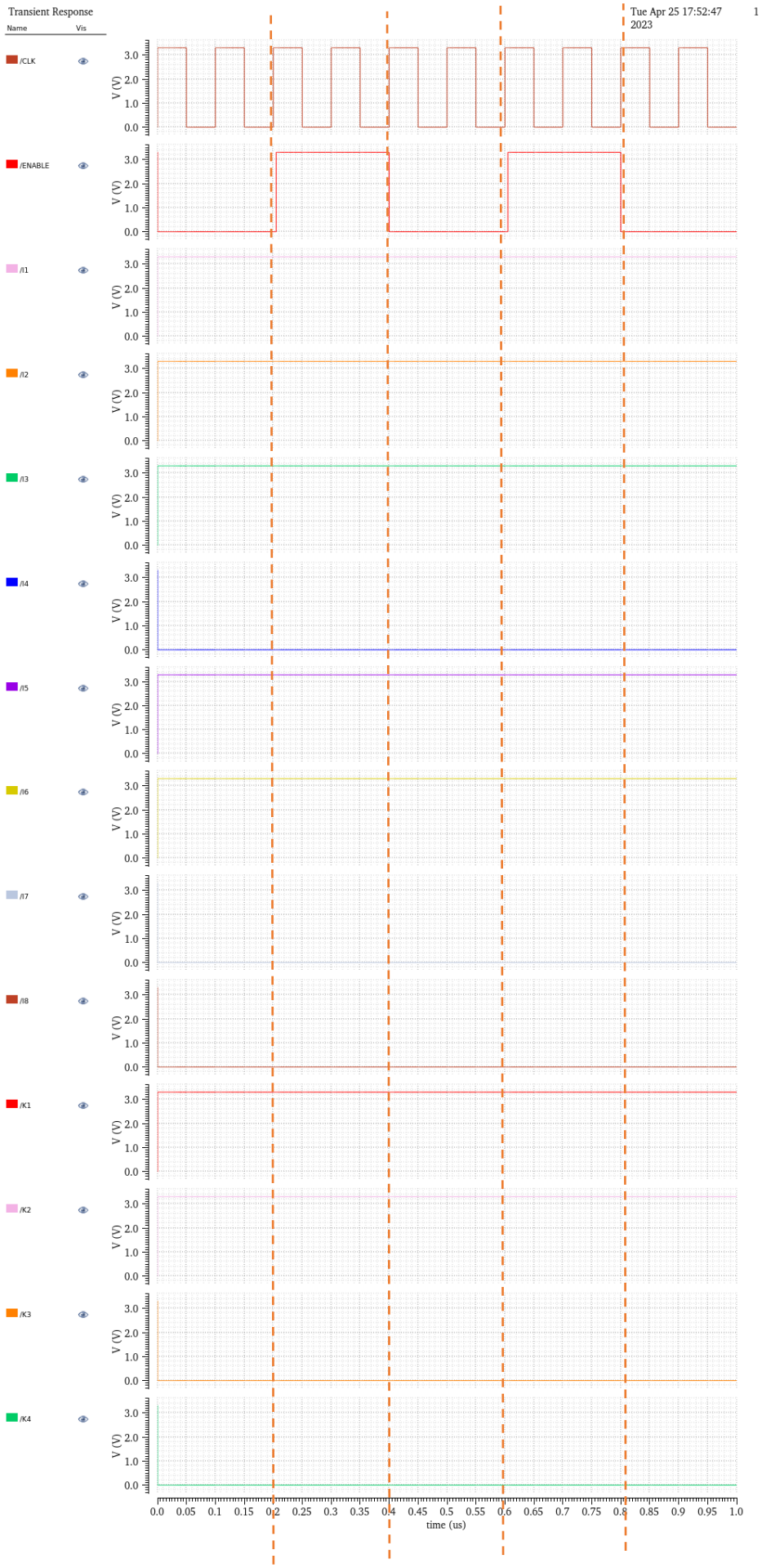
* Whole DES schematic. It’s a bit long and I split the image file in half. Below is the first one.

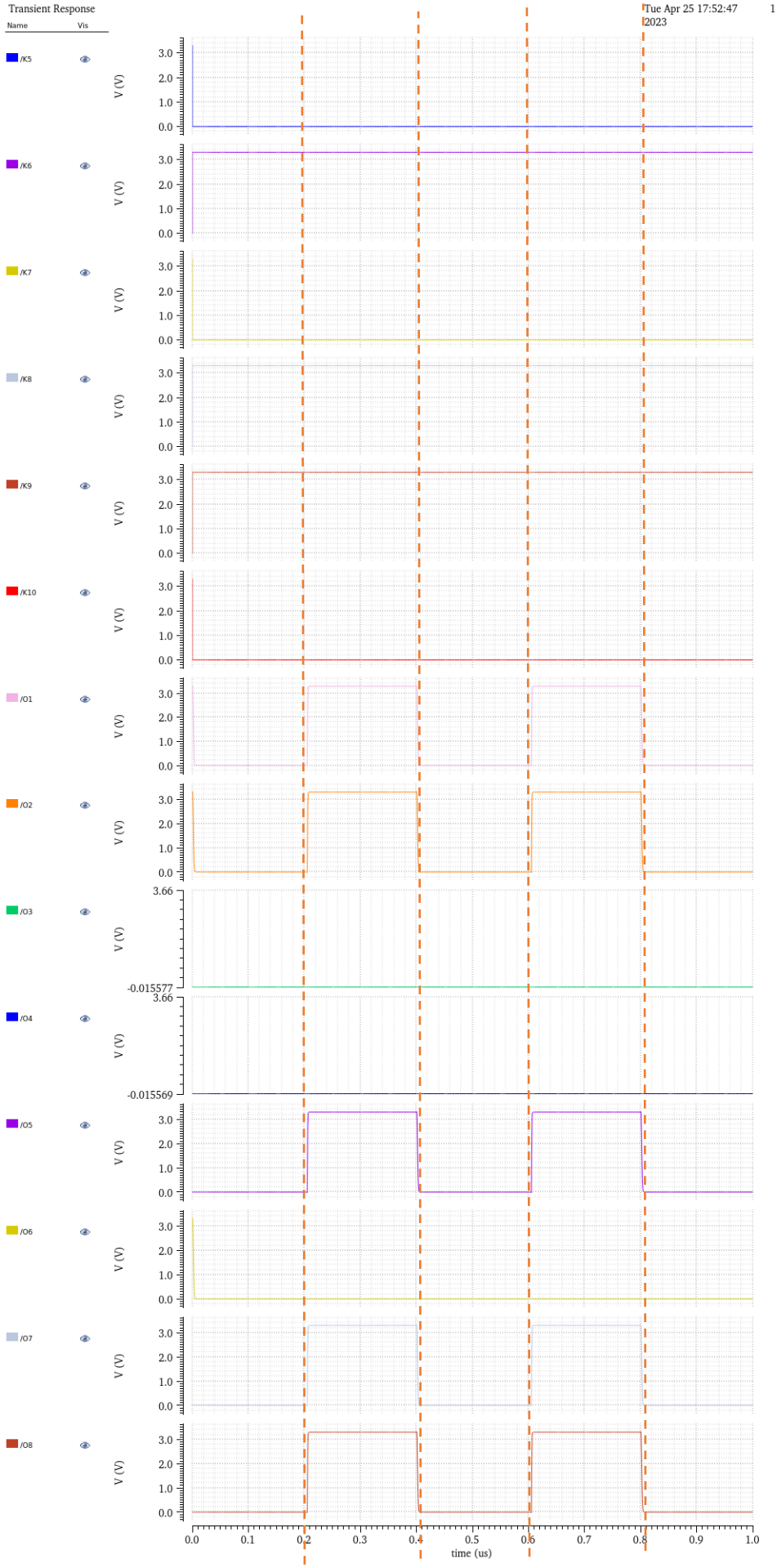


* Below is the second half.



* Test result: CLK, ENABLE, Input(I1, I2, …, I8), Key(K1, K2, …, K10), Output(O1, O2, …, O8)




Transient Response
Tue Apr 25 17:52:47 2023
1
Name
Vis
/K5
/K6
/K7
/K8
/K9
/K10
/O1
/O2
/O3
/O4
/O5
/O6
/O7
/O8
V (V)
3.0
2.0
1.0
0.0
3.66
-0.015577
-0.015569
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
time (us)