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PML2: The maskless multibeam solution for the 22nm node and beyond

C. Klein[a*], E. Platzgummer[a], J. Klikovits[a], W.Piller[a], H. Loeschner[a],
T. Bejdak[b], P. Dolezel[b], V. Kolarik[b],
W. Klingler[c], F. Letzkus[c], J. Butschke[c], M. Irmscher[c], M. Witt[d], W. Pilz[d],
P. Jaschinsky[e], F. Thrum[f], C. Hohle[f], J. Kretz[f], J.T. Nogatch[g], A. Zepka[g]

[a] IMS Nanofabrication AG, Schreygasse 3, 1020 Vienna, Austria
[b] Delong Instruments, Palackeho 153b, 612 00 Brno, Czech Republic
[c] Institut für Mikroelektronik Stuttgart - ims chips, Allmandring 30a, 70569 Stuttgart, Germany
[d] Fraunhofer Institut für Siliziumtechnologie, Fraunhoferstrasse 1, 25524 Itzehoe, Germany
[e] Fraunhofer Center for Nanoelectronic Technologies, Koenigsbruecker Str. 180, 1099 Dresden, Germany
[f] Qimonda Dresden GmbH & Co. OHG, Koenigsbruecker Str. 180, 1099 Dresden, Germany
[g] Synopsys Inc., 700 E Middlefield Rd, Mountain View, CA 94043, USA

Abstract

Projection Mask-Less Lithography (PML2) is a potentially cost-effective multi electron-beam solution for the 22 nm half-pitch node and beyond. PML2 is targeted on using hundreds of thousands of individually addressable electron-beams working in parallel, thereby pushing the potential throughput into the wafers per hour regime. With resolution potential of < 10 nm, PML2 is designed to meet the requirements of several upcoming tool generations.

Keywords: maskless lithography, parallel e-beam systems, multi electron beam

* e-mail: christof.klein@ims.co.at

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1. Introduction

Even though mask based optical lithography has been extremely successful in addressing the needs of the semiconductor industry so far, there has always been a pronounced interest in the realization of cost-effective electron-beam direct write (EBDW) technologies, which get rid of the costly photomasks altogether and allow for lithography of circuitry directly on the wafer. Especially now that photomask costs are sky-rocketing, interest in alternative concepts has intensified considerably.

Single beam EBDW tools have been around for decades and are still successfully used in the semiconductor industry as mask writers and for rapid device development. Typically, EBDW devices operate at 50 keV electron-beam energy and show excellent resolution capabilities. The only reason why those single beam EBDW tools are not widely used in production is their lack of throughput. Multi e-beam maskless lithography (ML2) on the other hand offers all the benefits of EBDW while resolving the volume problem by implementing a massive parallelization of electron beams. Consequently, there is currently pronounced interest in the realization of fully industry-compatible ML2 tools, especially in the field of fast prototyping and low volume chip production.[1] It is predicted, however, that ML2 will have the lowest cost of ownership of all lithographic techniques at the 32nm-hp node and beyond if it can achieve a throughput of 15 wafers (300mm) per hour.[2]

Projection Mask-Less Lithography (PML2)[3] is the multibeam maskless solution developed by IMS Nanofabrication and is based on its “charged particle large field projection optics” technology. The main strength of PML2 lies in the fact that pattern transfer is realized using an array of several hundreds of thousands individually addressable electron beams, thereby pushing the potential throughput from hours per wafer into the wafers per hour regime. Single-axis PML2 has 0.5 - 1 wph throughput potential for the 22nm hp node whereas multi-axis PML2 offers 5 - 10 wph, with possible extension to smaller nodes. Furthermore, several multi-axis PML2 tools can be clustered on the floor space allocated for an extreme ultraviolet lithography scanner, potentially providing 50 - 100 wph for the 22 nm hp node with the additional benefit of using the same common infrastructure.

2. Principles of Projection Mask-Less Lithography (PML2)

The basic concept of PML2 is shown schematically in Figure 1. In an electron-optical PML2 column, electrons are generated by a flat emitter of high brightness. The condenser below the electron source is used to form a large-field electron beam of high telecentricity, which then impinges with a kinetic energy of 5 keV onto the heart of every PML2 tool: the programmable aperture plate system (APS). Here, the homogeneous electron beam is split into several hundred thousand electron beamlets. These beamlets are accelerated to the final energy of 50 keV and projected with 200x reduction onto a resist-coated wafer. This way, 3.2 µm square openings in the APS are imaged as 16 nm spots, allowing for controlled 22 nm hp nanolithography on the wafer. Further reduction of the APS apertures

below 2 µm square will provide < 10 nm beamlets at the wafer and thus enable the extension to smaller nodes.

The programmable APS is located in the very center of a PML2 column and constitutes the object in the imaging electron optics. It consists of two silicon plates, both of which exhibit a periodic array of apertures. Individual beamlets are formed by the aperture plate, while dynamic structuring is realized by the blanking plate below. Deflection electrodes at every aperture of the blanking plate allow for individual control of the beamlets, i.e., each can be switched off at will. This is enabled by MEMS (micro-electro-mechanical-systems) fabricated deflection electrodes on a postprocessed CMOS chip with large openings. As shown in Figure 1, all deflected beams are blocked at a stopping plate close to the final crossover of the projection optics. Only undeflected beams are projected to the wafer surface with 200x reduction.

The first PML2 tool featuring all these properties is the PML2 Pre-Alpha Tool, which was developed within the European MAGIC (MAskless lithoGraphy for IC manufacturing) project.[4] This system is capable of handling 300 mm wafers and represents an upgrade to 50keV beam energy of the RIMANA 200× test bench,[5] which has demonstrated patterning capabilities down to 16 nm hp at 15keV.[6]

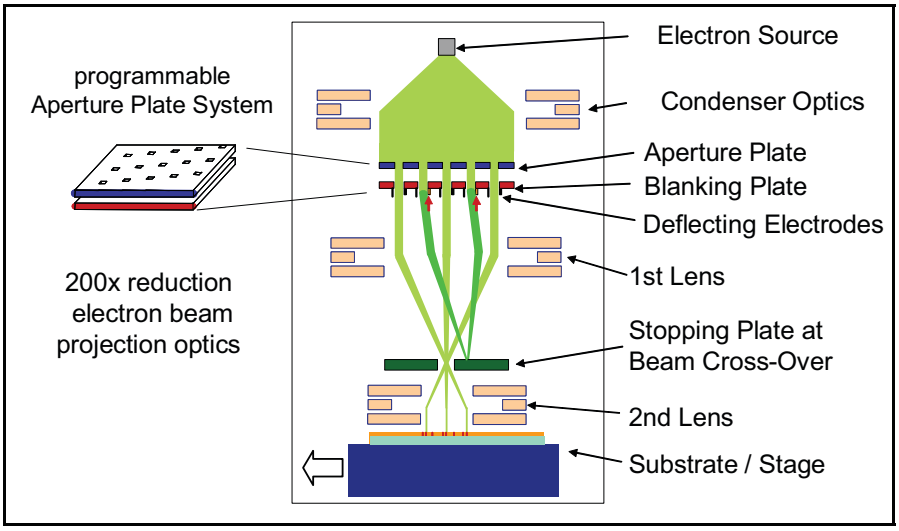


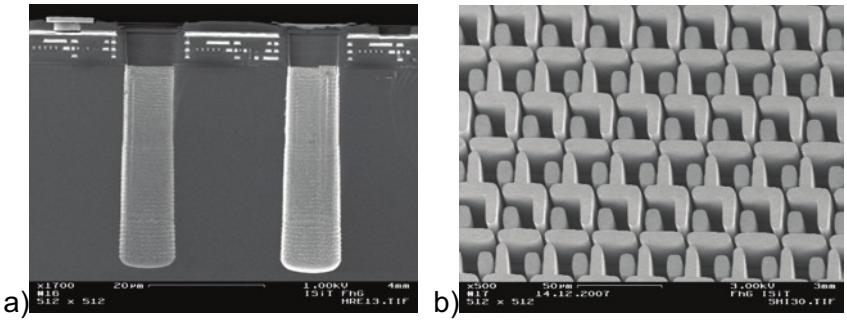
Figure 1: Principles of Projection Mask-Less Lithography (PML2)

3. CMOS-APS prototype for PML2 Pre-Alpha Tool

Within the RIMANA Project the Fraunhofer Institute for Silicon Technology (ISIT) has evaluated and developed the fundamentals for the MEMS fabrication process for the APS blanking plate chip with integrated CMOS electronics (CMOS-BLC). This complex fabrication process has been continually improved in order to end up with functional devices. The required measures comprised design modifications, process upgrades, yield improvements and the implementation of several process control steps. Eventually, fully

operational blanking plate chips with up to 99.96% functionality of the deflection electrodes have been fabricated.

Figure 2 shows some of the most important fabrication steps for such a CMOS-BLC. First, 8 x 8 μm^2 apertures have to be etched into the CMOS chip to 40 µm depth into the Silicon wafer by reactive ion etching (Figure 2a). Then blanking and ground electrodes are grown on top of the CMOS chip (Figure 2b) implementing optical LIGA techniques. Forming a 30 µm thick membranes the 8 x 8 μm^2 apertures are finally opened.



a) b)

Figure 2: CMOS-BLC fabrication. a) reactive ion etching through CMOS chip into 40 µm thick Si of Blanking Plate, b) electroplated blanking and ground electrodes (height: 35 µm)

After completion of all post-processing procedures the CMOS-BLC is mounted onto a Si base plate and connected to a 52-pin plug via wire-bonds (see Figure 3). This assembly is then tested in a 1x APS Testbench using 5 keV electron beams. Here, the deflection power of every single blanking electrode is tested and the quality of the openings is studied. The openings don't have to exhibit any particular shape they just have to be considerably larger than the apertures in the aperture plate and they must not show pronounced charging effects. Figure 3 shows the 1x APS Testbench results of a fully operational CMOS-BLC, which was used for the assembly of the first APS Prototype.

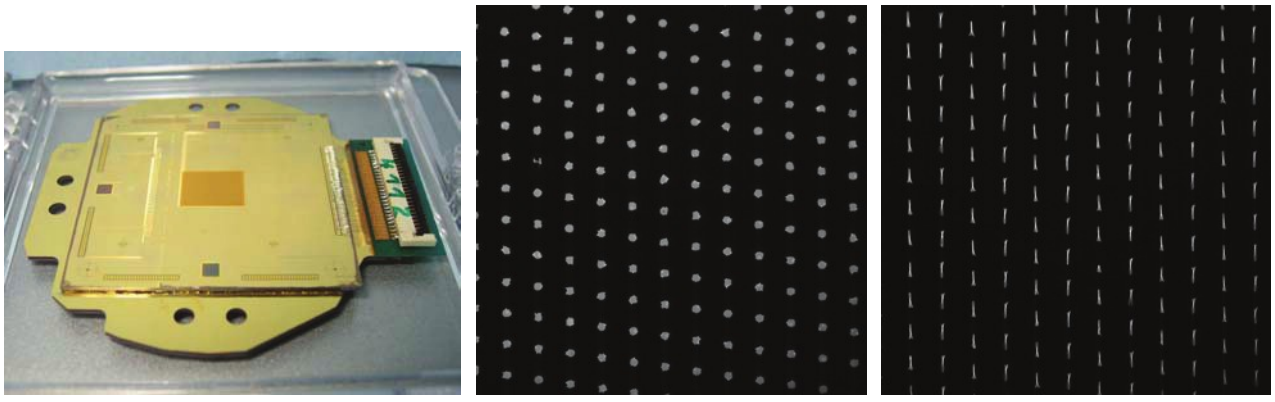


Figure 3: Foto (left) and 1x APS Testbench images of fully operational CMOS-BLC; center: unblanked status, moderate beamlet shape deformations due to imperfect etching and minor charging effects; right: blanked status (deflection: 1mrad), all beamlets within the field of view are working properly.

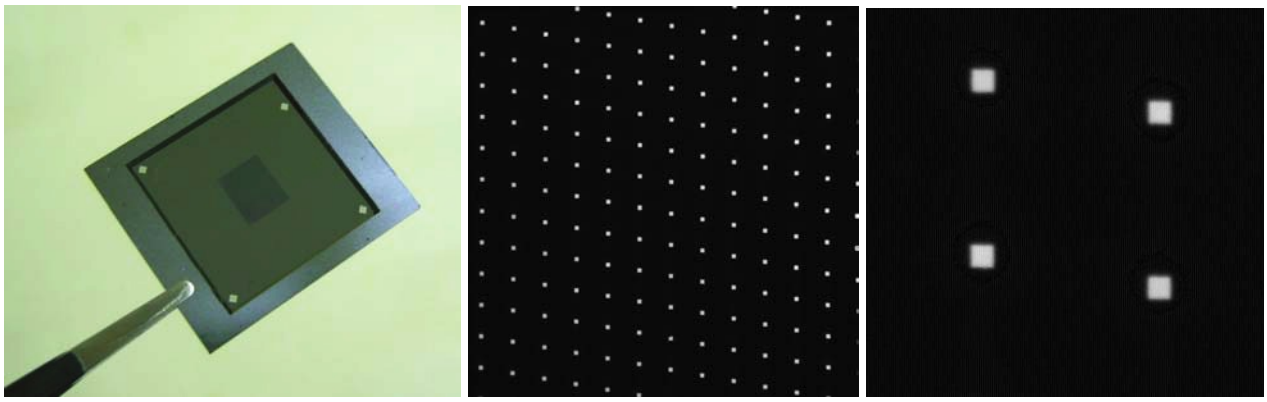


Figure 4: Foto (left) and 1x APS Testbench images of Aperture Plate with 3.75 µm x 3.75 µm openings and 30 µm periodicity. Magnified image of 4 randomly selected openings (right). No deformation of beamlet shape visible; i.e. no charging effects present.

Before final assembly of an APS, the selected aperture plate has to be tested for charging. Figure 4 shows 1x APS Testbench images of a 3.75 µm aperture plate; i.e. an aperture plate with 3.75 x 3.75 μm^2 openings. Here, the apertures are imaged as perfect squares showing absolutely no charging effects. Consequently, the aperture plate shown in Figure **4** can be used for APS assembly.

For the final APS assembly an alignment apparatus was realized (Figure 5) allowing for precise alignment of an aperture plate onto a post-processed CMOS-BLC with better than 0.5 µm accuracy (Figure 6).

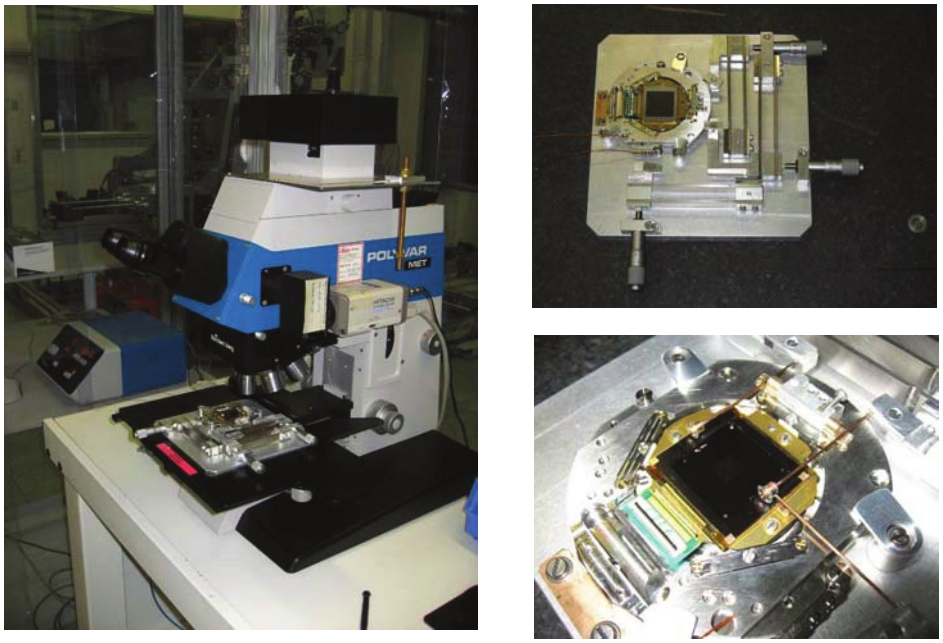


Figure 5: Alignment apparatus for APS assembly based on optical transmission microscopy. Aperture plates are mounted onto CMOS-BLCs with sub-µm accuracy.

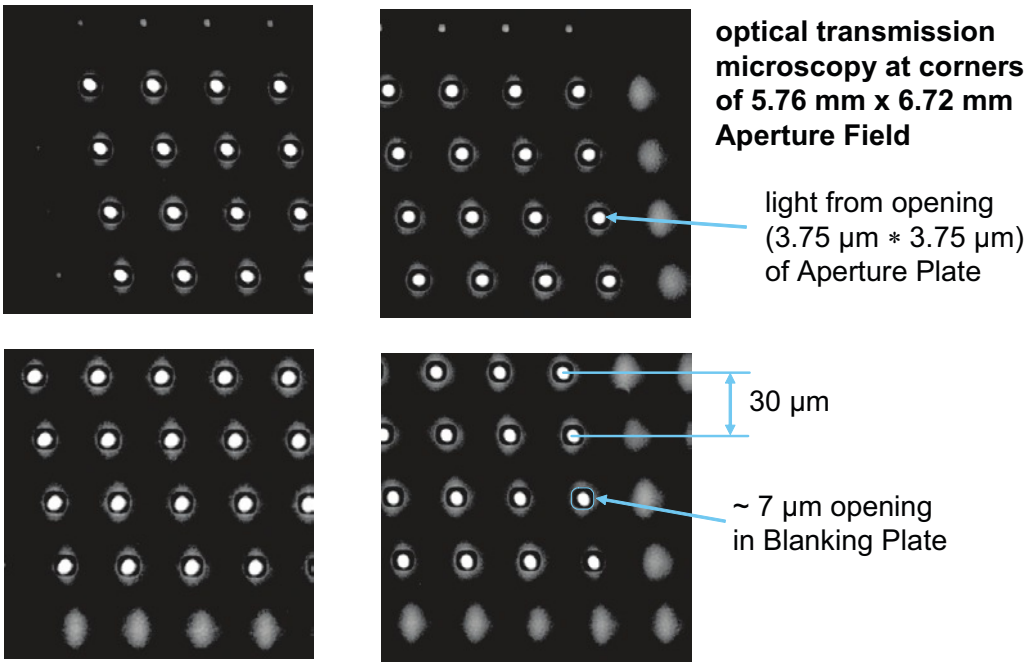


Figure 6: Demonstration of sub-µm alignment precision of APS alignment apparatus.

Figure 7 shows an assembled CMOS-APS consisting of the 3.75µm aperture plate shown in Figure 4 and the fully operational CMOS-BLC shown in Figure 3. In Figure 8 the corresponding 1x APS Testbench characterization results are shown, demonstrating the full functionality of this CMOS-APS unit. This prototype APS unit, however, will be mainly used for the generation of 32 nm hp node patterns due to its beam-size of 19 nm at wafer level.

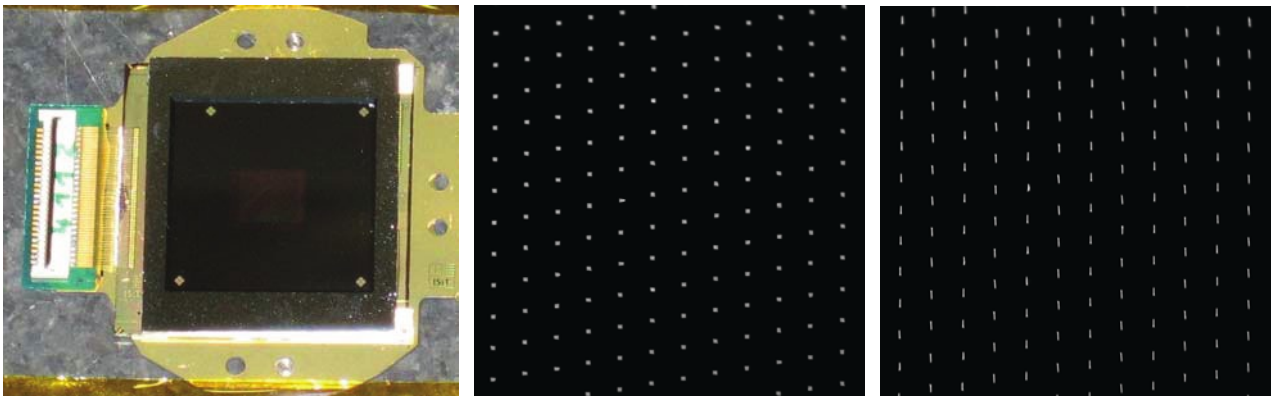


Figure 7: Foto (left) and 1x APS Testbench images of assembled CMOS-APS with 43k apertures. Center: undeflected beams; right: deflected beams.

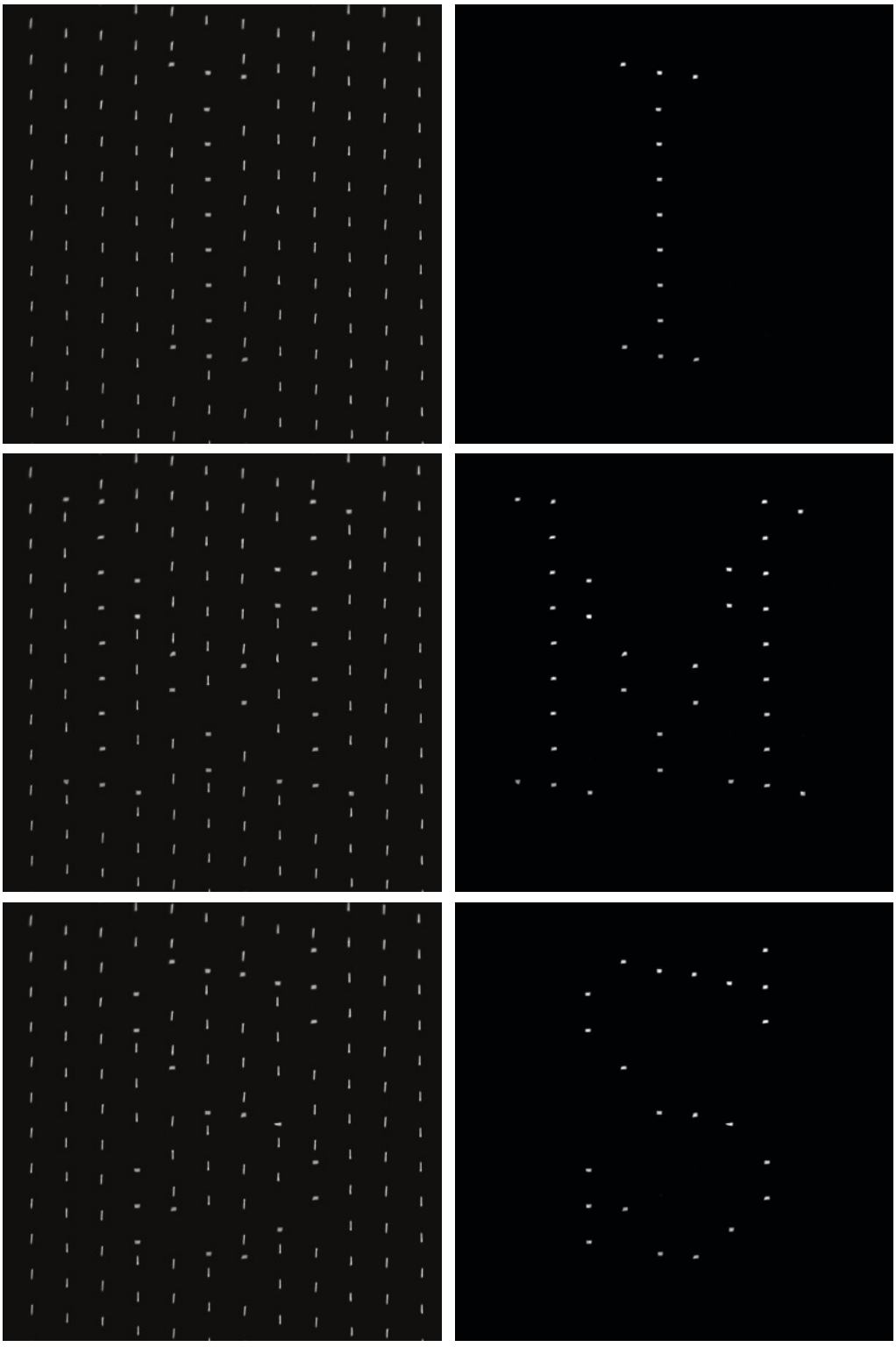


Figure 8: 1x APS Testbench characterization of CMOS-APS prototype. Screen shots of a movie demonstrating the CMOS-APS performance. The right side shows all beams reaching the wafer.

Using an aperture plate with 2.5 x 2.5 μm^2 openings and another fully operational CMOS-BLC a second CMOS-APS unit was assembled. Figure 9 shows the corresponding 1x APS testbench results. Deflected and undeflected images were superpositioned in order to allow for analysis of the deflection power of the individual electrodes. The deflection power of all blankers was found to be greater than 900 µrad which is considerably above the required 350 µrad (see Figure 10).

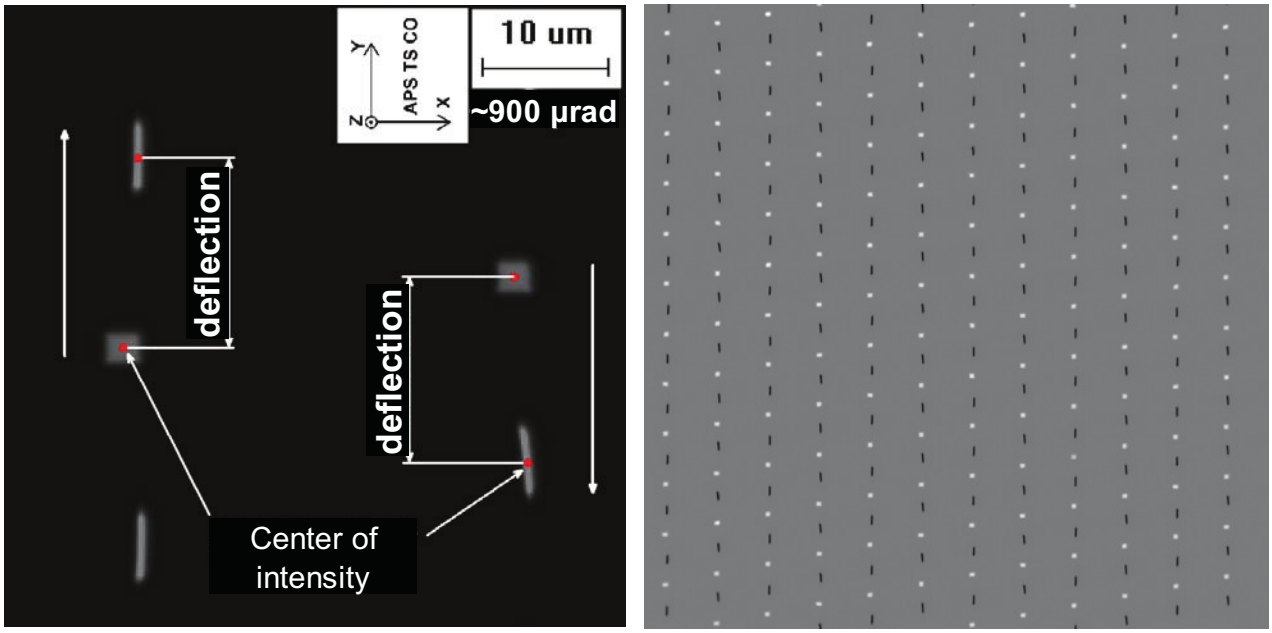


Figure 9: 1x APS Testbench characterization of second CMOS-APS prototype. Deflected and undeflected images were superpositioned in order to allow for analysis of deflection power.

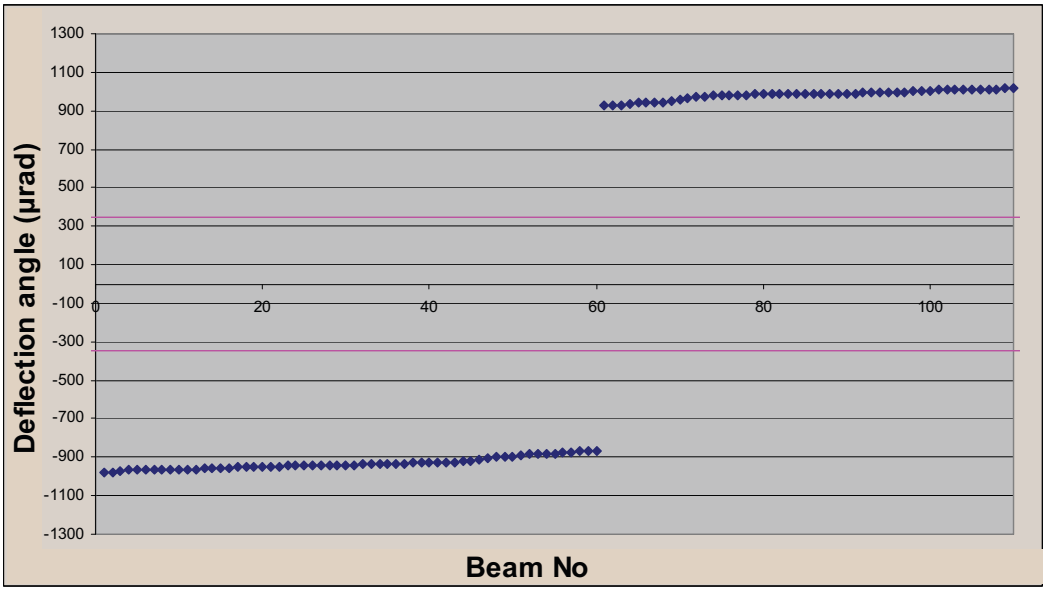


Figure 10: Analysis of the deflection power of the 110 blankers shown in Figure 9. All deflection angles were found to be considerably above the required value of 350 µrad.

Using the second 2.5µm-CMOS-APS it will already be possible to demonstrate 22nm hp structures (and beyond) due to its very small spot size at wafer level of 12.5 nm. Figure 11 shows the fully assembled APS module mounted in the APS chuck and ready for insertion into the PML2 Pre-Alpha Tool.

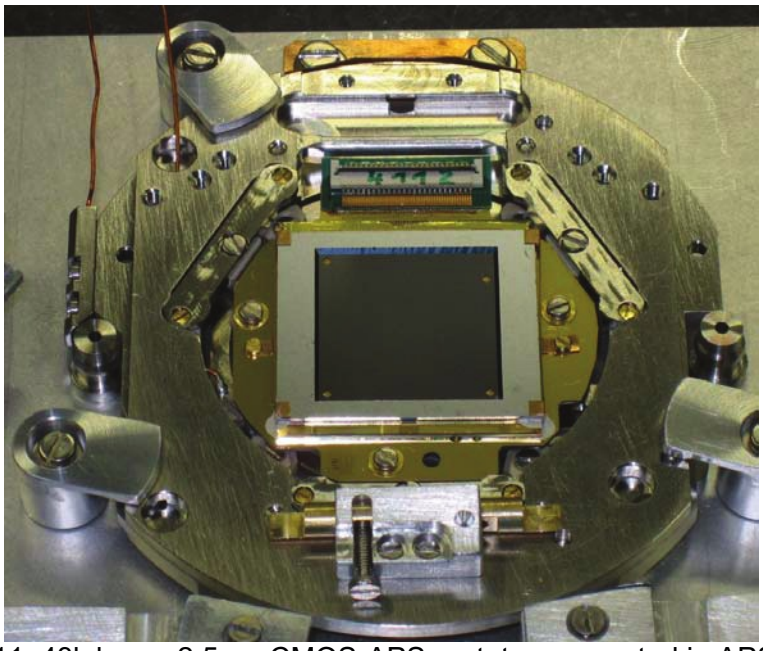


Figure 11: 43k beam 2.5µm-CMOS-APS prototype mounted in APS chuck

3. PML2 Pre-Alpha Tool

Within the 6th European framework program (FP6) IMS Nanofabrication coordinated the RIMANA (Radical Innovation MAskless Nanolithography) project.[5] As part of this project a PML2 proof-of-concept system, the RIMANA 200x Testbench, has been realized in 2007.

The electron-optical column of the PML2 proof-of-concept system contained already all critical components of a full-fledged PML2 tool while keeping very slim dimensions (length < 600mm; diameter < 150mm). The most space-consuming parts of this tool were wafer exposure chamber and air lock which were designed to handle 150 mm wafers. Due to cost and timing issues, however, the maximum exposure energy was kept at 15 keV. Details on the RIMANA 200x Testbench can be found elsewhere.[6]

This RIMANA 200x Testbench was upgraded to the MAGIC PML2 Pre-Alpha Tool in December 2008. Modifications included the realization of a new 300 mm toolbase, which enables the handling of 150 mm and 300 mm wafers and a new acceleration optics which allows for an increase of the electron beam energy at wafer level from 15 to 50 keV. Figure 12 shows pictures of the fully assembled PML2 Pre-Alpha Tool and its 300 mm wafer chuck.

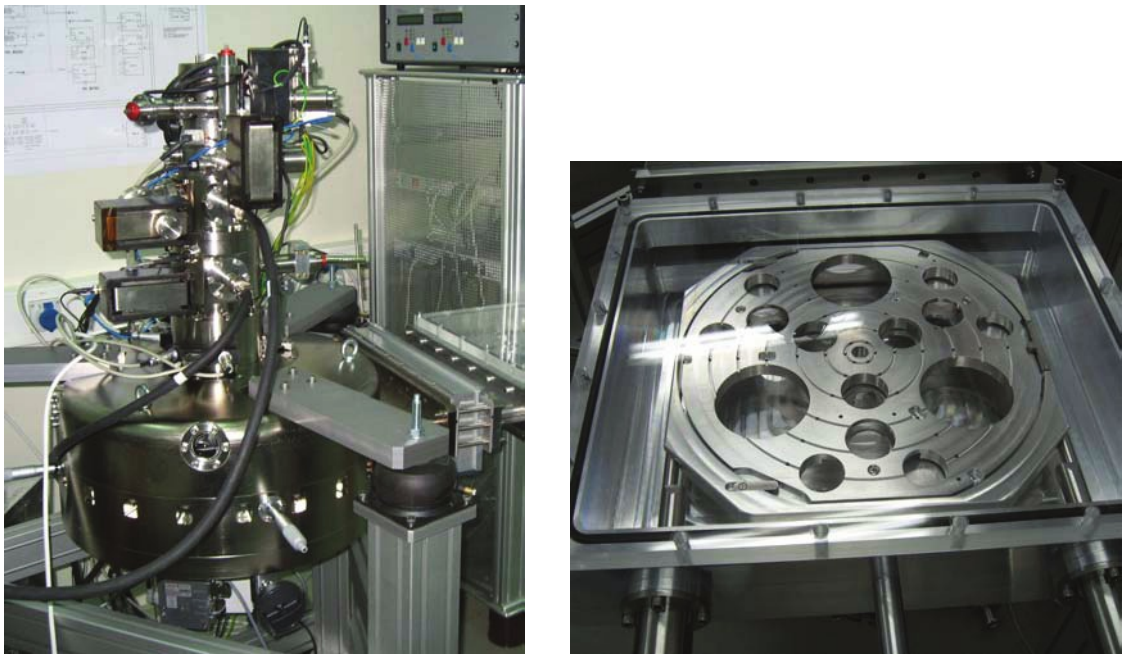


Figure 12: PML2 Pre-Alpha Tool (left); 300mm wafer chuck (right)

Alignment and optimization of the PML2 Pre-Alpha Tool is still ongoing and planned to be finished in March 2009. First preliminary results have already been generated and are shown in Figure 13 and Figure 14. In Figure 14 the line width variation within a given pattern is plotted and 2 different exposure areas are compared.

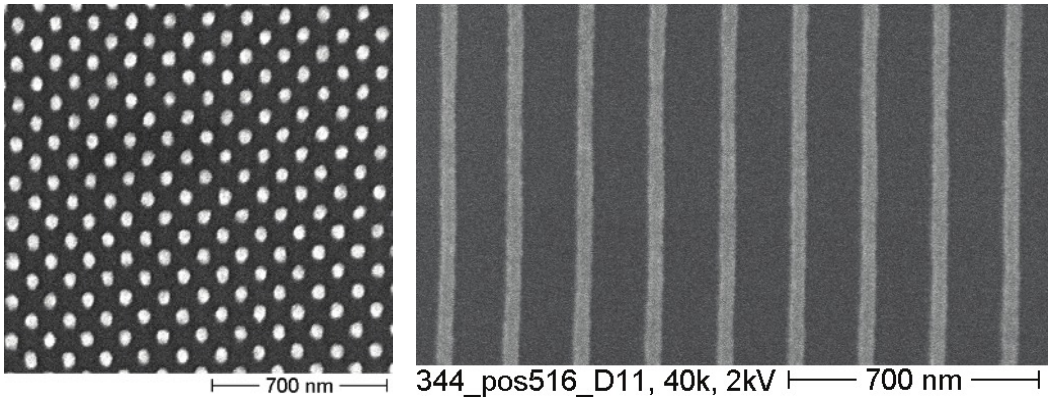


Figure 13: First exposure results in 50nm HSQ. Left: 50.2nm contact holes/dots (σ = 2.47nm, dose = 1969 μC/cm^2); right: 40nm lines with duty ratio 5.

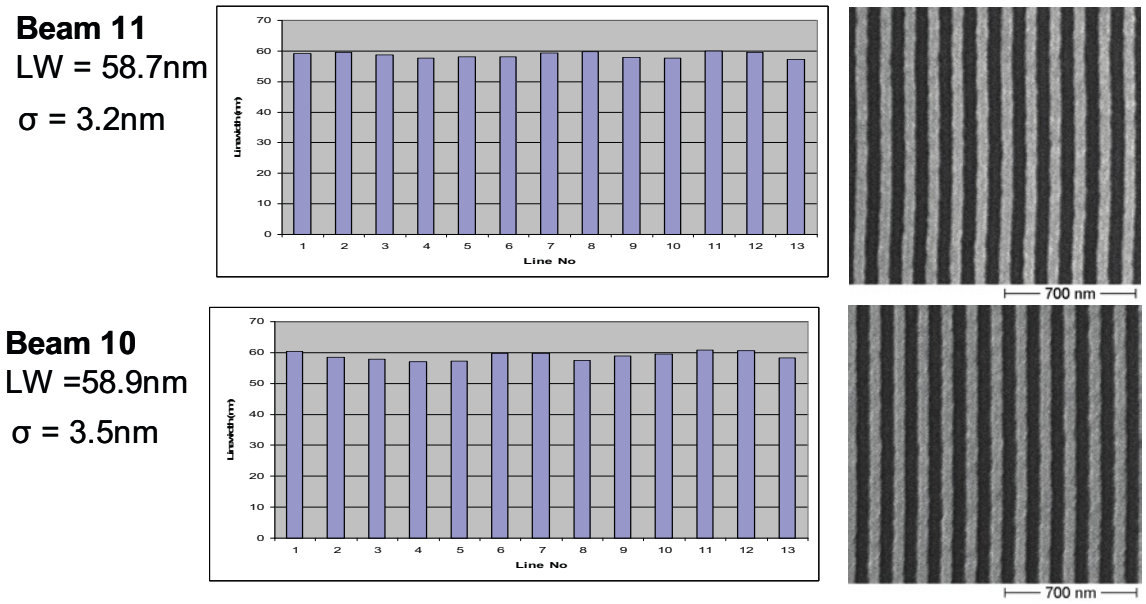


Figure 14: First exposure results in 50nm HSQ. 65nm hp lines and spaces (slightly underexposed).

As soon as the optimization of the PML2 Pre-Alpha Tool is completed, the new 2.5µm-CMOS-APS will be inserted and maskless multibeam patterning of 22 nm hp structures will be demonstrated.

5. PML2 Alpha Tool

Further development of PML2 is foreseen within the 7th European framework program (FP7) as part of the integrating project MAGIC[7]. Within MAGIC a PML2 Alpha Tool is being designed and realized, which can be operated at an end user site. The PML2 Alpha Tool will allow maskless e-beam lithography on 300mm wafers and device fabrication for the 32 nm & 22 nm hp (half pitch) technology nodes with in-situ die-to-die alignment and overlay capacity. Furthermore, it will be equipped with a large field programmable Aperture Plate System utilizing 256k beams and will exhibit full system integration. Together with the infrastructure developed within MAGIC, the PML2 Alpha Tool is destined to herald the introduction of mask-less lithography into the industrial environment.

Acknowledgements

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