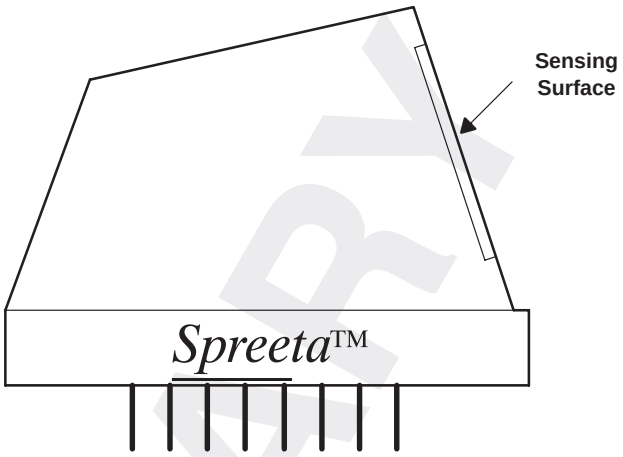
TSPR1A170100
Spreeta™ Liquid Sensor
Microcomponents Technology Center

SLYS009B – MARCH 2000

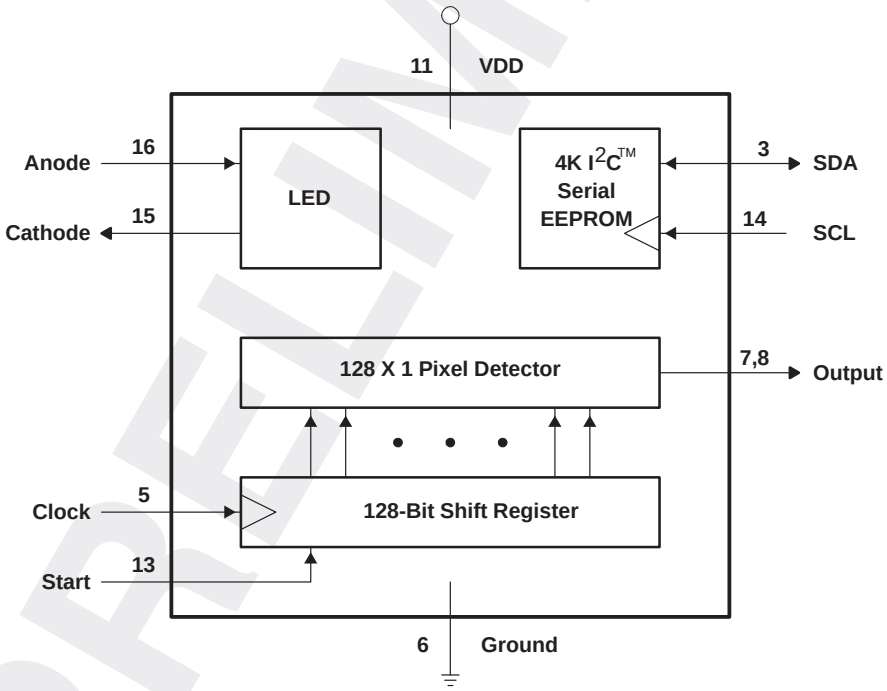
- **Real-Time Sensing**
- **Quantitative Analysis†**
- **Internal Fault Detection†**
- **On-Board Factory Set Calibration**
- **Robust Affordable Packaging**
- **Small and Lightweight**
- **Variety of Applications**
  - **Refractometry**
  - **Diagnostics**
  - **Quality Control**
  - **Distributed Process Control**



description

The Texas Instruments (TI) TSPR1A170100 *Spreeta*™ liquid analytical sensor allows you to measure the refractive index of liquids that come in contact with the sensing surface. This measurement is obtained using an ultrasensitive physical principle known as surface plasmon resonance (SPR). Electrical connections are made via pins that protrude from the bottom of the device. The pin configuration is similar to a standard 16-pin dual in-line device. The following sections provide detailed information.

functional block diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† When used in conjunction with processor board and *Spreeta* software

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Spreeta is a trademark of Texas Instruments.

Terminal Functions

TERMINAL NO.	TERMINAL NAME	I/O	DESCRIPTION
1	NC		No internal connection
2	NC		No internal connection
3	SDA	I/O	Read/Write calibration data
4	NC		No internal connection
5	CLOCK	I	Clocks the measurement and output cycles
6	GROUND		Device ground
7	OUTPUT	O	SPR information output (analog) (See Note 1)
8	OUTPUT	O	SPR information output (analog) (See Note 1)
9	NC		No internal connection
10	NC		No internal connection
11	VDD		Device power
12	NC		No internal connection
13	START	I	Initiates output cycle and internal reset
14	SCL	I	Clocks calibration data out or data in
15	C	O	LED cathode
16	A	I	LED anode

NOTES: 1. Pins 7 and 8 are connected together internally.

detailed description

The *Spreeta*™ sensor uses a physical principle called surface plasmon resonance (SPR) to measure the refractive index of liquids in contact with the sensing surface. The sensor consists of a light-emitting diode (LED), a sensing surface, and a light detector integrated into a unique optical package. Electrical connections are made to the sensor via pins at the bottom of the device. Detailed information on surface plasmon resonance can be found at http://www.ti.com/spreeta.

When a liquid comes in contact with the sensing surface and the appropriate signals are applied to the pins, the sensor provides an output that corresponds with the refractive index of the liquid. The output of the *Spreeta*™ sensor is a series of analog voltages, one per clock pulse, from which the refractive index of the liquid is derived when the voltages are digitized and processed with the proper algorithm.

The TSPR1A170100 *Spreeta*™ liquid sensor has a dynamic range of 1.320 to 1.368 refractive index units (RIU) with a resolution of 5 X 10^{-6} RIU. The physical dimensions of the *Spreeta*™ are shown in Figure 13 on page 14.

sensor operation

See the functional block diagram and Figure 1 for this discussion. Using the *Spreeta*™ sensor to measure the refractive index of a liquid requires the proper application of signals to the pins. See Figure 1 for a diagram of the measurement cycle. A pulse is applied to the START pin. On the subsequent positive edge of the CLOCK, the start pulse is clocked into the internal shift register initiating a reset cycle. Simultaneously, the data output cycle begins and the first data bit is presented to the OUTPUT pin. Data presented to the OUTPUT pin will always be data collected during the previous measurement cycle. An additional 127 clock pulses are required to complete the data output cycle. With each clock pulse during the data output cycle a new data bit is presented to the OUTPUT pin. One additional clock pulse, (129^{th}) is required to end the data output cycle and clear the internal shift register.

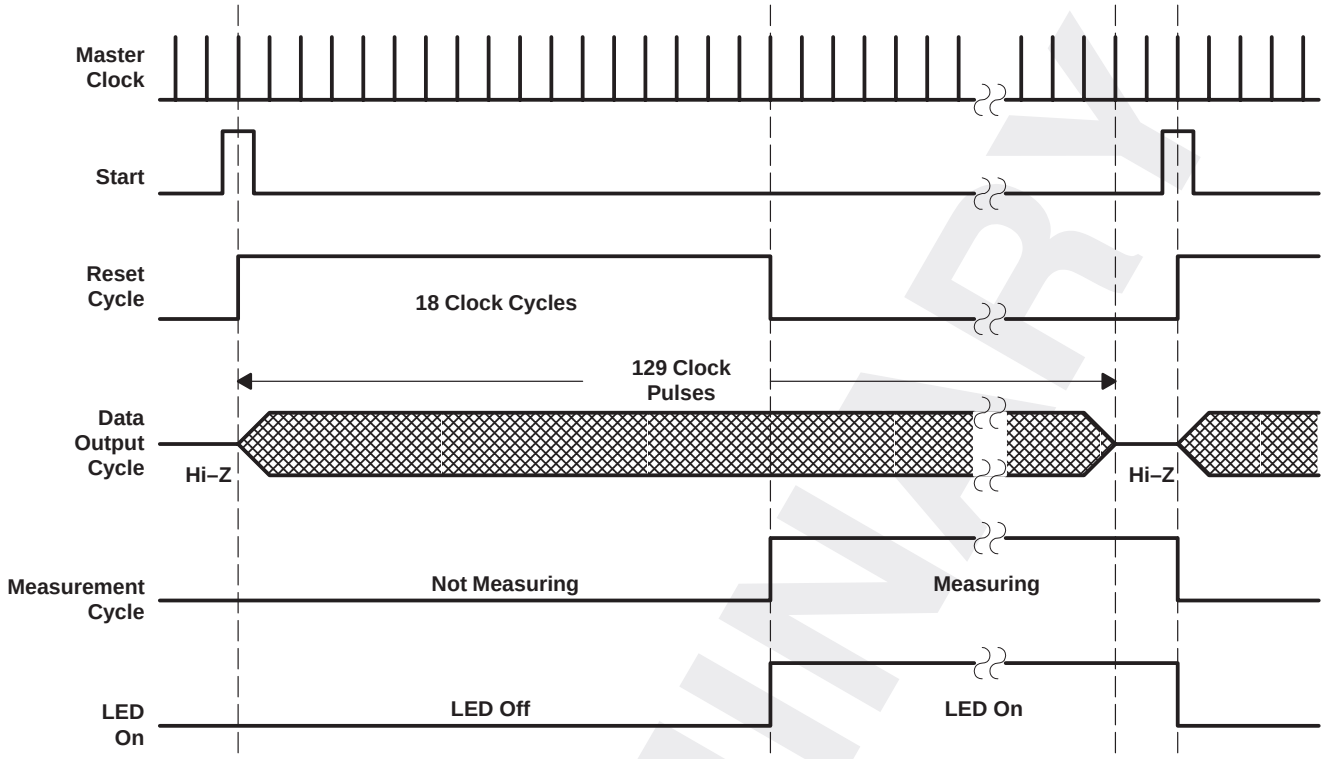

Figure 1. Timing Waveforms

The reset cycle continues for the first 18 clock pulses of the data output cycle. It is important that the start pulse go low before the second clock pulse in the data output cycle. Having more than one start pulse in the internal shift register is an illegal condition. After the 18th clock pulse, the reset cycle is complete and the measurement cycle begins. The measurement cycle continues until the next start pulse is clocked into the internal shift register. The minimum time allowed for the measurement cycle is 111 clock cycles (129 – 18 clock pulses).

After the 129th clock pulse of the data output cycle, the Clock may continue to run or be stopped. The measurement cycle continues with or without the presence of the Clock until the next start pulse is clocked into the internal shift register.

To measure a refractive index, the LED must be illuminated during the measurement cycle, although not necessarily for the entire measurement cycle. An external current-limiting resistor should be used to ensure that the LED does not experience excessive currents.

The output data consists of 128 bits of analog data from a charge mode linear array detector. The output voltage of each bit is a product of the measurement time and the LED illumination. The output voltage of each bit has a range of 100 mV (when the LED is off and the sensor is in a completely dark environment) to 3 V. The measurement cycle should be adjusted so that the average output voltage level of all 128 bits is 2.5 V with the LED illuminated, the sensor in a dark environment, and with no liquid on the sensing surface.

Texas Instruments offers the TSPREVM-0001 Evaluation Module, which provides the control, interface electronics, and software to operate the *Spreeta*™ sensor from a desktop PC or laptop computer. Developers interested in getting started with *Spreeta*™ sensing can find information about the EVM at the *Spreeta*™ web site.

Figure 2 illustrates operational waveforms for the *Spreeta*™ sensor.

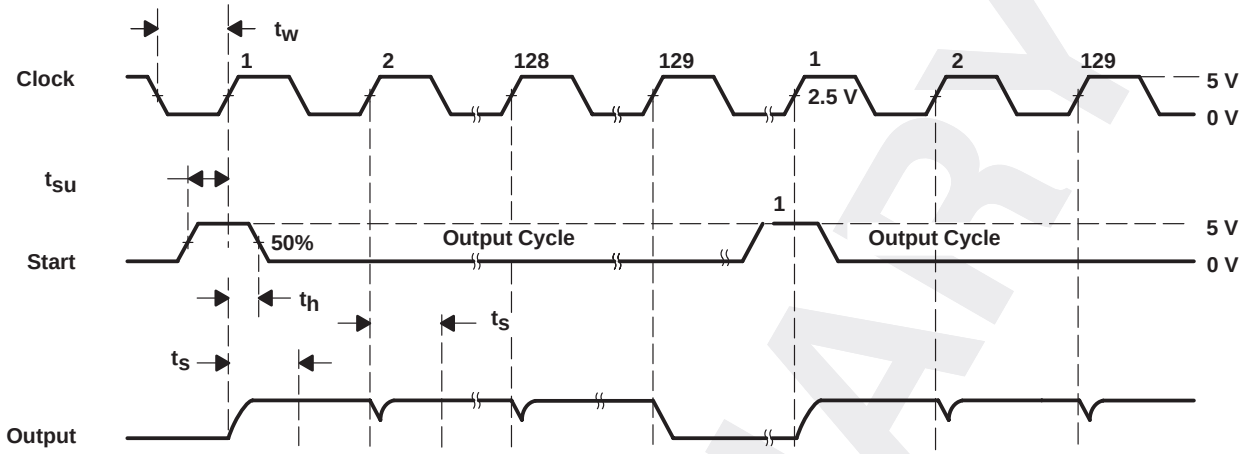

Figure 2. Operational Waveforms

absolute maximum ratings†

Supply voltage, V_{DD} . . . . . 7 V
Digital input voltage range, V_I . . . . . –0.6 V to VDD+1.0 V
Digital input current range, I_I . . . . . –20 mA to 20 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions, T_A = 25°C (unless otherwise noted) (see Figure 2 and Figure 1)

General	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5.0	5.5	V
High-level input voltage, V_{IH}	$V_{DD} \times 0.7$			V
Low-level input voltage, V_{IL}	0		$V_{DD} \times 0.3$	V
Measurement And Output Cycle				
Peak forward current, I_{PK} (See Note 2)	20		270	mA
LED forward voltage at 20 mA dc, V_f			1.7	V
Average power dissipation $P_{D(AVG)}$ (See Note 3)			50	mW
Start pulse setup time, $t_{su(ss)}$	0		t_w	ns
Start pulse, hold time, $t_{h(ss)}$ (See Note 2)	20			ns
Clock frequency, f_{CLOCK}	5	25	2000	kHz

NOTE 2: An external current-limiting resistor is required to avoid damaging the LED with excess currents.
NOTE 3: The current-limiting resistor should be selected to limit the current based upon the selected duty cycle.

performance characteristics at T_A = 25°C (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Refractive Index Range	TBD	1.320		1.368	RIU
Resolution	TBD		5×10^{-6}		RIU

NOTES: 4. Actual resolution varies depending upon the analog-to-digital (A/D) converter and algorithm used.

active-sensing region

The active-sensing region is an area of thin gold film that is actively used in liquid sensing. It is approximately 14.0 mm long by 1.0 mm wide on the face of the sensor (see Figure 3).

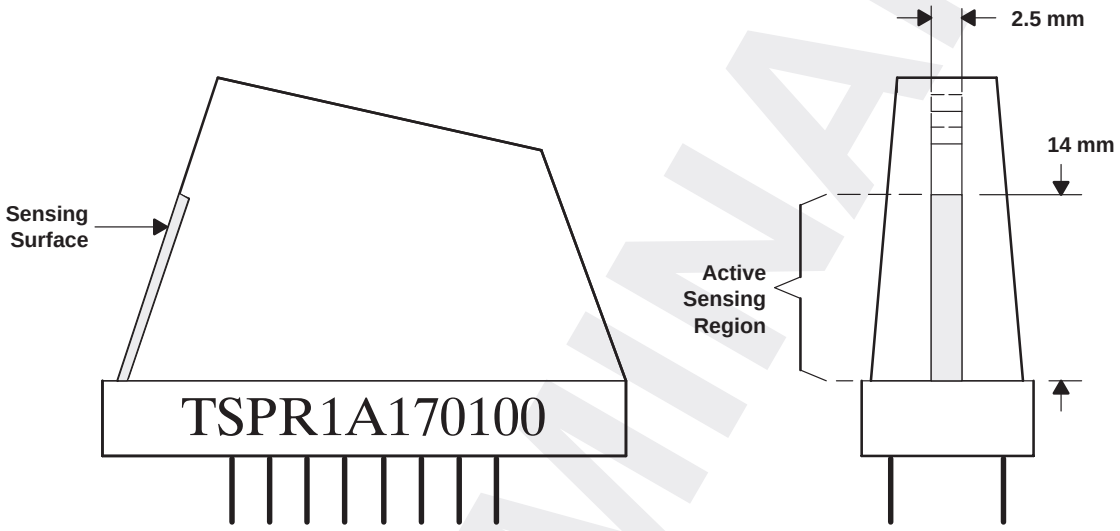

Figure 3. *Spreeta*™ Sensor Active Sensing Region

calibration data read/write

The TSPR1A170100 *Spreeta*™ sensor has been factory tested and calibrated. The initial factory-set calibration data is stored on-board the sensor in a 4K I^2C serial EEPROM. See Table 4 on page 12 for a description of the data stored on the memory chip. The following sections describe how to access the stored data and how to write new data to the memory.

functional description

The memory device protocol supports a bidirectional 2-wire bus and data transmission protocol.

bus characteristics

Bus timing data is shown in Figure 4 and Figure 5. Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is high. A change in the data line while the clock line is high is interpreted as a Start or Stop condition.

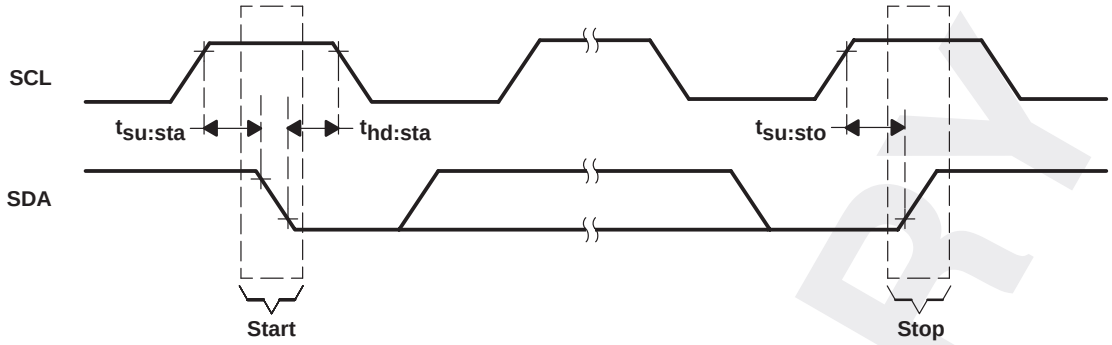

Figure 4. Bus Timing Start/Stop

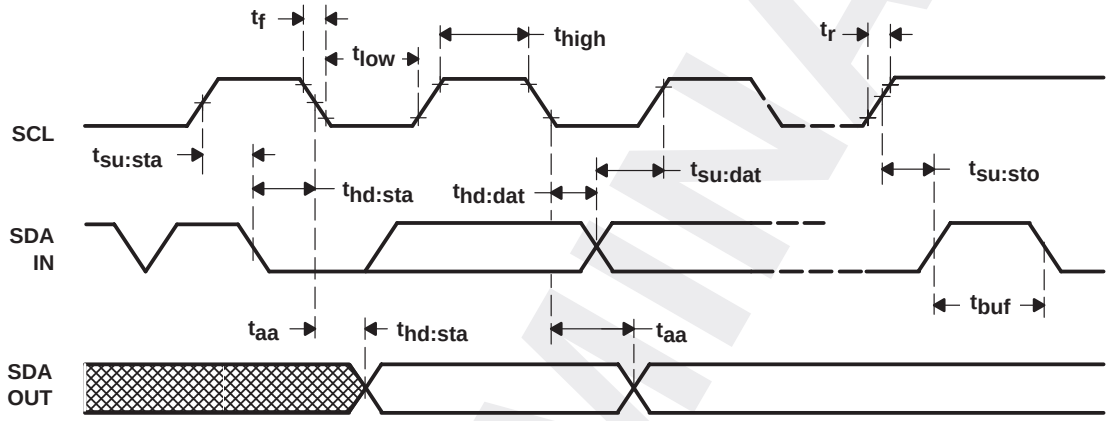

Figure 5. Bus Timing Data

bus characteristics (continued)

Calibration storage characteristics are listed in Table 1.

Table 1. Calibration Storage Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Clock frequency	f_{CLK}	–	100	kHz	
Clock high time	t_{HIGH}	4000	–	ns	
Clock low time	t_{LOW}	4700	–	ns	
Clock rise time	t_r	–	1000	ns	
Clock fall time	t_f	–	300	ns	
Start condition hold time	$t_{HD:STA}$	4000	–	ns	After this period, the first clock pulse is generated.
Start condition setup time	$t_{SU:STA}$	4700	–	ns	Only relevant for repeated start condition
Data input hold time	$t_{HD:DAT}$	0	–	ns	
Data input setup time	$t_{SU:DAT}$	250	–	ns	
Stop condition setup time	$t_{SU:STO}$	4000	–	ns	
Output valid from clock	t_{AA}	–	3500	ns	See Note
Bus free time	t_{BUF}	4700	–	ns	Time the bus must be free before a new transmission can start
Output fall time from V_{IH} min to V_{IL} max	t_{OF}	–	250	ns	See Note 1, CB ≤ 100 pF
Write cycle time	t_{WR}	–	10	ms	Byte or page mode

NOTES: 5. As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL. This is to avoid unintended generation of Start or Stop conditions.

bus conditions

Figure 6 illustrates the bus conditions.

The bus is considered not busy when both data and clock lines are high.

A Start condition occurs when a high-to-low transition occurs on the SDA line while the SCL line is high.

A Stop condition occurs when a low-to-high transition occurs on the SDA line while the SCL line is high.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. Data is valid after a Start condition when the data is stable during a high period of the clock cycle.

After receiving an address or data word, the memory acknowledges by responding with a zero on the ninth clock pulse.

start data transfer (B)

A high to low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

stop data transfer (C)

A low to high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

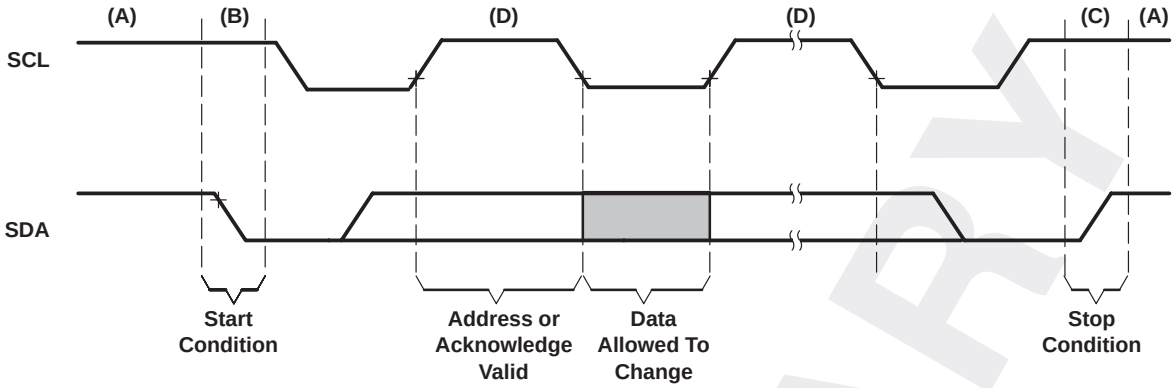

Figure 6. Bus Conditions

data valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device and is theoretically unlimited, although only the last 16 bits are stored during a write operation. When an overwrite does occur, it replaces data in a first-in first-out (FIFO) manner.

bus characteristics (continued)

acknowledge

Each receiving device, when addressed, must generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

NOTE:
The 24LC04B device does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. A master device must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master device to generate the Stop condition.

device addressing

The first byte sent after the Start condition must be the control byte. This 8-bit word is required to address the memory device. See Figure 7 and Table 2 for this discussion. The first four most significant bits (MSB) are the control code and they must always be 1010. The next two bits are *don't care* bits. The last bit of the control byte defines the operation as read (if set to 1) or write (if set to 0).

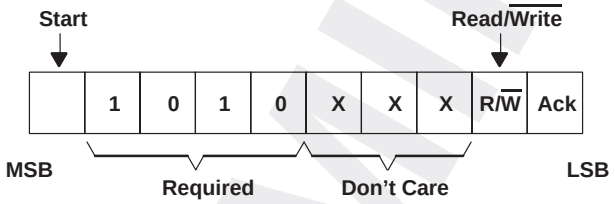

Figure 7. Control Byte Allocation

Table 2. Control Byte Operation

OPERATION	CONTROL CODE	BLOCK SELECT	R/$\overline{W}$
Read	1010	Block address	1
Write	1010	Block address	0

write operations

Byte write and page write operations are described here.

byte write

After a Start condition, a control byte with the R/$\overline{W}$ bit set to 0 is sent, which indicates to the memory device that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. The next byte transmitted is the word address and it is written into the address pointer of the memory device. After receiving another acknowledge signal from the memory device, the data word may be written into the addressed memory location. The memory device acknowledges again, and the master generates a Stop condition, which initiates the internal write cycle. During this time, the memory device does not generate acknowledge signals (See Figure 8).

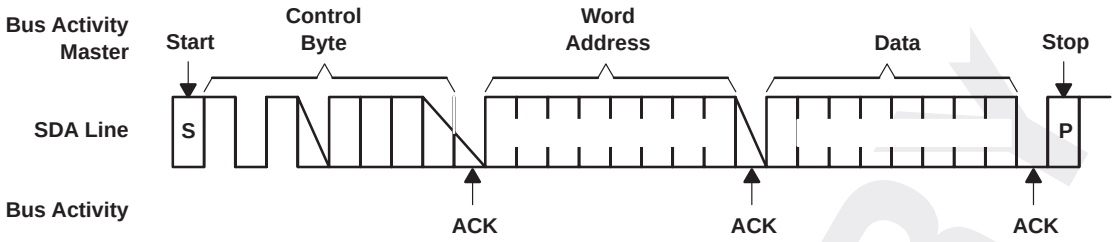

Figure 8. Byte Write

page write

To perform page write, the write control byte, word address, and first data byte are transmitted to the memory device in the same way as in a byte write. But, instead of generating a Stop condition, up to 16 data bytes are transmitted to the memory device, which temporarily stores them in the on-chip page buffer and writes them into the memory after receiving a Stop condition. After the receipt of each word, the four low-order address pointer bits are internally incremented by one. The high-order seven bits of the word address remain constant. if the memory device receives more than 16 words before generating the stop condition, the address counter rolls over and the previously received data is overwritten. As with the byte write operation, when the Stop condition is received, an internal write cycle begins (see Figure 9).

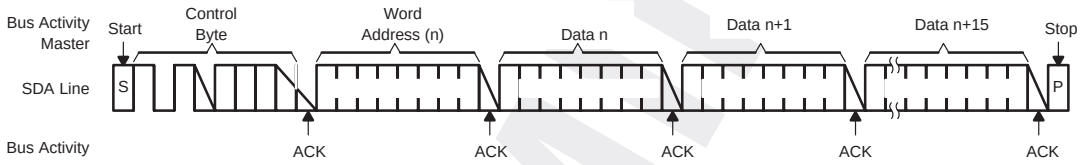

Figure 9. Page Write

read operations

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the control byte is set to 1. There are three basic types of read operations: current address read, random read, and sequential read.

current address read

The memory device contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the address with the R/$\overline{W}$ bit set to one, the memory device issues an acknowledge (ACK) and transmits the 8-bit data word. (see Figure 10).

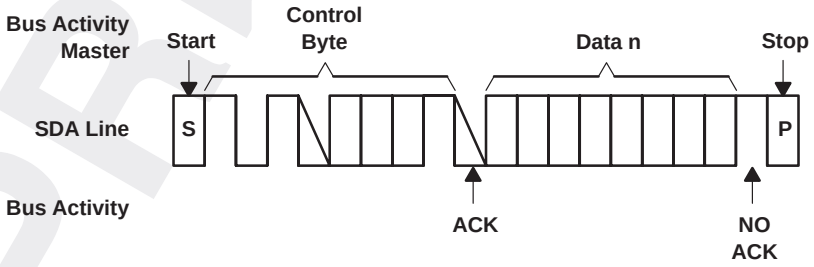

Figure 10. Current Address Read

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random read

Random read operations allow you to access any memory location in a random manner. To perform this type of read operation, you must first set the word address. This is done by sending the word address to the sensor as part of a write operation. After the word address is sent, you generate a Start condition following the acknowledge. This terminates the write operation, but only after the internal address pointer is set. Then, you issue the control byte again, but with the R/$\overline{W}$ bit set to one. The memory device then issues an acknowledge and transmits the 8-bit data word. You then generate a Stop condition, and the memory device discontinues transmission (see Figure 11).

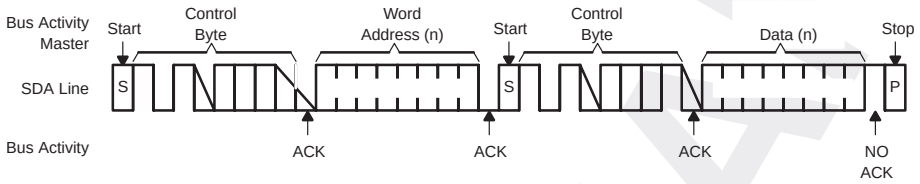

Figure 11. Random Read

sequential read

Sequential read operations are initiated in the same way as random read operations except that after the memory device transmits the first data byte, you issue an acknowledge instead of a Stop condition. This directs the memory device to transmit the next sequentially addressed 8-bit word (see Figure 12).

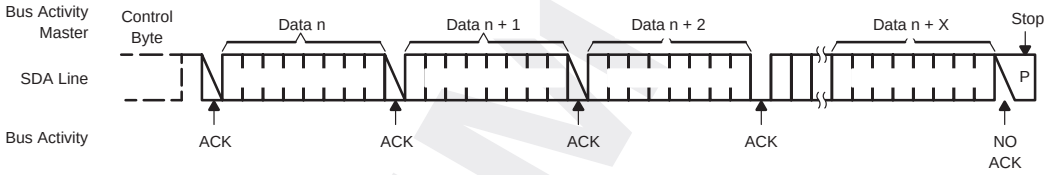

Figure 12. Sequential Read

To provide sequential reads, the memory device contains an internal address pointer that is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. Table 3 describes the memory map contents.

Table 4. Memory Map

MEMORY BLOCK	DESCRIPTION	# BYTES	# BITS	START BYTE	EXAMPLE
1	Air reference raw data	256	2048	1	128 pixels; 16 bits per pixel
2	Factory use only	5	40	257	N/A
2	Spreeta model number	10	80	262	TSPR1A170100
2	Chip ID number—Date code and serial number	20	160	272	12/31/2001, sensor #0 to 1,000,000,000 10 bytes + 10 bytes
2	LED setting (See Note 6)	1	8	292	0 to 15
2	Sensor integration time (See Note 7)	1	8	293	0 to 15
2	Factory use only	1	8	294	N/A
1	Moment level	1	8	295	0 to 255
2	Factory set calibration point 1	4	32	296	TBD
2	Factory set calibration point 2	4	32	300	TBD
2	Factory set calibration point 3	4	32	304	TBD
2	User calibration point 1	4	32	308	TBD
2	User calibration point 2	4	32	312	TBD
2	User calibration point 3	4	32	316	TBD

NOTES: 6. LED setting starts with 1 = 32-mA peak and follows a slope of approximately 0.0161 times N, which is 0.0017 mA, where N is the LED setting number. There is no internal current limit; hence, this number is for reference only.

NOTES: 7. Sensor integration time is the optimal time for achieving an average of 2.5 volts for all 128 pixels at a given LED setting. This number is for reference only.

care, handling, and cleaning

The *Spreeta*™ sensor is sensitive to high voltages, such as those produced by static electrical discharges. Normal handling is generally not a problem if you are properly grounded prior to handling the sensor.

Because the *Spreeta*™ sensing region that sustains the surface plasmon resonance is only a few hundred angstroms thick, handling of this surface must be done with care to avoid scratching and damaging it.

The integrated nature of the *Spreeta*™ sensor makes it rugged and shock resistant, but damage to the sensor can result from excessive bending of the pins, dropping the sensor, and exposure to excessive temperature changes.

ADDITIONAL INFORMATION

For details on the TI *Spreeta*™ liquid sensor and its components, see the *Spreeta*™ website at:

http://www.ti.com/spreeta

This website expands on the operation and application of the *Spreeta*™ liquid sensor, provides access to important documentation, and explains how you can order a *Spreeta*™ Evaluation Kit.

If you have questions or comments, please contact us through our website feedback form or email us at:

spreeta@ti.com

MECHANICAL INFORMATION

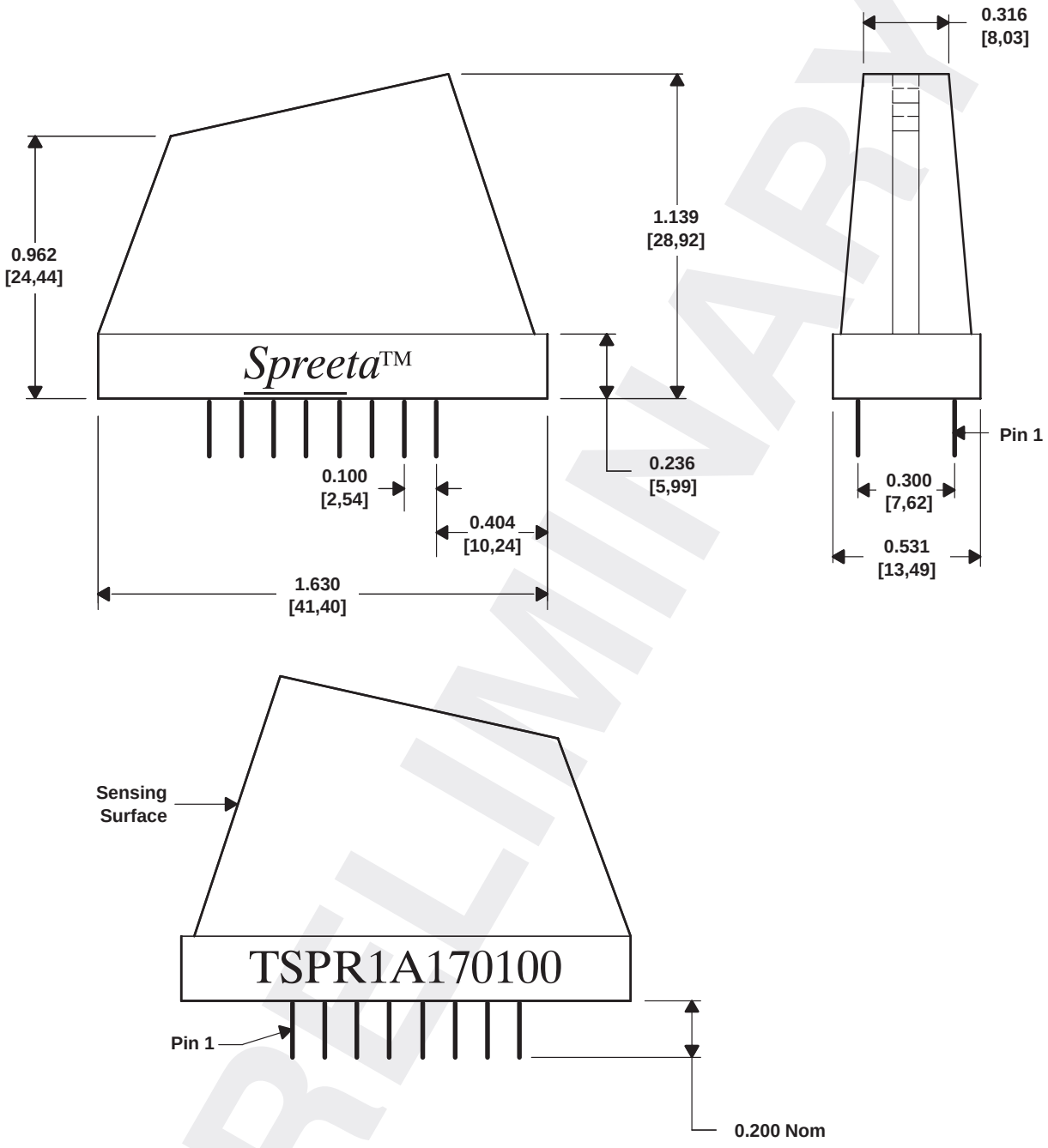

Figure 13. *Spreeta*™ Sensor Dimensions

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