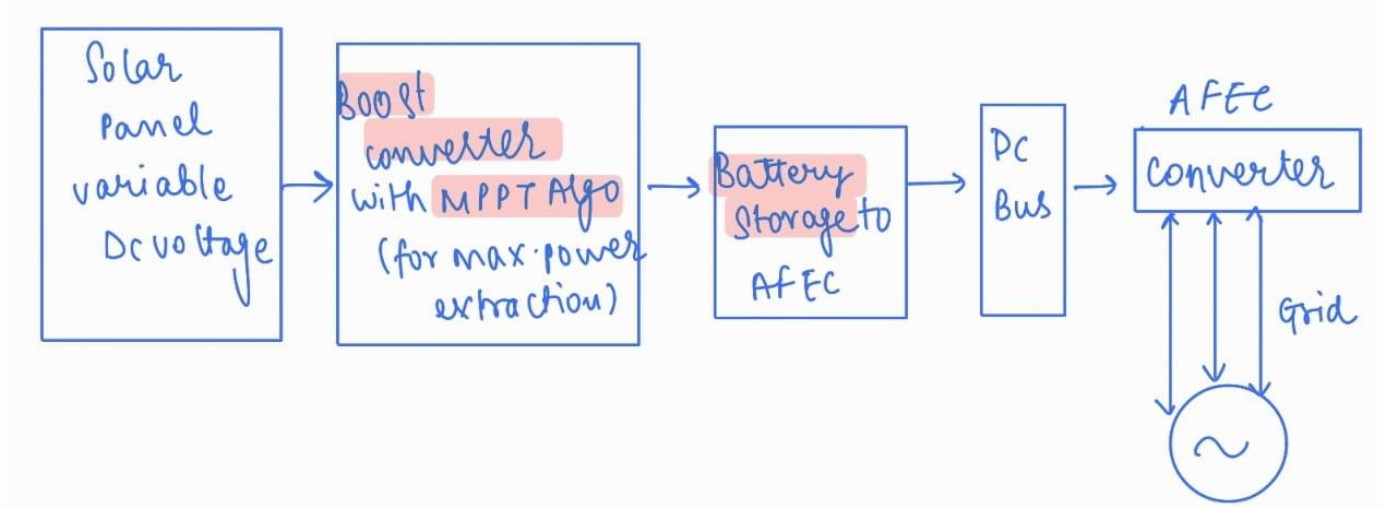
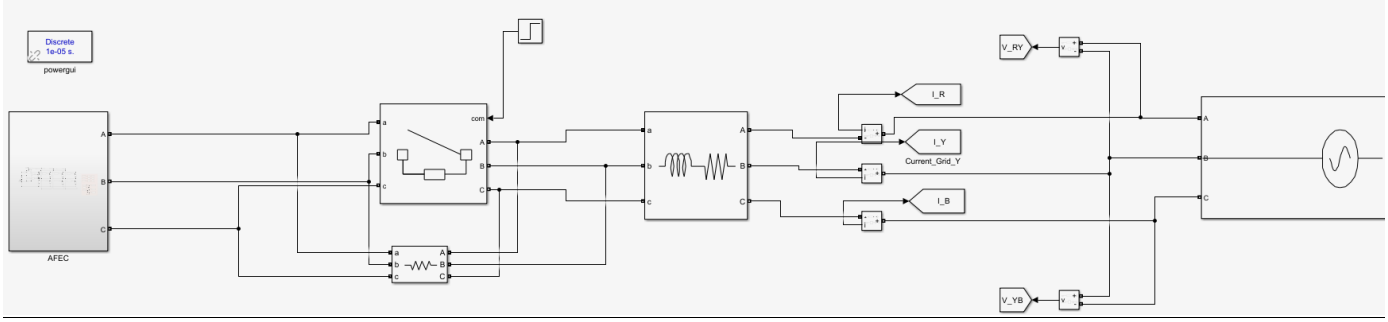
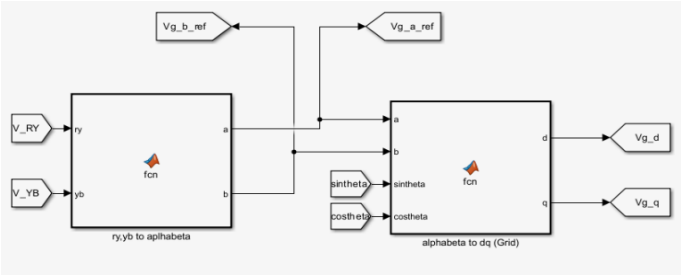
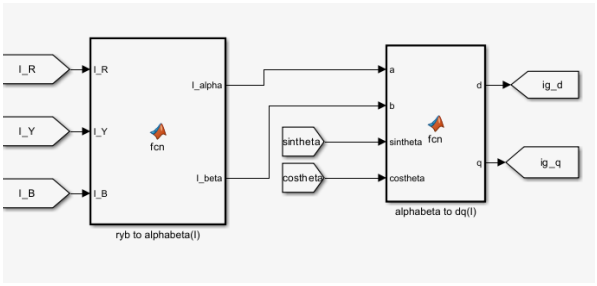
Suitable topology for the complete power generation unit



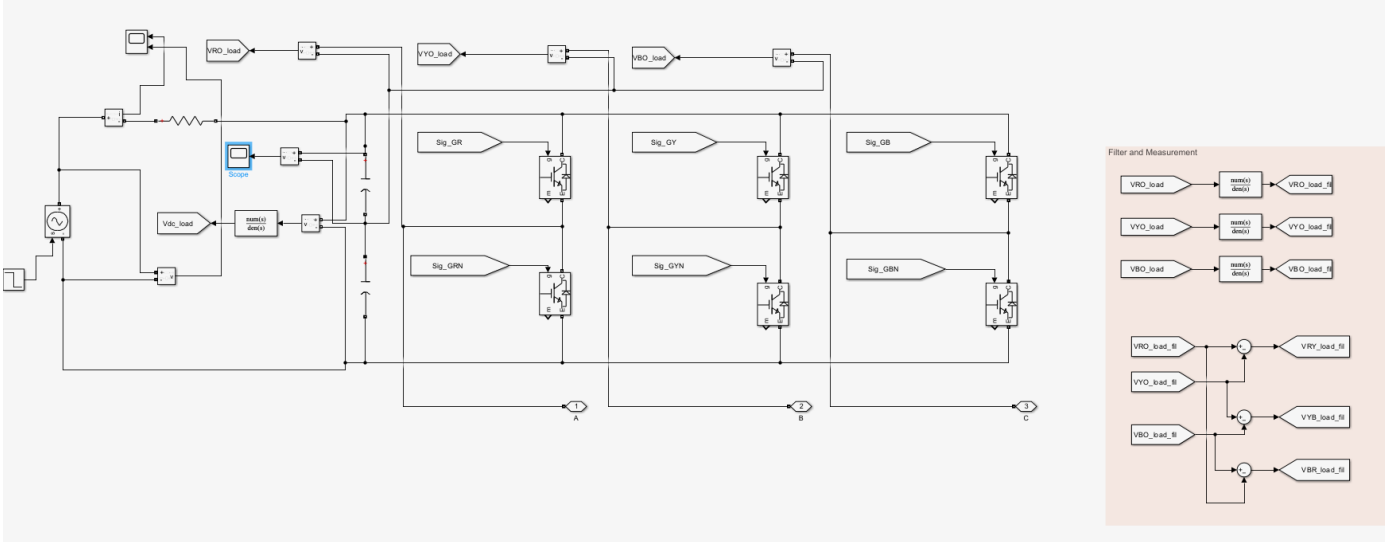


Grid Inverter Assembly

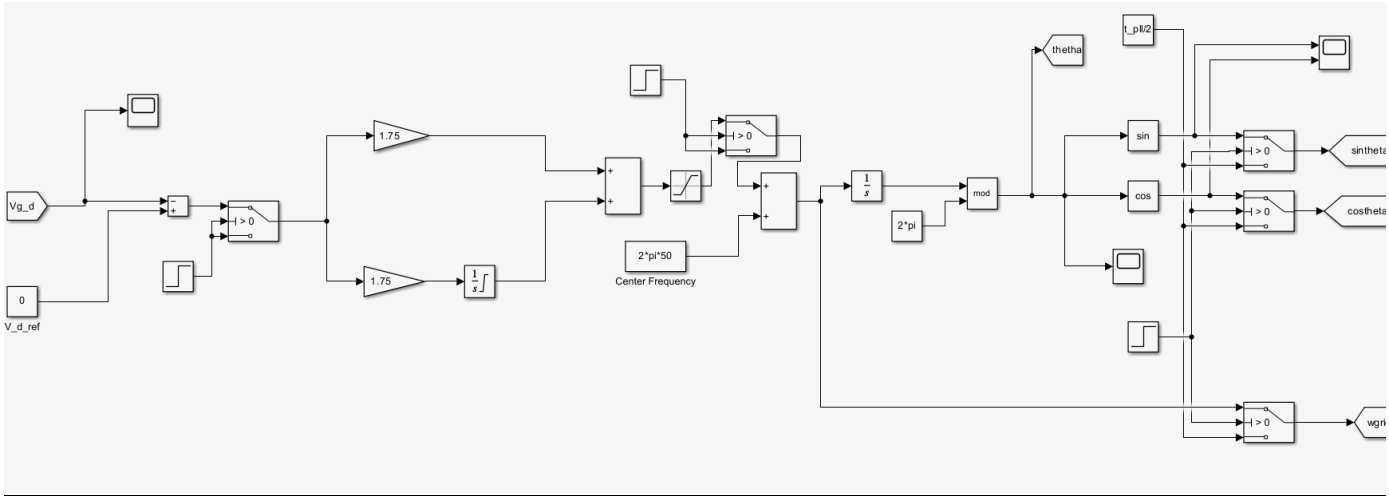




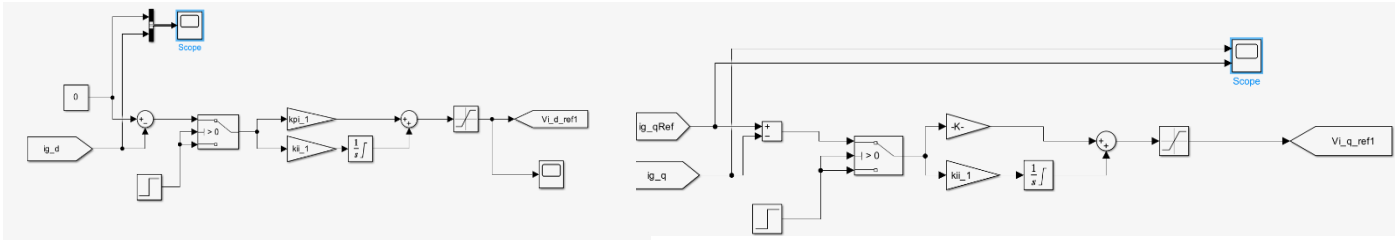
Conversion Blocks(MATLAB Functions)



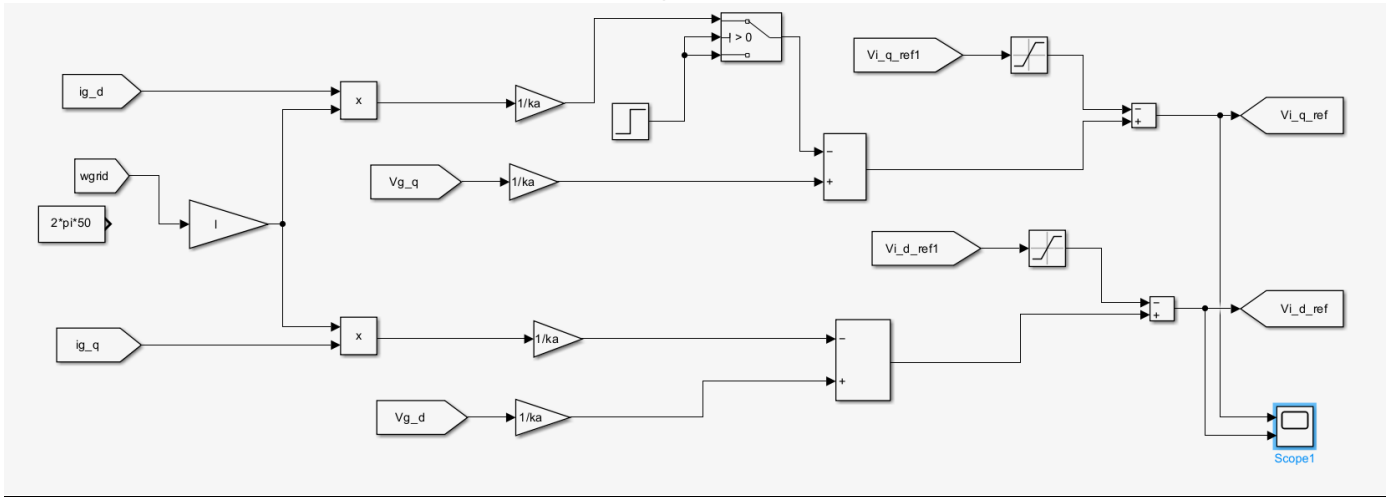
Active front end converter, Inverter Part



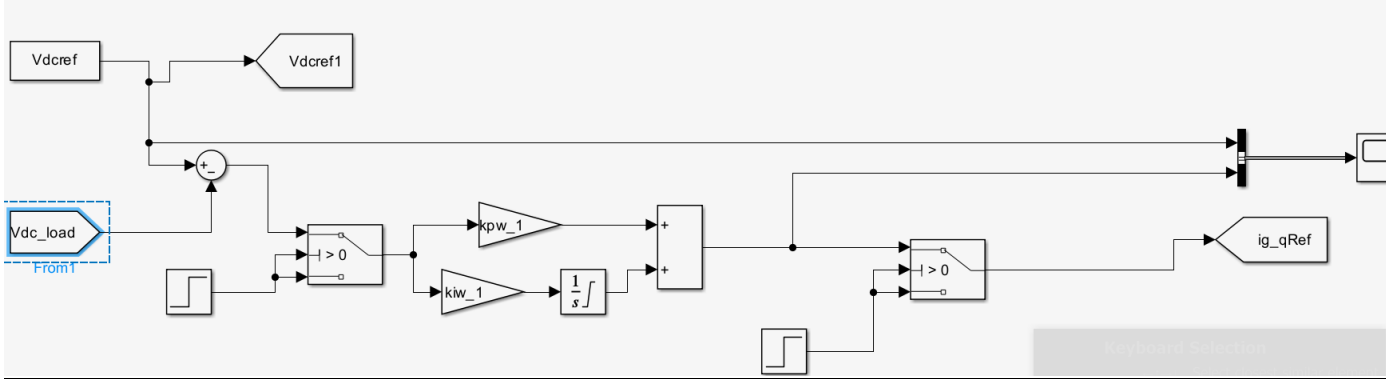
PLL



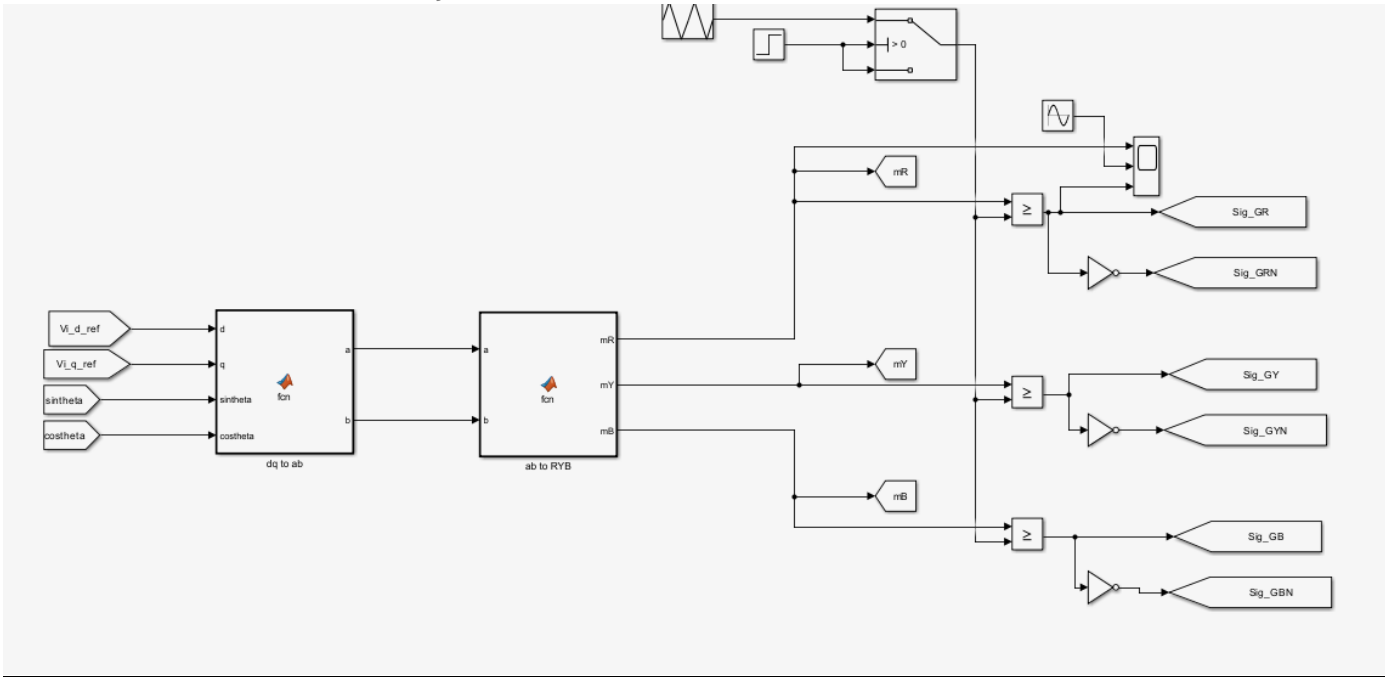
d-axis and q-axis Controller



Feed-Forward Compensator



DC Bus Voltage Controller



d-q to RYB conversion and then Generation of Gate signals for converter (PWM)

```
% Given power
P = 10e3;           % Power in watts

% Assumed and given voltages
Vbat = 800;         % Battery voltage (V)
Vll = 400;          % Grid voltage (V)
Vdcref = 757;       % DC reference voltage for modulation index m = 0.826

% Large capacitance to minimize voltage ripple
C1 = 750e-6;        % Capacitance in Farads

% Battery resistance calculation based on power and voltage differences
Rbat = (P / Vdcref) * (Vbat - Vdcref); % Battery resistance

% Angular frequency for a balanced 50Hz grid
w = 2 * pi * 50;    % Grid angular frequency (rad/s)

% Parameters for inductive reactance
l = 4.8e-3;           % Inductance in Henrys
r = 0.0045;          % Resistance in Ohms

% Gain factor for controlling d-axis current (based on Vdcref)
ka = Vdcref / 2;

% Precharge time, PLL time, and controller start times
t_precharge = 1;  % Precharge time in seconds
t_pll = 1.3;        % Time when PLL starts (in seconds)
t_c = 1.5;          % Time when current controller starts (in seconds)
t_v = 1.75;         % Time when voltage controller starts (in seconds)

% q-axis voltage for control
Vq = 1.5 * sqrt(2) * Vll / sqrt(3); % q-axis reference voltage

% Switching frequency and filter time constant
fsw = 5e3;        % Switching frequency (Hz)
tau_fl = 1 / 200;   % Filter time constant (seconds)
```

```
%% Current controller - d-axis current control loop parameters
% Set frequency for current controller, 1/10 of switching frequency
fbi = fsw/ 25;           % Frequency for current controller feedback
ka=Vdcref/2;
% Proportional and integral gains for the d-axis current controller
kii_1 = 2*pi*fbi*r/ka;              % Proportional gain for d-axis current controller
kpi_1 = 2*pi*fbi*l/ka;                % Integral gain for d-axis current controller

% Time constant for d-axis current controller, based on resistance and gain
tau_il = r / ka / kii_1;    % Time constant for d-axis current controller
```

```
%% Current controller - d-axis current control loop parameters
% Set frequency for current controller, 1/10 of switching frequency
fbi = fsw/ 25;           % Frequency for current controller feedback
ka=Vdcref/2;
% Proportional and integral gains for the d-axis current controller
kii_1 = 2*pi*fbi*r/ka;              % Proportional gain for d-axis current controller
kpi_1 = 2*pi*fbi*l/ka;                % Integral gain for d-axis current controller

% Time constant for d-axis current controller, based on resistance and gain
tau_il = r / ka / kii_1;    % Time constant for d-axis current controller
```

```
%% Voltage Controller - Parameters for voltage control loop
% Voltage control loop gain (ratio of q-axis voltage to reference DC voltage)
kl = Vq / Vdcref;             % Voltage control loop gain

% Total time constant for voltage controller, including filter and current control
tau_1l = tau_fl + tau_il;     % Total time constant for voltage controller

% Desired phase margin for the voltage controller (converted to radians)
PM = pi * 75 / 180;           % Phase margin (75 degrees in radians)

% Lead-lag controller parameter for voltage control
a_l = tan(PM) + sqrt((tan(PM))^2 + 1);  % Lead-lag parameter for voltage loop

% Proportional gain for voltage controller based on capacitance and time constant
% Integral gain for voltage controller, derived from lead-lag design
% Adjusted proportional gain for voltage controller, considering time constant and lead-lag design
kpw_1 =C1 / kl / a_l / tau_1l;   % Adjusted proportional gain for voltage controller
% Adjusted integral gain for voltage controller, considering the time constant and lead-lag design
kiw_1 =kpw_1 / (a_l^2 * tau_1l);     % Adjusted integral gain for voltage controller
```

```
%% PLL Controller
% PLL controller gain for phase-locked loop control
pll_gain = 1.75;               % PLL controller gain (value assumed)

% End of parameter setup
```

Parameters for the AFEC

The controller parameters are derived using analysis of bode plot where aim is to maintain system stability and improve bandwidth. The current controller gains (kpi_1, kii_1) are based on the system's inductance, resistance, and a frequency term fbi. The voltage controller gain kl is determined by the voltage ratio, and gains (kpw_1, kiw_1) are calculated using phase margin and time constants to ensure system stability. The PLL controller parameters are empirically set to 1.75 for phase tracking.

Working of the model and Inferences

PLL control turns on at 0.8 seconds, Current Controller at 1 sec and Voltage controller at 1.4 .
Because of different switching instants the various waveforms can be studied.

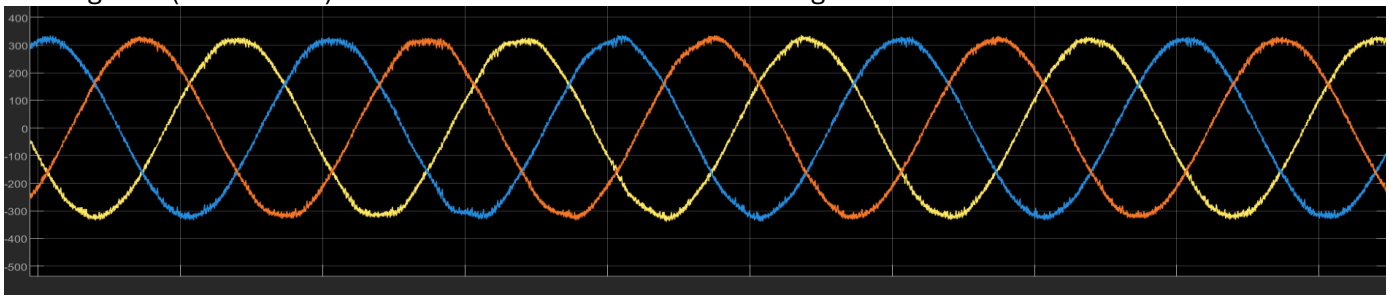
- As the stimulation Starts pre- charging takes place, capacitor gets charged and discharge with the grid voltage being supplied, As the Phase Locking Loop starts at 0.8 seconds there is some change and at around 1.2 seconds we can see that the output voltage on the inverter side is **in phase** with the grid input voltage and also **the magnitude is same**[1] (This is the task of PLL, important for **grid synchronisation** and **unity power factor** operation of the inverter, due to same magnitude, phase no reactive power transfer occurs from grid to load or load to grid; some ripples do exist in the inverter output voltage). Phase gets locked almost properly at 0.5 seconds
- At 0.5 sec the current controller comes into action and improves the settling of the DC reference voltage by tracking the **d and q components of the grid current**, A PI controller is utilised for tracking of d-axis and q-axis grid currents.
- Finally at 0.75 seconds the **voltage controller** comes into action which leads to selling of the **DC bus voltage to the desired value** and it then remains constant. Using large capacitors can smoothen the reference voltage, using smaller value capacitor could lead to some ripples in the dc voltage but the average value of the DC bus voltage will be as set in the reference only. **Feed-Forward compensation** is also done for the sake of maintaining the linearity of the system and rejecting any noise and disturbances and improving current and voltage regulation.
- To check the correct the Battery voltage is changed at 2 sec to 600 V from 800V (initial value), it is being observed that the **DC bus voltage remains fairly set** at the referenced value, but the **current in inverter changes direction**, that is the direction of current reverse in the DC load attached to the inverter(or DC bus, i.e. DC bus current reverses polarity). This implies that **power is being supplied by the grid to the load**, in contrast to the former case where active-power was being fed to the grid by settling the Battery voltage greater than the DC bus voltage.

Settling of Reference DC Bus Voltage

The voltage perfectly settles at around 0.76 seconds(0.01 second after switching on of current controller). Even after changing the voltage of battery i.e. change in the load the value remains constant (see around 2 seconds).
Value of DC bus voltage is Referenced at 757 V.
Modulation Index is =0.863

$$V = \frac{v_g\sqrt{2}}{\sqrt{3}} = \frac{mV_{dc}}{2}c$$

Here Vg=400 (Line-to-line) and m=0.863 and hence DC bus voltage is 757V.

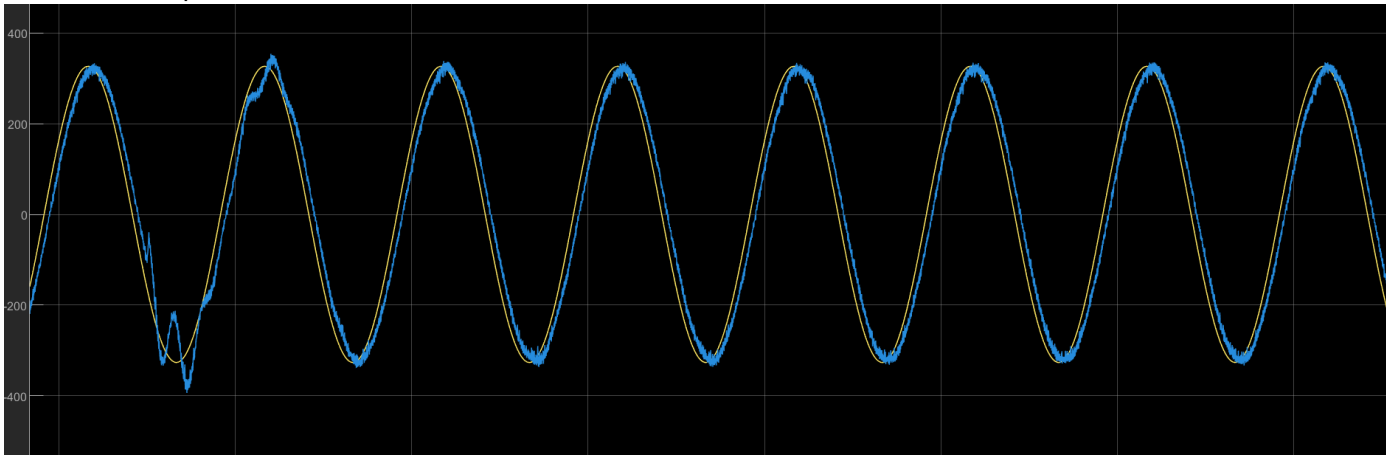


Inverter Voltage Waveform

[1] This could also be checked by checking the phase difference between beta component of grid voltage and cos thetha generated from PLL, they should be in phase

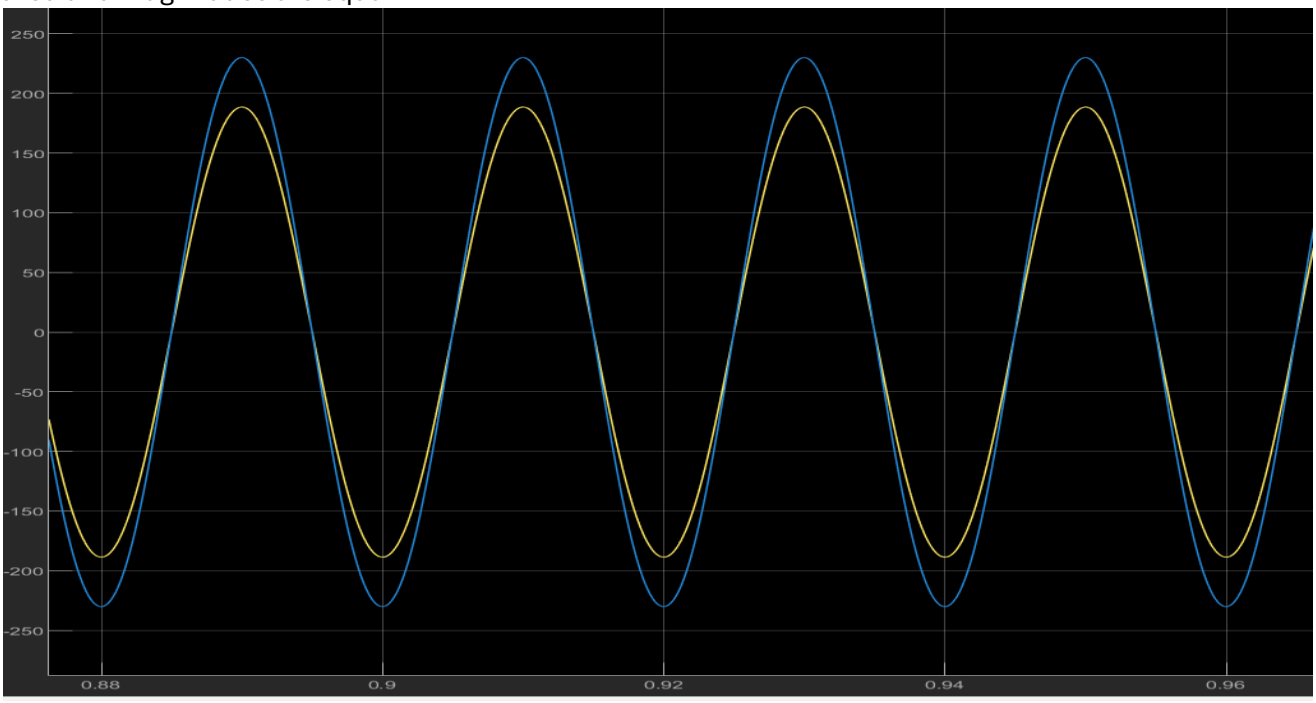
Value of Capacitor such that voltage ripple is within 5% of nominal voltage: 750microFarad

Grid-side output current THD should be restricted within 5 % under rated load conditions
For that value of Inductor: 5.8mH
Value of Resistance=0.015 ohm
System should maintain unity power factor under all operating conditions
This means one component out of d or q for the grid must be set to zero, This is done by using Phase Locked Loop, finally the voltage on grid and inverter side are qual in magnitude and in phase hence only active power transfer takes place.



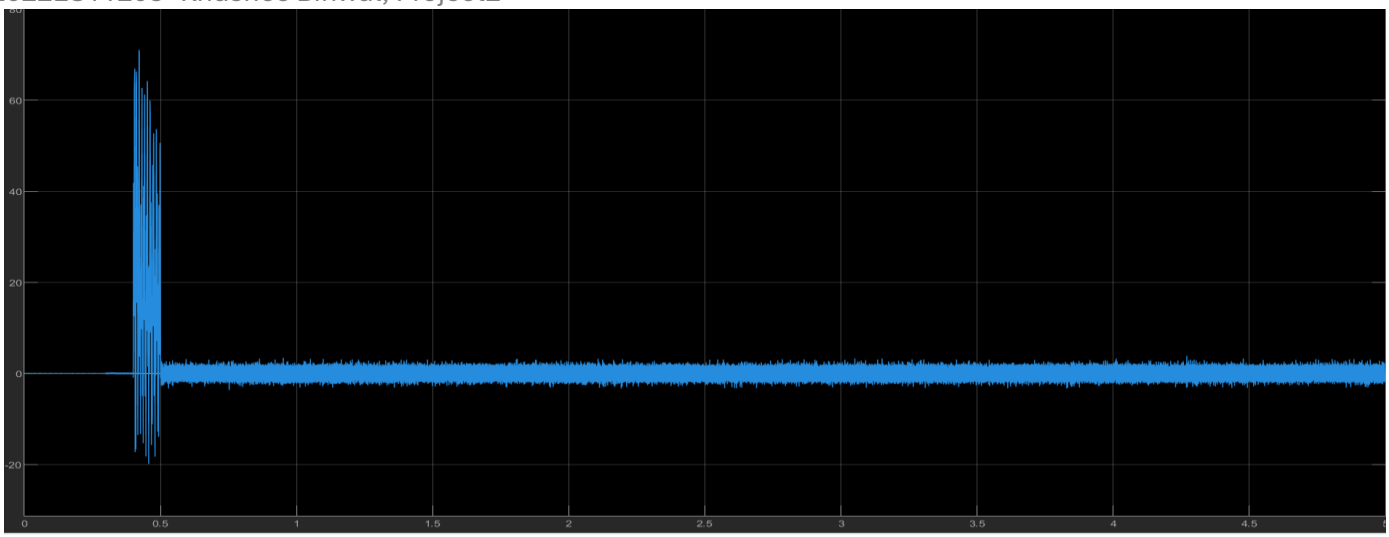
Grid Voltage (Yellow) and Inverter Voltage(Blue) in phase and locked

Slight disturbance occurs due to the switching on of the voltage controller. In steady state the phase are locked and magnitudes are equal.



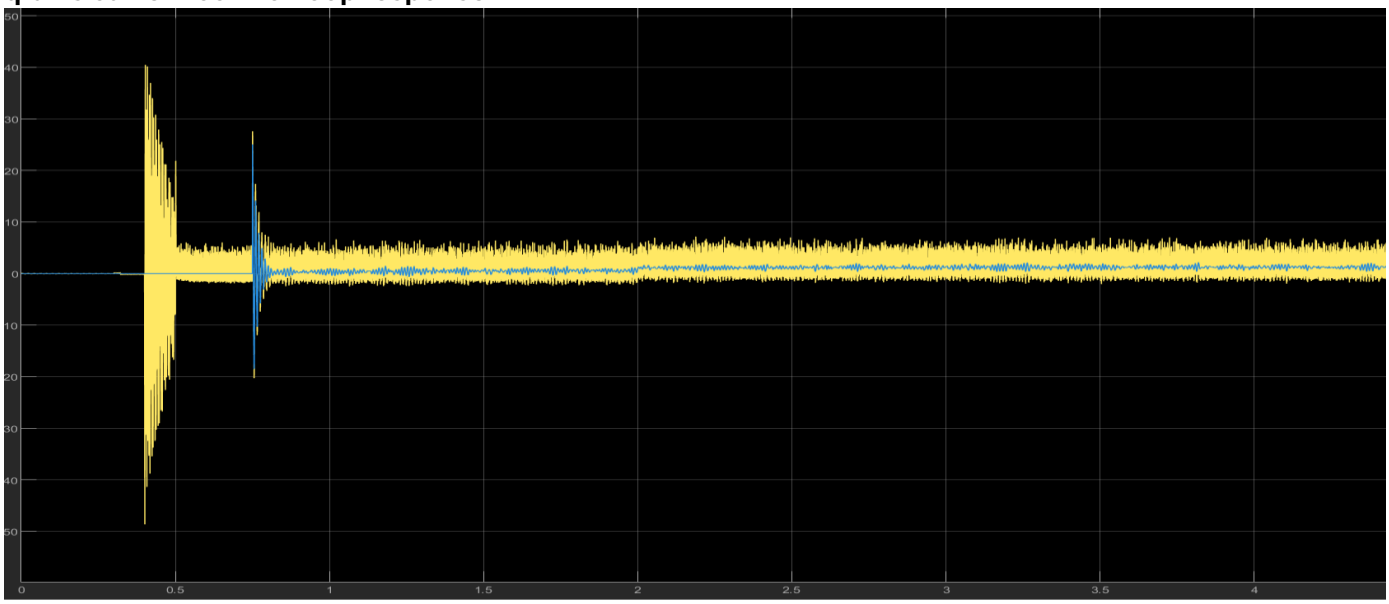
Costhetha generated and Vg_beta are in phase, another way to check accurate working of PLL

Response of d-axis current control loop



Value settles to 0 as referenced

q-axis current control loop response



The reference value(blue) is tracked(yellow) by the controller effectively