DP1.0 Summary Report
Group 12, ENSC 350
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1.0 Introduction

To whom it may concern,
We are writing to provide a progress update on the addition circuit design project (DP1) that we started last month. In this summary report, we explain our progress, timeline, and the issues we encountered so far. Our project is to design and evaluate an N-bit adder as a purely combinational Device Under Test (DUT), implemented and evaluated on FPGA targets. We are providing a concise progress update, evidence of milestone completion, and our plan to finish the remaining work.

In brief, we have implemented two adder topologies and verified functional correctness using file-driven test vectors and automated checking.

1.1 Background

Adders are fundamental components of datapaths and ALUs, and their design typically involves a trade-off between hardware cost (FPGA resources) and speed (critical path delay or maximum frequency). Because addition is used frequently in arithmetic-heavy systems, even small improvements in adder efficiency can meaningfully reduce overall area and improve system performance. For wide adders, carry handling dominates delay, which is why it is important to compare different carry strategies and evaluate how they map onto different FPGA families.

1.2 Purpose Statement

We wrote this summary report to refresh you on the project scope and to provide a concise progress update, including our current status, blockers, and next steps. The DUT specifications require a purely combinational N-bit adder (N is a power of 2) with inputs A, B, and Cin, and outputs S, Cout, and Ovfl for signed overflow. Our experimental procedure is to implement and simulate each design candidate using file-based test vectors to verify correctness, then synthesize each candidate in Quartus on Cyclone IV and Arria II to extract resource usage and timing for a cost–performance comparison.

Initial timeline: We started the main report Feb. 8th and scheduled it to be finished on Feb. 15th.
Summary report timeline: We started this summary report Feb. 6th and intended to finish it on Feb 14th.

2.0 Project Update

We have completed all programming tasks for DP1, including implementation of both adder topologies and integration of file-driven verification infrastructure. We are now organizing the final cost and performance evidence, including resource and timing summaries and normalized comparison tables, into the required concise format.

2.1 Milestones Reached

We have completed all required DP1 implementation and verification work. We implemented both adder topologies and all four design candidates for Cyclone IV and Arria II, and we verified correctness using file-driven test vectors with automated checking and readable simulation transcripts. We also generated Quartus compilation outputs needed for resource reporting and for building the final predicted-versus-measured, baseline-normalized cost tables.

2.2 Problems / Blockers

We also initially had uncertainty comparing cost across Cyclone IV and Arria II due to different resource units (LEs vs ALUTs/ALMs), but resolved it by using Cyclone IV LEs as the standard, estimating Arria ALMs as ALUTs/2, converting to LE-equivalent with k = 1.5, and normalizing to the baseline (155 LEs).

2.3 Workaround / Solution & Timeline

To finish DP1 analysis, we will finalize a consistent performance metric for all candidates (timing critical-path delay or constrained Fmax), then extract and compare timing results. We will also validate our Arria II cost conversion assumptions and update the cost table if needed. If time permits, we will test an additional design candidate to strengthen our final recommendation.

3.0 Conclusion

We have completed DP1 implementation and functional verification, including file-driven testbenches, automated checking, and transcript-based reporting. During integration, we addressed toolchain differences where ModelSim accepted code that Quartus rejected by updating the design to meet Quartus's stricter synthesis requirements. We also developed a consistent method to compare cost across FPGA families by using Cyclone IV logic elements (LEs) as the standard and converting Arria II results into LE-equivalent cost using our chosen normalization factor (k = 1.5), with all results referenced to the baseline cost of 155 LEs. Moving forward, our focus is to finalize performance extraction, validate remaining cost conversion assumptions if needed, and package the final normalized comparison tables and recommendation for submission.

3.1 Timeline Moving Forward

Next, we will (1) finalize the performance measurement approach and extract timing metrics for all candidates, (2) validate and, if needed, improve the Arria-to-Cyclone cost conversion, and (3) update the final comparison tables and recommendation based on the refined results.
Future timeline: Create a week by week schedule to make sure things are completed by Feb. 26

3.2 Final Statement

Thank you for your time; we will deliver the updated cost–performance comparison tables (with refined performance extraction and validated normalization) and a final design recommendation promptly.
Sincerely,
Group 12