Group #:
G12

Design Project 1

ENSC 350 1261

Project Submitted in Partial Fulfillment of the
Requirements for Ensc 350
Towards a Bachelor Degree in Engineering Science.

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DP1.0 Report Outline Document Structure:

Audience Definition:

- Shareholders and future investors.

Interests and Concerns of Audience:

- To find a suitable design candidate for an addition circuit.

Purpose of Report:

- To provide 4 design candidates meeting the Design Under Test (DUT) (Adder) specifications, outlining their design principles, topologies, and implementations.
- To provide functional verification results for each design candidate, derived through rigorous testing fulfilling the verification specifications.
- To provide a cost-benefit comparison between the design candidates, to allow the audience to select the best design candidate for their interests.

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1.0 Introduction

Content Rectangle 1.0.0 (Written Text): Identify the audience (Shareholders), give a short introduction

1.1 Background

Content Rectangle 1.1.0 (Written Text): Explain the motivation for making efficient addition circuits, and outline the specifications

1.2 Purpose Statement

Content Rectangle 1.2.0 (Written Text): Provide the purpose of the report

1.3 Experimental Procedure

Content Rectangle 1.3.0 (Written Text): Provide the functional verification procedure

Content Rectangle 1.3.1 (VHDL Code): Provide one, or several testbench code snippets which demonstrate crucial aspects of the functional verification procedure for the two topologies

Content Rectangle 1.3.2 (Image): Demonstrate the functional simulation results for the two topologies

2.0 Design Candidates

Content Rectangle 2.0 (Written Text): Give an overview of the four design candidates

2.1 Baseline Adder

Content Rectangle 2.1.0 (Written Text): Explain circuit theory for ripple adder (design principle), as well as design topology, and the design implementation on the Cyclone IV

Content Rectangle 2.1.1 (VHDL Code): Provide VHDL code snippet for ripple adder implementation

Content Rectangle 2.1.2 (Image): Provide Baseline RTL View

Content Rectangle 2.1.3 (Image): Provide Baseline Technology Viewer View

2.2 Design Candidate 1

Content Rectangle 2.2.0 (Written Text): Explain circuit theory for conditional sum adder (design principle), as well as design topology, and the design implementation on the Cyclone IV

Content Rectangle 2.2.1 (VHDL Code): Provide VHDL code snippet for conditional sum adder

Content Rectangle 2.2.2 (Image): Provide Design Candidate 1 RTL View

Content Rectangle 2.2.3 (Image): Provide Design Candidate 1 Technology Viewer View

2.3 Design Candidate 2

Content Rectangle 2.3.0 (Written Text): Ripple adder on Arria II: RTL, code, topology will be the same as Baseline. Mention this, and outline the differences only to avoid overlap
Content Rectangle 2.3.1 (Image): Provide Design Candidate 2 Technology Viewer

2.4 Design Candidate 3

Content Rectangle 2.4.0 (Written Text): CSA on Arria II: RTL, code, topology will be the same as Design Candidate 1. Mention this, and outline the differences only to avoid overlap
Content Rectangle 2.4.1 (Image): Provide Design Candidate 3 Technology Viewer View

3.0 Conclusion

Content Rectangle 3.0.0 (Written Text): Outline the purpose of the following sections

3.1 Performance Comparison

Content Rectangle 3.1.0 (Written Text): Explain how performance metrics are derived

Content Rectangle 3.1.1 (Written Text): Provide an analysis of the performance of the Baseline device

Content Rectangle 3.1.2 (Written Text): Provide an analysis of the performance of the three remaining design candidates

Content Rectangle 3.1.3 (Table): Illustrate the performance of each design candidate

	Baseline	Design Candidate 1	Design Candidate 2	Design Candidate 3
Speed				
…				
…				

3.2 Cost Comparison

Content Rectangle 3.2.0 (Written Text): Provide an analysis of the required FPGA resources of the Baseline device

Content Rectangle 3.2.1 (Written Text): Provide an analysis of the required FPGA resources of the three remaining design candidates

Content Rectangle 3.2.2 (Written Text): Provide a reasonable method for estimating the cost of an Arria II ALM compared to a Cyclone IV LE

Content Rectangle 3.2.3 (Table): Table of costs for comparison between design candidates

	Baseline	**Design Candidate 1**	**Design Candidate 2**	**Design Candidate 3**
Predicted Resource Usage				
Actual Resource Usage				
…				

3.3 Concluding Statement

Content rectangle 3.3.0 (Written Text): Give a final summary of results for candidates, as well as a cost-performance analysis for each design candidate