

# **Design Project 1.0 Report OUTLINE**

## **ENSC 350**

Group 12

Kane Zhan

Kirstin Horvat

Ben Britton

**DP1.0 Report Outline Document Structure:****Audience Definition:**

- Shareholders and future investors.

**Interests and Concerns of Audience:**

- To find a suitable design candidate for an addition circuit.

**Purpose of Report:**

- To provide 4 design candidates meeting the DUT (Adder) specifications, outlining their design principles, topologies, and implementations.
- To provide functional verification results for each design candidate fulfilling the verification specifications.
- To provide a cost-benefit comparison between the design candidates, to allow the audience to select the best design candidate for their interests.

## TABLE OF CONTENTS

---

<b>1.0 Introduction.....</b>	
<b>1.1 Background.....</b>	
<b>1.2 Purpose Statement.....</b>	
<b>1.3 Experimental Process.....</b>	
<b>2.0 Design Candidates.....</b>	
<b>2.1 Baseline Adder Performance.....</b>	
<b>2.2 Design Candidate 1 .....</b>	
<b>2.3 Design Candidate 2 .....</b>	
<b>2.4 Design Candidate 3 .....</b>	
<b>3.0 Conclusion.....</b>	
<b>3.1 Speed Comparison.....</b>	
<b>3.2 Cost Comparison.....</b>	
<b>3.3 Concluding Statement.....</b>	

## **1.0 Introduction**

**Content Rectangle 1.0.0: Identify the audience (Shareholders), abstract**

## **1.1 Background**

**Content Rectangle 1.1.0: Motivation for making efficient addition circuits, specifications**

## **1.2 Purpose Statement**

**Content Rectangle 1.2.0: Purpose of report**

## **1.3 Experimental Process**

**Content Rectangle 1.3.0: Functional verification procedure**

**Content Rectangle 1.3.1: Testbench code snippet**

## 2.0 Design Candidates

**Content Rectangle 2.0: Overview of design candidates, similarities, differences**

## 2.1 Baseline Adder

**Content Rectangle 2.1.0: Circuit theory for ripple adder (design principle), design topology, design implementation on Cyclone IV, prediction**

**Content Rectangle 2.1.1: VHDL code snippet**

**Content Rectangle 2.1.2: Baseline RTL View (Image)**

**Content Rectangle 2.1.3: Baseline Technology Viewer (Image)**

## 2.2 Design Candidate 1

**Content Rectangle 2.2.0: Circuit theory for conditional sum adder (design principle), design implementation, prediction**

**Content Rectangle 2.2.1: VHDL code snippet**

**Content Rectangle 2.2.2: Design Candidate 1 RTL View (Image)**

**Content Rectangle 2.2.3: Design Candidate 1 Technology Viewer (Image)**

### **2.3 Design Candidate 2**

**Content Rectangle 2.3.0: Ripple adder on Arria II: outline differences between the implementation here and the implementation for the Cyclone IV. RTL, code will be same Design Candidate 1**

**Content Rectangle 2.3.1: Design Candidate 2 Technology Viewer (Image)**

### **2.4 Design Candidate 3**

**Content Rectangle 2.4.0: CSA on Arria II: outline differences between the implementation here and the implementation for the Cyclone IV. code will be same Design Candidate 2**

**Content Rectangle 2.4.1: Design Candidate 3 Technology Viewer (Image)**

### 3.0 Conclusion

**Content Rectangle 3.0.0: Description of how the cost-benefit metric will be determined based on the functional verification results**

### 3.1 Speed Comparison

**Content Rectangle 3.1.0: Description of how speed was calculated**

**Content Rectangle 3.1.1: Table of speeds for each design candidate**

	Baseline	Design Candidate 1	Design Candidate 2	Design Candidate 3
Speed				
...				
...				

**Content Rectangle 3.1.2: Analysis of the findings**

### 3.2 Cost Comparison

**Content Rectangle 3.2.0: How is cost measured, comparison of resource utilization metrics, make reference to prior technology viewer images**

**Content Rectangle 3.2.1: Table of costs from compilations/flow report**

	Baseline	Design Candidate 1	Design Candidate 2	Design Candidate 3
LE/ALM Usage				
...				
...				

**Content Rectangle 3.2.2: Analysis of the findings**

### **3.3 Concluding Statement**

**Content rectangle 3.3.0: Summary of results for candidates, cost-benefit analysis for each design candidate**