Directory/Subdirectory	Filename	Description
./	DP1-FileList-G12-350-1261.pdf	Listing and short description of all files in the project
./	DP1.qpf	DP1 quartus project file
./	DP1.qsf	DP1 quartus settings file
./Documentation	DP1-Report-G12-350-1261.pdf	Project Report for DP1
./Documentation	DP1-Summary-G12-350-1261.pdf	Summary Report for DP1
./Documentation	DP1-VHDL-Listing-G12-350-1261.pdf	VHDL Sourcecode Listing
./Documentation	ProjectLog-G12-0049-350-1261.xlsx	Activity Log for Ben Britton
./Documentation	ProjectLog-G12-4645-350-1261.xlsx	Activity Log for Kane Zhan
./Documentation	ProjectLog-G12-9693-350-1261.xlsx	Activity Log for Kirstin Horvat
./Documentation/Images	N/A	Empty Directory
./Documentation/OutputFiles	DP1-Quartus-Summary-G12-350-1261.txt	Merged Summaries for the Four Design Candidates
./Documentation/OutputFiles	RCAN_Testing_Transcript_2026-02-15_21-32-20.txt	Human-Readable Testing Transcript for RCAN (N-bit Ripple Carry Adder)
./Documentation/OutputFiles	CSAN_Testing_Transcript_2026-02-15_21-32-10.txt	Human-Readable Testing Transcript for CSAN (N-bit Conditional Sum Adder)
./Simulation	CSANfv.do	Script for Functional Verification of CSAN (N-bit Conditional Sum Adder)
./Simulation	RCANfv.do	Script for Functional Verification of RCAN (N-bit Ripple Carry Adder)
./Simulation	ModelSim_DP1.cr.mti	Modelsim Project Configuration File
./Simulation	ModelSim_DP1.mpf	Modelsim Master Project File
./Simulation	TBCSAN.vhd	CSAN Testbench File
./Simulation	TBRCAN.vhd	CSAN Testbench File
./Simulation	waveCSAN.do	Script for Waveform Setup for CSAN testing in Modelsim
./Simulation	waveRCAN.do	Script for Waveform Setup for RCAN testing in Modelsim
./Simulation/Modelsim	N/A	Empty Directory
./Simulation/TestVectors	Adder00.tvs	Test Vector File for Functional Verification of Both Topologies
./Simulation/TestVectors	genTVDP1-1	Program for Generation of Test Vectors
./Simulation/TestVectors	verifyTVDP1-1	Program for Verification of Generated Test Vectors
./Simulation/Modelsim	N/A	./Simulation/TestVectors
./SourceCode	CSAN.vhd	Conditional Sum Adder for DP1 P3
./SourceCode	RCAN.vhd	Ripple Carry Adder for DP1 P2
./SourceCode	FA.vhd	Full Adder for DP1 P3
./SourceCode	FullAddr.vhd	Full Adder for DP1 P2
./SourceCode	Mux2c1b.vhd	2-Channel 1 Bit MUX
./SourceCode	Mux2cNb.vhd	2-Channel N Bit MUX
./SourceCode	Utils.vhd	VHDL Package File Containing Utility Functions for Testing