Silicon on Insulator Technology:

Advantages and Challenges

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***Abstract*— This report presents a brief description of silicon on insulator technology. We have tried to explain how wafers are manufactured by using this technology, its industrial need, techniques involved in it, benefits of this technology and finally the limitations of this technology. SOI technology has been able to carry Moore's law upto some extent, however it still has some limitations which have to be overcome in order to make this technology viable in future. Manufacturing techniques have been discussed briefly while advantages and challenges of the technology have been given importance. The last portion covers some points on the 20nm technology node in the SOI technology and the challenges faced in order to manufacture devices in this range.**

***Index Terms*— Moore's law, parasitic capacitance, latch up, wafer bonding, smart-cut, etch back, SIMOX, ELTRAN, floating body, recrystallization, grain boundaries, polysilicon**.

I. INTRODUCTION

With continuous enhancements in fabrication technology and demands for high speed, smaller chip area, better quality and durability of electronic devices, it has now become necessary to dig deep into crystals and wafers to further analyse and improve their electrical characteristics. This is done prevent undesirable effects from taking place which degrade the device performance. This requirement has led us to the Silicon on Insulator technology, where an insulating layer of oxide is developed on a silicon substrate and a third layer of silicon is deposited over it. With Silicon-On-Insulator wafers, transistors are formed in thin layers of silicon that isolates them from the main body of the wafer by a layer of silicon dioxide. The thickness of SiO_2 ranges from several microns for electrical power switching devices to less than 500 Å for high-performance microprocessors [1]. The structure comprises of a thin layer of silicon where the transistors are built, followed by an insulating layer of oxide below the first layer and finally a support of silicon wafer. The insulating layer is built of silicon dioxide material, usually referred to as 'BOX' which is an abbreviation for buried oxide. The report will, along with the advantages and challenges, also discuss briefly the methods for development of this buried oxide.

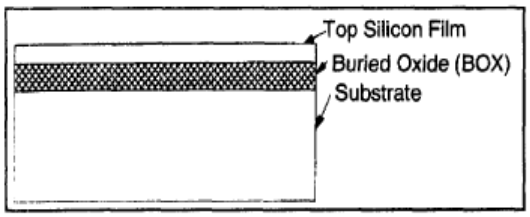

Fig. 1 Different regions of SOI [2]

II. NEED FOR SOI TECHNOLOGY

Early fabrication technologies which employed bulk silicon wafers suffered from parasitic effects. Also, junction capacitance which along with the other factors, limited the frequency response and switching speeds of the transistors on chip. These effects had to be minimized and the active region of the device was to be separated from the substrate body to avoid parasitic influence of the substrate. Moore's law which states that "the number of transistors on integrated circuits doubles approximately every two years", formed the basis of development of semiconductor technology. In order to attain these goals, it has now become trendy to develop such chips which can accommodate billions of transistors on them. However, for the technologies before SOI, it was difficult to increase the number of transistors on chip, simultaneously maintaining highest possible efficiency.

1) Extension of Moore's Law had become almost impossible for the then existing technologies.

2) The existence of a PN junction in the conventional bulk CMOS structure implies non-ideal behaviour. The barrier capacitance of the reverse-biased junction may significantly decrease the device operation speed.

3) The latch up problem- It is basically a short circuit path generated in a MOS circuit due to improper design which can damage the device. It was common in bulk CMOS circuits.

These factors led to the development of Silicon on Insulator technology.

III. TRANSITION FROM BULK CMOS TO SOI

The primary reason for this transition is the power consumption of scaled bulk CMOS technology. With the bulk CMOS technology, the effective channel length

does not work within the power constraints of the low-voltage applications as required. Since the circuit elements are isolated dielectrically, SOI technology on the other hand significantly reduces junction capacitances and allows the circuits to operate at high speed and substantially lower power at the same speed. The structure of the SOI device prevents latch up in circuit. It also improves the short channel effect.

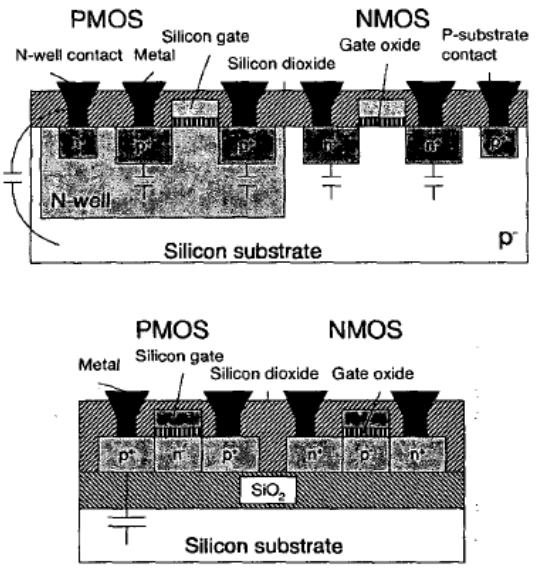

Fig. 2 Bulk CMOS vs. SOI [4]

The principal advances in the technology needed for the migration of CMOS devices to SOI based devices are the processes involved in fabrication of wafers and the architecture of the transistors.

These will be discussed as we proceed further. The major issues which were relaxed by SOI technology are-

1) The devices manufactured by this technology were inherently latch-up resistant.

2) When transistors were built on the thin top silicon layer, they ran at lower voltages and were much less vulnerable to signal noise from background cosmic ray particles.

3) Building circuits on SOI allowed for more compact chip designs, resulted in smaller IC devices and more chips per wafer.

4) Removal of p-n junctions between source-substrate and drain-substrate regions lead to elimination of capacitance which resulted in a reduction in the RC delay due parasitic capacitance, and hence a higher speed.

IV. DEVICE STRUCTURE

SOI devices are developed with very thin geometry. Initially single gate MOSFETs were developed which reduced the parasitic capacitance as well as the size of the structure [3]. For such films, metal gate is required in order to prevent high doping level in the channel and selective epitaxial growth had to be used for Source and Drain regions in order to reduce the access resistance. With a view to reduce constraints on SOI film thickness, multiple gate MOS devices have come up. This means that a single MOS transistor has more than one gate. This enhances the electrostatic performance of the device.

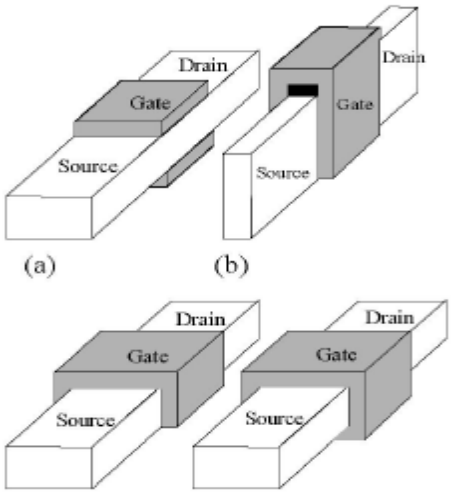

Fig.3 Multi gate structures [3]

The output efficiency for all the architectures depends on their geometry, like the SOI film thickness and the active area width.

V. PRODUCTION OF SOI WAFERS

SOI technology has its origin about three decades back when laser recrystallization was a popular method for the fabrication of 3D integrated circuits [1]. Although it suffered from grain boundaries, crystal disorientation etc. [1], it has now been improved and wafers with considerable efficiency can be generated. Zone melting recrystallization is another technique that is an enhancement over laser recrystallization with fewer defects.

There are a number of techniques used in SOI technology to produce wafers besides those mentioned above.

- Epitaxial Lateral Overgrowth
- Wafer Bonding
- Smart-Cut
- Bond and Etchback
- ELTRAN (Epitaxial Layer Transfer)
- SIMOX (Separation by Implantation of Oxygen)

These are some of the manufacturing techniques that are used to build devices based on SOI technology.

Smart cut process: In this process, a wafer called donor wafer is surface oxidized and then hydrogen ions are implanted into the wafer through the oxide layer. Then, this donor wafer is inverted and bonded with the handle

wafer. In the following step, the donor wafer is cut from the weak hydrogen-weakened zone. The thermal energy aids in the split of the two wafers. The donor wafers are polished and are again used for donating purpose to make another batch of SOI wafers. The process is based on the principle of blistering effect. The idea is to create a planar zone in the silicon wafer which is weak enough to break on the application of heat (400-500 degree Celsius). This would ease the cutting of the wafer once the donor and the handle wafers are adhered to each other. Hydrogen ions are implanted into silicon and these H+ ions create micro cavities. Also after a certain concentration, platelets are developed into the silicon wafer which tend to further trap hydrogen [7]. As a result during annealing of hydrogen induced wafers, micro cavities grow to form larger cavities and hydrogen diffuses from micro to larger cavities. This generates a dense hydrogen zone within the silicon wafer, which is easier to cut. An advantage of this process is that the donor wafer can be used many times as there is proper cleansing and controlled transfer of a layer of Si, hence the ultimate cost of the wafer is reduced.

Bond and Etchback: This process is specifically used when thick silicon dioxide layers, the thickness of which lie in between 10 and 100 microns, are required. In this process, two different Silicon wafers are initially oxidized and joined together on the oxidized surface to form one single structure. This results into a thicker oxide layer. The silicon wafer on the top is grinded, polished and etched to reduce its thickness. This process has a disadvantage that both the silicon wafers are completely consumed and there are no provisions for reusability unlike in the smart-cut process. Better thickness control can be achieved by using etch stop layers or at least depth markers [7].

SIMOX: It stands for Separation by IMplantation of OXygen. The idea is to implant sufficient amount of oxygen under a silicon layer while preserving the crystalline nature of silicon. The temperatures in the range 500-600 degree Celsius are suitable to avoid amorphization of the silicon layer under which the oxygen ions have to be introduced. In initial attempts to implement SIMOX, crystal damage was extensive. At room temperature, entire layer penetrated by the ions would lose its crystalline nature and become amorphous. Hence, to preserve the crystalline nature of layer to be penetrated, concurrent annealing is needed while the implantation is taking place. Very high temperature annealing is needed in order to enable reaction of oxygen and silicon. Annealing at 1405 degree Celsius for half an hour results into sharp and planar surfaces [7].The temperature at which wafer is placed during the implantation is also significant to achieve quality structure. It has been found that the implantation temperature of 600 degrees results into minimum dislocations.

Also to obtain thinner films, lower implantation energy and lower oxygen dose is needed. This also has an advantage of improving crystalline quality of wafers.

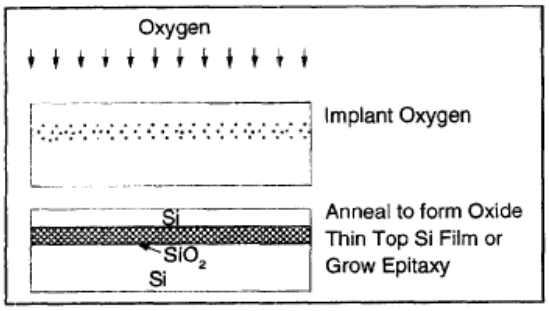

Fig. 4 preparation of SOI Wafers by SIMOX [2]

Wafer Bonding: SOI wafer bonding is based on the mechanism of chemical assistance through hydrogen bonds and water molecules. After RCA solution and water treatment, surfaces are coated with OH groups. These OH groups attract water molecules which hold the two surfaces together.

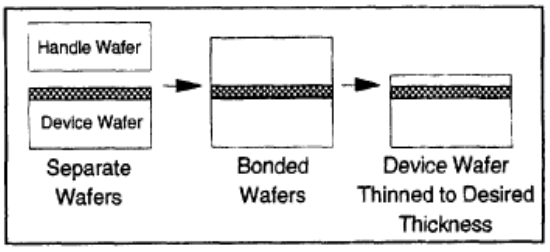

Fig.5 Preparation of SOI Wafer by Wafer Bonding [2]

There are a number of methods used for holding the surfaces together. Application of mechanical strength, passing of light along the interface between the two oxidized silicon wafers, heating the structure to remove water between the two adhered surfaces are some of the mechanisms by which the wafers can be generated.

ELTRAN: ELTRAN stands for epitaxial layer transfer. It is based on wafer bonding. A weak zone of porous Silicon formed by electrochemical processes is transferred from seed wafer to the handle wafer. For this to happen, porous silicon has to be sealed by thermal annealing in hydrogen. This temperature annealing greatly increases the mobility of silicon atoms which seal the pores at the surface of the substrate. This helps in improving the quality of substrate for subsequent growth. A slight mechanical stress along the porous Silicon layer is done for complete layer transfer [7].

VI. SOI BASED DEVICES

Before describing how SOI is used to produce MOS devices, we must understand what exactly is a floating body. In SOI technology, gate, source and drain are insulated from the substrate by a layer of silicon dioxide.

The body of each transistor is typically left unconnected and that results in a floating body. The floating body can get charged or discharged freely due to the transients (Switching) and this condition affects threshold voltage and many other device characteristics.

Partially Depleted MOS: When a positive voltage is applied to the gate of an N-MOS transistor, it depletes the body of p type carriers and induces an n type inversion channel along the surface of the body. However, if the insulated layer of silicon is made considerably thick, the inversion layer will not be able to occupy the body's full depth but can reach only partial depth of the body. Such a structure is called a partially depleted MOSFET and technology designed to produce such a structure is called partially depleted SOI technology. The thickness of the inversion layer depends on the body voltage. Lower initial body voltage results in a thinner inversion layer. However, a higher body voltage results in faster switching.

In this technology, the current body voltage depends on the history, i.e. previous values of voltages of source, drain and gate.

Fully Depleted MOS: When a positive voltage is applied to the gate of an N-MOS transistor, it depletes the body of p type carriers and induces an n type inversion channel along the surface of the body. If the insulated layer of silicon is made considerably thin, the inversion layer reaches full depth of the body. Higher channel mobility and hence higher performance are achieved, as well as lower variability from one device to another. Fully Depleted SOI enables a CMOS LP (low power) technology with un-doped body. It gives the best performance, low leakage couple, and hence a perfect choice for Low Power Applications.

Floating Body Effect: It is the dependence of body potential of a transistor designed with SOI as the producing technology on the history of biasing and carrier concentrations. There is a development of charge in the transistor's body against the insulated substrate. This stored charge may have adverse effects on the operational efficiency of the transistor like opening up of parasitic transistors in the structure, cause leakage currents; also in the case of DRAMs this can lead to information loss from memory cells. Floating body effect is also a cause of History Effect. History Effect is the dependence of threshold voltage of transistor on its previous states.

In order to avoid this effect, fully depleted MOS devices are used. This does not mean that partially depleted MOS are not in use. Partially depleted SOI devices are now used essentially in radiation hardness applications besides others.

History Effect perturbs the threshold voltage of the MOS transistor thereby causing variation in the circuit delay and mismatch between two identical devices. During the switching process of a transistor, the body voltages of the transistor will change from their previous state (steady or ideal) condition.

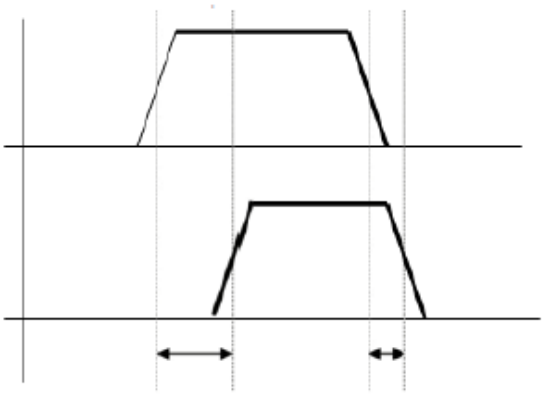

Fig.6 History Effect

Modelling Timing Parameters of the Transistor and Circuit considering the History Effect is critical for the success of Silicon technology. If a circuit is not active for long enough time to be in a steady state and then it switches, then this switching activity is called first switch. On the other hand, if the circuit is switching more regularly, then this is called second switch.

Due to floating body in partially depleted MOS and low substrate effect in fully depleted MOS, in a stack of transistors, the threshold voltage of the upper device results to be smaller than in the bulk, thus improving performance. The first switch is typically 20-30 % faster than in bulk, while the second switch is even faster. This is called Stack Height Effect.

VII. ADVANTAGES OF SOI TECHNOLOGY

SOI technology has a number of advantages over conventional bulk CMOS wafer manufacturing techniques. Latch up free operation, high speed of the circuits, reduced junction capacitance, radiation hardness, nearly ideal sub-threshold and improved drivability are some of the major advantages of SOI technology.

Firstly, the architecture of SOI devices has very low parasitic capacitance due to insulation between substrate and source and drain regions, this removes time constant of the capacitor (RC), thereby increasing the speed of operation of the SOI MOSFETs. Also, application of BOX results into reduction of amount of electrical charge to be transported by the transistor during switching operation; this enables the transistor to switch its state at less energy [5].

Secondly, since the circuit elements are dielectrically isolated, the transistor latch up is eliminated. SOI uses dielectric isolation to surround the entire device sides and bottom. Also, it has no wells into the substrate and therefore has no latch up. Figure shows the setup where latch up occurrence is very common.

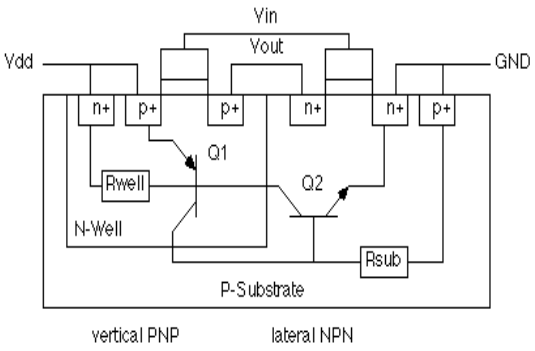

Fig. 7 Latch up in bulk CMOS

Here, the collector of each BJT is connected to the base of the other transistor in a positive feedback structure. Latch up can occur when both BJTs conduct, hence creating a low resistance path between V_{dd} and GND. If sufficient current flows through R_{sub} to turn on Q2, this will draw current through R_{well}. If the voltage drop across R_{well} is high enough, Q1 will also turn on, and a self-sustaining low resistance path between the power rails is formed. The result is circuit damage. In the case of SOI-CMOS devices, each element is completely isolated by BOX oxide film, so no parasitic thyristors are formed and the latch-up phenomenon does not occur.

Thirdly, due to the buried oxide structure, the source/drain regions of the SOI CMOS devices can be placed against each other without worrying about the possibility of latch up. Therefore, SOI CMOS devices may have a much higher device density [2]. Also, reverse biased junctions and well isolations are not needed in the SOI devices, hence, their power consumption is small. As a result, these devices are appropriate to design low-power circuits.

Fourthly, with the increased integration of digital and analog circuits on the same die, substrate noise issue is dominant in the bulk CMOS technology. Especially the digital noise can affect the sensitive analog circuits. In SOI technology, the Buried Oxide layer acts a die-electric barrier and it helps reducing Substrate Noise.

Leakage currents are reduced to minimum. Also, SOI CMOS devices are much less sensitive to high temperatures. Also, in fully depleted MOSFETs, threshold voltage variation with temperature is many times reduced. Manufacturing of multiple gate device has improved the electrostatic performance of the device. This also has led to the evolution of a new type of species in SOI CMOS, which is referred to as FINFETs.

Lastly, SOI improves the device performance by introducing strain in the device channel. To improve the mobility, channel has to be stressed by depositing certain layers. SOI technology incorporates the strain directly at the substrate level. This is based on the lattice mismatch between Si and SiGe. The first option is to fabricate a SOI substrate where the top silicon layer is bi-axially strained. SiGe layer is used to stress the Si layer deposited on top of the structure. At the end of the process, the SiGe layer is removed using the smart-cut process, leading to a strained-SOI wafer. Another option is similar to the above process, but the SiGe layer is not removed and hence, SiGe on insulator wafer is formed.

VIII. CHALLENGES IN SOI TECHNOLOGY

Although, SOI technology has a large number of advantages over conventional wafer producing techniques, but it is still in its development phase. There are still many debates going on around the globe for its further improvement. Semiconductor industry faces many challenges for efficient wafer production by SOI technology, some of which are history effect, bipolar currents, self-heating issues, inability of production of wafers with larger diameters etc.

A primary technology challenge is the mass production of SO1 wafers with large diameters, i.e. greater than 12" that too at reasonable cost.

There exists a dilemma in the choice of fully-depleted or partially-depleted MOSFETs. It is believed that partially-depleted SO1 MOSFETs are more user-friendly as they are a result of a slight manipulation of conventional bulk-Si technology. However, fully-depleted transistors have superior capability if they become more tolerant to short-channel effects [2].

Also, there are thin film issues. Thin-film SOI wafers are like the pseudo-MOS transistor where the Si substrate is biased as a gate to induce a conduction channel at the film-oxide interface. Source and drain probes are used to measure MOSFET characteristics from which most valuable material parameters are extracted [2].

As with the thin films, there exist mobility issues. As the thickness is reduced below 5-7 nm, mobility is reduced considerably. Thickness fluctuations also result in the degradation of performance of thin films. With the reduction in the thickness of the film, silicon doping becomes tougher. This is due to the amorphization of the silicon surface because of consistent doping.

There is a low gain parasitic bipolar transistor on every floating body SOI MOS transistor which is in parallel with the MOS transistor which could falsely switch on the MOS transistor. In this case, when source and drain are low, a pulse is seen at the output even when the gate is low; this is due to bipolar currents. This is referred to as kink effect. Kink effect worsens the differential drain conductance of the device and it is strongly dependent on the operating speed, which affects the performance of analog circuits.

Self-heating is a minor issue in SOI MOS technology. The BOX layer introduces a potential temperature difference between the devices. This is referred to as self-heating which becomes evident in the high power regions. This happens because proper heat sink is not

possible in the SOI devices because the structure is such that the heat cannot flow out.

Finally, multi gate structures use thin films for which very less resistance is needed. This has been a challenge for SOI technology. And last but not the least, good quality substrate materials are still under study which can be used in the SOI technology to give good characteristics.

IX. SUB 20-nm TECHNOLOGY

The SOI technology can be used in the 20nm technology node in the form of the fully depleted SOI (FDSOI). Although this field is still less known today as compared to PDSOI because it is still under research but we will see it in near future for sure. FDSOI presents many advantages over the earlier methods like higher immunity to the local variations and better electrostatic control.

Controlling Threshold Voltage: The use of the FDSOI devices, which are in the 20nm node, can provide with the ability to control the Voltage Threshold (V_T) value. In this case, the value for the V_T depends only on the gate material work-function and we need not control the doping. It has been found that the use of the Quarter gap materials can be helpful in this case.

Challenges: Initially when 65 and 45 nm nodes were analysed, it was found that the challenge for the further improvement would require improvement of materials as well as manipulation in device structures [5]. Then, multi-gate architectures came into existence that led to the growth of FINFETs. FINFETs were able to further minimize the node, but for successful 20 nm or even upto 15 nm nodes, fully depleted extremely thin SOI technology have to be used.

In ETSOI (extremely thin SOI), the transistor channel is kept undoped and so no masking processes are needed for the fabrication of transistors. However, the challenge lies in the fact that in extremely thin body devices, raised source and/or drain structures are needed. These raised structures generate parasitic capacitance when they come in contact with the gate. Although process like faceted epitaxy [6] is developed but still there is a need for further improvement in order to obtain desired results.

Future possibilities: It is estimated that the device scalability can be made to reach the 8nm node. But this is only possible by making use of the Buried Oxide (BOX). In ultra-thin Si and ultra-thin BOX structure, it is found that the short channel effect is further improved when a sufficiently-thin BOX is used. Without the use of the BOX, in order to reach the 8nm node technology, the thickness of the silicon film should be around 3nm. On the other hand, if the BOX is scaled down to 10nm, the thickness of the oxide film can be around 5nm. For reducing the technology node to below 8nm, nanowire type of the transistors have to be used.

X. CONCLUSION

This report considers all the major challenges in the field of SOI technology in addition to the benefits provided. We also saw how this technology can be used for 20nm node technology. The device design and the important effects like history effect and floating body effect were discussed. Thus, we saw that this technology can help us to overcome the drawbacks of the CMOS technology and design better and faster processors but still many features of this novel technique like FDSOI need to be explored. We hope that in the coming period of time we can see a new emerging technology which can fully replace the traditional bulk CMOS technology and would be able to fulfill the goals set on the basis of Moore's law.

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