Project Title: Single-Electron Devices

Course: Principles of Solid State Nano Devices

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Dr. M. Z. Kabir

By:

Khosa Komal Bir Singh (27135173)

Singh Karmvir (27159447)

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Abstract:

This report explains the use of single electron devices for designing alternatives to MOSFETs. The transistors today are reaching their limit because the size cannot be increased beyond a certain point. This is so because the problems like high capacitances come into picture when the size is decreased. Thus single electron transistors are being studied now a days. We studied few of the popular single electron devices, their fabrication and working. We also saw their merits like the small size, radiation withstanding ability etc. But there are also some demerits or problems related to this field like lithography process, background charge etc.

In a nutshell, it is established that these devices can prove to be an asset for the future technology. With the help of more research devoted to this topic, new techniques for their fabrication and use can be devised with can help eliminate the problems linked to them.

Introduction [1]:

The transistors replaced vacuum tubes because they had few features associated with them like low power consumption, low capacitances involved and faster speed of operation. Also the size of the transistors was much smaller than the tubes. Thus the device density is very high on a single chip. This fact is greatly being exploited in the technical field in order to manufacture smaller and smaller devices. But the scaling of the devices like MOSFETs is only possible upto a certain limit because after that the device starts showing the quantum effects. Thus there was a need to come up with a new manufacturing technique that can make us of this problem so that the size can be further reduced.

Thus a new type of devices making use of the discrete nature of tunneling electrons were introduced and these are called single-electron devices. They involve effects like Coulomb blockade. Theoretically, these devices should be capable of working at the limit of one transferred carrier per bit but this requires that the devices are synthesized very precisely so that the island are placed at the correct position with respect to the electrodes.

The heterostructures are used to achieve the **2DEG (2-Dimensional Electron Gas)** in **HEMTs (High Electron Mobility Transistors)**. For making the heterostructures using single electron principle, the 2DEG is patterned in this case using the electrostatic contacts i.e. the Schottky Contacts at the top of the device for creating small charged islands also called Quantum dot separated from the source and drain by tunnel barriers. The electron gas in this case is zero dimensional and has the property similar to that of the atoms and hence a name artificial atoms is given to this structure. Some of the earliest synthesized heterostructures had the problem that the islands were stretched over a larger distance so they had to be cooled to a cryogenic temperature of less than 1K for the single electron effects to be made useful. Thus there arises the need for making the islands in the sub-100nm range so as to able to use these devices at room temperature.

Having known now the general idea behind the single electron devices, we will now study about the various devices built using this technology and their fabrication in short. Silicon is the most important element for fabrication processes because of its many advantages like high abundance and high temperature withstand capability.

Si along with other elements like GaAs are already being used for the manufacturing of:

- Single electron transistors
- Switching devices
- Memory devices etc.

Coulomb Blockade in General Sense[1]:

The electrons are transferred from one island to the other and this can lead to the charging of the nearby grains and hence the electrostatic energy involved is given by:

$$E_C = \frac{e^2}{2C}$$

Where C is the effective capacitance of the island. Thus the electron transfer is only possible if this energy is overcome by the thermal excitations at temperature T given by:

$$T \sim T_0 = \frac{E_C}{k_B}$$

Or by the external voltage V given by:

$$V \sim V_t = \frac{E_C}{e} = \frac{e}{2C}$$

This suppression is known by the name Coulomb Blockade (CB). As the voltage is increased beyond V_t, the electron can tunnel through the barrier and only one electron can tunnel at a time until the voltage has been increased by an amount $\Delta V = e/C$.

Types of Single Electron Devices:

As we have already mentioned in the introduction part the various devices that can be constructed using the single electron concept, the list can yet be expanded. This concept can also be used in the field of metrology. In this section of the report we will look into the various types of the devices possible with this technique and also their fabrication processes in short.

1. Single Electron Transistor (SET) [2]:

- The MOS transistors are already reaching their limits since the channel length cannot be reduced beyond a certain point. This is so due to the other effects like surface capacitance, velocity saturation etc. that come into picture as the channel length is reduced more and more. Thus the future is seen in the single electron devices which use a quantum dot instead of the channel and hence making the device much smaller.
- The energy levels are quantized in these devices due to the quantum effects involved.
- Due to the absence of the channel, the device size is reduced. The quantum dot is placed in between the source and drain as the reservoirs and the tunneling junction is made of aluminium.

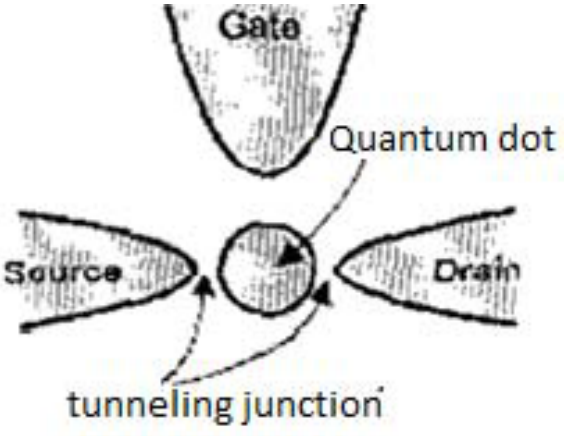


Fig 1 [2]: Quantum Dot in SET

- There is an inverse relation between the quantum dot or island size and the energy level spacing of the electrons. The energy level has either one or no electron. The relation that holds here is:

$$E_n = \frac{1}{2m^*}\left(\frac{h\Pi N}{d}\right)^2$$

Here d is the diameter of the island, m^* is the effective mass of the electron, h is the plank's constant and N is the quantum number of the energy level.

- Due to the quantum mechanism involved here, each of the energy level can only hold integer number of electrons and the electron gains or loses energy depending on whether it jumps to higher level or lower level respectively.

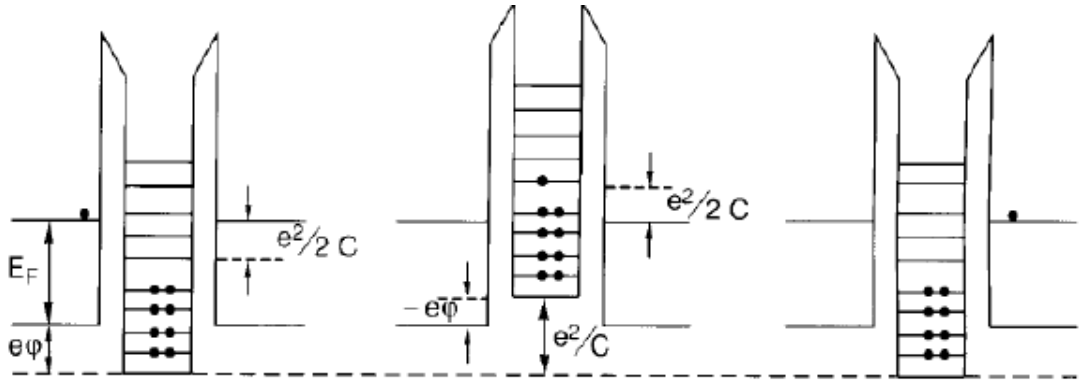


Fig 2 [2]: Energy Level Representation and Moving of Electron from Source to Island to Drain

- The probability of finding the electron in any of the energy state is given by the Fermi-Dirac relation:

$$f(E - E_x) = \frac{1}{1 + \exp\left(\frac{E - E_x}{kT}\right)}$$

Here k is the Boltzmann's Constant, T is the temperature, E is the energy of the particular energy level under study and E_x is the energy on the left or right of the island.

a. Fabrication [3]:

In this part we will study the fabrication process involved in the synthesizing of the Si SET. The method discussed here involves the use of the Silicon on Insulator (SOI) type substrate. Earlier it was not possible to observe the single electron effects at high temperature due to

large size of the island but now the observation is possible at high temperature of 100K. This has been made possible by reducing the size of the islands.

Miniaturization also involves reducing the size of the other components in the device like wires etc. in addition to the island size.

- Fabrication method used for this case is called Pattern-dependent oxidation (PADOX). The basic Si pattern used here is shown below. The pattern actually is a type of SOI.

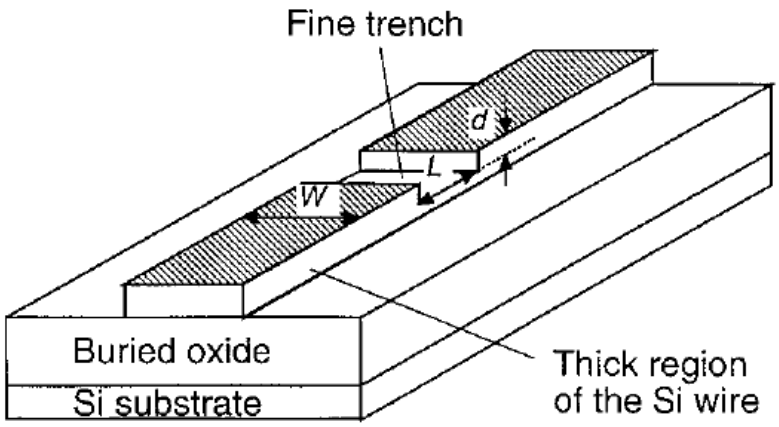


Fig 3 [3]: Si Pattern for Fabrication. Si Wire with a Fine Trench. W, L, d are Wire Width, Trench Length and Trench Depth Respectively

- The trench does not cut all the way through the wire. The main step in the fabrication is thermal oxidation which is carried out after defining the trench. The original method used is PADOX while here we use V-PADOX. The difference is that in the original method, the fabrication is carried out along length while here it is carried out along the vertically modulated Si pattern.
- The oxidation process here takes place at a temperature of 900^0C. The thick Si wire retains its shape after oxidation while the thin wire below the trench gets converted to islands. The reason is the accumulation of stress at the edges leading to the formation of the islands due to reduction in oxidation. Thus in this process, we will have two side gates in the device. The process is shown below:

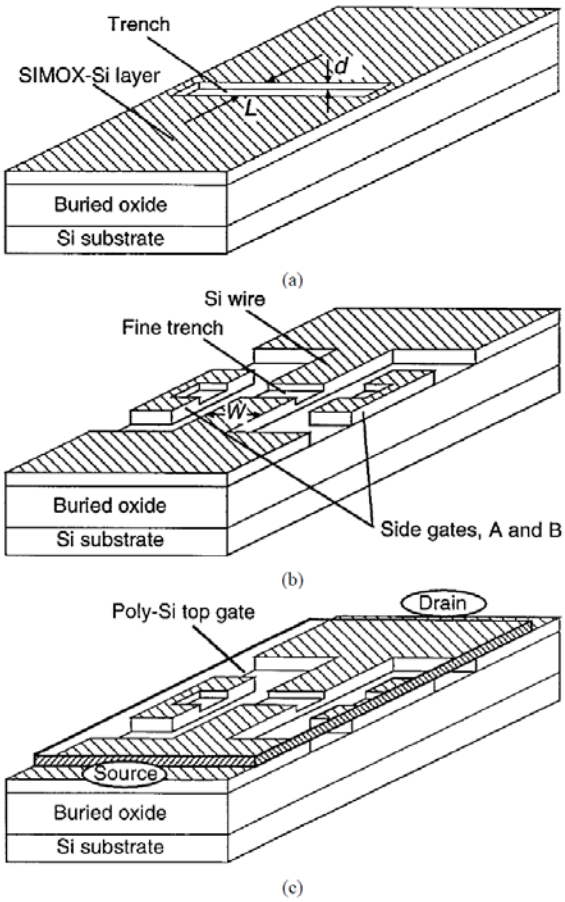


Fig 4 [3]: (a) Trench Formation, **(b)** Wire and Side-Gate, **(c)** Top-Gate in SET

- The equivalent circuit for the SET transistor is given below:

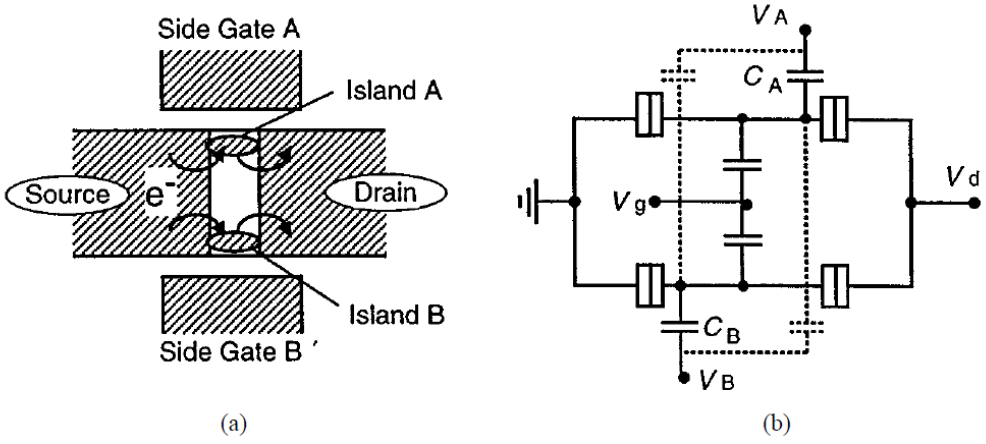


Fig 5 [3]: (a) Top View (top-gate not shown), **(b)** Equivalent Circuit, C_A and C_B are Capacitances Between Side Gates and Target Islands While for Opposite Sides it is given by Dotted Lines, V_A, V_B, V_g, V_d being Voltage to Side Gates, Top Gate and Drain Respectively

b. Coulomb Blockade in SET [4]: (See Appendix for Graph Calculations)

- In the case of SET, the tunneling process can be initiated by source and single electron island. The condition in this case is:

$$\frac{V_d C_d}{C} + \frac{V_g C_g}{C} \geq \frac{e}{2C}$$

The minimum value of the drain voltage is V_{cb} i.e. coulomb barrier voltage and thus the value is given as:

$$V_{cb} = \frac{e}{2C_d} - \frac{V_g C_g}{C_d}$$

And thus the slope is negative with a value of:

$$\frac{dV_{cb}}{dV_g} = -\frac{C_g}{C_d}$$

- In another case, the tunneling process can be initiated by drain and single electron and the condition involved in this case is written as:

$$V_{cb} = \frac{\frac{e}{2} + V_g C_g}{C_g + C_s}$$

The slope in this case is given by:

$$\frac{dV_{cb}}{dV_g} = \frac{C_g}{C_g + C_s}$$

- These two conditions when drawn as a graph, give the following figure:

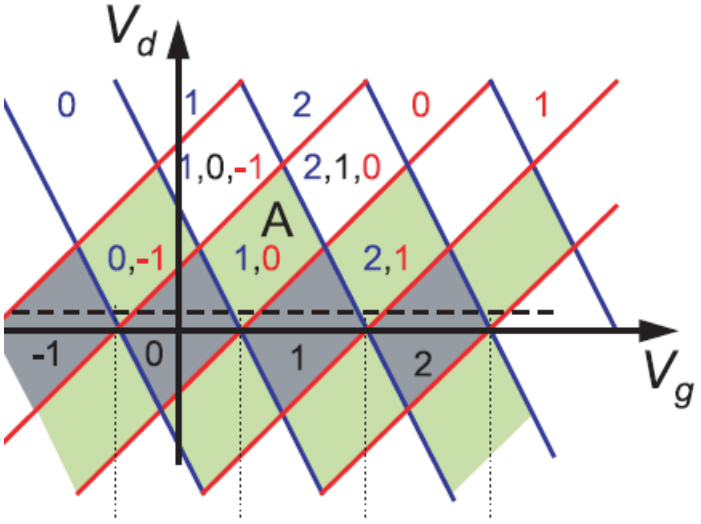


Fig 6 [4]: Graph to Show Regions for Coulomb Blockade

Coulomb blockade occurs only in the diamonds and current will flow for certain discrete values of V_g irrespective of V_d. These values are given by:

$$\frac{ne}{C_g} + \frac{e}{2C_g} = V_g$$

c. Working [2]:

- The working of the SET is mainly based on the effect called coulomb blockade. It has to be made sure that only one electron passes from the source to the island at a time.
- The island also contains electrons and hence the tunnel junction acts as a dielectric between the two electrodes. It is polarized and has the polarization capacitance C.
- When a bias potential is applied which is working against this capacitance, this causes an electron to travel towards the junction and charge it with an extra potential of V.
- Tunneling is only possible if the charging energy is greater than the thermal energy of excitation i.e.

$$\frac{e^2}{2C} > k_B T$$

  Thus the electron for which this condition is not met, they do not undergo tunneling and hence only one electron tunnels at a given time.
- If the bias potential is increased more and more, the number of electrons which can tunnel are increased from one to two and so on. This can be shown in the form of the staircase characteristics as shown below:

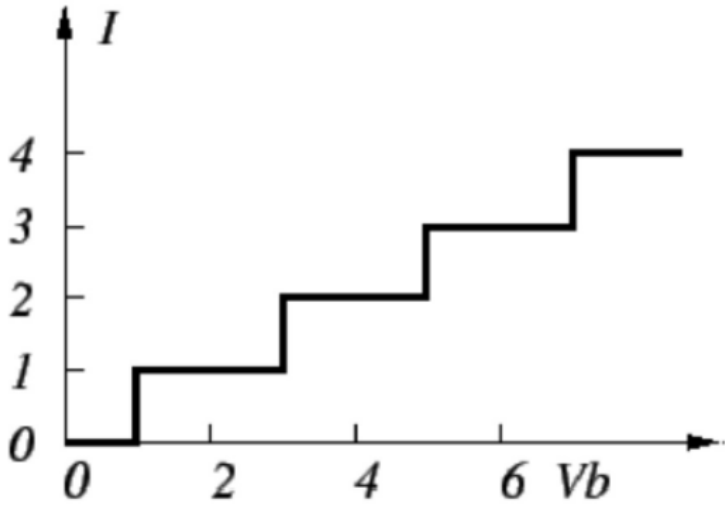


Fig 7 [2]: Graph Showing the Variation of Number of Electrons (I) with Bias Potential (V_b)

(See Appendix for how this Curve is obtained)

2. Si Memory Device Using SET Detector [5]:

Flash memory Si devices are now being studied extensively because of their low-power consumption and small size. In order to be useful for memory purpose, the electron tunneling rate between the gate and channel should be low and for this purpose MOSFET is combined with a SET to act as gateway for the electron. This is done so that the storage time can be increased.

- The schematic is shown in the following figure. The memory island is connected to the source of electron via a MOSFET and it is connected to SET island capacitively. Both of these islands are formed on SOI layer.

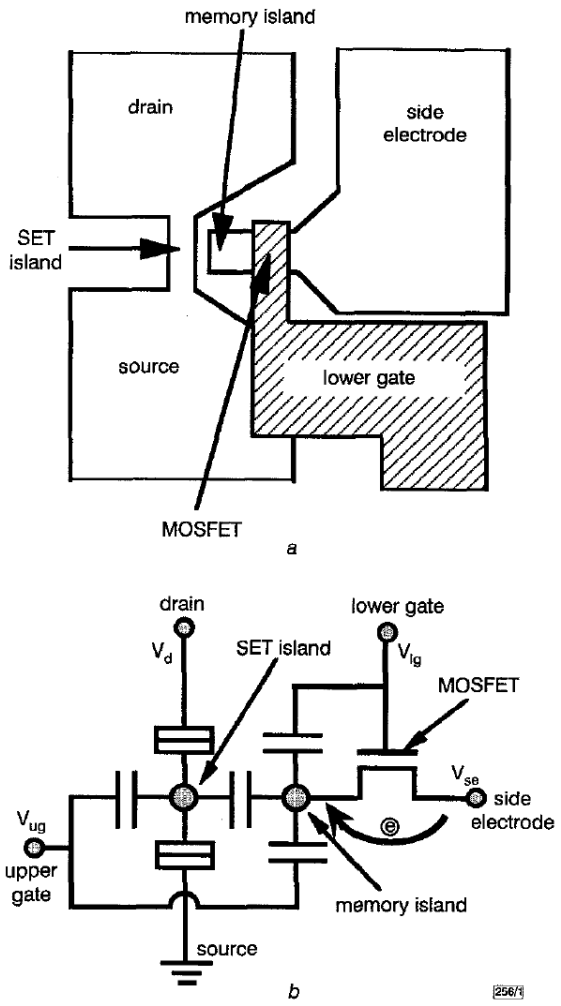


Fig 8 [5]: (a) Schematic Structure of Si based Memory Device, **(b)** Equivalent Circuit of Memory Device

- Operation speed can be controlled since a MOSFET controls the electron transfer from the reservoir to the memory island. Also SET senses the electrons stored in the memory island, thus only few electrons are required and hence this allows ultra-low power operation.

a. Fabrication:

- The fabrication is carried out on SIMOX (separation by implanted oxygen) wafer with a flat top Si layer which is obtained by 40 hours of annealing in Ar/O_2 environment at 1350^0C.
- The structure (except for the lower gate) shown in (a) is obtained by electron beam (EB) lithography and reactive ion etching in top 30nm of Si layer. Thermal oxidation of the wire (40nm wide and 100nm long) is used to create the islands and the tunnel barriers as explained in the previous case.
- Another wire of the same measure is used near the SET island to create the memory island by the same technique. The electrode thus formed will act as the lower gate. This gate acts as the separation between memory island and the electron reservoir (i.e. side electrode). The width of the lower gate is equal to the channel length of MOSFET i.e. 50nm and the memory island is 100nm long.
- This is followed by the formation of the upper gate. Then phosphorus ions are implanted in the top Si layer for electrical activation.

b. Operation:

- MOSFET is turned off in order to store the electrons in the memory island. The side electrode voltage (V_{se}) is set to -1V from 0V before the lower gate voltage (V_{lg}) is varied.
- The MOSFET gets turned on at V_{lg} = -2.3V and this corresponds to 'write' function. The information is retained while the voltage is turned back to less than -2.3V.
- The capacitance of the memory island has been estimated to be C_i = ~15±7aF. The number of electrons for the write voltage of -1V have been estimated to be ~100. Thus the information stored as 1 can be detected by SET.

$$\boldsymbol{Q = ne = C_i V_{se}}$$

Here 'n' is the number of electrons.

- The working temperature and number of electrons required for operation can be reduced by reducing further the size of the device.

3. Probabilistic Switches Using Single Electron Threshold Logic [6]:

As the size of the devices is reduced further, certain problems start coming up in the CMOS devices. Due to this, nanometer-scale devices using quantum effect are being studied. Single-electron devices are such devices. But these devices cannot be used reliably for logic operations because they are susceptible to random noises and parameter variation and also there may be faulty tunneling due to heating.

- It has been estimated that in order to save energy, probabilistic devices in inexact design can help. This is possible by utilizing the random thermal noises using the CMOS technology. This can be useful in some applications where some percentage of fault is acceptable.

- In this field, the relation between the energy for a single tunneling event and probability for being in the correct state after tunneling is obtained. The temperature of observation here is low, about 5K.

a. Working:

The digital logic here is controlled by controlling the flow of electrons. The logic zero is equivalent to one electron charge. General set up is shown in the figure below:

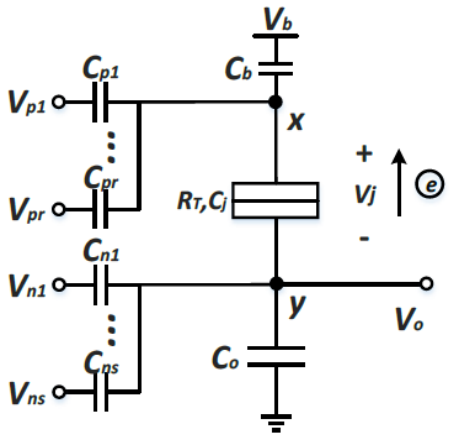


Fig 9 [6]: Single Electron Threshold Logic Gate

- The inputs are summed here at nodes x and y. The parallel combination of R_T and C_J represents here the single electron device. Depending upon if the tunnel voltage V_j is greater than a specific critical voltage V_c, the electron is allowed to tunnel otherwise not.
- In order to study the effect of the background noises, the tunneling rate relation is used here. The regular tunneling rate is given by:

$$\Gamma = \frac{V_j - V_c}{eR_T[1 - \exp(-\frac{e(V_j - V_c)}{k_B T}]}$$

The probability of being in the correct state is given by:

$$r = \frac{\Gamma}{\Gamma + \Gamma'} = \frac{1}{1 + \exp[-\frac{e(V_j - V_c)}{k_B T}]}$$

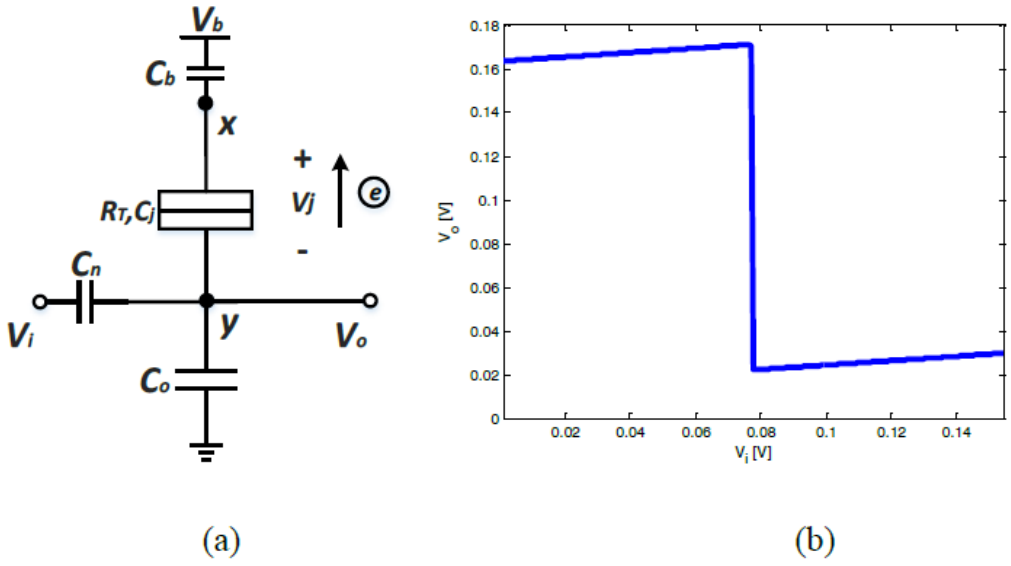
Where 'e' is the charge of the electron, R_T is the resistance of the tunnel junction, k_BT is the thermal energy, Γ' is the inverse tunnel rate computed by using $-V_j$ in place of V_j.

- In order to obtain energy-reliability tradeoff, different bias voltages (V_b) are applied. This helps in studying the effect of noise on the functionality of the device. From the figure

given below, the bias voltage is expressed as the function of tunnel voltage (V_j) and input voltage (V_i) as:

$$V_j(V_b, V_i) = \frac{(C_n + C_o)C_b.V_b - C_nC_bV_i}{C_\tau}$$

Here $C_\tau = C_bC_j + (2C_b + C_j)(C_b + C_j)$. Thus it can be seen that the bias voltage affects the tunnel voltage and hence the reliability r.



(a) (b)

Fig 10 [6]: (a) Structure of Probabilistic Inverter Using SE Threshold Logic, **(b)** Static Voltage Transfer Characteristics, Parameters being V_b = 155mV, C_b = 1.37aF, C_j = 0.1aF, C_o = 0.81aF, C_n = 0.1aF and $R_T = 10^6\Omega$. **(See appendix for details)**

- The energy associated with a single tunneling event is given by the following relation. Thus this relation is also affected by bias voltage due to the dependence of 'r' on it and hence we can obtain a relation between energy and reliability which is as given below:

$$E = e(V_j - V_c)$$

$$E = k_BT.\ln(\frac{r}{1-r})$$

The magnitude of k_BT gives the magnitude of thermal noise. This is an exponential relation and also the limit for energy consumption in the case of deterministic switching is $k_BT.\ln 2$ while it is $k_BT.\ln(2r)$ for probabilistic switching and it depends upon r.

Advantages or Merits of Single Electron Devices [7]:

We have already discussed few fields where single electron concept is being used. These fields are only developed because single electron devices make use of quantum effects which are responsible for many advantages over the conventional devices. This section will highlight some of these advantages.

- One of the major advantage of these devices is that they have small size because they make use of quantum dot and hence the overall size of the chip can be reduced and the packing density can be increased. Thus they can be used for large scale integrated circuits.
- SET possess the ability to withstand radiation in a much better way than the traditional MOSFETs or BJTs. This makes it possible for these transistors to be used at places which are exposed to radiations like the satellites etc.
- Yet another advantage can be seen in the case of signal processing. Conventional transistors have the leakage problem and hence there is a problem of background current. This occurs because in the OFF state the electrons still leak. This is not seen in the SET.
- The sensitivity of SET is better than the MOSFET and hence it can be used in the devices used to measure the charge. Since SET can easily detect the presence of the electron and hence it can easily detect the charge.
- Since the island can easily be made to hold the electron and hence the SET can be used as memory and the read write time for this kind of memory is 20ns. The data can be retained in these memories for few weeks. SET memory is advantageous since the size of these kind of memories is really small because of the use of Quantum dot.
- Because there is no interference problem in SET so they can lead to faster processors. They are also compatible with the existing technology as explained in the previous section and hence the new technology can make use of both MOSFET or BJT features as well as the SET features.

Disadvantages or Demerits/Problems Associated with Single Electron Devices [8]:

After briefly discussed the advantages of the single electron devices but there are also some problems associated with these devices. Most of the devices now a days use the single electron concept by using SET and hence we will mainly discuss the problems associated with them. Some of the main issues involved are:

- **Lithography Process:**
  One of the major problem with the single electron devices that the size of the island should be as small as possible at room temperature. But in order to fulfil this requirement, the thermal energy has to be high. The island are in the sub-nanometer range and hence the lithography techniques should be very accurate so as not to distort the shape. This is desired because even for a small variation in the shape can lead to undesirable and unpredictable variations in the energy spectrum and this can also disturb the device threshold values for switching.

- **Background Charge:**
  Since there is always an electron present in these devices and hence this charge polarizes the island. Thus in the calculations involved, we have to subtract this charge from the external charge available.

- **Co-tunneling:**
  More than one electron (N>1) can be made to tunnel but the rate of tunneling in this case is smaller than the case in which only one electron tunnels. This rate is $(R_Q/R)N-1$ times less than the ideal case. It comes from the orthodox theory which deals with the islands of diameter $\geq$ 100nm and hence the tunneling resistance in this case is 6.4kΩ (= R_Q) as compared to 25.8kΩ in the actual theory. Here R_Q is the quantum unit of resistance and R is the combined resistance of all the tunnel barriers.

- **Operation at Room Temperature:**
  With the techniques available now in the industry, the island size still needs to be reduced before it can be used in the large scale integrated circuits. Because of the large island size, the temperature of operation is very low. As long as the working temperature is not increased to the room temperature, the single electron devices cannot be used in practical applications. In order to achieve this, the island size has to be reduced more and more.

- **SETs and Remaining Circuit:**
  There are some of the issues associated with the formation of the devices using SETs due to the small size and the quantum effects involved. The SETs can be connected to the remaining circuit by two methods. The first method involves the use of the MOSFETs to integrate the SET with the other circuit components. This involves the use of the wire. This method is advantageous in the sense that the packing density can be increased. The other method involves the use of the static electronic force in order to create the clusters and hence a circuit is created by using only the force and this circuit is called Quantum Cellular Automata (QCA). The advantage of this method is that the transfer speed of the information can be as high as the speed of light and also the size of the cells can be as small as 2.5nm. This will help in reducing the overall size of the future computers

Applications of Single Electron Devices [8]:

We have discussed in the first part of the report how the single electron concept can be used in various devices, how are they fabricated and how they work. We also discussed the merits and demerits associated with these devices. In this section of the report, a brief introduction is given about the applications of the single electron devices, how they are being used in the industry today.

- **Supersensitive Electrometer:**
  SET is very sensitive to the presence of electron and hence they can be used to measure low dc currents (~10^{-20} A). They can also be used for the detection of single electron effects in single electron box.

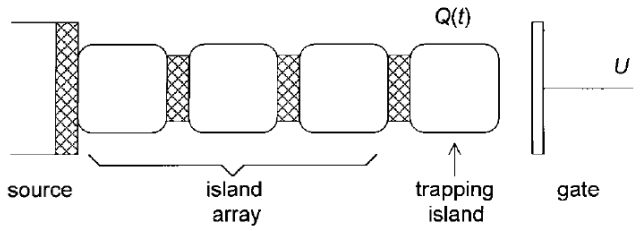
- **Single Electron Spectroscopy:**
  Single electron electrometry can be used to detect the electron addition energies and hence the energy level distributions in quantum dots and other nanoscale objects. This can be very useful for studying the quantum effects.

- **Voltage State Logics:**
  The single electron transistors can be used in the 'voltage state' mode. In this mode, the gate voltage controls the flow of the electrons in the same way as it is done in the case of the conventional transistors. Thus the logic 1/0 can be represented by high/low dc voltage (physically not quantized). This is quite useful, but the only problem here is that if the circuit has large number of components then there can be a considerable amount of power loss involved.

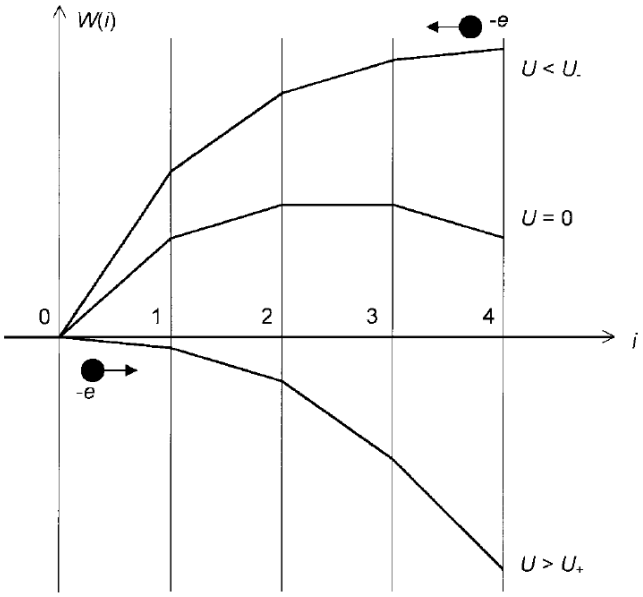
- **Charge State Logics:**
  Another application of single electron devices is in their use in the form of charge state logic. In this logic, the presence of electron in the island represents that the information is present otherwise it means that there is no information stored. This application is really useful because there is no problem of static current since there is no electron present in the static state which can produce the dc current.

- **Single-Electron Box:**
  The device consists of one island separated from the large electrode (which acts as source) by a tunnel barrier. External electric field may be applied using gate electrode which is separated from the island using a thick insulator. This prevents tunneling. The single electron box can be used in the circuits for information storage but the problem is that the number of electrons that can be stored are dependent upon the applied voltage. Thus the use is very limited.

- **Single-electron Trap [9]:**
  This application is a further extension of single-electron box application. In this case, more than one island with more than one electron are connected by the use of tunnel barriers. The advantage of this type of the device is that the system can remain in more than one stable state under certain range of the applied voltage U. This multistability exists because the electron in one of the islands extends its field to a certain distance because of the electric polarization effects.
  Thus the single electron solitons interact with the array edges upto a certain distance given by $M = (C/C_0)^{1/2}$, here C is the mutual capacitance between neighbouring islands and C_0 is the effective stray capacitance of the island. The maximum self-energy is found in the middle of the array (middle trace in the figure below part (b)). By applying sufficiently high gate voltage, the electron can be shifted to the edge island and other electrons experience repulsion and hence do not follow. In order to remove the electron from this island, gate voltage has to be reduced as it is seen in the upper curve of part (b) in the following figure.



(a)



(b)

Fig 11 [9]: Single Electron Trap **(a)** Schematic, **(b)** Electrostatic Energy of an Extra Electron as a Function of its Position Different Values of Gate Voltage (U)

- **DC Current Standards [9]:**
  In this application of single electron devices, the SET oscillations are phase locked in an oscillator with external RF source of frequency f. This locking enables for the transfer of fixed number of electrons (m) for each period of RF signal and hence generate the DC current which can be given by the equation:

$$\boldsymbol{I = mef}$$

  This application can be used in the functioning of single-electron turnstiles and pumps.

Future of Single Electron Devices:

- Single electron devices are still under study and the technology is still in its infant stage. There are few issues associated with these devices which have to be overcome before they can be used at room temperature for practical purposes. The problems have been discussed in the previous section. Also we studied various single electron devices and how they are used in the industry.
- The future of these devices is really bright because the existing MOSFET technology is already reaching its limit. Due to this, the size of the devices cannot be reduced further and the single electron devices provide a solution for this problem because they make use of the quantum-effects at sub-nanometer range.
- We have already discussed the devices possible using this technology. Apart from all these devices, there are certain other devices which are under study to be used in near future. These include the temperature standards, resistance standards, infra-red detectors etc.
- The use of the single electron devices for designing the memory will help in further reducing the overall size of the computers.
- As more and more study will be done in the field of quantum mechanics, more insight can be gained in these devices.

Conclusion:

In this report we studied the basic single electron devices, their fabrication and how they work. The next part of the report is dealing with the merits and demerits of these devices which clearly shows how these devices can help overcome the problems faced today with the MOSFET technology. The single electron device concept is solely based on the quantum effects involved at nanometer scale and hence the fabrication of these devices is still under study. Since the scale is really small and hence the fabrication process is difficult because accurate positioning of components is really hard at this scale.

Also for the working of these devices the placing of the islands with respect to the source and drain is a very critical process and needs a high rate of precision. The problems like the leakage of charge in the background can be serious if large number of components are involved. Thus in order to use these devices, the size of the islands has to be as small as possible so that they can be used at room temperature.

Finally, the applications of the single electron devices show the future possibilities in this field. Some of these are even under testing to be used shortly. These devices can easily overpower the existing technology if their control is made possible at high temperatures.

Thus these devices especially the SETs are capable of shrinking the size of the transistors to less than 10nm or even shorter which will be a major breakthrough in the field of semiconductor technology.

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Appendix:

1. Fig 6:

Equations for V_{cb} :-

Tunneling process initiated by source and single e^- island :-

Case I: $V_{cb} = \frac{e}{2C_d} - \frac{V_g C_g}{C_d}$ —①

slope : $\frac{dV_{cb}}{dV_g} = \frac{-C_g}{C_d}$

Tunneling process initiated by drain and single e^- island :-

Case II: $V_{cb} = \frac{\frac{e}{2} + V_g C_g}{(C_g + C_s)}$ —②

slope : $\frac{dV_{cb}}{dV_g} = \frac{C_g}{(C_g + C_s)}$

Now, plotting a graph b/w V_d and V_g :-

In case ①,

When $V_g = 0$

Then $V_d = \frac{e}{2C_d}$ (from eqn. ①)

and a -ve slope of $\frac{-C_g}{C_d}$

When V_{cb} or $V_d = 0$

$0 = \frac{e}{2C_d} - \frac{V_g C_g}{C_d}$ (from eqn ①)

$\Rightarrow V_g = \frac{e}{2C_g}$

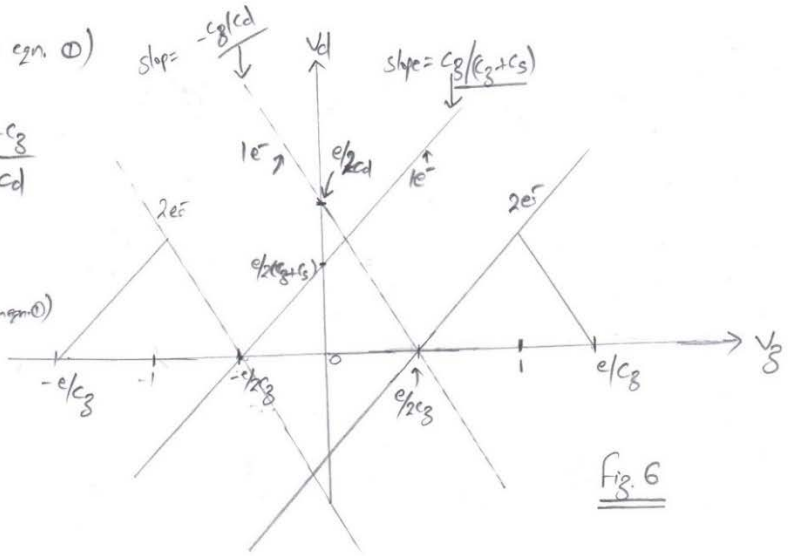


Fig. 6

In case ②,

When $V_g = 0$

Then $V_d = \frac{e}{2(C_g + C_s)}$ (from eqn. ②)

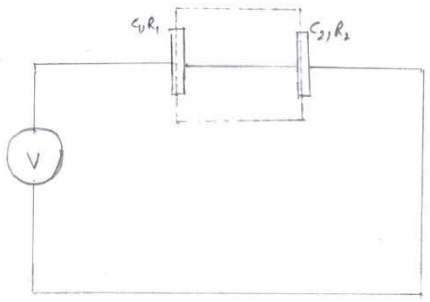
When $V_{cb} = 0$

$0 = \frac{\frac{e}{2} + V_g C_g}{(C_g + C_s)}$ (from eqn. ②)

$\Rightarrow V_g = -\frac{e}{2C_g}$

As the number of e^-s keep on increasing, we obtain other graph lines as shown in the graph for 2 e^-s.

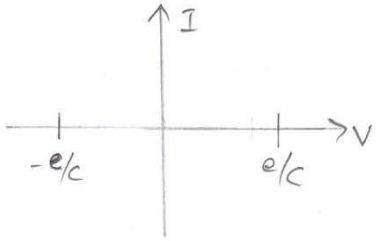
2. Fig 7:



1) For the first case: (Symmetric junction)

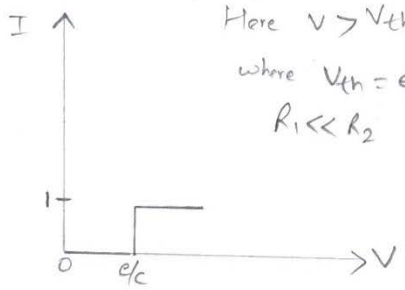
When $C_1 = C_2$ and $R_1 = R_2$

Then Current flow, $I = 0$ and we obtain two points for I-V graph.



The voltage remains less than 'e/C'.

2) In second case: when voltage is increased beyond threshold value, then current starts flowing and single electron tunnels towards the drain.



Here $V > V_{th}$

where $V_{th} = e/C$

$R_1 \ll R_2$

Here, $I = \frac{V}{R} = \frac{e}{2R_tC}$

$R_t \rightarrow$ tunneling Resistance

R_t (min. value) $= 25.8k\Omega$

Capacitance value is in attofarads (aF)

Therefore, the value of I has to be in the range of mA:

$I \rightarrow \frac{10^{-19}}{10^3 \cdot 10^{-18}} = \frac{10^{-19}}{10^{-15}} = 10^{-4} \approx 0.1mA$

3) Third case: When the voltage is increased more, more amount of current flows and the number of electrons tunneling also increases.

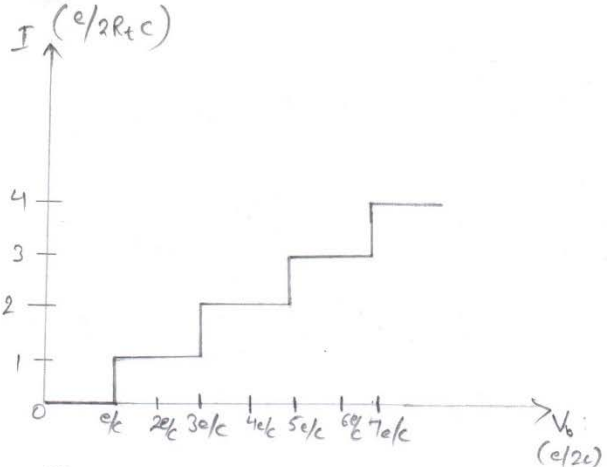


fig 7

CURRENT FLOW IS THE PERIODIC FUNCTION OF VOLTAGE.

3. **Fig 10 [6]:**

The application of the single electron concept for probabilistic is a recent concept and is still being studied. The curve shown for this application indicates the transfer characteristics for SE threshold inverter. The simulations are performed using Monte Carlo (MC) simulation for SE threshold logic using SIMON simulator.

The drop in the curve shows the tunneling event taking place. It can be seen in the graph that the threshold value for the event is approximately half of the input range which maximizes the noise margin. The following findings are included by the authors in reference 6:

- The input signal and its transient response obtained using the given set up is as below:

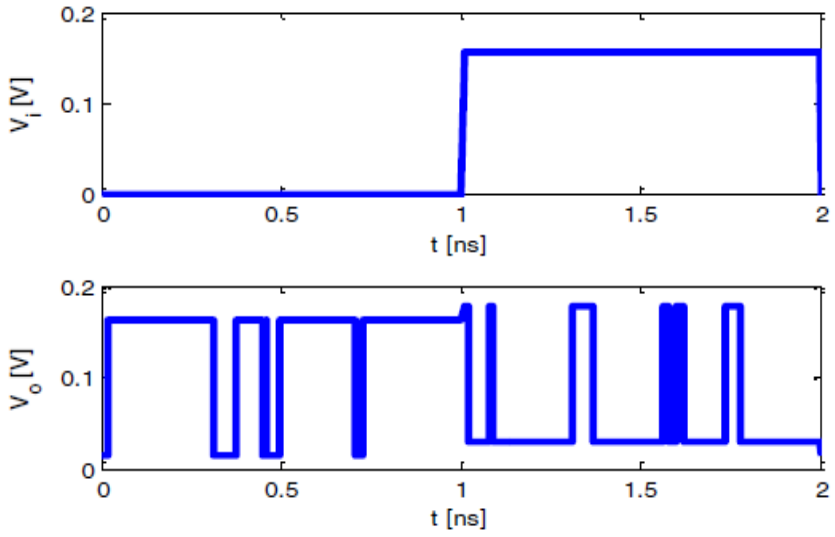


Fig [6]: Dynamic Characteristics of Probabilistic SE inverter for T = 30K

- The reliability of the inverter can be improved either by decreasing the thermal energy magnitude or by increasing the bias voltage (i.e. Switching Energy)
- The Energy reliability relation was compared with the results obtained from the simulation and the results are quite satisfactory. The simulation results are shown in the following figure:

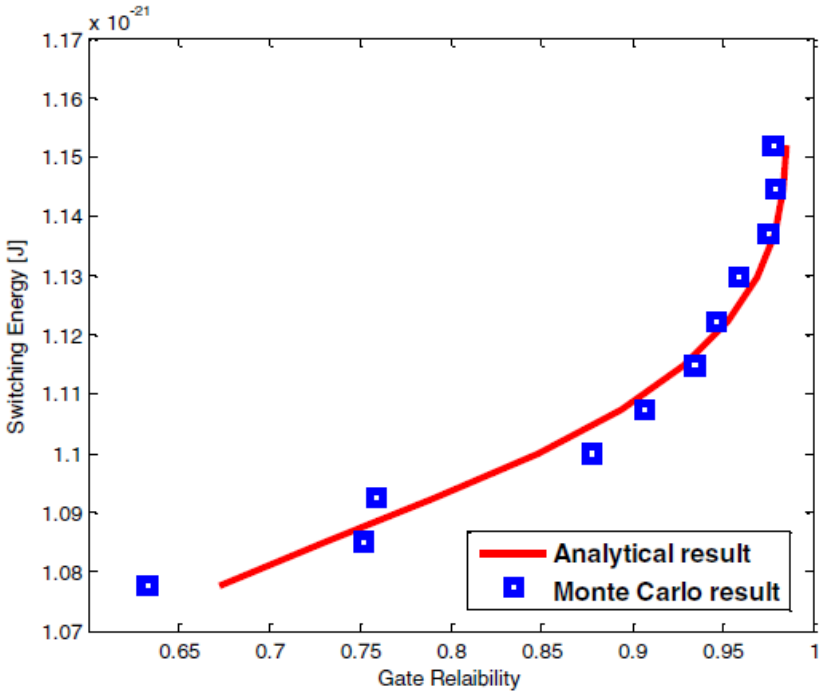


Fig [6]: Simulation Results compared with the Energy - Reliability Relation Results (T = 20K)

- It is found that at the same temperature (noise magnitude), the switching energy has to be increased in order to get higher value of the reliability and hence there is trade-off involved between the energy and the reliability for the inverter. This can be seen in the following curve:

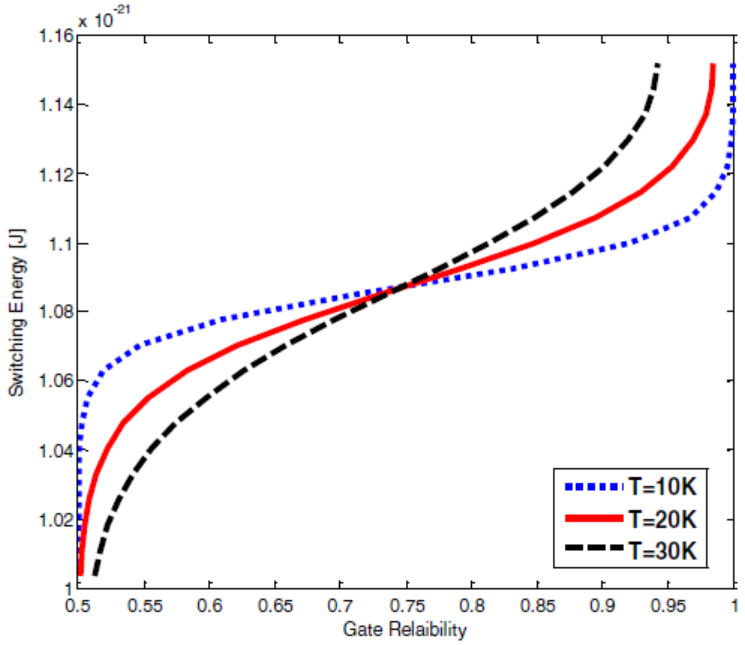


Fig [6]: Energy-Reliability Trade-off under Different Temperatures

- The relation between energy and temperature for a fixed reliability is clear form the following curve.

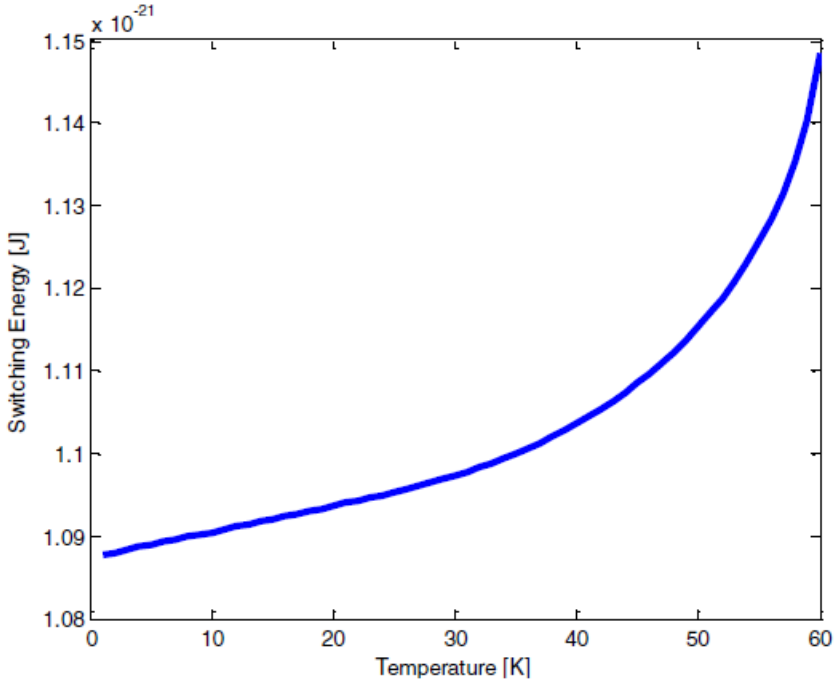


Fig [6]: Relation between Energy and Temperature for a Fixed Reliability (r = 0.8) for SE Inverter

- Last but not the least, there can be delay in the tunneling of the electron. It has been found that the delay is proportional to the tunnel rate. Higher value of the bias voltage means higher switching energy and hence smaller delay.