Lab 3: Pipelined CPU + Branch Predictor

Announcement

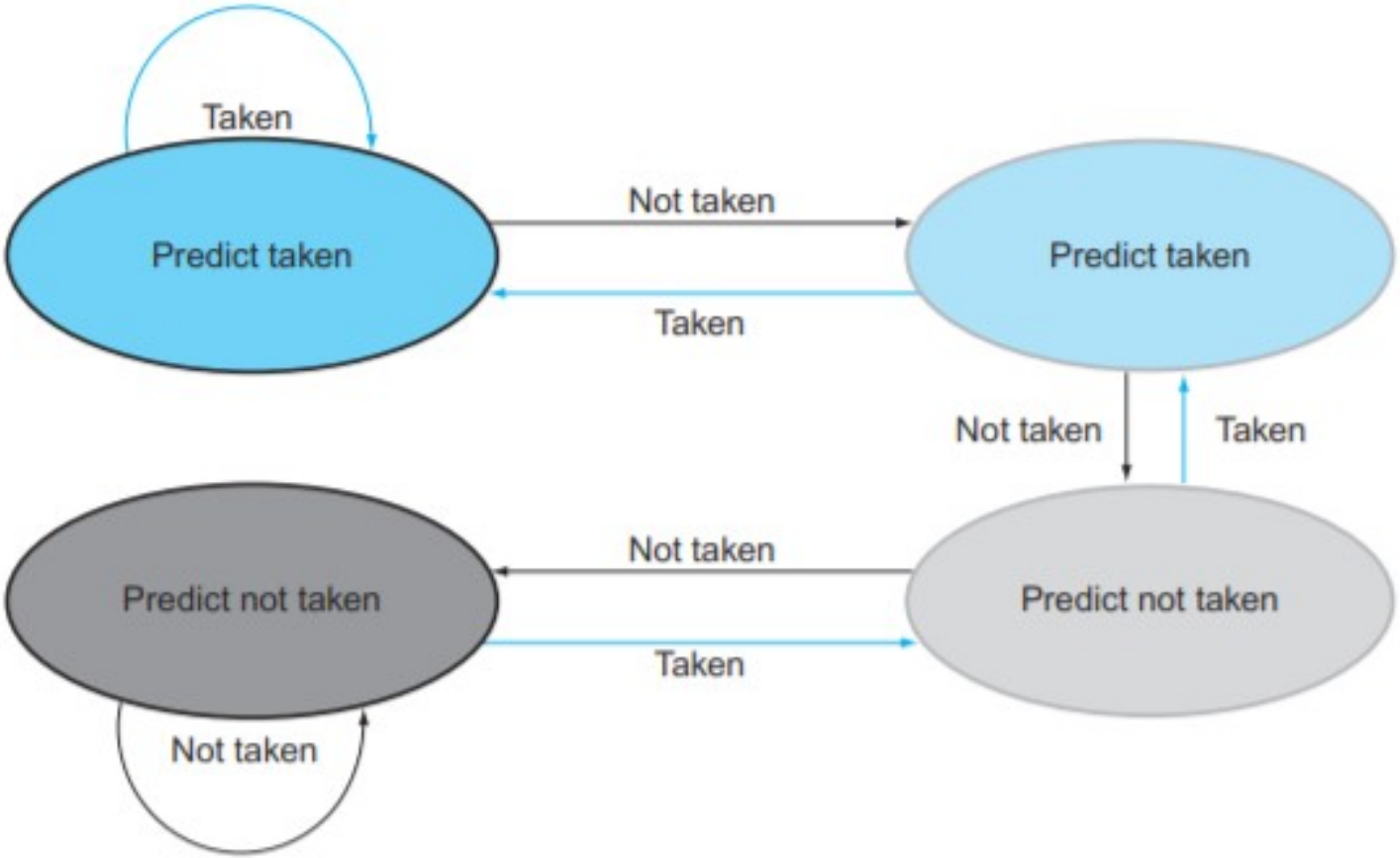
- Individual Lab
- Lab Deadline: 06/13 (Tue.) 23:59

- Demo:
  - Time slot: TBD
  - Show the execution of your program to TA and answer a few questions

Specification

- Lab 2 determines the actual branch decision with an “equal” module at ID stage
- In this lab,
  - “equal” module → 2-bit dynamic branch predictor
  - utilize the original resource of ALU (“sub”) to examine the actual branch decision in EX stage
- All branches share the same predictor (global)

2-bit Dynamic Branch Predictor



Initial state is strong taken (Top Left)

Machine Code

funct7	rs2	rs1	funct3	rd	opcode	function
0000000	rs2	rs1	111	rd	0110011	and
0000000	rs2	rs1	100	rd	0110011	xor
0000000	rs2	rs1	001	rd	0110011	sll
0000000	rs2	rs1	000	rd	0110011	add
0100000	rs2	rs1	000	rd	0110011	sub
0000001	rs2	rs1	000	rd	0110011	mul
imm[11:0]		rs1	000	rd	0010011	addi
0100000	imm[4:0]	rs1	101	rd	0010011	srai
imm[11:0]		rs1	010	rd	0000011	lw
imm[11:5]	rs2	rs1	010	imm[4:0]	0100011	sw
imm[12,10:5]	rs2	rs1	000	imm[4:1,11]	1100011	beq

Things to Add

- ALU_Control & ALU
  - You have to add additional control signals to support the examination of the `beq` condition
- Additional Flushes
  - Since the the actual branch decision is determined at the EX stage now, you need to add proper flushes to the pipeline registers (e.g., ID/EX) if any misprediction occurs
- Others
  - Any detail to let your CPU perform correctly

testbench.v

- Load instruction.txt into instruction memory
- Create clock signal
- Dump Register files & Data memories in each cycle
- Print result to output.txt
- You can modify the provided reference file but make sure not changing the output format (`$fdisplay` part)

Grading Policy

- (80%) Programming
  - You will get 0 point if your code cannot be compiled
  - Grading at demo. You have to answer several questions about how you implement at demo. You may get 0 point on this part if you cannot clearly answer the questions (regarded as plagiarism)
- (20%) Report
  - Implementation of each modules
  - Difficulties encountered and solutions in this lab
  - Development environment
- Late policy: 10 points per day

Submission Rules

- studentID_lab3 (dir)
  - studentID_lab3/codes/*.v
  - studentID_lab3/studentID_lab3_report.pdf

- studentID should be ASCII-printable characters

- MUST REMOVE
  - Data_Memory.v
  - Instruction_Memory.v
  - Registers.v
  - PC.v
  - testdata/*

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