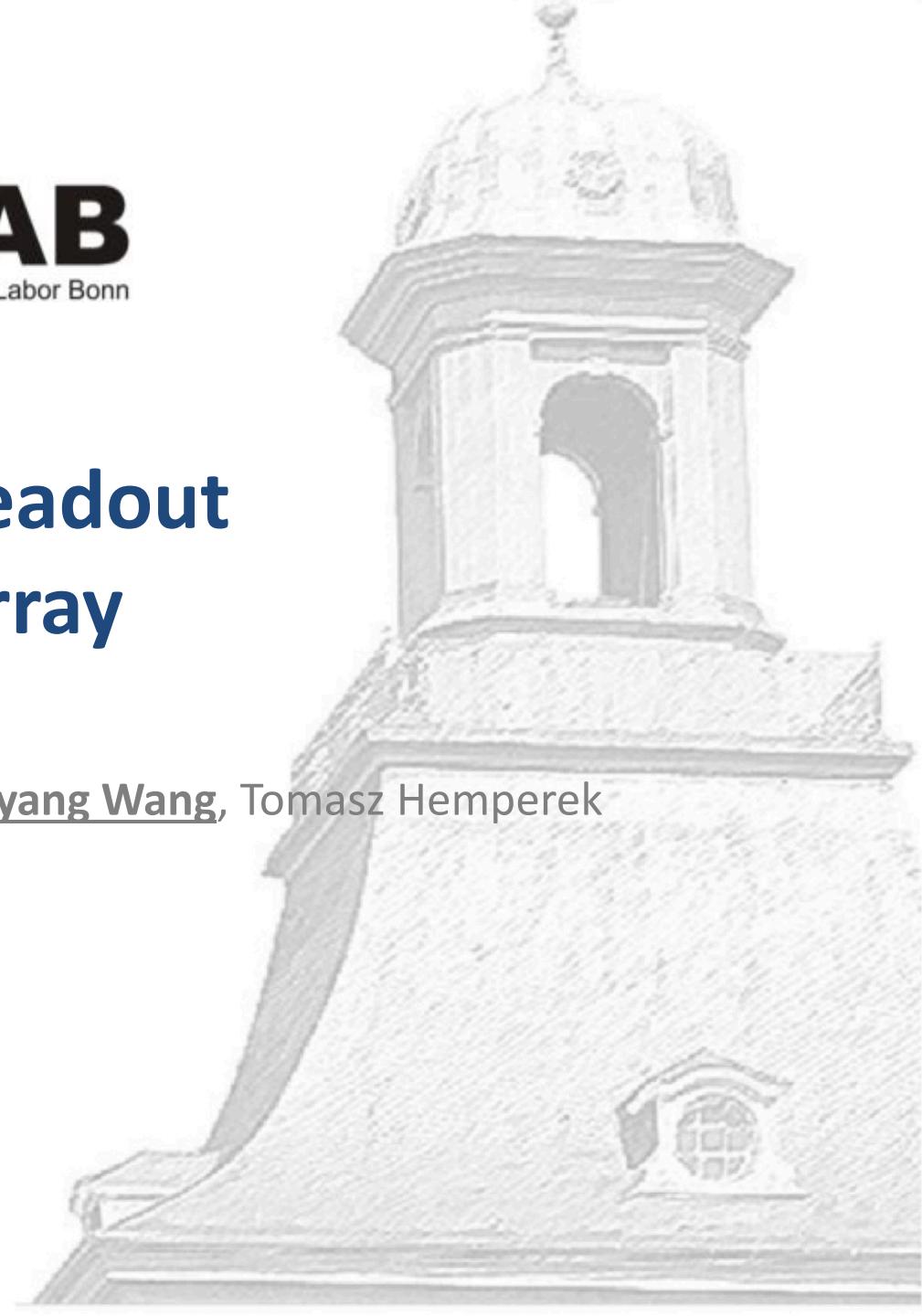




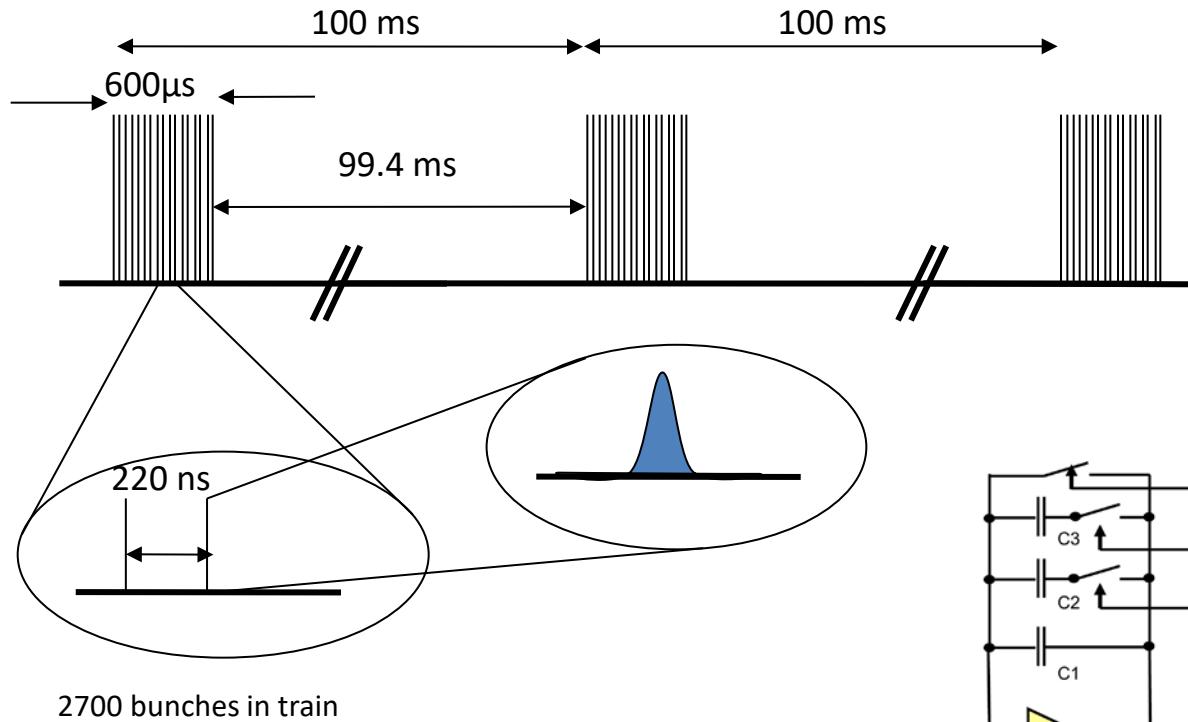
ADC for Continuous Readout Digitizing Imager Array

Hans Krueger, Themis Kamilaris, Tianyang Wang, Tomasz Hemperek



- BSS switching – Bidirectional Single-Sided switching
- CRS – Correlated reverse switching
- AW – attenuated weighting
- RE – short for redundancy here

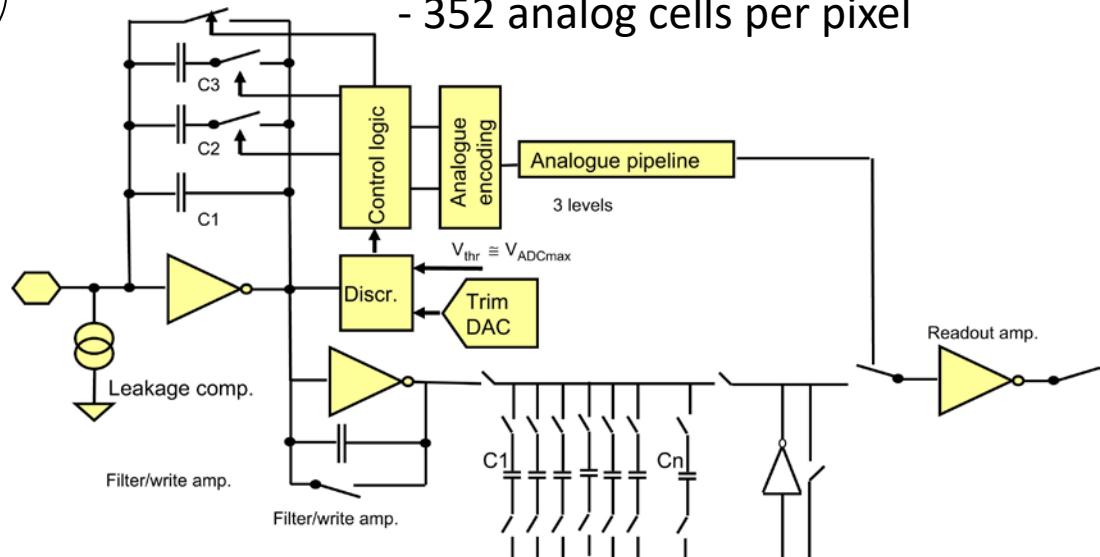
- Current European XFEL bunch structure



**27 000 bunches/s
with 4.5 MHz bursts**

Solution: AGIPD detector

- Gain switching => high dynamics
- 352 analog cells per pixel

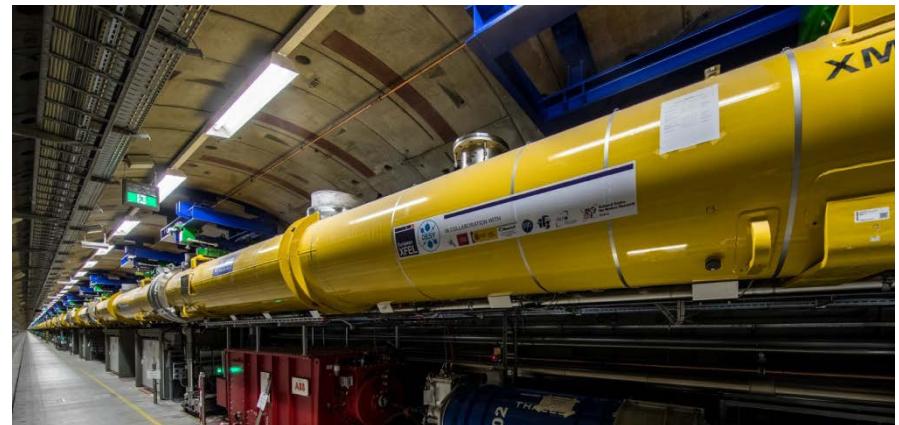


- Future sources

PETRA-IV (~2027)



CW-XFEL (~2028)



- Diffraction-limited synchrotron
- Approx. continuous X-ray beams
- **x 100** increase in X-ray brilliance

- Free electron laser
- Extremely intense X-ray pulses
- **100 kHz to 1MHz** continuous bunch rate (source)

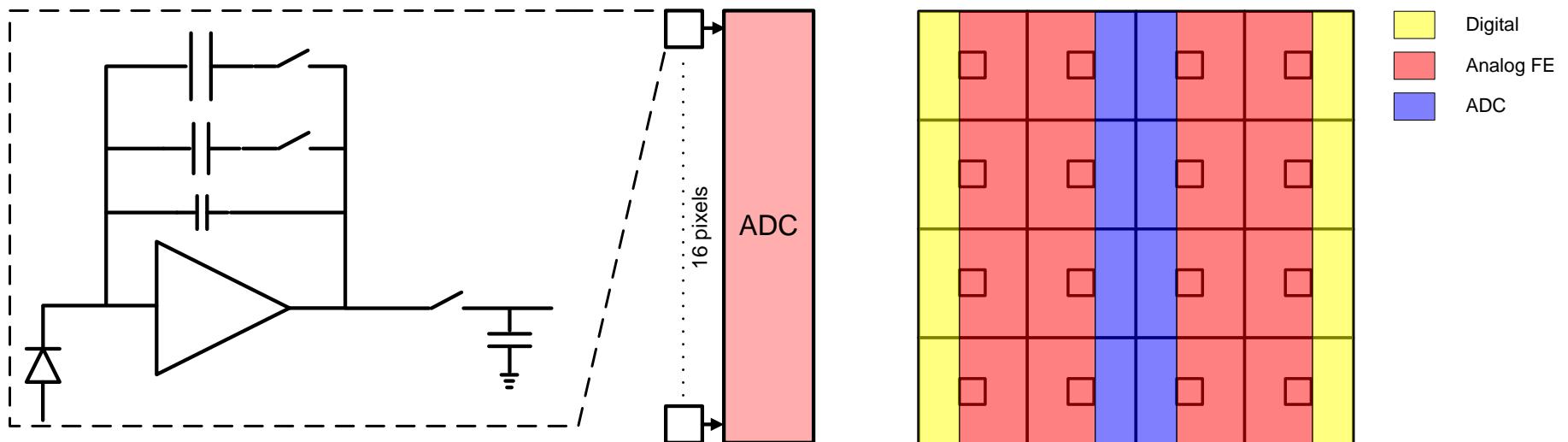
Average rate for AGPID ~ 10 kHz => require new development

- From AGIPD to CoRDIA (**Continous Readout Digitizing Imager Array**)
 - Dynamic range: $> 10^4$ photons (12 keV) with single photon sensitivity
 - Adaptive gain switching derived from AGPID
 - Frame rate: ≥ 100 kHz
 - Pixel size: $100 \mu\text{m}$ by $100 \mu\text{m}$

ADC requirements:

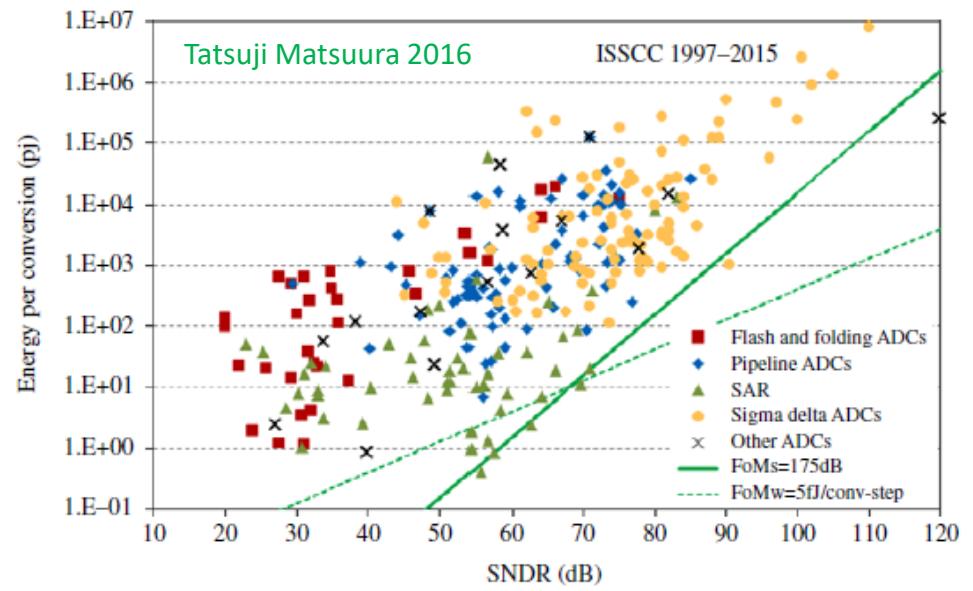
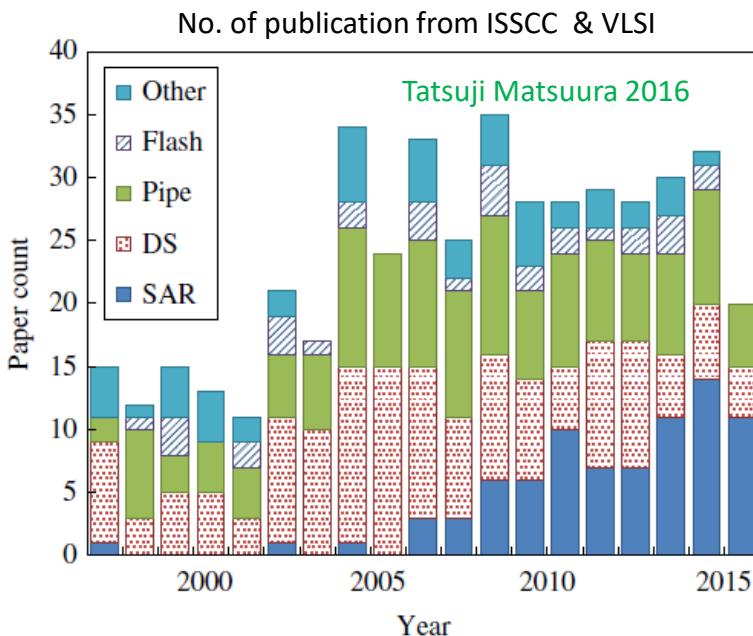
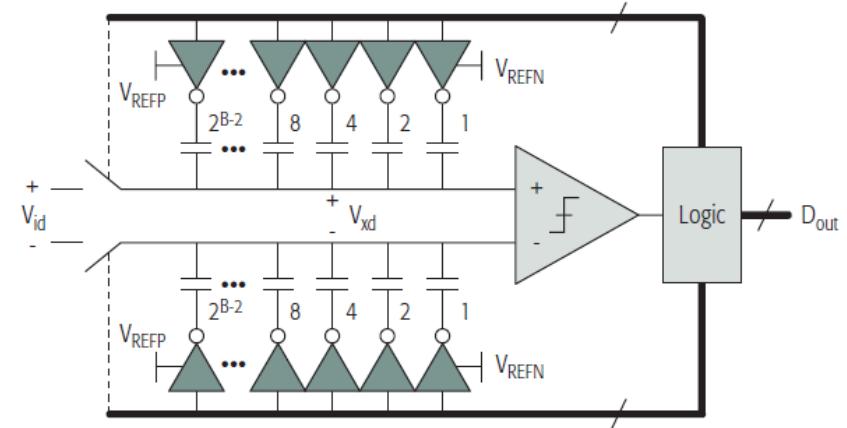
- ENOB: $\sim 10\text{b}$
- Sampling rate: $\sim 2 \text{ MS/s}$
- Area: $\sim 80 \mu\text{m}$ by $400 \mu\text{m}$
- Power: $10\text{s of }\mu\text{W}$

4 by 4 pixels sharing one ADC



Introduction

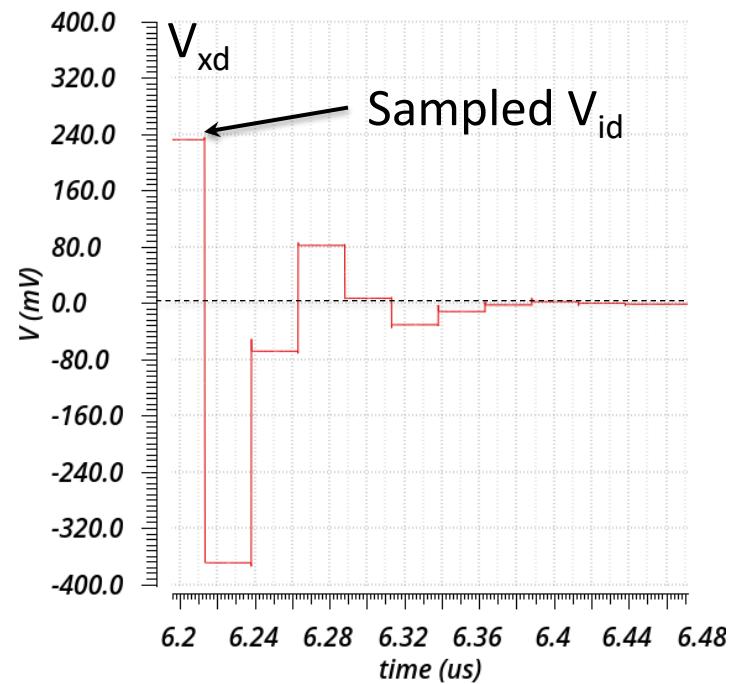
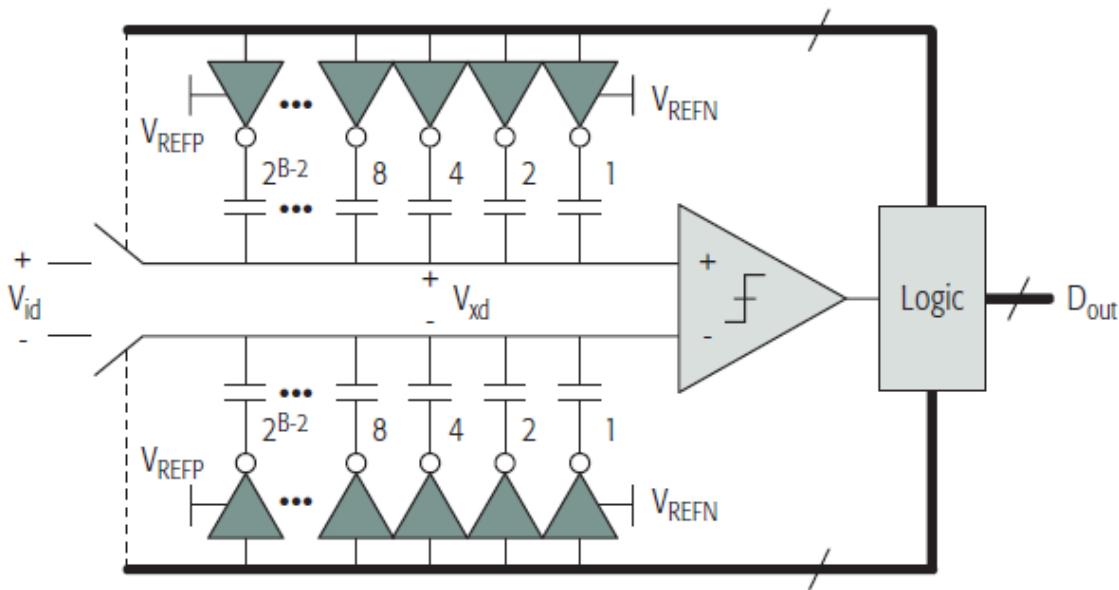
- SAR ADC has been chosen
 - Widely used for medium resolution & speed
 - Simple and most power efficient archit.
 - Benefit from tech. scaling



ADC design

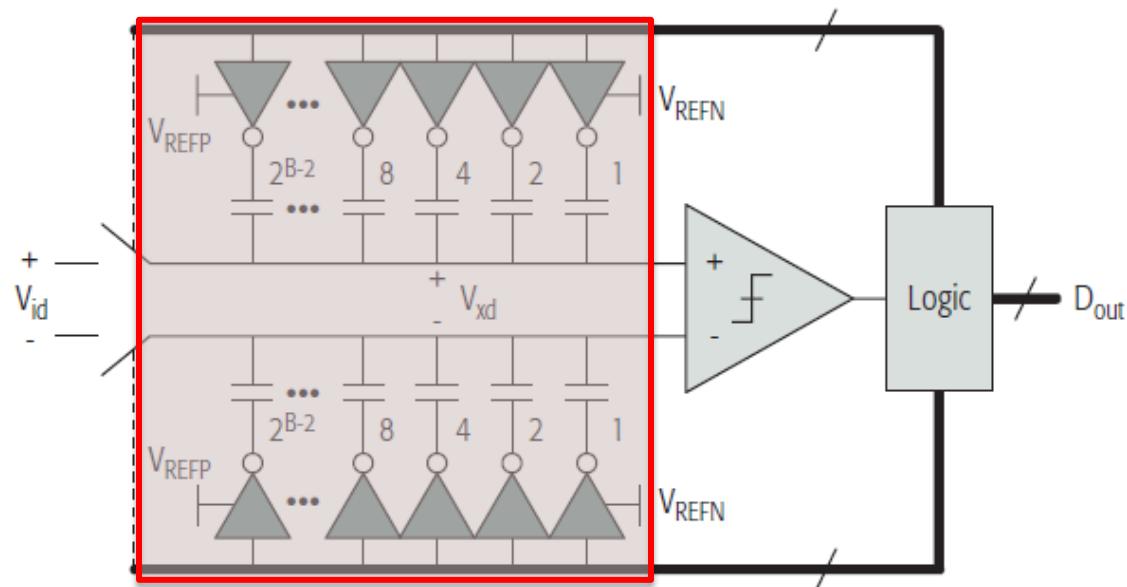
Principle of SAR ADC

- SAR - successive approximation register
 - Track & Hold + DAC + comparator + SAR logic
 - CDAC as the hold capacitor
 - Approximate the input voltage using the DAC with **binary search** algorithm



CDAC design

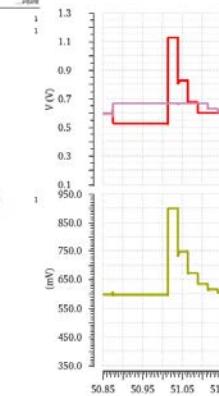
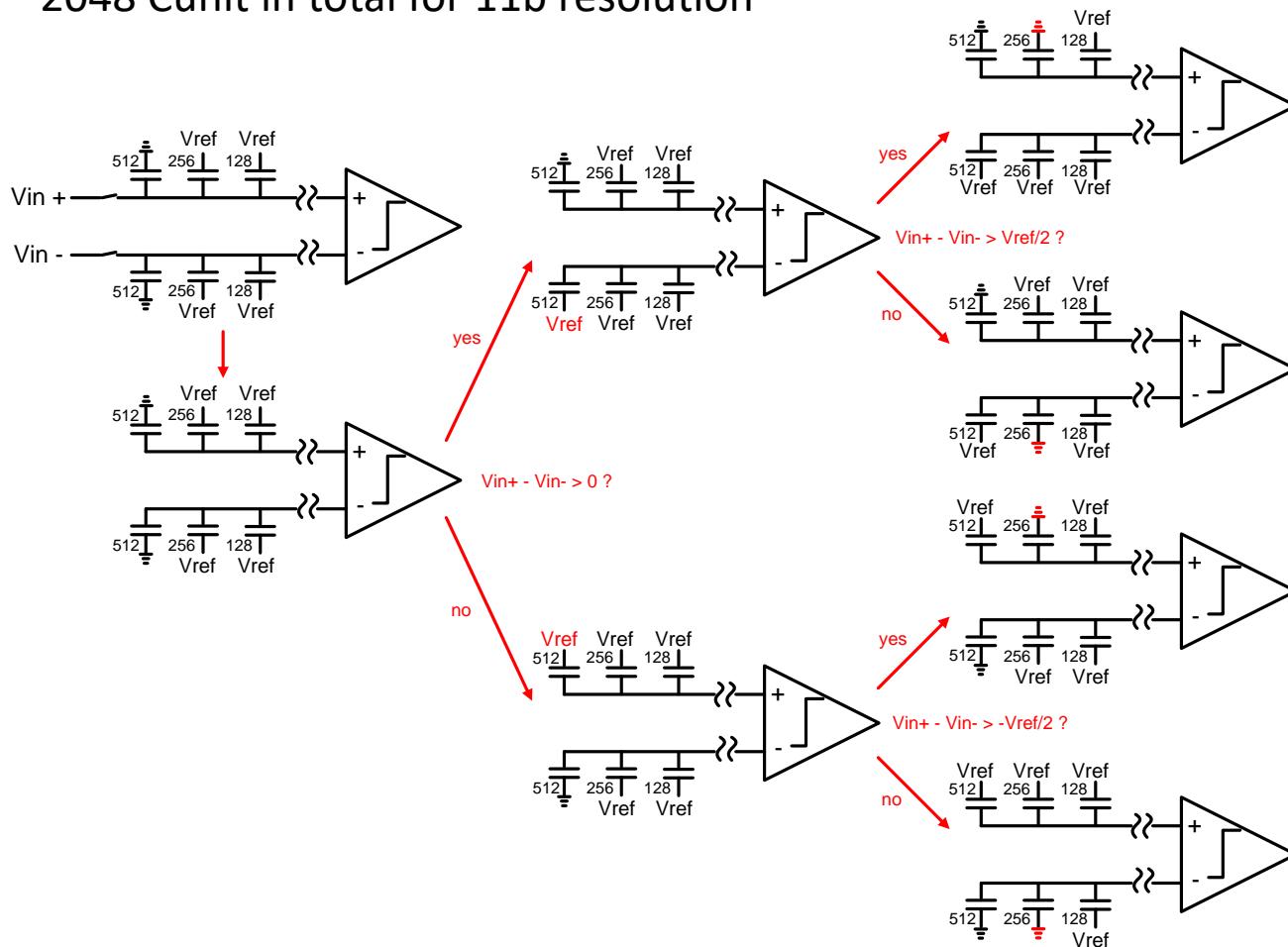
- CDAC switching technique
- CDAC driver
- Unit capacitor (Cunit) design



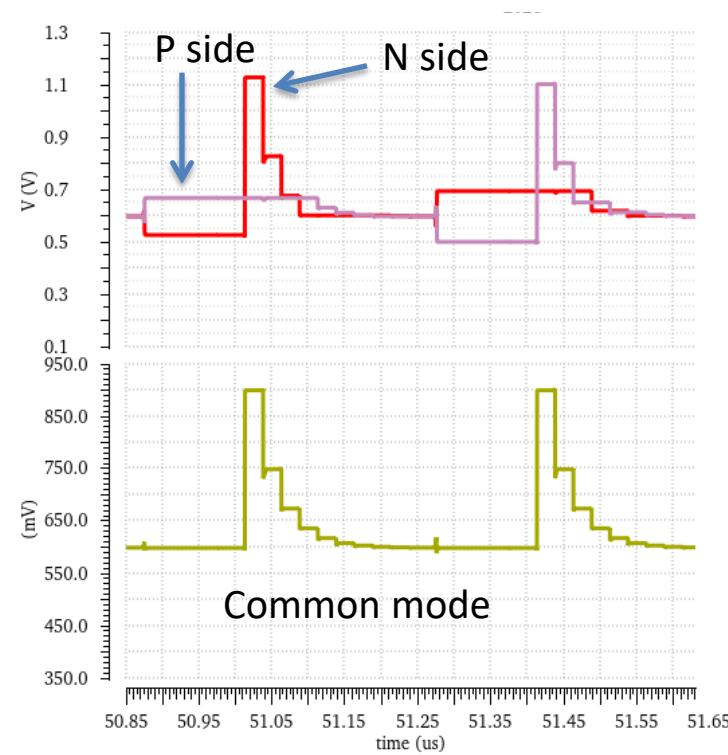
CDAC switching technique

- Bidirectional Single-Sided switching
 - Top-plate sampling (original BSS uses bottom plate sampling)
 - 2048 Cunit in total for 11b resolution

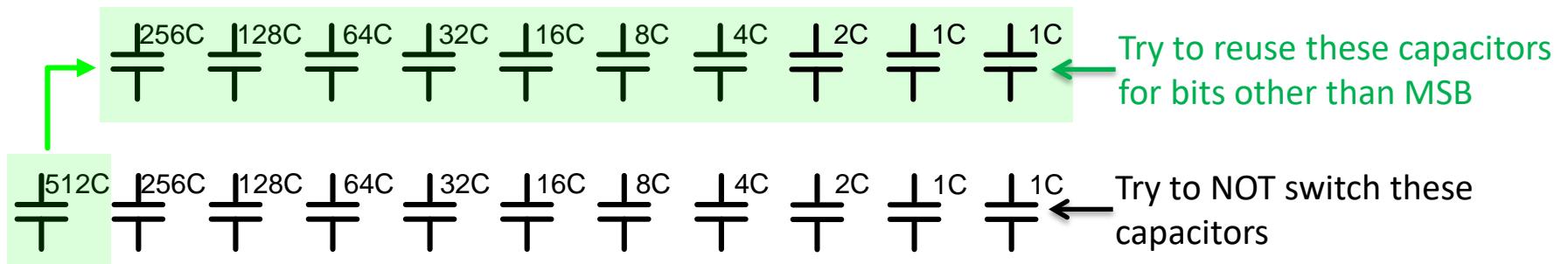
Arindam Sanyal 2014 & Long Chen 2014



- Bidirectional Single-Sided switching
 - Top-plate sampling (original BSS uses bottom plate sampling)
 - 2048 Cunit in total for 11b resolution
 - Common mode converge to V_{cm}



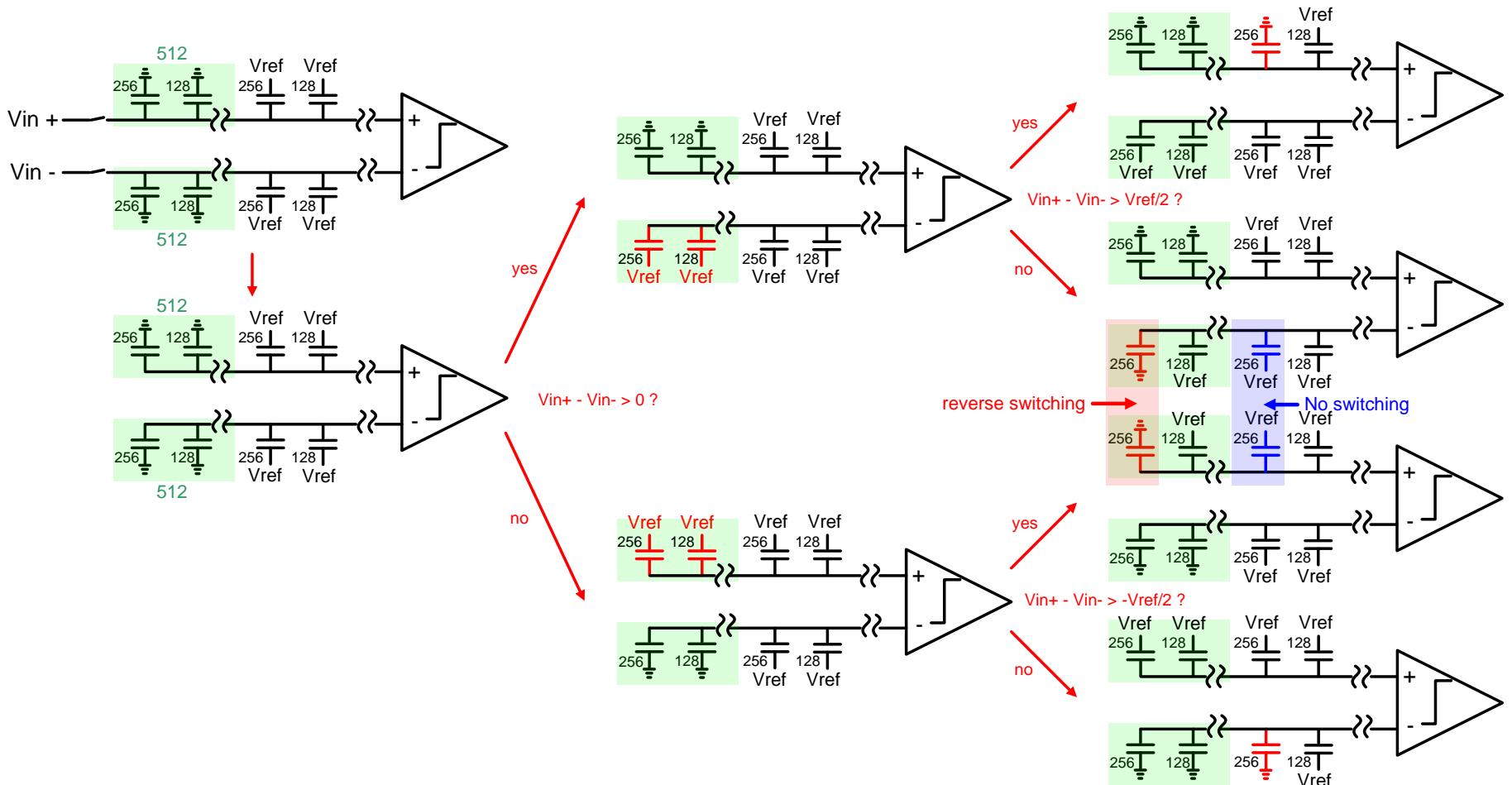
- Correlated Reverse Switching (CRS) Jen-Huan Tsai 2015
 - MSB capacitor splitted into a binary array that is the same as the rest C array
 - Switching similar to BSS, but try to reuse the splitted capacitor from MSB during conversion instead of using “new” capacitor from the rest array
 - Typically, the random errors for each capacitor accumulate during conversion
 - no correlation between error introduced by each conversion
 - If one reuses (reverse switch) a capacitor that has been already used in previous conversion cycles, then no new error is accumulated
 - Some errors are correlated



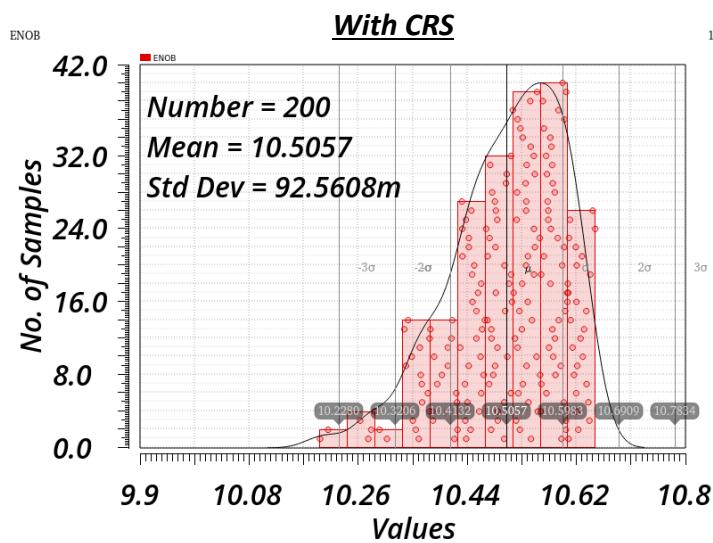
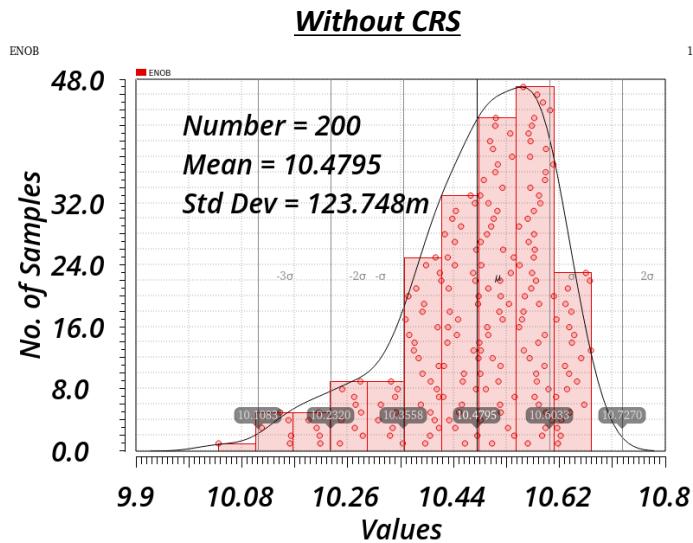
CDAC switching technique

- Correlated Reverse Switching (CRS)

Jen-Huan Tsai 2015

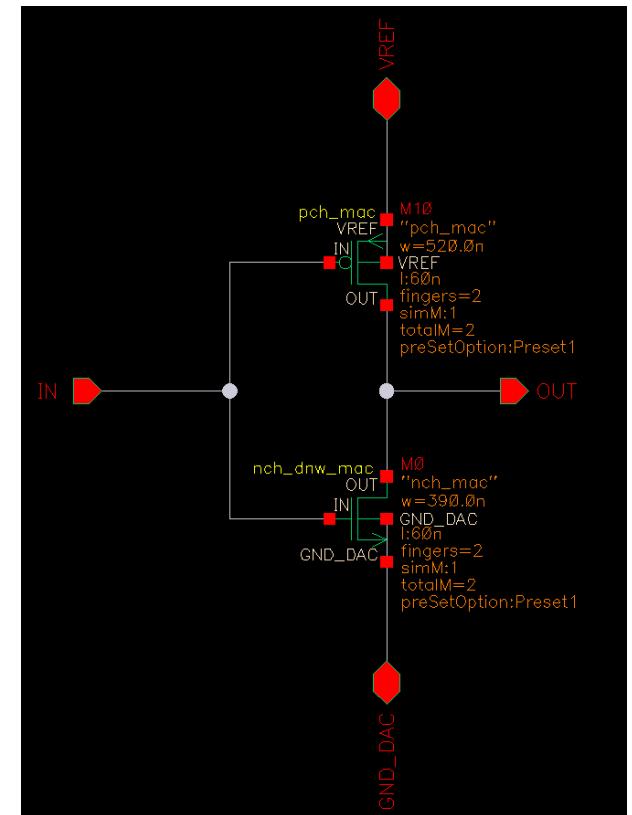
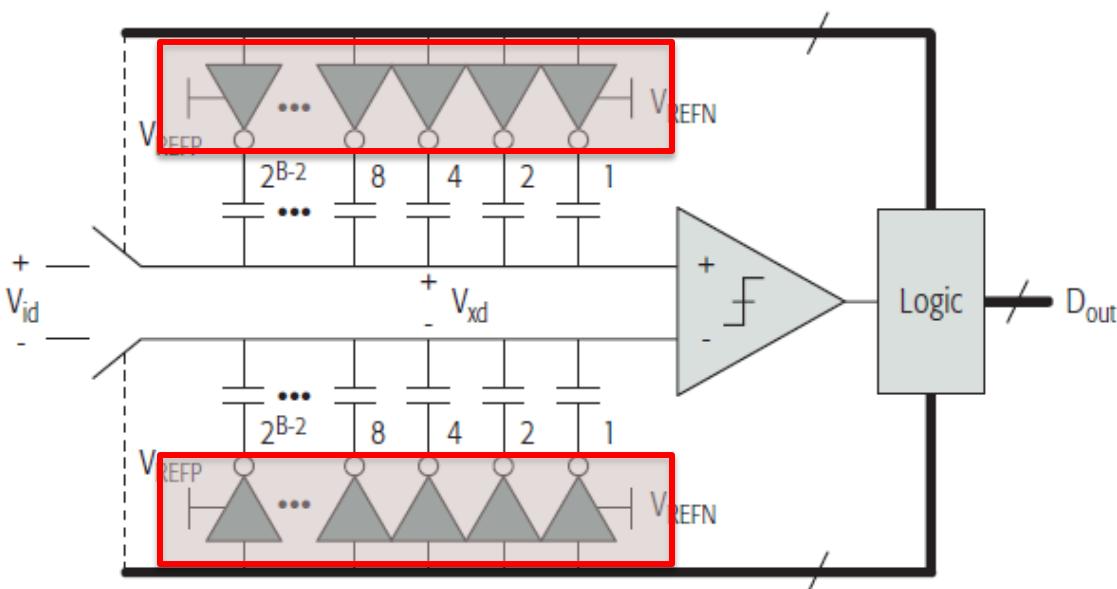


- Correlated Reverse Switching (CRS) Jen-Huan Tsai 2015
 - Schematic Monte Carlo simulation with $\frac{\sigma(C_{unit})}{C_{unit}} = 1\%$
 - Histogram of ENOB
 - Less dispersed performance with CRS
=> should be beneficial for our application (1024 ADCs in the pixel matrix)



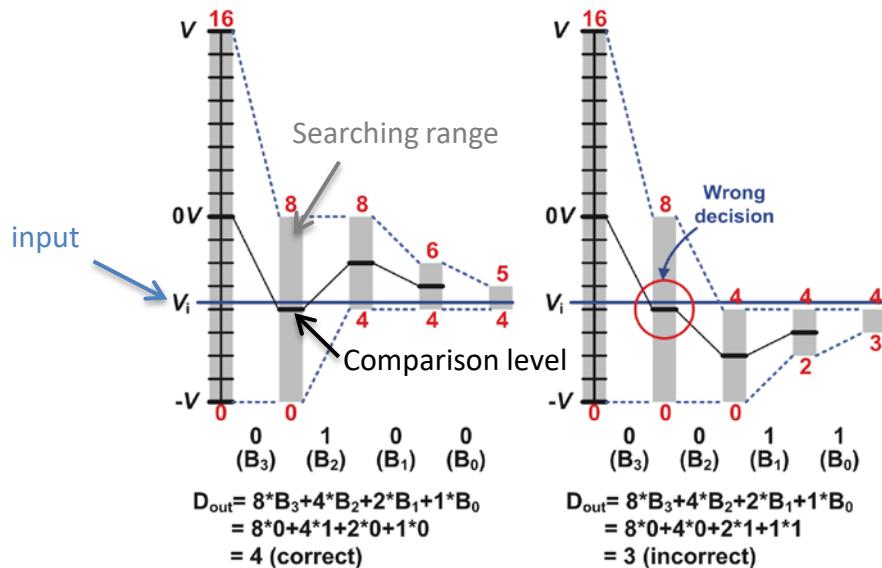
CDAC switching driver

- CDAC switching driven by inverter cells
 - Basic cell with MOS size equivalent to INVD2 from standard library
 - Two additional cells with size X2 and size X4
 - Drive 128C and 256C

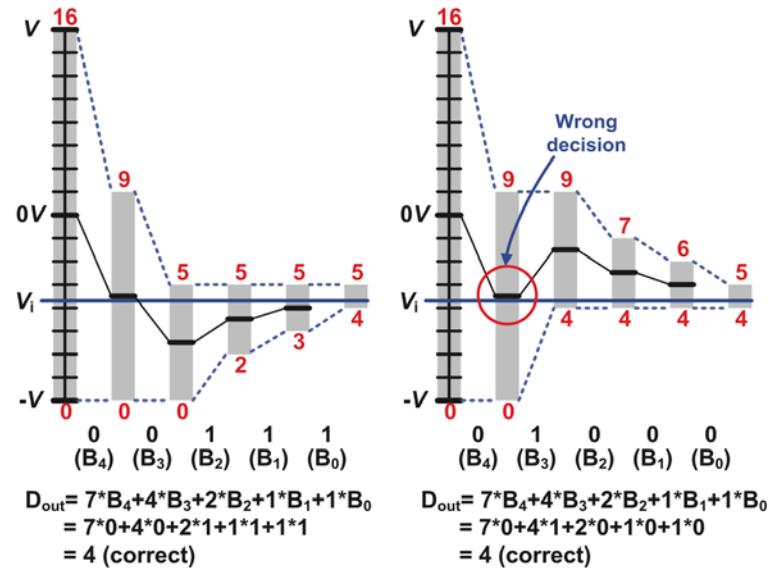


- Non-binary weighted CDAC with redundancy
 - Current bit weight < Σ weights of later bits
 - Tolerate to some extend conversion error due to incomplete settling, etc.
 - Possible to calibrate CDAC non-linearity
 - But need more bits

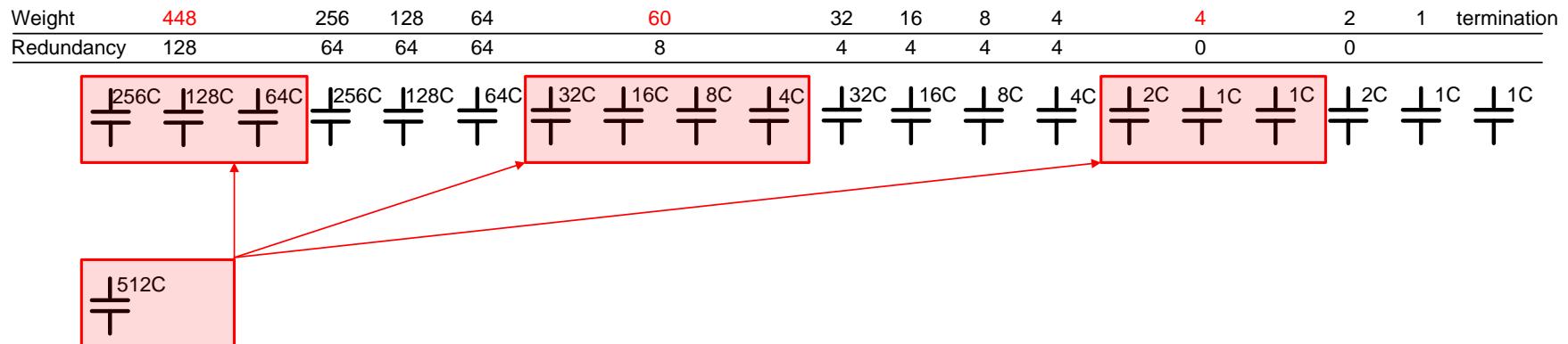
4b binary search



4b 5-step search with redundancy

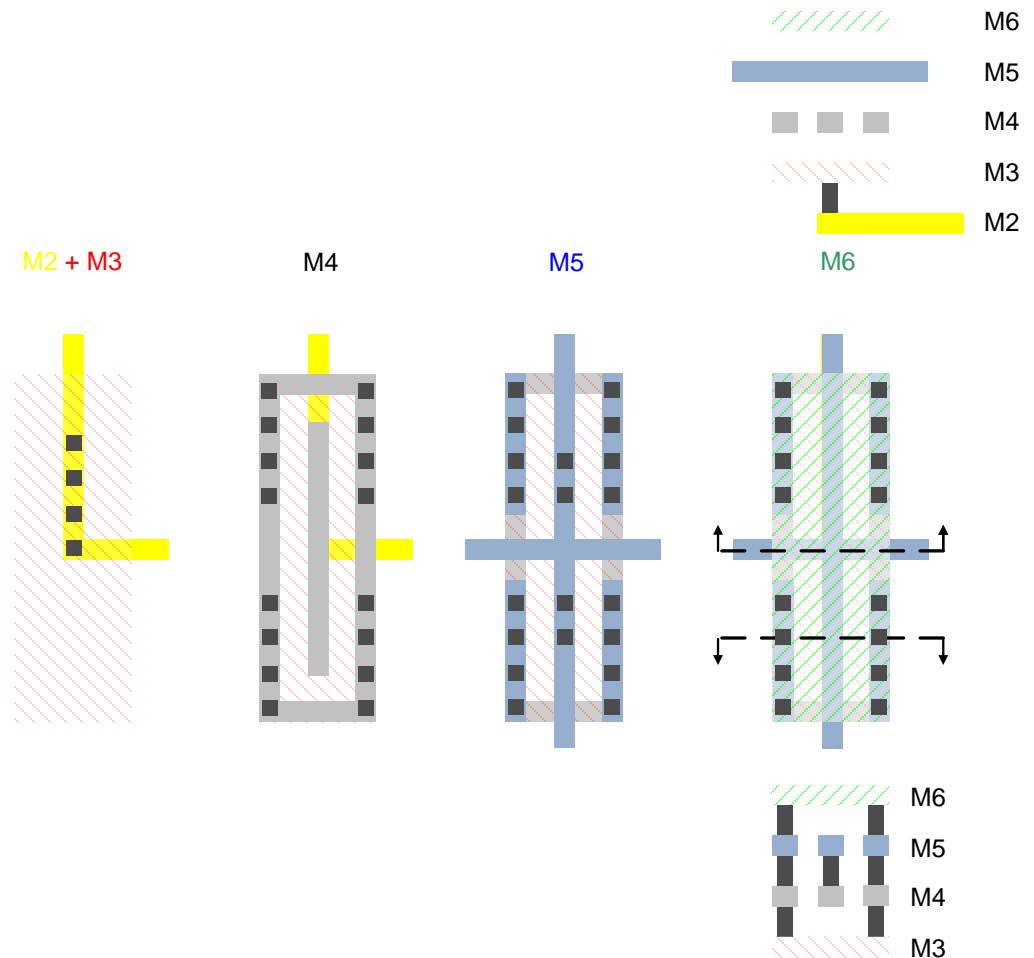
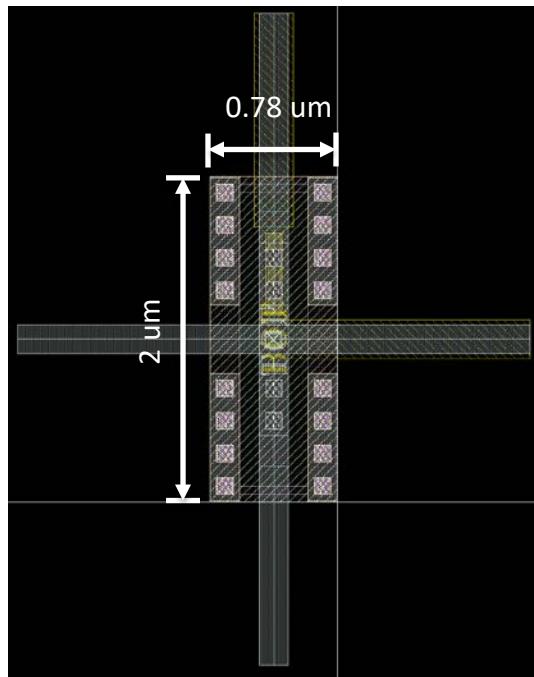


- Redundancy method: Binary-Scaled Recombination Weighting Chun-Cheng Liu, 2015
 - Reduce weights from MSB and add them to later bits
 - The total capacitor number maintained
 - All capacitor values are still power of 2 based
 - Can basically reuse the exact same CDAC array design as the one without redundancy
- The redundancy is chosen arbitrarily
 - No complete study made for optimal redundancy setting
 - 2 extra bits => 13 bit raw data for 11 bit resolution



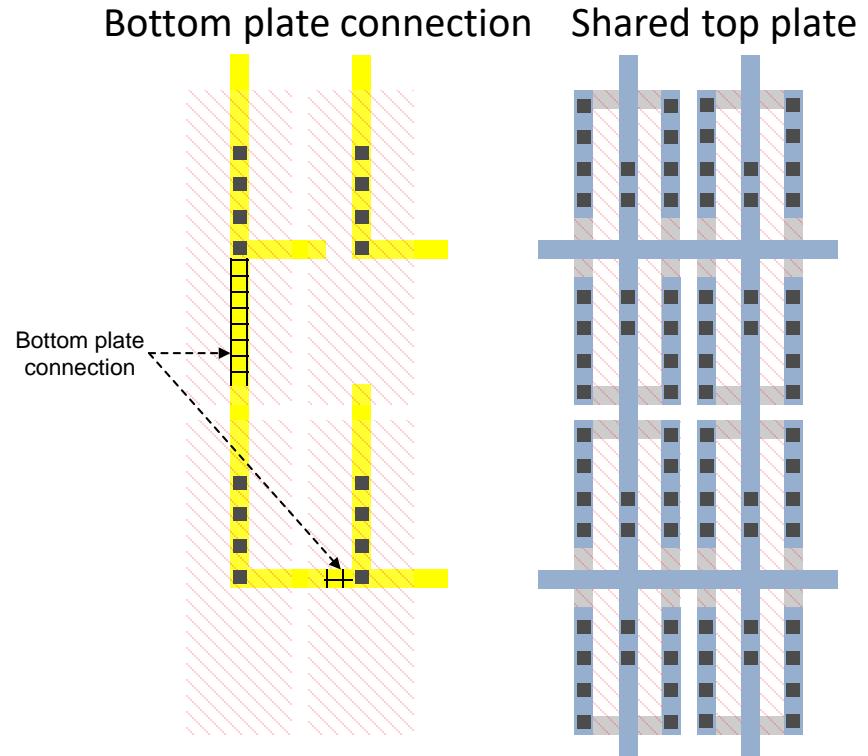
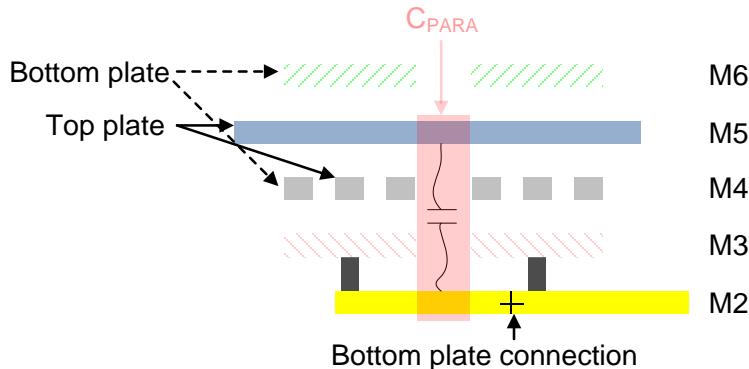
Unit capacitor design

- Concept from Wan Kim, 2016
- M3 – M6
- $\sim 940 \text{ aF}$



Unit capacitor design

- Bottom plate connection line M2 only stretched out to left and top
 - Parasitic exists between M5 (top plate) and M2 (bottom plate)
 - Each C_{UNIT} contains two and only two C_{PARA} due to M2 lines
- Top plate is shared and directly connected in M5 between neighbor C



CDAC layout

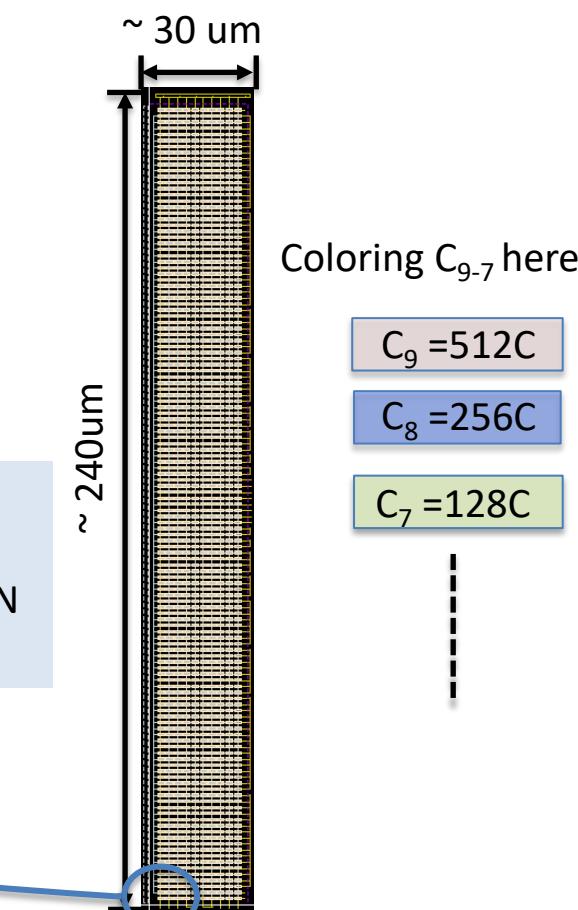
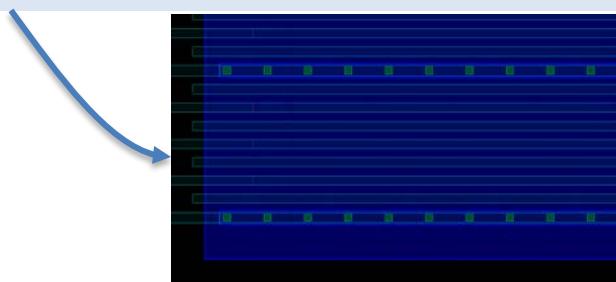
- 130 x 10 Cunit array (including dummy)
 - One dummy “ring” surrounding the main array
- “common centroid” placement
- Sampling capacitance
 - **1.077pF** in total (one side)
 - **~ 110fF** parasitic
 - Diff. KT/C noise $\sim 90\mu\text{V}$
 - LSB $\sim 1\text{mV}$ ($\sim 2\text{Vpp}$)
 - $N_Q \sim 280\mu\text{V}$

What is under the CDAC

Poly plate connected to VREF_N

M1 finger cap. => decoupling between VREF_P/N

OD dummy stripes

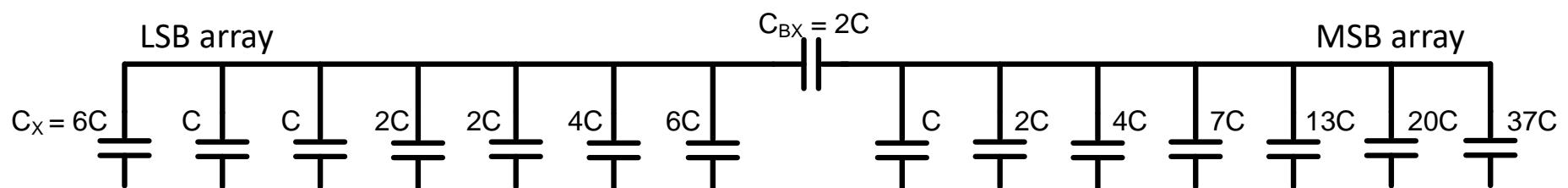


| | |
|-------|-----|
| 128 C | |
| 128 C | |
| 64 C | |
| 64 C | |
| 32 C | |
| 32 C | |
| 16 C | |
| 16 C | |
| 8 C | |
| 8 C | |
| 8 C | |
| dummy | 4 C |
| dummy | 4 C |
| 8 C | |
| 8 C | |
| 16 C | |
| 16 C | |
| 32 C | |
| 32 C | |
| 64 C | |
| 64 C | |
| 128 C | |
| 128 C | |
| 1 C | 1 C |
| 2 C | 2 C |
| 1 C | 1 C |
| | 20 |

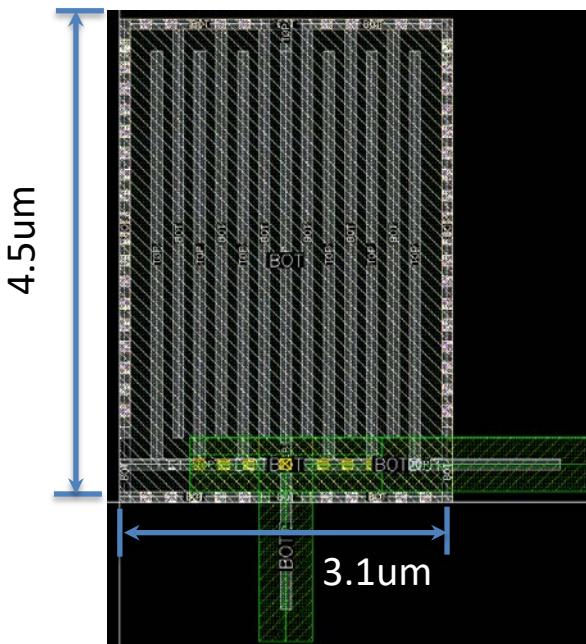
Attenuated weighting CDAC array

- Attenuated array is also widely used for high resolution SAR ADC
 - Avoid exponential increase of C elements => potentially less area
 - => But more sensitive to parasitic, especially at bridging capacitor C_{BX}
- A design borrowed from [Albert Hsu Ting Chang, 2013](#)
 - Design only include unit value C => use $C_{BX} = 2*C_{unit}$ as bridging capacitor
 - Avoid voltage on LSB arrays go beyond rails => Add an additional C_x on LSB array

| weight | 444 | 240 | 156 | 84 | 48 | 24 | 12 | 6 | 4 | 2 | 2 | 1 |
|------------|-----|-----|-----|----|----|----|----|---|---|---|---|---|
| redundancy | 136 | 100 | 28 | 16 | 4 | 4 | 4 | 4 | 2 | 2 | 0 | 0 |

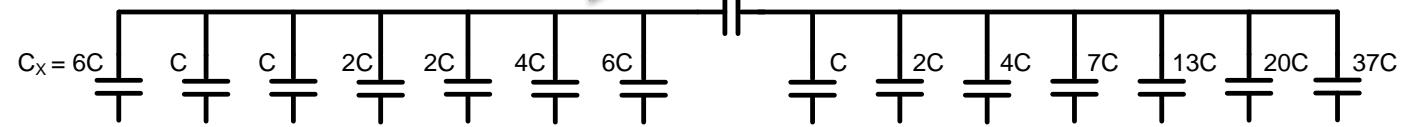
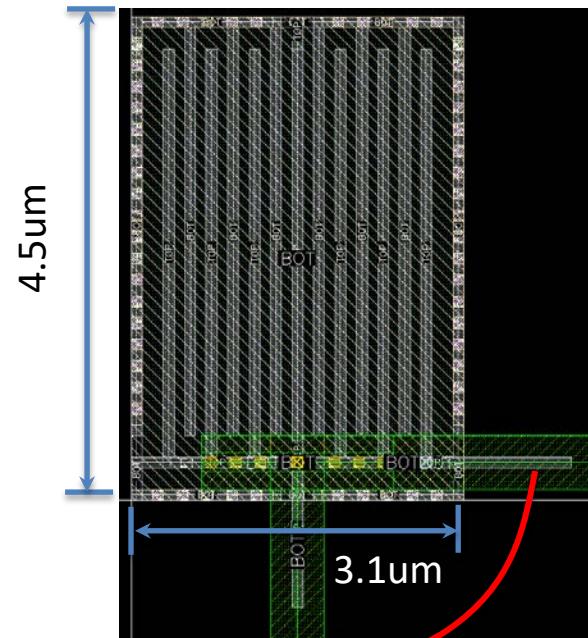
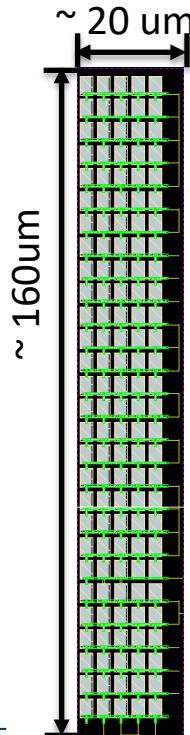


- Similar concept as shown previously, only more fingers
- M3 – M7
 - Top plate M5
 - Bottom plate routing with M2 as well as M7
 - M7 to shield the shared M5 top plate lines in order to avoid parasitic to other nets
- $\sim 11.7\text{fF} \Rightarrow$ value not driven by matching (hard to estimate), but rather to C_{sample}



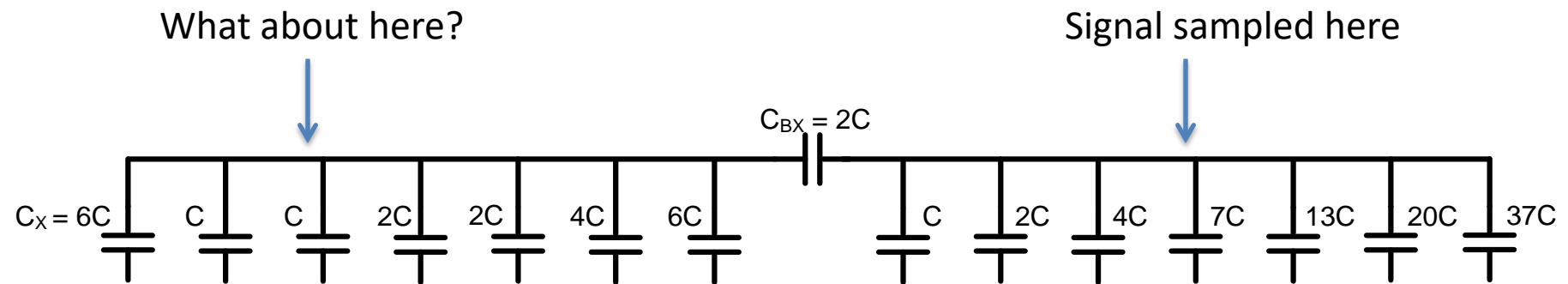
Layout – Attenuated weighting CDAC array

- 28 x 5 Cunit array (including dummy) - much less area than the former CDAC
 - One dummy column on left => no dummy on left to avoid parasitic on LSB top plate
 - LSB top plate parasitic $\sim 200\text{aF}$
 - Not very “common centroid”
- Sampling capacitance $\sim 1.1\text{pF}$ (one side)
 - Parasitic $\sim 100\text{fF}$



One question

- Do we need to reset the top plate of LSB array during sampling?
 - Comment from Marek => leave it floating!

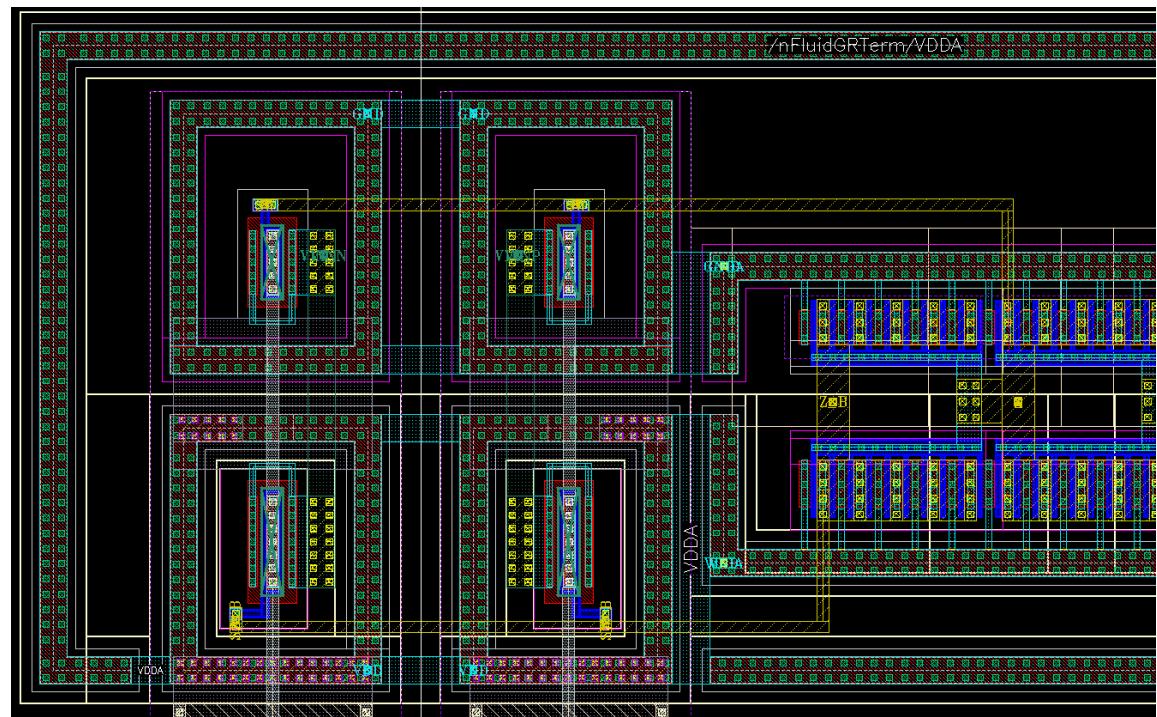
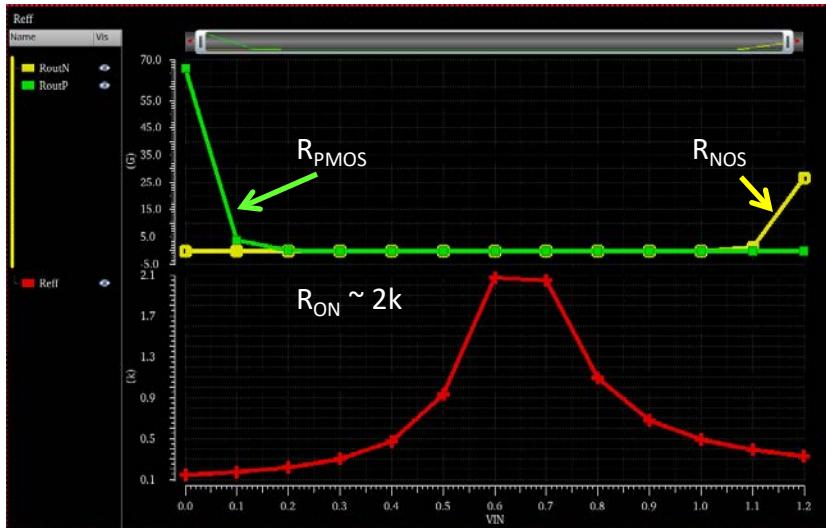


Sampling switches

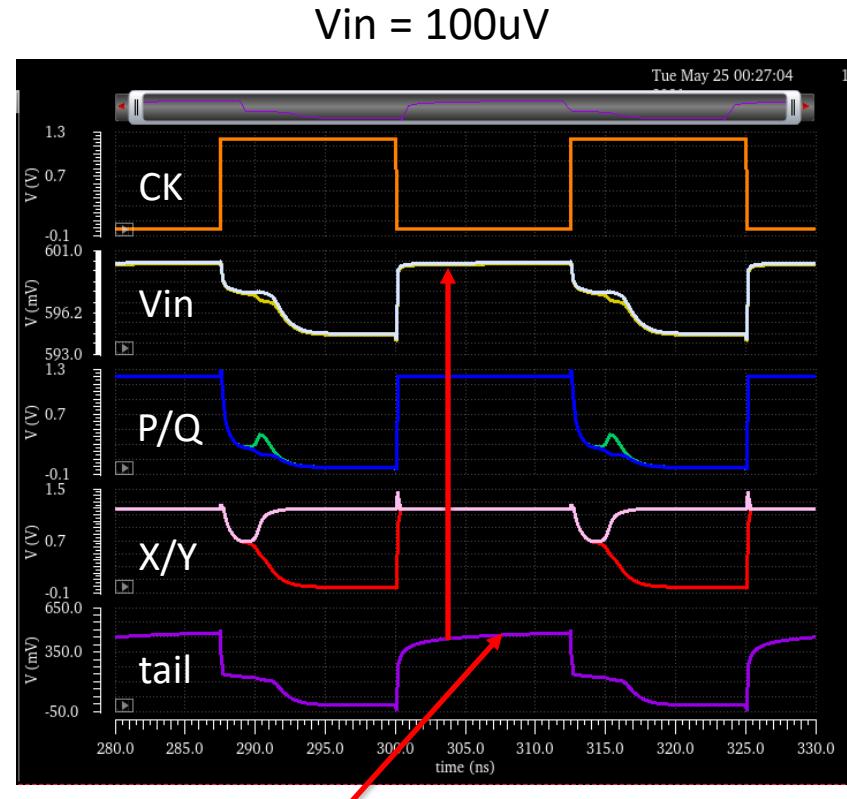
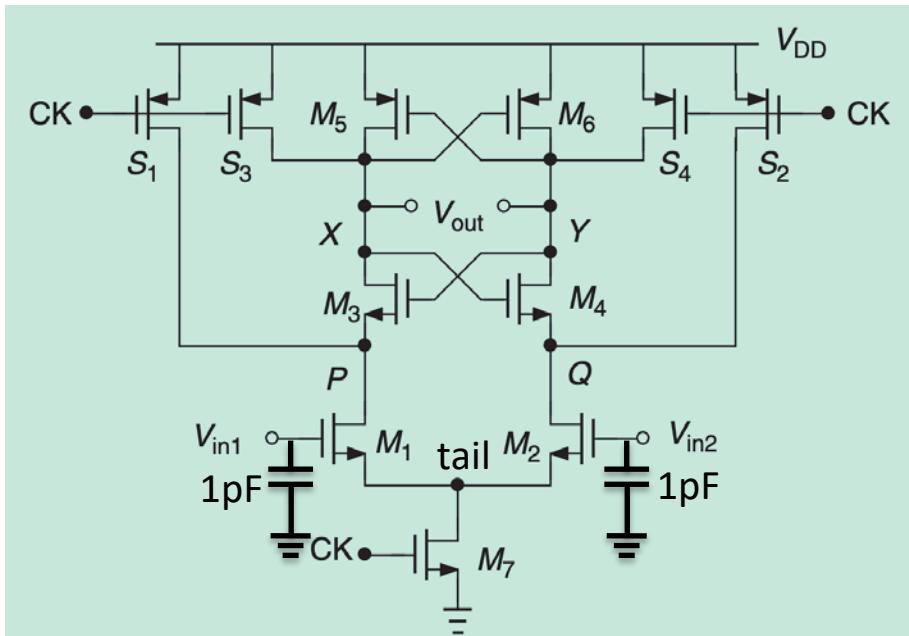
- Transmission-gate based sampling switches
 - Settling time is the main consideration – sample static signal only
 - 75ns – 125ns expected for sampling phase
 - Enclosed layout to minimize the leakage after TID
 - PMOS is also enclosed mostly for nicer layout

$$\begin{aligned} \text{NMOS} &= 2.5\mu/0.6\mu \\ \text{PMOS} &= 3.5\mu/0.6\mu \end{aligned}$$

$R = 2k$, $C=1p$
Settling to 0.01% need $\sim 20\text{ns}$



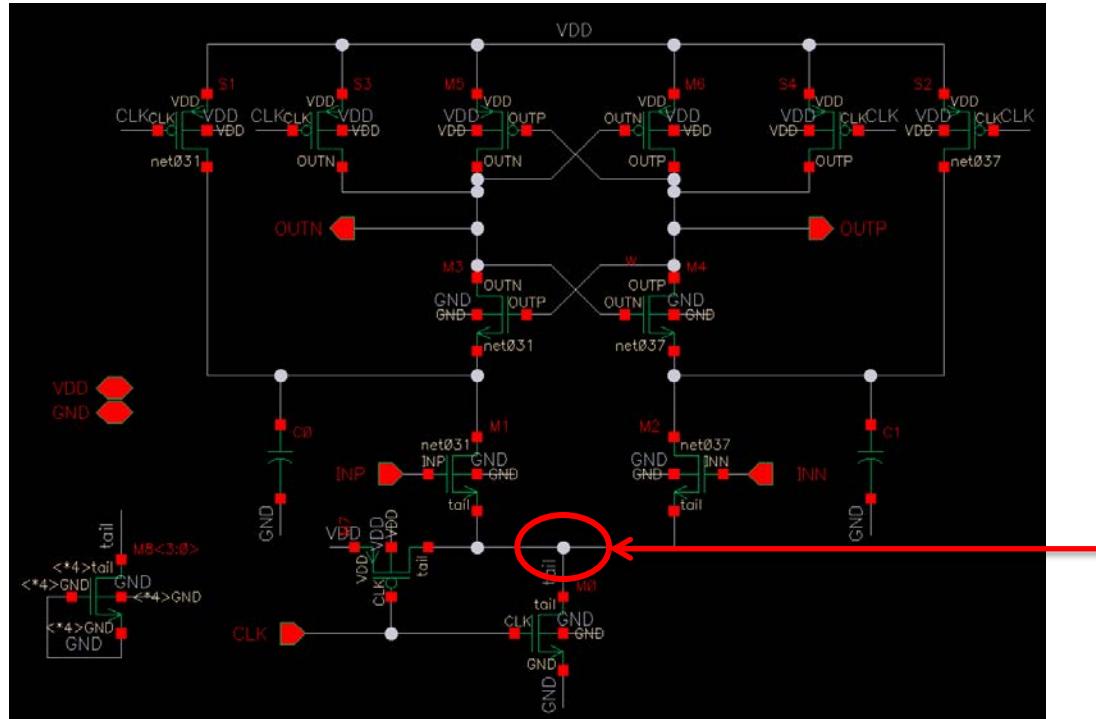
- Conventional regenerative latch



Undefined potential during reset

Comparator

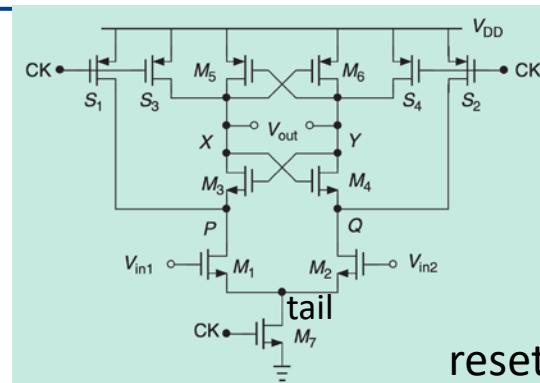
- Conventional regenerative latch



reset to VDD during reset phase

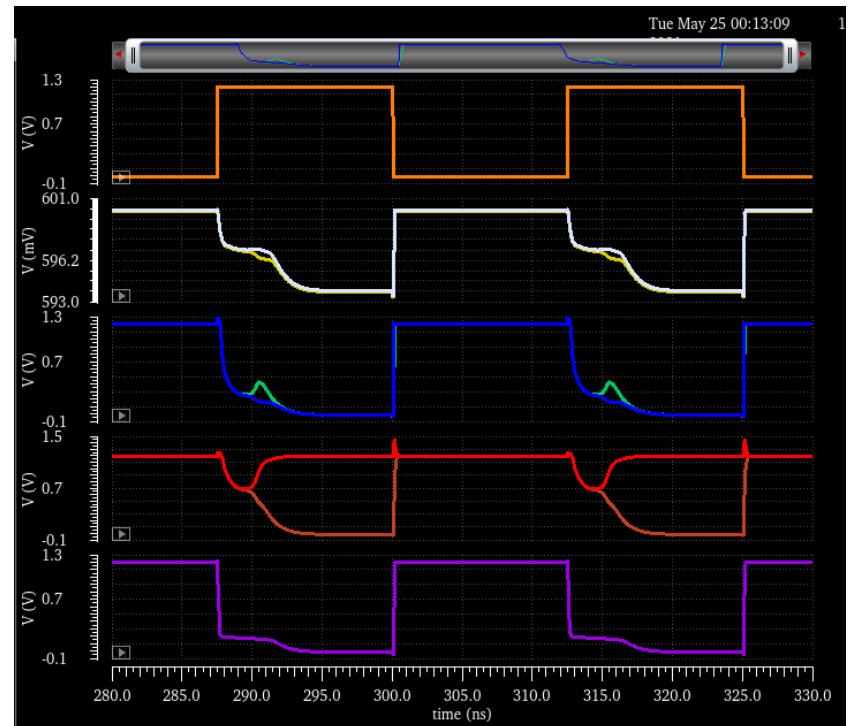
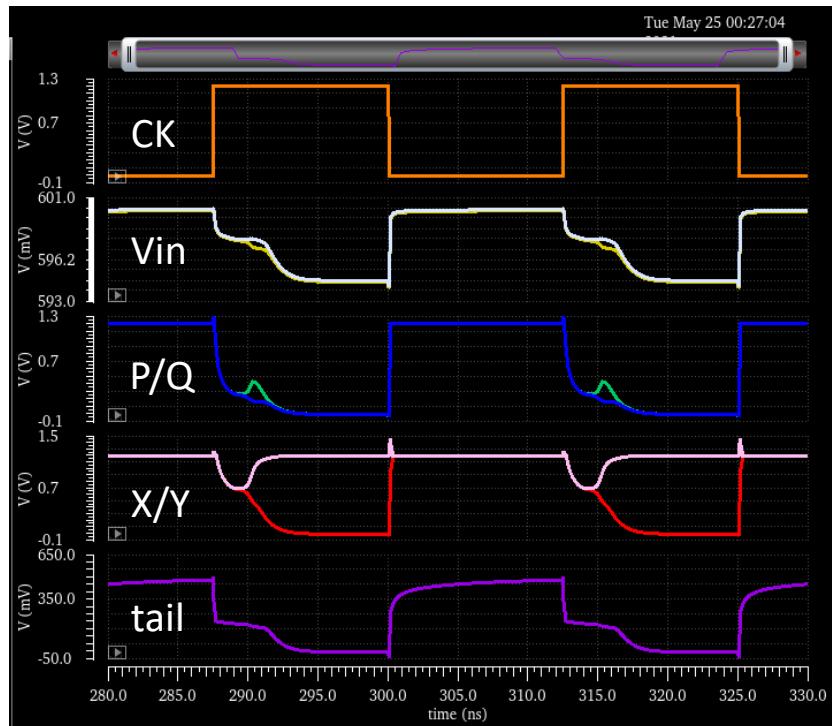
Comparator

- Waveform comparison



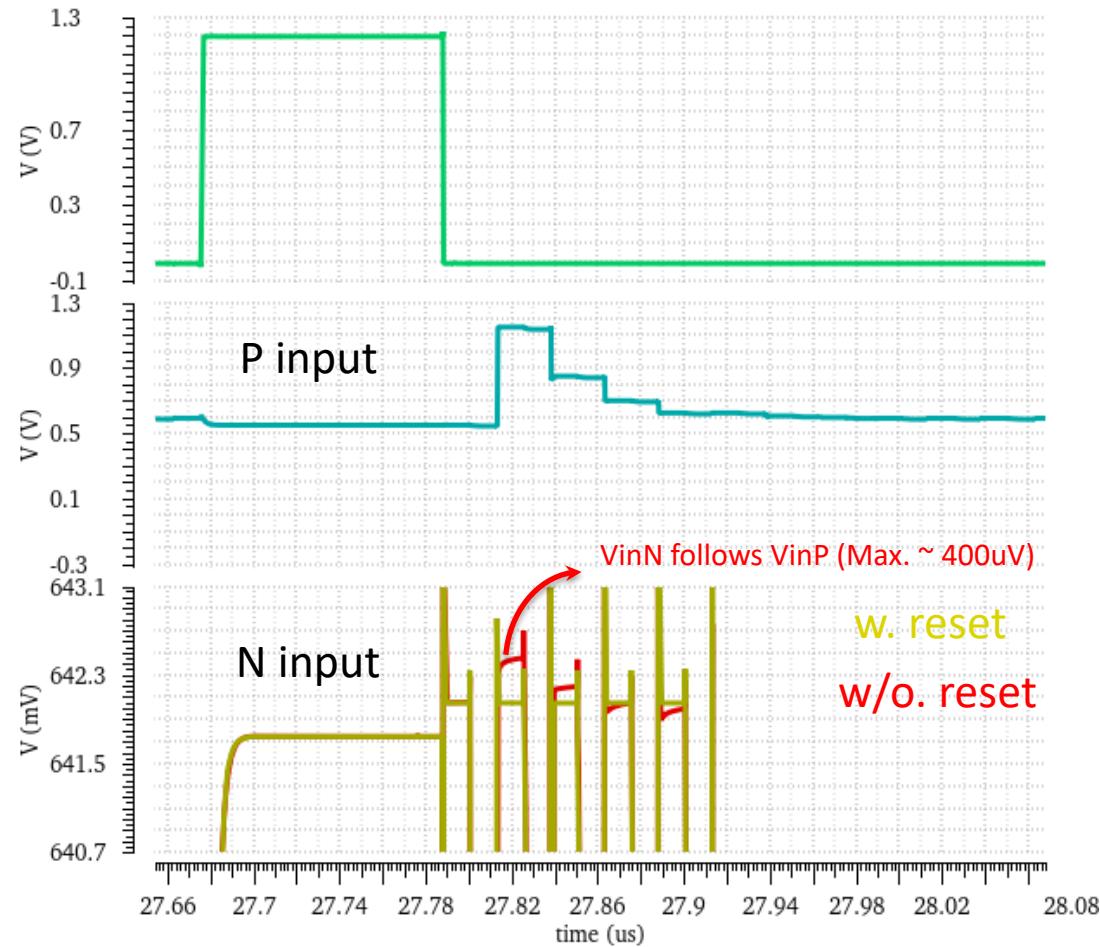
w/o reset the drain of tail transistor

reset the drain of tail transistor



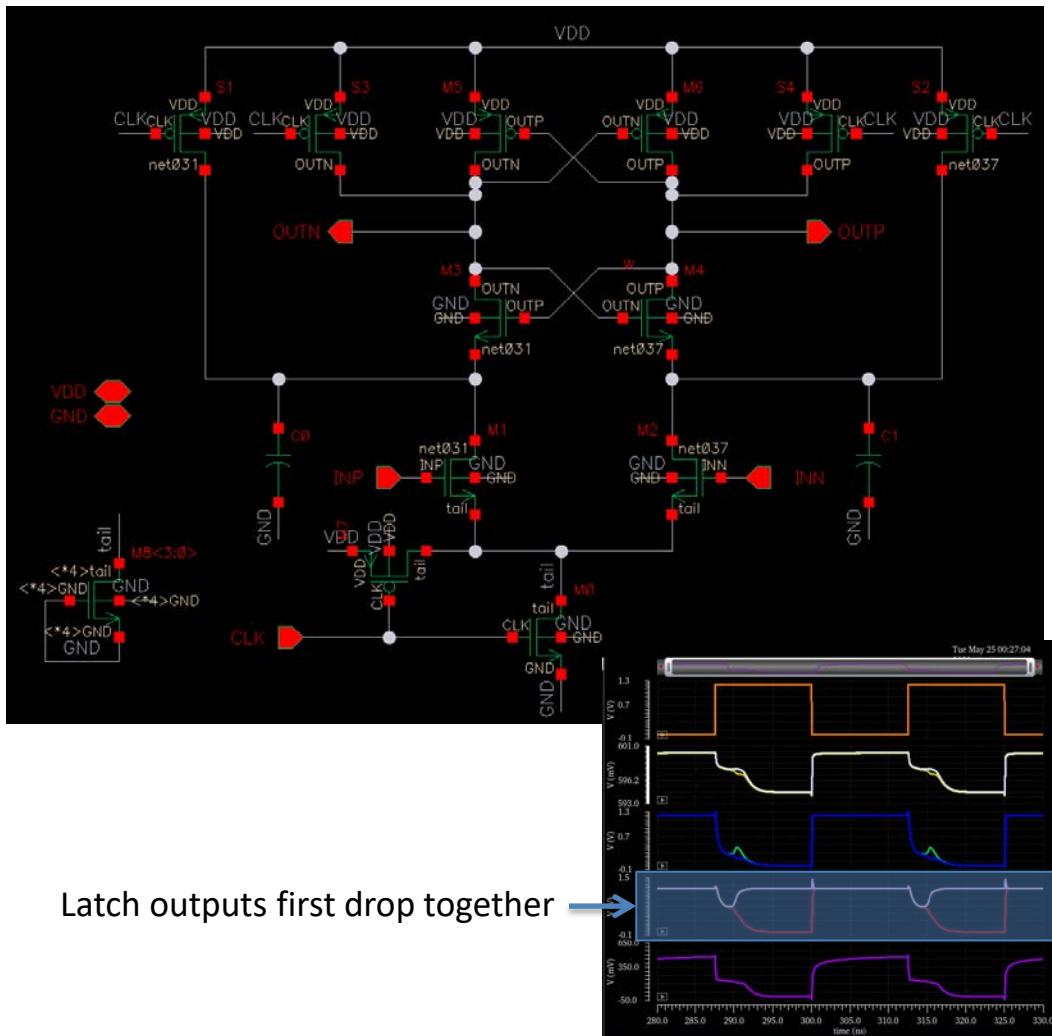
Comparator

- Reset tail transistor drain also helps to remove feedthrough between two inputs

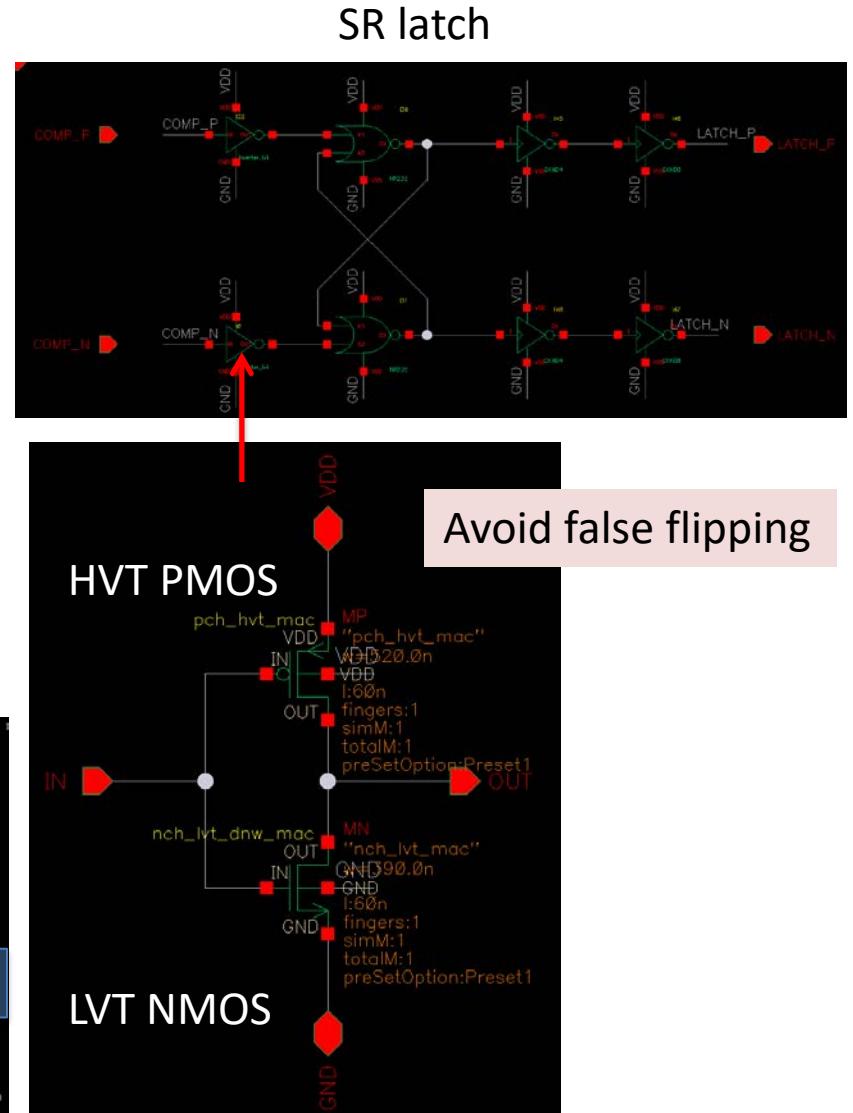


Comparator

- Conventional regenerative latch

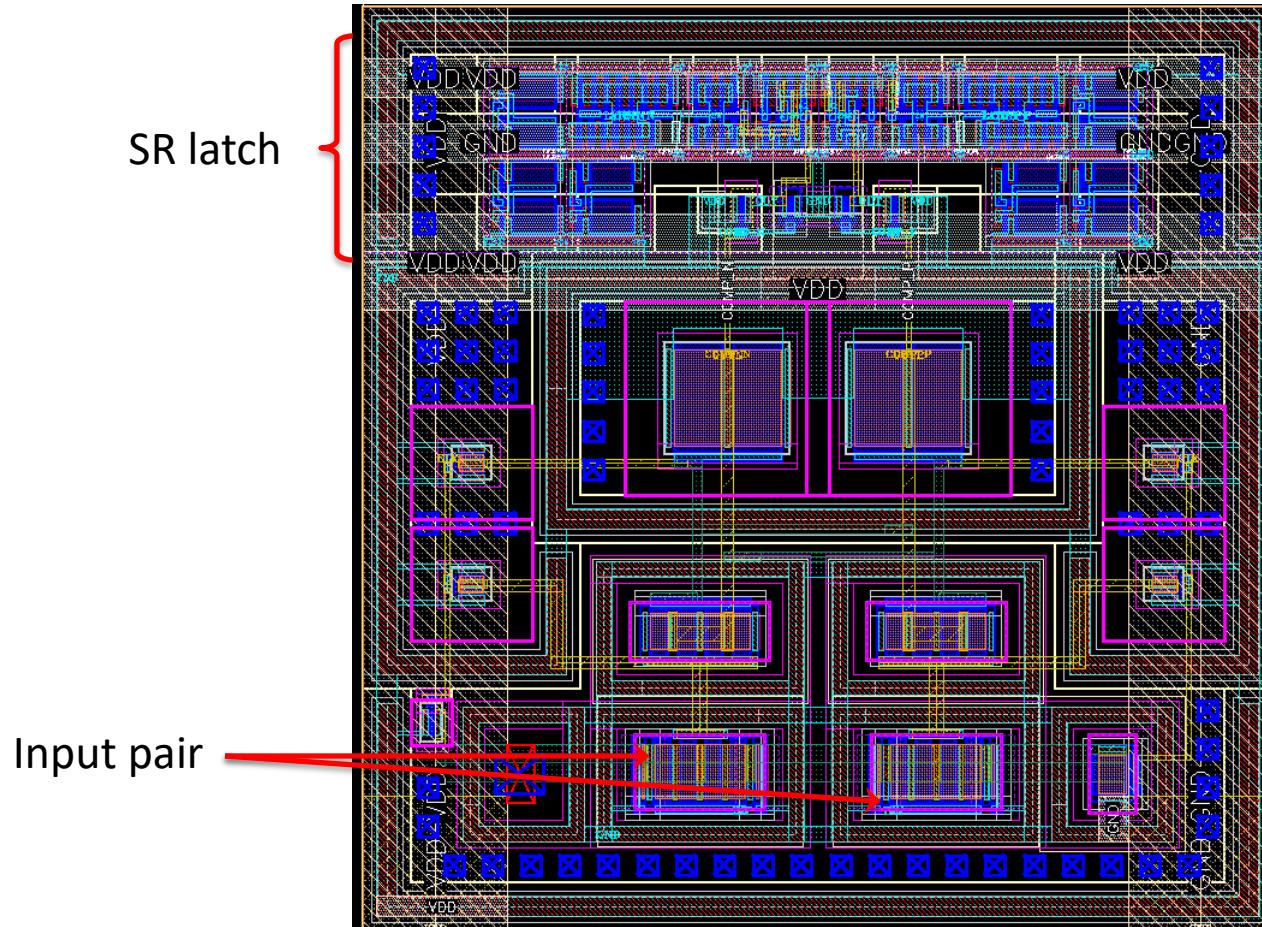


Latch outputs first drop together



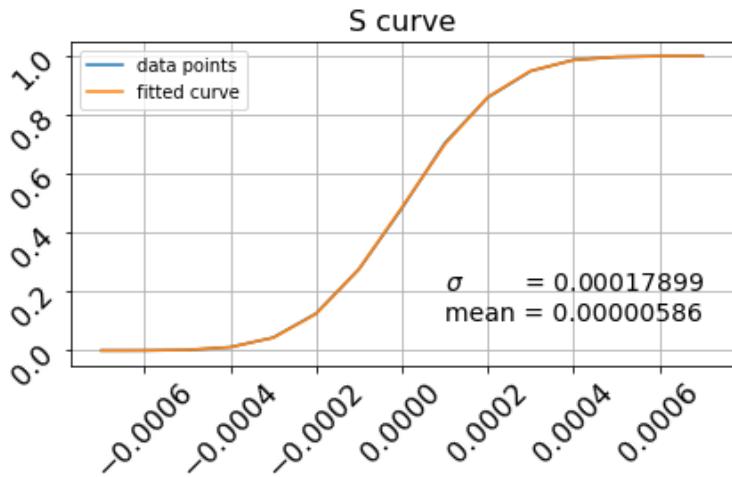
Comparator

- Layout
 - ~ 20um by 20um

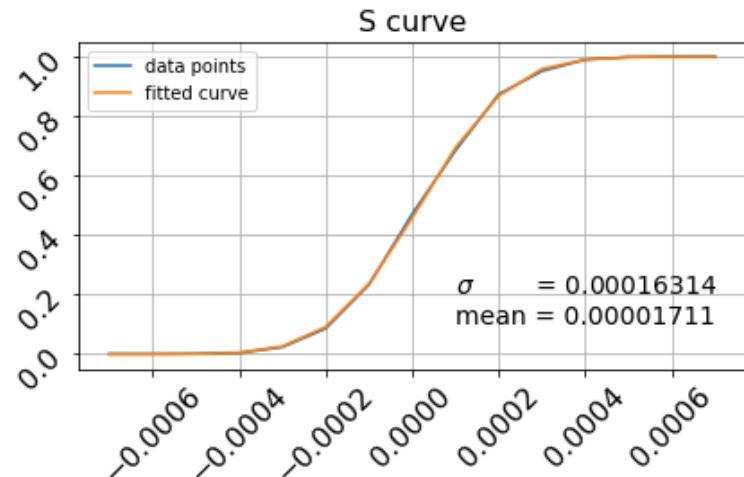


- Noise simulation (transient)
 - Noise level $\sim 160\text{uV}$ in post layout (vs $\sim 280\text{uV} N_Q$)

Schematic

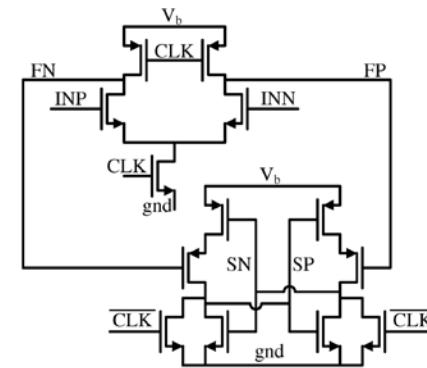
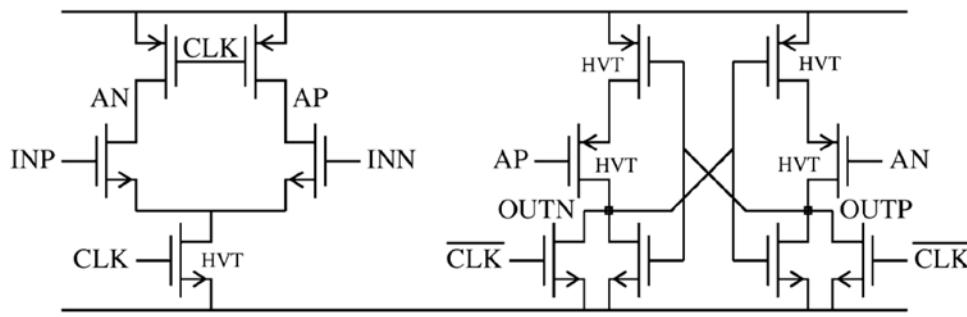


RC extracted (QRC FS)

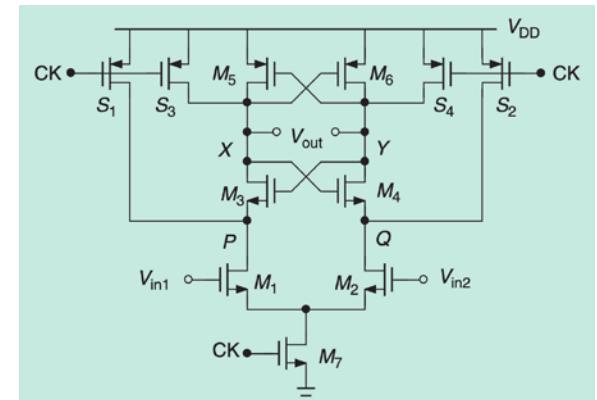


- Power
 - Average current: **6.38/6.73uA**
 - Peak current $\sim 800\text{uA}$

- Two other comparator structures are implemented as individual test circuit
 - Designed by another person (Themis) => more power, but less noise
 - See reports in SOS repository

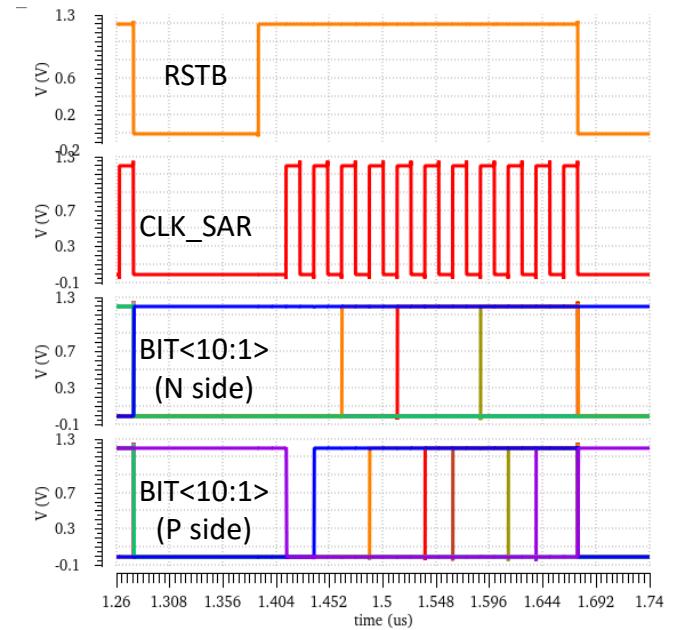
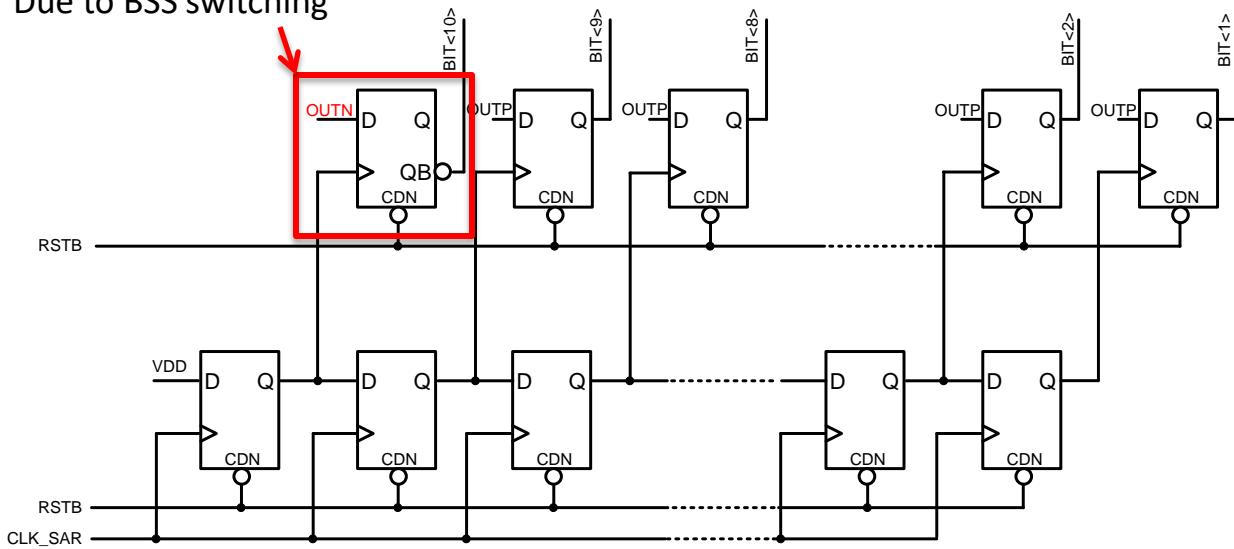


- In addition, a conventional latch with additional loading is implemented
 - Custom fringe capacitor added at P/Q and X/Y node
 - $C_{X/Y}=6.5\text{fF}$, $C_{P/Q}=1.3\text{fF}$
 - Decrease the noise from $\sim 163\mu\text{V}$ to $\sim 148\mu\text{V}$



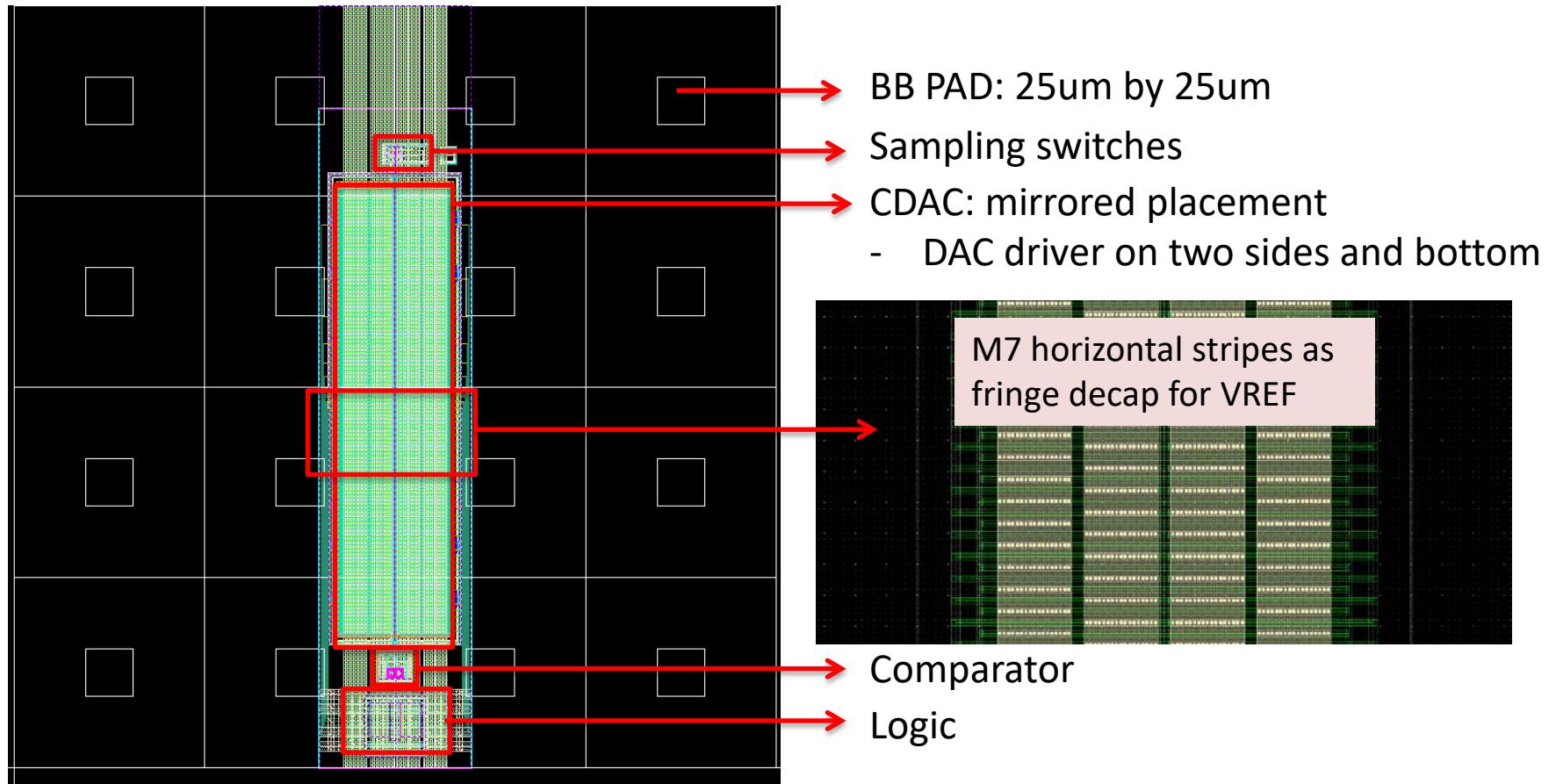
- Composed of two shift register chain
 - Use standard library cells

Due to BSS switching



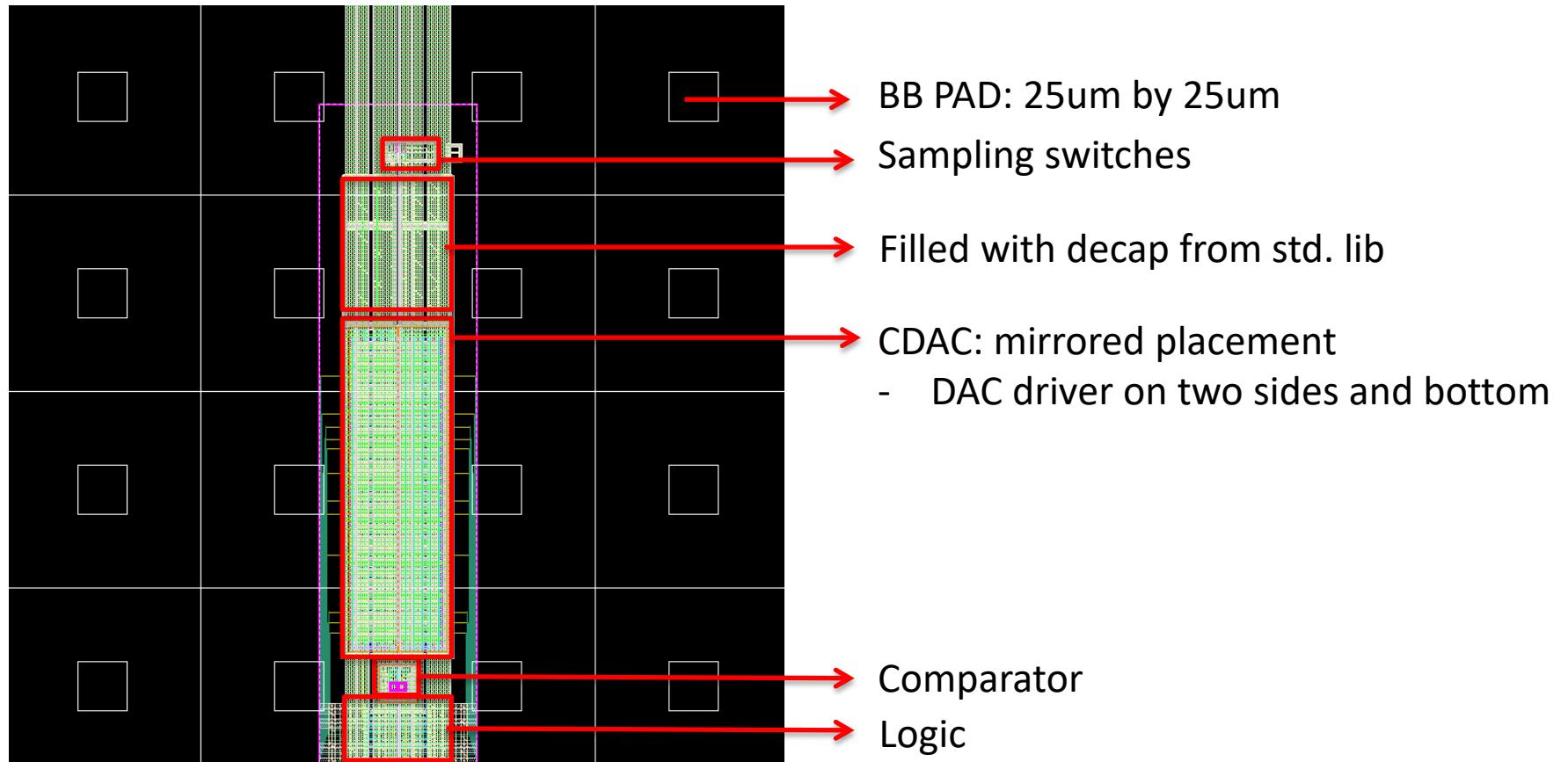
ADC layout

- Width ~ 80um, height ~ 330um
- Core circuit using M1 – M6, M8 – M10 (thick metal) for PG and VREF

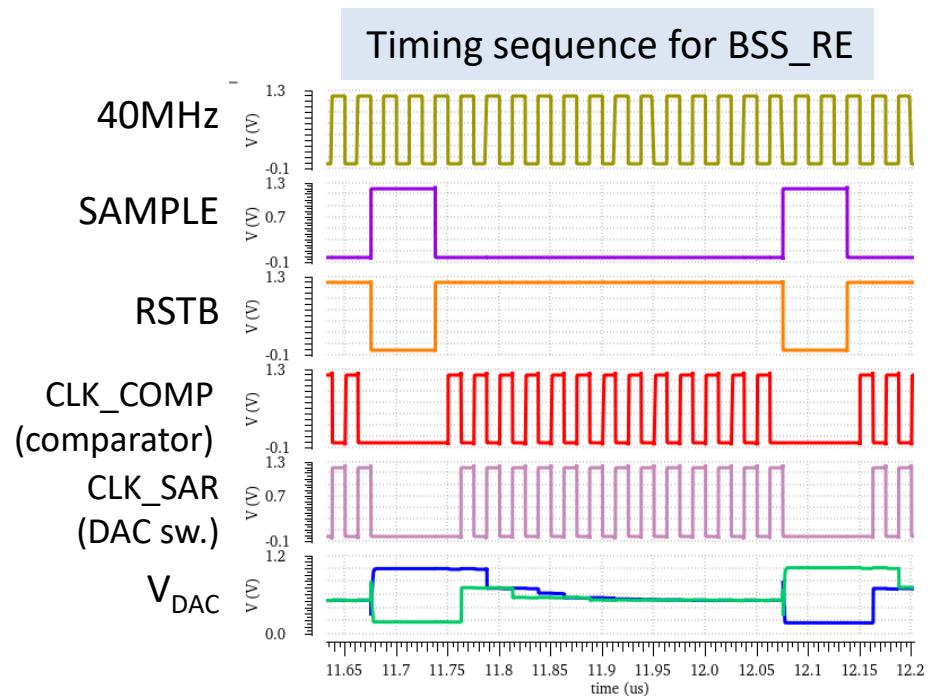
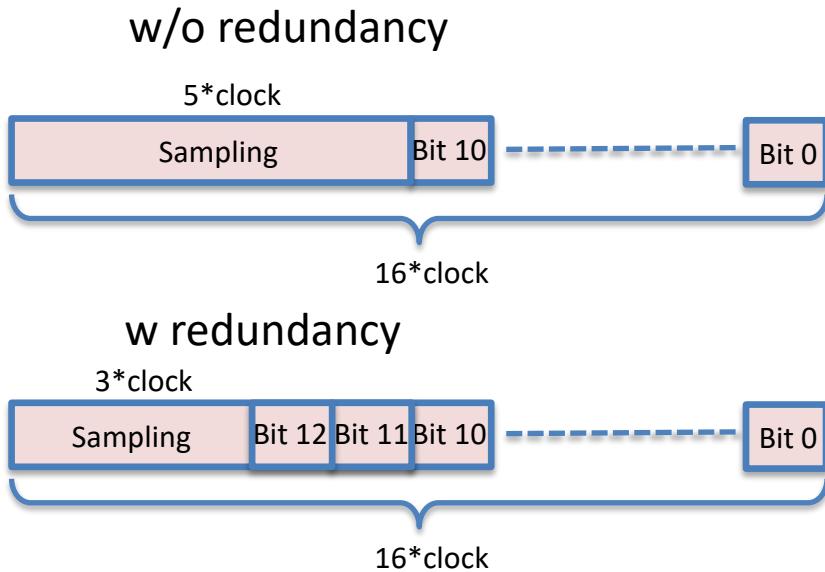


ADC layout – attenuated array

- Width ~ 80um, height ~ 330um (the same floorplan for easier top layout int.)
- Core circuit using M1 – M7, M8 – M10 (thick metal) for PG and VREF

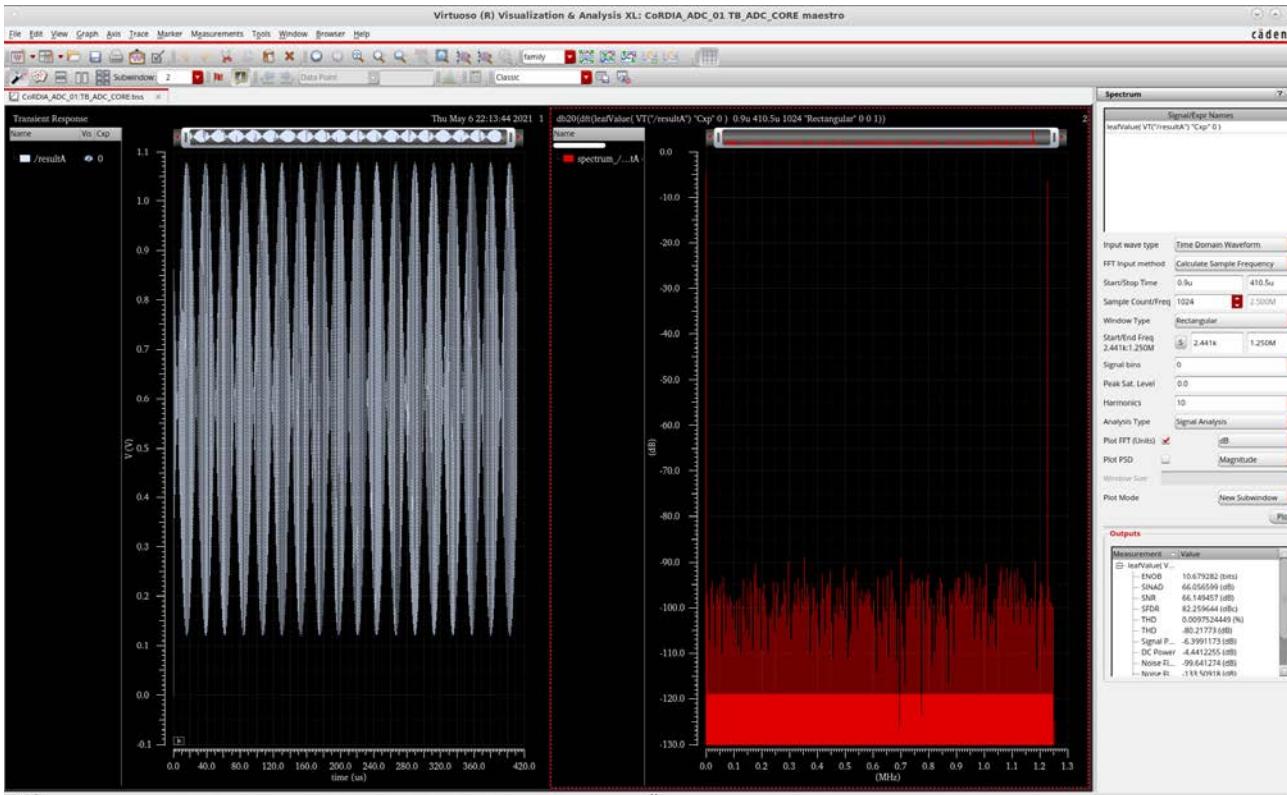


- Synchronous operation
 - Expected to be driven by 40MHz clock => all control sequence derived from this clock
 - 16 clock cycles for one conversion => 2.5 MS/s
 - Each conversion step takes 1 clock = 25ns
 - Normal ADC has 11 raw bit, redundancy takes another 2 bits (2 clock less sampling time)
 - In this prototype, all control sequence given **externally** => More flexible for circuit evaluation



ENOB simulation

- Fsample = 2.5MS/s
- Sine input
 - Fin = $(503/1024) * \text{Fsample} \sim 1.228\text{MHz}$
 - Input amplitude 2 Vpp (**smaller than full scale**) => will have artificially smaller ENOB
- Spectrum analysis with 1024 points



ENOB simulation summary

Schematic simulation

| Cell | BSS | BSS RE | CRS | BSS AW RE |
|------|-------|--------|-------|-----------|
| ENOB | 10.67 | 10.67 | 10.67 | 10.68 |

Schematic with transient noise (noisefmax = 10G)

| Cell | BSS | BSS RE | CRS | BSS AW RE |
|------|-------|--------|-------|-----------|
| ENOB | 10.45 | 10.47 | 10.49 | 10.5 |

C

| Cell | BSS | BSS RE | CRS | BSS AW RE |
|------|-------|--------|-------|-----------|
| ENOB | 10.92 | 10.9 | 10.92 | 10.83 |

C QRC/QUANTUS field solver

| Cell | BSS | BSS RE | CRS | BSS AW RE |
|------|-------------|--------|-------|-----------|
| ENOB | 10.08/10.82 | 10.2 | 10.72 | 10.58 |

RC

| Cell | BSS | BSS RE | CRS | BSS AW RE |
|------|--------|--------|-----|-----------|
| ENOB | 10.896 | -- | -- | -- |

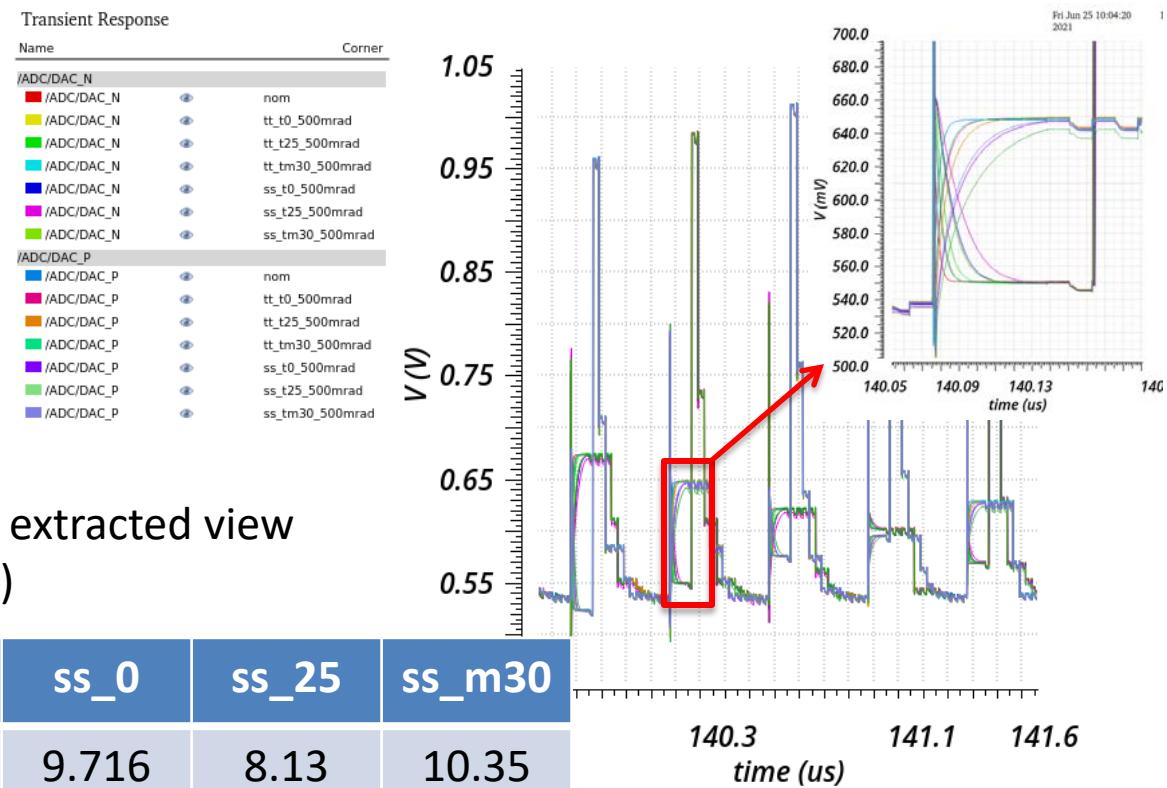
C only view

| Cell | BSS | BSS RE | CRS | BSS AW RE |
|---------|---------|---------|---------|-----------|
| Digital | 13.77uA | 14.56uA | 14.79uA | 14.49uA |
| VREF | 5.323uA | 5.28uA | 4.2uA | 3.626 |

RC view

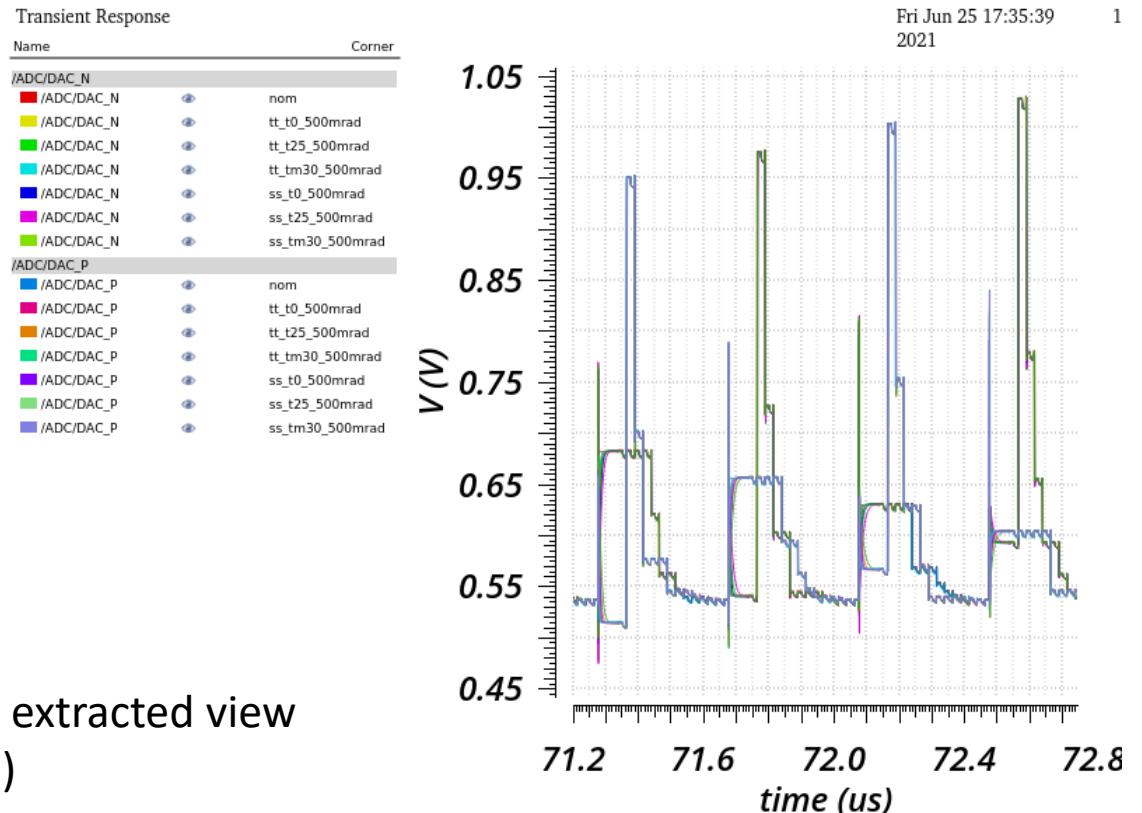
| Cell | BSS | BSS RE | CRS | BSS AW RE |
|---------|---------|--------|-----|-----------|
| Digital | 13.73uA | -- | -- | -- |
| VREF | 5.313uA | -- | -- | -- |

- Use 500Mrad transistor model to simulate ENOB
 - 3 temperature: -30, 0, 25
 - 2 transistor corner: tt, ss
- More problematic for ADC with redundancy => less time for sampling (75ns)
 - ss corner doesn't fully settle



| Corner | tt_0 | tt_25 | tt_m30 | ss_0 | ss_25 | ss_m30 |
|--------|-------|-------|--------|-------|-------|--------|
| ENOB | 10.98 | 10.96 | 10.87 | 9.716 | 8.13 | 10.35 |

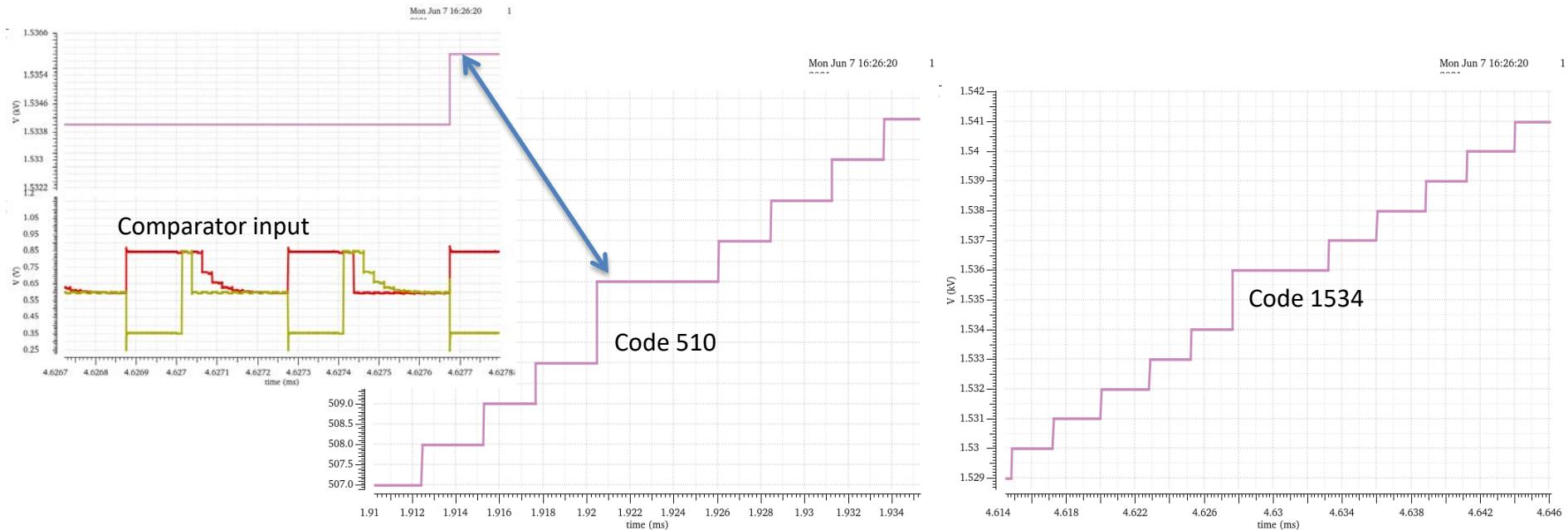
- Change normal VT transistor to LVT for sampling switches



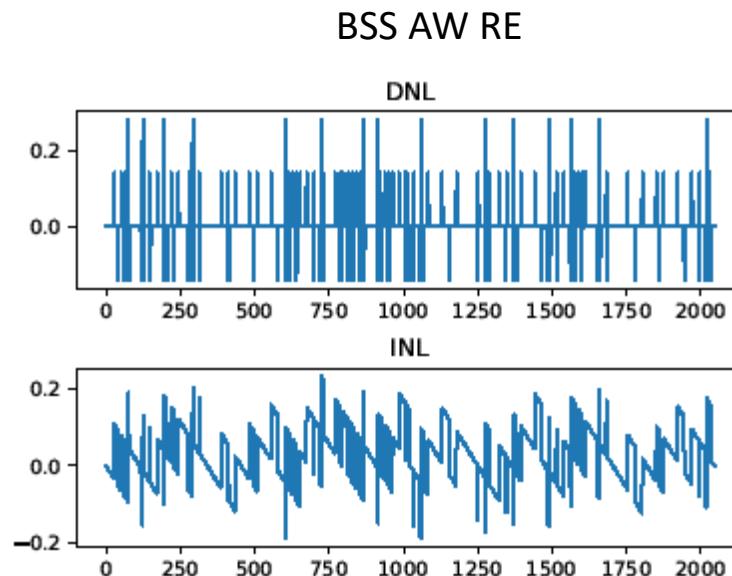
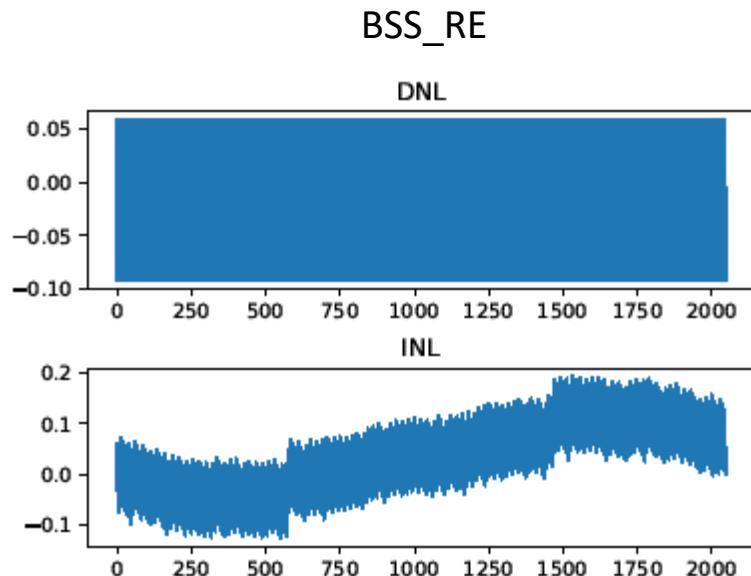
| Corner | tt_0 | tt_25 | tt_m30 | ss_0 | ss_25 | ss_m30 |
|--------|-------|-------|--------|------|-------|--------|
| ENOB | 11.01 | 11.01 | 10.85 | 11 | 10.73 | 11 |

Ramping scan

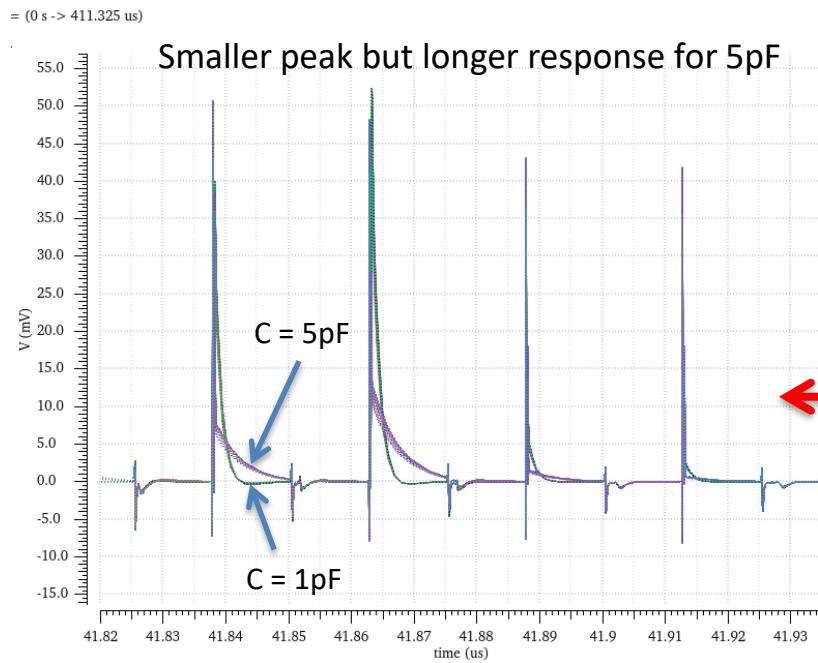
- Input ramping from 0 to 2.4V
 - slow enough ($> 6\text{ms}$) to have good code coverage => ~ 8 samples/LSB range
- Two missing code happens for BSS and CRS
 - Happens when two inputs close to each other after first switching
 - Common mode elevated
 - Comparator has common mode dependent offset => decision error



- This effects not shown for ADC with redundancy
 - Equivalent to decision error for the second conversion recovered by redundancy

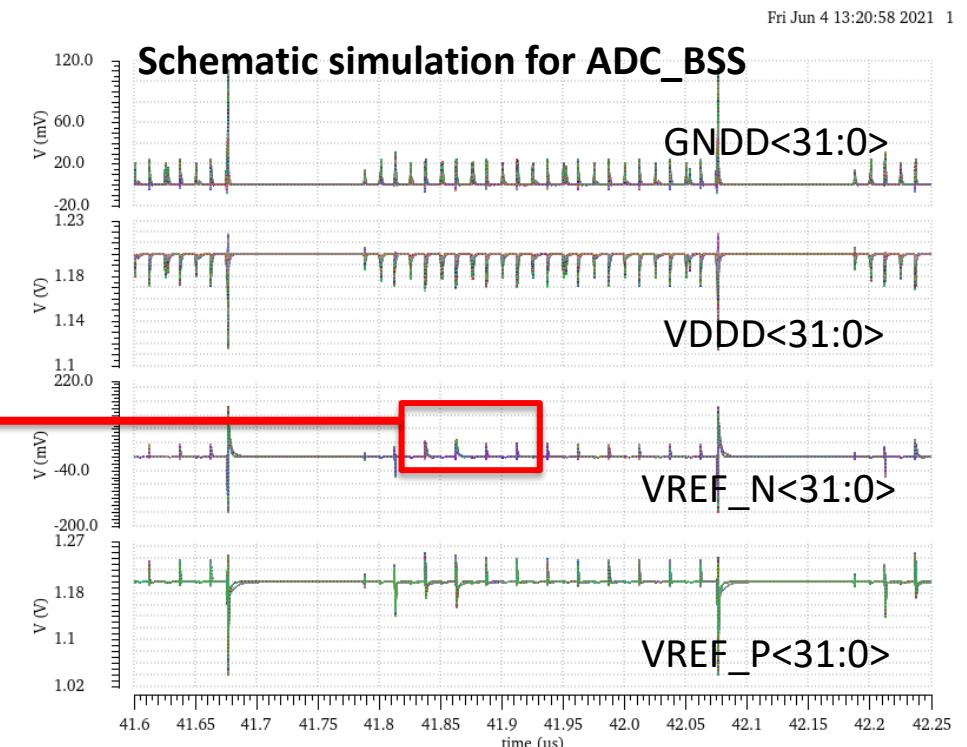
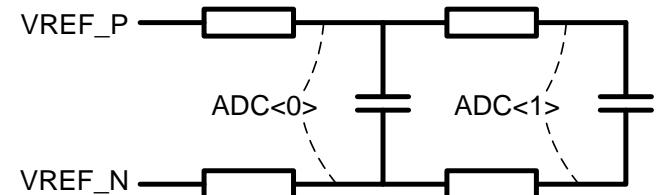


- Emulate 32 ADCs in a super column
 - M8 – M10 for VREF_P/N, width 2×12um
 - Decoupling due to parasitic
 - ~ 6pF for normal CDAC
 - ~ 1pF for AW CDAC
 - Simulated done with 1/5 pF for both CDAC



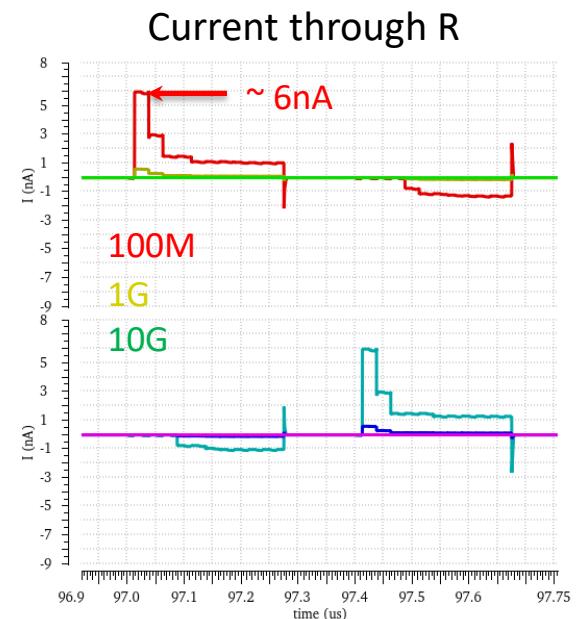
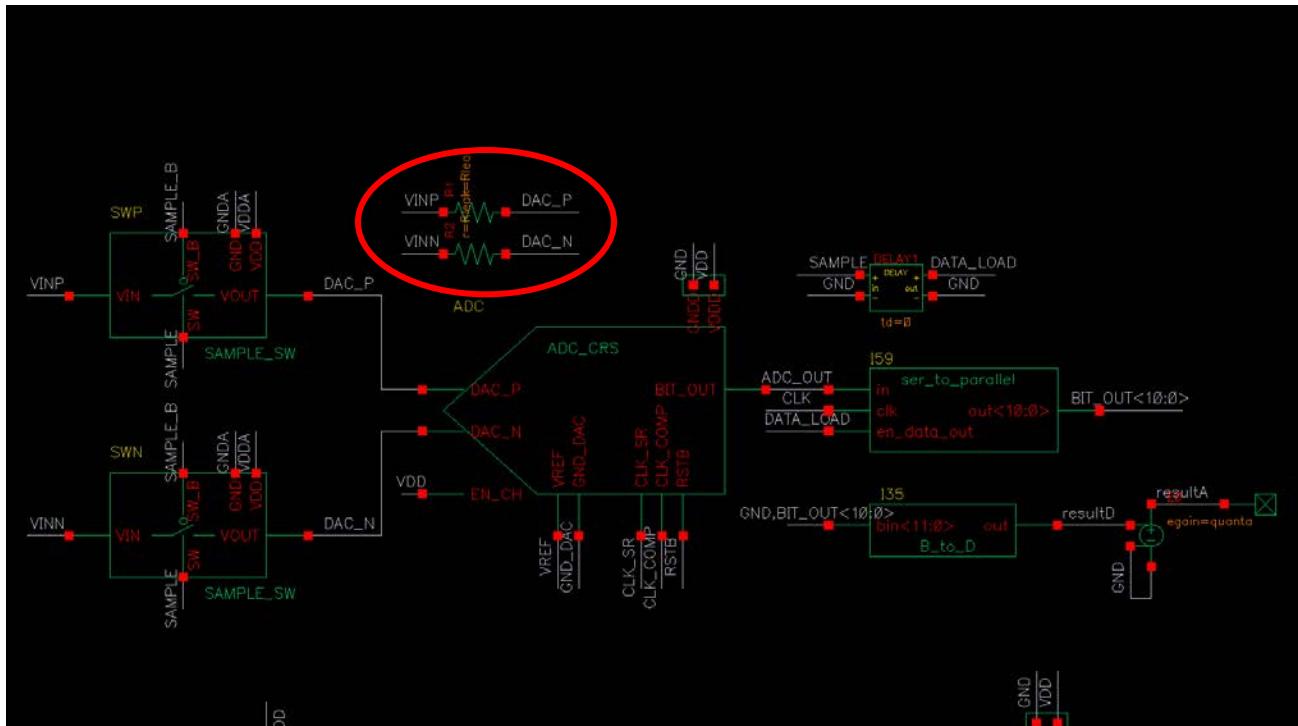
VREF network model

$$R = 0.2 \quad C = 1/5\text{pF}$$



How about leakage on sampling switch

- Emulate leakage path by a resistor in parallel with sampling switch
 - $R = 100M, 1G, 10G$

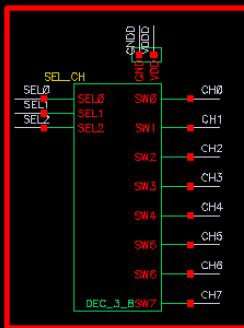


| R | 100M | 1G | 10G |
|------|-------|-------|-------|
| ENOB | 10.35 | 10.72 | 10.74 |

Core schematic

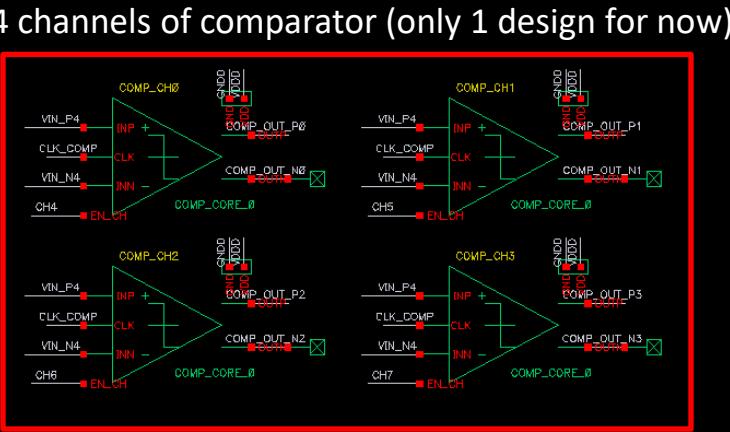
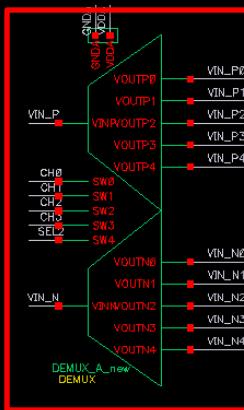
4 channels of comparator (only 1 design for now)

3-8 decoder

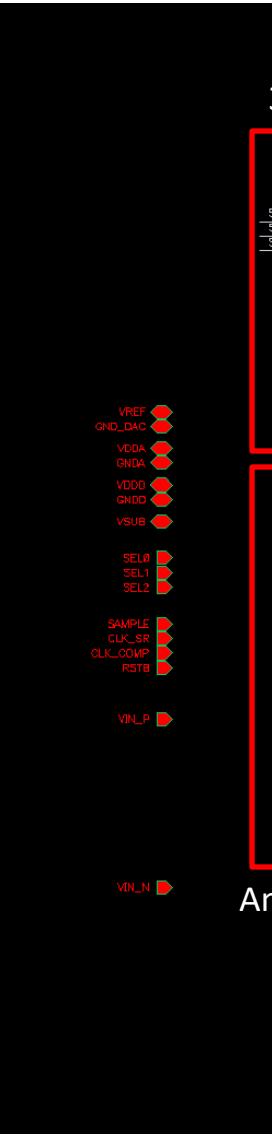
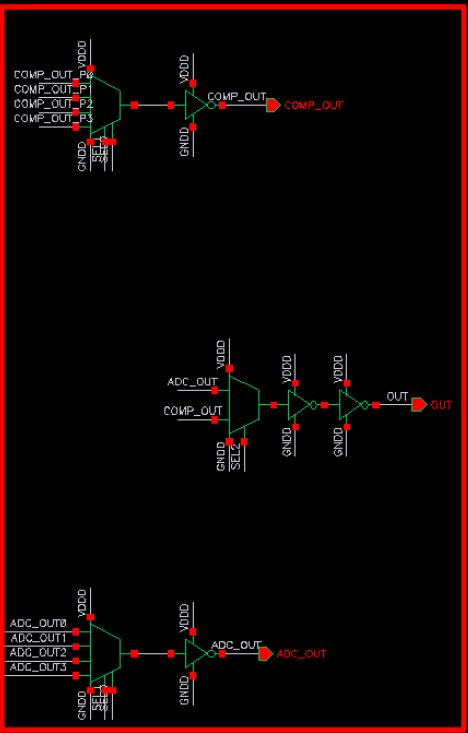


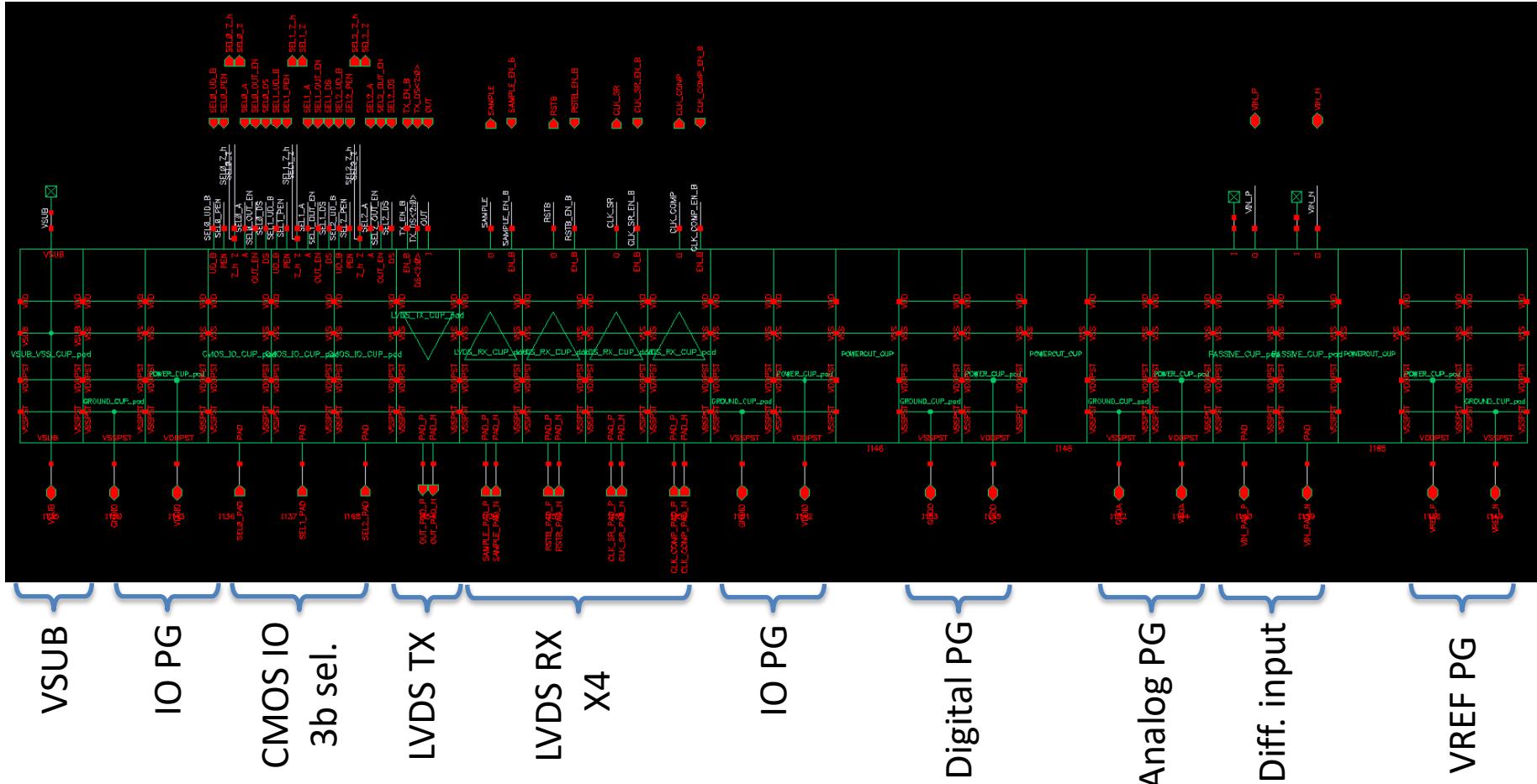
4 channels of ADC (3 designs for now)

Analog switches

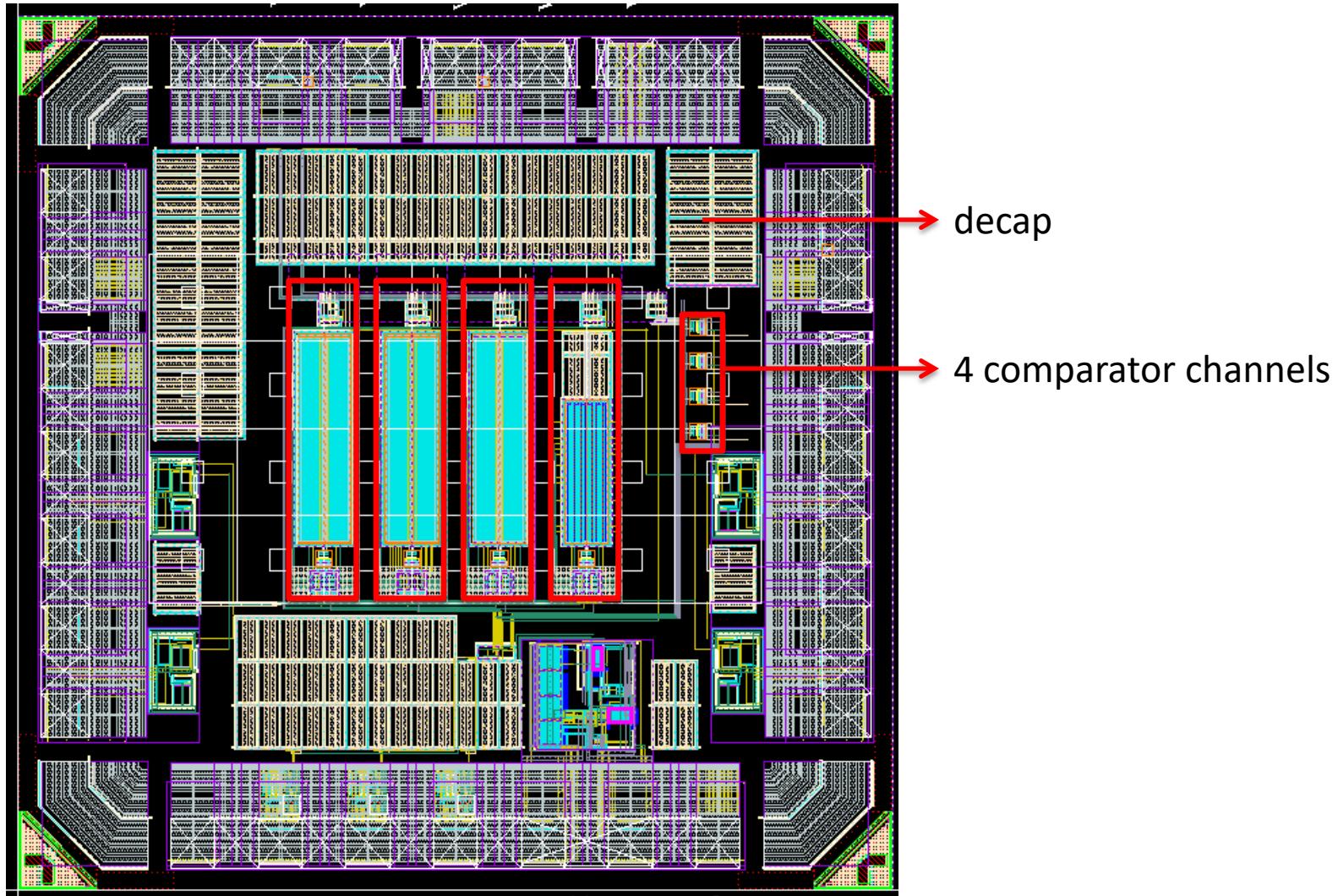


Output multiplexer

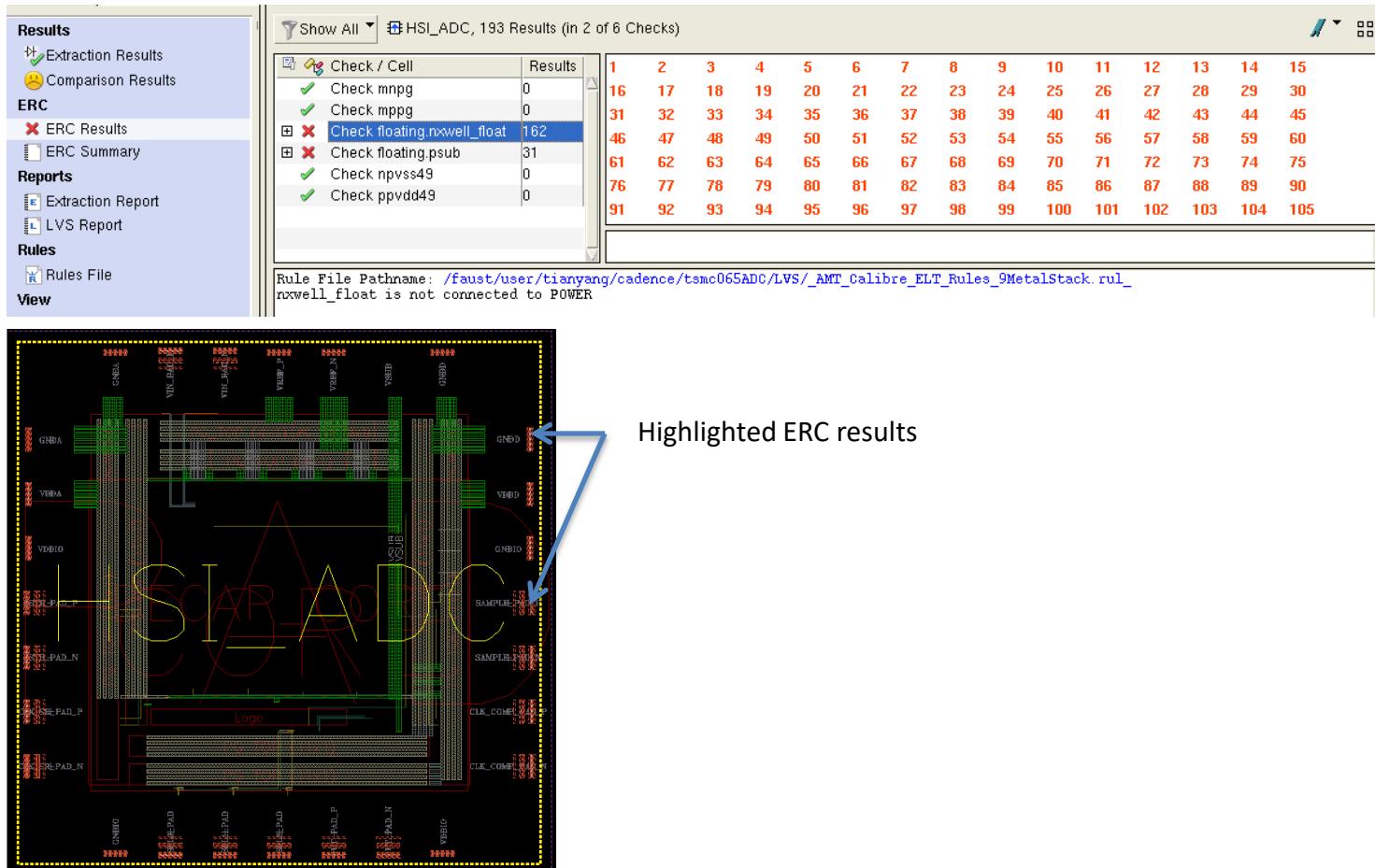




TOP layout



- LVS results
 - ERC results all due to IO cells



- LVS results
 - Property error
 - LVT enclosed transistor

| Layout Cell / Type | Source Cell | Count | Nets | Ins |
|--------------------|-------------------|---------|----------------|-----|
| C_CUSTOM_AW | C_CUSTOM_AW | LVS Box | OL, OS | OL, |
| C_CUSTOM_Sandwich | C_CUSTOM_Sandwich | LVS Box | OL, OS | OL, |
| HSI_ADC | HSI_ADC | 8 | 30375L, 30375S | 658 |
| Discrepancies | | | | |
| Property Errors | | | | |
| Discrepancy #1 | | | | |
| Discrepancy #2 | | | | |
| Discrepancy #3 | | | | |
| Discrepancy #4 | | | | |
| Discrepancy #5 | | | | |
| Discrepancy #6 | | | | |
| Discrepancy #7 | | | | |
| Discrepancy #8 | | | | |

| LAYOUT NAME | SOURCE NAME |
|--|---|
| Discrepancy #1 in HSI_ADC | |
| X18/X45/M0(347.920,651.010) MN(NCH_LVT_DNW) | XCORE/XADC_CH0/XSWN/MM0 MN(NCH_LVT_DNW) |
| l: 0.0634128 u | l: 0.06 u |
| w: 2.725 u | w: 2.5 u |
| 5.69% 9% | |
| Discrepancy #2 in HSI_ADC | |
| X18/X46/M0(352.080,651.010) MN(NCH_LVT_DNW) | XCORE/XADC_CH0/XSWP/MM0 MN(NCH_LVT_DNW) |
| l: 0.0634128 u | l: 0.06 u |
| w: 2.725 u | w: 2.5 u |
| 5.69% 9% | |
| Discrepancy #3 in HSI_ADC | |
| X18/X47/M0(447.920,651.010) MN(NCH_LVT_DNW) | XCORE/XADC_CH1/XSWN/MM0 MN(NCH_LVT_DNW) |
| l: 0.0634128 u | l: 0.06 u |
| w: 2.725 u | w: 2.5 u |
| 5.69% 9% | |
| Discrepancy #4 in HSI_ADC | |
| X18/X48/M0(452.080,651.010) MN(NCH_LVT_DNW) | XCORE/XADC_CH1/XSWP/MM0 MN(NCH_LVT_DNW) |
| l: 0.0634128 u | l: 0.06 u |
| w: 2.725 u | w: 2.5 u |
| 5.69% 9% | |
| Discrepancy #5 in HSI_ADC | |
| X18/X49/M0(547.920,651.010) MN(NCH_LVT_DNW) | XCORE/XADC_CH2/XSWN/MM0 MN(NCH_LVT_DNW) |
| l: 0.0634128 u | l: 0.06 u |
| w: 2.725 u | w: 2.5 u |
| 5.69% 9% | |
| Discrepancy #6 in HSI_ADC | |
| X18/X50/M0(552.080,651.010) MN(NCH_LVT_DNW) | XCORE/XADC_CH2/XSWP/MM0 MN(NCH_LVT_DNW) |
| l: 0.0634128 u | l: 0.06 u |
| w: 2.725 u | w: 2.5 u |
| 5.69% 9% | |
| Discrepancy #7 in HSI_ADC | |
| X18/X69/X7/M0(647.920,651.010) MN(NCH_LVT_DNW) | XCORE/XADC_CH3/XSWN/MM0 MN(NCH_LVT_DNW) |
| l: 0.0634128 u | l: 0.06 u |
| w: 2.725 u | w: 2.5 u |
| 5.69% 9% | |
| Discrepancy #8 in HSI_ADC | |
| X18/X69/X8/M0(652.080,651.010) MN(NCH_LVT_DNW) | XCORE/XADC_CH3/XSWP/MM0 MN(NCH_LVT_DNW) |

- DRC results
 - rule file from RD53 signoff folder: “cern.chip.calibre.drc”
 - Additionally, antenna has been checked => OK

Show All ▾ HSI_ADC, 848 Results (in 7 of 11 Checks)

| Check / Cell | Result |
|---------------------------|--------|
| Check DRM.R.1 | 1 |
| Check POR.1 | 2 |
| Check POR.4 | 2 |
| Check RM.WARN.2 | 660 |
| Check RM.WARN.4:M2 | 180 |
| Check LUP.1g | 2 |
| Check ESD_WARN_1 | 1 |
| Check DENSITY_PRINT_FILES | 0 |

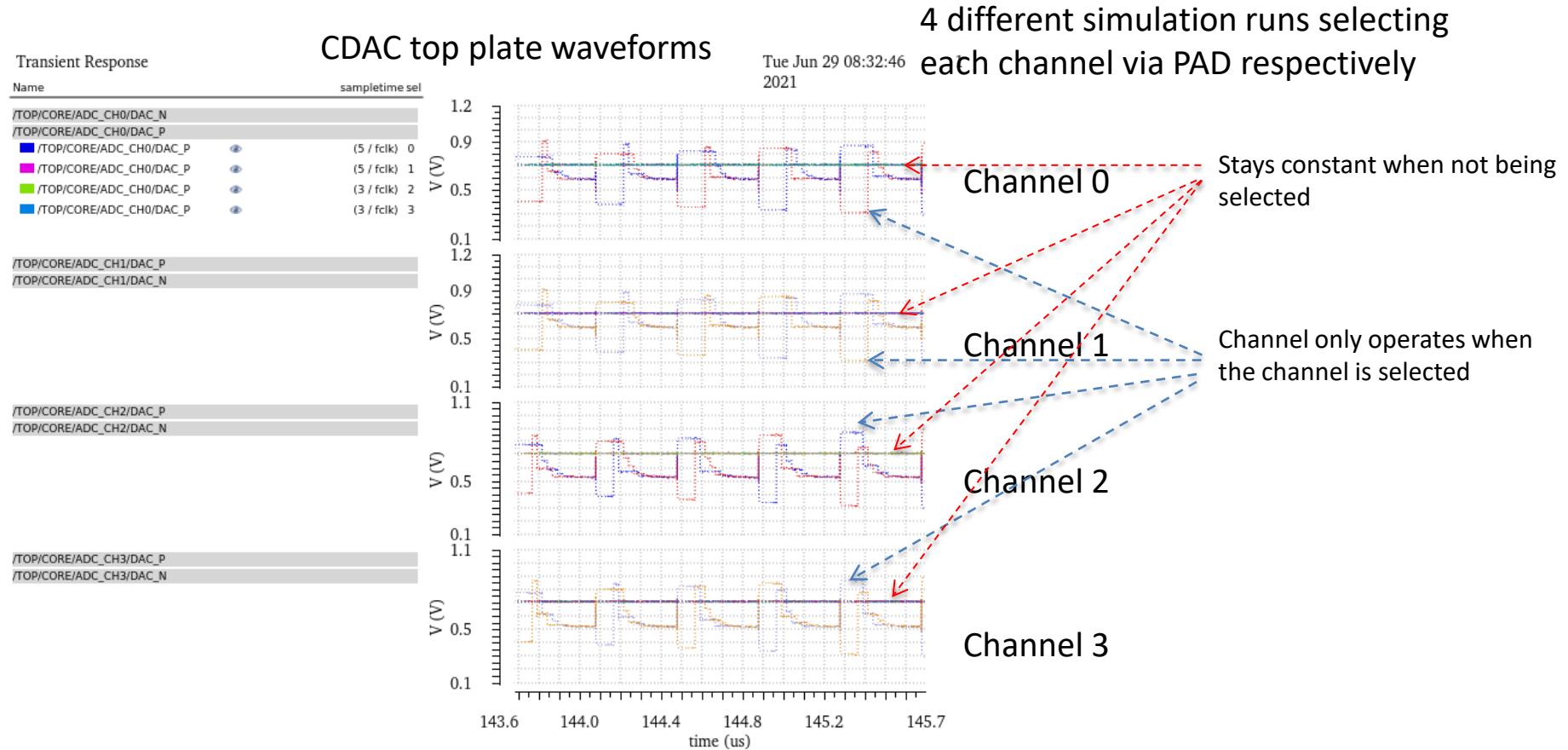
846 847

Due to enclosed transistor

Known error/warning due to IO cells

```
LUP.1g { @ Any N+ OD injector or an N+ OD injector cluster connected to an I/O pad must be surrounded by a P+ guard-ring.  
        @ Any P+ OD injector or a P+ OD injector cluster connected to an I/O pad must be surrounded by a N+ guard-ring.  
        POST_DRIVER_NACT NOT INSIDE PTAP_guard_ring_hole  
        POST_DRIVER_PACT NOT INSIDE NTAP_guard_ring_hole  
}
```

- All power/reference connected to **1 Ohm** and **5 nH** in series to emulate the bonding wire



- All power/reference connected to **1 Ohm** and **5 nH** in series to emulate the bonding wire

Schematic

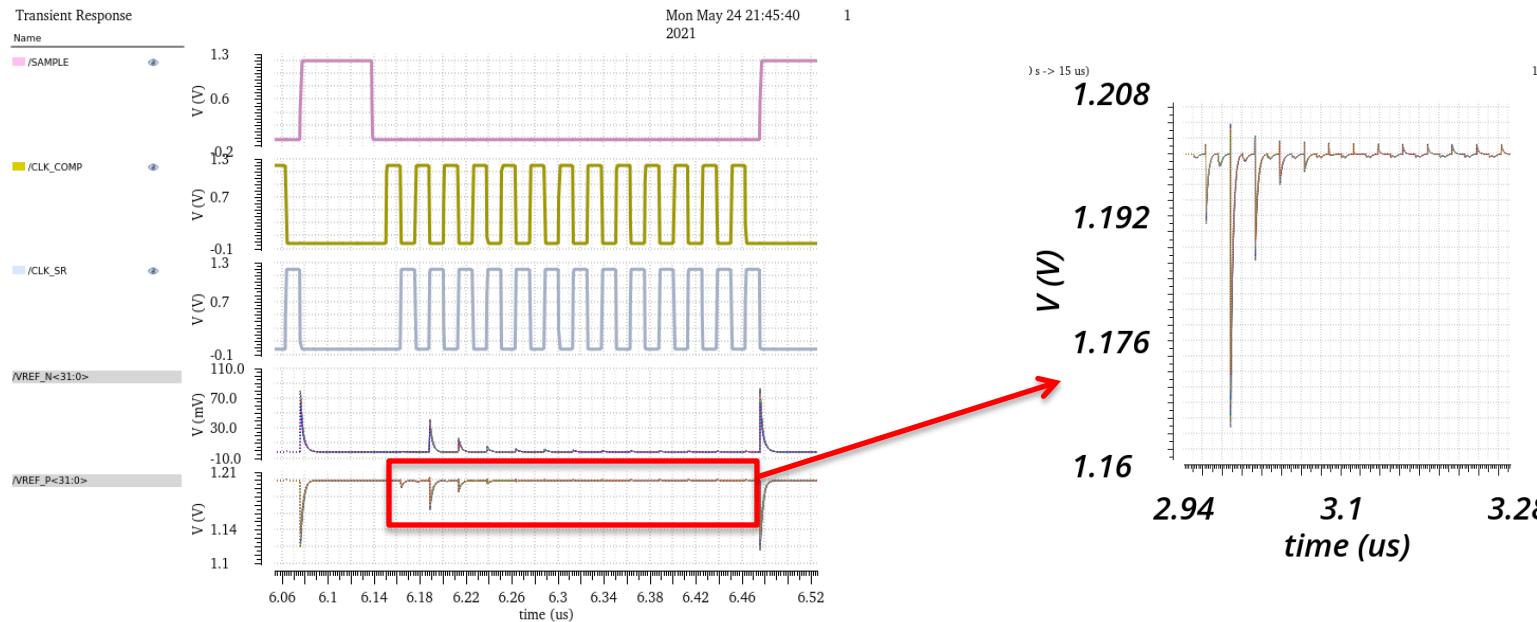
| Cell | BSS | BSS RE | CRS | BSS AW RE |
|------|-------|--------|-------|-----------|
| ENOB | 10.64 | 10.64 | 10.64 | 10.73 |

C only (with DECAP using ideal view)

| Cell | BSS | BSS RE | CRS | BSS AW RE |
|------|-------|--------|-------|-----------|
| ENOB | 10.94 | 10.94 | 10.92 | 10.85 |

Effects of VREF settling

- Decoupling between VREF_P & VREF_N
 - ~ 5pF for normal CDAC
 - ~ 1pF for attenuated CDAC
- Use a distributed RC network to emulate the power parasitic
 - $R = 0.2 \text{ Ohm} \Rightarrow \text{M8-M10}$ in parallel
 - $C = 5\text{pF}$ or 1pF



- CoRDIA is a readout chip for pixel detector meeting the challenge of future high brilliance light sources
 - The key is to make A-D conversion within the matrix
- A first prototype to study the ADC circuit has been designed
 - A conventional channel with BSS switching (ADC_BSS)
 - what is the intrinsic linearity?
 - CRS switching (ADC_CRS)
 - Can it have higher intrinsic linearity?
 - BSS switching with redundancy (ADC_BSS_RE)
 - what if intrinsic linearity is not good enough or reference is rippling?
 - BSS switching with attenuated CDAC array with redundancy (ADC_BSS_AW_RE)
 - Can it be beneficial for less area?

-
- Backup slides

ENOB simulation

Schematic simulation

| Cell | BSS | BSS RE | CRS | BSS AW RE |
|------|-------|--------|-------|-----------|
| ENOB | 10.67 | 10.67 | 10.67 | 10.68 |

Schematic with transient noise (noisefmax = 10G)

| Cell | BSS | BSS RE | CRS | BSS AW RE |
|------|-------|--------|-------|-----------|
| ENOB | 10.45 | 10.47 | 10.49 | 10.5 |

C QRC

| Cell | BSS | BSS RE | CRS | BSS AW RE |
|------|-------|--------|-------|-----------|
| ENOB | 10.08 | 10.2 | 10.72 | 10.58 |

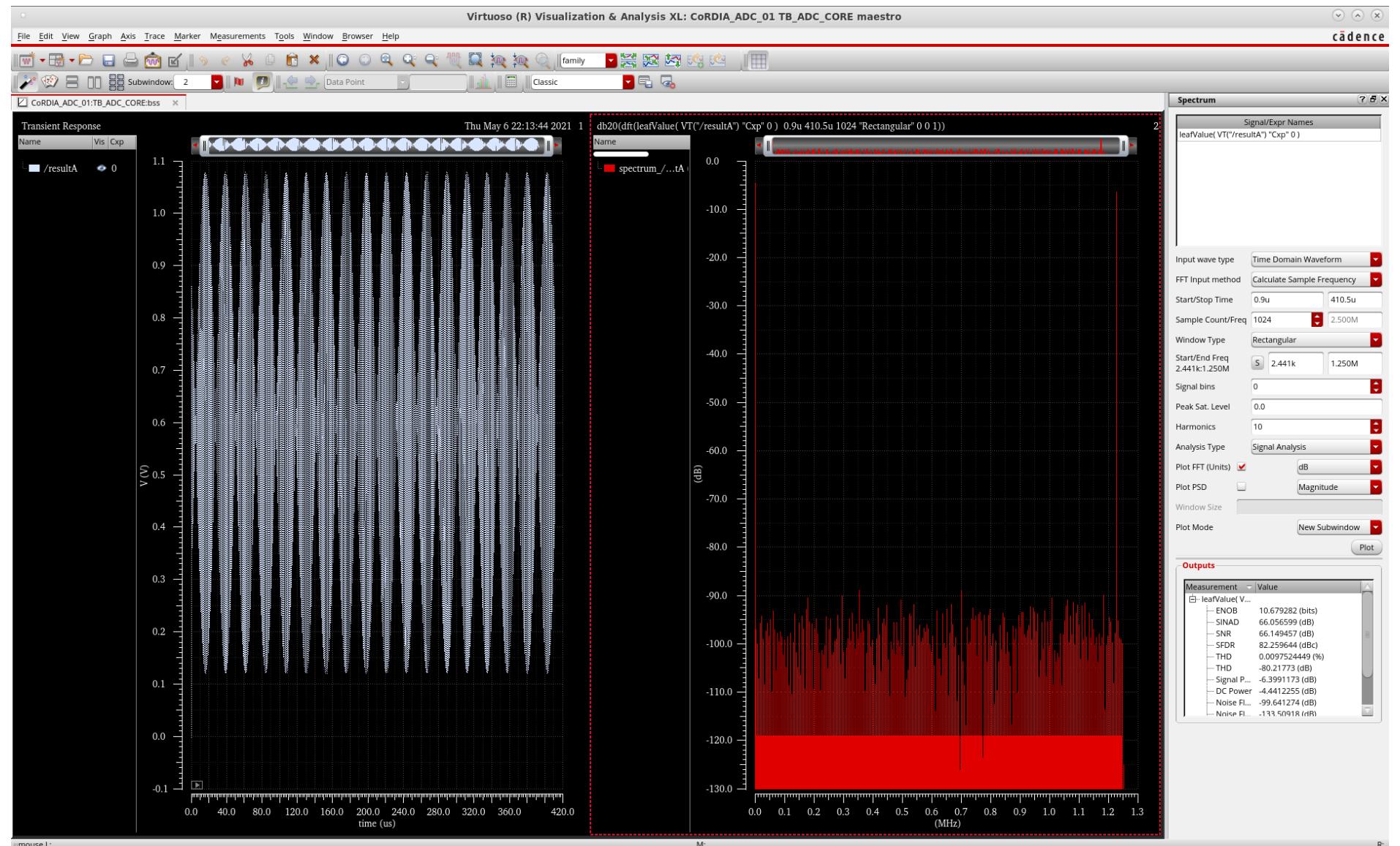
| Cell | BSS |
|------|-----|
| ENOB | |

C blackbox CDAC C_QRC (no parasitic between bb cell and top cell?)

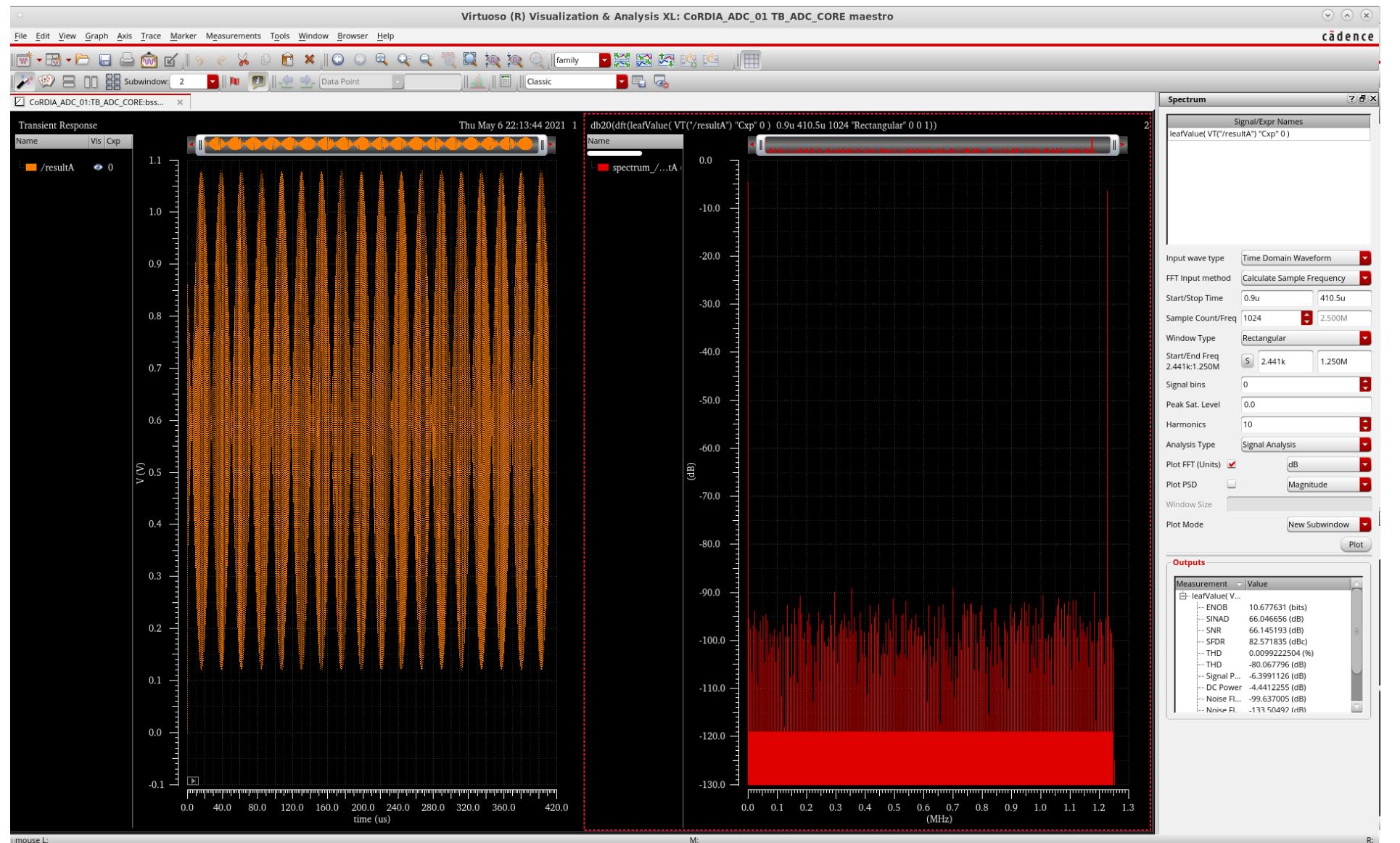
| Cell | BSS | BSS RE | CRS | BSS AW RE |
|------|-------|--------|-------|-----------|
| ENOB | 10.29 | 10.37 | 10.59 | 10.43 |

| Cell | BSS |
|------|-----|
| ENOB | |

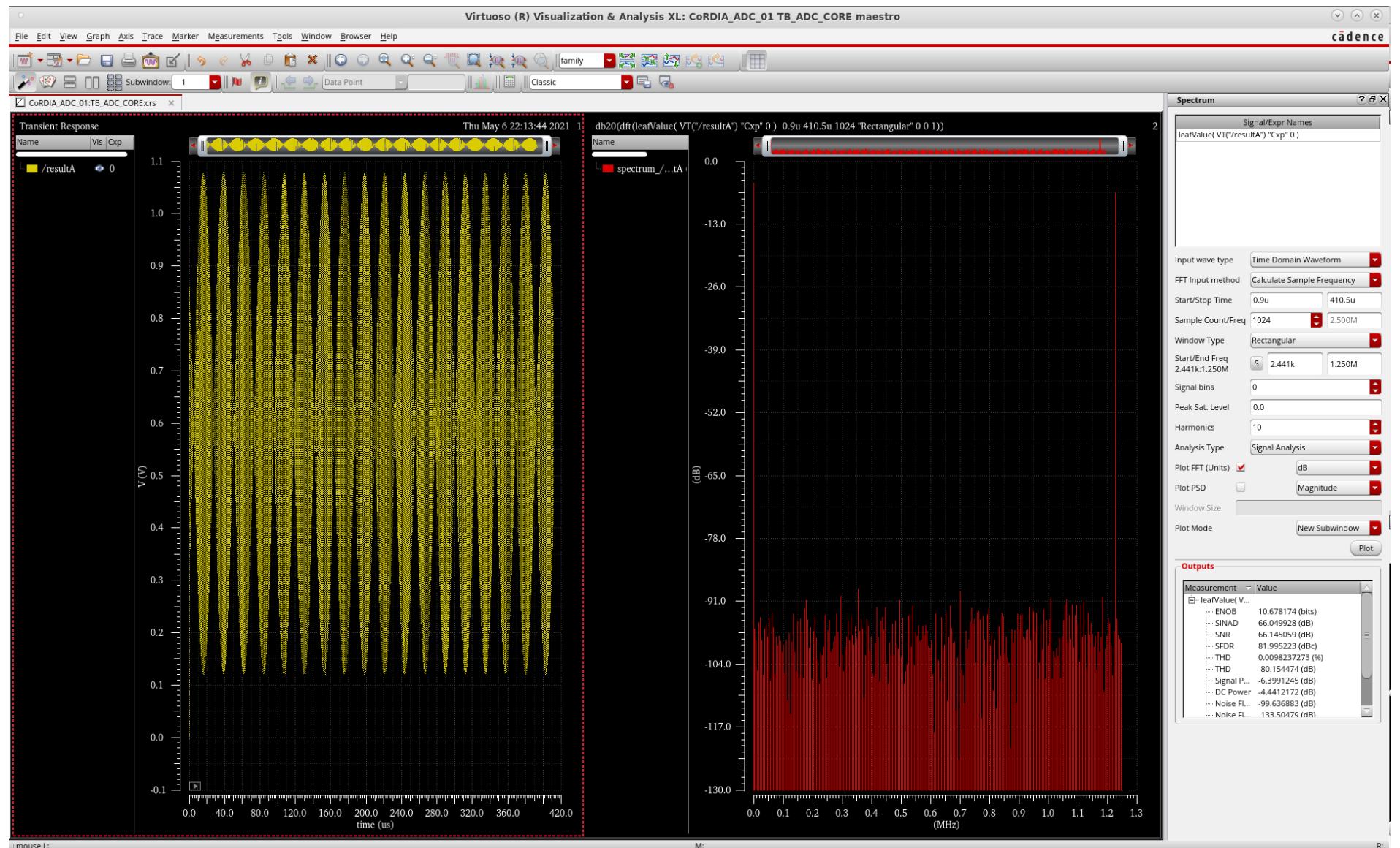
Bidirectional single-sided switching (BSS)



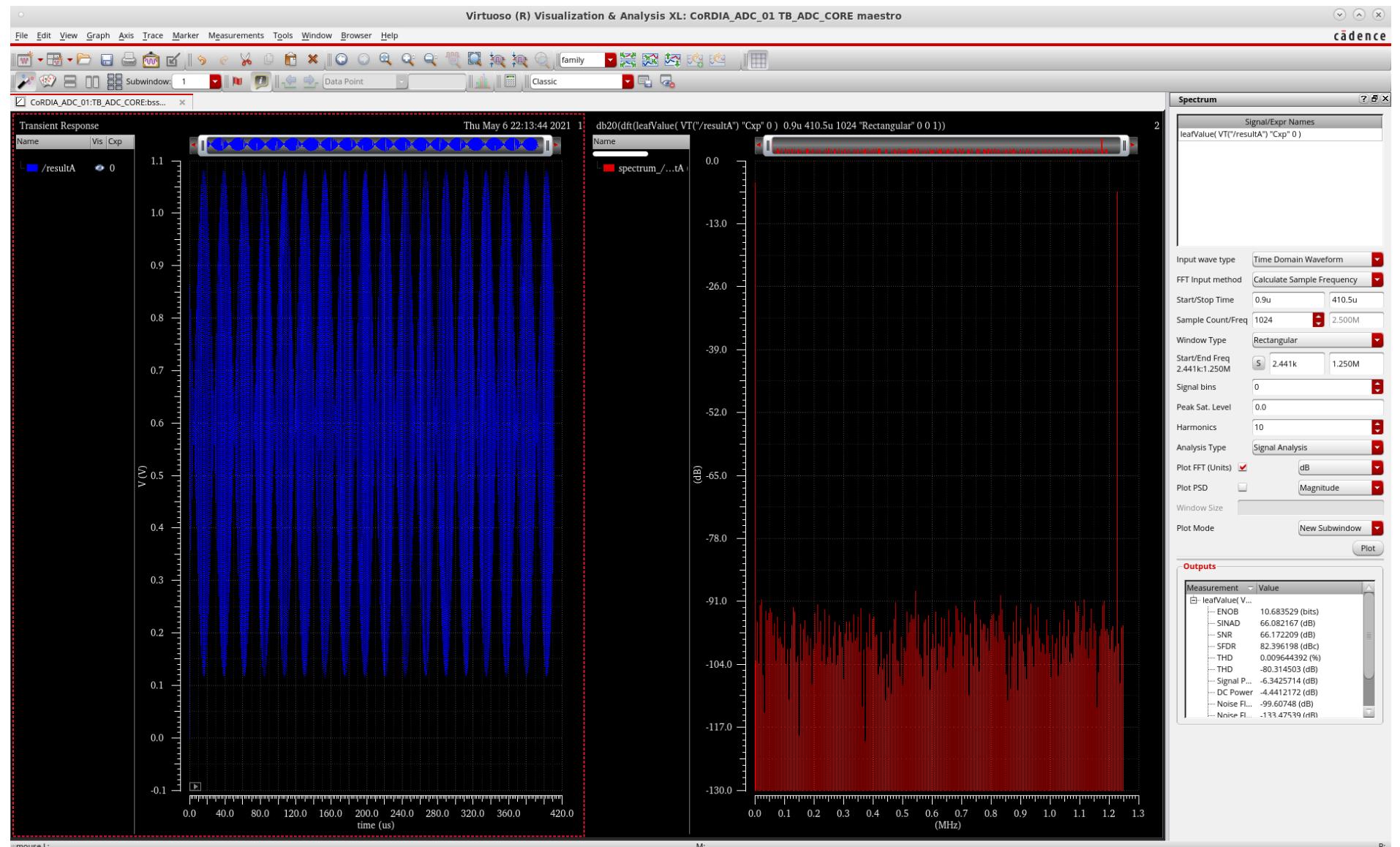
BSS with redundancy



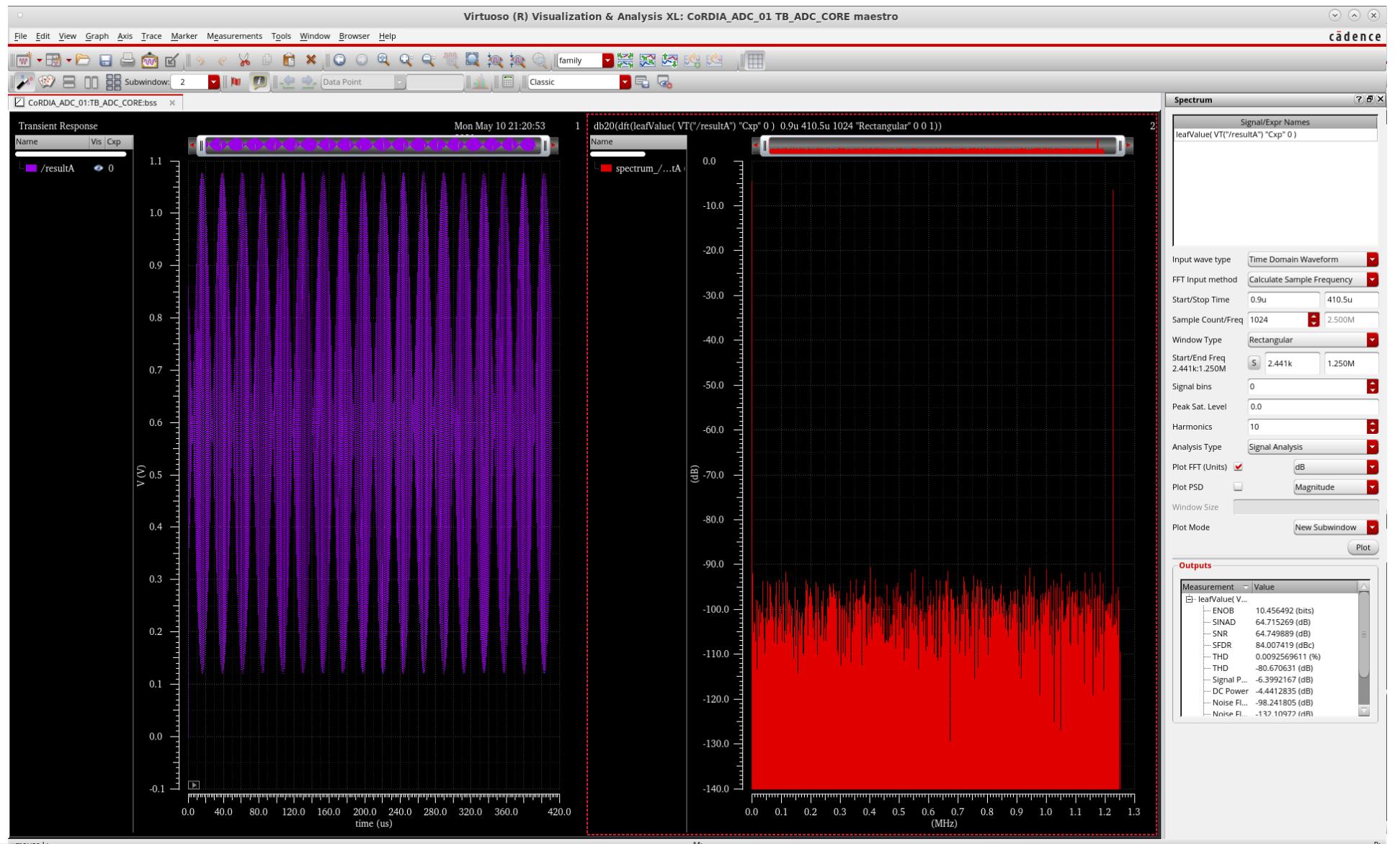
Correlated reverse switching (CRS)



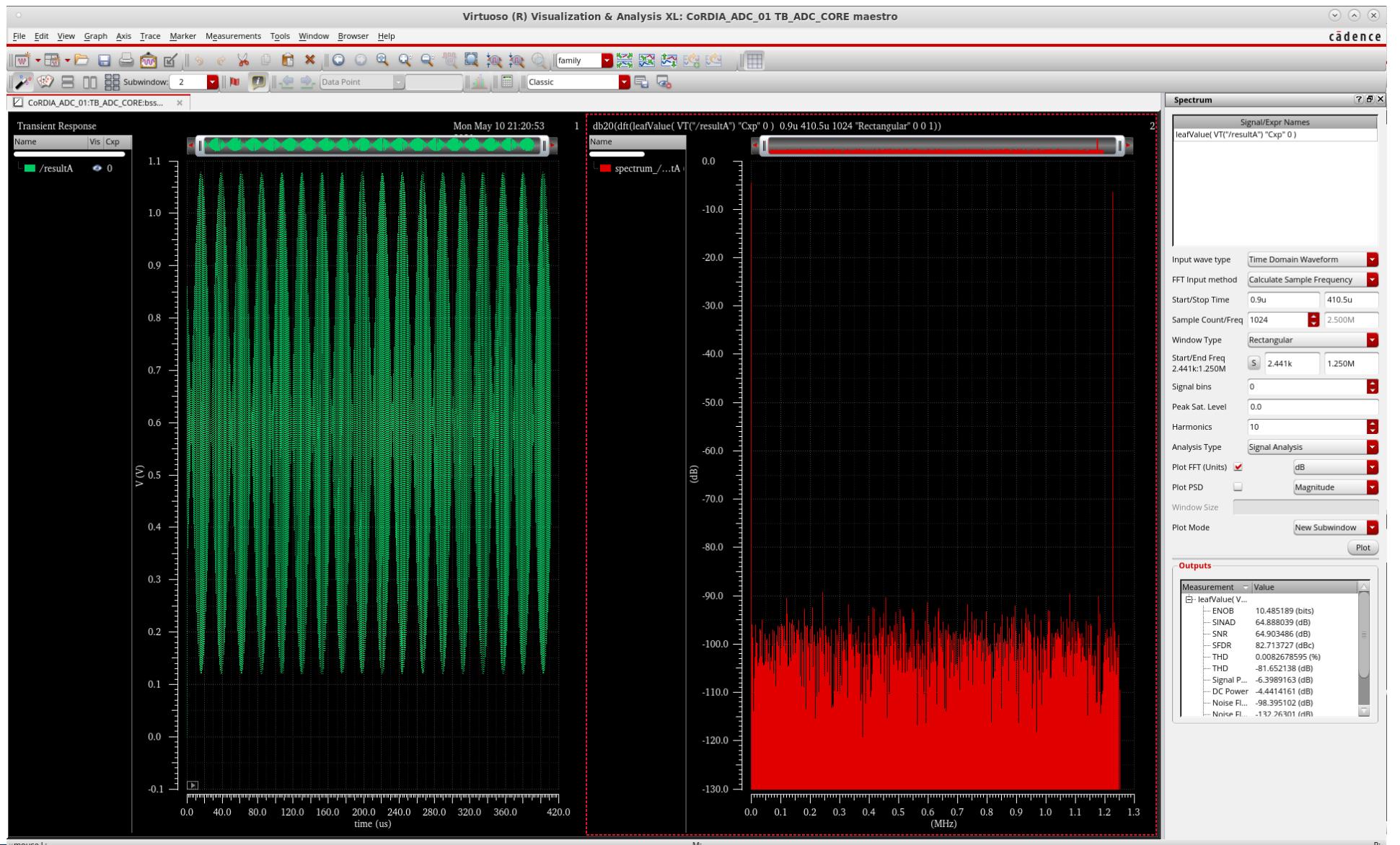
BSS attenuated array with redundancy



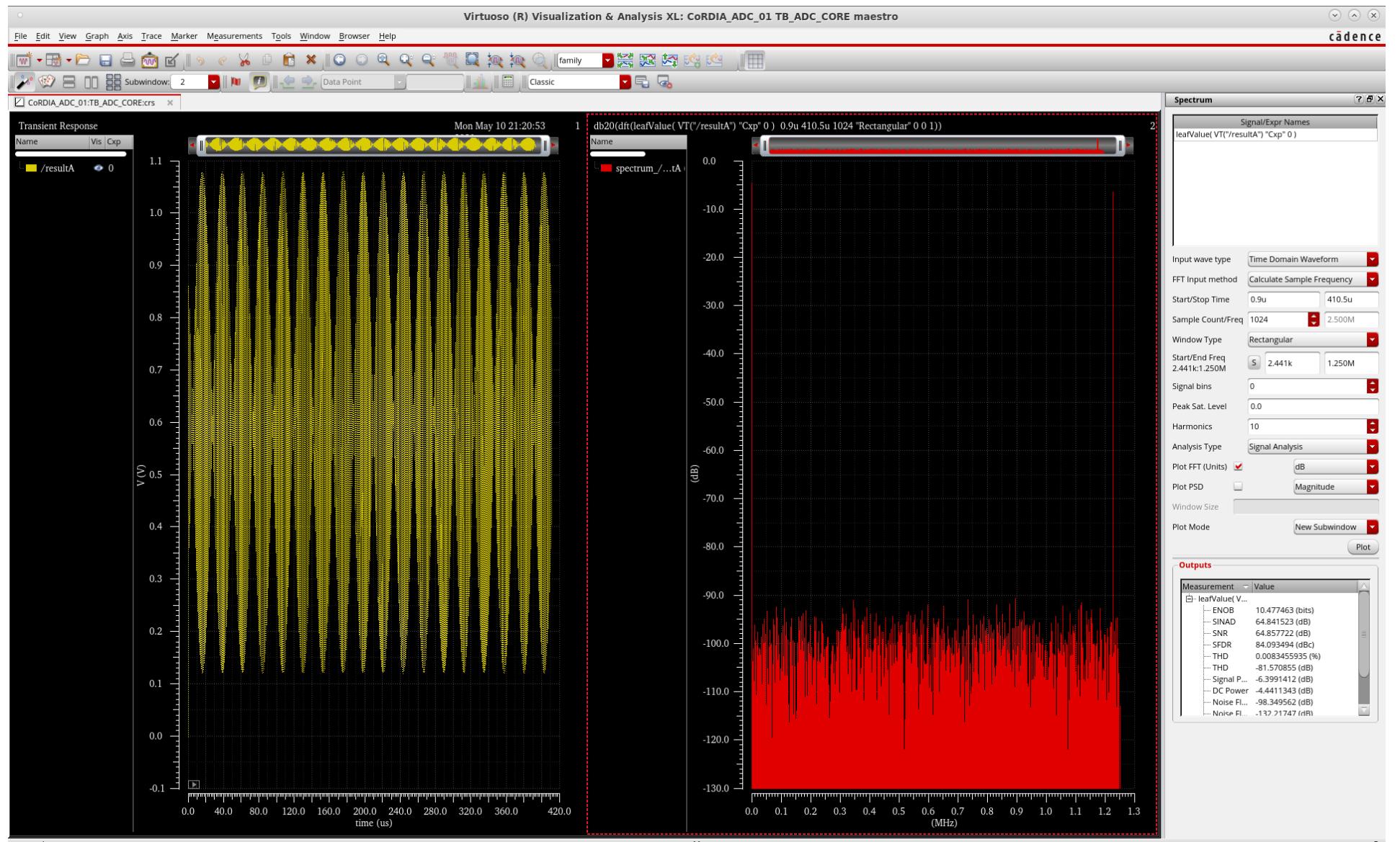
Bidirectional single-sided switching (BSS) – with noise



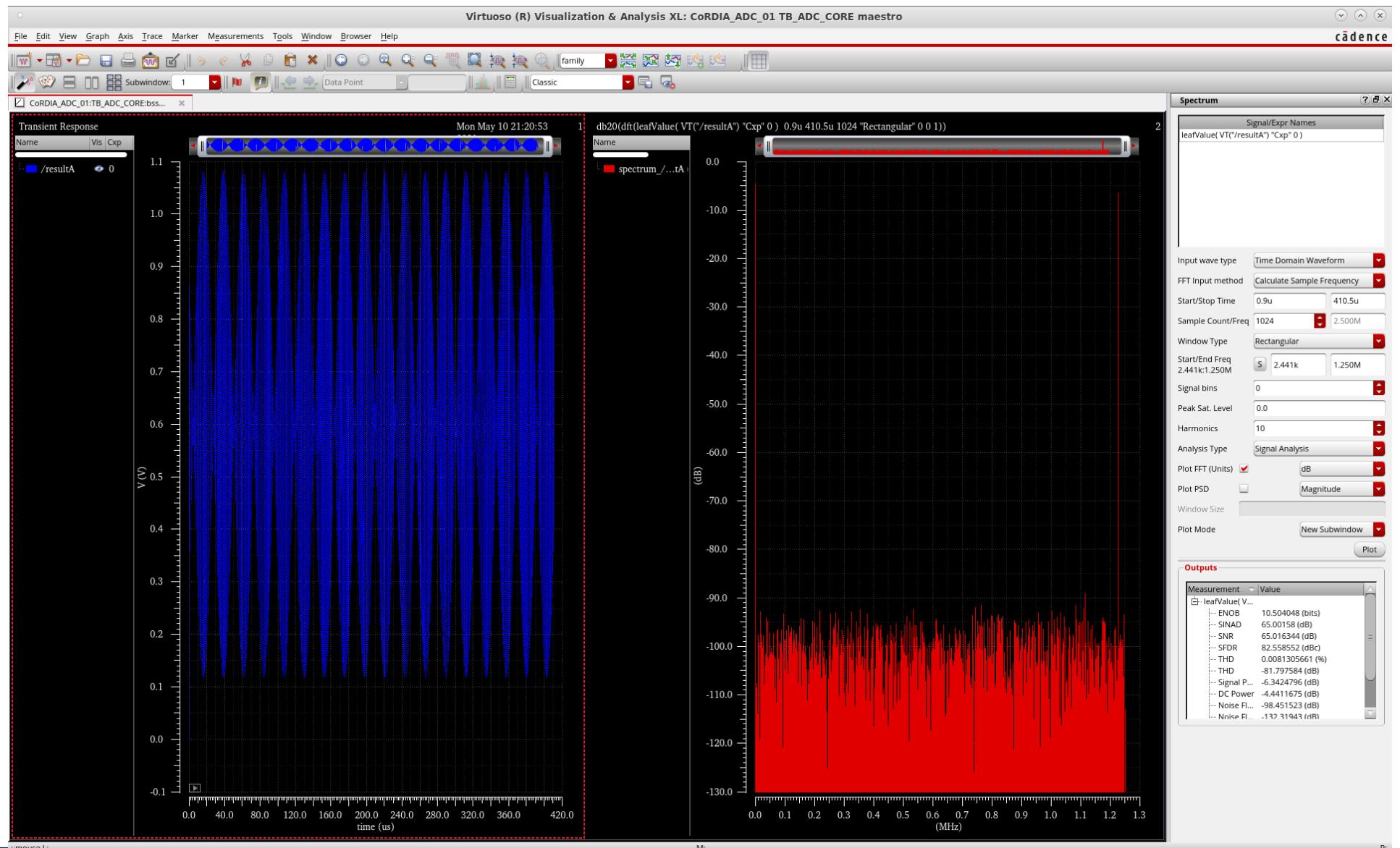
BSS with redundancy – with noise



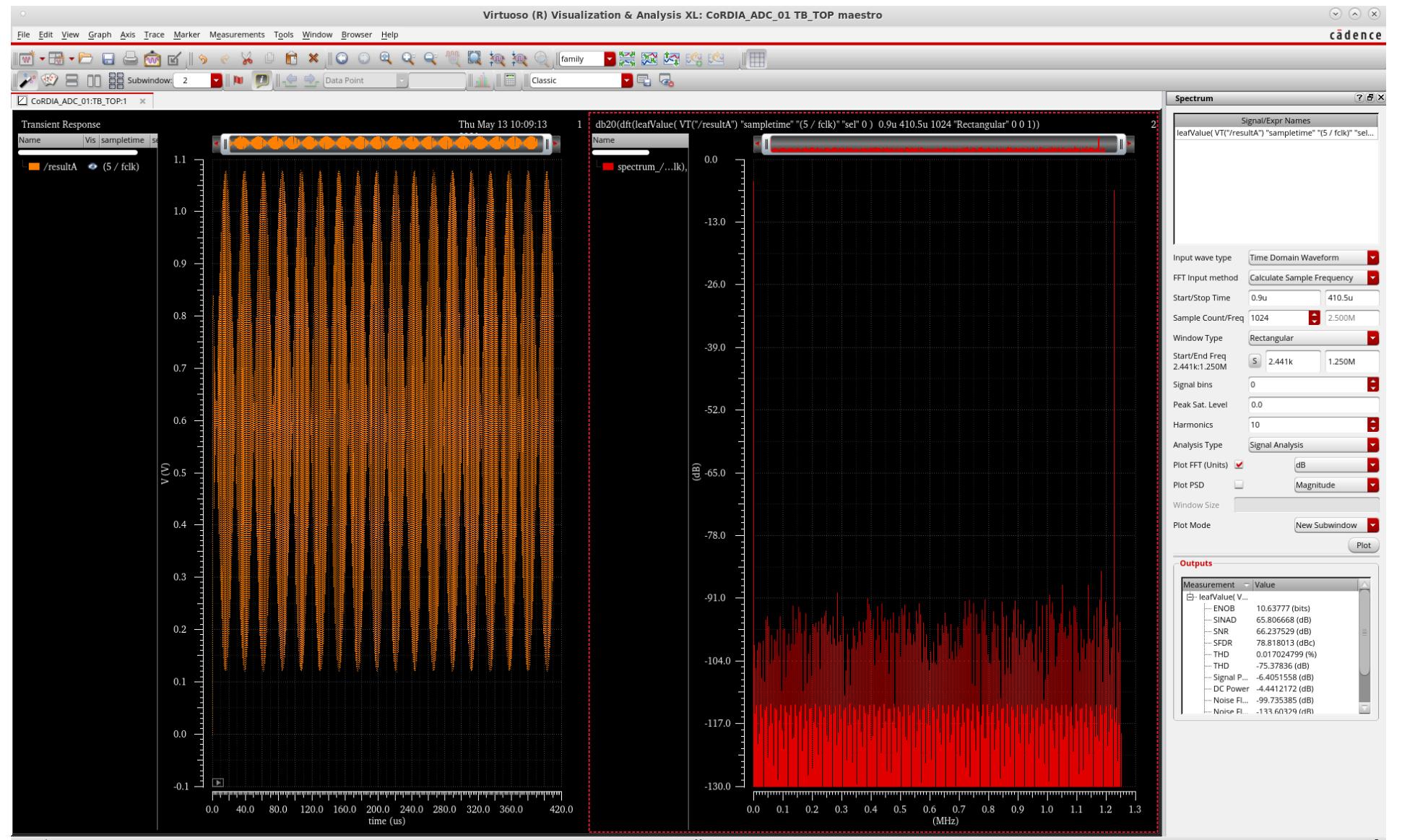
Correlated reverse switching (CRS) – with noise



BSS attenuated array with redundancy – with noise



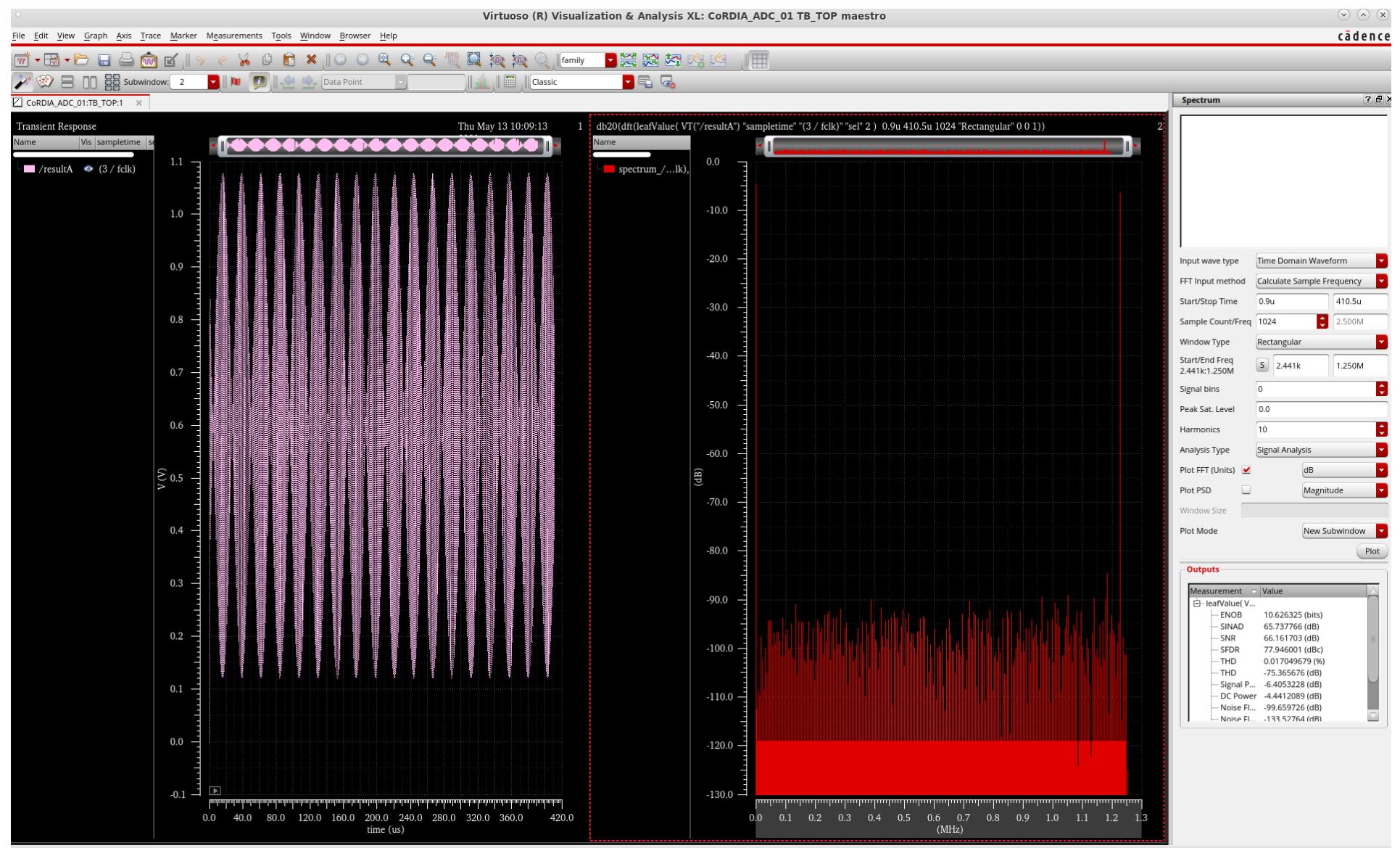
Bidirectional single-sided switching (BSS) – TOP



BSS with redundancy – TOP

Correlated reverse switching (CRS) – TOP

BSS attenuated array with redundancy – TOP



- Consider only capacitor variation on bit 4

- Weight error of binary array: $\frac{\sigma(16*C_{unit})}{16*C_{unit}} * LSB = 4 * \frac{\sigma(C_{unit})}{C_{unit}} * LSB$
- Weight error of attenuated array: $16 * \frac{\sigma(C_{unit})}{C_{unit}} * LSB$
=> One Cunit in MSB array is 16 LSBs

