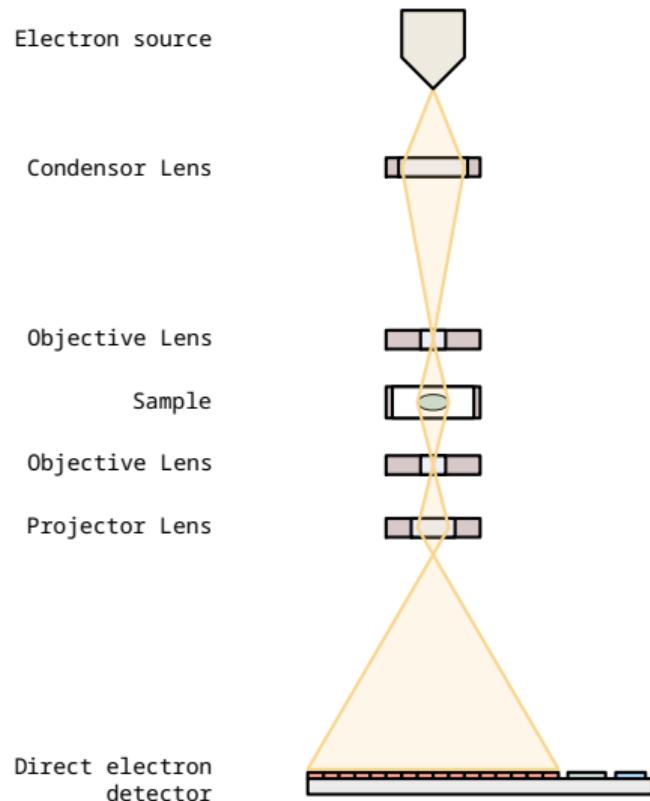
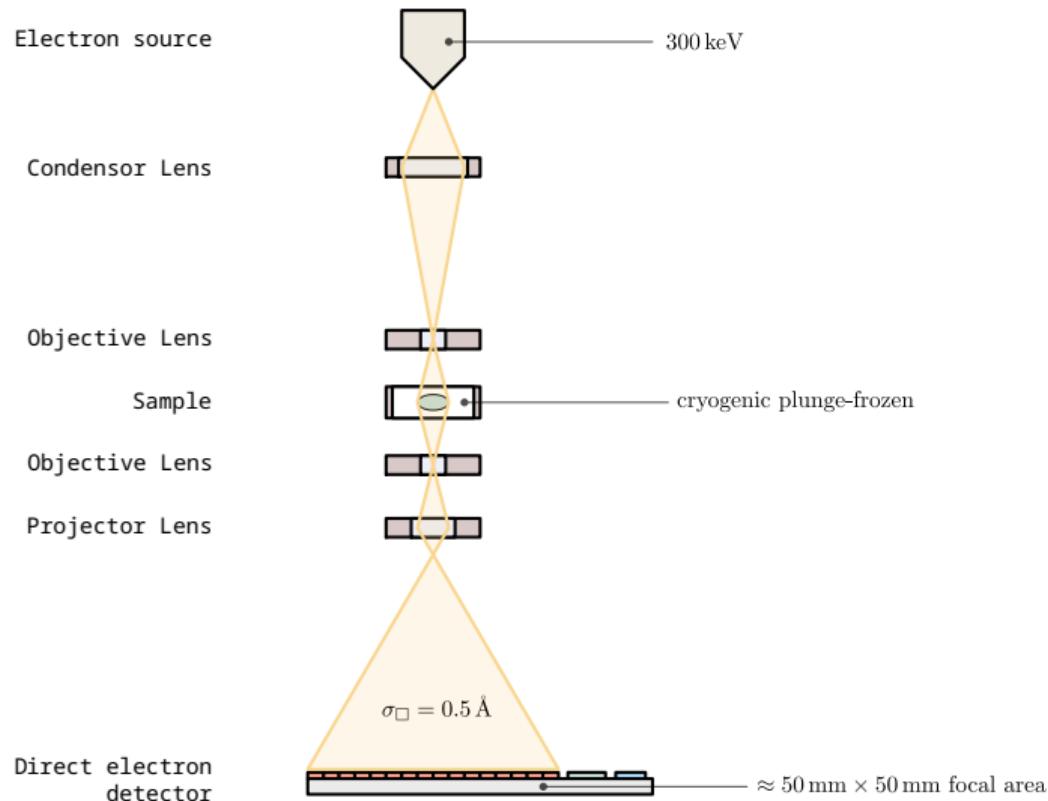
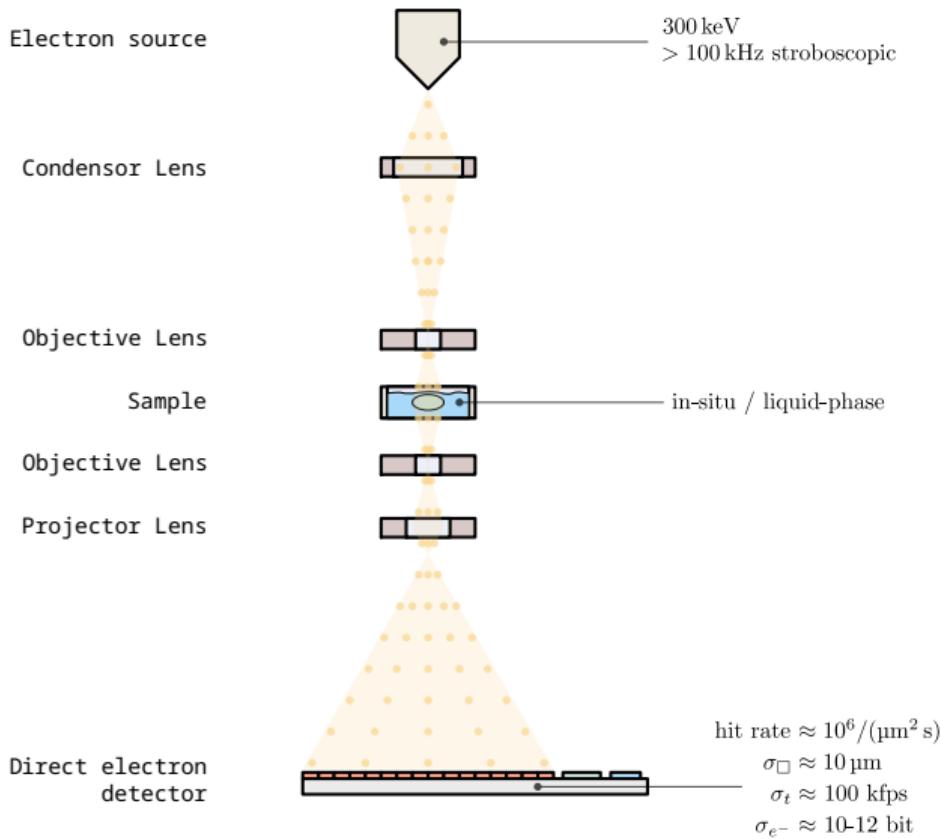


# **Modeling data converters for high frame rate imaging detectors**

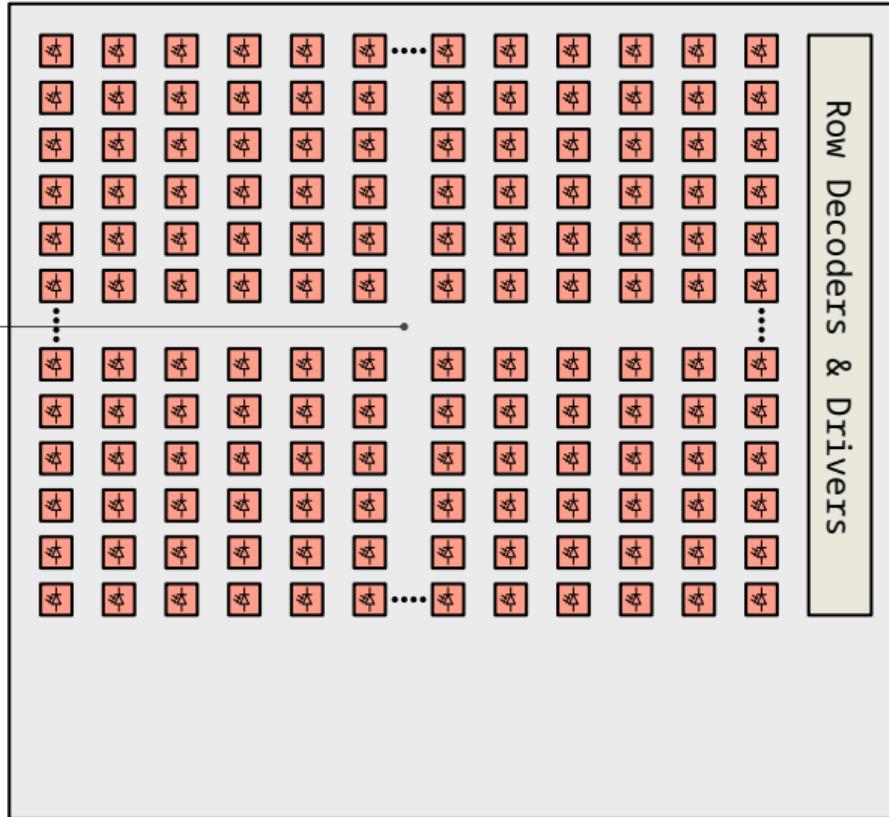


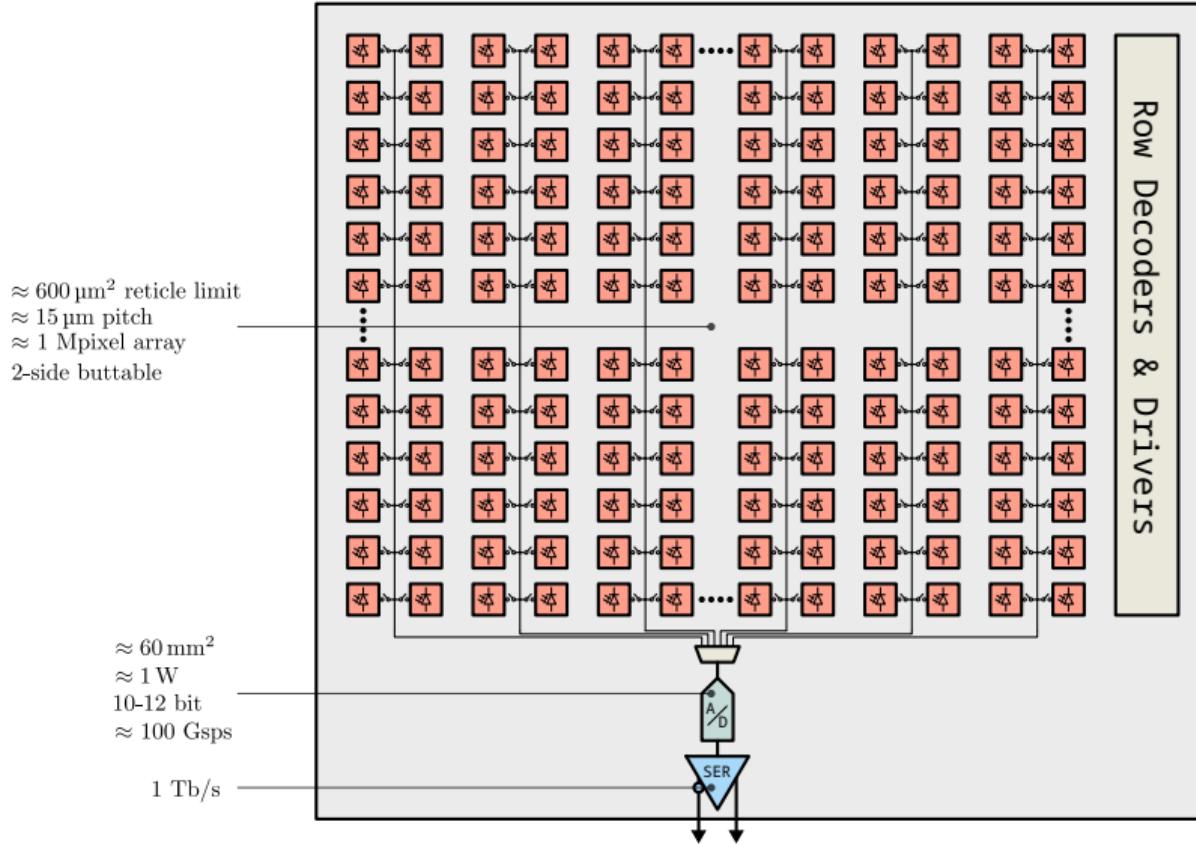






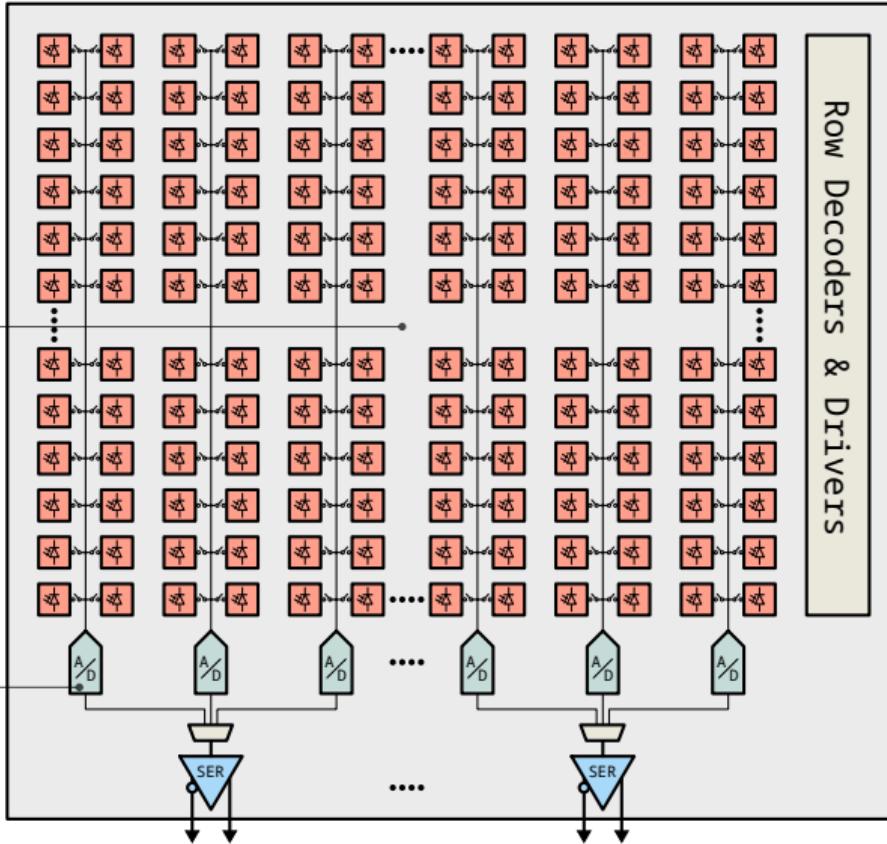
$\approx 600 \mu\text{m}^2$  reticle limit  
 $\approx 15 \mu\text{m}$  pitch  
 $\approx 1 \text{ Mpixel array}$   
2-side buttable

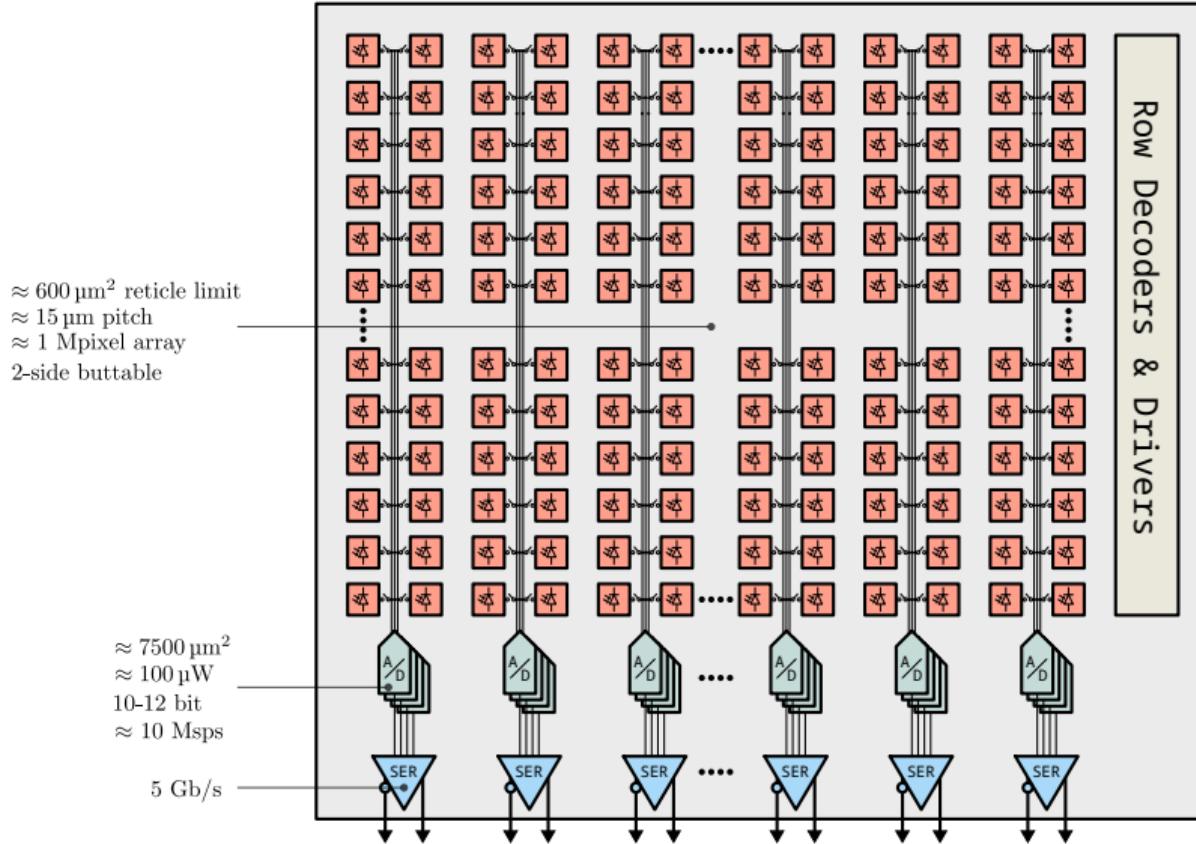


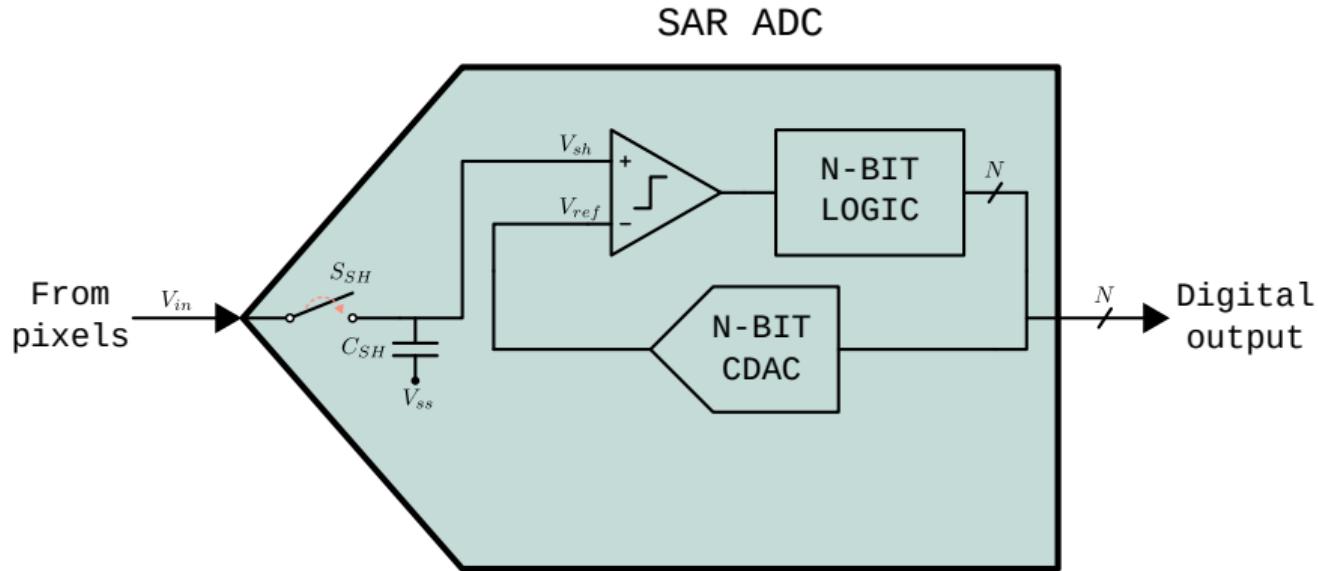


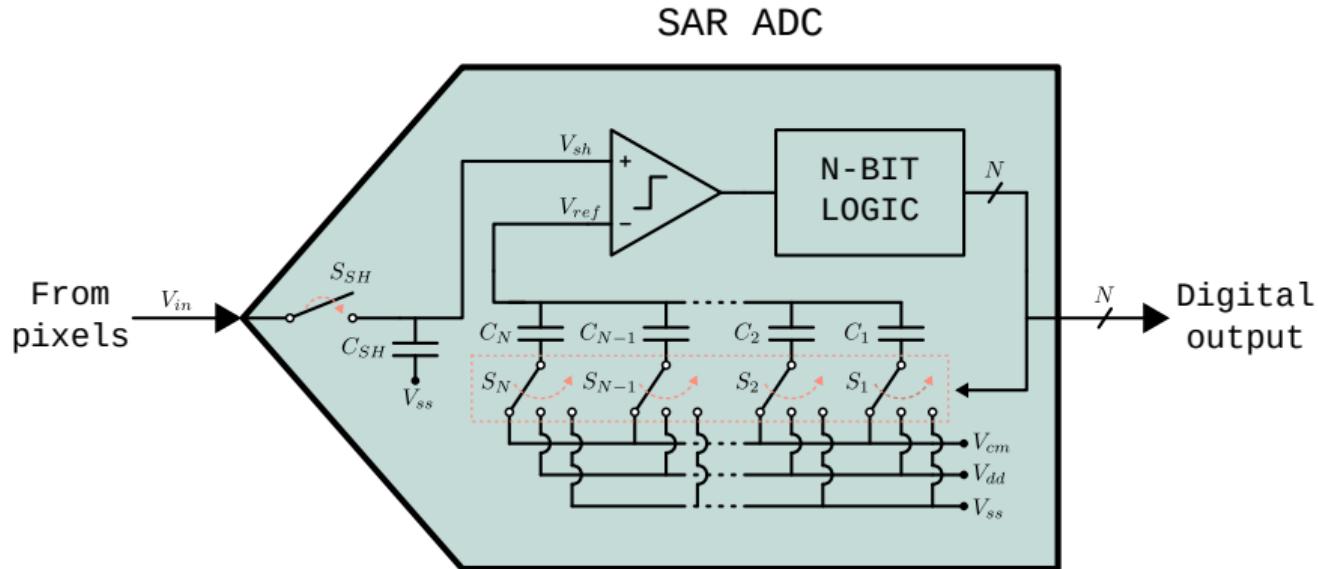
$\approx 600 \mu\text{m}^2$  reticle limit  
 $\approx 15 \mu\text{m}$  pitch  
 $\approx 1 \text{ Mpixel array}$   
2-side buttable

$\approx 120\,000 \mu\text{m}^2$   
 $\approx 1 \text{ mW}$   
10-12 bit  
 $\approx 200 \text{ Msps}$

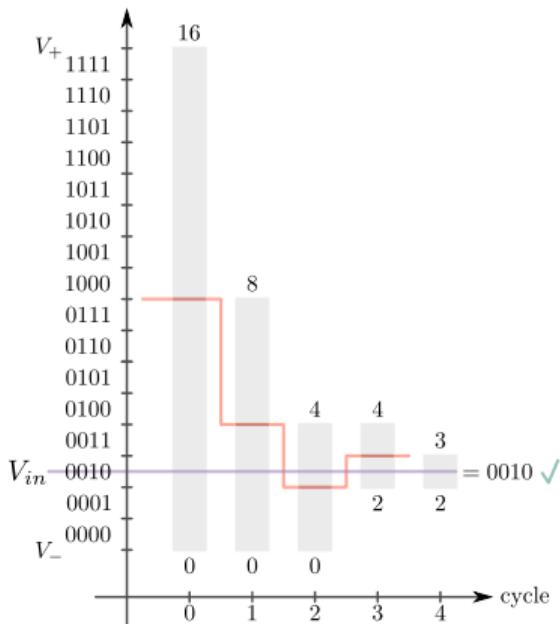
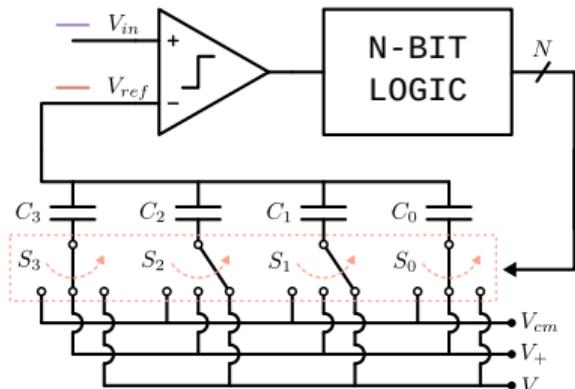




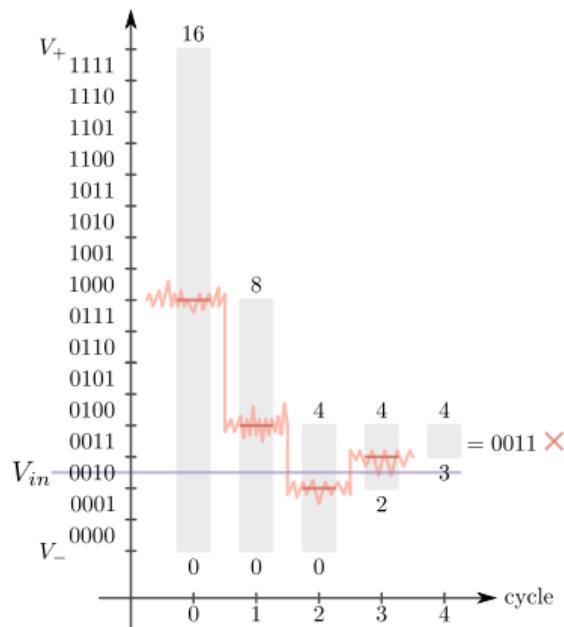
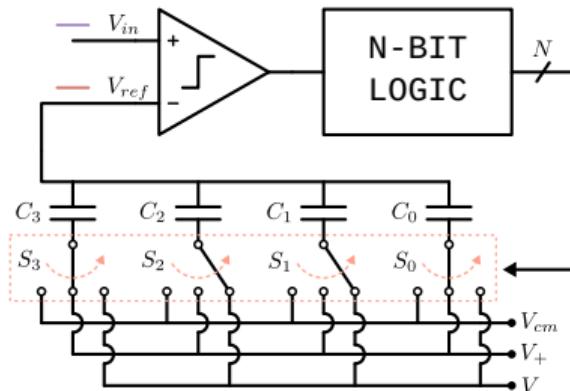




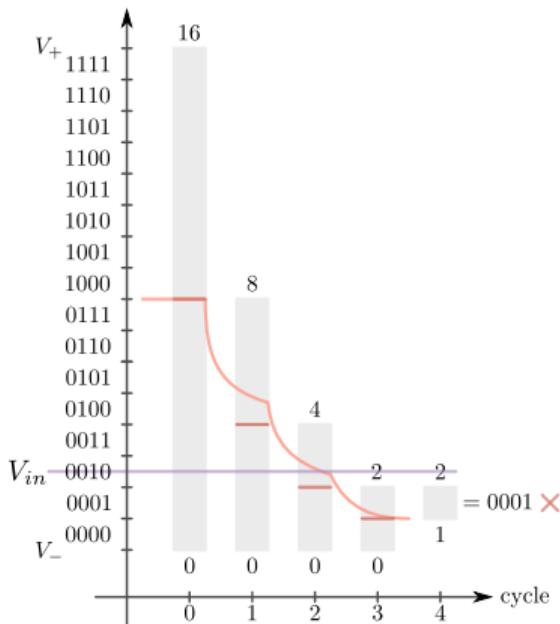
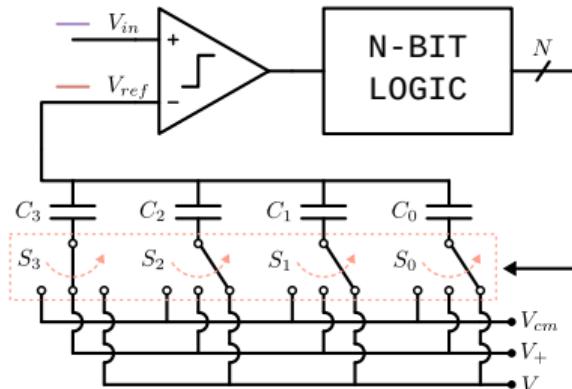
# Basic ideal operation



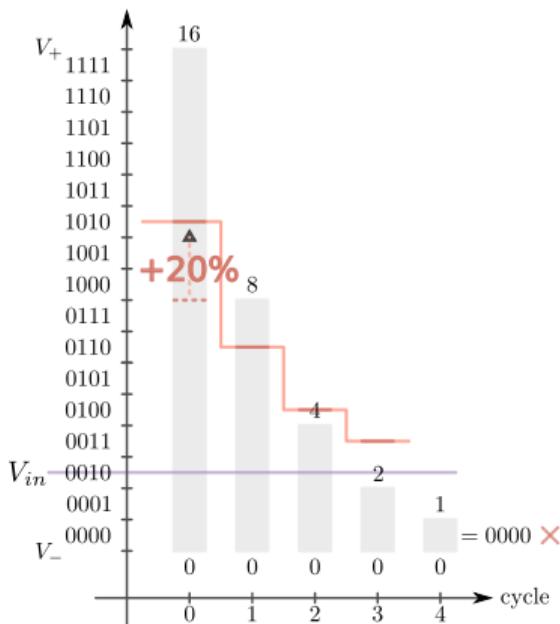
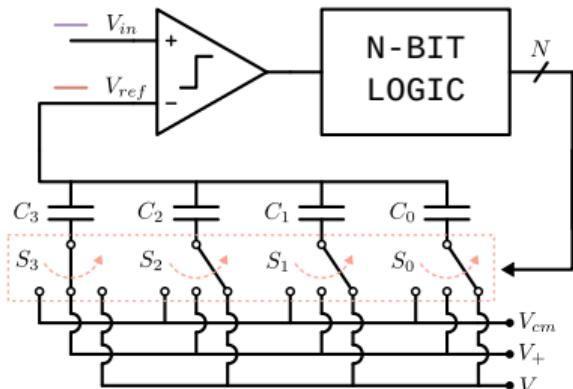
# Threshold and reference noise (dynamic error)



# Settling error (dynamic error)

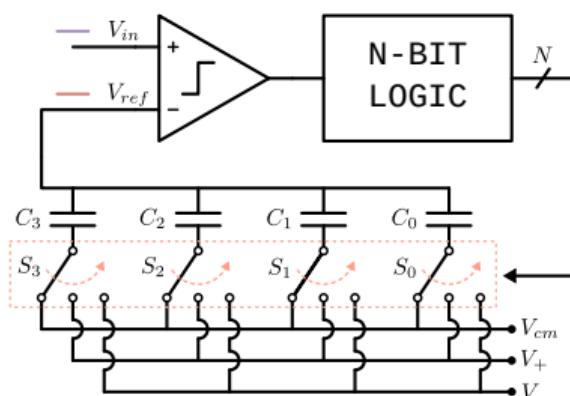


# Mismatch errors (static error)



## CDAC construction principles

For complete capacitor array. We'd like to be as close to min capacitance as possible, to the point that we'd have 125aF for unit caps in 10-bit design



$$\text{MOM cap density} \approx 0.5 \text{ fF}/\mu\text{m}^2$$

$$E_{CDAC} \approx CV^2$$

$$\tau_{CDAC} \approx R_{switch} \times C_{total}$$

$$C_\sigma \approx \frac{1}{\sqrt{C_{total}}}$$

$$V_{rms} = \sqrt{\frac{k_B T}{C}}$$

## CDAC construction principles

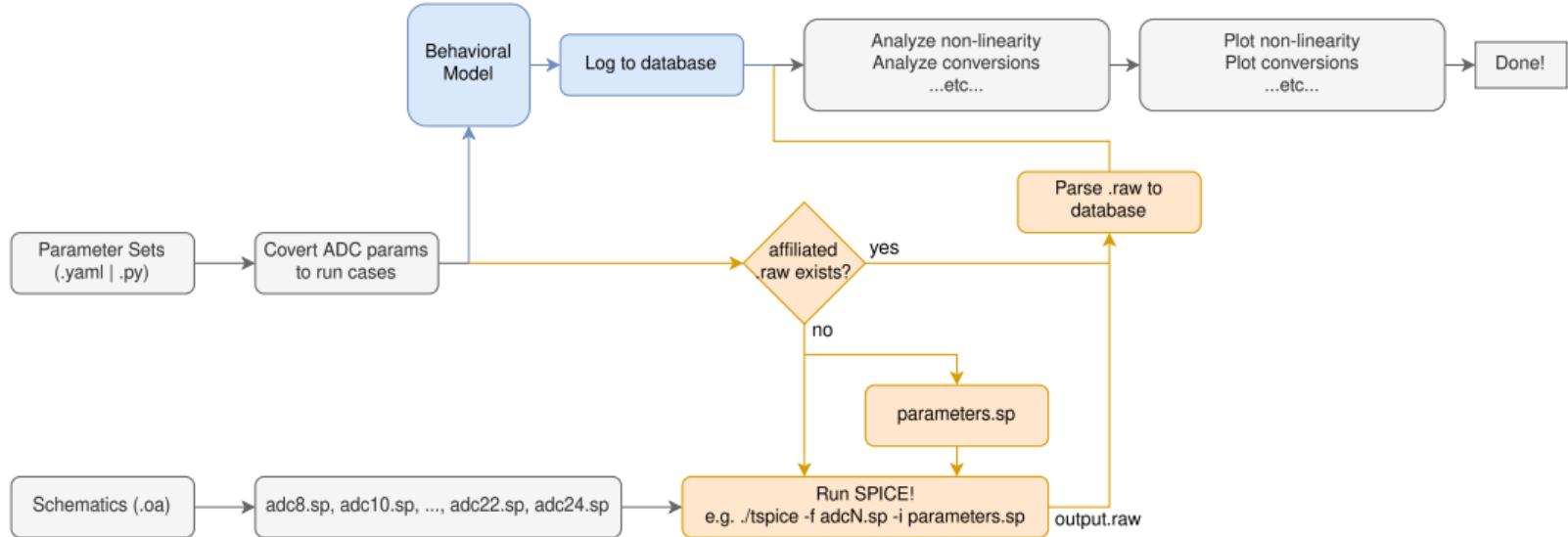
For individual capacitor weights

- ▶ Defining each bit weights as integers simplifies cap implementation; improves matching
- ▶ And defining each bit weight as sum of binary scaled values keeps DEC to just adders
- ▶ Finally, keeping sum total to binary scaled total prevents overflow

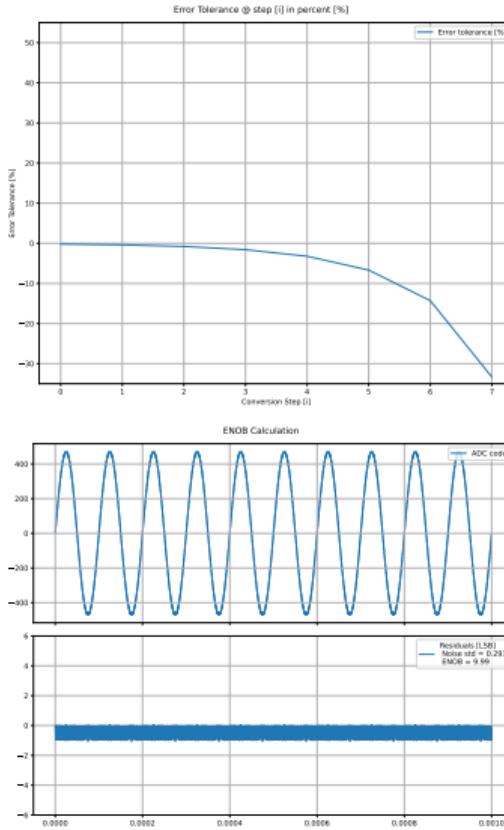
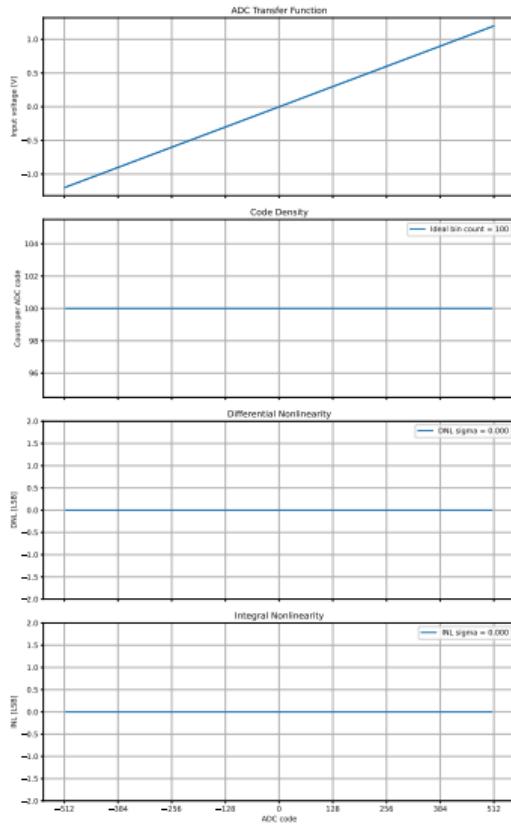
## SAR modeling status

- ▶ Threshold noise and variation, reference noise, settling error, capacitor mismatch supported
- ▶ Arbitrary CDAC weights, with support for "extended range bits"
- ▶ Monotonic and bidirectional-single-side switching supported (CRS, CAS, MCS to be added)
- ▶ Analyses for static and dynamic performance analyses ( $ENOB@f_s$ )
- ▶ Single test case requires 20 seconds
- ▶ Compatibility with T-Spice, AFS, and Spectre simulator (30hr run, 4hr with Spectre)

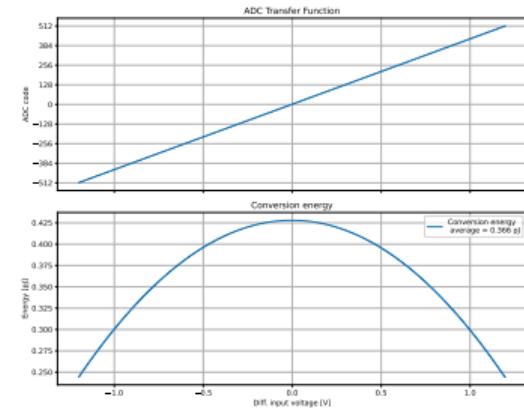
# SAR modeling status



# Ideal 10-bit operation



Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[256 128 64 32 16 8 4 2 1]	
DAC weights sum (+1)	512	
DAC capacitor array size	9	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	0.000	mV
Comparator offset	0.000	mV
Reference voltage noise	0.000	mV
DNL	0.00	LSB
INL	0.00	LSB
ENOB	9.99	bits
FOM (energy/conversion)	0.04	pJ



## Error tolerance strategies

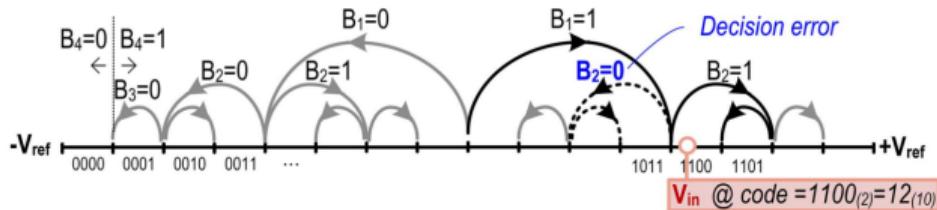
### Sub-radix 2 steps

- ▶ Creates overlapping search voltages
- ▶ In  $D_{out}$  processed as  $W_i \times B_i$
- ▶ Can also satisfy calibratability requirements

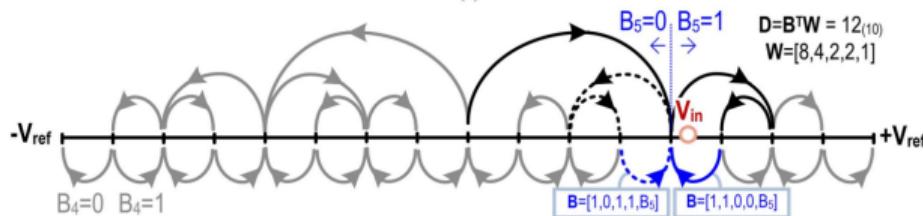
### Extended search steps

- ▶ In  $D_{out}$  processed as  $W_i \times (B_i - 0.5)$
- ▶ Decreases input amplitude swing to  $V_{ref} \times \frac{C}{d}$
- ▶ Introduced by CC Liu 2010, where they were additional cap,

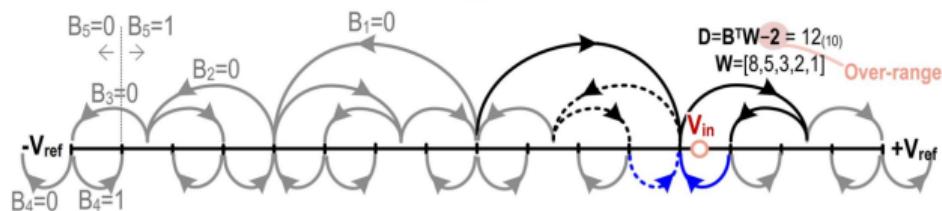
# Error tolerance strategies



(a)



(b)

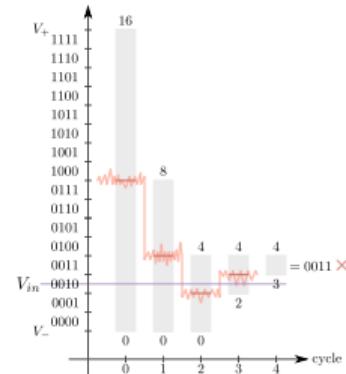
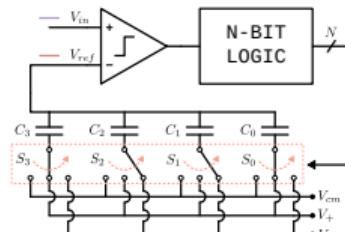


from HS Tsai 2015

## Device and reference noise correction

- ▶ In most common case, only small LSBs errors will occur from thermal noise.
- ▶ Can be corrected by single post-bits, or more comparator power

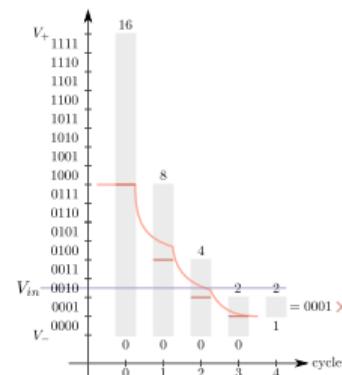
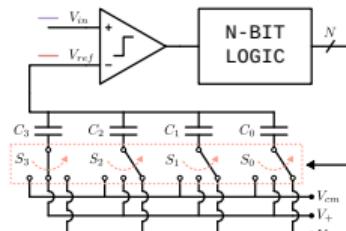
$$\sigma_n^2 \leq LSB^2 / 2 \times 12$$



# Settling error correction

Most pronounced in MSBs, recovery determined by remaining caps:

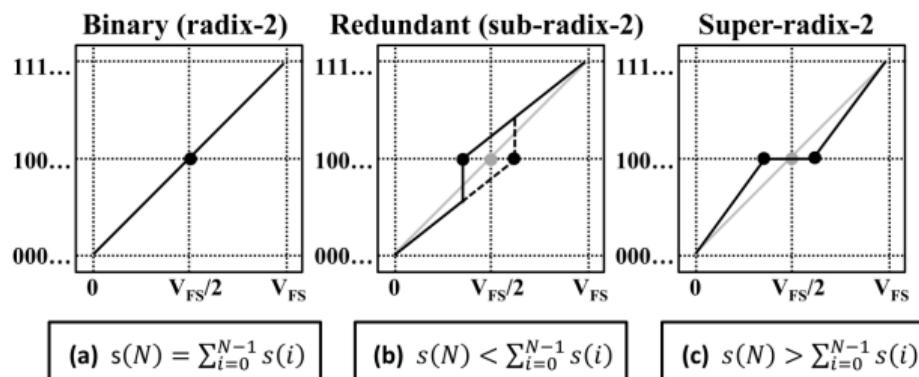
$$\text{Error tolerance } @B_i = \frac{\sum_{i+1}^M B_j - B_i}{\sum_i^M B_j} \times 100\%$$



## Mismatch static error & calibratability

- ▶ Redundancy can absorb static error, but what about mismatch?
- ▶ 1-bit comparator = inherently linear, so CDAC dominates
- ▶ Assuming monotonic switching, without cap-reuse like CRS [Tsai 2015]

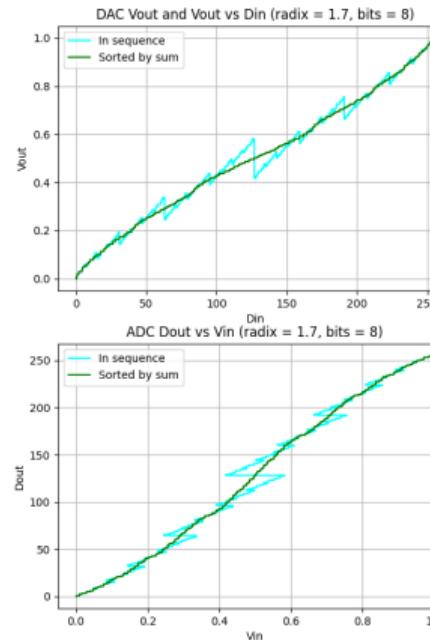
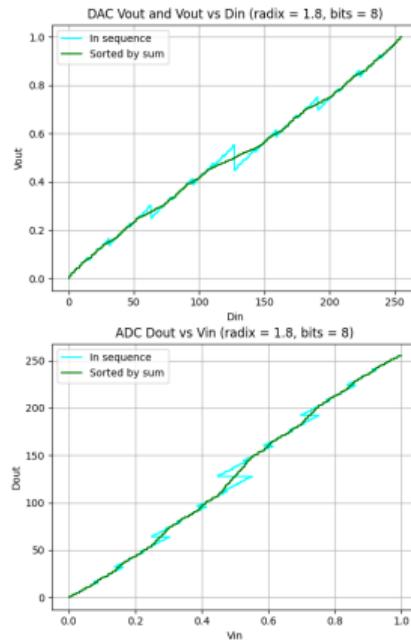
$$\sigma_{INL_{max}} \approx \frac{1}{2}(\sigma_{C_{unit}})\sqrt{2^N}$$



Visual from both A. Hsu 2013 and W. Liu 2010

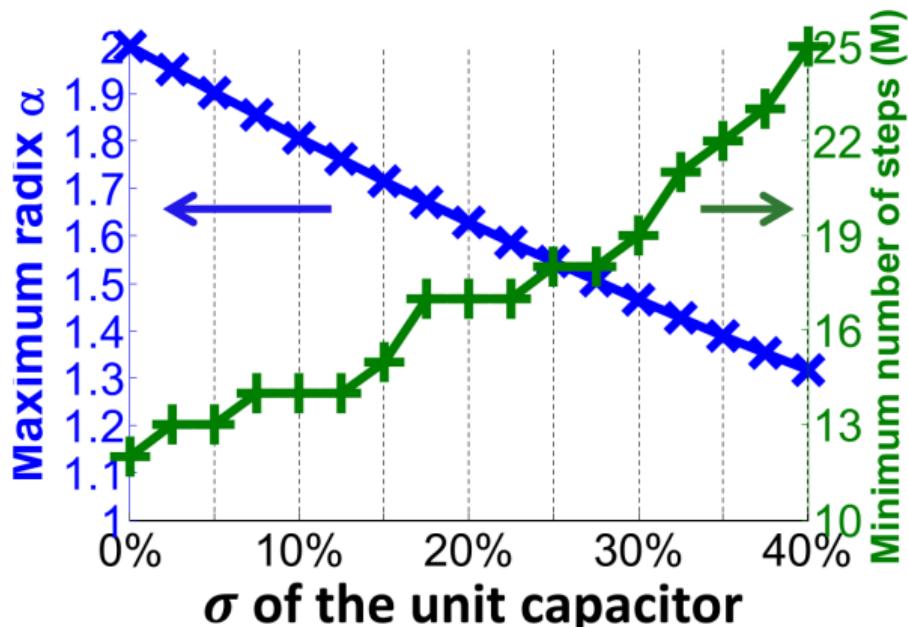
# Mismatch static error & calibratability

Lower radices create more overlap tolerance to prevent missing levels

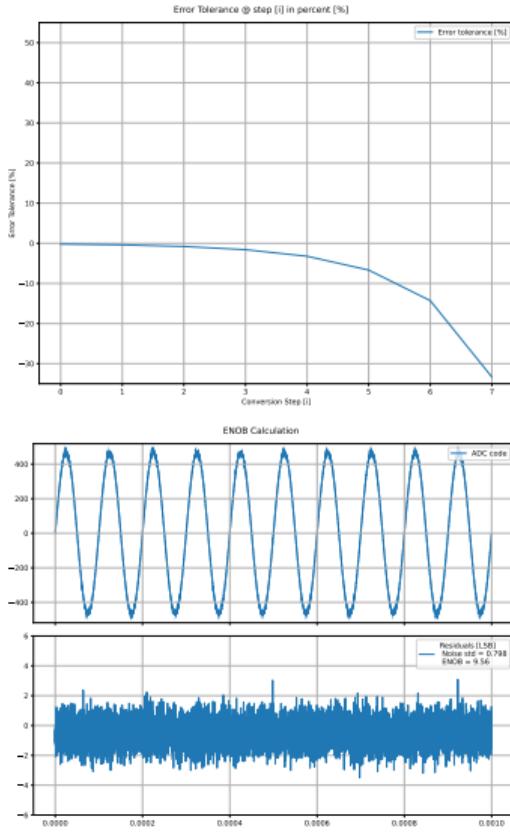
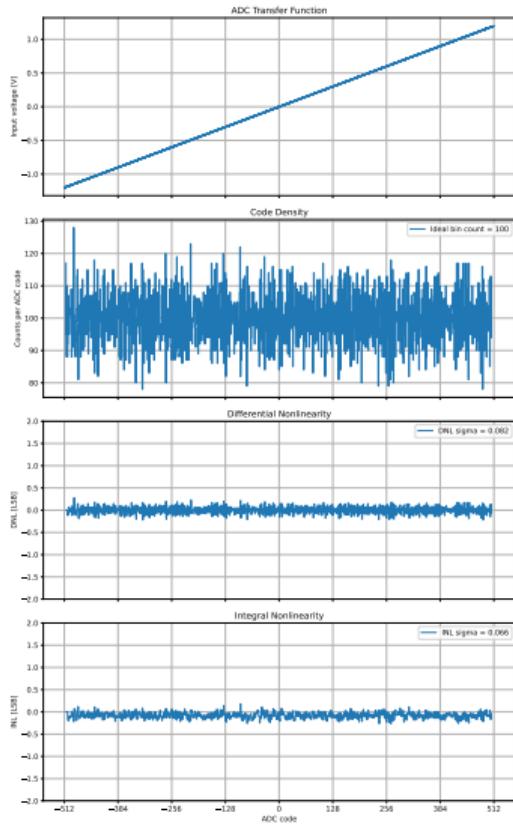


## Mismatch static error & calibratability

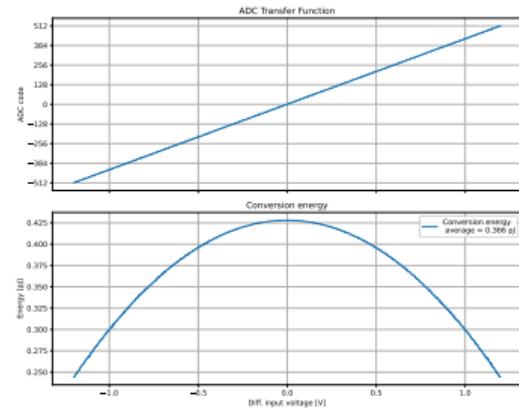
Radix  $\beta$  and min. steps vs unit cap mismatch  $\sigma_{C_{unit}}$  (A. Hsu 2013)



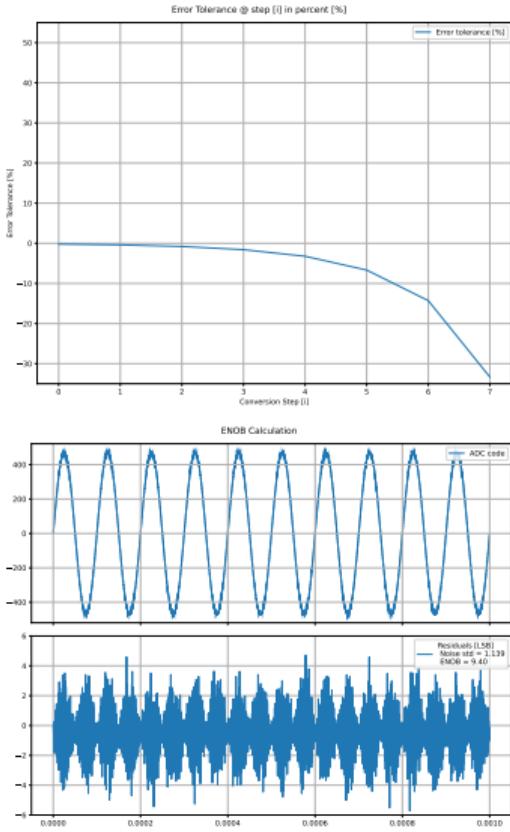
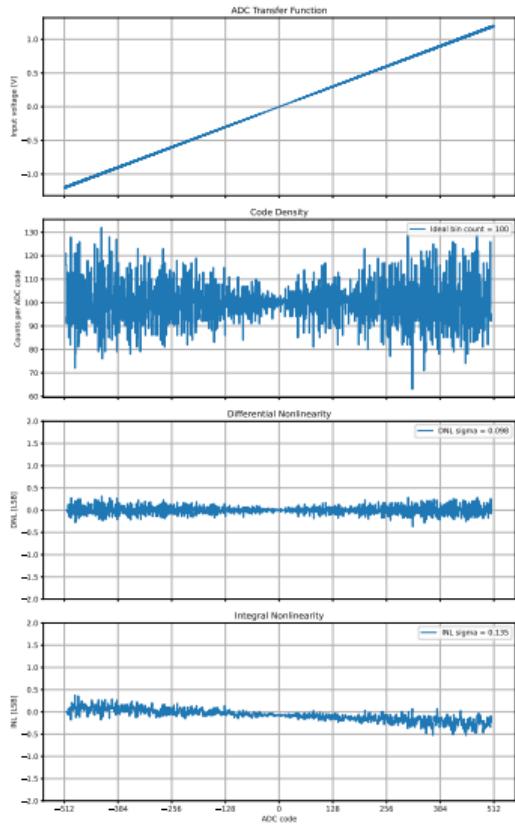
# 10-bit w/ device noise



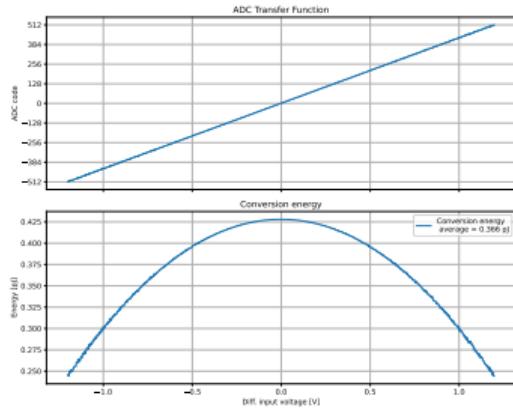
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[256 128 64 32 16 8 4 2 1]	
DAC weights sum (+1)	512	
DAC capacitor array size	9	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	0.000	mV
DNL	0.08	LSB
INL	0.07	LSB
ENOB	9.56	bits
FOM (energy/conversion)	0.04	pJ



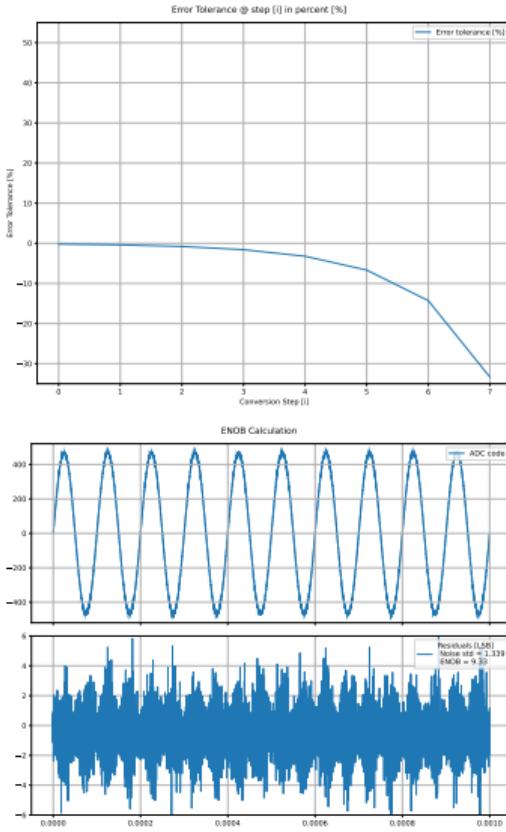
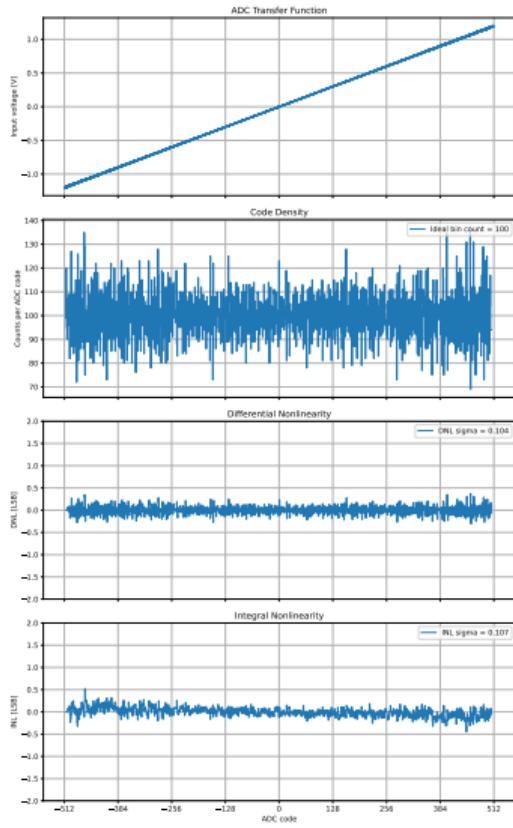
# 10-bit w/ reference noise



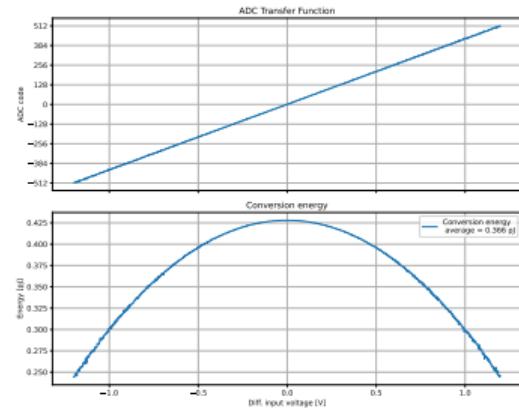
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[256 128 64 32 16 8 4 2 1]	
DAC weights sum (+1)	512	
DAC capacitor array size	9	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	0.000	mV
Comparator offset	0.000	mV
Reference voltage noise	5.000	mV
DNL	0.10	LSB
INL	0.13	LSB
ENOB	9.40	bits
FOM (energy/conversion)	0.04	pJ



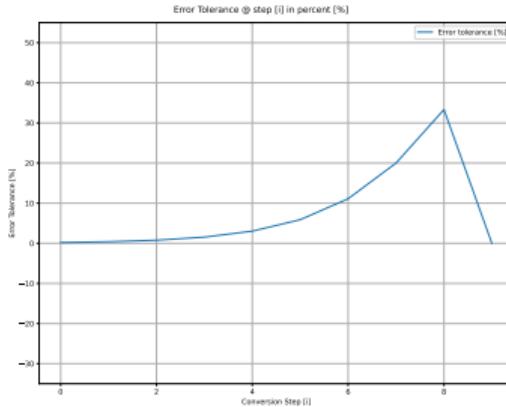
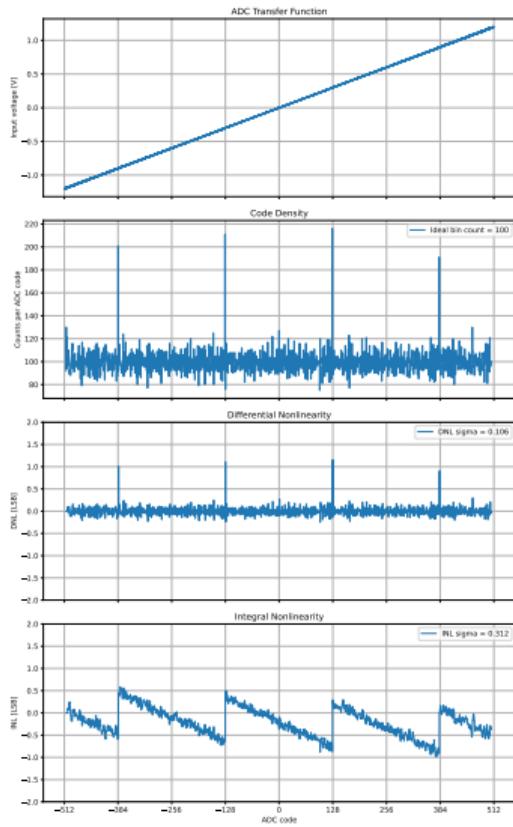
# 10-bit w/ device and reference noise



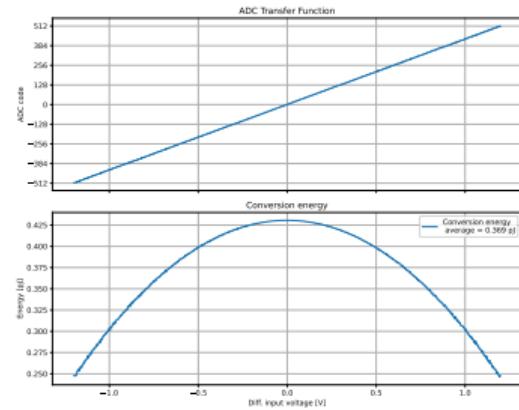
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[256 128 64 32 16 8 4 2 1]	
DAC weights sum (+1)	512	
DAC capacitor array size	9	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	5.000	mV
DNL	0.10	LSB
INL	0.11	LSB
ENOB	9.33	bits
FOM (energy/conversion)	0.04	pJ



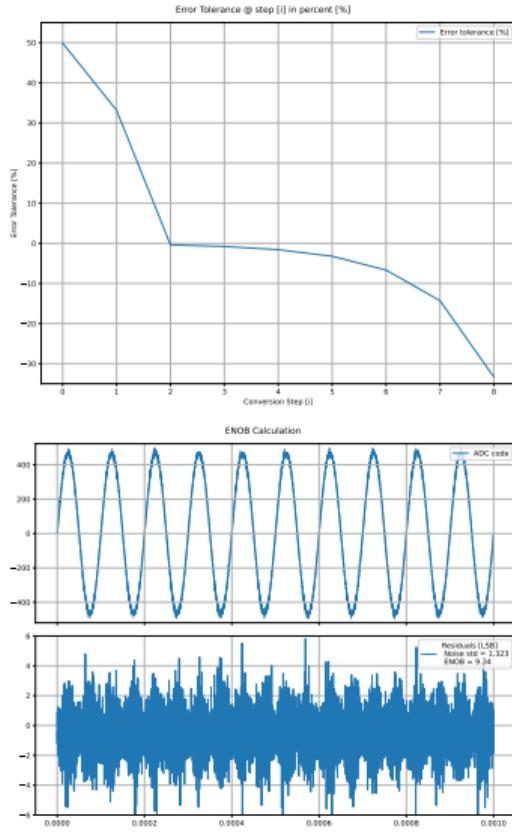
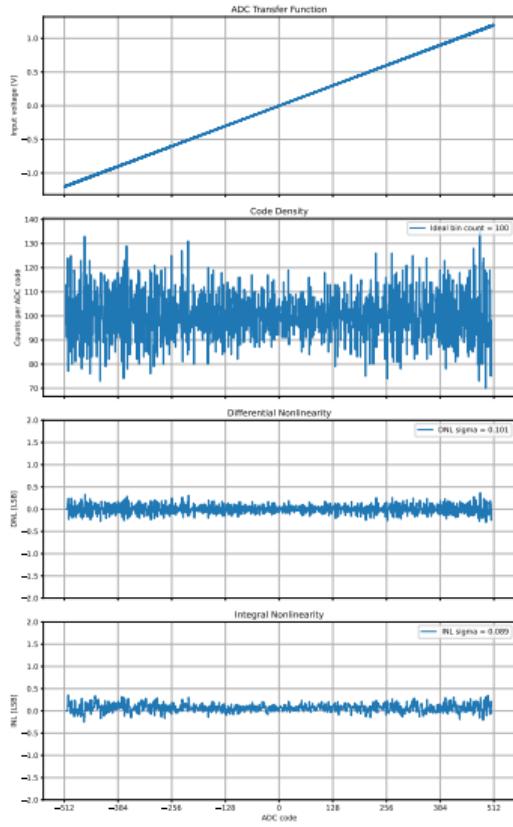
# 10-bit w/ noise and postconversions



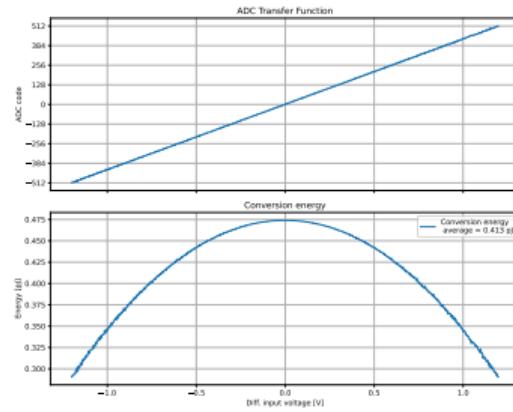
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[256 128 64 32 16 8 4 2 1 1 1]	
DAC weights sum (+1)	514	
DAC capacitor array size	11	fF
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	pF
DAC total capacitance	0.514	%
DAC settling error	0.00	mV
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	5.000	mV
DNL	0.11	LSB
INL	0.31	LSB
ENOB	9.42	bits
FOM (energy/conversion)	0.04	pJ



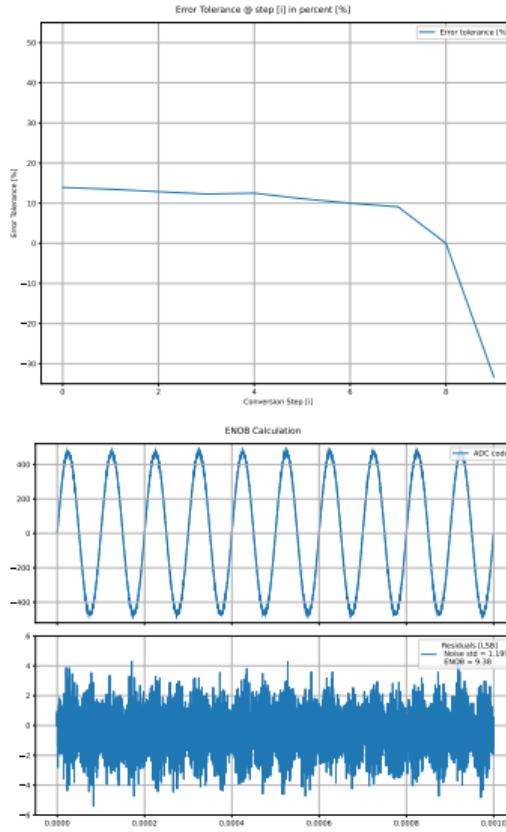
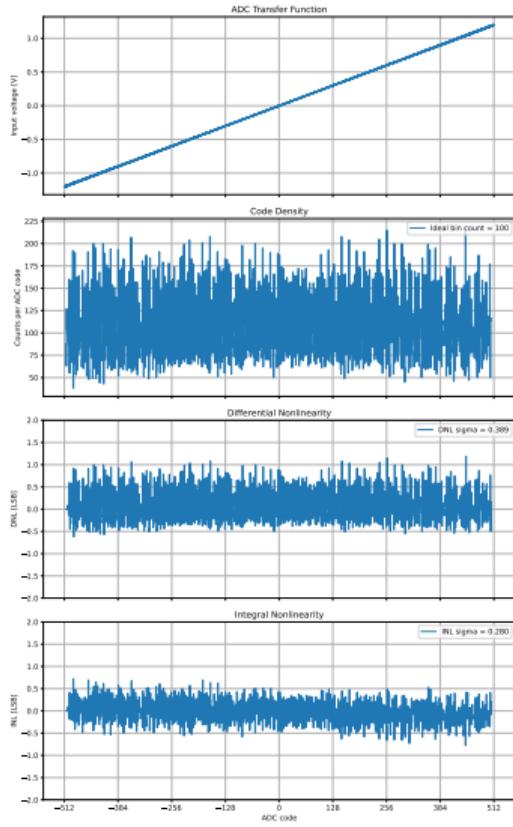
# 10-bit w/ noise and split MSB



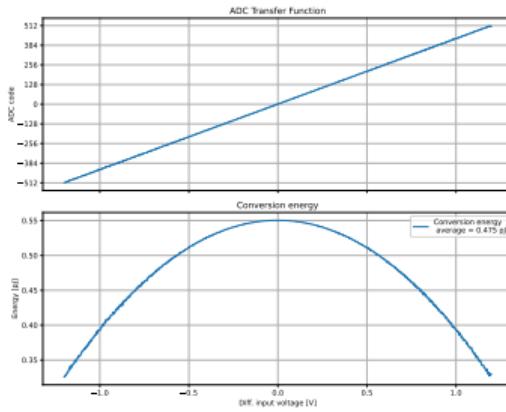
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[128 128 128 64 32 16 8 4 2 1]	
DAC weights sum (+1)	512	
DAC capacitor array size	10	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	5.000	mV
DNL	0.10	LSB
INL	0.09	LSB
ENOB	9.34	bits
FOM (energy/conversion)	0.04	pJ



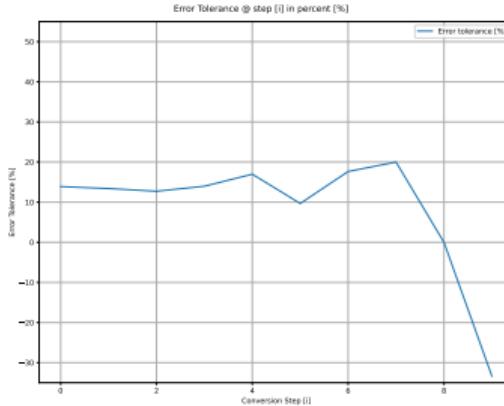
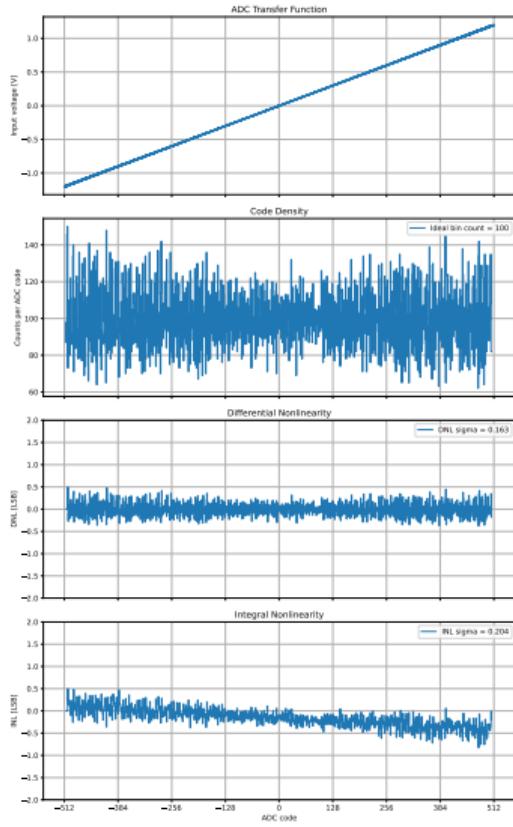
# 10-bit w/ noise and radix 1.75



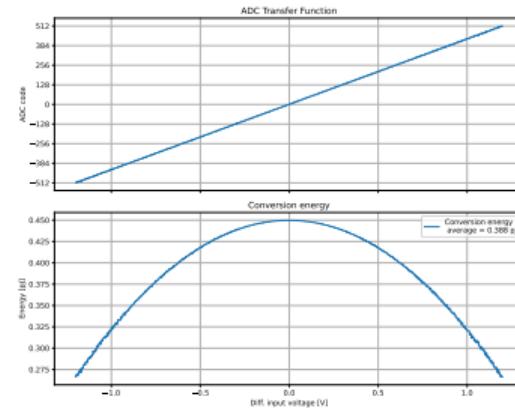
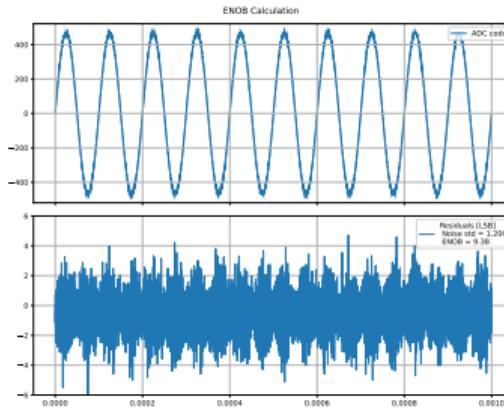
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[269 154 88 50 28 16 9 5 3 2 1]	
DAC weights sum (+1)	626	
DAC capacitor array size	11	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.626	pF
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	5.000	mV
DNL	0.39	LSB
INL	0.28	LSB
ENOB	9.38	bits
FOM (energy/conversion)	0.05	pJ



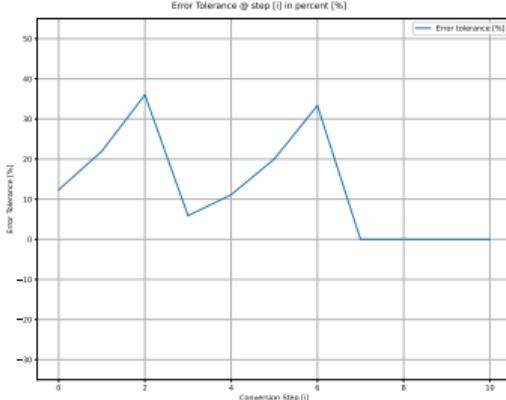
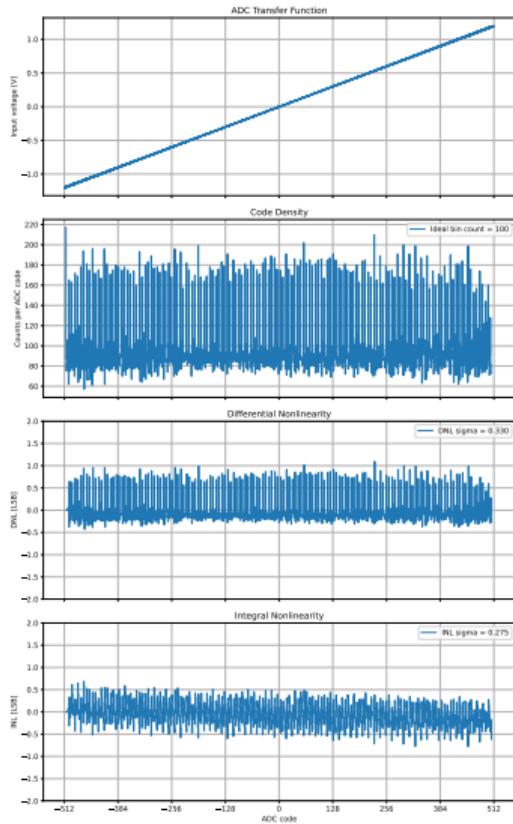
# 10-bit w/ noise and radix 1.75 normalized



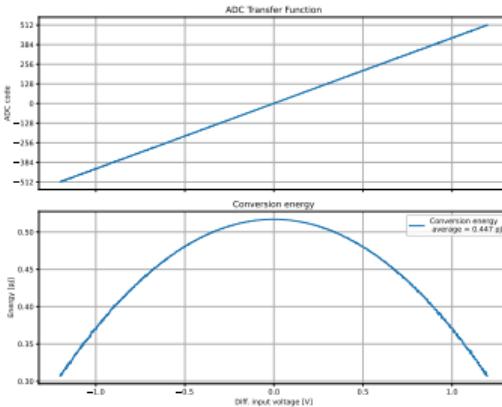
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[220 126 72 40 22 14 7 4 3 2 1]	
DAC weights sum (+1)	512	
DAC capacitor array size	11	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	pF
DAC total capacitance	0.512	%
DAC settling error	0.00	mV
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	5.000	mV
DNL	0.16	LSB
INL	0.20	LSB
ENOB	9.38	bits
FOM (energy/conversion)	0.04	pJ



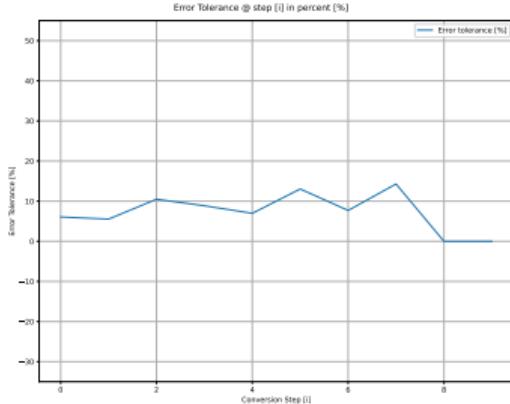
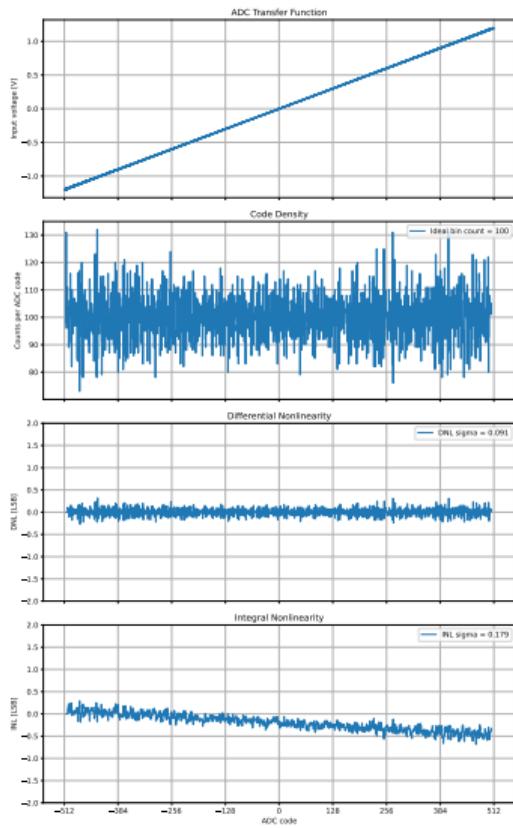
# 10-bit w/ noise and binary compensation



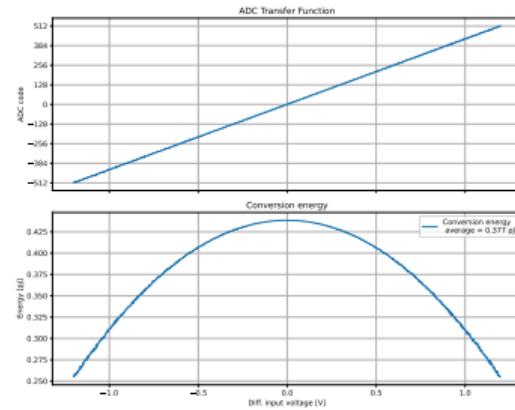
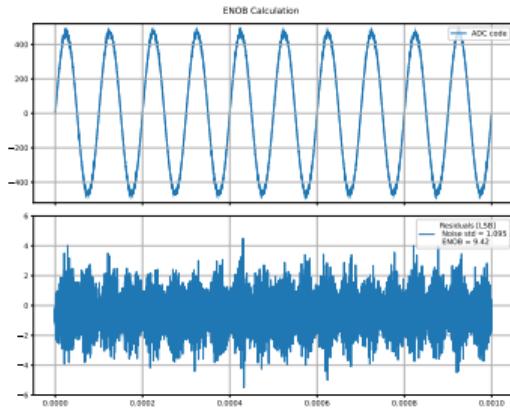
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[256 128 64 64 32 16 8 8 4 2 1 1]	
DAC weights sum (+1)	585	
DAC capacitor array size	12	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	pF
DAC total capacitance	0.585	
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	5.000	mV
DNL	0.33	LSB
INL	0.27	LSB
ENOB	9.40	bits
FOM (energy/conversion)	0.04	pJ



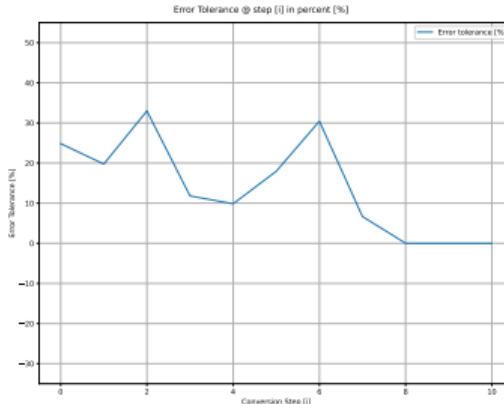
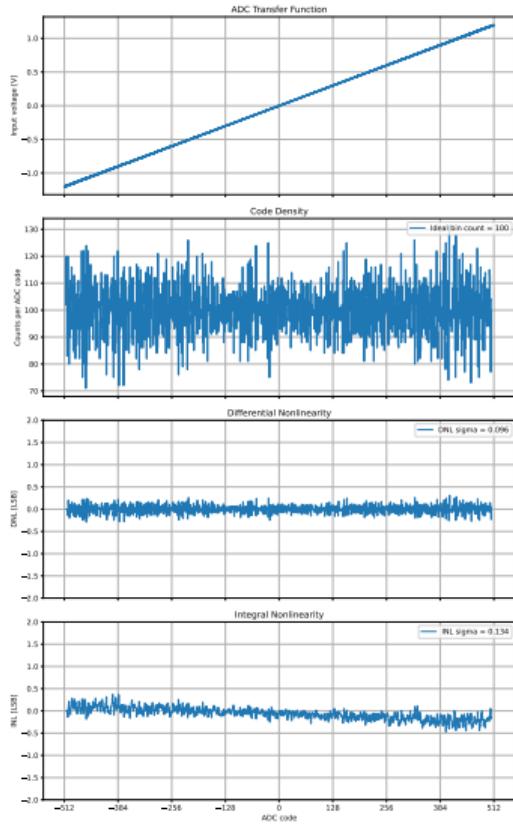
# 10-bit w/ noise and binary recombination



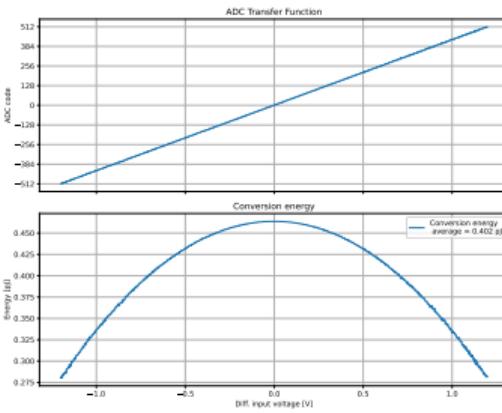
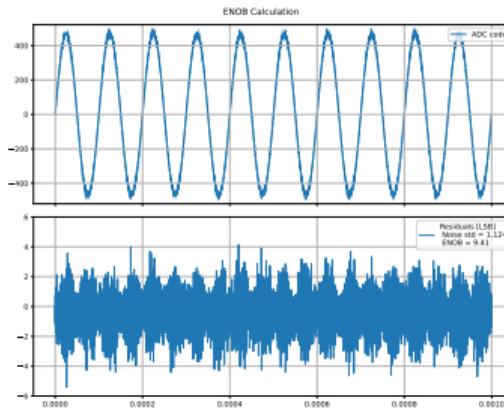
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[240 128 64 36 20 10 6 3 2 1 1]	
DAC weights sum (+1)	512	
DAC capacitor array size	11	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	5.000	mV
DNL	0.09	LSB
INL	0.18	LSB
ENOB	9.42	bits
FOM (energy/conversion)	0.04	pJ



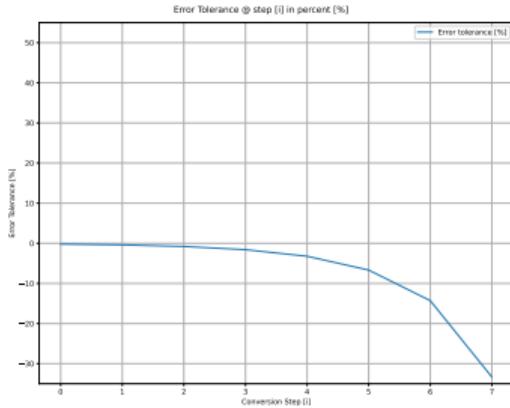
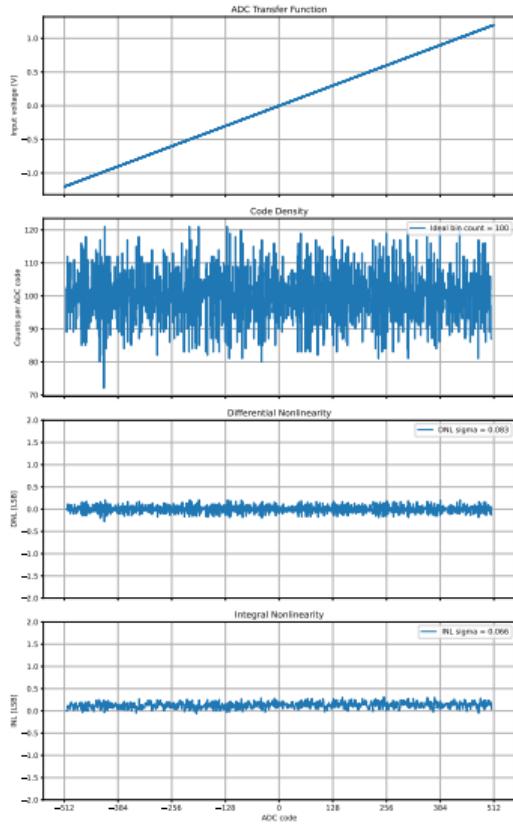
# 10-bit w/ noise and SC-ADEC



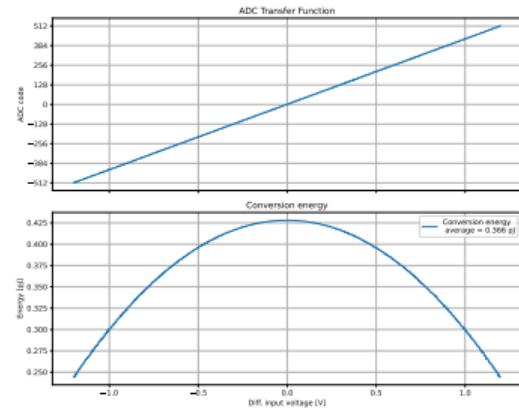
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[192 128 64 56 32 16 8 7 4 2 1 1]	
DAC weights sum (+1)	512	
DAC capacitor array size	12	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	pF
DAC total capacitance	0.512	
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	5.000	mV
DNL	0.10	LSB
INL	0.13	LSB
ENOB	9.41	bits
FOM (energy/conversion)	0.04	pJ



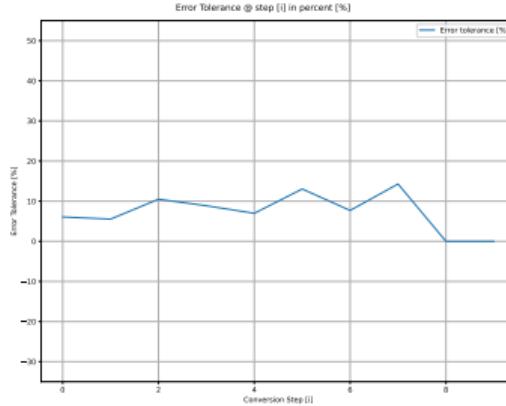
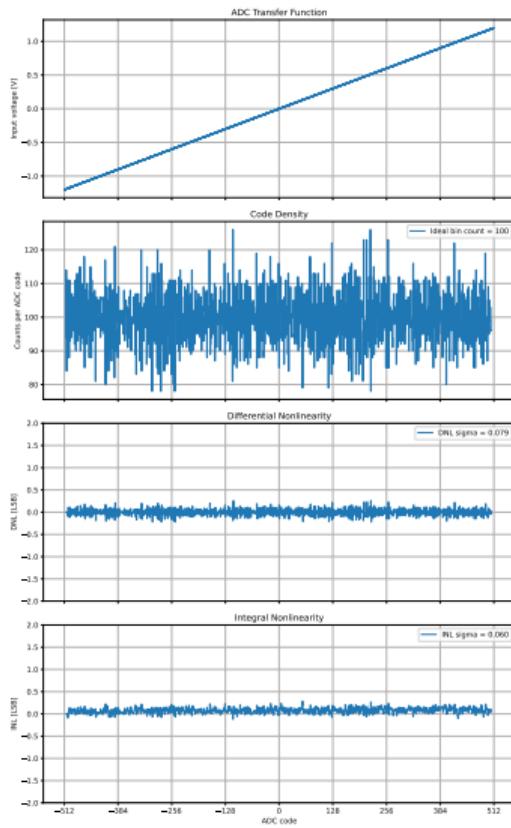
# 10-bit w/ settling error



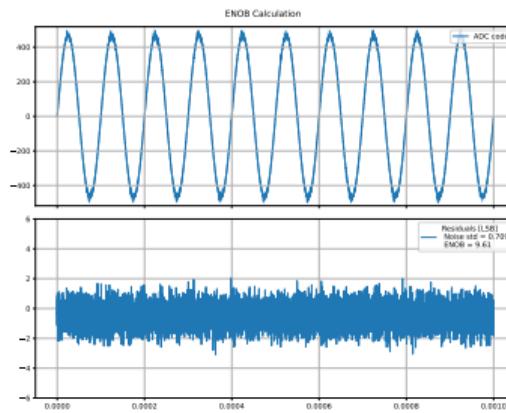
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[256 128 64 32 16 8 4 2 1]	
DAC weights sum (+1)	512	
DAC capacitor array size	9	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	0.000	mV
DNL	0.08	LSB
INL	0.07	LSB
ENOB	9.55	bits
FOM (energy/conversion)	0.04	pJ



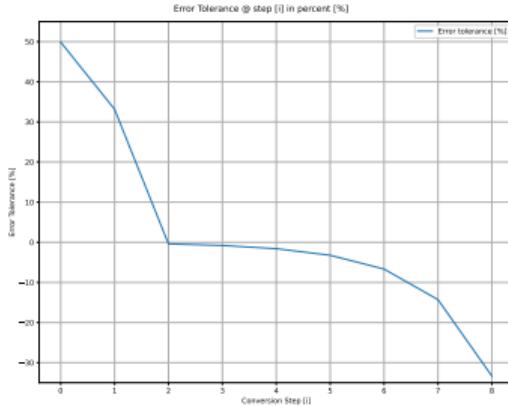
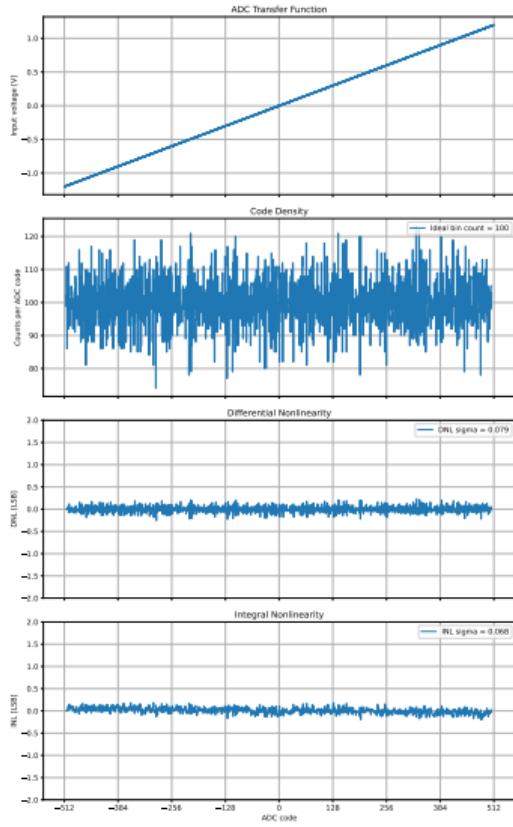
# 10-bit w/ settling error and binary recombination



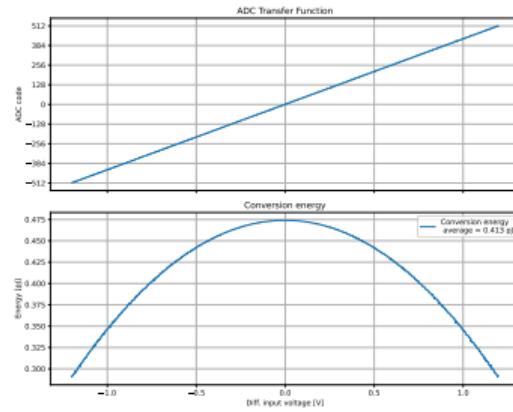
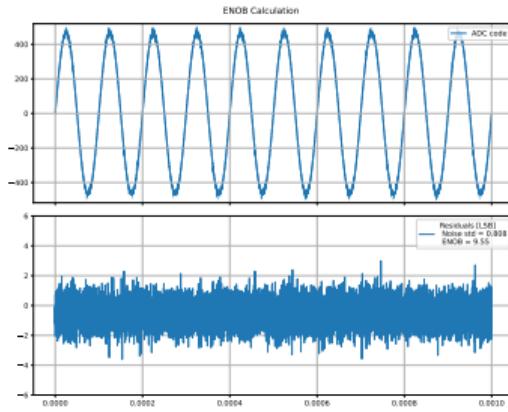
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[240 128 64 36 20 10 6 3 2 1 1]	
DAC weights sum (+1)	512	
DAC capacitor array size	11	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	pF
DAC total capacitance	0.512	
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	0.000	mV
DNL	0.08	LSB
INL	0.06	LSB
ENOB	9.61	bits
FOM (energy/conversion)	0.04	pJ



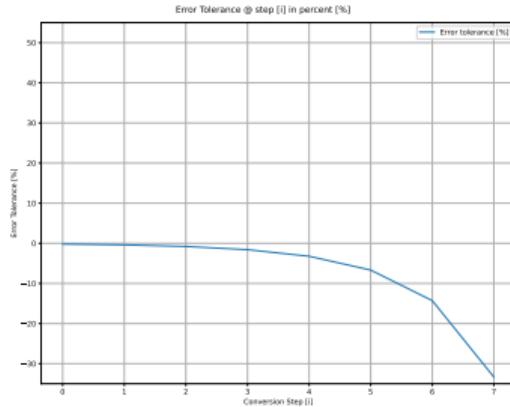
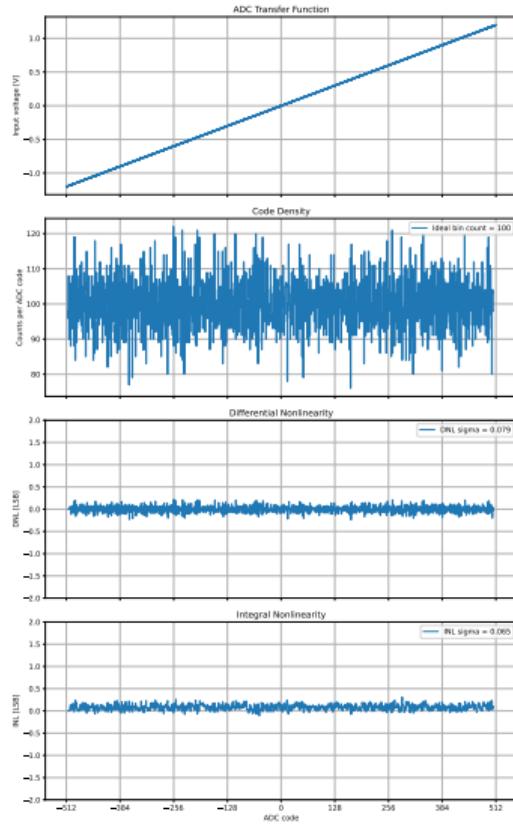
# 10-bit w/ settling error and SC-ADEC



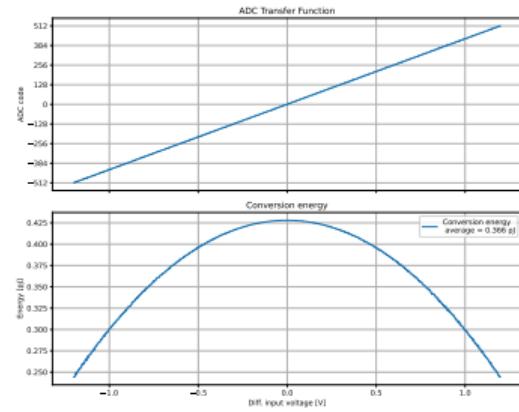
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[128 128 128 64 32 16 8 4 2 1]	
DAC weights sum (+1)	512	
DAC capacitor array size	10	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	0.000	mV
DNL	0.08	LSB
INL	0.07	LSB
ENOB	9.55	bits
FOM (energy/conversion)	0.04	pJ



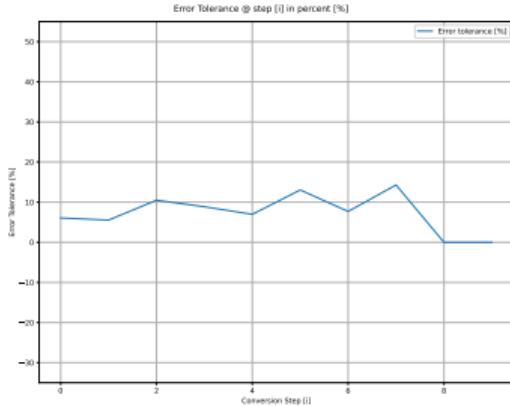
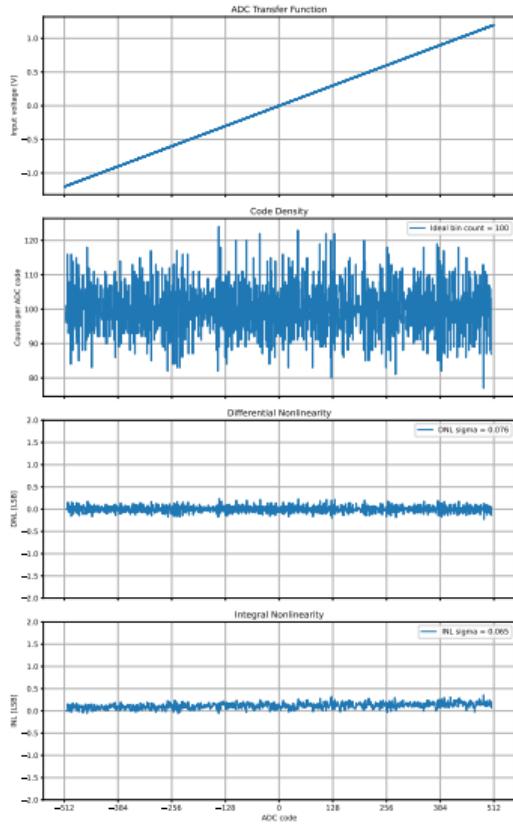
# 10-bit w/ mismatch



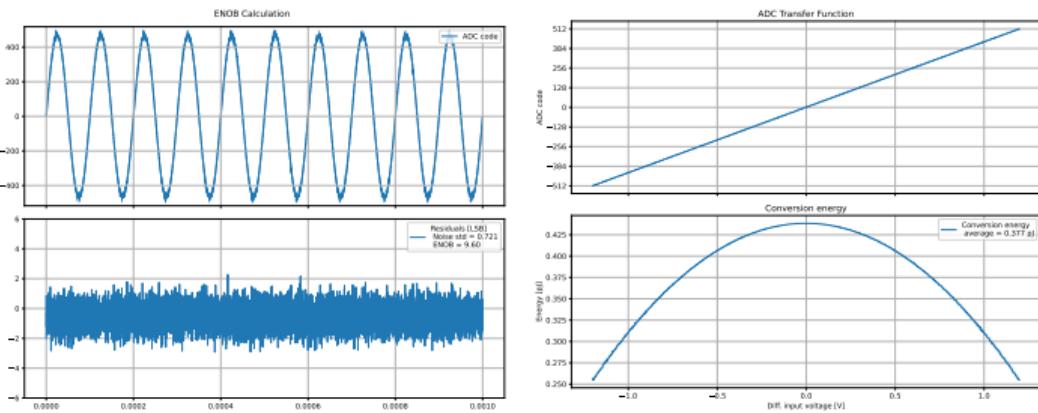
Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[256 128 64 32 16 8 4 2 1]	
DAC weights sum (+1)	512	
DAC capacitor array size	9	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	0.000	mV
DNL	0.08	LSB
INL	0.06	LSB
ENOB	9.56	bits
FOM (energy/conversion)	0.04	pJ



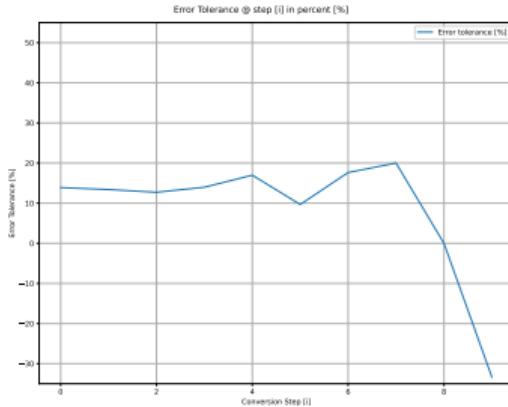
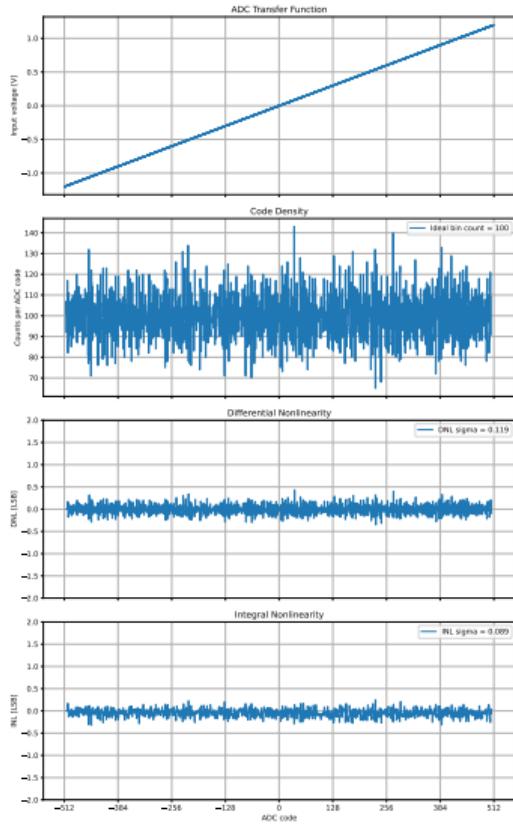
# 10-bit w/ mismatch and binary recombination



Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[240 128 64 36 20 10 6 3 2 1 1]	
DAC weights sum (+1)	512	
DAC capacitor array size	11	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	0.000	mV
DNL	0.08	LSB
INL	0.06	LSB
ENOB	9.60	bits
FOM (energy/conversion)	0.04	pJ



# 10-bit w/ mismatch and radix 1.75 normalized



Parameter	Value	Unit
Resolution	10	bits
Sample frequency	10.000	MspS
LSB size	2.344	mV
DAC weights array	[220 126 72 40 22 14 7 4 3 2 1]	
DAC weights sum (+1)	512	
DAC capacitor array size	11	
DAC unit capacitance	1.000	fF
DAC parasitic capacitance	1.000	fF
DAC total capacitance	0.512	pF
DAC settling error	0.00	%
Comparator noise	2.000	mV
Comparator offset	0.000	mV
Reference voltage noise	0.000	mV
DNL	0.12	LSB
INL	0.09	LSB
ENOB	9.58	bits
FOM (energy/conversion)	0.04	pJ

