

# A 0.003 mm<sup>2</sup> 10 b 240 MS/s 0.7 mW SAR ADC in 28 nm CMOS With Digital Error Correction and Correlated-Reversed Switching

Jen-Huan Tsai, Hui-Huan Wang, Yang-Chi Yen, Chang-Ming Lai, Yen-Ju Chen, Po-Chuin Huang, Ping-Hsuan Hsieh, Hsin Chen, and Chao-Cheng Lee

**Abstract**—This paper describes a single-channel, calibration-free Successive-Approximation-Register (SAR) ADC with a resolution of 10 bits at 240 MS/s. A DAC switching technique and an addition-only digital error correction technique based on the non-binary search are proposed to tackle the static and dynamic non-idealities attributed to capacitor mismatch and insufficient DAC settling. The conversion speed is enhanced, and the power and area of the DAC are also reduced by 40% as a result. In addition, a switching scheme lifting the input common mode of the comparator is proposed to further enhance the speed. Moreover, the comparator employs multiple feedback paths for an enhanced regeneration strength to alleviate the metastable problem. Occupying an active area of 0.003 mm<sup>2</sup> and dissipating 0.68 mW from 1 V supply at 240 MS/s in 28 nm CMOS, the proposed design achieves an SNDR of 57 dB with low-frequency inputs and 53 dB at the Nyquist input. This corresponds to a conversion efficiency of 4.8 fJ/c.-s. and 7.8 fJ/c.-s. respectively. The DAC switching technique improves the INL and DNL from +1.15/-1.01 LSB and +0.92/-0.28 LSB to within +0.55/-0.45 LSB and +0.45/-0.23 LSB, respectively. This ADC is at least 80% smaller and 32% more power efficient than reported state-of-the-art ADCs of similar resolutions and Nyquist bandwidths larger than 75 MHz.

**Index Terms**—Capacitor mismatch, DAC settling, digital error correction, dynamic comparator, metastability, SAR ADC, switching scheme.

## I. INTRODUCTION

SUCCESSIVE-APPROXIMATION-REGISTER (SAR) ADCs with capacitive DAC are renowned for their prominent energy efficiency, and have recently been widely used in sensor networks, biomedical ASICs, video and many general purpose applications [1] as the process technology progressively advances. In the past decade, significant efforts have been invested in the quest for ever-improving the figures-of-merits (FOM)<sup>1</sup> and speed of SAR converters. Fig. 1 shows the performance summary of state-of-the-art SAR ADCs. Excellent

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J.-H. Tsai is with National Tsing Hua University, Hsinchu, Taiwan (e-mail: jentsai1015@gmail.com).

H.-H. Wang, Y.-C. Yen, C.-M. Lai, Y.-J. Chen, P.-C. Huang, P.-H. Hsieh, and H. Chen are with National Tsing Hua University, Hsinchu, Taiwan.

C.-C. Lee is with Realtek Semiconductor Corporation, Hsinchu, Taiwan. Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

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<sup>1</sup>The (Walden) FOM for Nyquist ADCs is defined as:  $FOM = \frac{\text{Power}}{\text{Sampling Speed}} \times 2^{\text{ENOB}_{\text{Nyquist}}}$

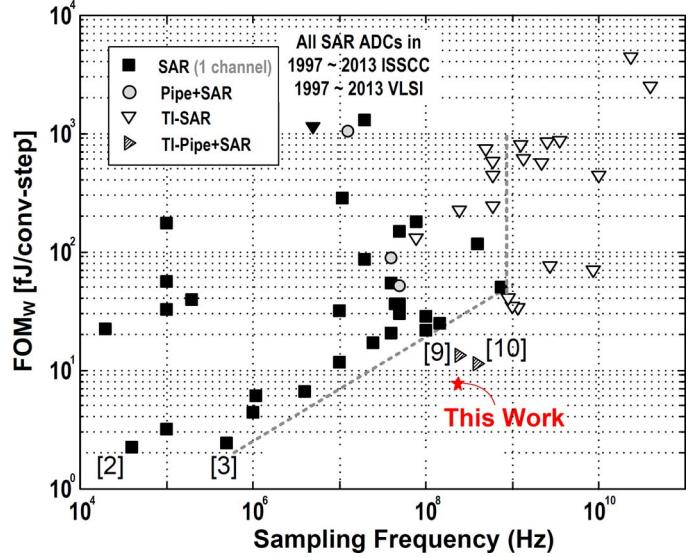


Fig. 1. Performance comparison of  $FOM_W$  with all SAR ADCs from ISSCC/VLSI 1997 ~ 2013.

FOMs of less than 3 fJ/conversion-step (fJ/c.-s.) are recently achieved in [2]–[4] at a speed lower than 4 MS/s by introducing energy-efficient DAC switching methods and suppressing the comparator noise. For SAR ADCs, higher sampling rate above 100 MS/s is conventionally realized by employing time-interleaving, pipelining operations [5]–[11], hybrid architectures with a fast coarse ADC [5]–[7]. Among these architectural approaches, the dynamic pipelined SAR architecture with time-interleaving (TI) [9], [10] outstands with the best energy efficiency, as revealed in Fig. 1. In [10], the 410 MS/s 2× TI pipelined SAR ADC reports an SNDR of 59.8 dB with an FOM of 11.4 fJ/c.-s.. However, it occupies an area of 0.11 mm<sup>2</sup> in the 28 nm CMOS process and requires calibration. Moreover, the speed of the constituent single-channel ADC is still limited to 205 MS/s in spite of being pipelined. Another method to achieve high speed is to convert more bits at a time, as shown with the 9 bit 900 MS/s 2× TI SAR ADC in [11]. However, the overhead of the extra comparators and DACs for reference generation leads to an area of 0.038 mm<sup>2</sup> and an FOM of 40.5 fJ/c.-s. in the 45 nm process. In summary, prior Nyquist ADCs of all kinds with the resolution above 8 bits and speed higher than 160 MS/s exhibit an FOM greater than 11.4 fJ/c.-s. [9] and an area larger than 0.015 mm<sup>2</sup> [12]. In particular, the

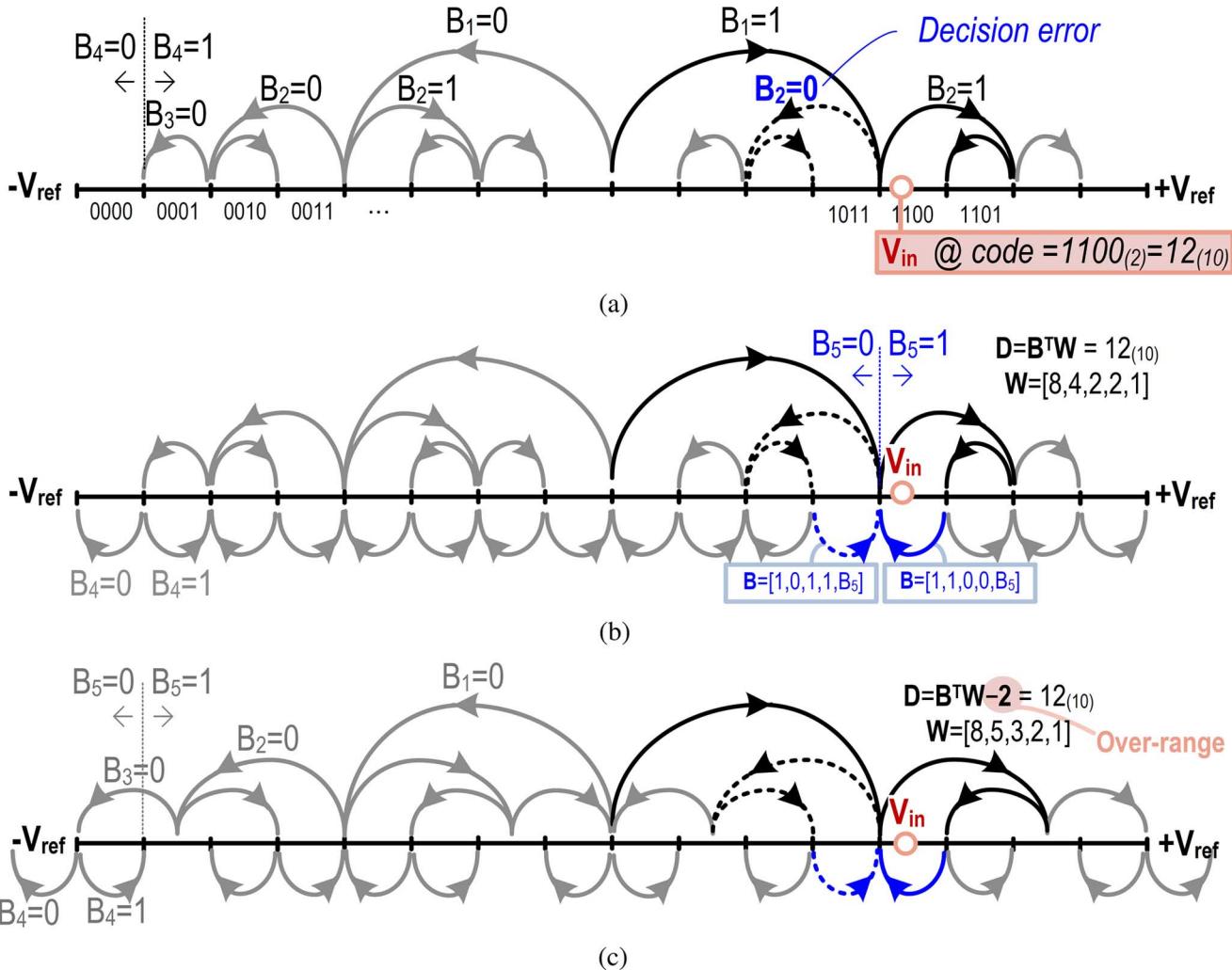


Fig. 2. Search processes of a 4 bit SAR ADC employing various algorithms. (a) Conventional binary search : (Cap. array:  $2^2, 2, 1$ ) (b) Extended binary search : (Cap. array:  $2^2, 2, 1, \underline{2^0}$ ) (c) Sub-radix-2 : (e.g., Cap. array:  $2^{12/6}, 2^{8/6}, 2^{4/6}, 2^0$  for radix- $2^{4/6}$ ).

sampling rate of a single-channel SAR ADC with a resolution greater than 9 bits remains below 220 MS/s [12]. In order to further improve the performance of the SAR-based ADCs, the fundamental design issues are carefully analyzed.

The performance indexes of a SAR ADC, including the power, speed, area and input impedance, are closely related to its DAC, whose total capacitance hinges upon either the ( $kT/C$ ) noise or the matching requirement for linearity. Premised on achieving an ENOB above 9 bits and the maximum DNL/INL smaller than 1/2 LSB with a yield greater than 99.7% ( $\pm 3\sigma$  coverage) [13], [14], the overall performance is usually limited by the large capacitance of the DAC for sufficient matching. Traditionally, calibration techniques are utilized to trim the static DAC non-ideality in either an analog [15] or a digital [16] manner, but the overheads are non-negligible. On the other hand, as incomplete DAC settling also degrades linearity, high-speed SAR conversion dictates a prohibitively high bandwidth, and hence high power consumption for the reference generation. For example, the DAC in a 10 bit 240MS/s SAR ADC has to settle down with 10 bit accuracy within 0.2 ns, given that leaving equal amount of time for sampling and conversion.

As surveyed exhaustively in [17], various redundancy techniques have been proposed to relax the settling issue, speed up the conversion and reduce the power of the peripheral buffers. The robustness of high-speed conversion is also improved since incomplete DAC settling might as well be resulted from PVT variations, or other dynamic interferences such as the power/ground bouncing. In [18], B. Murmann reviews prior designs with redundancy: R. Vitek re-introduces the prevalent 1.5 bit concept in pipeline ADCs to the SAR ADC [12]. Some extend the searching beyond binary levels by adding redundant (binary) search levels [19], [20]. The others resort to the sub-radix-2 algorithm with either a fixed radix [16], [21]–[23] or non-fixed radices of less than two [24]. Fig. 2(a) reveals how the conventional binary search is vulnerable to intermediate errors. As each quantization level has only one unique search trajectory, decision errors are irrevocable. In contrast, Figs. 2(b)–2(c) illustrate the later two types of non-binary techniques. Overlapped searching paths provide bounded tolerance to errors in the sense that multiple bit patterns  $B$  can lead to the same approximation  $D$  (within  $\pm 0.5$  LSB to the input  $V_{in}$ ) after multiplying  $B$  with proper bit-weights  $W$  (i.e.,  $D = BW^T$ ) and eliminating the coding offset.

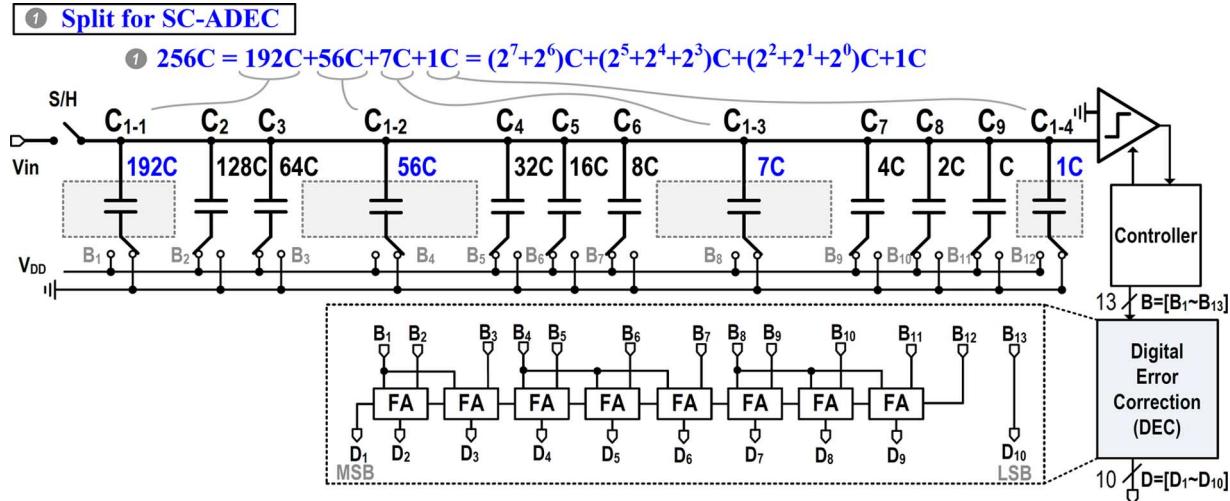


Fig. 3. The half circuit of the proposed 10 bit differential SAR ADC with the SC-ADEC technique (DAC at the sampling phase, and FA stands for a full adder).

This paper describes a 10 bit 240 MS/s SAR ADC without interleaving nor pipelining. Several techniques are exploited to improve the power, speed and area efficiency, seeking to break beyond the performance barrier of a single-channel SAR ADC as outlined in Fig. 1. An addition-only Digital Error Correction (DEC) technique based on splitting capacitors is proposed to provide a wide error-tolerance range without requiring redundant capacitors beyond the binary levels. Design guidelines for optimizing speed and DEC logic are also given. In addition, a DAC switching technique called correlated-reversed switching (CRS) is proposed to suppress the DAC non-linearity due to capacitor mismatch, allowing an equivalent 1 bit improvement of the DAC linearity. Furthermore, other circuit implementation techniques are proposed for high-speed operation. Adopting all these techniques, this work overcomes the performance bottleneck, reporting an FOM of 4.6~7.8 fJ/c.-s. across the Nyquist band and an area of 0.003 mm<sup>2</sup> without any calibration in place. The rest of this paper is organized as the following. After an architecture overview, Section II explains the two techniques addressing the dynamic and static non-idealities, respectively. The circuit implementations are detailed in Section III. The measurement results are discussed in Section IV. Finally, Section V concludes the contribution.

## II. ARCHITECTURE OVERVIEW AND THE PROPOSED TECHNIQUES

Fig. 3 shows the half circuit of the 10 bit differential SAR ADC. It highlights the initial DAC arrangement for redundancy. The ADC consists of a top-plate-sampling DAC, a comparator, a controller, and a DEC logic that converts raw 13 bit output codes B to error-corrected 10 bit codes D. The differential realization reduces the hardware of DAC to 9 bits.

### A. Redundancy Based on Split-Capacitor With Addition-Only DEC (SC-ADEC)

As illustrated in Fig. 4, the proposed SC-ADEC technique splits the original MSB capacitor ( $C_{MSB}$ ) to several sub-capacitors, which are either inserted in between or added to the original binary capacitors. Conceptually, this is analogous

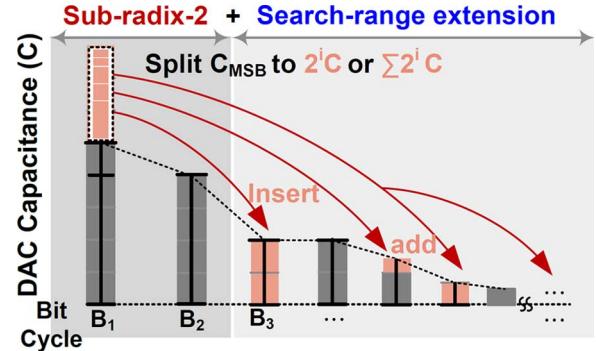


Fig. 4. The proposed SC-ADEC technique and the DAC switching sequence.

to the combination of the fore-mentioned sub-radix-2 and search-range extension techniques (Figs. 2(b)-2(c)). As revealed in Fig. 5, postponing the search with the split capacitors to later steps generates overlapped searching paths, while the total number of DAC capacitors is unchanged. Applying this approach to this work, the original  $C_{MSB}$  of  $2^8 C$  is split into four capacitors  $C_{1-1} \sim C_{1-4}$  of [192 C, 56 C, 7 C, 1 C] respectively, as shown earlier in Fig. 3 where C is the unit capacitor. These four capacitors are interleaved and sorted monotonically with the binary LSB capacitors  $C_2 \sim C_9$ . Since the split capacitors  $C_{1-2} \sim C_{1-4}$  are redundant to the binary LSB DAC, they extend the search ranges for the LSB steps. Meanwhile, the MSB searching becomes less aggressive with a smaller  $C_{MSB}$ , analogous to the sub-radix-2 algorithm. This arrangement tolerates at least 14.3% of settling errors in each cycle.

As also shown in Fig. 3, the DEC logic consists of only eight full-adders (FA). It converts the raw output codes B with bit-weights of W into the error-corrected codes D by  $D = BW^T$ , as depicted in Fig. 6. In order to let the elements of W be digitally representable without extra quantization error, every split capacitor ( $C_{1-i}$ ) has the form of either  $2^k C$  or  $\sum 2^k C (k \in N)$ . The splitting design keeps the total DAC capacitance unchanged such that the DEC computes with “addition” only without overflowing. Moreover, since an FA takes three inputs in maximum,

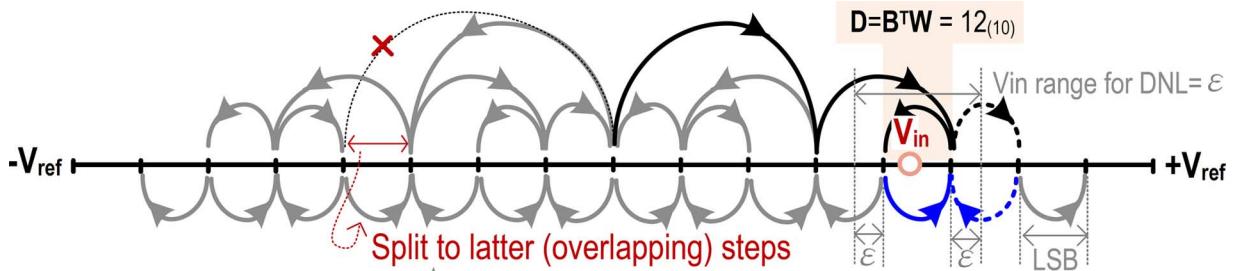
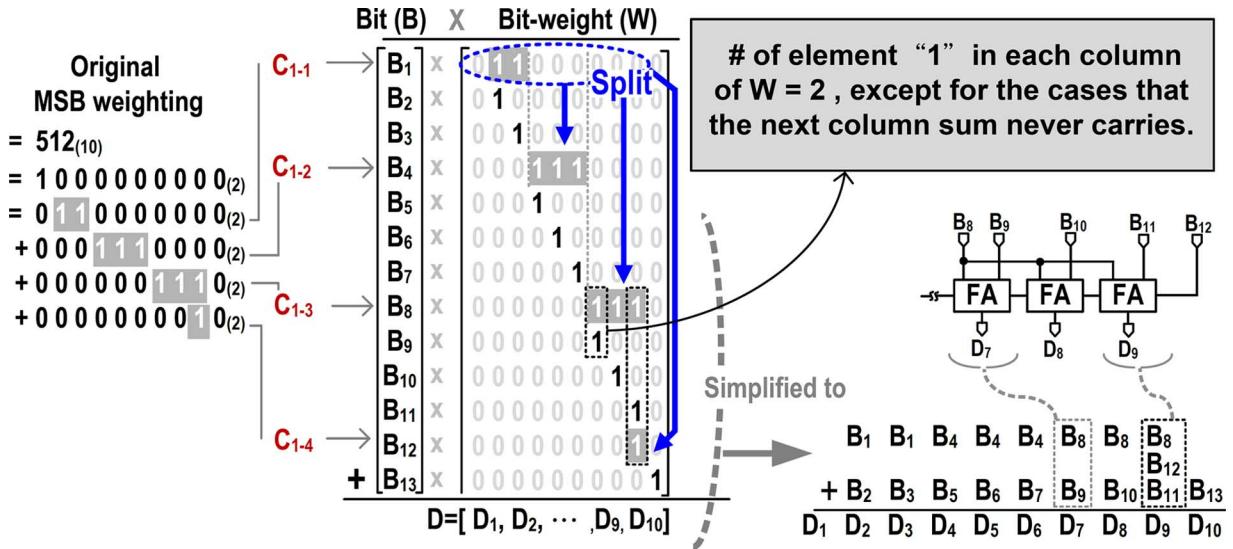
Fig. 5. Proposed approach for redundancy generation with Cap. array:  $2^2-2^0, 2^1, 2^0, 2^0$ . (In this example,  $\mathbf{W} = [8-2, 4, 2, 2, 1] = [6, 4, 2, 2, 1]$ ).

Fig. 6. Arithmetic table illustrating the constrained splitting for simpler DEC logics.

the following constraint can be enacted to minimize the number of FAs: Any two split capacitors contain no identical binary capacitor components. As highlighted in Fig. 6, each bit-weight column contains two “1”s in maximum except for  $D_9$  whose subsequent column ( $D_{10}$ ) never has carries. The hardware for DEC as well as the conversion latency are thus minimized.

In the choice of the amount of the capacitors being split out and additional bit-cycles, this design aims at a tolerance range larger than 12.5% as in [19], [22] for all cycles to mainly cover the DAC settling error and possible process variations. We want all cycles covered by redundancy since the robustness of the LSB section is equally important for an accurate conversion.

Considering an  $N$ -bit differential SAR ADC with a binary-scaled DAC and an MSB capacitor  $C_{MSB}$  of  $2^{N-2}C$ , a redundancy of  $2^{-x}(x > 0)$  of the full scale can be obtained by adding a geometric capacitor series  $[2^{-x}C_{MSB}, 2^{-2x}C_{MSB}, \dots, 1 C]$  to extend the searching range coverage based on the principle in Fig. 2(b). Instead of using extra redundant capacitors, the proposed SC-ADEC borrows the search-extending capacitors from the original  $C_{MSB}$ . The new  $C_{MSB}$  reduces to about  $2^{N-2}(1 - 2^{-x})C$  after the splitting. The amount of additional cycles is thus estimated as:  $N_{excess} \cong \log_2[2^{N-2}(1 - 2^{-x})]/\log_2 2^x \cong [N - 2/x]$ . Apply  $x = 3$  for a redundancy of at least  $2^{-3}$  of the previous decision range. Three extra cycles are used accordingly for this design. Then, instead of splitting out only binary-scaled

capacitors with  $[2^{-x}C_{MSB}, 2^{-2x}C_{MSB}, \dots, 1 C] = [32 C, 4 C, 1 C]$  as the redundant capacitors, we adopt  $[(2^5 + 2^4 + 2^3)C, (2^2 + 2^1 + 2^0)C, 2^0 C] = [56 C, 7 C, 1 C]$  to obtain larger redundancy in MSBs as more steps are postponed, and a simpler DEC logic (by obeying the enacted constraint), and facilitates the combination with the CRS technique (Section II-B). Since the last redundancy step adds only 1 LSB in redundancy and still costs a complete cycle, it could be removed at the cost of a reduced code range if the robustness of LSBs is not a concern.

On the other hand, redundancy also elevates the conversion speed as inaccurate settling is tolerable. By assuming the time required for each cycle is the same and confined by the longest cycle, the total conversion time can be estimated by taking into account the time penalty, denoted as  $T_{cmp}$ , for each comparator decision. For simplicity, we define a parameter  $\rho = T_{cmp}/\tau_{DAC}\ln 2$ , where  $\tau_{DAC}$  is the time constant of the DAC. As derived in the Appendix, the optimal solution maximizing the speed requires a redundancy of  $2^{-\lceil \sqrt{\rho(N-2)/N} \rceil} \cdot 100\%$  for the SC-ADEC and search-range extension techniques [19]. For  $T_{cmp} = 4\tau_{DAC}$ , choosing three redundant cycles maximizes the speed. Note that the proposed SC-ADEC technique can also be realized by other decent decompositions for different considerations, and hence not necessarily following the presented design step. For instance, selecting  $[192, 128, 80, 40, 32, 16, 8, 6, 4, 2, 2, 1]$  optimizes

TABLE I  
COMPARISON OF ERROR TOLERANCE TECHNIQUES.

Reference	This Work	JSSC'11 [1] Sang-Hyun Cho	ISSCC'10 [19] Chun-Cheng Liu	VLSI'11 [24] Hung-Yen Tai	ISSCC'02 [22] Franz Kuttner
Technique	SC-ADEC	ADEC	Binary Error Compensation (BEC)	AWCA	Sub-radix-2
Capacitor	integer (binary + non-binary)	integer (binary)	integer (binary)	integer	integer
Radix	< 2 @ MSB & 2 @ LSBs	2	2 (Add radix-2 caps.)	<2 (Non-fixed)	<2 (Fixed 2 <sup>10/12</sup> ~ 1.78)
Capacitor Overhead	None			Additional Capacitance ( $C_{\text{total}} > 2^{\text{bit}-1}$ C) Need overflow & underflow removal	None
DEC Logics / Digital Logics	8 FA	7FA <sup>†3</sup>	1 FA, 6 HA	9 FA, 1 HA, 10 MUX	11 × 10-b ROM, 10-b Adder (Sequential logics) <sup>†4</sup>
(Minimum) Tolerance Range	≥ 14.3%	≥ 20%	≥ 12.5%	≥ 12.5%	≥ 7.5%
†1 Reduced Total Settling Time	62.56%	69.03%	37%	59.99%	58.47%
Total Bit Cycles / Resolution	13 / 10b		12 / 10b	13 / 10b	11 / 10b
†2 Improved Normalized Speed	26.72%	29.99%	15.44%	25.43%	27.89%
†3	The other mentioned decomposition [192,128,80,40,32,16,8,6,4,2,1] based on the proposed SC-ADEC and optimization guidelines.				
†4	It calculates the output error-corrected code and the corresponding DAC control codes. The output binary code are decoded to thermometer DAC control codes.				

<sup>†1</sup> Numbers are calculated with  $\varepsilon = 0.5$  for all techniques and normalized to that of a conventional binary SAR ADC.

<sup>†2</sup> Assume  $T_{\text{cmp}} = 2\tau_{\text{DAC}}$  and the sampling time equals to the total conversion time.

<sup>†3</sup> The other mentioned decomposition [192,128,80,40,32,16,8,6,4,2,1] based on the proposed SC-ADEC and optimization guidelines.

<sup>†4</sup> It calculates the output error-corrected code and the corresponding DAC control codes. The output binary code are decoded to thermometer DAC control codes.

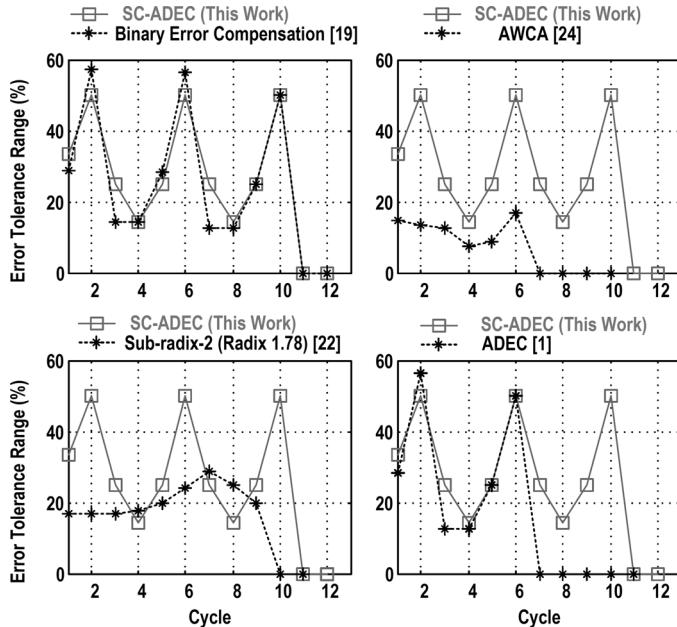


Fig. 7. DNL-free error tolerance range in each switching cycle ( $\varepsilon = 0$ ).

the redundancy and DEC logics (gate counts and latency) concurrently.

Fig. 7 compares the error tolerance capability of this and the other designs [1], [19], [22], [24]. This work achieves a wide redundancy coverage. Table I further compares the cost and performance of these different non-binary designs. Prior sub-radix-2 designs entail complex arithmetical units [22], [24]. Over-/under-flow removals are typically employed for designs that use extra redundant capacitors [19]–[21], [24]. They also suffer from reduced conversion gains as the LSB level becomes smaller. The extended range (e.g., 10.2 bit range in [19]) is

hardly usable because it generally gets truncated to accommodate an integer-bit binary coding unless the over-range is resided in a pipelined SAR stage as in [25]. In comparison, this design achieves comparable tolerance and speed improvement with minimal circuit overheads. In particular, as in [1], [22] the amount of total DAC capacitors (loading) is maintained on par with that in conventional binary-weighted designs [26] without redundancy.

In principle, all non-binary techniques for redundancy are based on the  $\beta$ -expansion for real numbers [18], [27], and differ in the radix and DAC selections. The DACs are mostly realized by an integer amount of unit capacitors for better matching. Extended beyond by the discussions in [18], [28], Table II summarizes the non-binary techniques. Note that  $[r]$  outputs the first integer larger than the real number  $r$ . The redundancy resides in the flexibility of multiple sets of code  $B_i$  in constructing the same ADC input  $y$  (normalized to the full-scale range). The proposed SC-ADEC method guarantees a unity conversion gain ( $\alpha$ ) and provides more flexibility in tweaking the redundancy via the relaxed constraint for DAC's radix (i.e.,  $\beta_i/\beta_{i+1}$ ). In practice, redundancy can be used to repair errors from different non-idealities and hence can be optimized in different ways and through various dedicated (referred) design strategies. The presented DAC design takes the redundancy coverage, speed and circuit overhead into accounts. As to be seen soon, the compatible CRS technique further reduces the unit capacitance for higher speed.

#### B. Correlated Reversed Switching (CRS) for Capacitor Mismatch Compensation

With an inherently-linear, 1 bit quantizer in the SAR feedback loop, the maximum achievable linearity is limited by the DAC. While the applied redundancy technique absorbs dynamic

TABLE II  
EXPRESSING A/D CONVERSION BASED ON BETA-EXPANSION

		the beta-expansion and constraints
*Generalized A/D conversion		$\hat{y} = \alpha \left( \sum_{i=1}^M B_i [2^N \beta_i] 2^{-N} \right) = \frac{\mathbf{B}^T \mathbf{W}}{\sqrt{\mathbf{W}^T \mathbf{W}}}$
Conventional binary (radix-2)		$\beta_i = 2^{-i}, \alpha = 1, M = N$
Non-binary	sub-radix-2	fixed radix $2^{N/M}$ [22, 23]
		$\beta_i = (2^{N/M})^{-i}, \alpha \approx 2^{N/M} - 1, M > N$
		$\beta_i = \sum 2^{-j}, j \in \mathbb{N}, \alpha = (\sum_{i=1}^M [2^N \beta_i] 2^{-N})^{-1}, 1 < \beta_i / \beta_{i+1} < 2$
		Same as the above row, except $\beta_i / \beta_{i+1} \in \{1, 2\}$
radix-2 with extended search [1, 19]		
sub-radix-2 with extended search (this work)		$\beta_i = \sum 2^{-j} \text{ or } 2^{-j}, j \in \mathbb{N}, \alpha = 1, 1 \leq \beta_i / \beta_{i+1} \leq 2$

\* $N$ -bit  $M$ -cycle SAR ADCs for a continuous input variable  $0 \leq y < 1$ .  $\hat{y} - y$  is the quantization error.  $\mathbf{B} = [B_1, B_2, \dots, B_M]$ ,  $B_i \in \{0, 1\}$ . The bit-weight  $\mathbf{W} = [w_1, w_2, \dots, w_M]$ .  $w_i$  is  $[2^N \beta_i]$ .

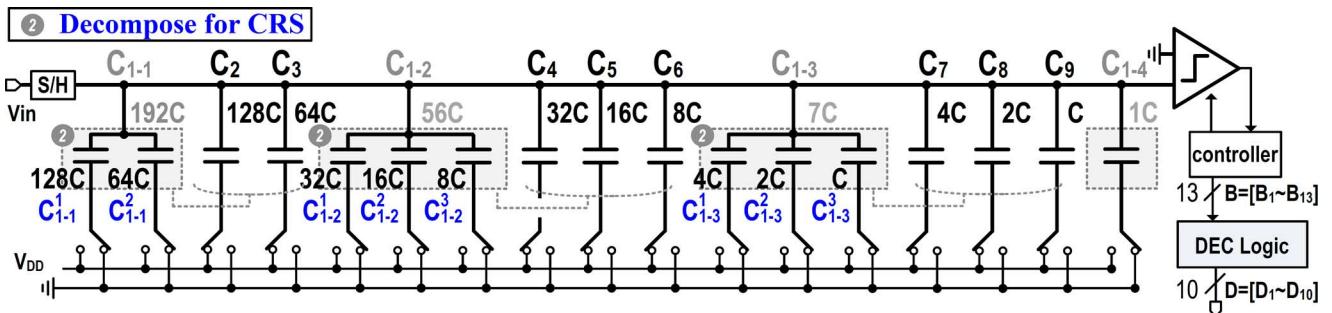


Fig. 8. The final DAC arrangement for both the SC-ADEC and CRS techniques (sampling phase).

errors, static DAC nonlinearity caused by capacitor mismatch remains untackled. Therefore, the CRS technique is proposed to mitigate such static errors. The main idea of the CRS is to compensate for the errors introduced in the preceding bit-cycles by the subsequent DAC switching processes. Instead of always switching new capacitors for each new bit-cycle as in the conventional designs, the CRS tries to reuse the prior switched capacitors, from which the errors (voltage) are induced at the first place, and switches them in a reversed direction to suppress the accumulated error.

Fig. 8 shows the finalized capacitor array in this work. After splitting  $C_{MSB}$  to  $C_{1-1}$ ,  $C_{1-2}$  and  $C_{1-3}$  for redundancy,  $C_{1-1}$ ,  $C_{1-2}$  and  $C_{1-3}$  are further decomposed into sub-capacitors  $C_{1-i}^j$  ( $i, j \in \{1, 2, 3\}$ ) to implement the capacitor reusing for the CRS technique. As indicated by dashed lines, the matched capacitors of same capacitance are paired for reusing (e.g.,  $C_{1-1}^1$  is with  $C_2$  and  $C_{1-1}^2$  is with  $C_3$ ). Fig. 9 illustrates the operations in the first two bit-cycles, and Fig. 9(b) marks the “reusing” events. The MSB capacitor  $C_{1-1}$  comprising of  $C_{1-1}^1$  and  $C_{1-1}^2$  is switched after  $B_1$  is decided. During the second bit-cycle, if  $B_2 = B_1$ ,  $C_2$  of 128 C is switched as shown in the upper- and lower-most switching paths. When  $B_2 \neq B_1$ ,  $C_{1-1}^1$  instead of  $C_2$  is switched as  $C_{1-1}^1$  is able to transfer the same amount of charge as  $C_2$  (both are of 128 C and connected to  $V_{DD}$  after the MSB cycle). The DAC now always tries

to switch used capacitors instead of new ones. Similarly, the switchings of  $C_2 \sim C_9$  can be replaced by the switching of the corresponding decomposed sub-capacitors with the same capacitance and connections when their matched sub-capacitors have switched previously. As illustrated in Fig. 9(c), by reversely switching the previously-switched capacitors, the correlated errors are cancelled *in situ*. A stronger correlation leads to a better compensated result. With such switching method, the ADC shows better linearity, while the number of bit-cycles and the DEC logic remain unchanged.

The theoretical effectiveness of the CRS is summarized in Table III, based on similar calculations in [29], [30]. The  $i$ -th DAC capacitance can be expressed as  $C_i = 2^{N-1-i}C + \delta_i C$ , where  $i$  corresponds to  $i$ -th bit numerated from the MSB,  $i \in [1, N-1]$ ,  $\delta_i$  the mismatch error term assumed independent and identically distributed Gaussian random,  $E[\delta_i] = 0$ ,  $E[\delta_i^2] = 2^{N-1-i}\delta_o^2$ , and  $\delta_o^2$  is the variance for an unit  $C$ . Let  $V_{err}(B)$  be the cumulative error voltage (normalized to 1 LSB) of the DAC for a specific code set  $B$ . Conventionally,  $\sigma_{DNL}^2$  reaches maximum for the half full-scaled code ( $FS/2$ ), i.e.,  $B = 511_{(10)}$  or  $512_{(10)} \equiv FS/2$ . By the definition of DNL, we have  $\sigma_{DNL}^2(FS/2) = E[(0 - V_{err}(FS/2))^2]$ , where  $V_{err}$  depends on the DAC switching scheme, and the zero term is owing to the mismatch-free MSB decision. For the switching scheme in Fig. 9,

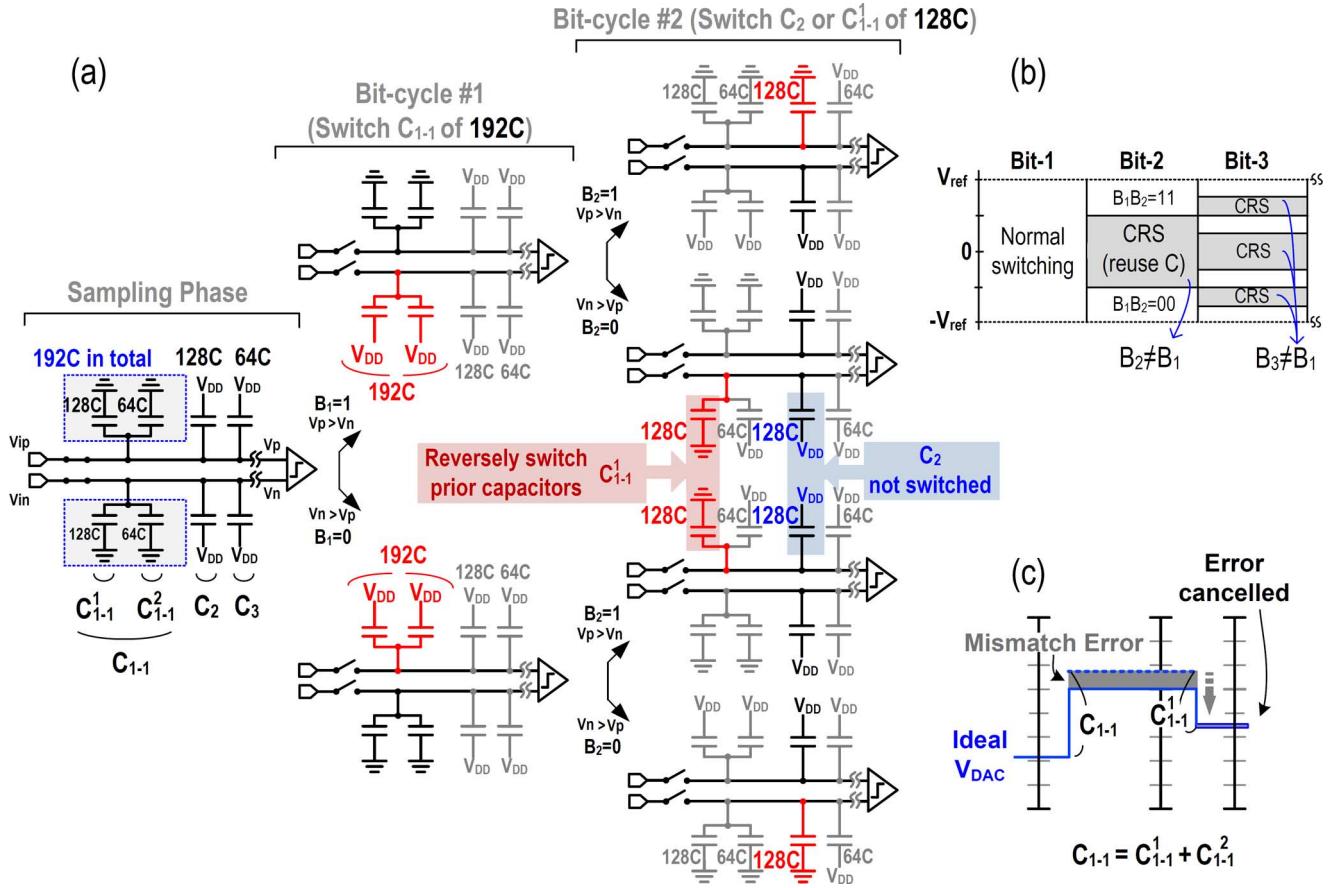


Fig. 9. (a) The first 2 bit-cycles of the 10 bit SAR ADC with the CRS (b) the reusing activities in this work (c) Error suppression mechanism.

TABLE III  
THEORETICAL EFFECTIVENESS OF THE CRS.

Switching type	V <sub>CM</sub> -based		V <sub>ref</sub> (power-rails)-based	
*DAC switching scheme	MCS [31]	MCS [31] + CRS	Monotonic [26] /Bidirectional (see Section II-C )	Monotonic [26] /Bidirectional + CRS
$\sigma(\text{INL}_{\max})$	$\cong \frac{1}{2}\sigma_u\sqrt{2^N}$	$\cong \frac{1}{4}\sigma_u\sqrt{2^N}$	$\cong \frac{1}{2}\sigma_u\sqrt{2^N}$	$\cong \frac{1}{2}\sigma_u\sqrt{2^{N-1}}$ (best-fit INL) $\cong \frac{1}{2}\sigma_u\sqrt{2^N}$ (end-point INL)
$\sigma(\text{DNL}_{\max})$	$\cong \frac{1}{2}\sigma_u\sqrt{2^N}$	$\cong \frac{1}{2}\sigma_u\sqrt{2^{N-1}}$	$\cong \sigma_u\sqrt{2^{N-1}}$	$\cong \frac{1}{2}\sigma_u\sqrt{2^N}$
Var(ENOB)	$\sigma_{enob}^2$	$\cong \frac{1}{2}\sigma_{enob}^2$	$\sigma_{enob}^2$	$\cong \frac{1}{2}\sigma_{enob}^2$
Mean(ENOB)	$M_{enob}$	$\cong M_{enob} + 0.5$	$M_{enob}$	$\cong M_{enob} + 0.1$ †

\* N-bit top-plate-sampling differential SAR ADC.  $\sigma_u^2$  is the variance of the unit capacitor mismatch.

† Results obtained from Monte-Carlo simulations.

$V_{err}(B) = (\overline{B_1}\delta_{1,p} - B_1\delta_{1,n}) + \sum_{i=2}^{N-1} (-B_i\delta_{i,p} + \overline{B_i}\delta_{i,n})$ , where  $B_i \in \{0, 1\}$ . The subscript p/n indicate the error from the p-n-side DAC. According to  $B_i$ , each switched capacitor  $C_{i,p/n}$  brings an error  $\delta_{i,p/n}$ . As for the MCS [31],  $V_{err}(B) = \sum_{i=1}^{N-1} (-1)^{B_i}(\delta_{i,p} + \delta_{i,n})/2$ . Without applying the CRS, all mismatch error  $\delta_{i,p/n}$  fully accumulate to the due error power  $E[V_{err}^2(B)]$ .

In contrast, reusing  $C_i$  (i.e.,  $\bigcup C_i \subseteq C_1 (\forall i > 1)$ ) results in  $\delta_i \subseteq \delta_1$  and  $E[\delta_i\delta_1] = \delta_i^2$ . Then, if  $B_i = \overline{B_1}$ , the  $i$ -th error term ( $\delta_i$ ) directly cancels the correlated error terms contained

in  $\delta_1$  before calculating the  $\sigma_{DNL}^2$ . Similarly, the same story applies to  $\sigma_{INL}^2$  (Appendix). The compensated error profile is illustrated in Fig. 10. The maximum  $\sigma_{INL,\text{best-fit}}^2$  and  $\sigma_{DNL}$  are reduced by a factor of (at least)  $\sqrt{2}$  because the error power is halved by the compensation in the worst case. Hence,  $\sigma_{ENOB}^2$  is also reduced by approximately two times [14]. For the MCS switching [31] (V<sub>CM</sub>-based type classified in Table III), the improvement by employing the CRS is even

<sup>2</sup>Note that the best-fit INL yields the best repeatability, and it serves as a true representation of linearity.

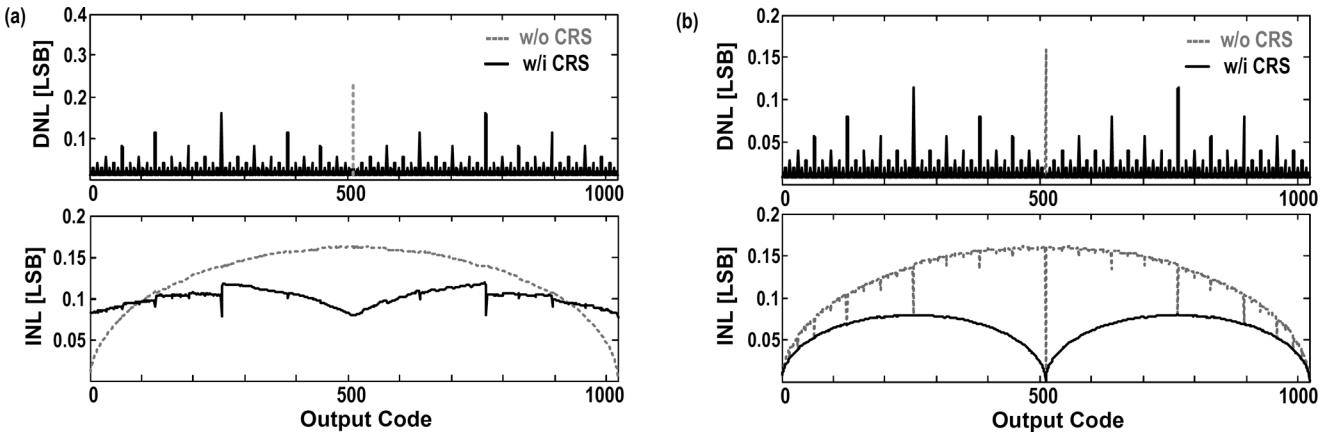


Fig. 10. RMS DNL/INL profiles for (a) Bidirectional switching (Section II-C) (b) MCS switching (1% mismatch).

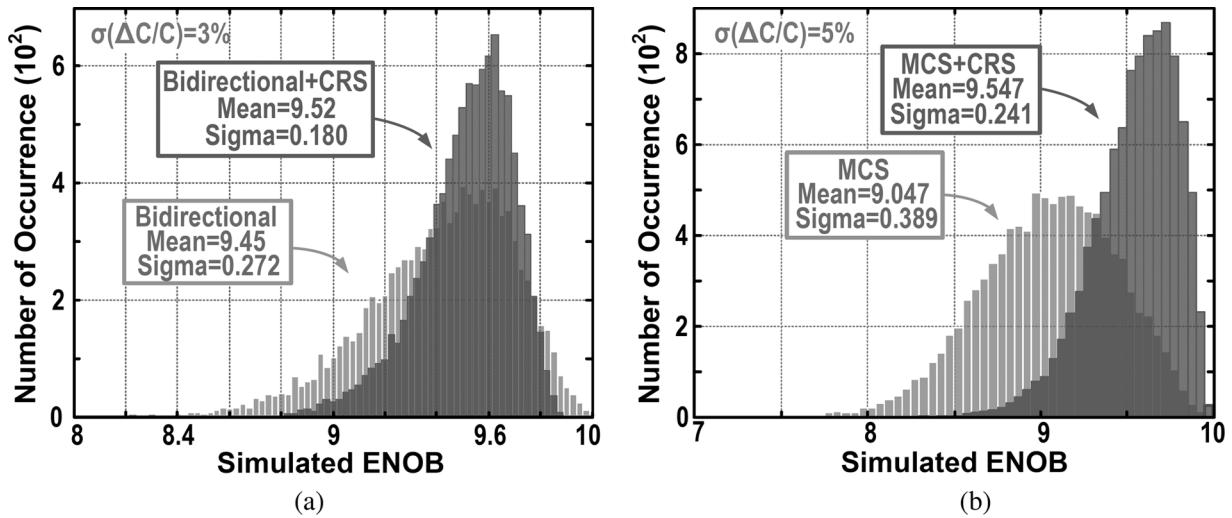


Fig. 11. ENOB histogram with random capacitor mismatch (w/i and w/o enabling CRS). (a) Bidirectional switching (b) MCS switching.

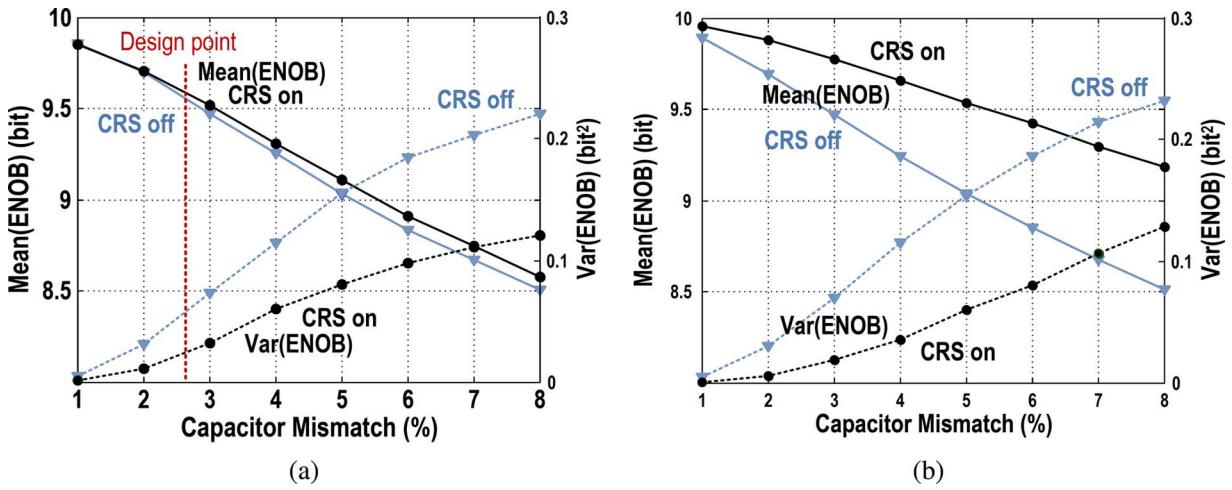


Fig. 12. ENOB improvement by CRS (a) Proposed bidirectional switching (b) MCS switching.

more eminent due to the point symmetry of the reduced INL with respect to the mid-code. Nevertheless, since  $V_{CM}$ -based switchings require an extra reference voltage and compromise the speed seriously, this work employs a bi-directional, power-rails-based DAC switching scheme (Section II-C). In

Figs. 11 and 12, Monte-Carlo simulations show the ENOB improvement as a result of the CRS. Intuitively, INL is reduced because some errors are cancelled rather than accumulated to induce significant non-linearity. This leads to a more linear A-to-D transfer curve statistically. Moreover, although the

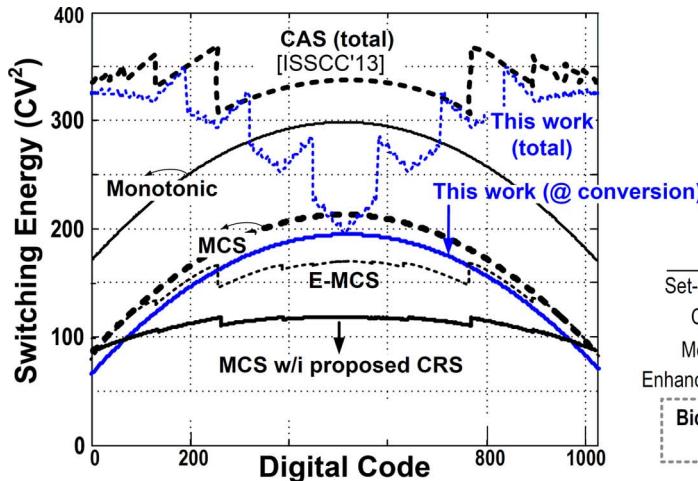


Fig. 13. Comparison of switching energies.

effectiveness of the CRS depends on the actual error profile, the mismatch errors are completely cancelled for the worst mid-code since the fully-reversed DAC switching guarantees that the total net (error-)charge transfer is zero. The dominant mid-code DNLs are thus always suppressed to be nearly zero, ensuring continuity near middle codes as in [32]. This property is especially beneficial for converting small input signals.

The revealed perspectives can also explain the enhanced INLs or DNLs in [29], [30], [32], [33]. Basically, they share the same nature of a reduced amount of total mismatch errors. In conventional designs, a thermometer-coded MSB DAC is often adopted to reduce DNL, as binary-weighted DACs suffer from more severe DNL than INL. However, a coarse sub-ADC might be needed for resolving the MSBs first [33], or the ADC has to switch the same DAC for the MSB binary search. In either case, the MSB DACs have to adjust their switchings to fit the thermometer profile after decoding the binary MSBs. The DAC needs up to 3 bit thermometer MSB and 6 bit binary LSB segmentation to achieve a similar  $DNL_{max}$  as in this work (see Appendix), and the mid-code DNLs still remain non-zero. Additionally, further segmentation is futile for linearity as mismatch errors have already corrupted the MSB decisions. As a result, the CRS always achieves better linearity with less power and area overhead than a thermometer-coded DAC.

### C. Bi-Directional, Rail-to-Rail Switching

As the CRS and the SC-ADEC techniques are generally applicable to various DAC switching schemes, a design freedom is remained to leverage for the best benefit. A wealth of switching schemes have been reported in prior literatures in which the focuses are mostly on lowering the mean switching energy. Fig. 13 compares the energy consumption of several major schemes and the bidirectional rail-to-rail switching proposed in this work. Due to the capacitor reusing in the CRS, the energy at the reset phase is spared code-dependently. As a result, this work dissipates 18% less power than the charge-average switching [3]. In addition, the direct switching between power rails facilitates faster and easier DAC control as in the monotonic switching [26] whose DAC is directly driven by inverters

Switching scheme (differential)	Mean Switching Energy ( $CV_{ref}^2$ )	
	@ Conversion	Total
Set-and-Down(Monotonic Switching)	255.5	255.5
Charge-average Switching (CAS)	88.6	344
Merged-capacitor Switching (MCS)	170	170
Enhanced merged-capacitor Switching (E-MCS)	149	149
Bidirectional switching + CRS (This work)	152	291
MCS + Proposed CRS	116.9	116.9

without the need for voltage-boosted controls in  $V_{CM}$ -involved switchings [3], [31]. Compared to [26], the proposed scheme drains at least 50% smaller peak dynamic current from the reference. It is also notable that, for low-speed operation, the MCS in [31] combined with the CRS is a good alternative to achieve an even lower switching energy and better linearity, as shown by Fig. 13 and Table III. The achieved linearity is (one of) the best among all prior binary switching schemes to the author's knowledge, which potentially yields the smallest DAC area. The Enhanced-MCS [32] reports the same best linearity, but at the cost of complicated control and 27% larger power (Fig. 13) due to non-minimal DAC switching.

In addition, the proposed bidirectional switching scheme lifts the input common mode of the comparator to expedite its decision. This is achieved by switching only the p-side or n-side of the DAC at every cycle. For example, in Fig. 9, if  $B_1 = 1$ , only the p-side  $C_{1-1}$  is switched to  $V_{DD}$ , while the n-side DAC remains unchanged. The common mode is therefore shifted up.

## III. CIRCUIT IMPLEMENTATION

### A. Dynamic Comparator

Fig. 14(a) depicts the proposed dynamic comparator, modified from the one in [34]. A preamplifier cascaded by a latch provides fast decisions. The dynamic preamplifier uses the NMOS input pair to obtain higher transconductance ( $gm$ ) as they dominates 70% of the noise ( $\sigma_n^2$ ). Since the static comparator offset does not degrade the linearity and is easily removable by digital processing, the comparator is optimized for the tradeoff between the speed and noise. Low noise is preferable for LSB accuracy (typically,  $\sigma_n^2 \leq LSB^2/2 \times 12$ ), while high speed is preferable for the MSB decision to avoid the output glitch or latch contention shown in Fig. 14(c). Some design intuitions for the comparator are summarized in Table IV, derived based upon [34], [35].

With redundancy, the comparator needs not to be accurate and fast simultaneously. As the speed and noise of the comparator with a clocked switch tail instead of a current source are dependent on its common-mode input voltage ( $V_{CMI}$ ), which can

TABLE IV  
COMPARATOR DESIGN INTUITION.

Speed (1/T)	Input-referred Noise ( $V_n$ )	Speed $\times$ Accuracy( $V_n^2$ ) $\times$ Energy $^{-1}$
$T = T_{\text{pre-Amp}} + T_{\text{latch}},$ $T_{\text{pre-Amp}} \propto \frac{C_a}{I_1},$ $T_{\text{latch}} \propto \frac{C_L}{gm_{L,\text{eff}}},$	$V_n \propto \left( \sqrt{C_a \left( \frac{gm_1}{I_1} \right)} \right)^{-1}$	$\propto (C_a \cdot gm_1)^{-1}$ (for pre-Amp) $= (C_a \cdot V_{ov1})^{-1}$ when (W/L) is fixed

\*  $C_a$ ,  $I_1$ ,  $gm_1$ ,  $V_{ov1}$ ,  $C_L$  and  $gm_{L,\text{eff}}$  are the capacitive loading on  $M_1$ 's drain, current of  $M_1$ ,  $gm$  of  $M_1$ , overdrive of  $M_1$ , capacitive loading and equivalent  $gm$  of latch, respectively.

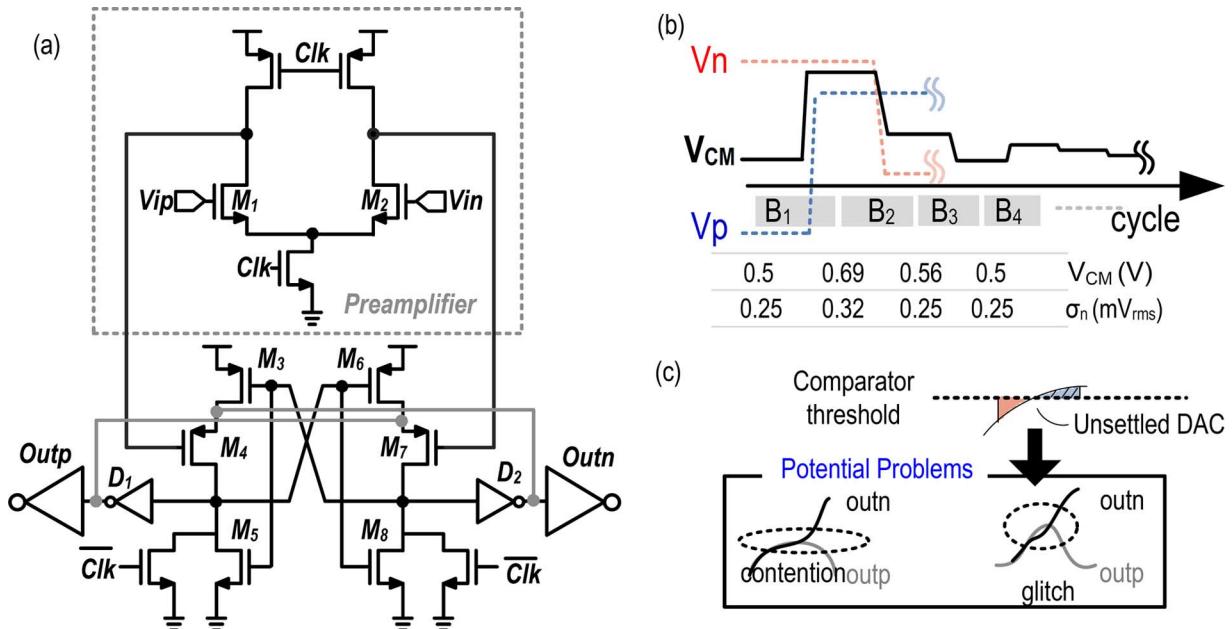


Fig. 14. (a) Schematic of the proposed comparator (b) Comparator transient common-mode levels [TT corner] (c) Latch contention and output glitch due to an unsettled DAC.

be inferred<sup>3</sup> from Table IV, an adaptive biasing scheme is further proposed. During MSB conversions,  $V_{CM1}$  is intentionally lifted by the asymmetric DAC switching to enhance the speed of the comparator by 12% in maximum. The  $V_{CM1}$  then returns to its initial value to minimize the noise during LSB cycles, as summarized in Fig. 14(b). The power consumption of the comparator remains fairly constant at the high-speed biasing as the preamplifier consumes only the same dynamic precharging energy (proportional to the loading capacitor  $C_a$ ). As also revealed in Table IV, adjusting the overdrive of the input pair brings a similar level of tradeoff as compared to adjusting the loading capacitor  $C_a$  [20]. Although the adaptive  $V_{CM1}$  could induce dynamic offsets and extra noise, these non-idealities during MSB decisions can be corrected by the redundancy as MSB decision errors due to an unsettled DAC or noise are indistinguishable<sup>4</sup>. Overall, an extra 80 ps is gained for signal tracking in the worst process corner.

<sup>3</sup>Higher  $V_{CM1}$  results in a faster speed since the dynamic current  $I$  discharging  $C_a$  increases, but a lower average ( $gm/I$ ) ratio of  $M_1$  and  $M_2$ , hence large noise, due to a shorter time the input pair stays in saturation.

<sup>4</sup>A low-noise LSB decision is still required since errors due to unsettled DAC eventually subside whereas noise is restless.

In addition, the comparator in this work contains positive feedback loops with enhanced regeneration strength. In case the main latch consisted of  $M_3$ ~ $M_8$  is metastable, the additional positive feedback, borrowed from the output buffers, from  $D_1/D_2$  to the sources of  $M_4/M_7$  helps to escape the metastability since the equivalent latch  $gm$  for regeneration increases.

#### B. Asynchronous SAR Controller

The ADC is controlled asynchronously [23] to avoid GHz clock generation. The digital controller and its operation (see Fig. 15) is similar to that in [26], except that the adopted DAC controller is actually a differential circuit based on [36], which provides fast speed, common-mode rejection for comparator outputs and reduced metastability. Further in this work, in order to reuse and reversely switch prior capacitors according to the CRS, the corresponding DAC control is immediately reset once the capacitor it driven is detected reusable (by the XOR gates with negligible area and latency). This minimizes circuit switchings (loss) since both the controllers and the DAC are required to reset anyhow before the next conversion in conventional designs.

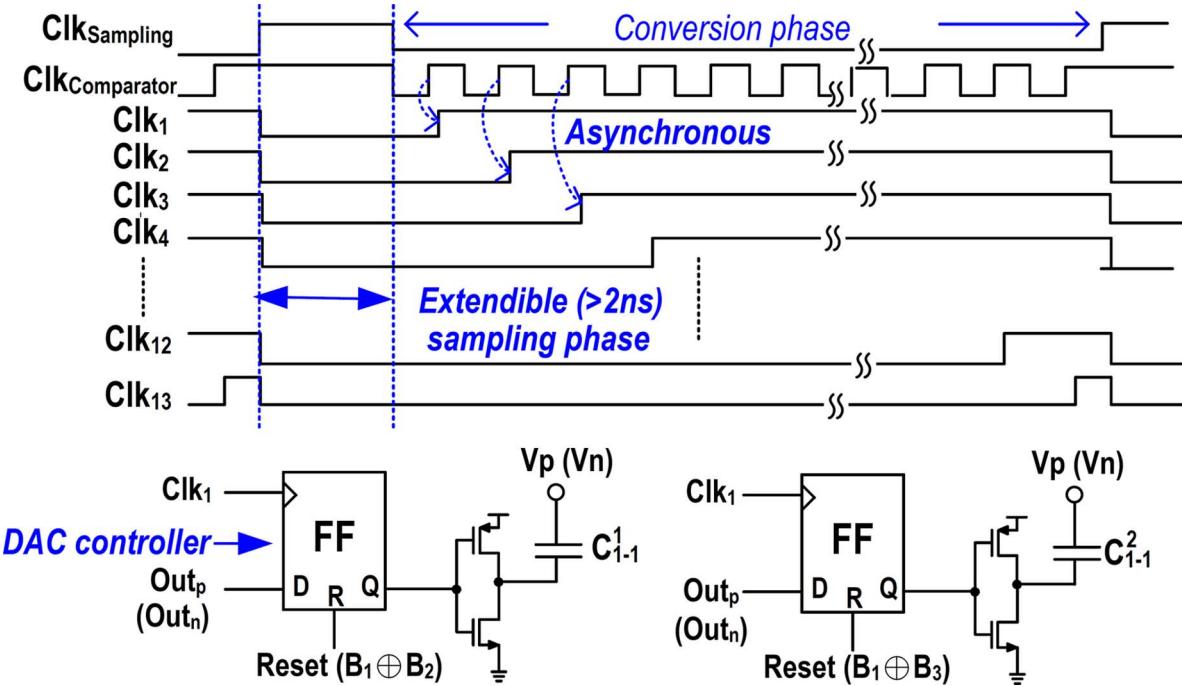


Fig. 15. The asynchronous DAC controller (logic overhead for deactivating CRS not shown).

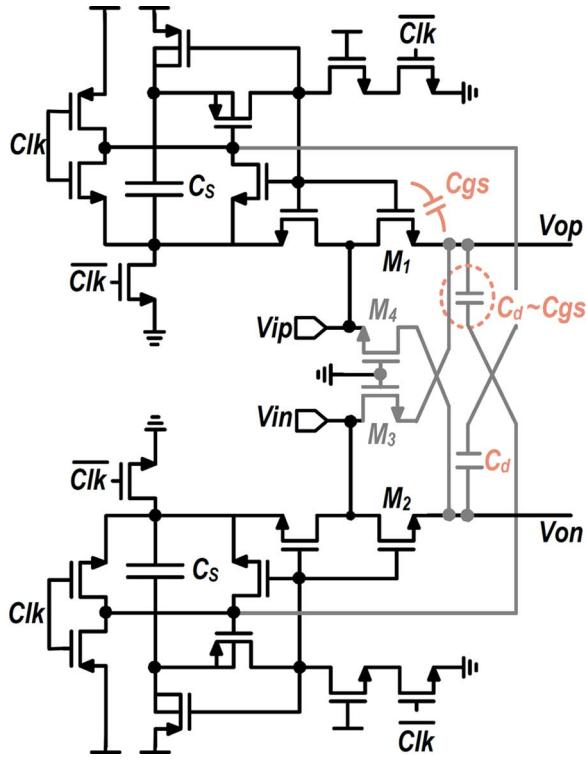


Fig. 16. Schematic of the bootstrapped sampling switches.

### C. Bootstrapped Sampling Switch

Fig. 16 shows the sampling circuit, analogous to that in [37]. The sampling switches ( $M_1, M_2$ ) receive boosted gate voltages to have a nearly constant  $g_{on}$ . Two gate-grounded replica switches ( $M_3, M_4$ ) compensate for high-frequency

couplings from the drains to the sources of  $M_1$  and  $M_2$ . In addition, dummy capacitors ( $C_d$ ) realized by routing parasitics along with replica poly gates adjacent to the sources of  $M_1$  and  $M_2$ , mitigate the signal-dependent charge injection via  $C_{gs}$ . Moreover, the input-tracking time of the ADC is controlled asynchronously by the event-driven manner [1], [38]. As soon as each conversion is complete, the sampling switch turns on to gain extra time for settling, as shown in Fig. 15. This alleviates the required bandwidth and slew-rate for the input buffer, and tolerates the duty cycle distortion of the received ADC clocking.

### D. Capacitive DAC

Fig. 17(a) shows the customized MOM unit capacitor for the DAC. Although minimal metal spacing is preferable for a high capacitance density, a smaller capacitor inevitably exhibits larger random variations due to the augmented line edge roughness effect [39]. An unit capacitor of 0.6 fF is sufficient for an SNR of 60 dB with a full-scaled differential input range of 1.6Vpp in this work, but it would take 1 fF to achieve the target linearity. Nevertheless, by the merit of the CRS, 0.6 fF rather than 1 fF is used. This reduces the power and area of the DAC by 40%, and relaxes the DAC drivers as well. Note that the overheads for splitting and decomposing capacitors in the SC-ADEC and CRS are trivial since all capacitors are realized by an integer amount of unit capacitors. The matching property is also preserved the same as that in the binary-weighted case. The DAC was carefully shielded and checked by 3-D RC extractions to prevent systematic errors, and the CRS technique will compensate for the rest uncontrollable fabrication errors.

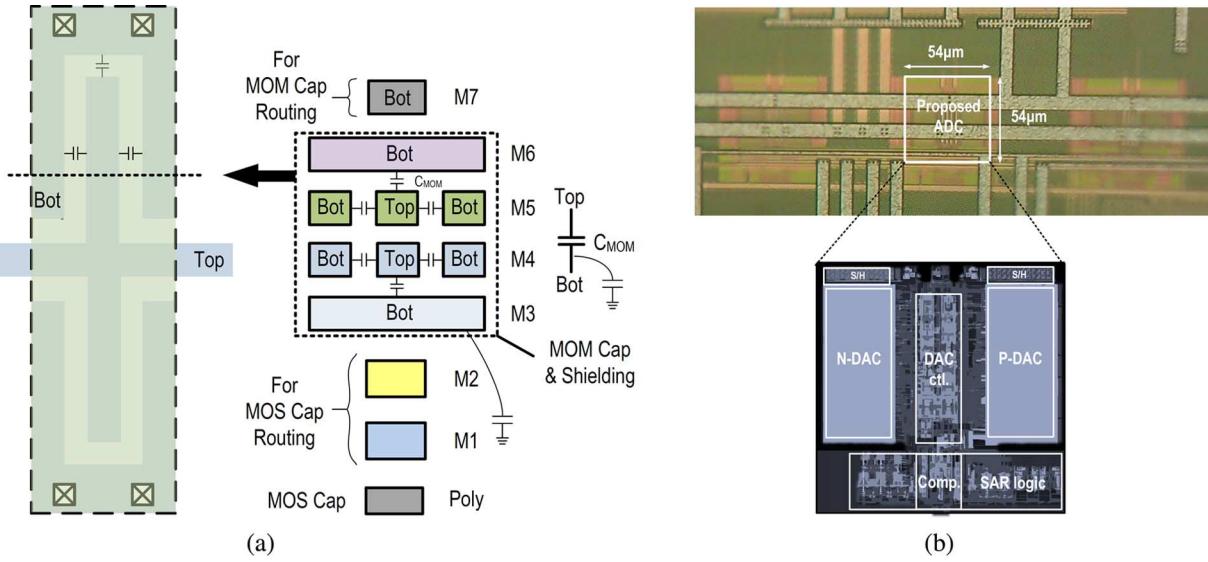


Fig. 17. The layout plan and chip photograph. (a) Aerial and cross-section views of the unit DAC capacitor. (b) The die photograph of the prototype SAR ADC.

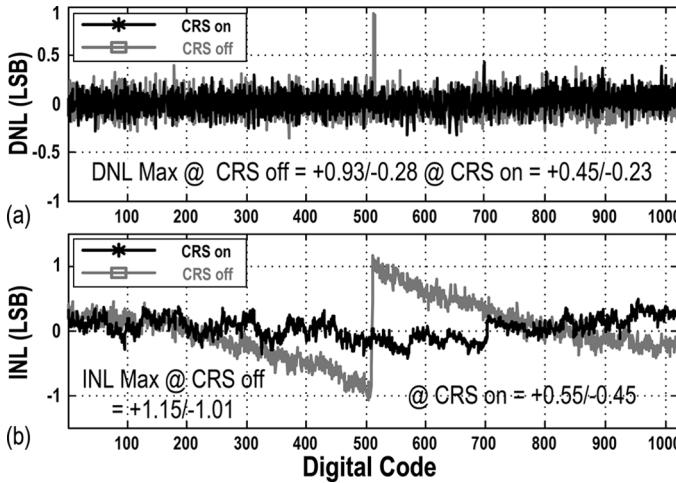


Fig. 18. Measured (a) DNL and (b) INL w/i and w/o enabling CRS.

#### IV. MEASUREMENT RESULTS

Fig. 17(b) shows the ADC fabricated in the UMC 28 nm High-Performance Low Power (HLP) (Poly/SiON) CMOS process<sup>5</sup>. The circuit area including MOS decoupling capacitor of 8.4 pF under the DAC is  $54 \times 54 \mu\text{m}^2$ . The 10 bit ADC operating at 240 MS/s and under an 1 V supply consumes only 0.68 mW, 41% of which is consumed by the comparator, 22% by the DAC and 37% by the controller and the S/H. The reported power and area exclude those of the ADC peripheral circuits. The DEC logic is carried out off-chip in this prototype. It would contribute another 13.2  $\mu\text{W}$  (1.9% of power) and  $33.4 \mu\text{m}^2$  (1% of area) if implemented on chip.

Fig. 18 shows the measured INL and DNL. The CRS improves the INL and DNL by more than one LSB and 0.5 LSB,

<sup>5</sup>Not the High Performance for Mobile (HPM) process with high-K metal gates and faster speed.

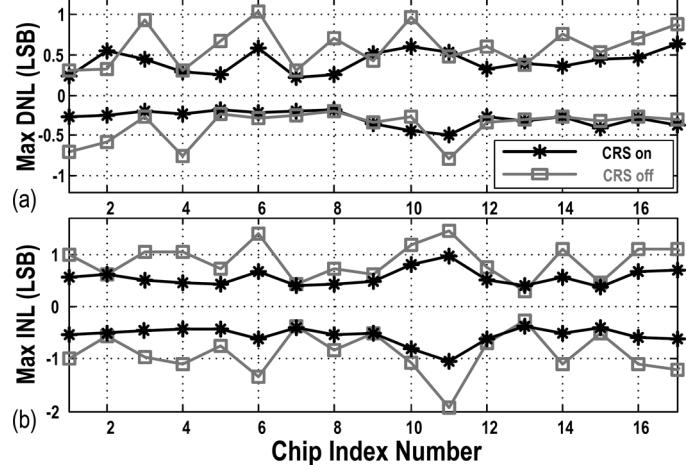


Fig. 19. Measured (a) DNL and (b) INL with and without enabling the CRS technique.

respectively<sup>6</sup>. The originally dominant mid-code DNL is suppressed to near zero as expected. To verify that the mismatch compensation is effective, the maximum DNLs/INLs of 17 chips are measured and shown in Fig. 19. Although chips #6, #11, and #14 suffer from relatively poorer linearity, the improvement introduced by CRS is more evident for these chips. This property enhances the yield of ADCs. The worst standard deviations of INL/DNL are reduced by 85% and 68%, respectively, by activating the CRS. Moreover, Fig. 20 reveals the mid-code DNLs for the 17 chips are all suppressed from  $[+1.1, -0.95]$  to well below  $\pm 0.1$  LSB. Good linearity is thus preserved even for smaller inputs ( $> 68$  dB SFDR at a  $-10$  dBFS input). The INLs of all ADCs are all smaller than  $\pm 1$  after the mismatch compensation. The SNDR becomes

<sup>6</sup>Extra AND gates are added before the reset signal to disable or enable the CRS (not shown in Fig. 15), just for the testing purpose. When the CRS is deactivated, the DAC is reconfigured as that in Fig. 3 to allow a sequential switching without reusing.

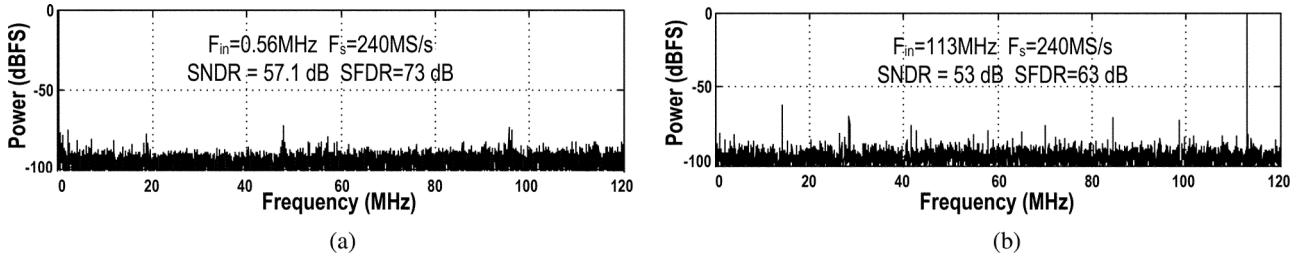


Fig. 21. The output spectrum. (a) At a low-frequency input (b) At a near-Nyquist input.

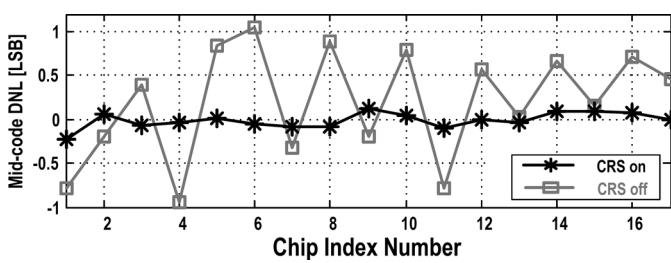


Fig. 20. Measured mid-code DNLs w/i and w/o enabling CRS.

limited by the noise rather than the capacitor mismatch. The maximum SNDRs at 50 MS/s and 240 MS/s are 58 dB and 57.1 dB, respectively, as shown in Fig. 21(a). The SNDR degrades to 53 dB at the Nyquist frequency, as shown by Fig. 21(b). The SNDRs and SFDRs at 240 MS/s and 50 MS/s for input signals with different frequencies are measured and shown in Fig. 22. The SFDR is 73 dB at low input frequencies, and 63 dB at the Nyquist input. With the CRS, the low-frequency SFDR is improved by about 7 dB.

Compared to the with state-of-the-art ADCs with a similar resolution and a comparable speed [5]–[8], [11], [12], [25], [40], [41], the proposed ADC consumes at least 80% less area and 32% less power as indicated by Table V. Other ADCs with comparable speed employ either pipelined architecture or multiple comparators, thus costing more power and area. To further compare the performance in terms of energy efficiency, both Walden FOM ( $\text{FOM}_W$ ) and Schreier FOM ( $\text{FOM}_S$ ) [42] are plotted versus speed in Figs. 1 and 23(a), respectively, for all state-of-the-art SAR ADCs [42]. Fig. 1 reveals that the presented ADC achieves the best energy efficiency of 7.8 fJ/c.-s. as compared to all SAR ADCs with a bandwidth greater than 2 MHz. The improvement is even more pronounced as compared to other single-channel SAR ADCs. Fig. 23(a) further shows that the proposed ADC achieves an  $\text{FOM}_S$  of 165.4 dB. For broadband converters whose performance at the Nyquist frequency is not crucial for applications with an OSR greater than one (e.g., serial links), the ENOBs for lower-frequency inputs are compared. In this context, the proposed ADC reports an  $\text{FOM}_W$  of 4.8 fJ/c.-s. and an  $\text{FOM}_S$  of 169.6 dB. Finally, Fig. 23(b) compares the normalized areas versus speed for SAR ADCs with a resolution of 5~12 bits. SAR-related architectures are singled out as they generally exhibit smaller areas than the pipeline counterparts. This SAR ADC achieves a higher speed

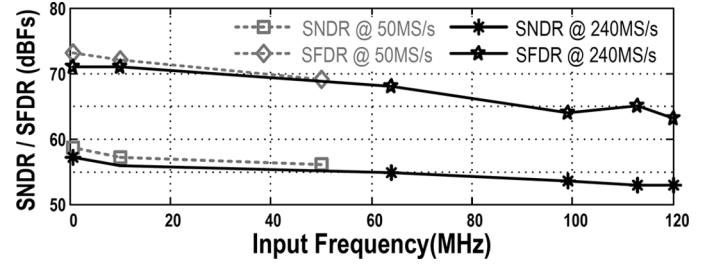


Fig. 22. The measured SNDR/SFDR vs. input frequencies at 50 MS/s and 240 MS/s.

and a better resolution with comparable area efficiency. It survives well in the 28 nm CMOS process node of a low intrinsic device gain.

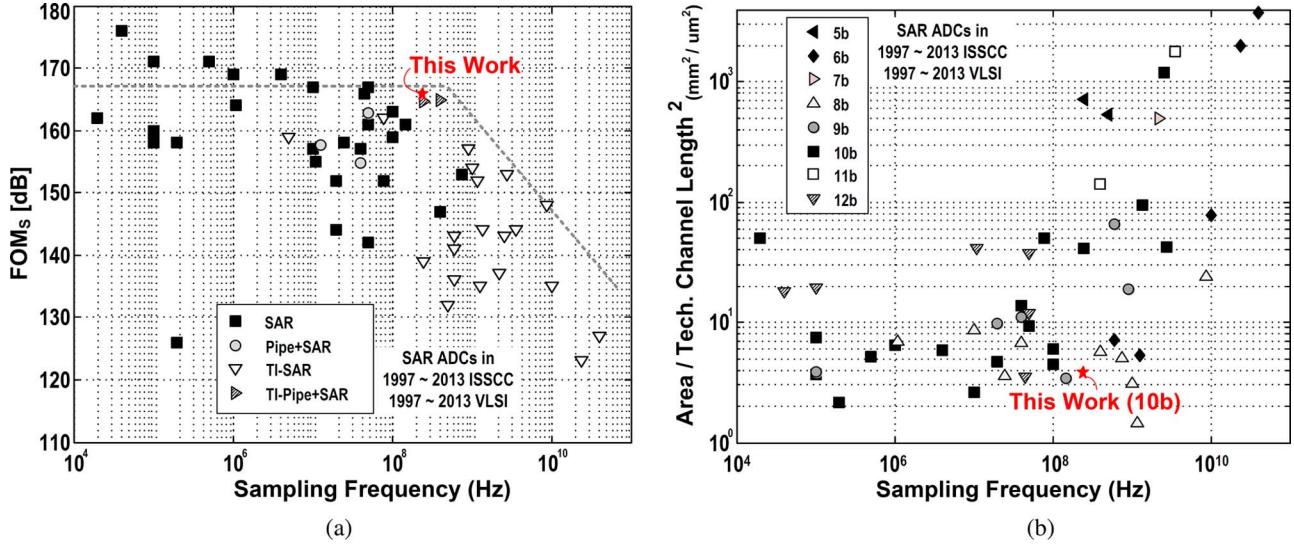
## V. CONCLUSION

This paper presents a single-channel, calibration-free 10 bit 240MS/s SAR ADC. The proposed DAC switching method suppresses static DAC non-idealities, such that the unit capacitor is noise-bounded and a minimal circuit circuit area is achieved. In addition, an efficient redundancy generation method via splitting the MSB capacitor is presented. Bit errors are tolerable within a certain bound, while the total DAC capacitors remain unchanged. Systematic design guidelines catering to various optimization goals are also discussed. The proposed ADC is energy- and area-efficient than most contemporary ADCs and have a low input capacitive load. It offers a promising choice for low-cost data conversion or interleaving to a higher speed.

## APPENDIX

### Speed Optimization and the Precise Redundancy Equations:

For an  $N$  bit conventional SAR ADC, the DAC settling time  $t_{DAC}$  is bounded by  $N\tau_{DAC} \ln 2$ , where  $\tau_{DAC}$  is the time constant of the DAC. Similarly, with a redundancy of  $2^{-x}$ ,  $t_{DAC} = x\tau_{DAC} \ln 2$ , and the added extra cycle  $N_{excess} = \lceil (N-2)/x \rceil$  as derived in Section II-A. To optimize speed, assume  $T_{cmp}$  is the time penalty for an extra cycle, and define a parameter  $\rho = T_{cmp}/\tau_{DAC} \ln 2$  for simplicity. The total conversion time is expressed as  $T_{tot} = (N + N_{excess} - 1)t_{DAC} + (N + N_{excess})T_{cmp} \approx (x + \rho) \cdot (N + (N-2)/x)\tau_{DAC} \ln 2$ . Let

Fig. 23. SAR ADCs from ISSCC/VLSI 1997–2013. (a) Performance comparison of  $FOM_S$ . (b) Normalized area vs. speed.TABLE V  
PERFORMANCE SUMMARY AND COMPARISON

Reference	Architecture	Tech. (nm)	Bits (bit)	Peak SNDR (dB)	Sampling Rate (MS/s)	Channel Sampling Rate( MS/s)	Power (mW)	Power /Fs (pJ/con- version)	Nyquist FoM (fJ/con- step)	Area (mm <sup>2</sup> )	Cal- ibration
[43] VLSI'11 T.Miki	Pipe	40	11	56.0	300		40.00	133	258.6	0.42	yes
[44] VLSI'11 M. Miyahara		90	10	50.0	320		40.00	125	483.8	0.46	-
[25] ISSCC'12 Y. Chai		65	10	57.0	200		5.37	27	46.4	0.19	-
[5] CICC'12 Si-Seng Wong	BS.+2X-Ti SAR	65	10	54.6	170	85	2.30	14	36.4	0.104	yes
[6] ASSCC'12 Jianyu Zhong	SAR+2X-Ti Pipe+SAR	65	10	55.7	470	235	7.40	16	31.5	0.049	yes
[7] VLSI'12 Yan Zhu		65	10	55.4	500	250	8.20	16	34.0	0.046	yes
[8] ASSCC'11 Yan Zhu	2X-Ti Pipe+SAR	65	10	55.4	160	80	2.72	17	35.0	0.21	yes
[9] ISSCC'12 B. Verbruggen		40	11	56.0	250	125	1.70	7	13.2	0.066	yes
[10] VLSI'13 B. Verbruggen		28	11	60.0	410	205	2.14	5	11.4	0.11	yes
[11] ISSCC'13 H-K Hong	2X-Ti SAR (3 comparators)	45	9	53.7	900	450	10.80	12	40.5	0.038	yes
[12] CICC'12 R. Vitek	SAR (2 comparators)	65	10	51.7	220		4.30	20	63.0	0.015	-
This work	SAR (1 comparator)	28	10	57.1	240		0.68	3	7.8	0.003	-

$\partial T_{tot}/\partial x = 0$ , then  $x = \sqrt{\rho(N-2)/N}$ . Hence, a redundancy of  $2^{-\lceil \sqrt{\rho(N-2)/N} \rceil}$ . 100% maximizes the speed.

With redundancy, the tolerable settling error  $E_{tol}(i) = [\sum_{j=M-1}^{i-1} C_j - C_{i+1} + (1+\varepsilon)C]/C_i \times 100\%_{(i+1 < M-1)}$ , for  $i$ -th cycle, where  $C_i$  is the capacitance switched in the  $i$ -th cycle, and  $\varepsilon$  equals 0.5 for DNL =  $\pm 0.5$  LSB. The equation is self-explained by revisiting Fig. 57, and  $t_{DAC}$  can be rewritten

<sup>7</sup>When the voltage shift due to  $C_i$  fails to settle in time,  $B_{i+1}$  is erroneous.  $C_{i+1}$  then switches incorrectly. The rest capacitors  $C_{j(j \geq i+2)}$  will try to compensate for such error. The extra  $(1+\varepsilon)C$  term accounts for a settling-error-free LSB step and the DNL.

to  $-\tau_{DAC} \ln[E_{tol}(i)]$ . Values reported in Fig. 7 and Table II are calculated by the above equations.

#### INL Reduction by the CRS:

Traditionally, the worst (end-point) INL is estimated by

$$\sigma_{INL}^2(FS/2) = E[((V_{err}(0) + V_{err}(FS))/2 - V_{err}(FS/2))^2]$$

. (Equations in [30] are not all correct.) The CRS ensures that  $V_{err}(FS/2) = 0$ . For the MCS combined with the CRS,  $\sigma_{INL}^2(FS/2) = E[(0/2 - 0)^2]$ . The 0/2-term is due to the point-symmetry nature of the MCS, while the second nulled

Requirement (DAC)	Thermometer-coded	Segmented	Binary-weighted
$\sigma_{INL,max}$		$\frac{1}{2}\sigma_u\sqrt{2^N}$	
$\sigma_{DNL,max}$	$\sigma_u$	$\sigma_u\sqrt{2^{B_b}+1}-1$	$\sigma_u\sqrt{2^N}-1$
Number of switched elements	$2^N - 1$	$B_b + 2^{B_T} - 1$	$N$

Assume an  $N$ -bit DAC is segmented into  $B_T$ -bit thermometer coded MSB part and  $B_b$ -bit binary LSB part ( $N=B_b+B_T$ ).

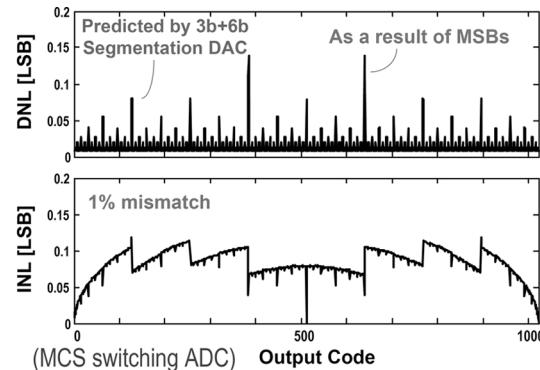


Fig. 24. INL and DNL profiles of segmented DAC.

term is as the result of the CRS. The  $\sigma_{INL,max}^2$  shifts from  $FS/2$  to  $FS/4$  and  $3FS/4$ . All calculated results are summarized in Table III.

### Segmented DAC:

The INL/DNLs of an  $N$  bit segmented DAC are summarized in Fig. 24. For an  $N$  bit top-sampling differential SAR ADC, an  $(N-1)$  bit DAC is used. The achieved INL/DNL profiles of the MCS scheme with a 3b + 6b segmented DAC are also shown below (MCS gains extra DNL reduction by nature). Note that the obtained INL/DNLs are worse than that applying the CRS as the segmented MSB DACs still respond to the binary MSBs contaminated by the mismatch.

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**Jen-Huan Tsai** received the B.S., M.S and Ph.D. degree from Electrical Engineering of National Tsing Hua University, Taiwan in 2009, 2010, 2014 respectively.

Since 2014, he has been an Engineer in Mediatek HsinChu Taiwan, where he has been engaged in research and development of wireless communication systems. His research interests include analog and mixed-signal integrated circuits design. He was the recipient of the Novatek fellowship in 2013, and won the distinguished design award in ASSCC 2014.



**Hui-Huan Wang** was born in Tainan, Taiwan, R.O.C., in 1990. He received the B.S degrees from Electrical Engineering Department of National Tsin-Hua University, Hsinchu, Taiwan in 2012, where he is currently working toward the M.S degree. His current research interest is high-resolution analog-to-digital converter.



**Yang-Chi Yen** was born in Hsinchu, Taiwan, R.O.C., in 1989. He received the B.S degrees from Electrical Engineering Department of National Tsin-Hua University, Hsinchu, Taiwan in 2012, where he is currently working toward the M.S degree. His current research interests are analog circuit and MEMS sensor design.



**Chang-Ming Lai** received the B.S., M.S and Ph.D. degree from Electrical Engineering of National Tsing Hua University, Taiwan in 2003, 2005, 2013 respectively.

Since 2013, he has been an Engineer in Mediatek HsinChu Taiwan, where he has been engaged in research and development of wireless communication systems. His research interests include CMOS RF, analog and mixed-signal integrated circuits design.



**Yen-Ju Chen** received the B.S. degree in Electrical Engineering from the National Tsing Hua University, Hsinchu, Taiwan, in 2010. She is currently working toward the Ph.D. degree at the Department of Electrical Engineering at the National Tsing Hua University, Hsinchu, Taiwan. Her research interest is mainly focused on the silicon-based RF, mixed-mode integrated circuit (PLL/ADC) and system design.



**Po-Chiun Huang** received the B.S. and Ph.D. degrees in electrical engineering from National Central University, Hsinchu, Taiwan, in 1992 and 1998, respectively. During the summers of 1992 and 1996, he was an Intern with the Computer and Communication Research Laboratory, ITRI, and Lucent Technology, during which time he investigated design techniques for optical and RF communication systems. From 2000 to 2002, he was with MediaTek Inc., where he was involved with chipset design for optical storage products. In 2002, he joined National

Tsing Hua University, Hsinchu, Taiwan.



**Ping-Hsuan Hsieh** was born in Taipei, Taiwan. She received the B.S. degree from National Taiwan University, Taipei, Taiwan, in 2001, and the M.S. and Ph.D. degrees from the University of California, Los Angeles, in 2004 and 2009, respectively, all in electrical engineering. She was an Intern with Texas Instruments, Dallas, TX, in the summers 2004–2006. From 2009 to 2011, she was with the IBM T.J. Watson Research Center, Yorktown Heights, NY, where she worked on the design of mixed-signal integrated circuits for high-speed serial data communication. In 2011, she joined the Electrical Engineering Department of National Tsing Hua University, Hsinchu, Taiwan, where she is currently an Assistant Professor. Her research interests focus on mixed-signal integrated circuit designs for high-speed electrical data communications, clocking and synchronization systems, and energy-harvesting systems for wireless sensor networks and machine-to-machine applications.



**Hsin Chen** was born in 1974 in Taiwan. He received the B.S. and M.S. degrees in electrical engineering in 1996 and 1998, respectively, from National Tsing-Hwa University (NTHU), Taiwan. After obligating two years' military service in the Taiwan Air Force, he received the Ph.D. degree in electronics in 2004 from Edinburgh University, Edinburgh, U.K. Since then, he was appointed Assistant Professor with the Department of Electrical Engineering, NTHU. His electrical engineering expertise lies in analog- and mixed-mode VLSI design.



**Chao-Cheng Lee** received the B.S. degree from National Chiao-Tung University in 1988 in electrical engineering. He received the M.S. degree from National Taiwan University in 1990 in physics. He joined Realtek Semiconductor in 1992 and is currently the Senior Vice President of Engineering in Realtek. His research interests includes PLL, filter, high speed ADC/DAC, Serdes, and mismatch calibration. He has more than 30 U.S. patents granted or pending. He is the winner of 18th Industrial Technology Advancement Award, Taiwan.