

# FRIDA Design Review

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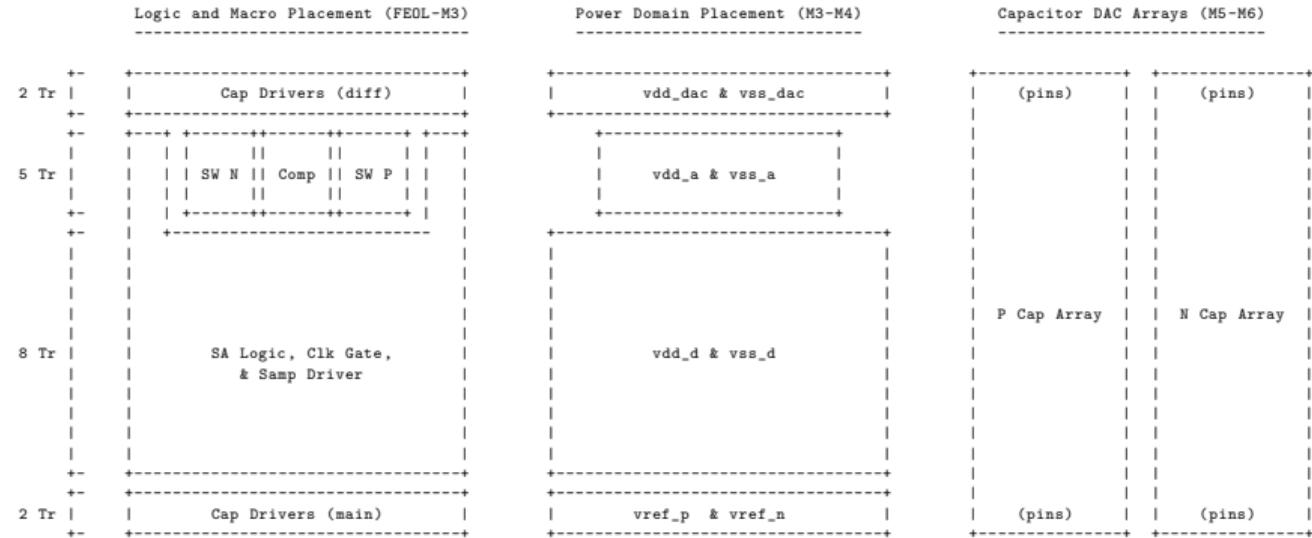
Wednesday, 28 January 2026

# ADC Target Specifications

Parameter	CD v1	CoRDIA	M	H	F (target)
Resolution	8-bit	10-bit	8-bit	10-bit	12-bit
ENOB	8.3	8.8	8.0	9.5?	11.0?
Conversion rate	6.25 MHz	2.5 MHz	4.5 MHz	10 MHz	10 MHz
ADC dimensions	$40 \times 55 \mu\text{m}$	$80 \times 330 \mu\text{m}$	$60 \times 800 \mu\text{m}$	$15 \times 100 \mu\text{m}$	$50 \times 50 \mu\text{m}$
ADC area	$0.002 \text{ mm}^2$	$0.026 \text{ mm}^2$	$0.048 \text{ mm}^2$	$0.0015 \text{ mm}^2$	$0.0025 \text{ mm}^2$
Power per ADC	$960 \mu\text{W}$	$30 \mu\text{W}$	$700 \mu\text{W}$	$100 \mu\text{W}$	$200 \mu\text{W?}$
$\text{FOM}_{\text{csa}} (\text{Hz}/\mu\text{m}^2)$	3125	95	105	5000	5000
$\text{FOM}_{\text{wal}} (\text{fJ}/\text{conv-step})$	487	26	608	14	10

- ▶  $F$  = FRIDA target: 12-bit, 10 MHz,  $50 \times 50 \mu\text{m}$  footprint
- ▶  $\text{FOM}_{\text{csa}}$  = conversion rate / area;  $\text{FOM}_{\text{wal}}$  = energy per conversion step

# Sketch of ADC Floorplan



# Unit Fringe Capacitor

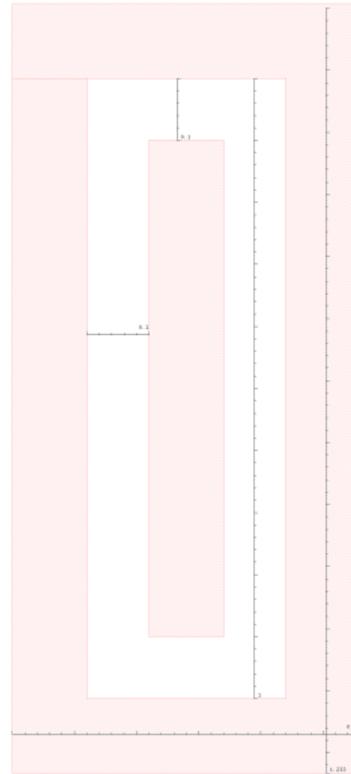
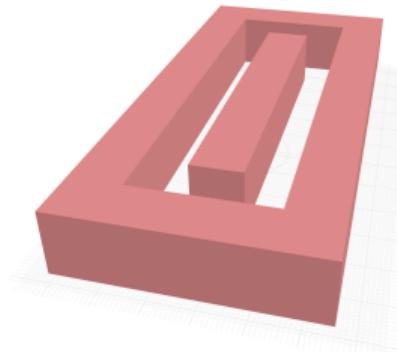
1 layer:  $0.31 \text{ fF}/\mu\text{m}^2$

2 layers:  $0.62 \text{ fF}/\mu\text{m}^2$

3 layers:  $0.93 \text{ fF}/\mu\text{m}^2$

Matching coefficient:

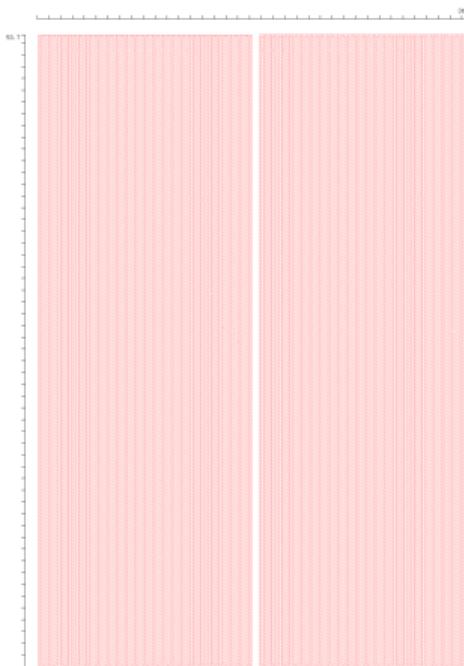
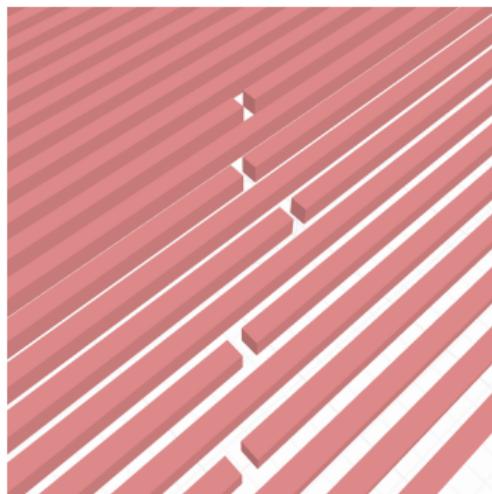
$$\sigma(\Delta C/C) = 0.85\% \times \sqrt{C \text{ [fF]}}$$



# CDAC Array Overview

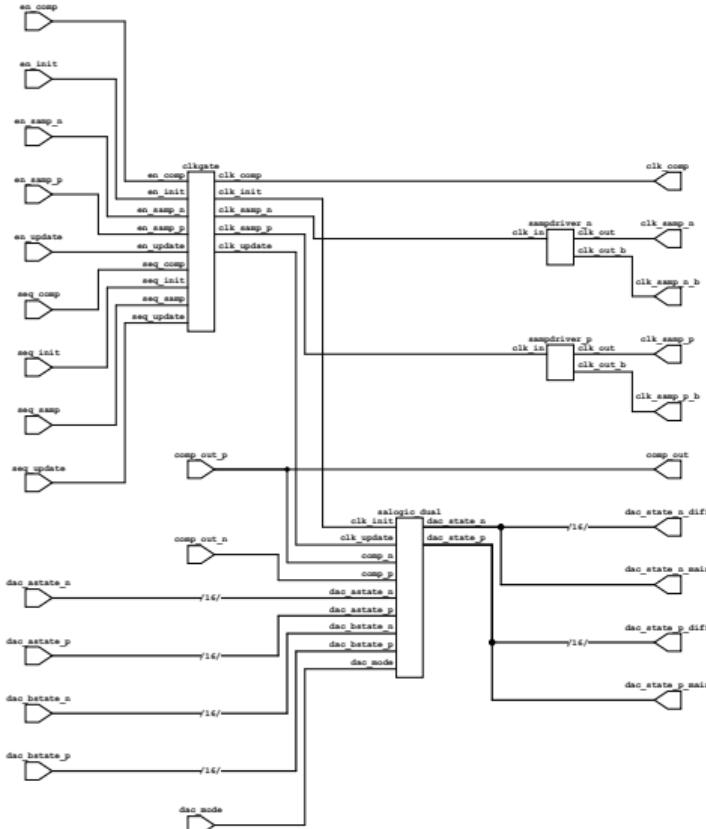
Total Area =  $1940 \mu\text{m}^2$

$$C_{\text{tot}} = 1.4 \text{ pF}$$



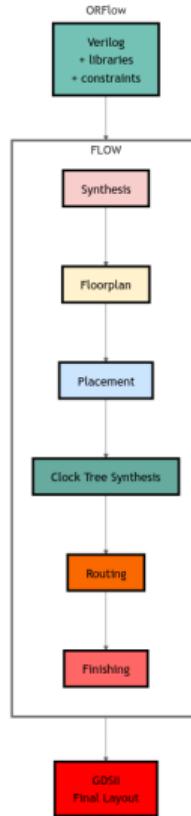
# ADC Digital Block Netlist

- ▶ **salogic**: SAR sequencing FSM
- ▶ **clkgate**: Clock gating for power
- ▶ **sampdriver\_p/n**: Sampling switch drivers
- ▶ Symmetric P/N halves for differential operation
- ▶ salogic and clkgate shared between halves



# OpenROAD Flow Scripts (ORFS)

- ▶ **Yosys:** RTL synthesis
  - ▶ Verilog parsing and elaboration
  - ▶ Logic optimization (ABC)
  - ▶ Technology mapping to standard cells
- ▶ **OpenROAD:** Physical design
  - ▶ Floorplanning and PDN
  - ▶ Placement (global + detailed)
  - ▶ Clock tree synthesis
  - ▶ Routing (global + detailed)
  - ▶ Timing analysis (OpenSTA)
- ▶ **KLayout:** Final verification
  - ▶ DRC and LVS checks
  - ▶ GDS export



# Yosys: Step 1 - RTL Synthesis

## Input Files

- ▶ adc\_digital.v (top module)
- ▶ clkgate.v, salogic.v, sampdriver.v
- ▶ cells\_tsmc65.v (cell wrappers)

## Synthesis Statistics

- ▶ Total cells: 350
- ▶ Total area: 893.88  $\mu\text{m}^2$
- ▶ Sequential elements: 49.6% of area
- ▶ 48 flip-flops (DFQD1, EDFD2)
- ▶ 5 clock gates (CKLNQD1LVT)

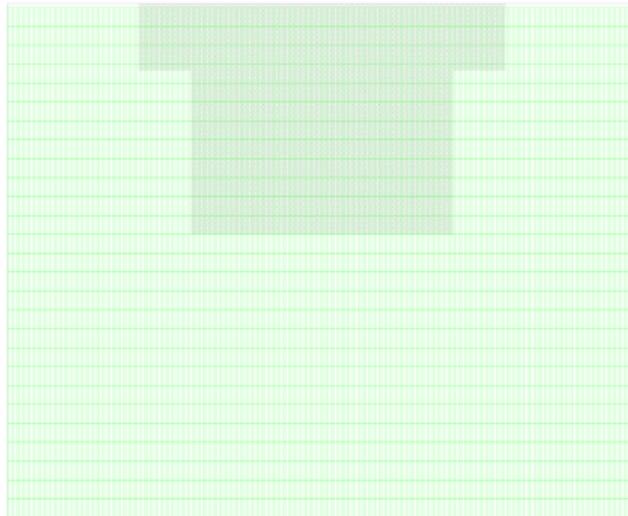
## Technology Mapping (ABC)

Module	Cells	Area
-----		
adc_digital	38	54.36
clkgate	6	33.48
salogic	302	798.84
sampdriver	2	3.60
-----		
Total	350	893.88

## Key Cell Types

EDFD2LVT (edge DFF)	32	334.08
DFQD1LVT (DFF)	16	109.44
NR2D0LVT (NOR2)	93	133.92
BUFFD0LVT (buffer)	69	99.36
CKLNQD1LVT (clkgate)	5	32.40

# OpenROAD Step 2.1: Floorplan



- ▶ Die and core area:  $60\mu\text{m} \times 49\mu\text{m}$
- ▶ Row height:  $2.8\mu\text{m}$  (17 rows)
- ▶ Blockages reserve space for analog macros
- ▶ Custom I/O pin placement for DAC interface

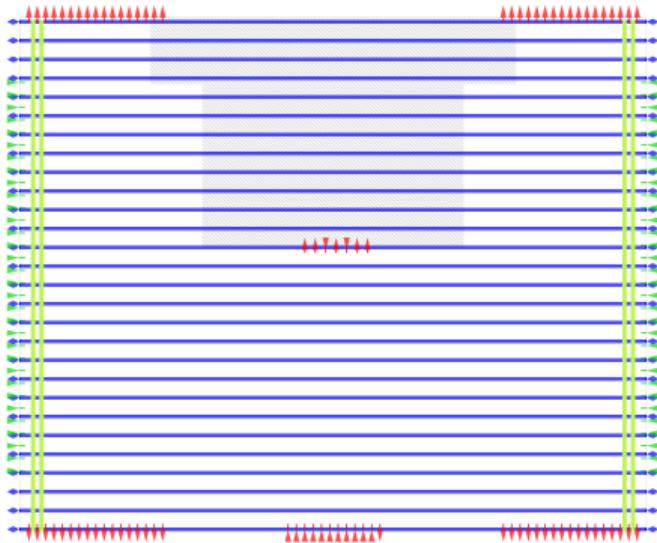
## config.mk

```
export DIE_AREA = 0 0 60 49
export CORE_AREA = 0 0 60 49
export CREATE_BLOCKAGES = .../create_blockages.tcl
```

## create\_blockages.tcl

```
# Reserve area for comparator
create_blockage -region {17.5 27.0 42.5 49}
# Reserve areas for sampling switches
create_blockage -region {12.5 42.6 21 49}
create_blockage -region {39 42.6 47.5 49}
```

# OpenROAD Step 2.2: Power Distribution Network



- ▶ M4 vertical stripes at edges for vdd\_d/vss\_d
- ▶ M1 horizontal stripes follow standard cell rows
- ▶ M1-M4 connections for power delivery

## pdn.tcl

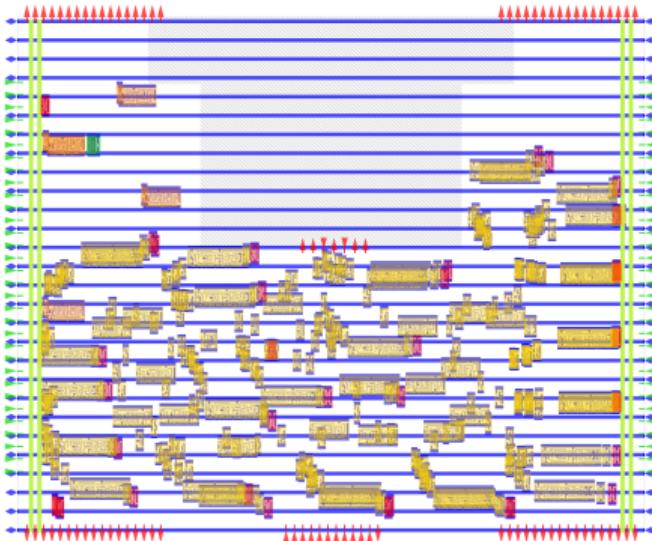
```
add_global_connection -net {vdd_d} \
    -inst_pattern {*} -pin_pattern VDD -power
add_global_connection -net {vss_d} \
    -inst_pattern {*} -pin_pattern VSS -ground

define_pdn_grid -name "Core" -pins {M4}

add_pdn_stripe -grid "Core" -layer M4 \
    -width 0.4 -offset 1.3 -nets {vdd_d}
add_pdn_stripe -grid "Core" -layer M4 \
    -width 0.4 -offset 2.1 -nets {vss_d}

add_pdn_stripe -grid "Core" -layer M1 \
    -followpins -width 0.33
add_pdn_connect -grid "Core" -layers {M1 M4}
```

# OpenROAD Step 3.1: Global Placement (Skip I/O)



- ▶ Initial cell spreading before I/O placement
- ▶ Routability-driven placement disabled (OpenROAD bug)
- ▶ 50% target placement density

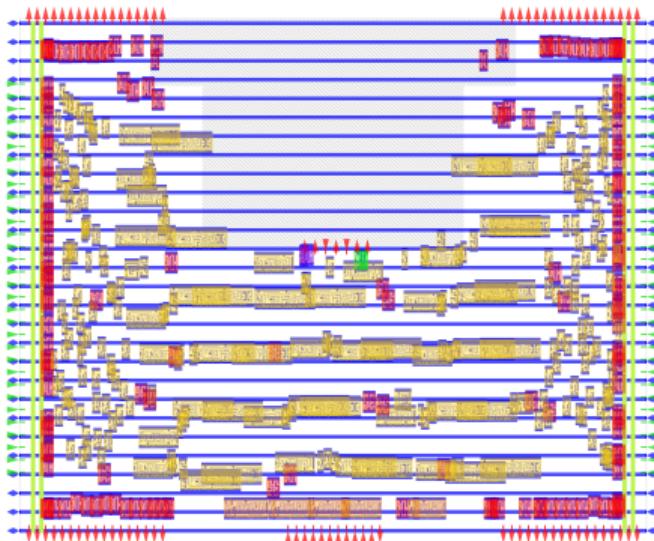
## config.mk

```
# Disable routability-driven placement
# due to OpenROAD crash in cutFillerCells()
export GPL_ROUTABILITY_DRIVEN = 0

# Standard cell placement density
export PLACE_DENSITY = 0.50

# I/O pin layers
export IO_PLACER_H = M3
export IO_PLACER_V = M2
```

# OpenROAD Step 3.2: Global Placement



- ▶ I/O pins now placed on die boundary
- ▶ DAC pins on left/right edges (M3),  $2.8\mu\text{m}$  spacing
- ▶ Control signals on bottom (M2)

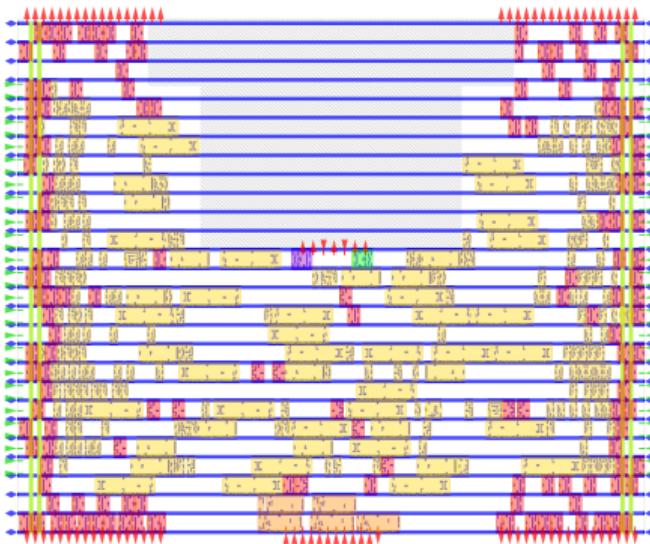
## io.tcl

```
# Left side - DAC astate positive pins
place_pin -pin_name dac_astate_p[0] \
    -layer M3 -location {0.0 5.6} \
    -force_to_die_boundary

# Right side - DAC astate negative pins
place_pin -pin_name dac_astate_n[0] \
    -layer M3 -location {60.0 5.6} \
    -force_to_die_boundary

# Bottom - Control signals
place_pin -pin_name seq_update \
    -layer M2 -location {32.9 0.0} \
    -force_to_die_boundary
```

# OpenROAD Step 3.3: Detailed Placement



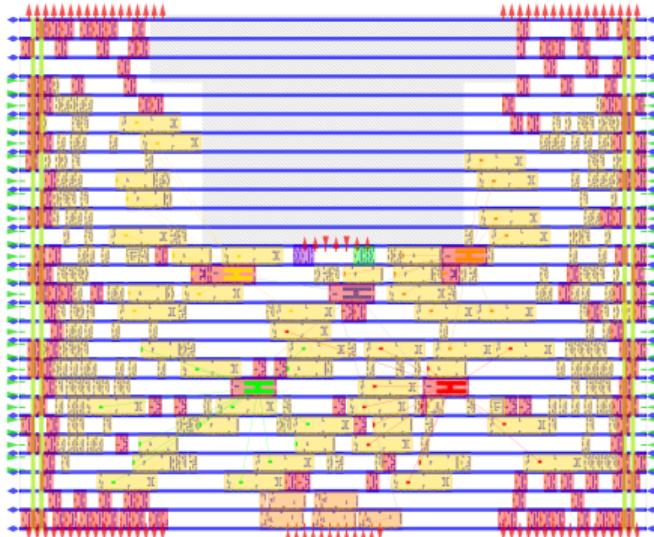
- ▶ Cells snapped to placement grid
- ▶ Critical buffers protected from removal
- ▶ Clock gate and sample driver cells preserved

## **dont\_touch.tcl**

```
# Protect sampdriver instances
set sampdriver_instances [get_cells -quiet \
    -filter "full_name == sampdriver_*"]
foreach inst $sampdriver_instances {
    set_dont_touch $inst
}

# Protect clkgate cells (TSMC65 CKLNQD1LVT)
set clkgate_cells [get_cells -quiet \
    -filter "ref_name == CKLNQD1LVT"]
foreach inst $clkgate_cells {
    set_dont_touch $inst
}
```

# OpenROAD Step 4.1: Clock Tree Synthesis



- ▶ System clock: 10 MHz (100ns period)
- ▶ Samp/comp clock: 200 MHz (5ns period)
- ▶ 50ps clock uncertainty
- ▶ Balanced tree for minimal skew

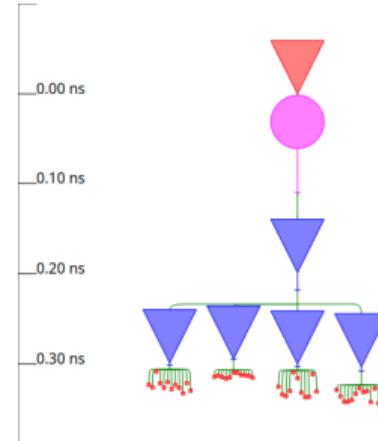
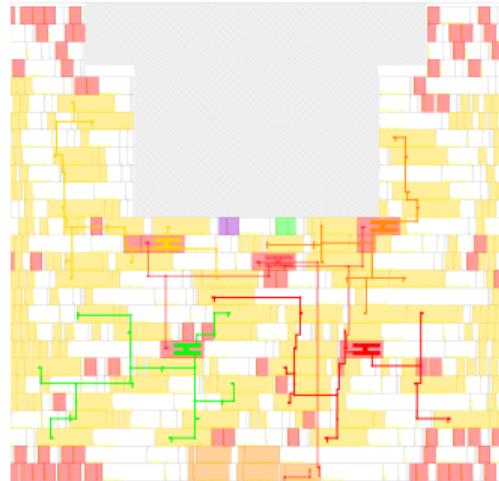
## constraint.sdc

```
current_design adc_digital

# Create clock for sequencing (200 MHz)
create_clock -name seq_update \
-period 5 [get_ports seq_update]

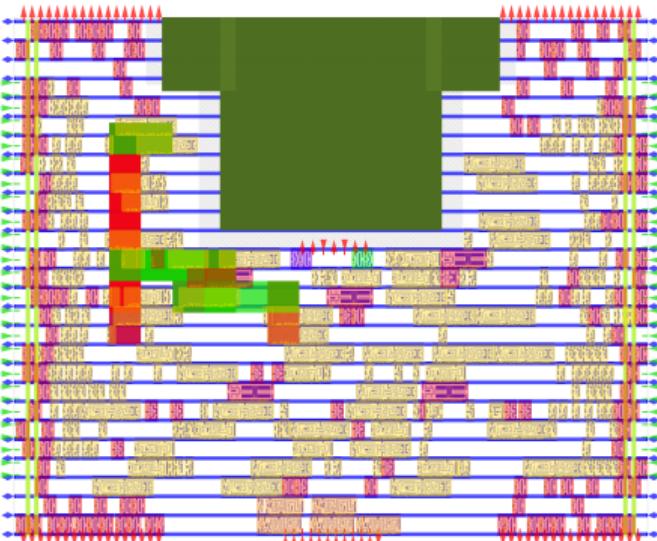
# Set clock uncertainties
set_clock_uncertainty 0.05 [all_clocks]
```

# OpenROAD Step 4.1: Clock Tree Views



**CTS Results:**  $f_{\max} = 1760 \text{ MHz}$  | Worst slack = 4.43 ns | Setup skew = 0.07 ns | Power =  $182 \mu\text{W}$

# OpenROAD Step 5.1: Global Routing



- ▶ Route guides shown for global routing
- ▶ M2-M3 routing layers only
- ▶ Routing obstructions for analog areas

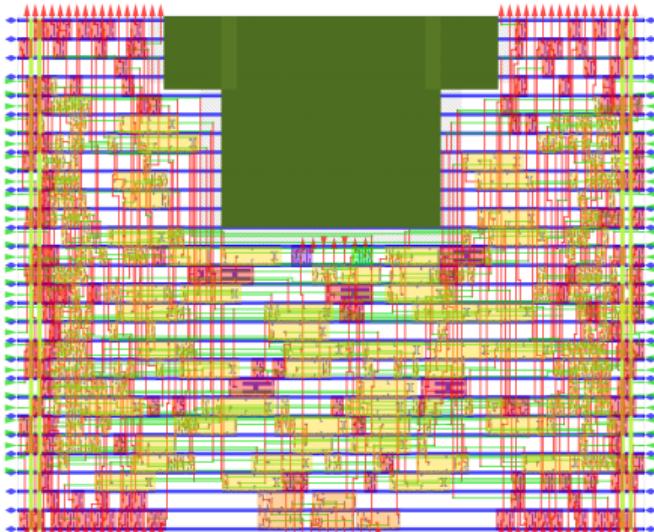
## config.mk

```
export MIN_ROUTING_LAYER = M2
export MAX_ROUTING_LAYER = M3
export PRE_GLOBAL_ROUTE_TCL = \
.../routing_blockages.tcl
```

## routing\_blockages.tcl

```
# Create obstructions on M1-M4 for analog
odb::dbObstruction_create $block $layer_M1 \
$comp_llx $comp_lly $comp_urx $comp_ury
odb::dbObstruction_create $block $layer_M2 \
$comp_llx $comp_lly $comp_urx $comp_ury
```

# OpenROAD Step 5.2: Detailed Routing

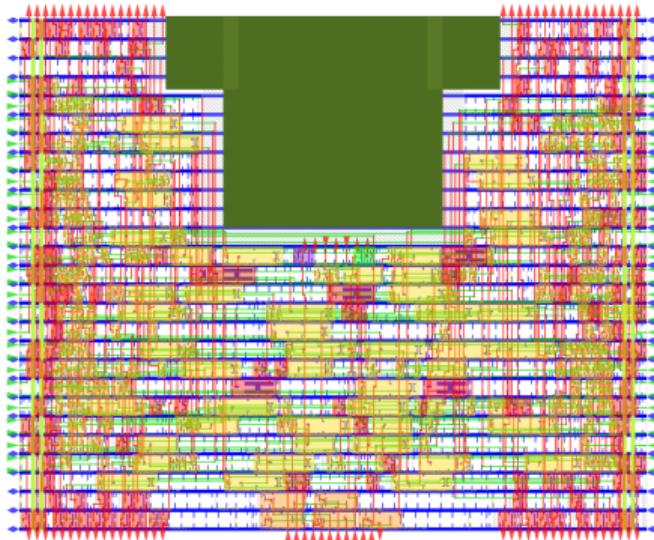


- ▶ Final metal routing on M2/M3
- ▶ All signals routed to I/O pins
- ▶ DRC-clean routing around blockages

## config.mk

```
# Based on TSMC65LP metal stack  
# from tcbn65lp_9lmt2.lef  
export MIN_ROUTING_LAYER = M2  
export MAX_ROUTING_LAYER = M3
```

## OpenROAD Step 5.3: Fill Cells

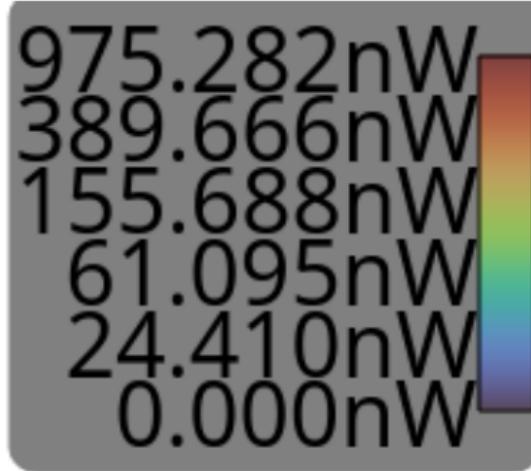
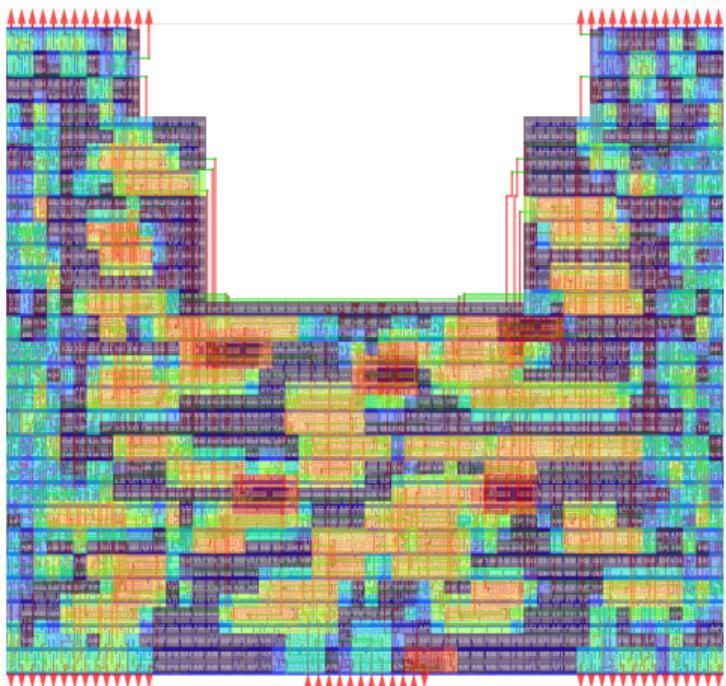


- ▶ Decap fill cells added (FEOL)
- ▶ Metal fill disabled (BEOL)
- ▶ Fills gaps in standard cell rows

### config.mk

```
# Only disables metal fill  
# FILL_CELLS in routing step still  
# adds FEOL decap fill cells  
export USE_FILL = 0
```

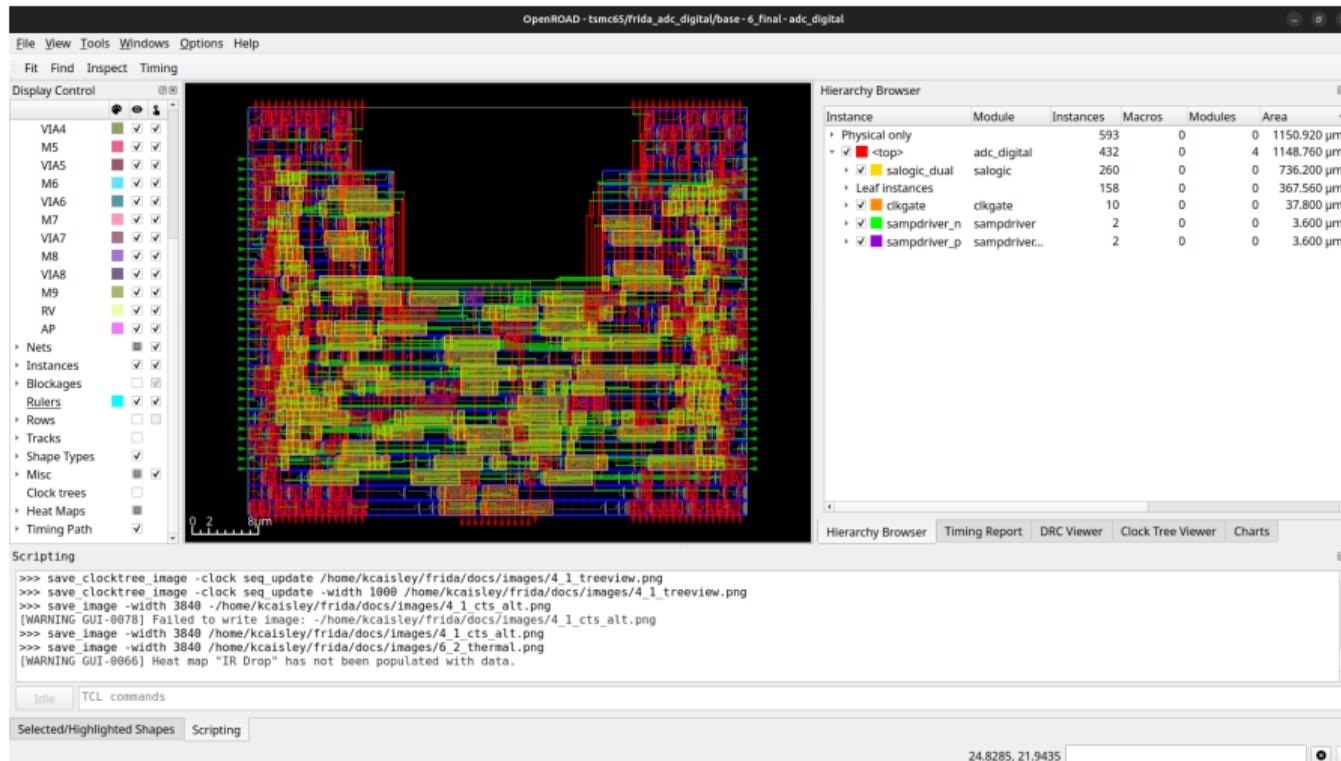
## OpenROAD Step 6.1: Heat Maps



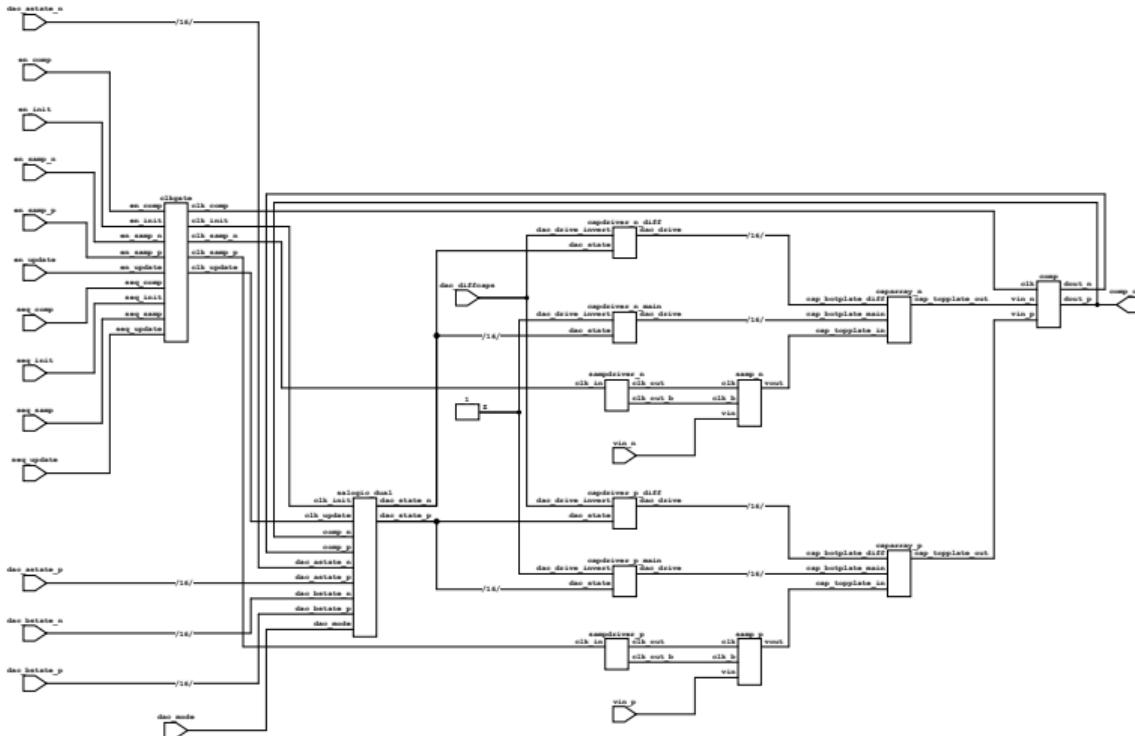
- ▶ Spatial visualizations for IR drop, thermal dissipation, placement density, pin density, and power consumption are available

# OpenROAD GUI

- ▶ Interactive GUI, net tracing, hierarchical cell grouping, timing reports, DRC viewer, heatmaps



# ADC Top-Level Assembly



- ▶ ADC assembled using hierarchical Verilog as well, with protected routing for sensitive analog nets

# ADC Level Integration

