

CS 5220 Pre-Class Questions 2

Ian MacCormack

August 31, 2015

Question 1

Accelerators:

$(2 \text{ flops/FMA}) * (8 \text{ FMA/vector FMA}) * (1.053 \text{ GHz}) * (15 \text{ accelerators}) = 250 \text{ GFLOPS}$

Cores:

$(2 \text{ flops/FMA}) * (8 \text{ FMA/vector FMA}) * (3.2 \text{ GHz}) * (60 \text{ cores}) = 3.02 \text{ TFLOPS}$

Total: 3.27 TFLOPS

Question 2 In light of the calculation done in the lecture slides, given that I also have an i5 Haswell processor (albeit a 1.3 GHz one), following the same calculation as the professor, I arrive at roughly 42 GFLOPS.

Question 3 According to the lecture slides, the maximum speedup would be p , independent of the number of tasks.

Question 4

Minimum serial time = 2.75 hrs.

Minimum parallel time = 2.25 hrs. (will add diagram after lecture)

Question 5 This plot (on next page) tells me that my computer has markedly poor performance when accessing the L3 cache with a moderate stride on a very large array. This is pretty clear from the dramatically red wedge corresponding to these processes at the upper center of the graphic.

Question 6 Unsurprisingly, Totient appears to perform slightly better than my machine. There is a temporary, observable plateau between stride sizes of 2^6 and 2^{10} (roughly). This corresponds to what I think is L2 cache access, telling us that Totient has a fairly ample L2 cache. After strides of around 2^{10} bytes, we see a dramatic spike in processing time, indicating that the L3 cache access is not quite as speedy. (See plot below)

Question 7 The execution times resulting from these three algorithms (run on my machine) are as follows:

Version 1: 3.994100e-03

Version 2: 7.231180e-03

Version 3: 7.238760e-03

It is clear that the first is fastest, roughly by a factor of 2. This may be due to having a single loop and only having a single memory location for the array.



