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ELEC 311 HW #1

In this assignment we were suppose to design analyse and simulate an inverter.

1)Verilog Part

I applied clock-like signal from 0 to 1.8V and took snapshot(figure 1.2) of input and output, to prove functionality. Also figure 1.1 show the code of verilog part.

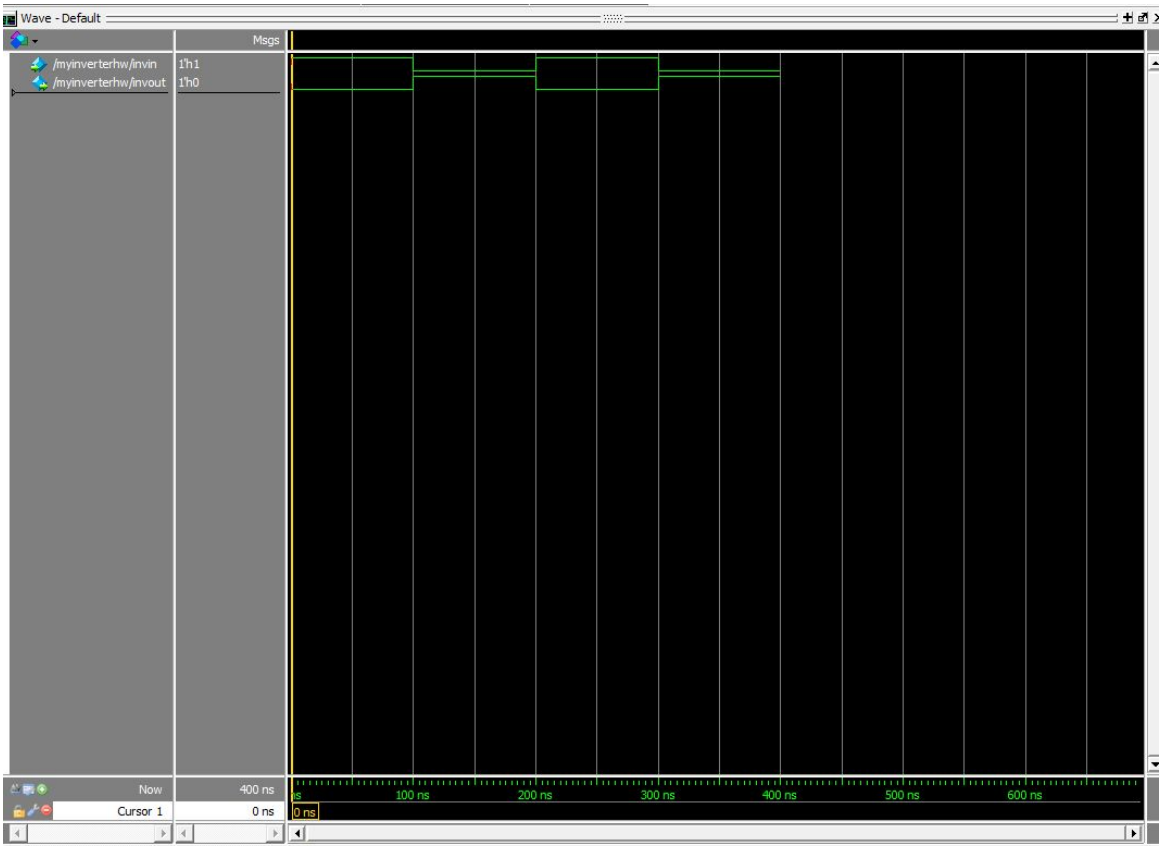


Figure 1.1

```
1
2   module myinverterhw(invin, invout);
3   input invin;
4   output invout;
5
6   assign invout = ~invin;
7
8   endmodule
```

Figure 1.2

2)LTSpice Part

To make an inverter in spice I used 1-1.5 rule. Figure 2.1 shows designed inverter and figure 2.2 shows symbol design of the inverter. Transistor lengths are always minimum in digital design so I used 0.24u for NMOS and PMOS. Also for width I used minimum values with 1 – 1.5 ratio. Figure2.3 shows the transient analyse design of switch. I added pulses so I reached simulation of the design in figure 2.4 . Figure 2.5 shows 5 and 10 inverter parallel and simulation of them in figure 2.6.

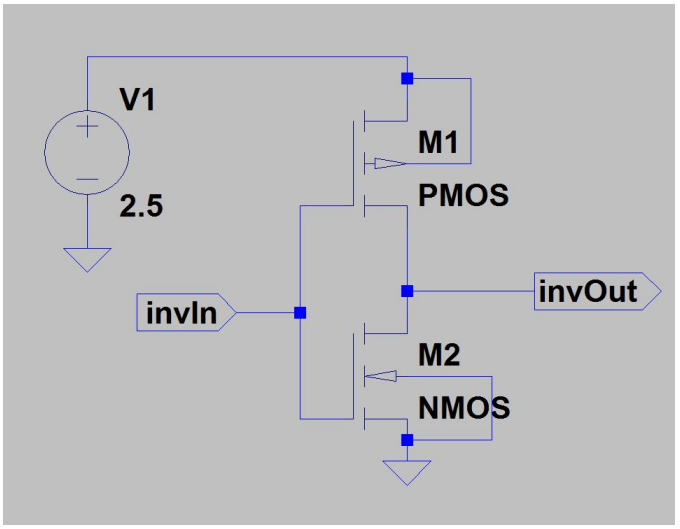


Figure 2.1

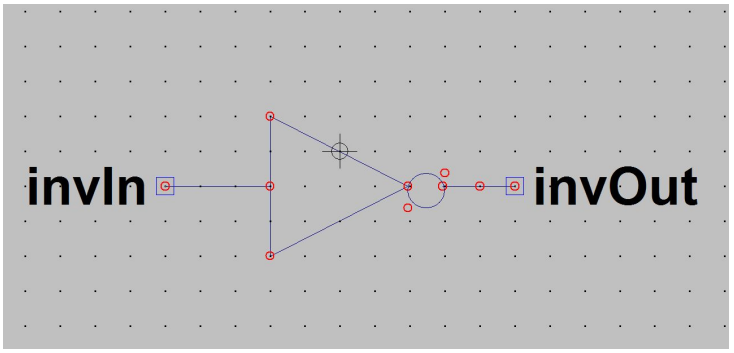


Figure 2.2

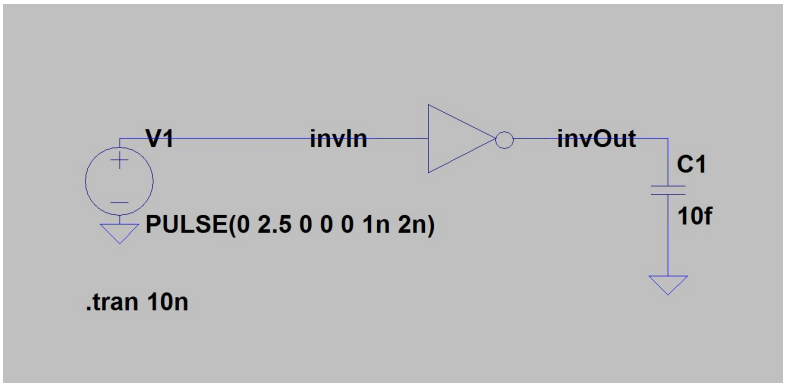


Figure 2.3

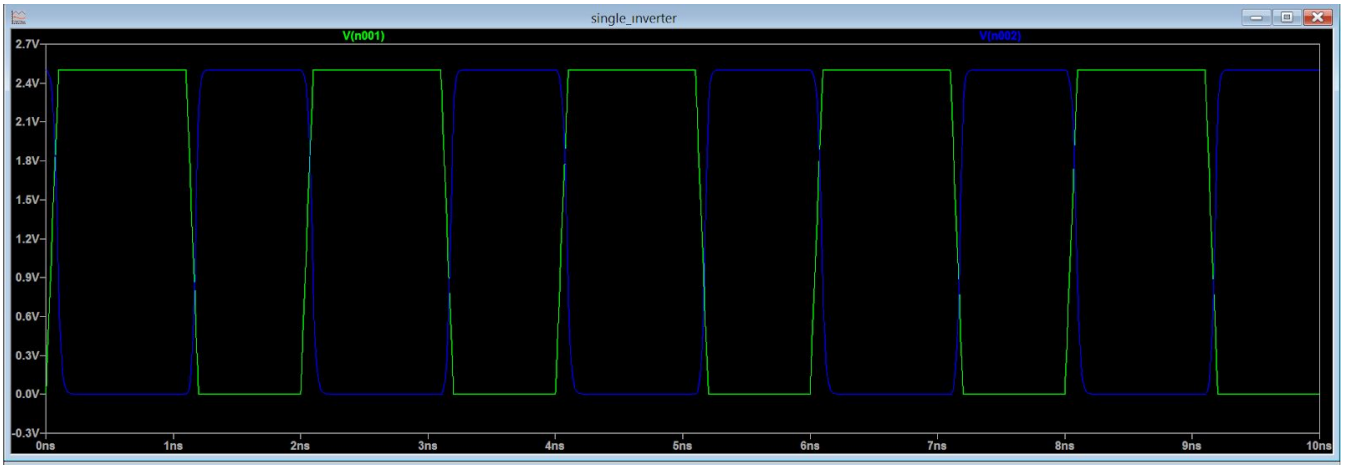


Figure2.4

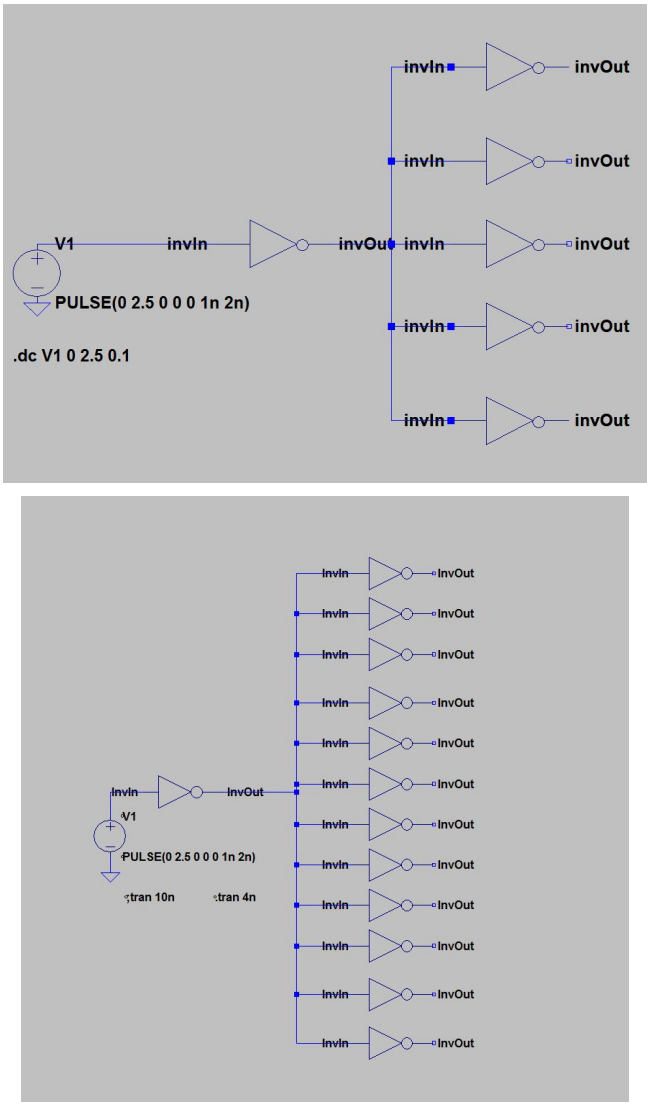


Figure 2.5

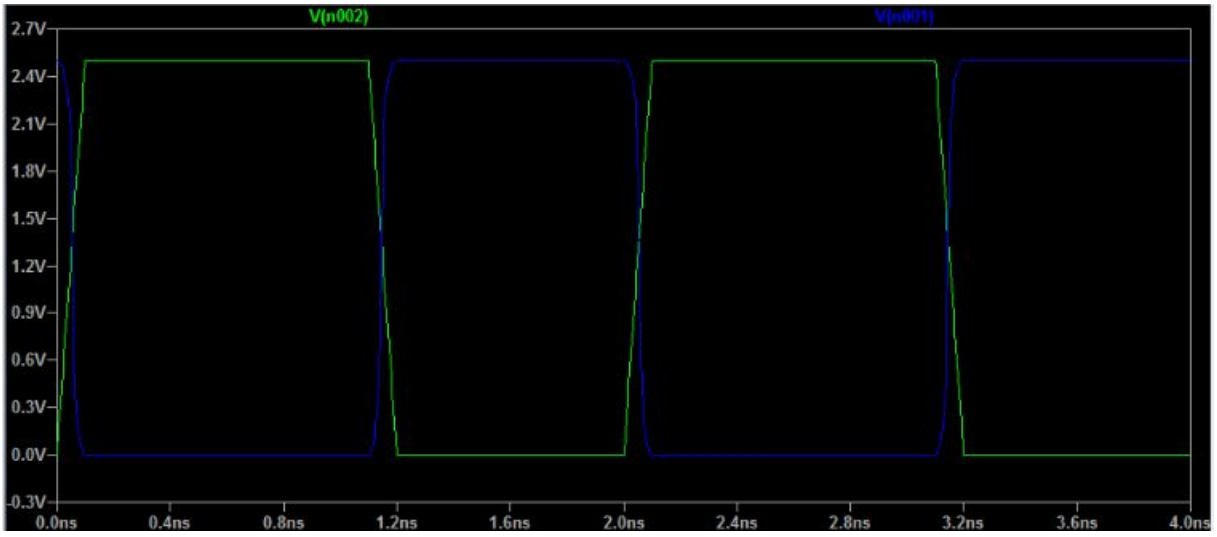
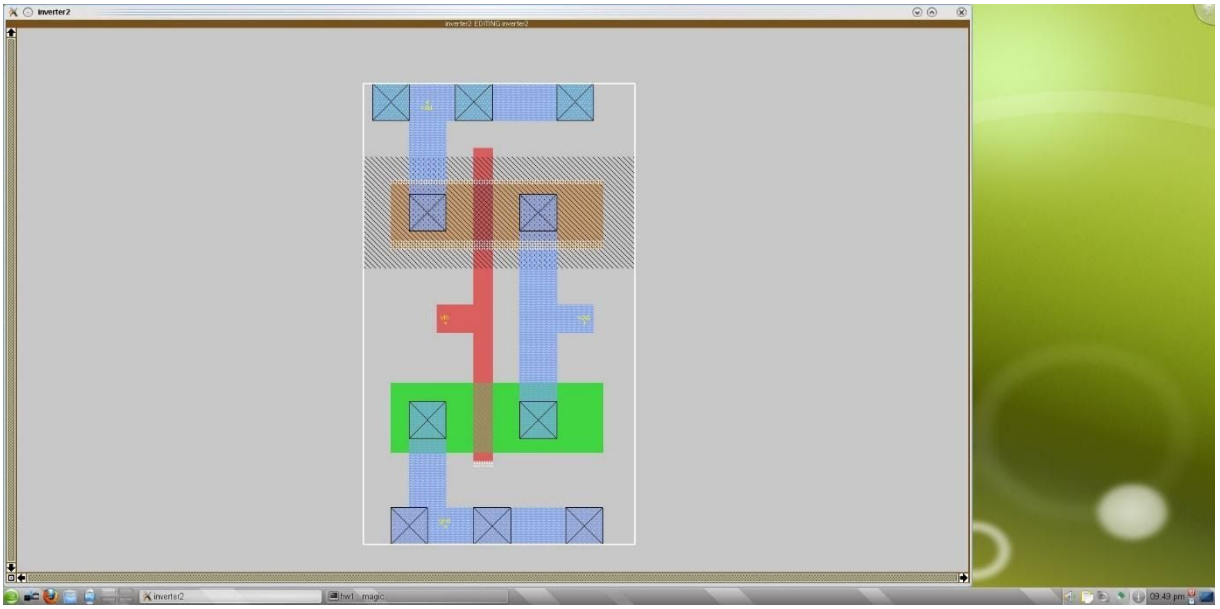
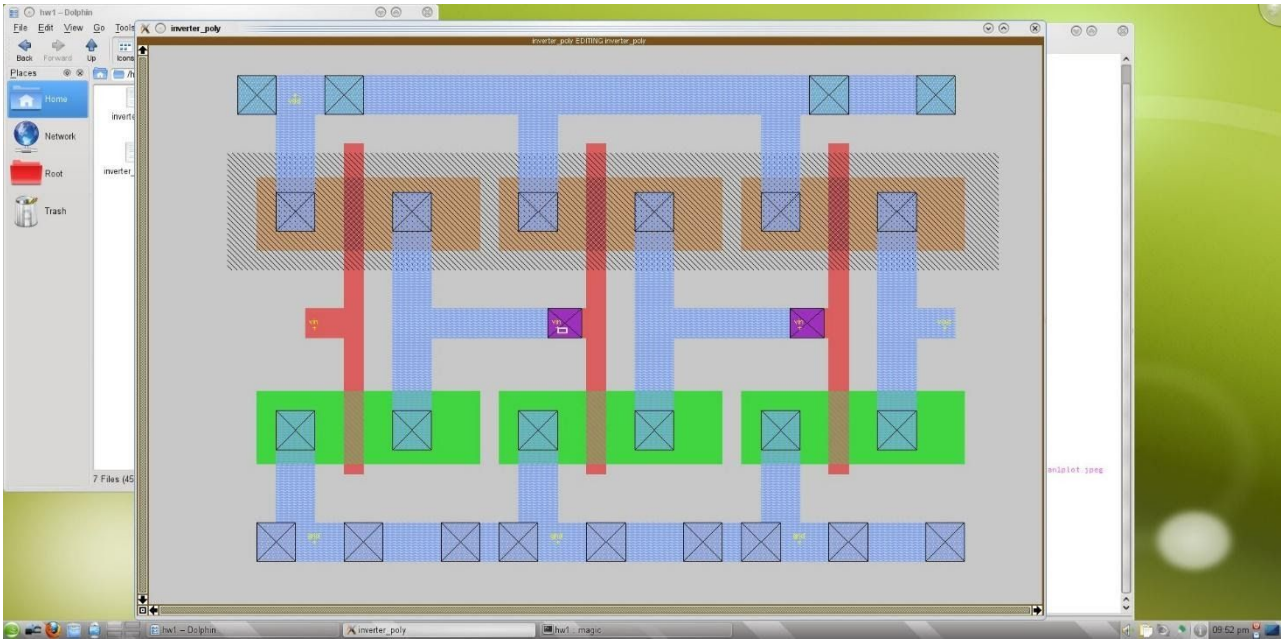


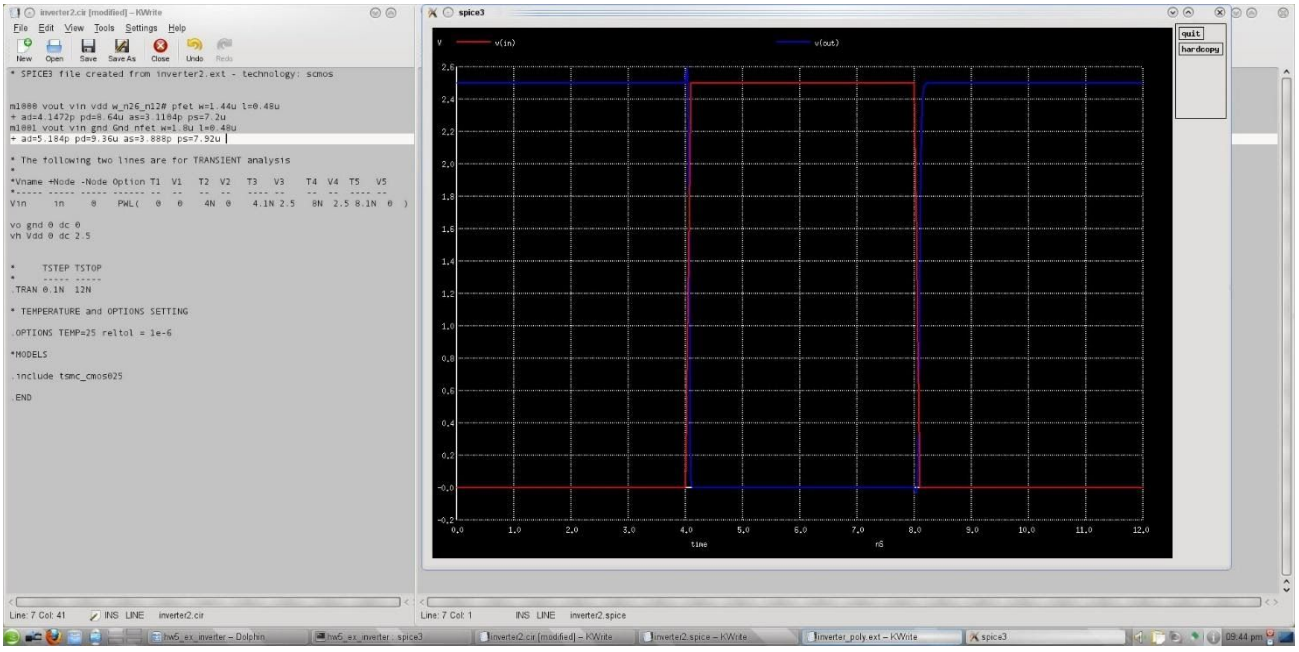
Figure 2.6

3)Magic VLSI Layout Tool Part

Before starting to do this part I setup linux operating system via virtual machine. And using terminal commands let me build new magic file. The file started to work with the technology: SCN5M_DEEP.12.The layout consists of polysilicon(poly), metal1(m1), nwell,p-diffusion layer(pdiff),pwell,n-diffusion layer,p-d contact(pdc),n-d contact(ndc),n-substract contact,p-substract contact. After saving I extracted it to spice(ext2spice). Figure 3.1 shows single inverter layout , figure3.2 shows 3 inverter in series , figure3.3 show simulation of extracted netlist.

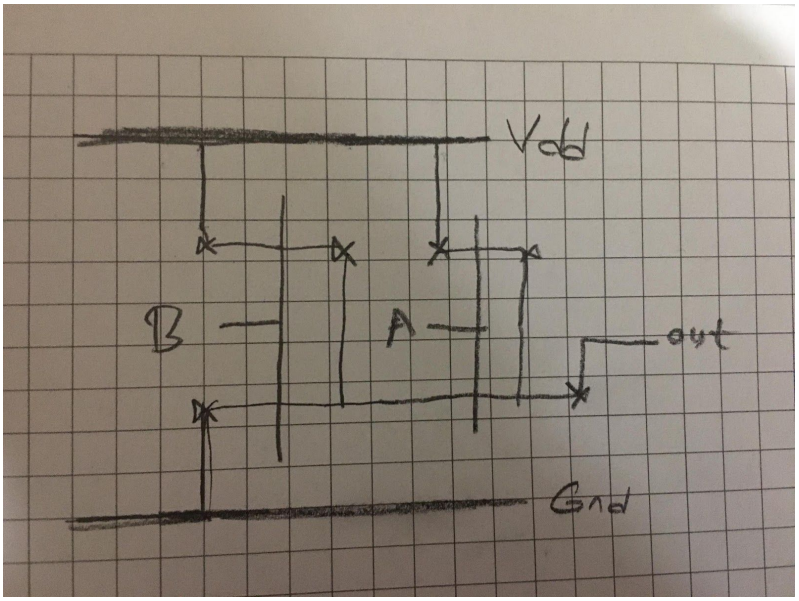






4)Stick Diagram

Figure shows the stick diagram of the inverter.



References

1. http://asic-world.com/verilog/
2. http://opencircuitdesign.com/magic