ELEC311 STANDARD CELL LIBRARY REPORT

For this group project, the aim is to build a standard cell library which consists of INV1X, INV2X, INV4X, INV8X, XOR, XNOR, NAND2X1, NAND3X1, NOR2X1, NOR3X1, transmission gate, MUX2X1, DFF. The group members and distribution of work is as following:

Gökhan Gürbilek	INV1X, INV2X, INV4X, INV8X
Abdülhamit Parlak	XOR, XNOR
Korhan Alper	Transmission gate, MUX2X1, DFF
Kağan Cenan	NOR2X1, NOR3X1
Ömer Faruk Yüksekten	NAND2X1, NAND3X1

In all the cell that consists of inverter in its internal design, INV1X is used as the inverter. The length of the unit inverter is 2.4um. The widths of the NMOS and PMOS that are used in the design are 15.36um and 46.08um respectively. All the other inverters are designed based on this unit inverter. Each section of this report describes a cell with its, transistor sizes, magic layout, functional simulation, rise/fall time simulations, schematic, symbol, and its simulation in LTSPICE.

All the files of this standard library can be accessed via the link below.

https://drive.google.com/drive/folders/0B7VfIIMTjPF9cm1xU1VzM3E3aUU?usp=sharing

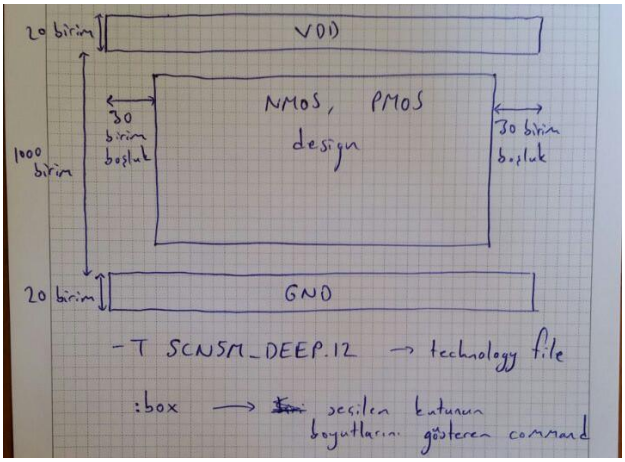

Figure 1: Sizing specifications for every cell

INV1X

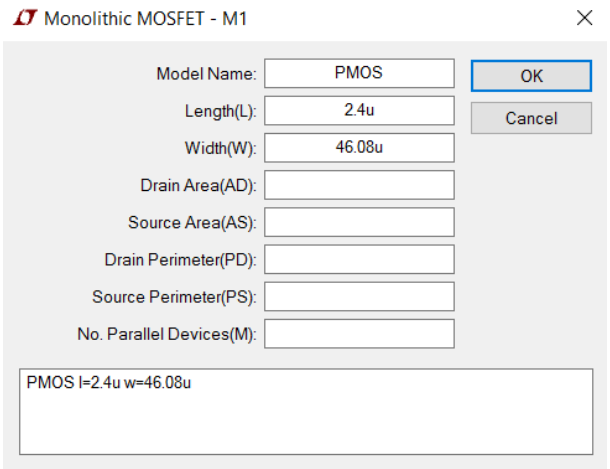

Figure 2: Size of PMOS (INV1X)

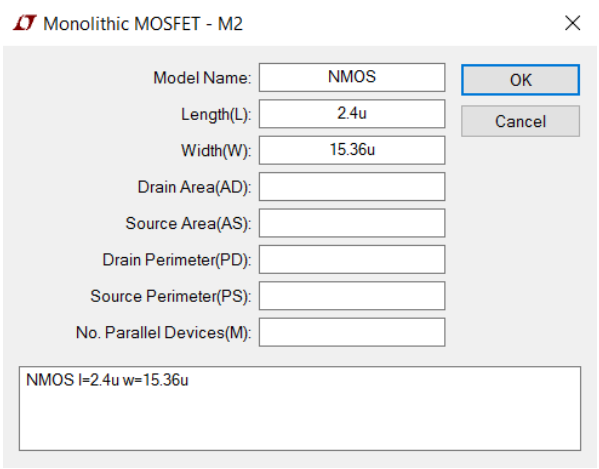

Figure 3: Size of NMOS (INV1X)

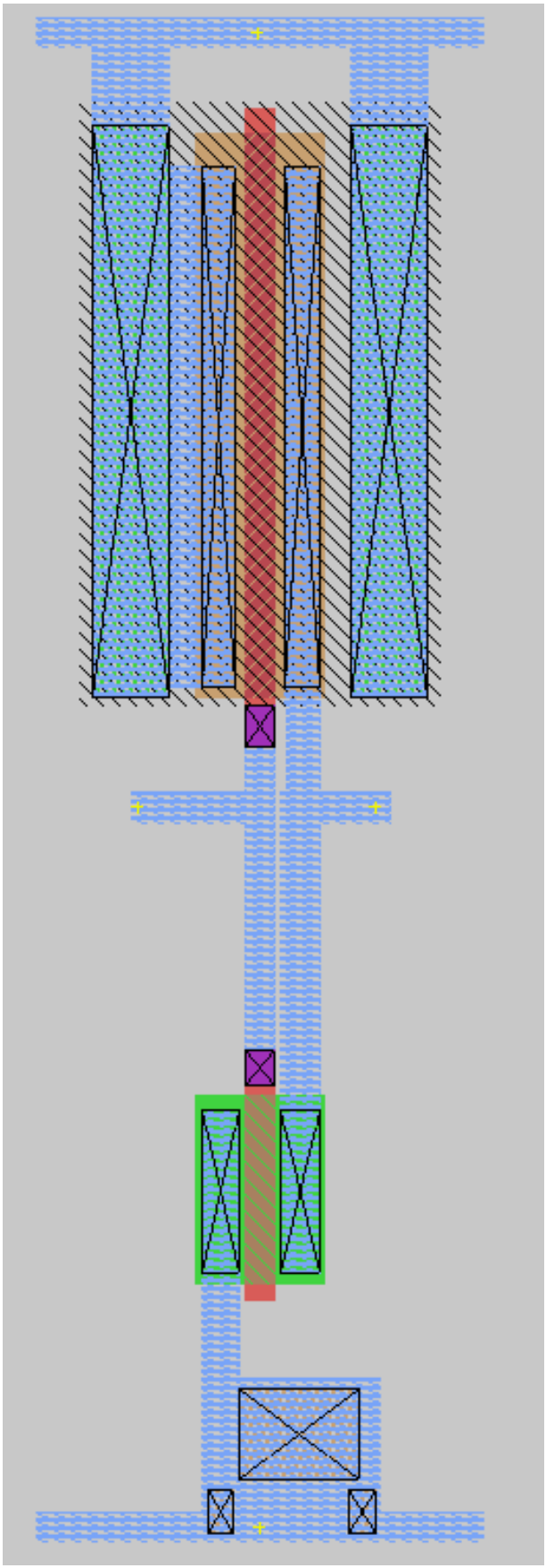

Figure 4: INV1X VLSI design in Magic

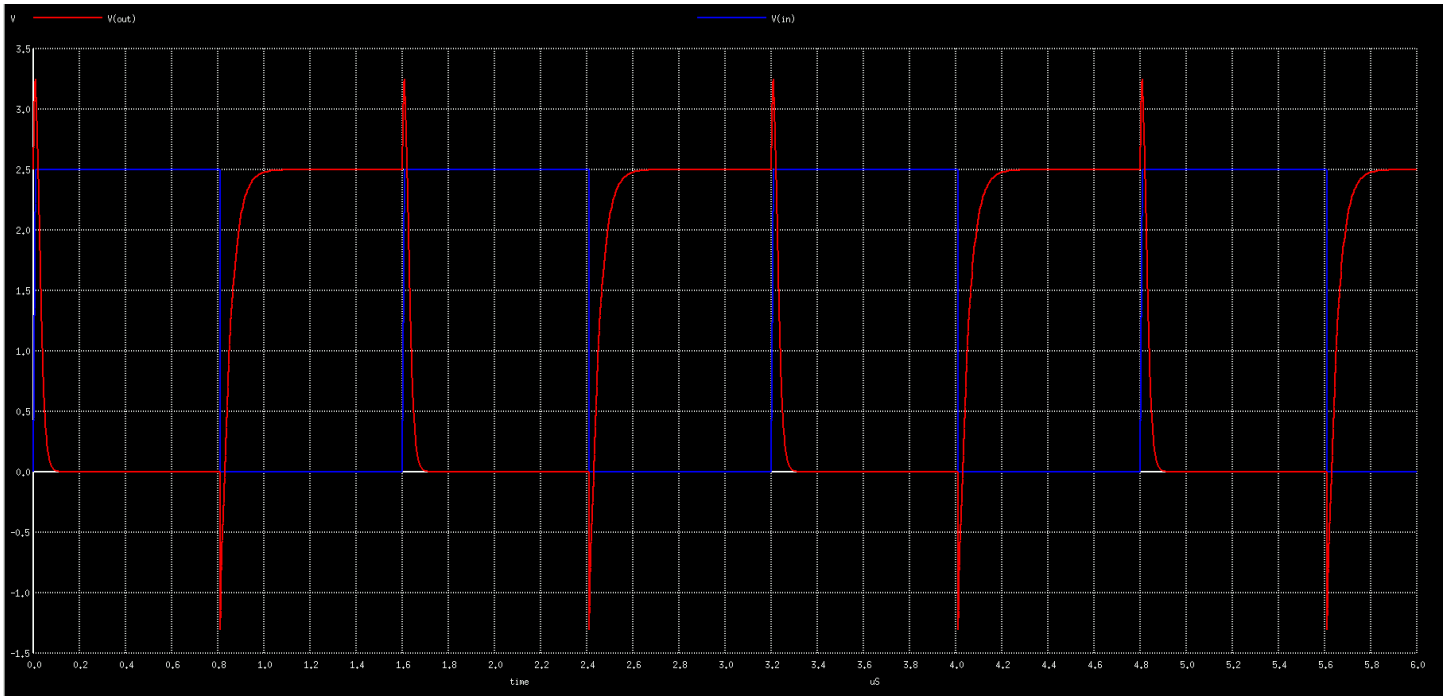

Figure 5: Functional simulation of INV1X

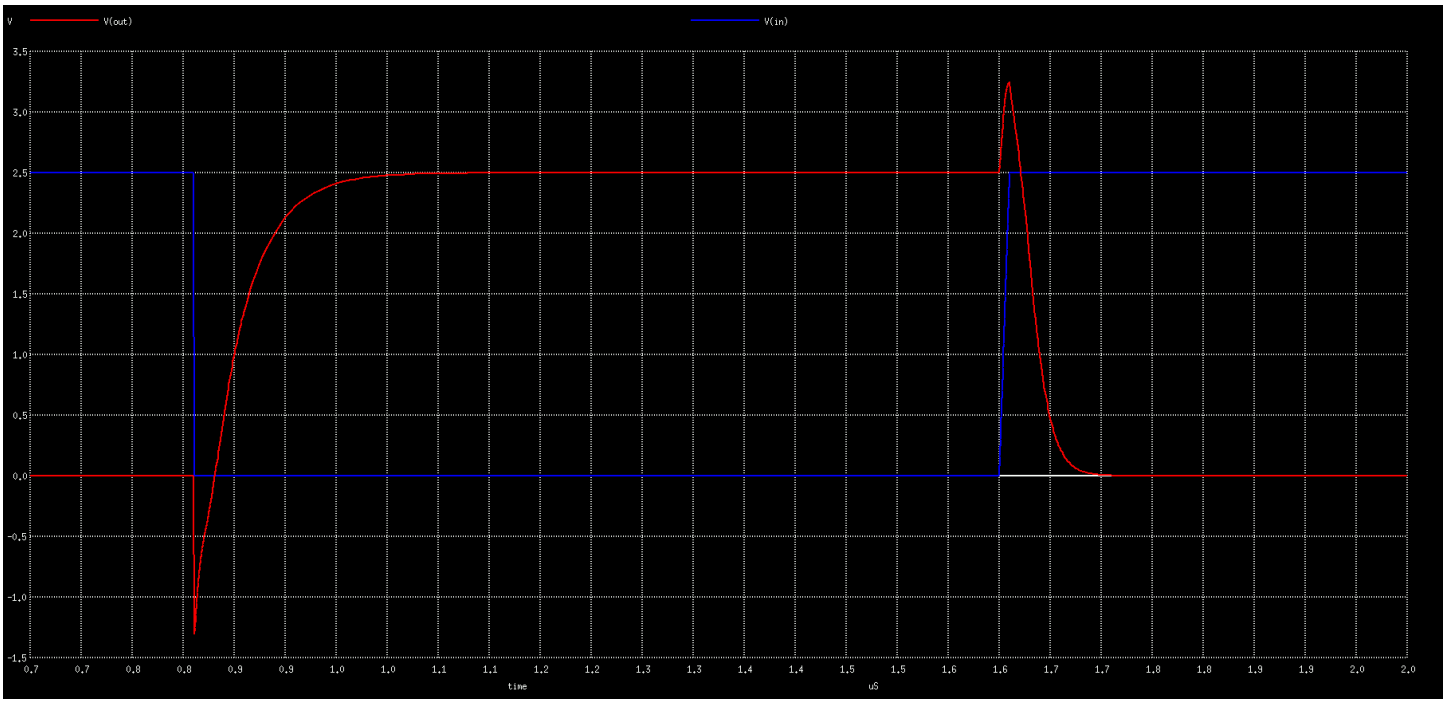

Figure 6: Fall/Rise time of INV1X

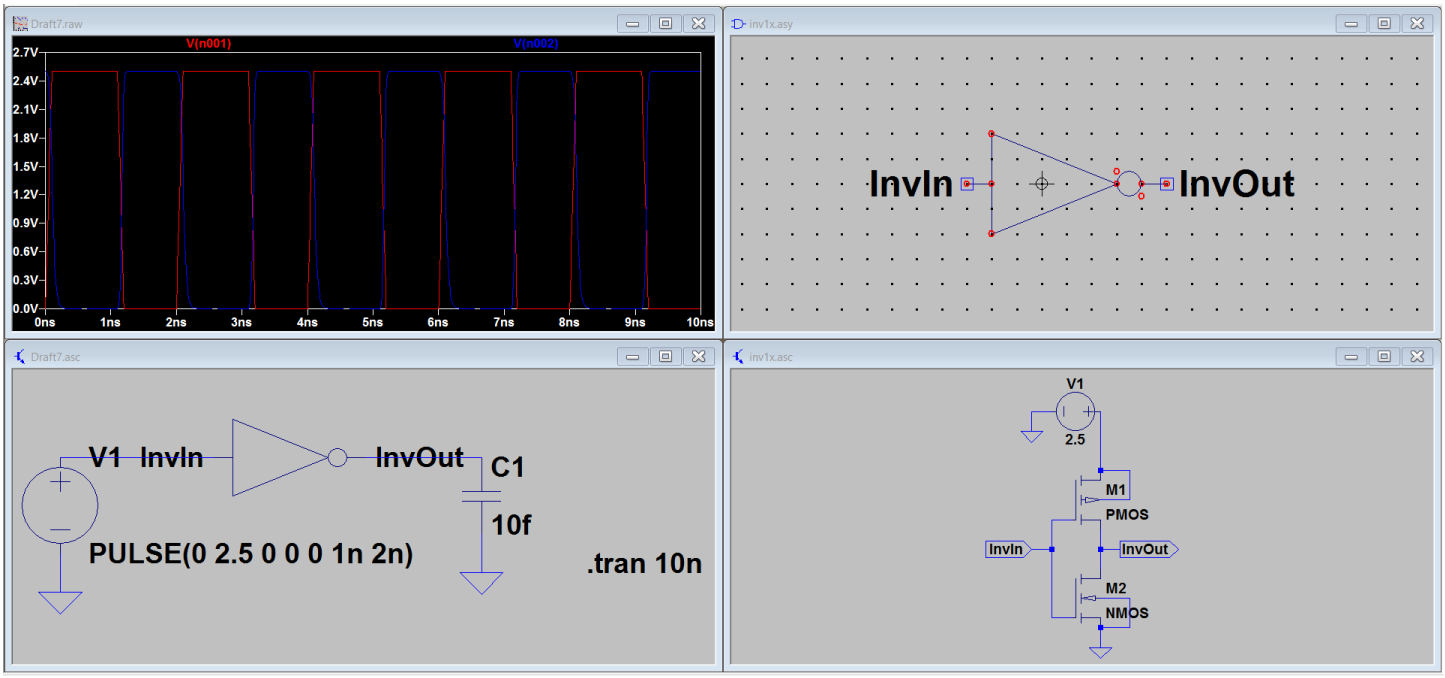

Figure 7: Symbol and circuit schematic of INV1X with its functional simulation

INV2X

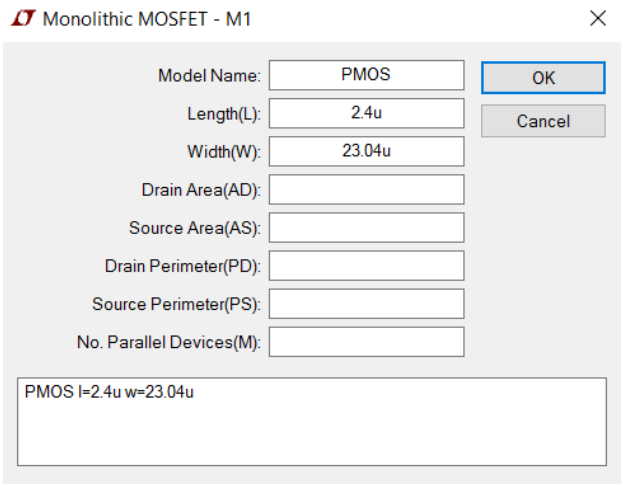

Figure 8: Size of PMOS (INV2X)

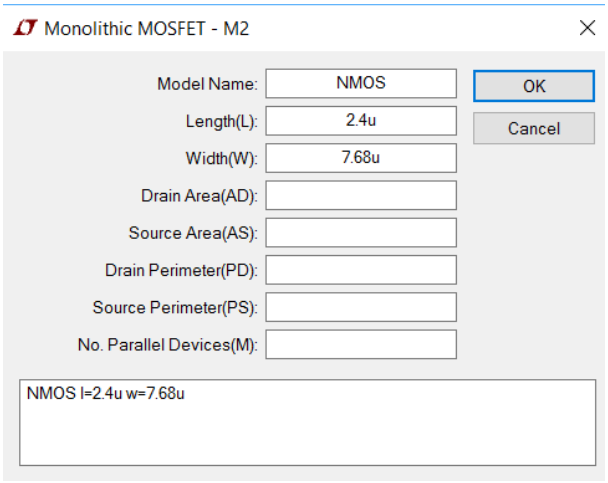

Figure 9: Size of NMOS (INV2X)

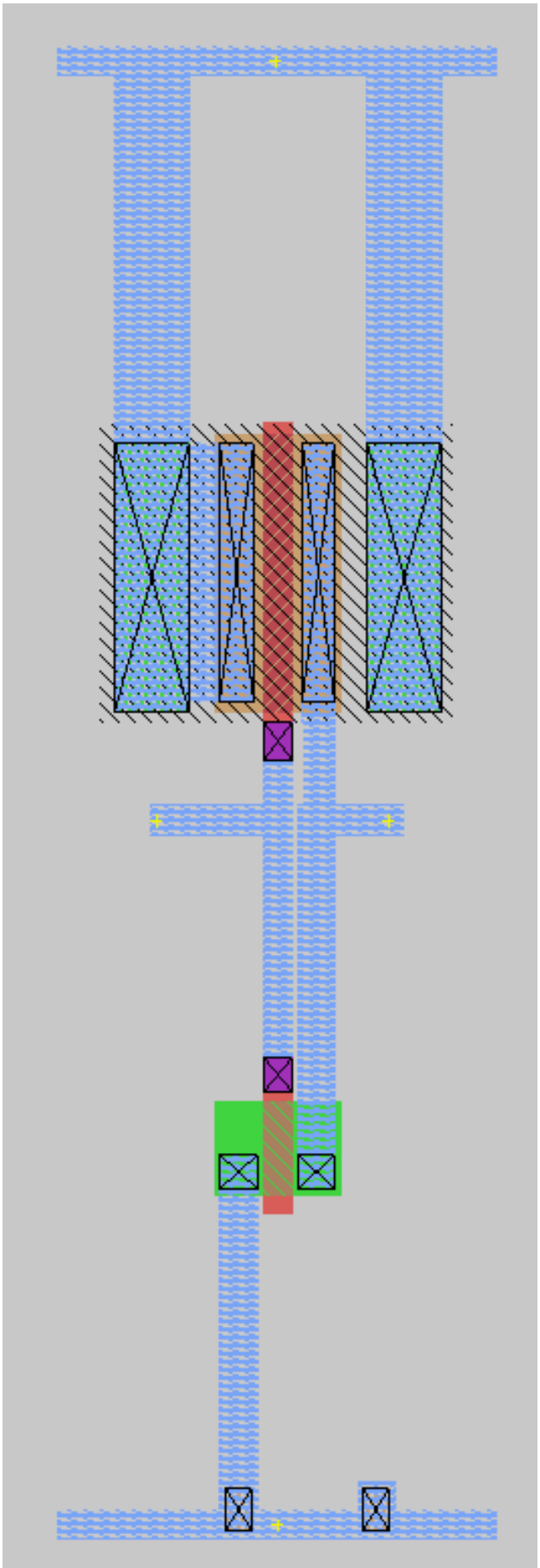

Figure 10: INV2X VLSI design in Magic

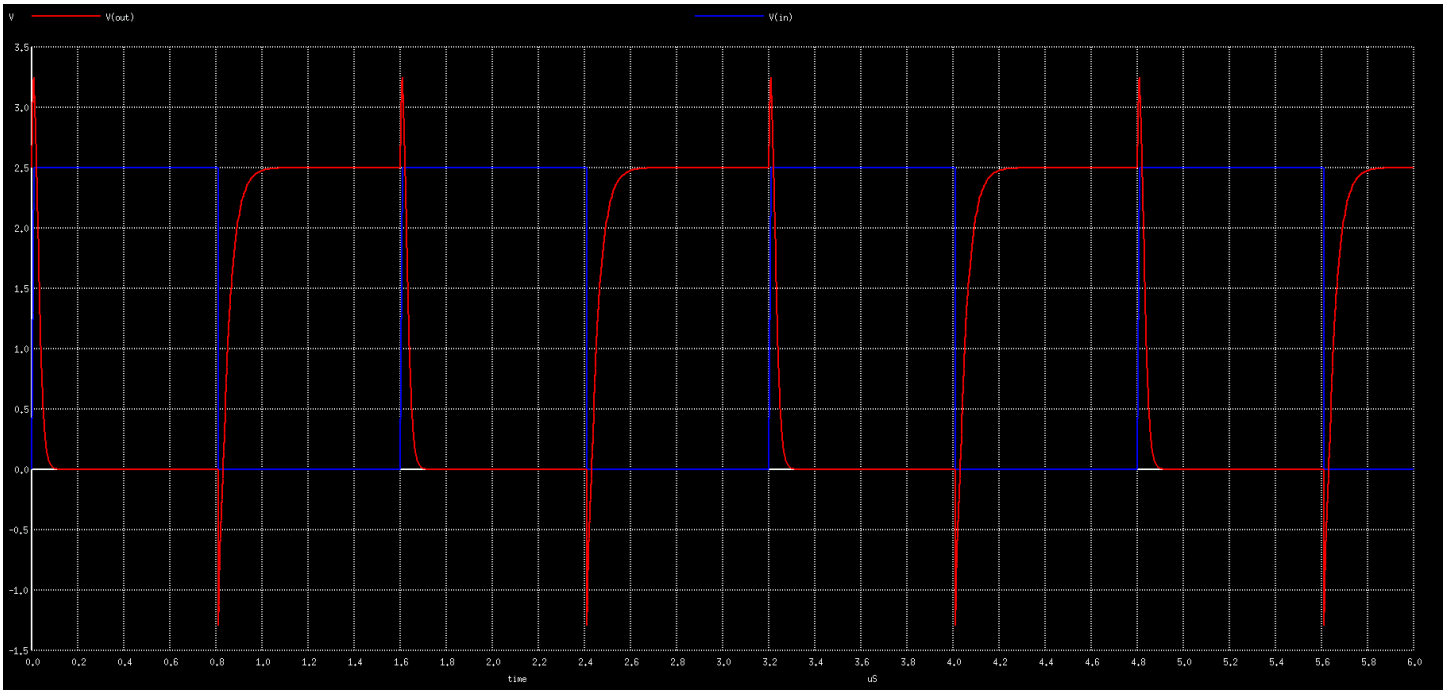

Figure 11: Functional simulation of INV2X

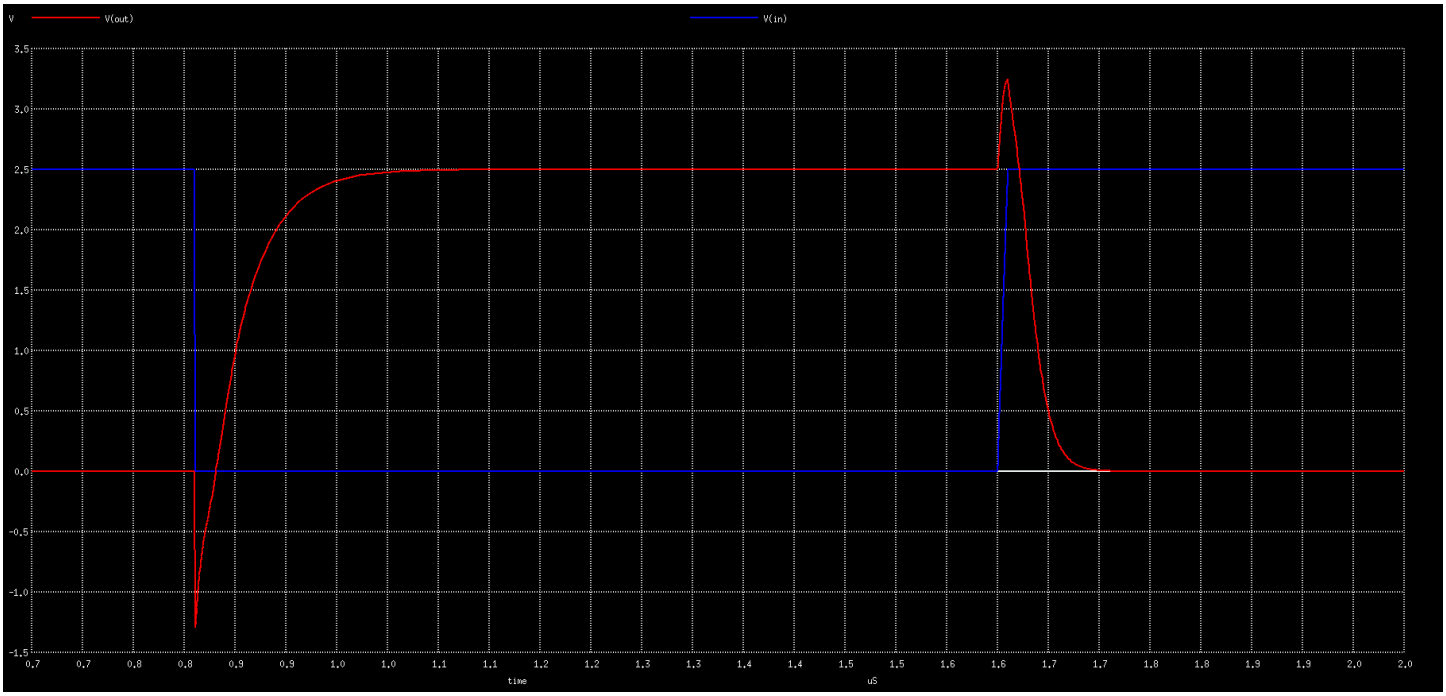

Figure 12: Fall/Rise time of INV2X

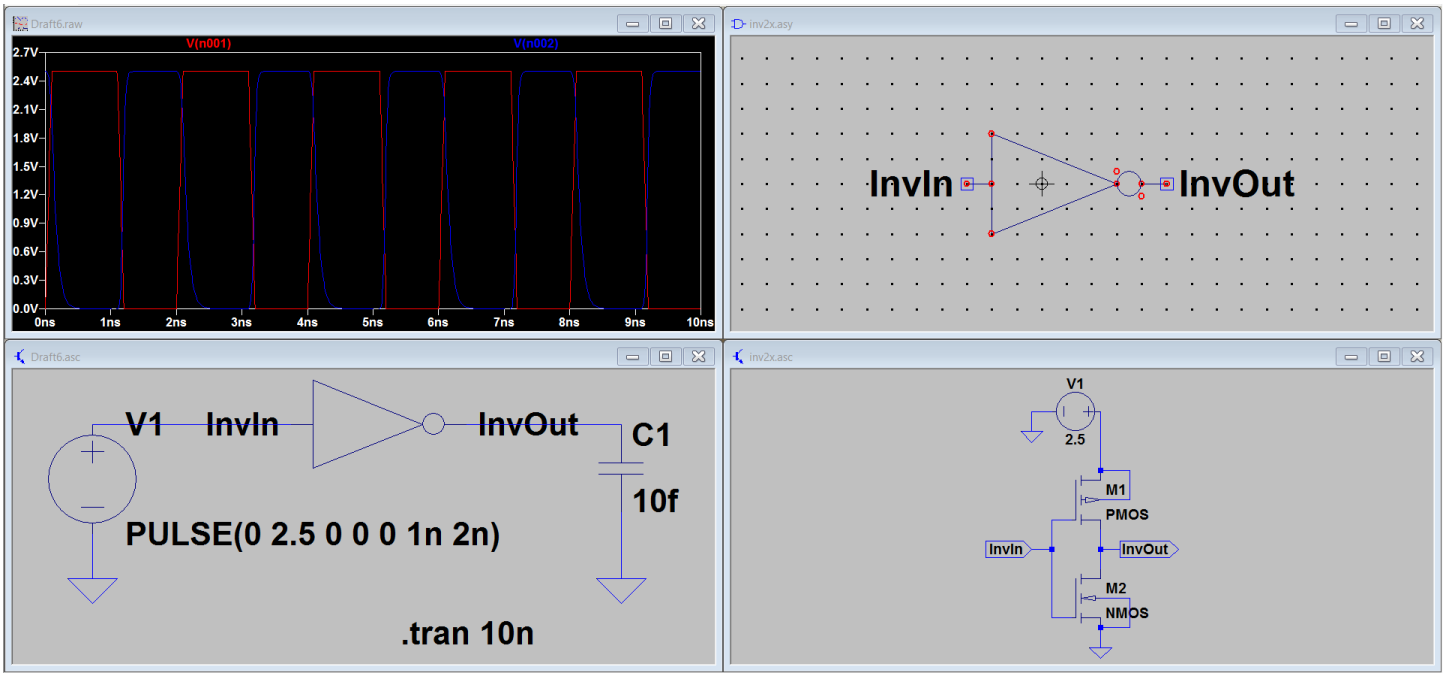

Figure 13: Symbol and circuit schematic of INV2X with its functional simulation

INV4X

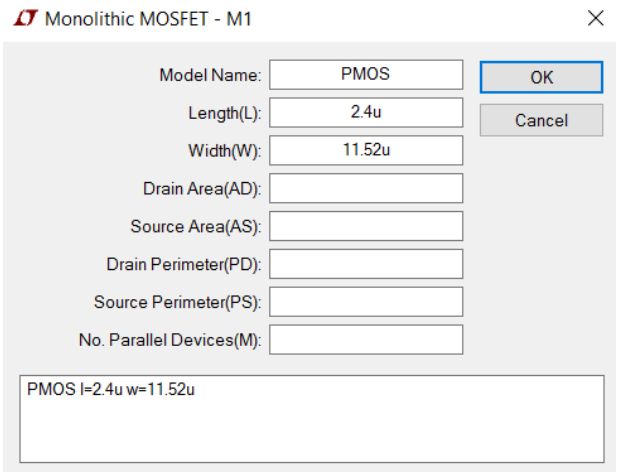

Figure 14: Size of PMOS (INV4X)

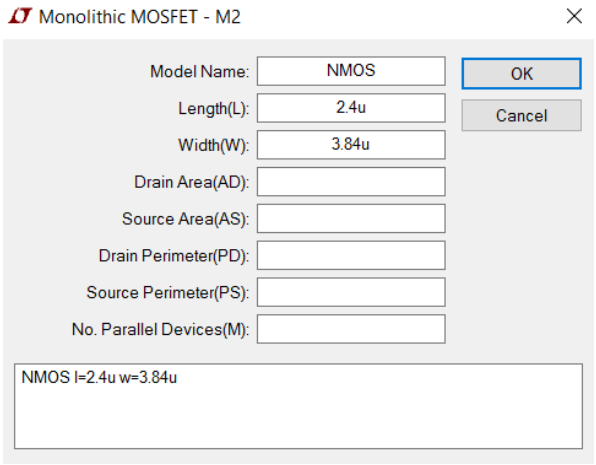

Figure 15: Size of NMOS (INV4X)

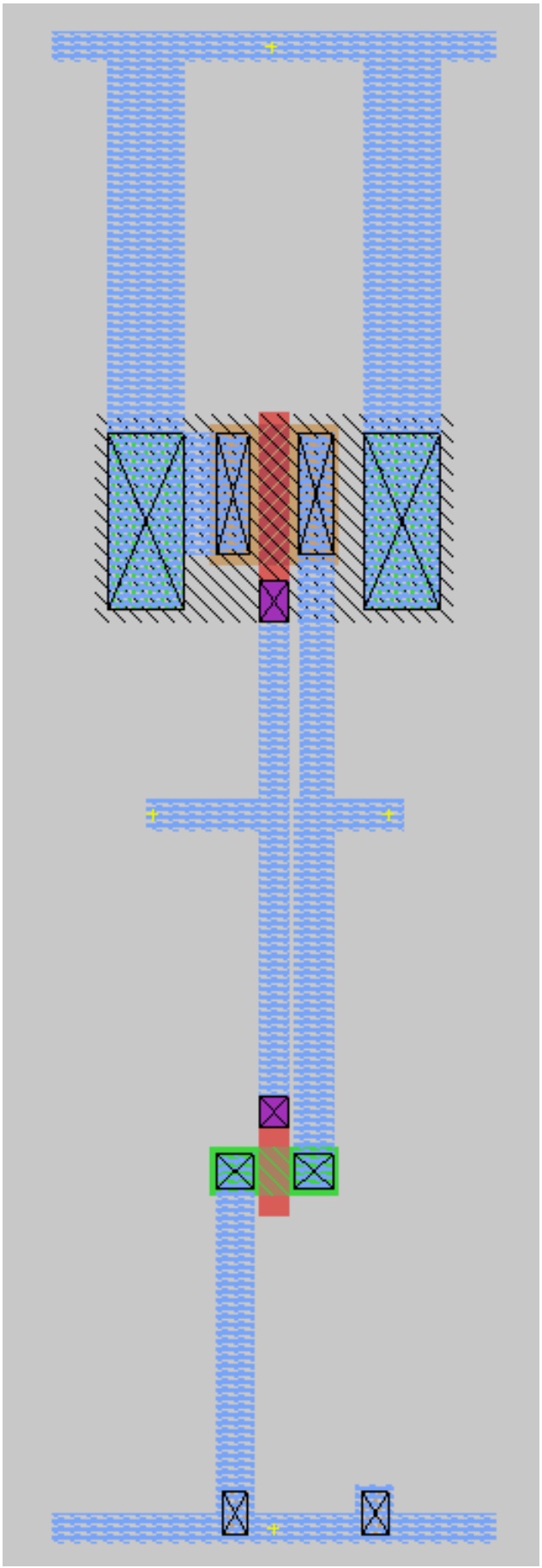

Figure 16: INV4X VLSI design in Magic

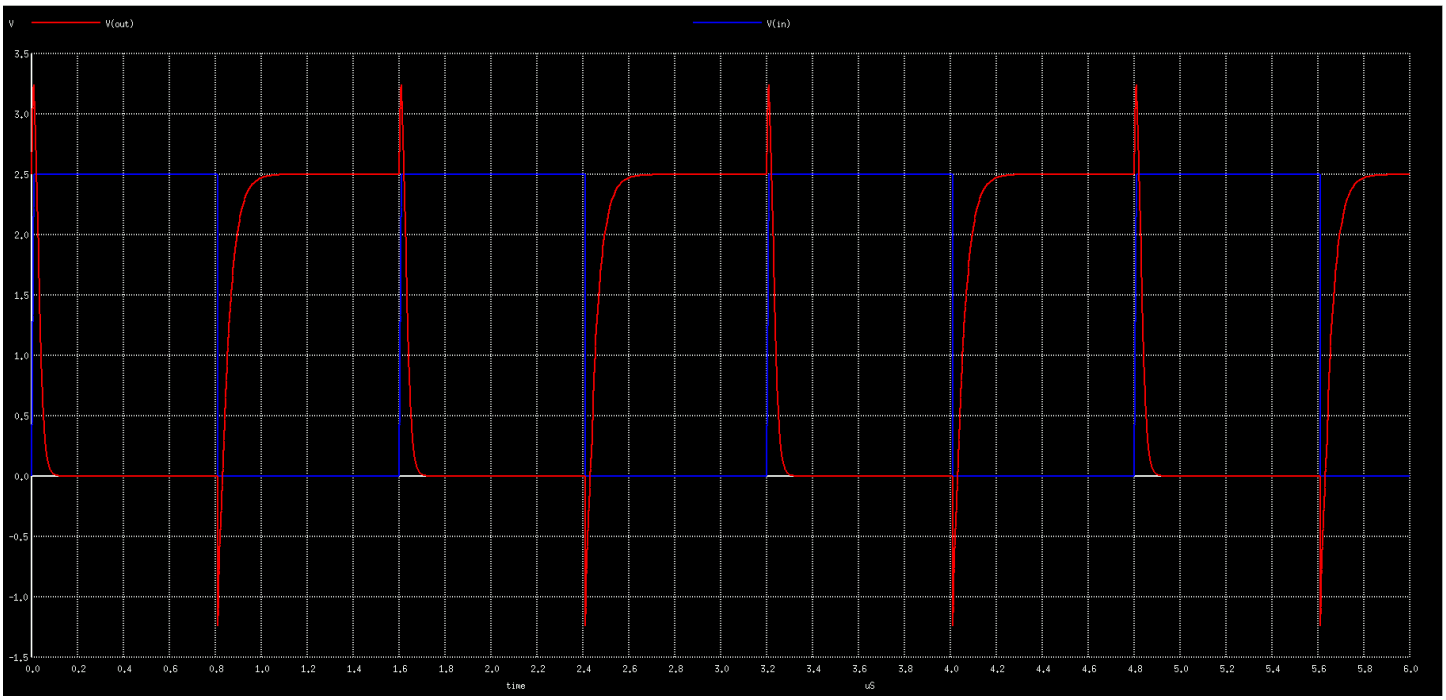

Figure 17: Functional simulation of INV4X

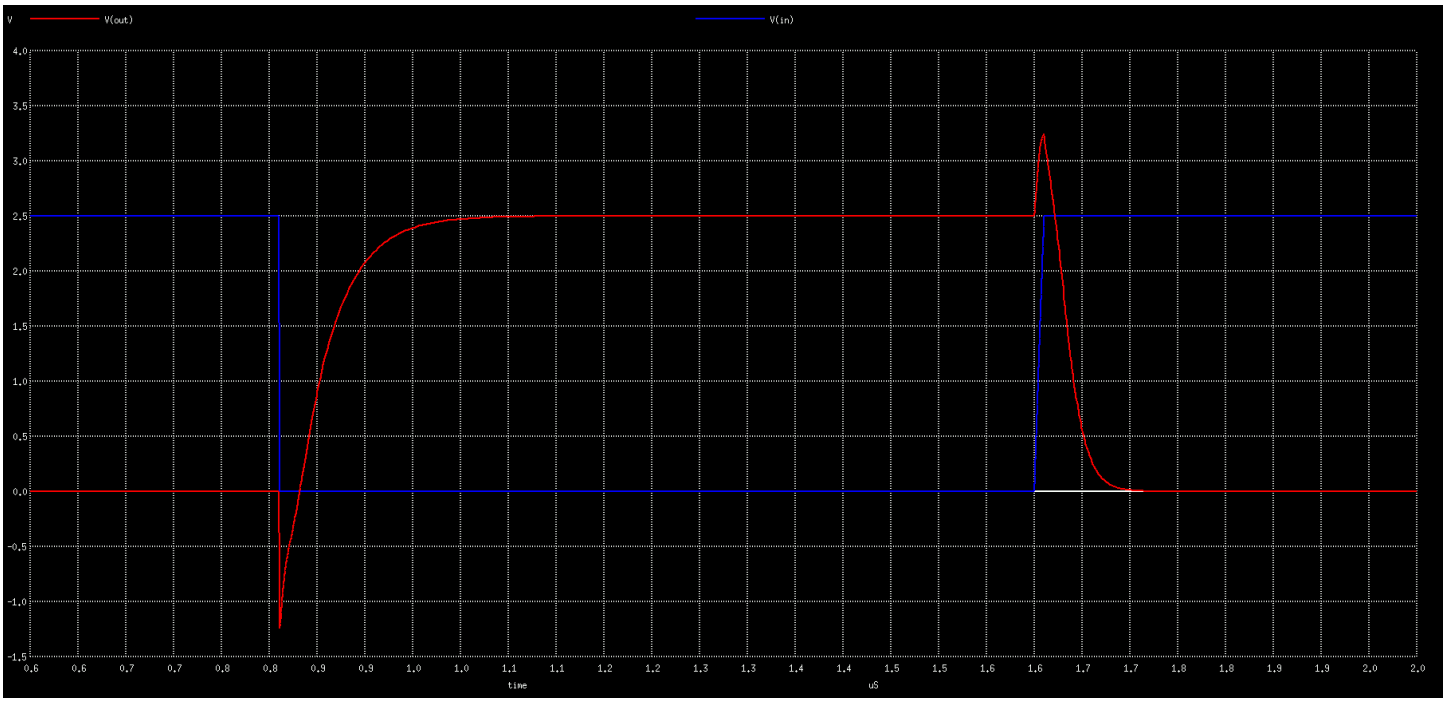

Figure 18: Fall/Rise time of INV4X

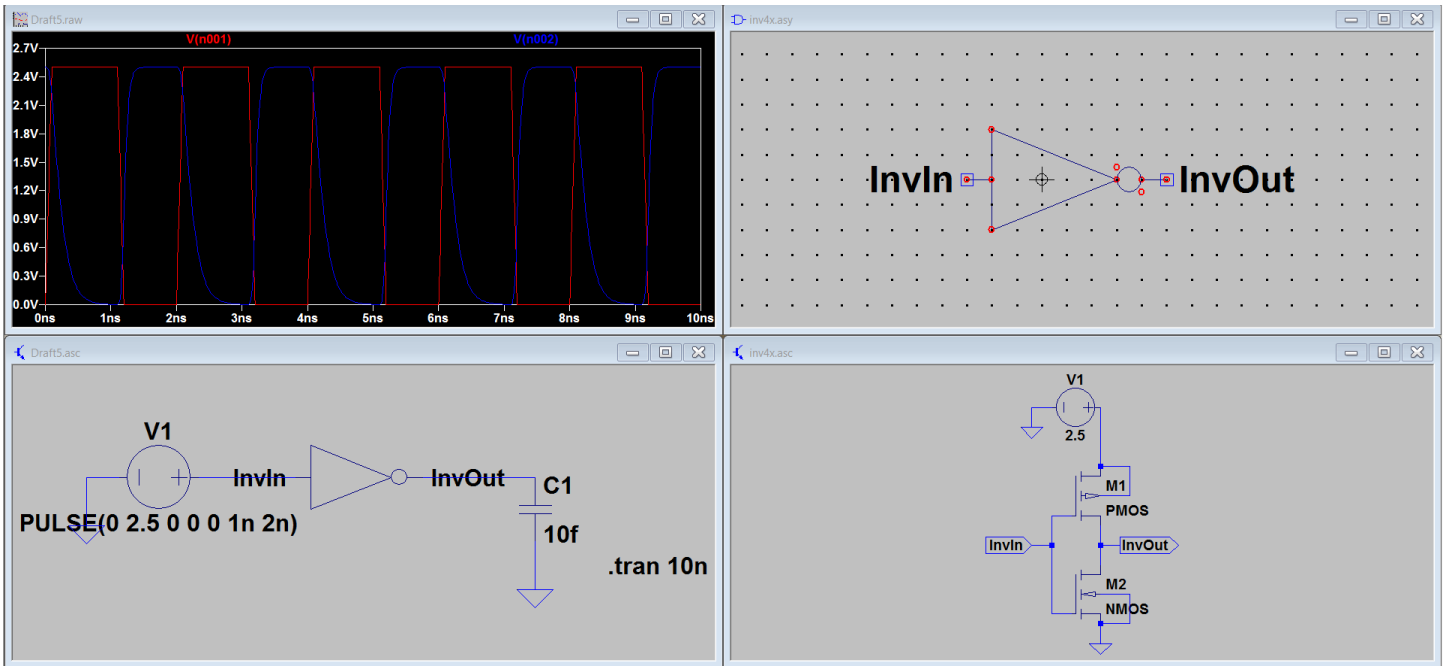

Figure 19: Symbol and circuit schematic of INV4X with its functional simulation

INV8X

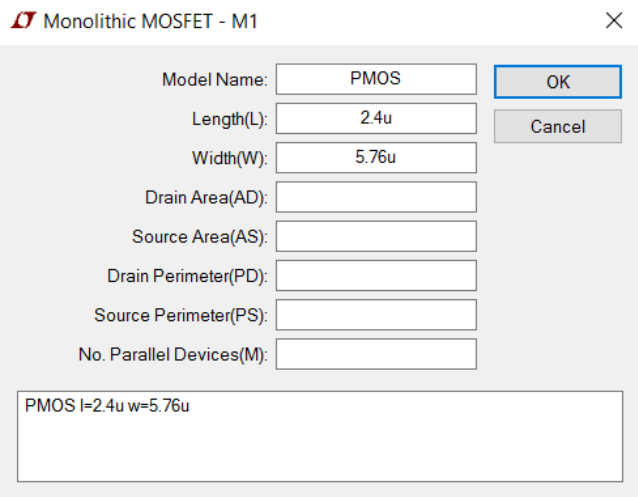

Figure 20: Size of PMOS (INV8X)

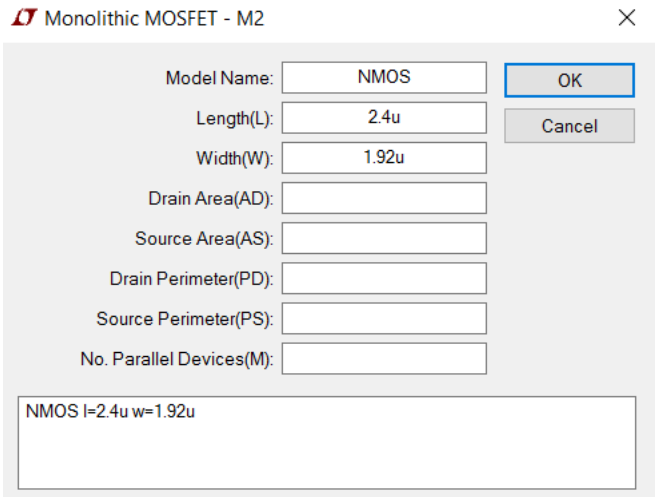

Figure 21: Size of NMOS (INV8X)

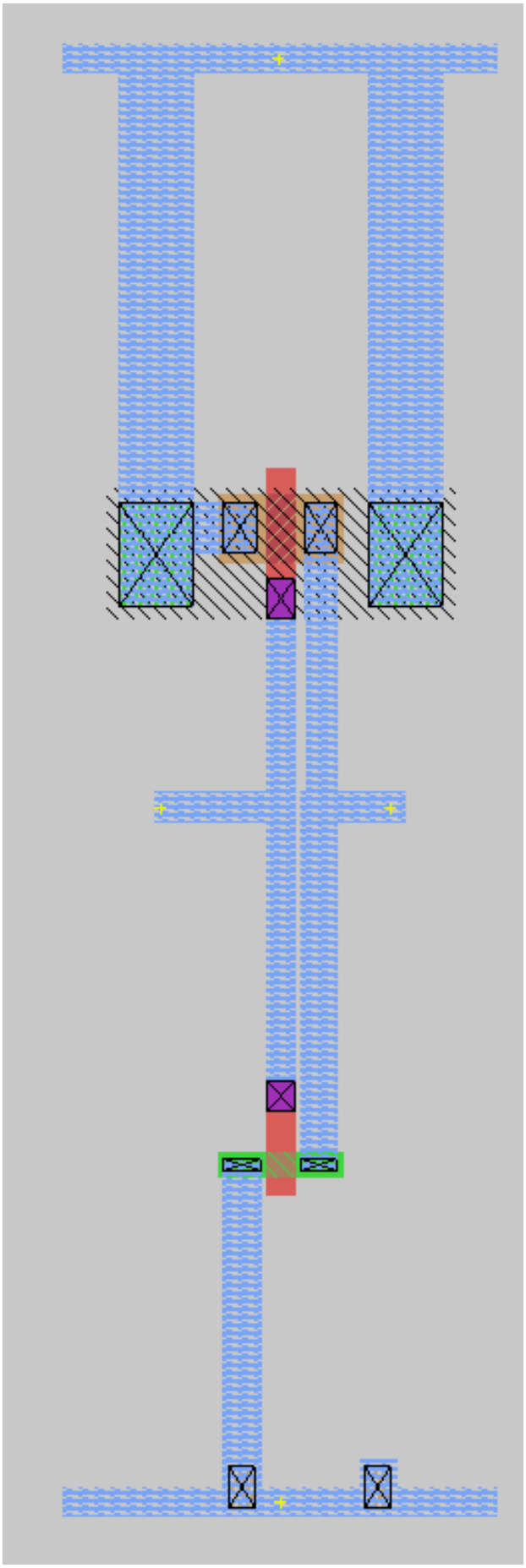

Figure 22: INV8X VLSI design in Magic

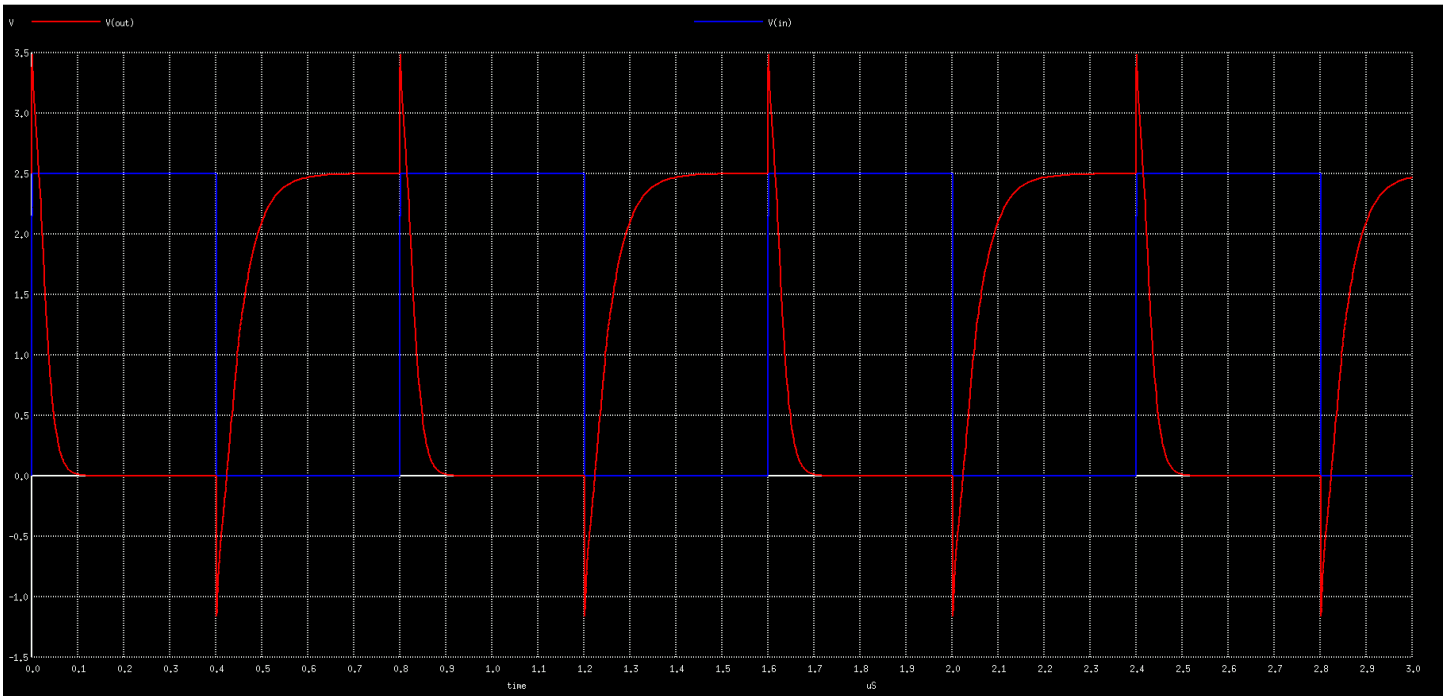

Figure 23: Functional simulation of INV8X

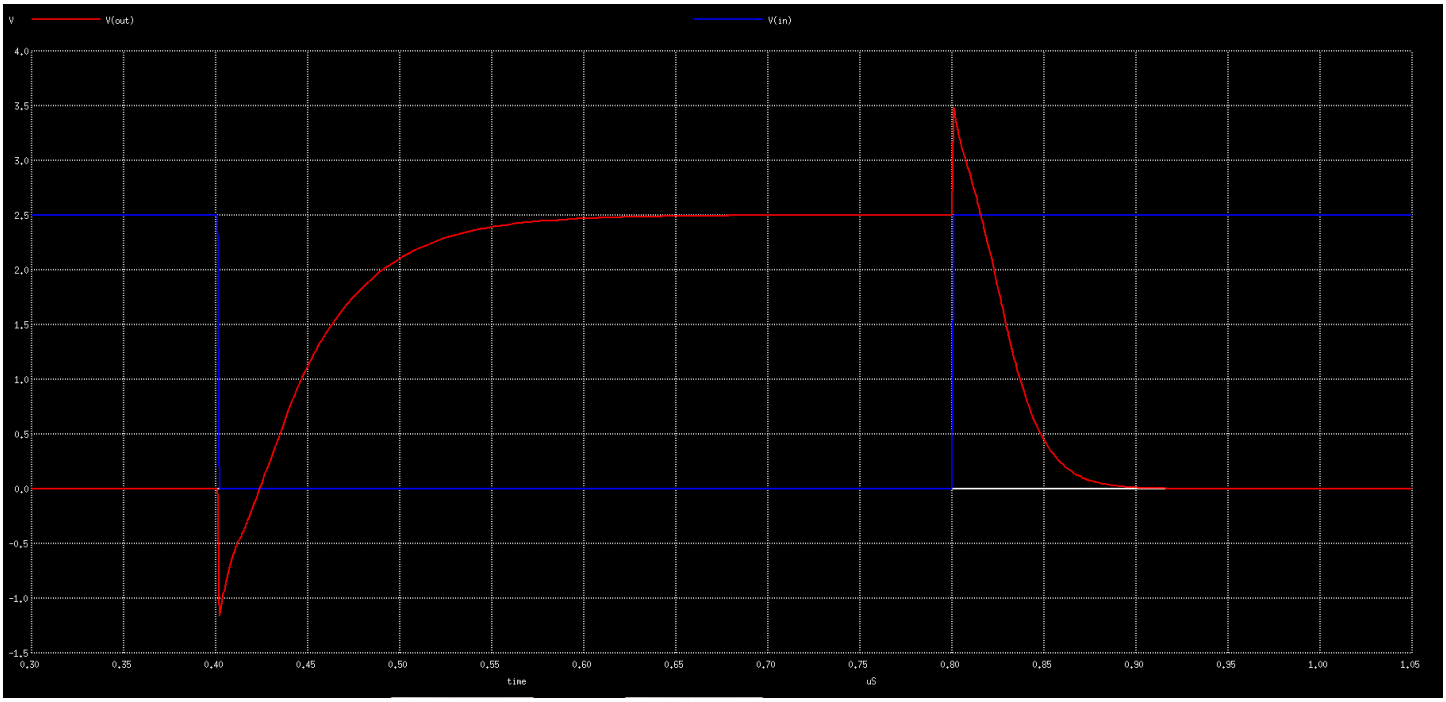

Figure 24: Fall/Rise time of INV8X

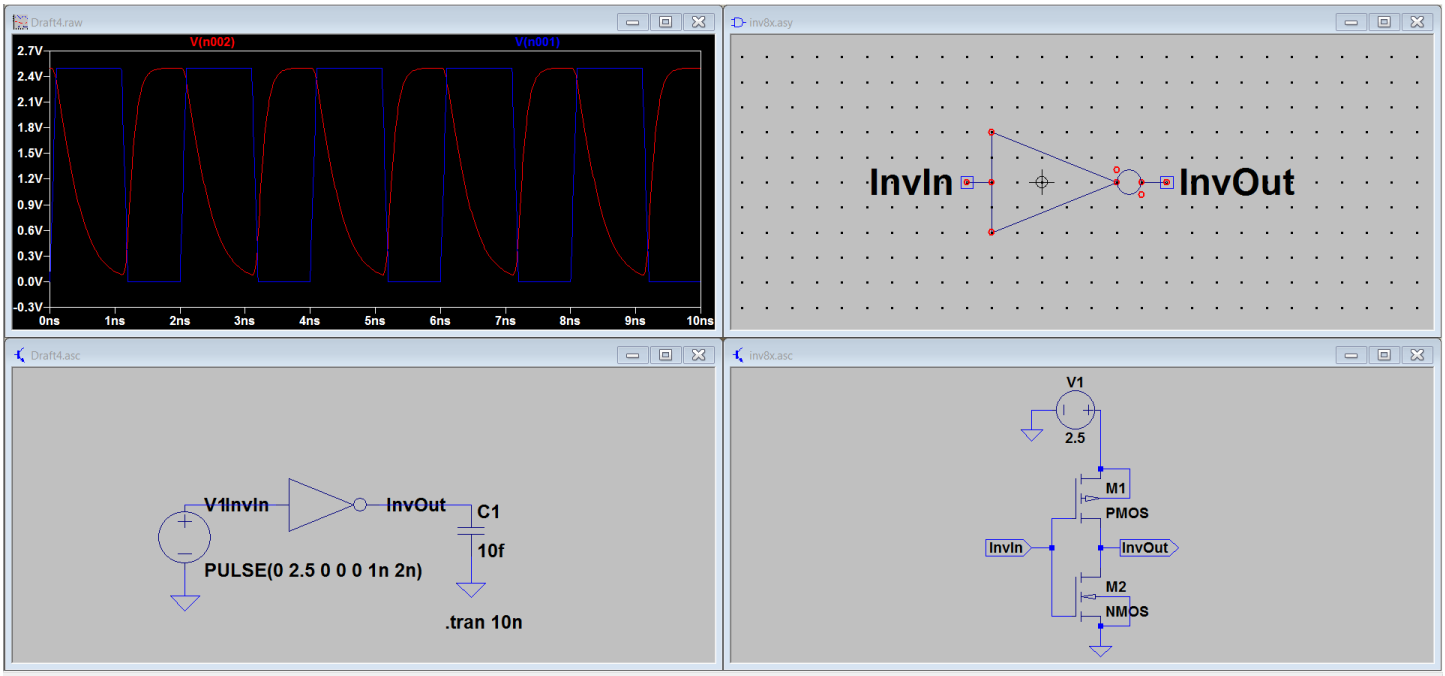

Figure 25: Symbol and circuit schematic of INV8X with its functional simulation

XOR

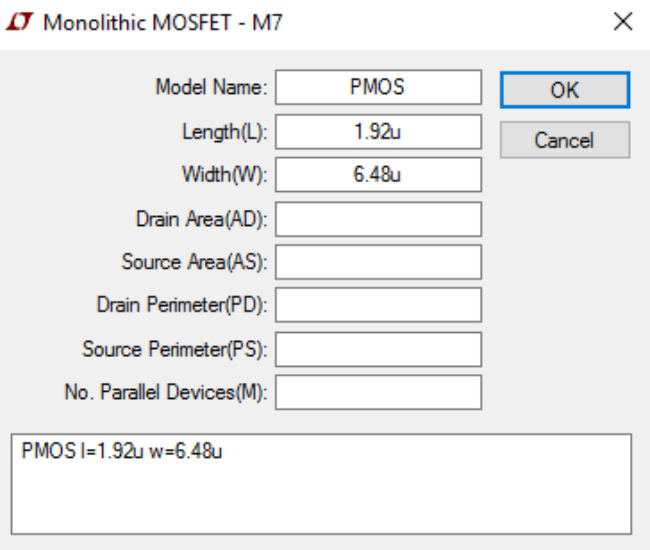

Figure 26: Size of PMOS (XOR)

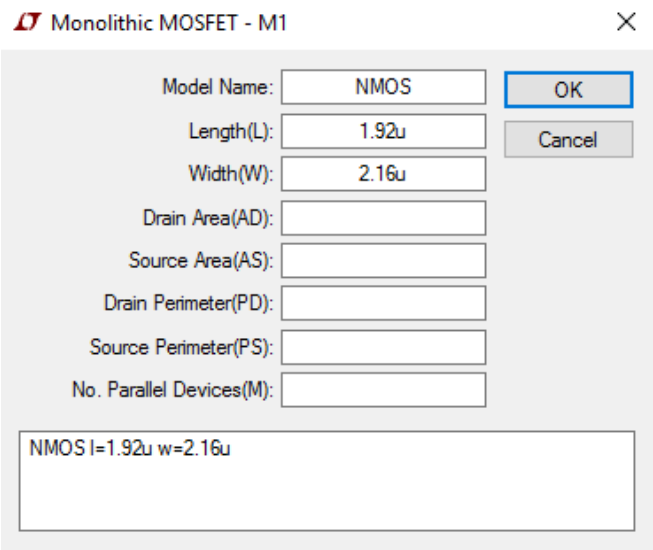

Figure 27: Size of NMOS (XOR)

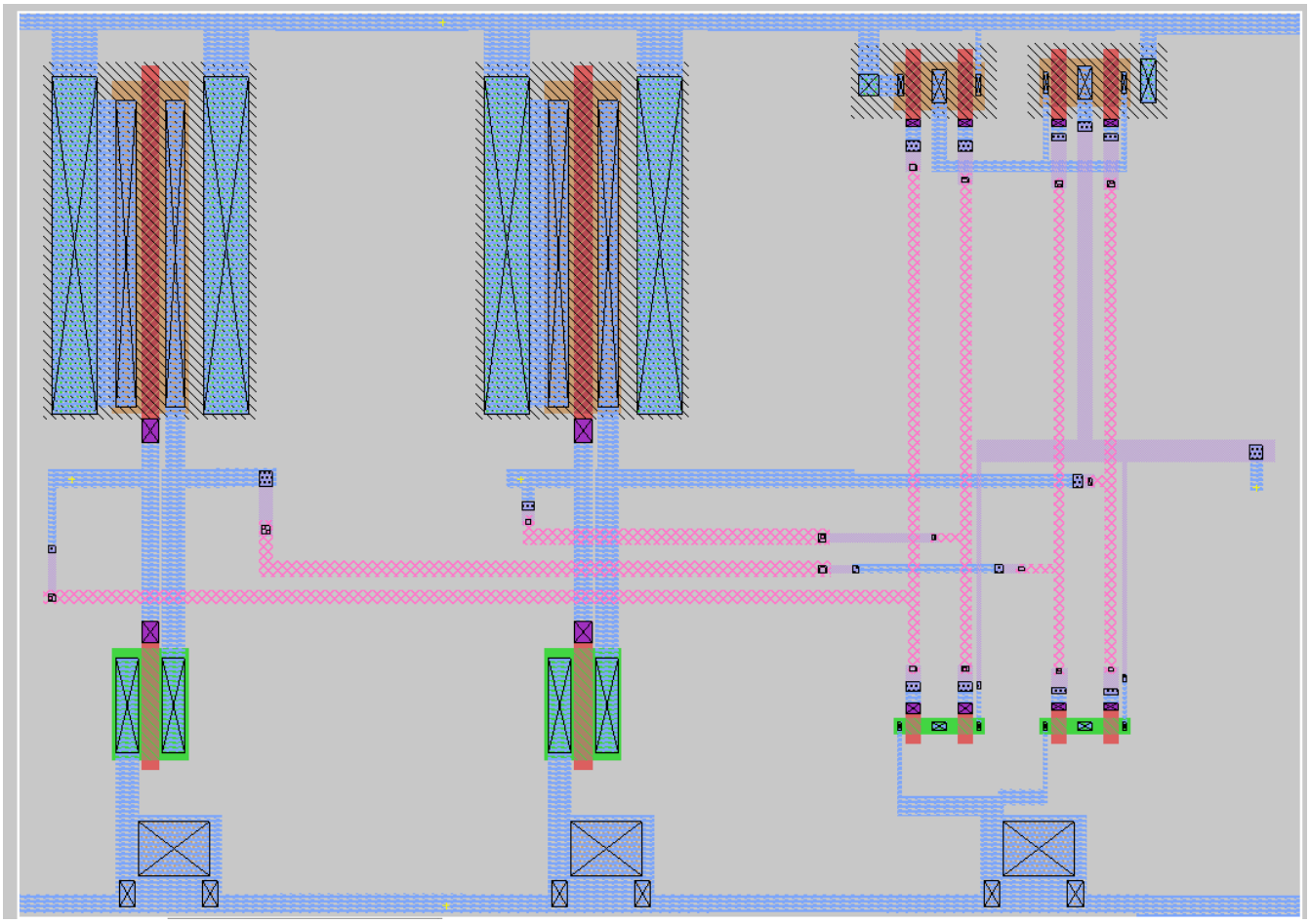

Figure 28: XOR VLSI design in Magic

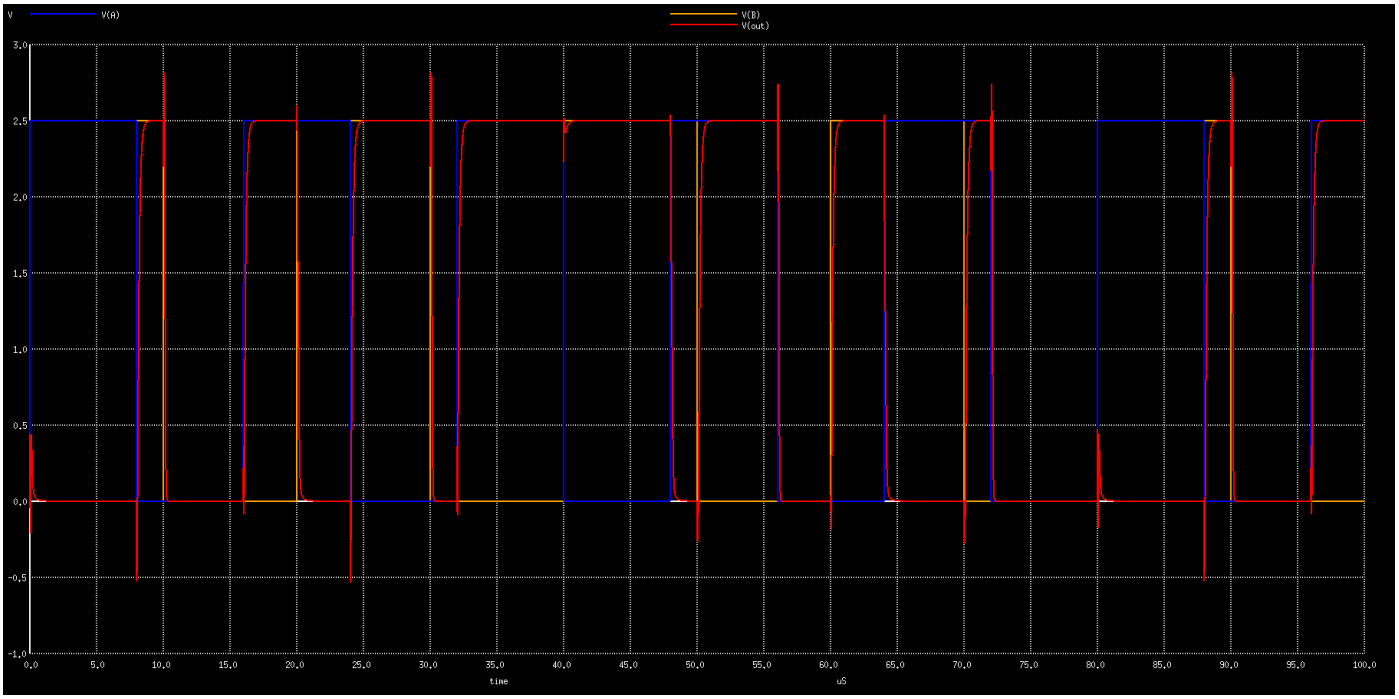

Figure 29: Functional simulation of XOR

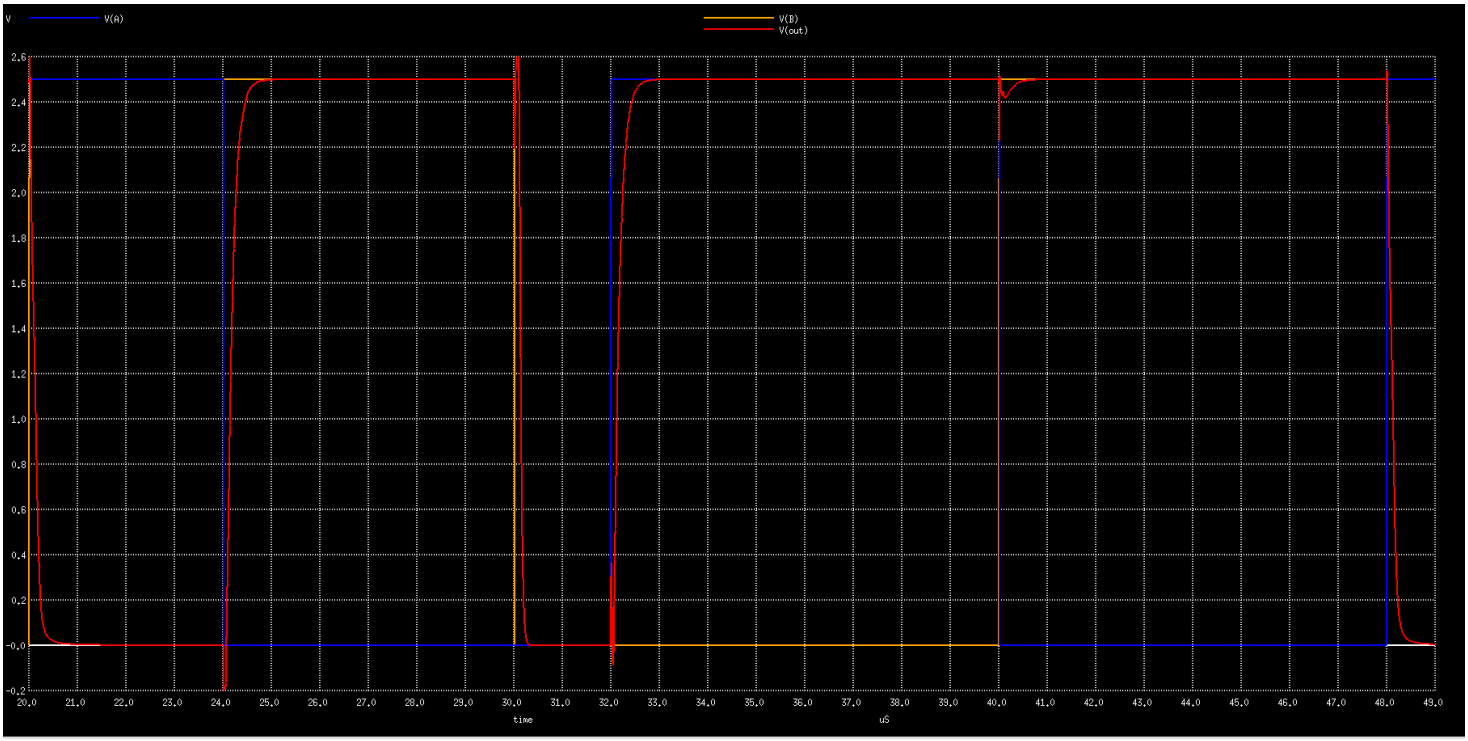

Figure 30: Fall/Rise time of XOR

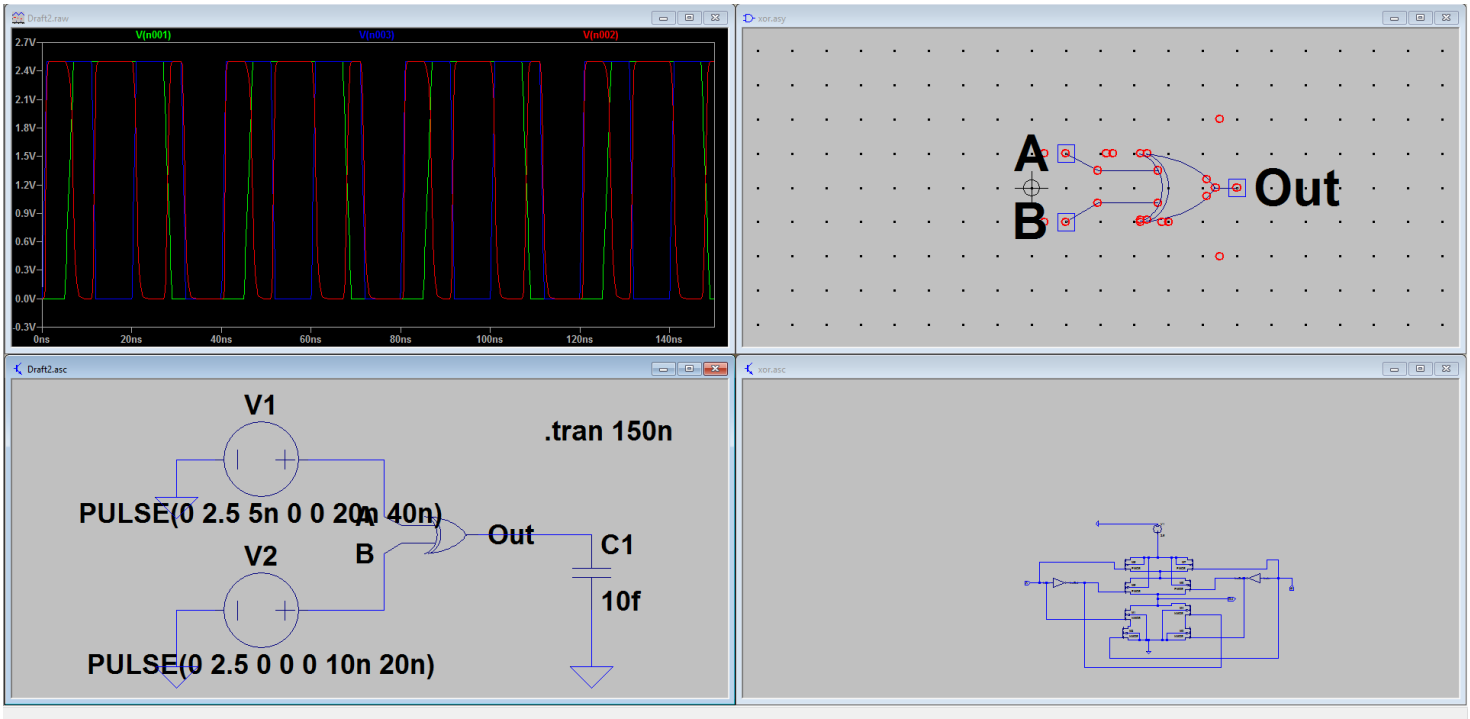

Figure 31: Symbol and circuit schematic of XOR with its functional simulation

XNOR

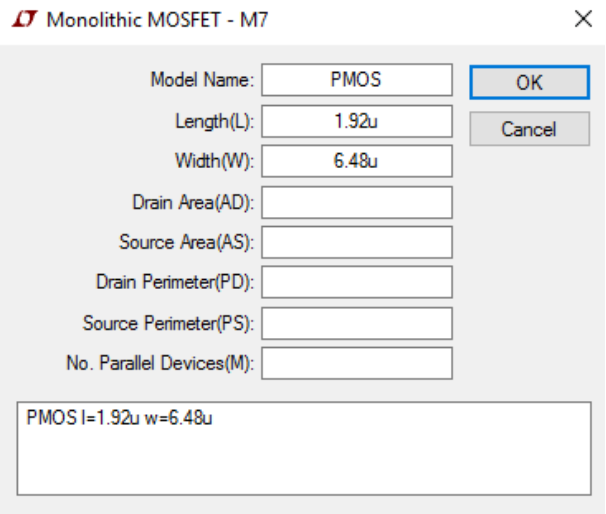

Figure 32: Size of PMOS (XNOR)

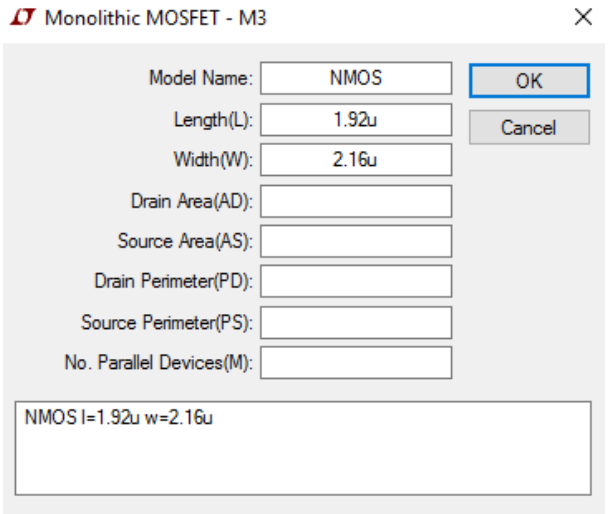

Figure 33: Size of NMOS (XNOR)

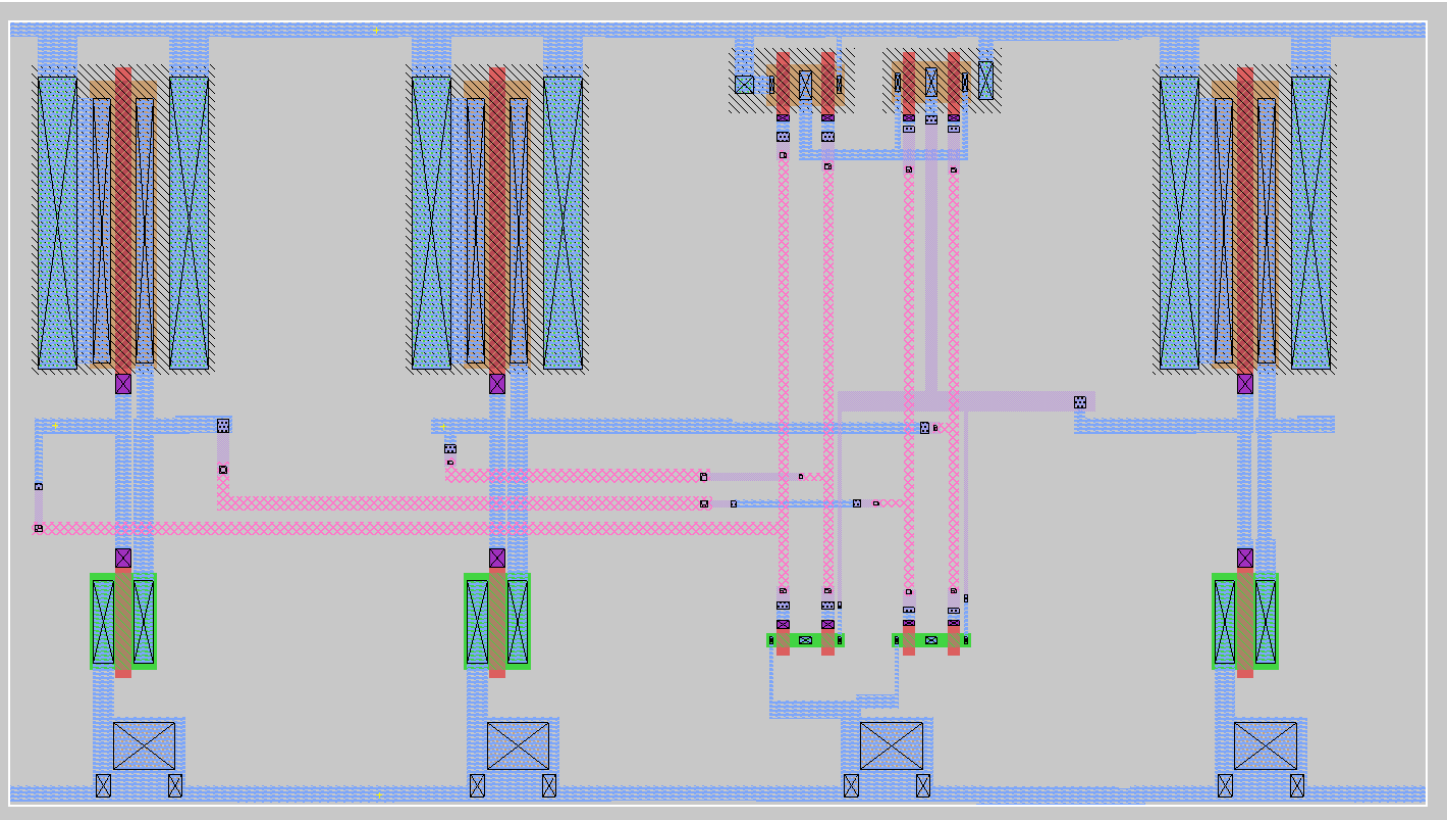

Figure 34: XNOR VLSI design in Magic

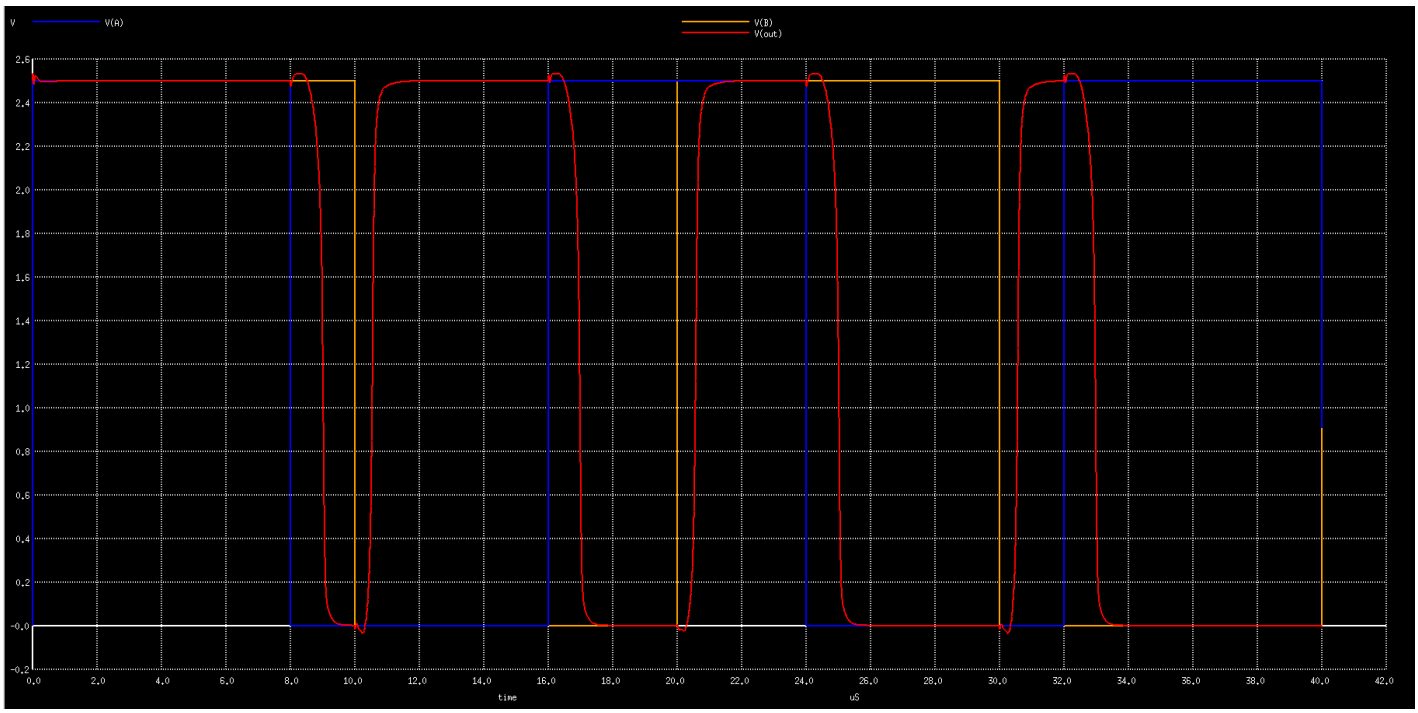

Figure 35: Functional simulation of XNOR

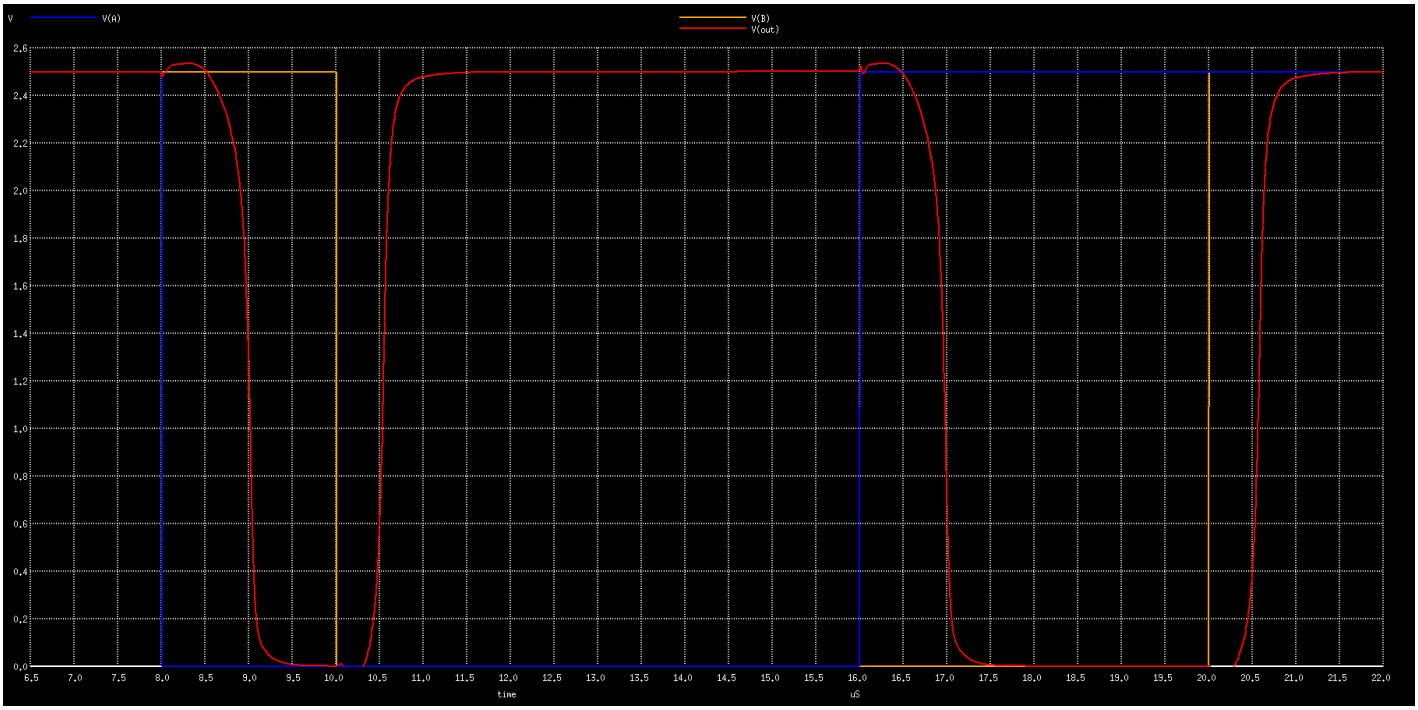

Figure 36: Fall/Rise time of XNOR

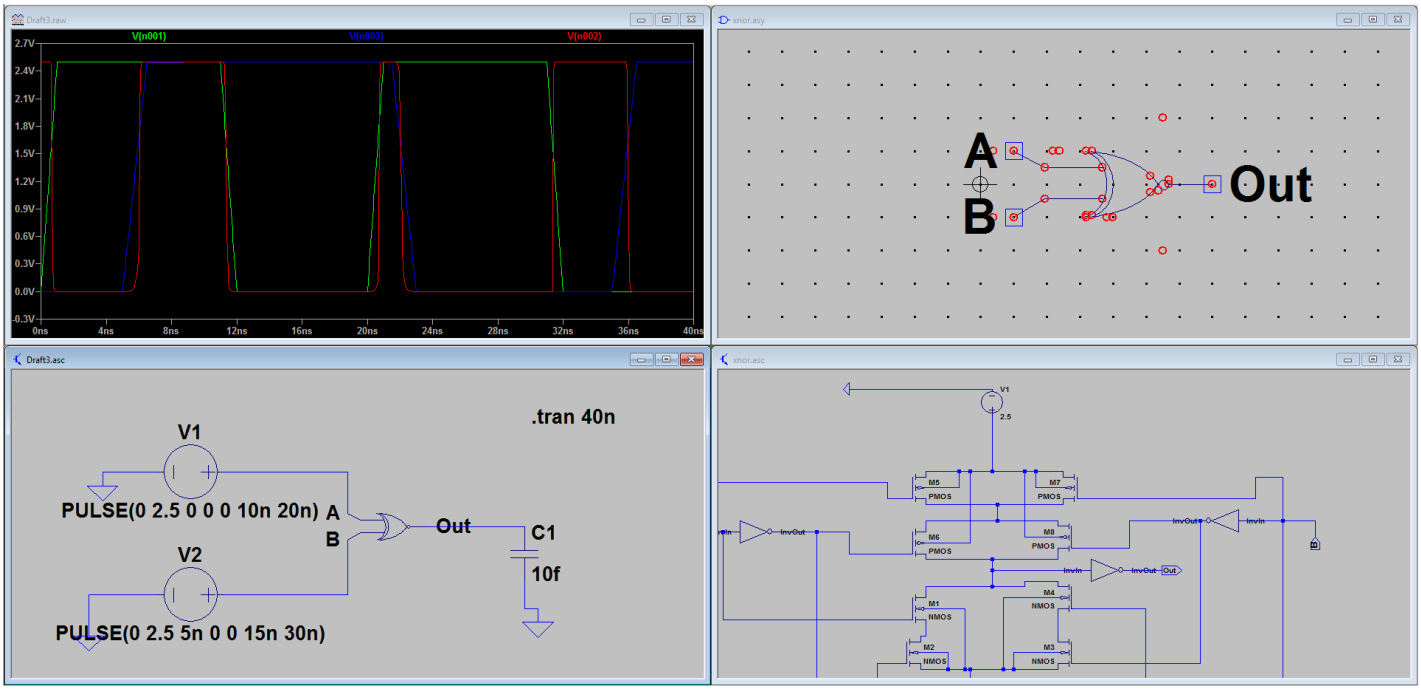

Figure 37: Symbol and circuit schematic of XNOR with its functional simulation

Transmission Gate

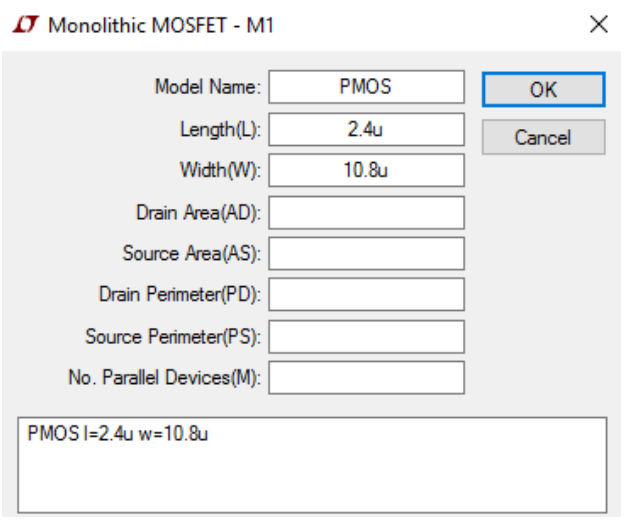

Figure 38: Size of PMOS (TX)

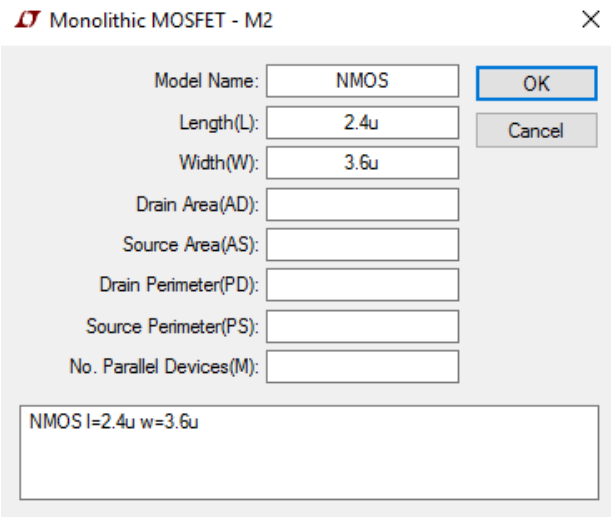

Figure 39: Size of NMOS (TX)

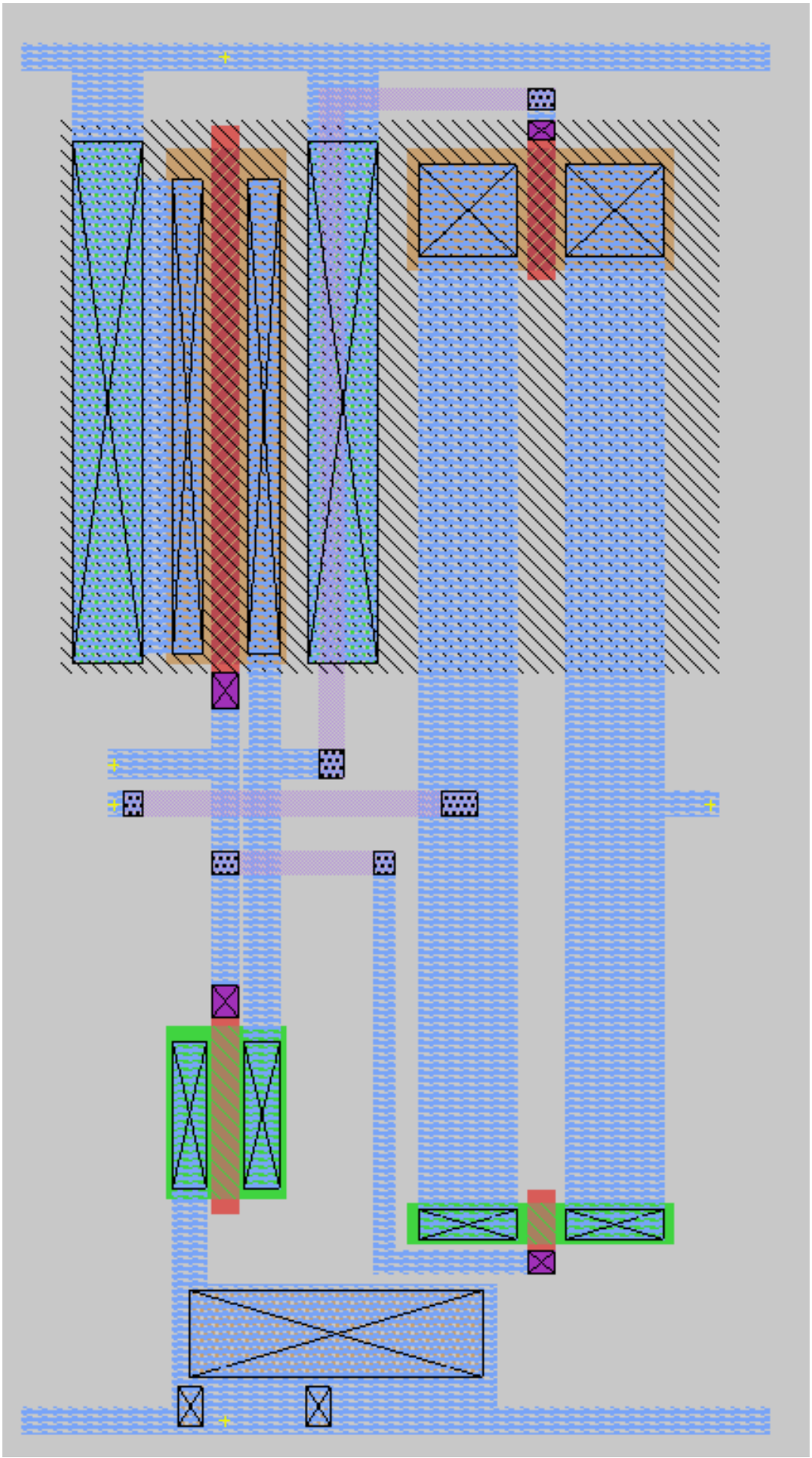

Figure 40: TX VLSI design in Magic

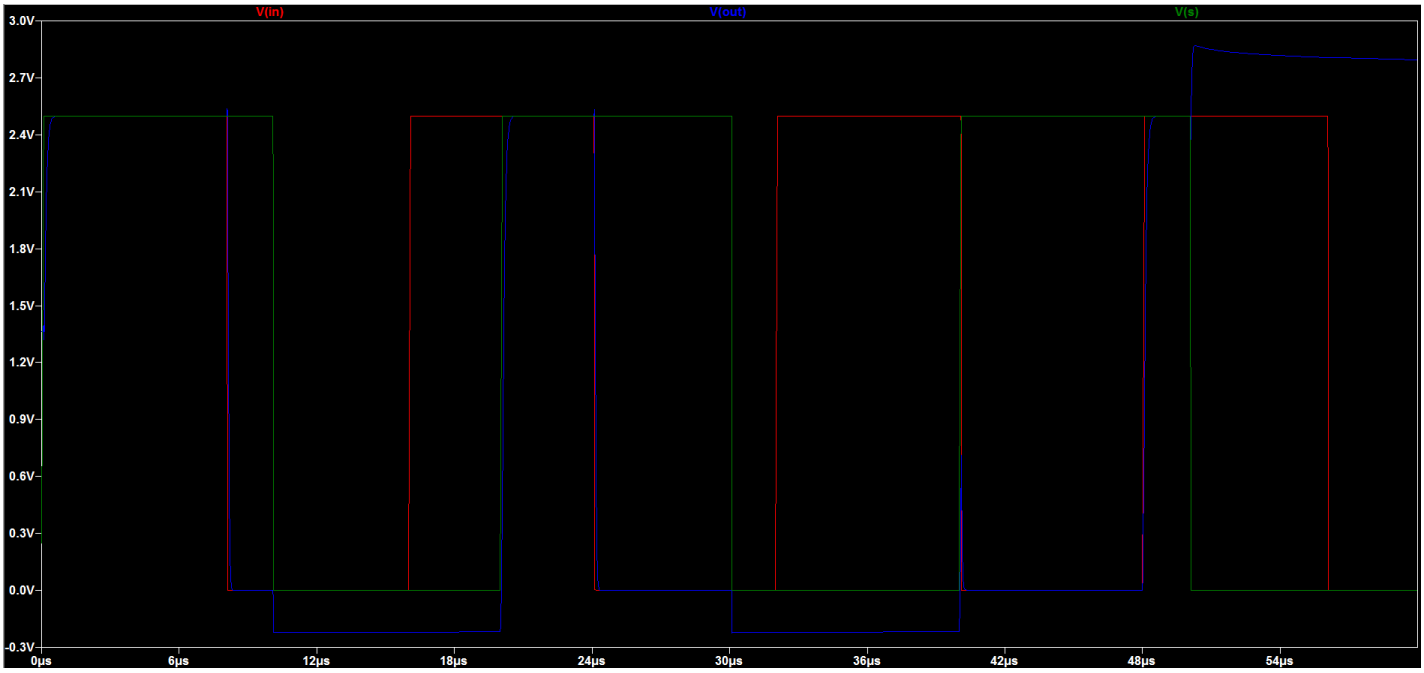

Figure 41: Functional simulation of TX

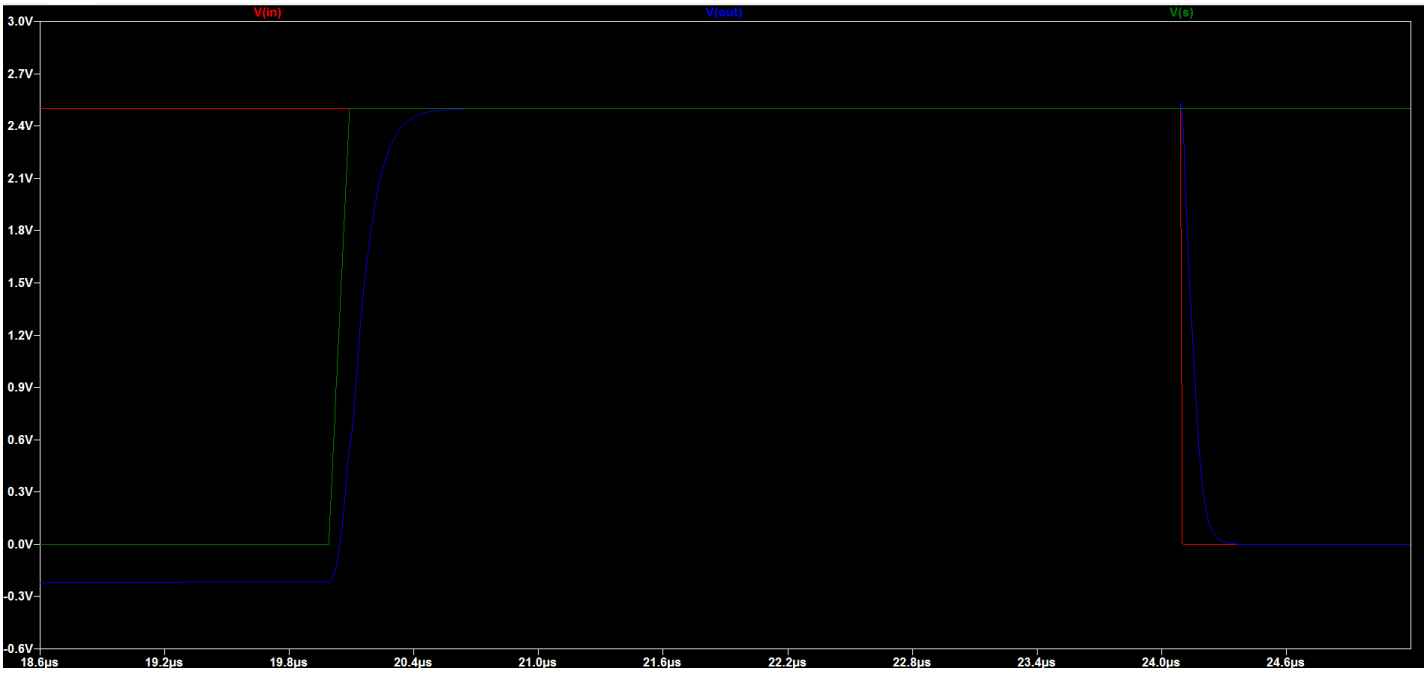

Figure 42: Fall/Rise time of TX

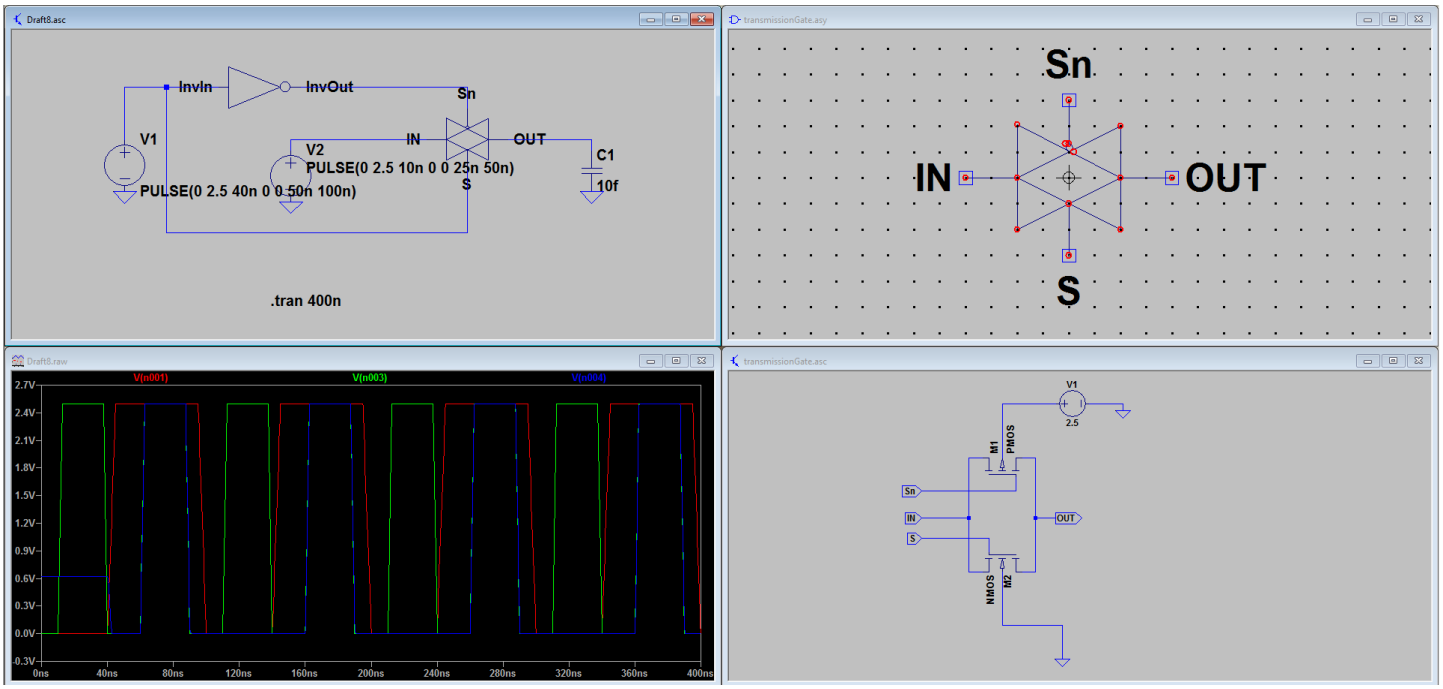

Figure 43: Symbol and circuit schematic of TX with its functional simulation

MUX2X1

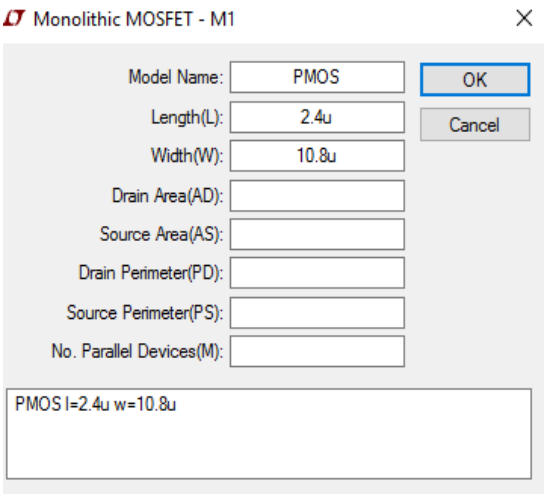

Figure 44: Size of PMOS (MUX2X1)

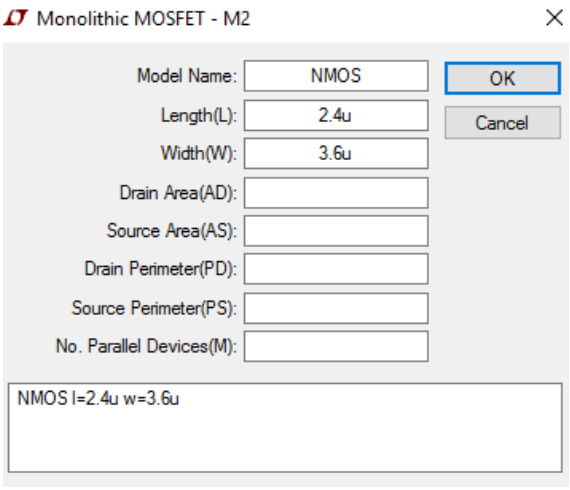

Figure 45: Size of NMOS (MUX2X1)

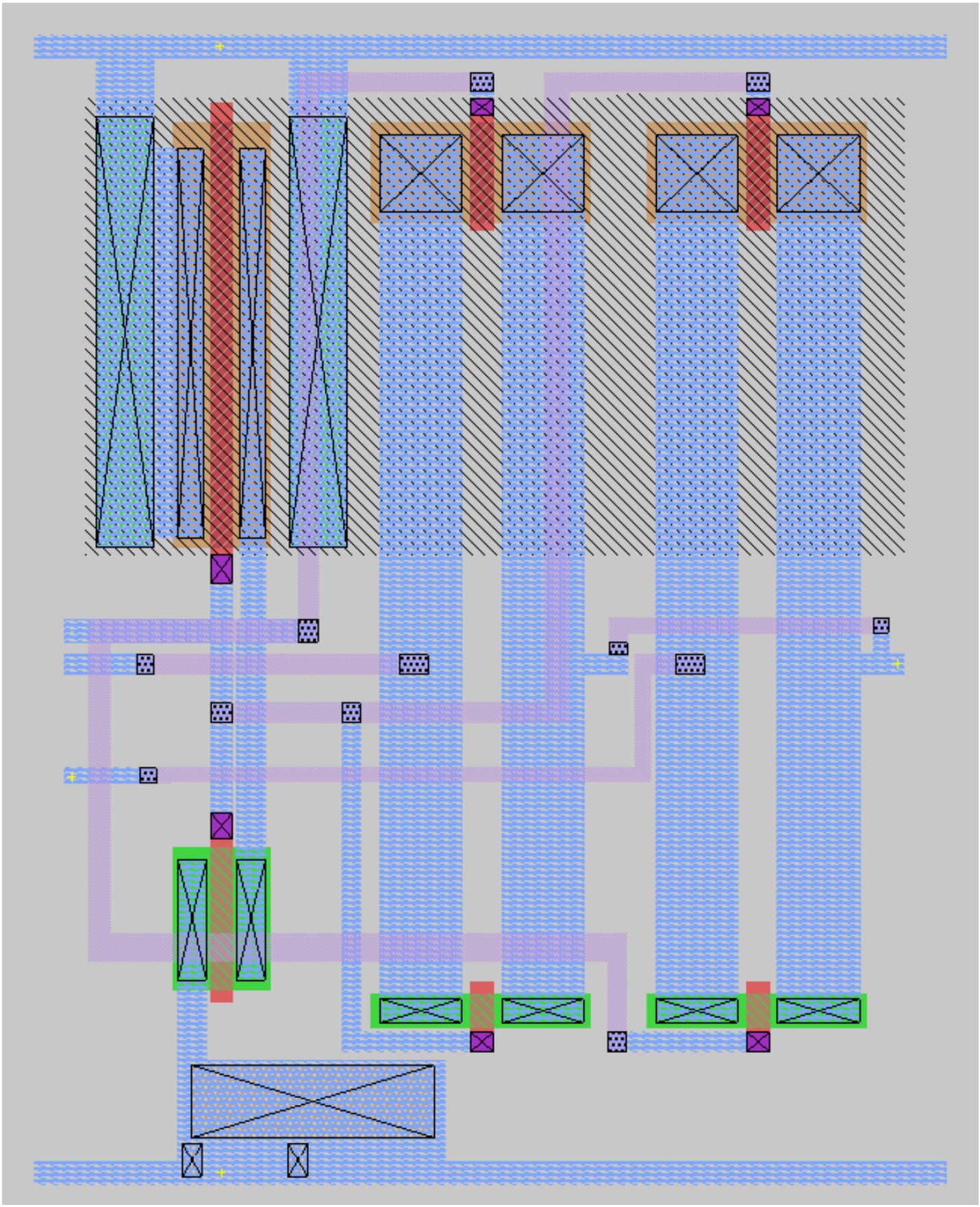

Figure 46: MUX2X1 VLSI design in Magic

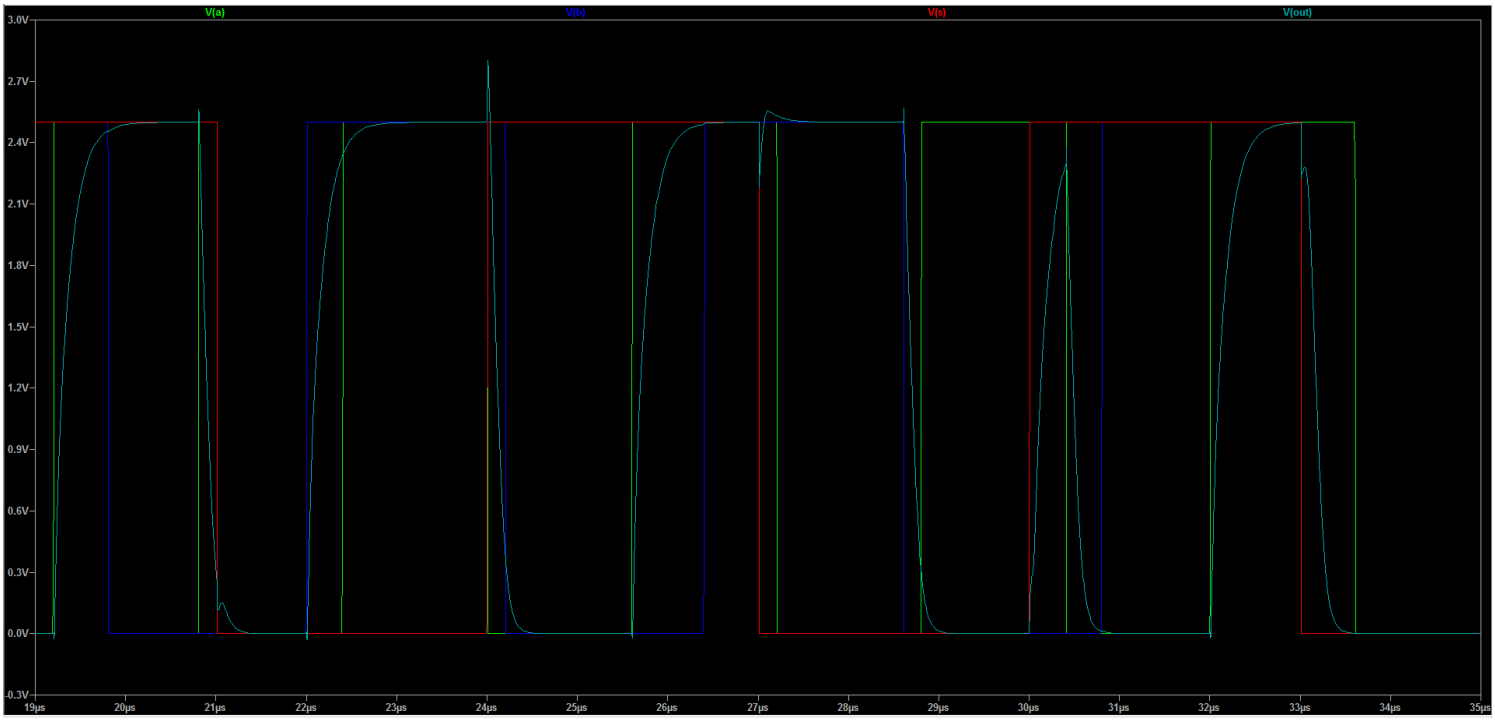

Figure 47: Functional simulation of MUX2X1

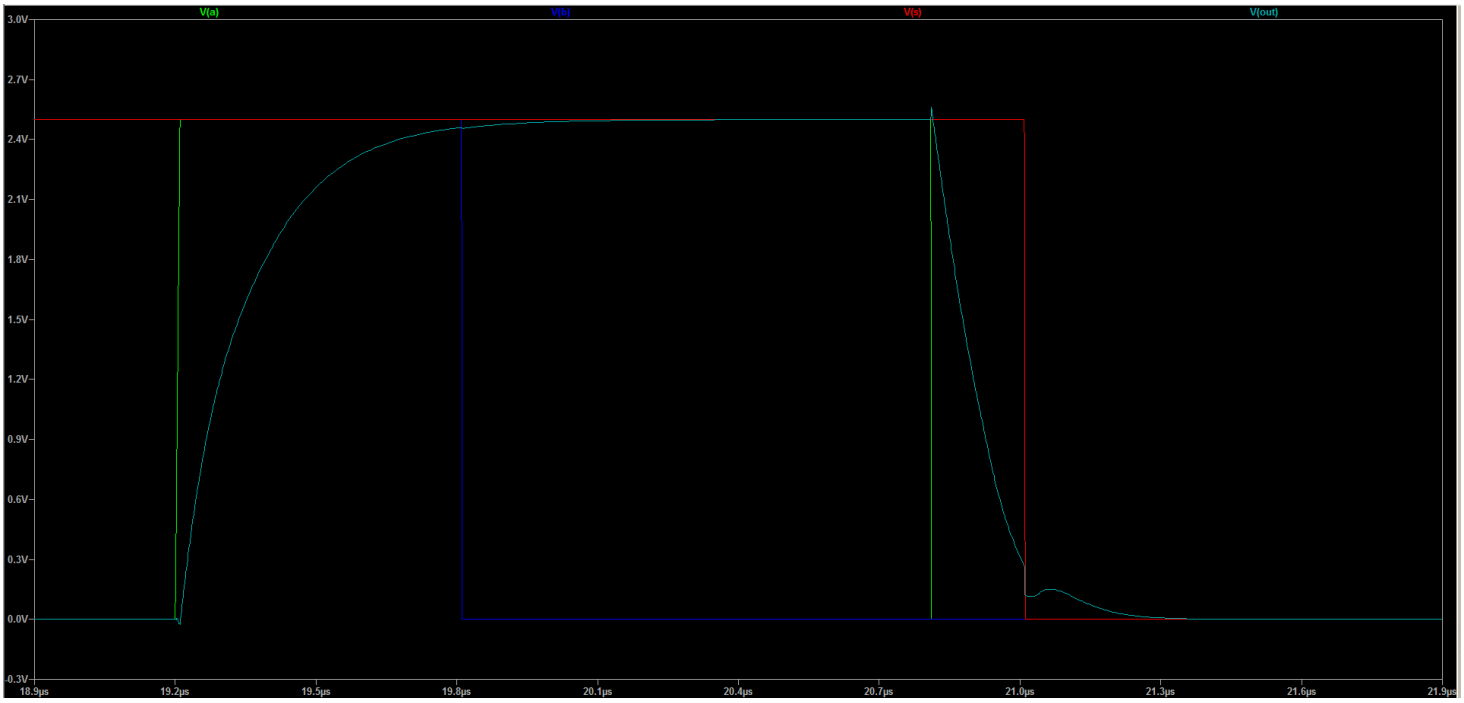

Figure 48: Fall/Rise time of MUX2X1

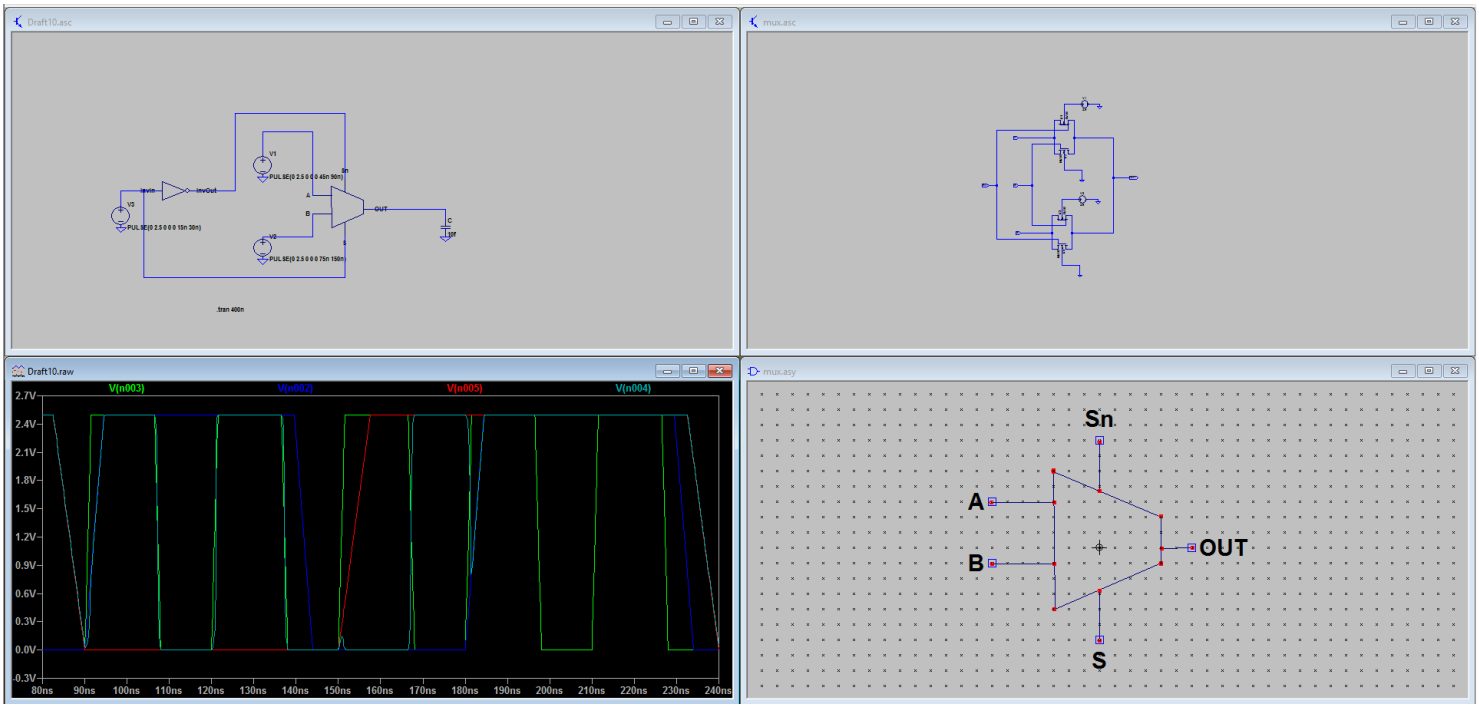

Figure 49: Symbol and circuit schematic of MUX2X1 with its functional simulation

DFF

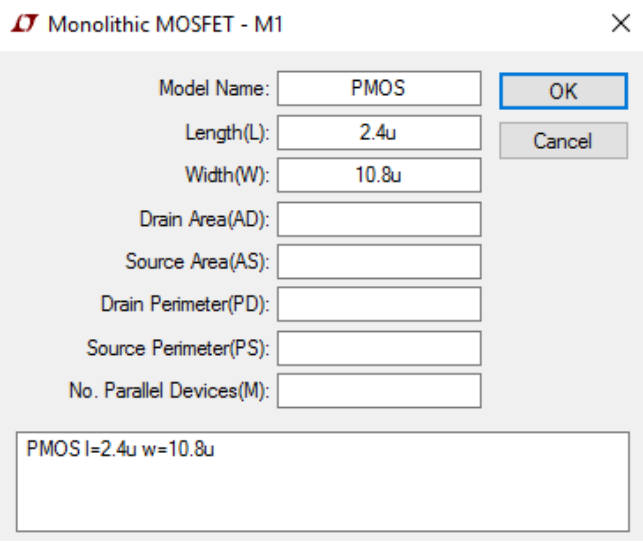

Figure 50: Size of PMOS (DFF)

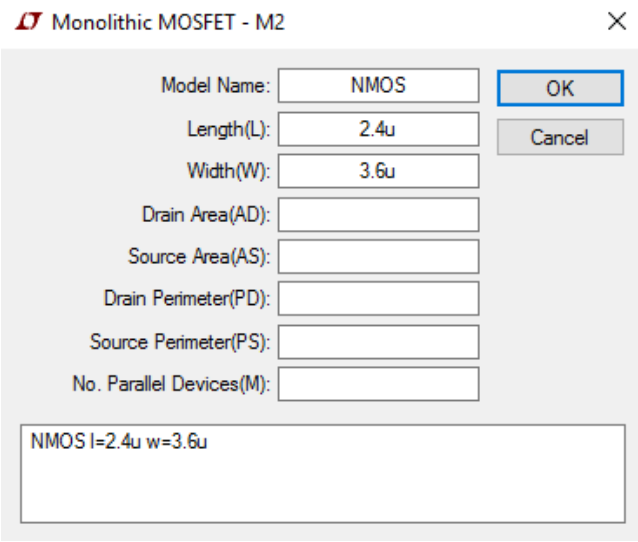

Figure 51: Size of NMOS (DFF)

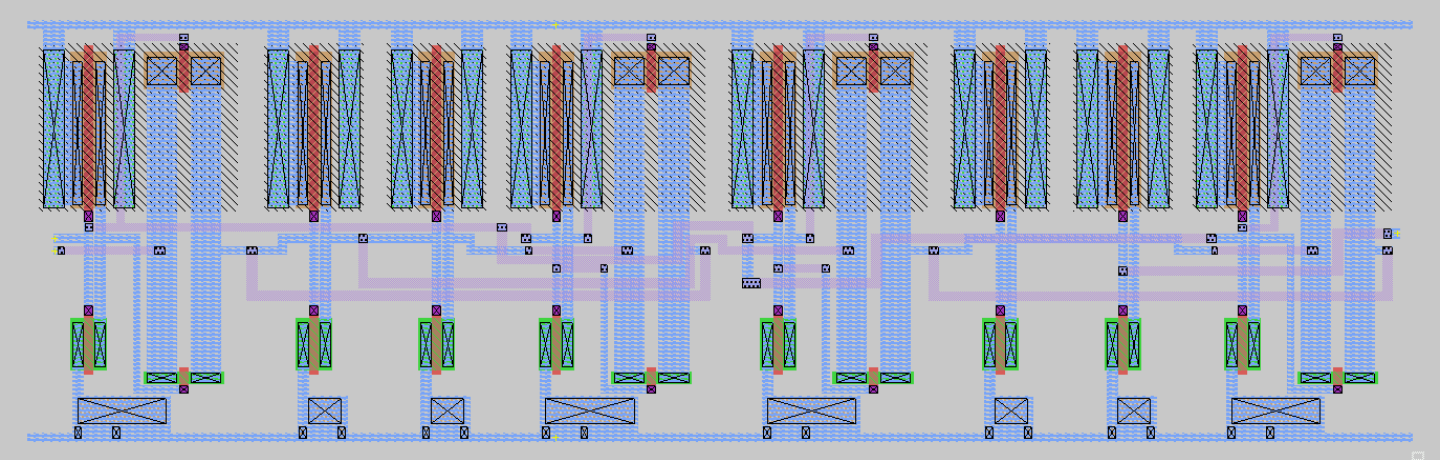

Figure 52: DFF VLSI design in Magic

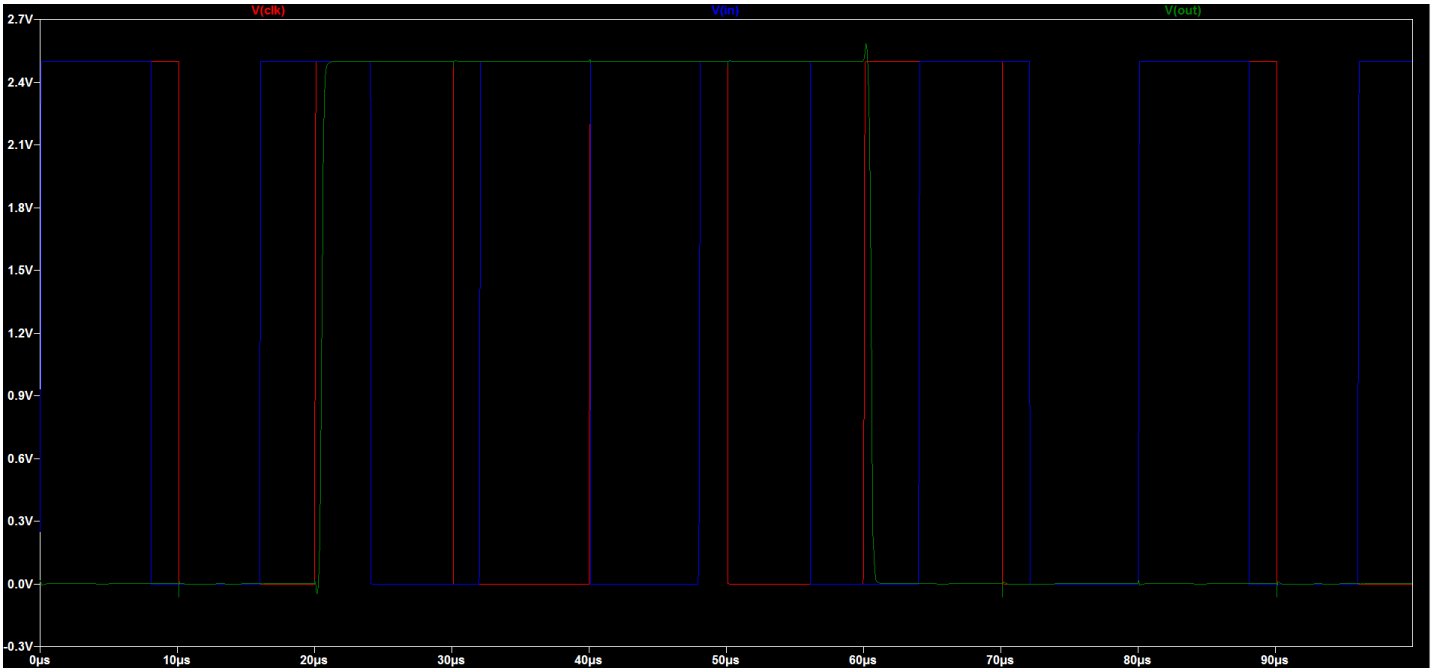

Figure 53: Functional simulation of DFF

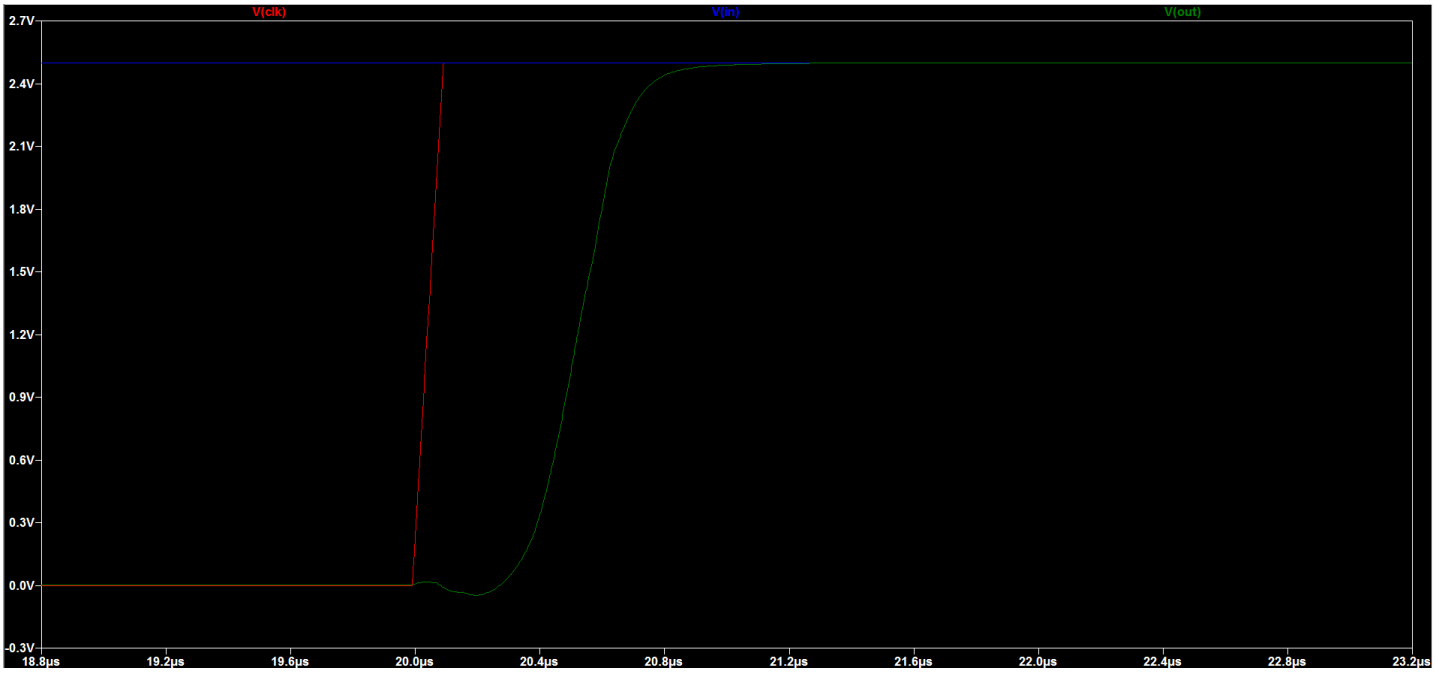

Figure 54: Rise time of DFF

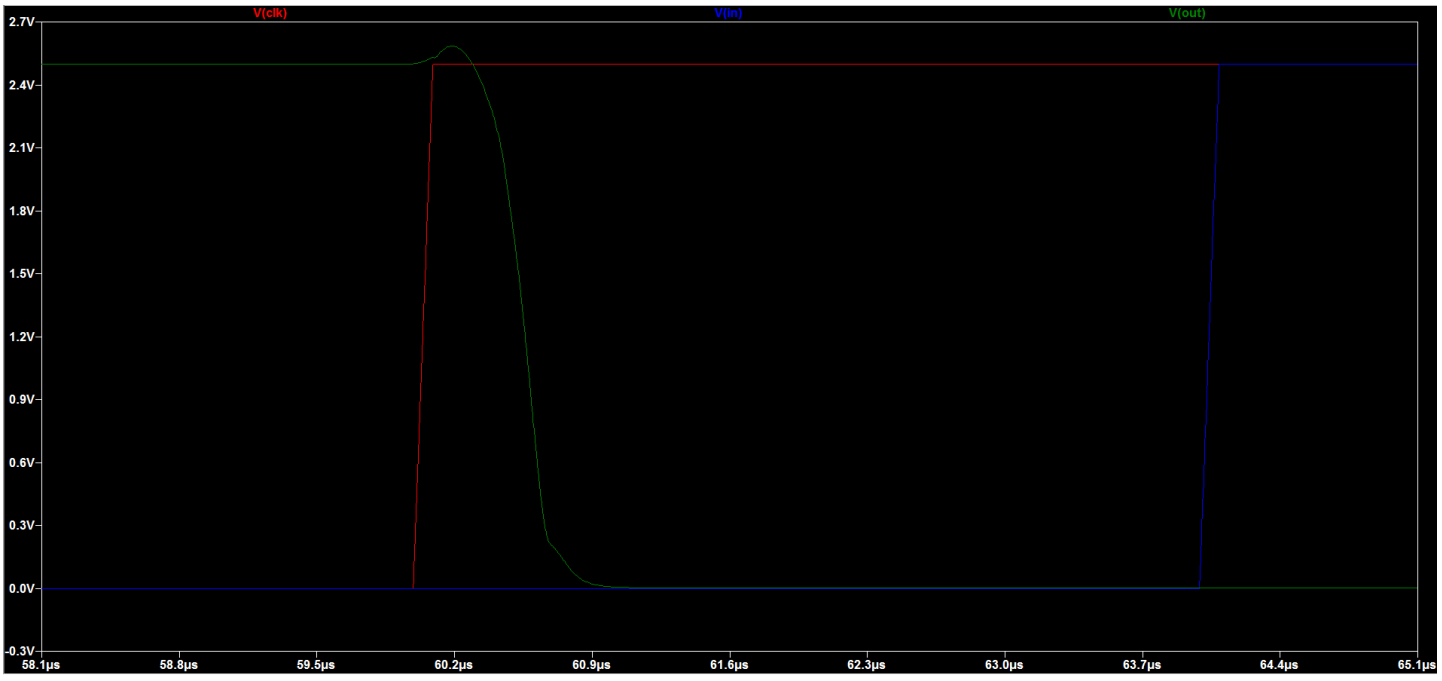

Figure 55: Fall time of DFF

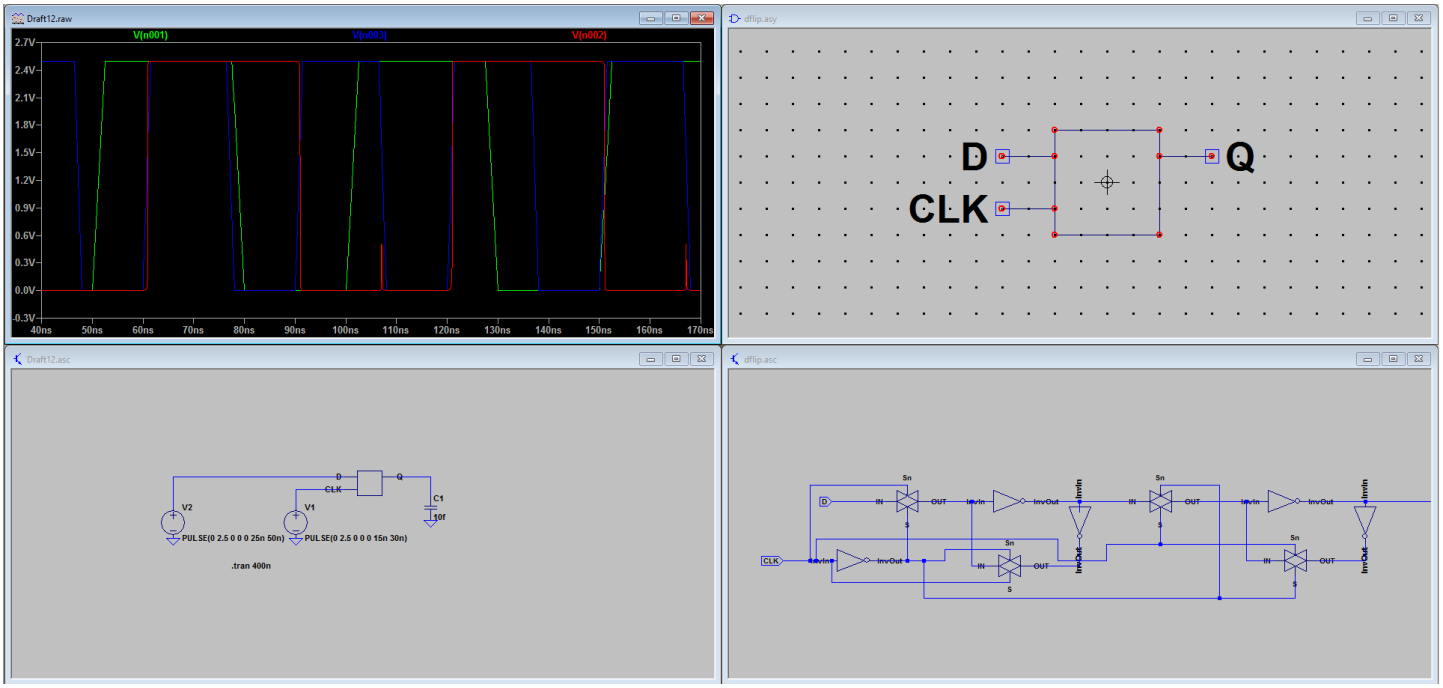

Figure 56: Symbol and circuit schematic of DFF with its functional simulation

NOR2X1

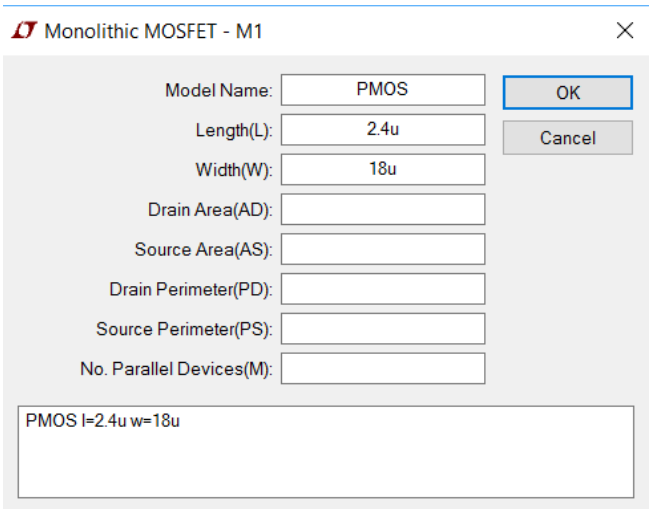

Figure 57: Size of PMOS (NOR2X1)

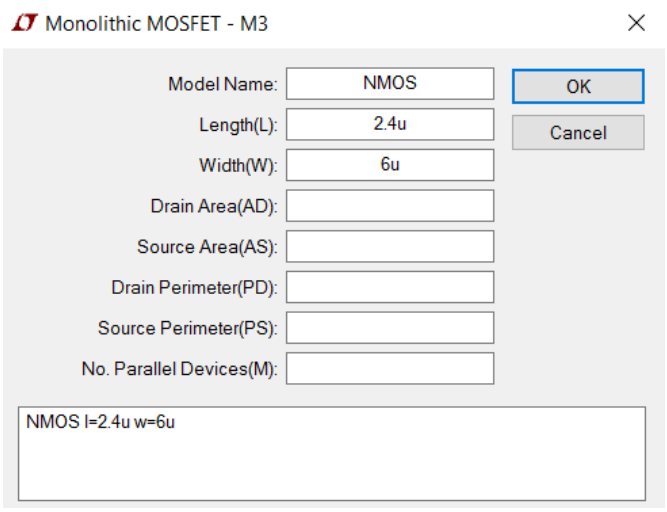

Figure 58: Size of NMOS (NOR2X1)

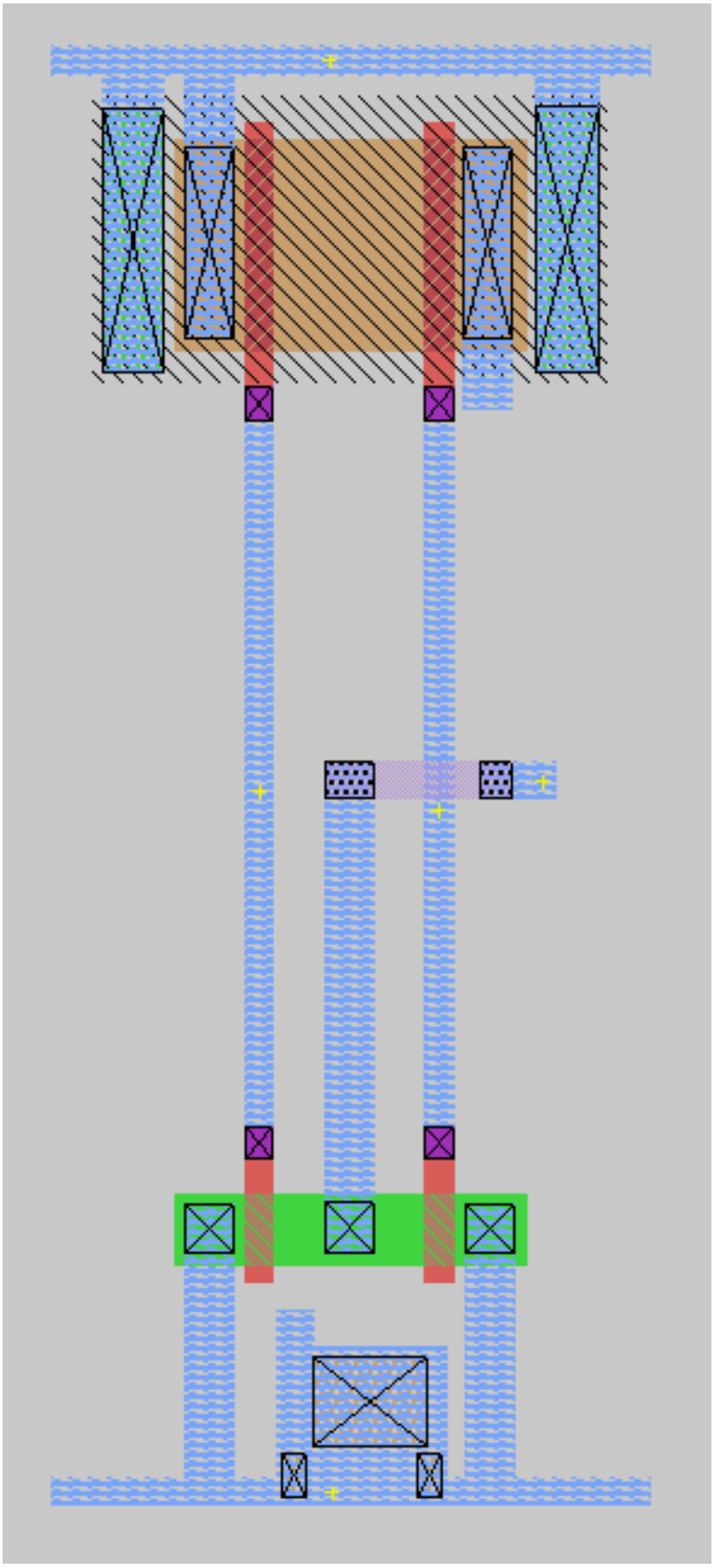

Figure 59: NOR2X1 VLSI design in Magic

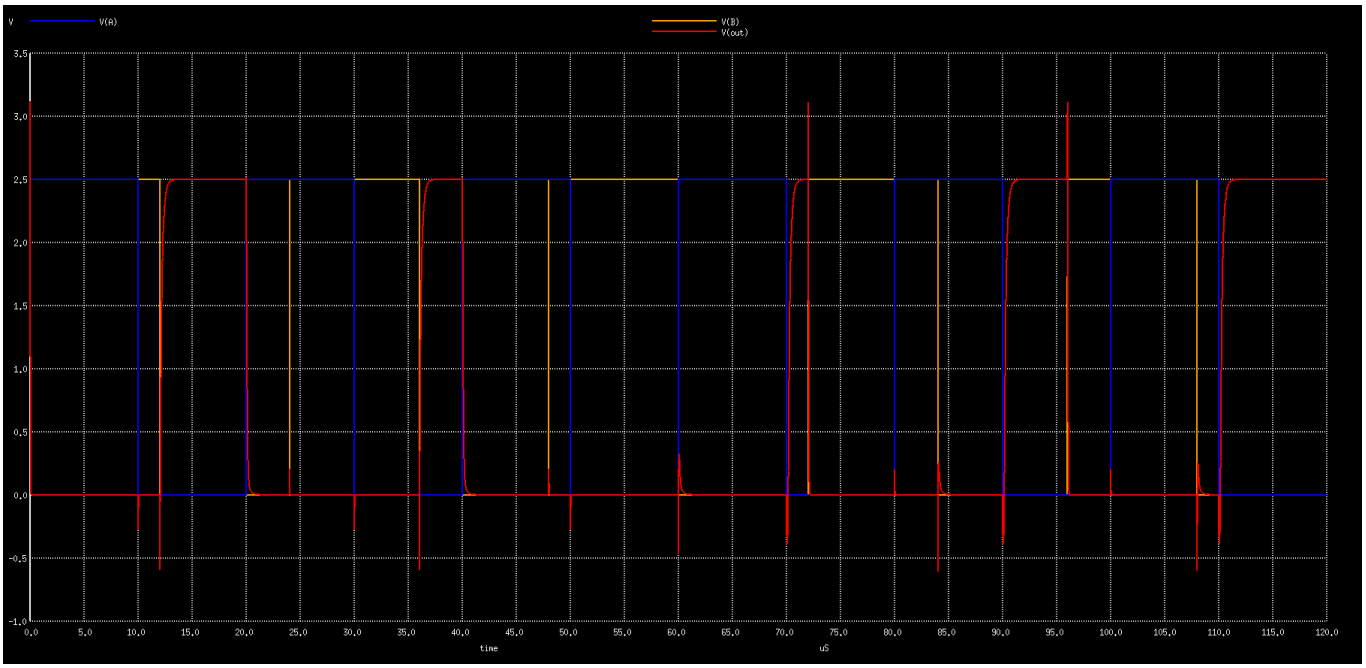

Figure 60: Functional simulation of NOR2X1

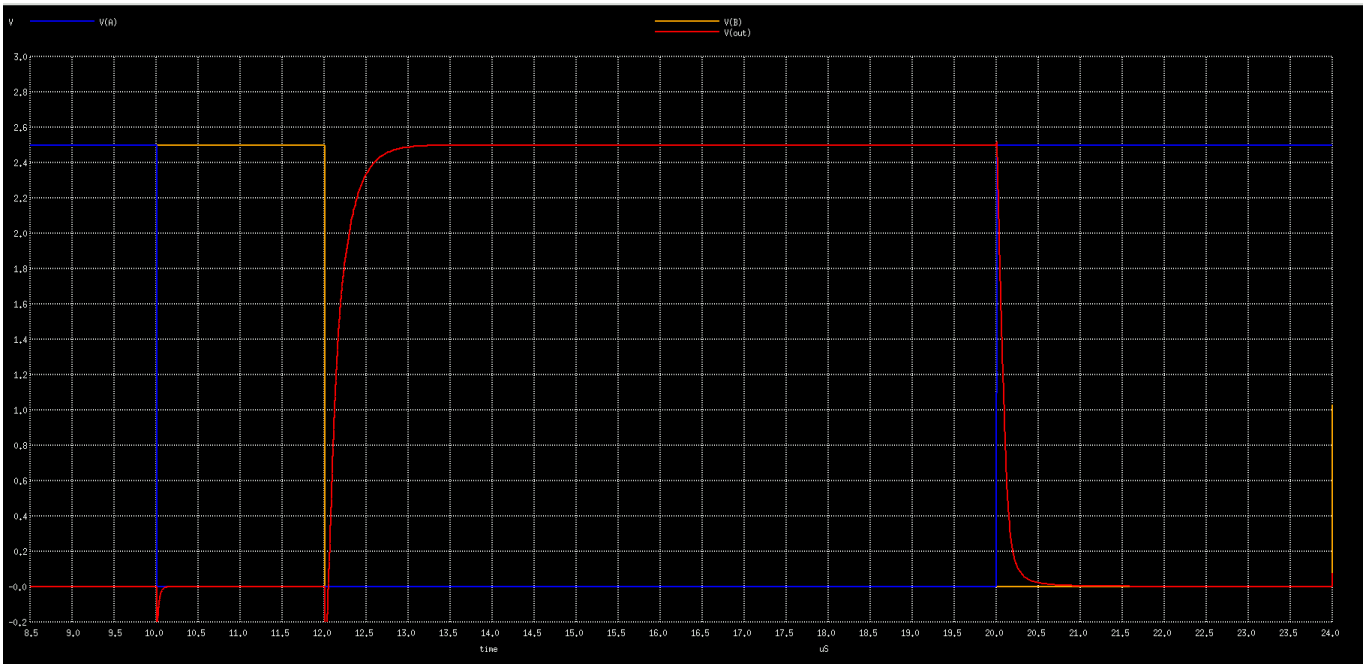

Figure 61: Fall/Rise time of NOR2X1

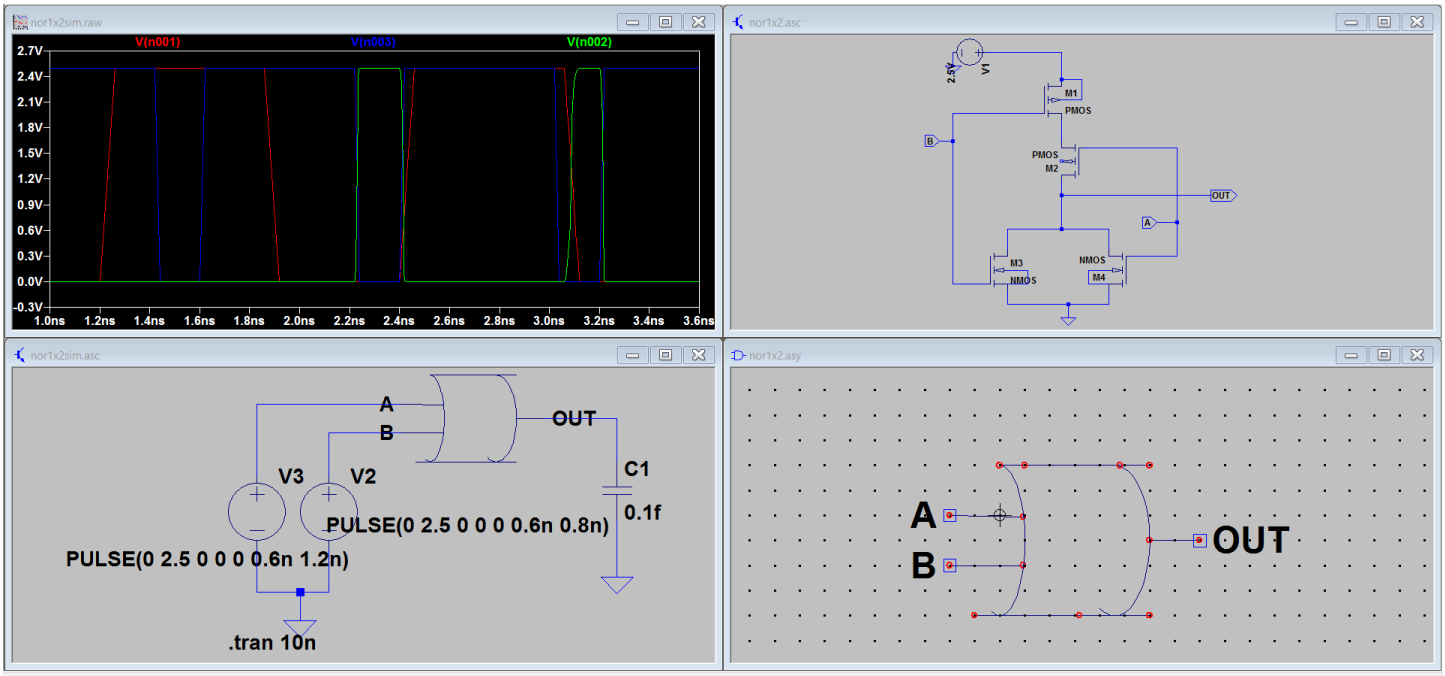

Figure 62: Symbol and circuit schematic of NOR2X1 with its functional simulation

NOR3X1

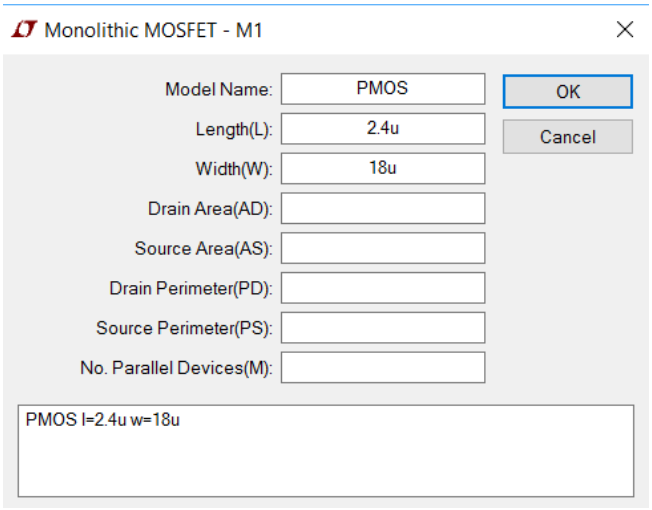

Figure 63: Size of PMOS (NOR3X1)

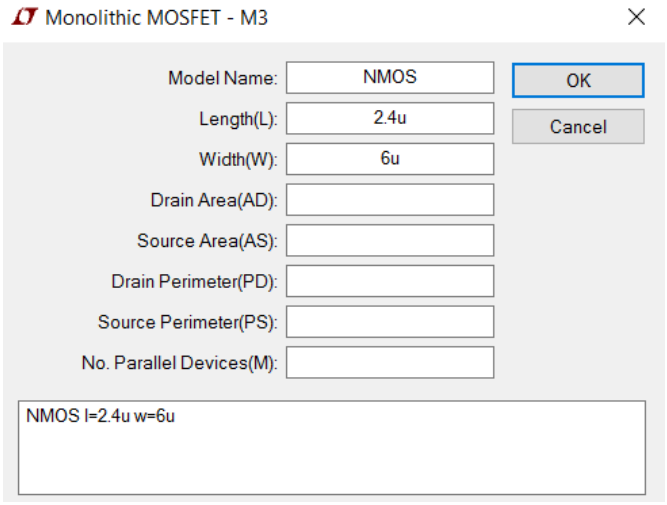

Figure 64: Size of NMOS (NOR3X1)

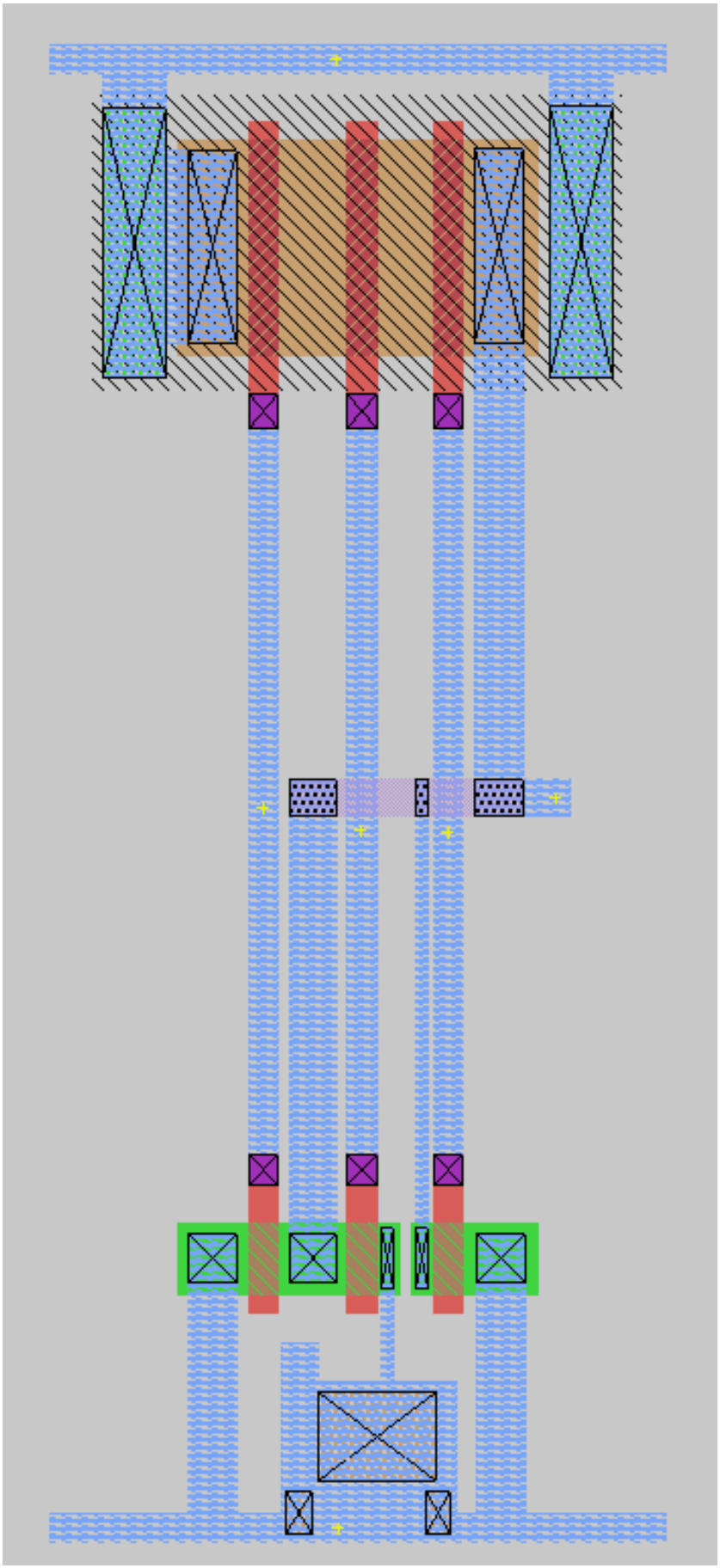

Figure 65: NOR3X1 VLSI design in Magic

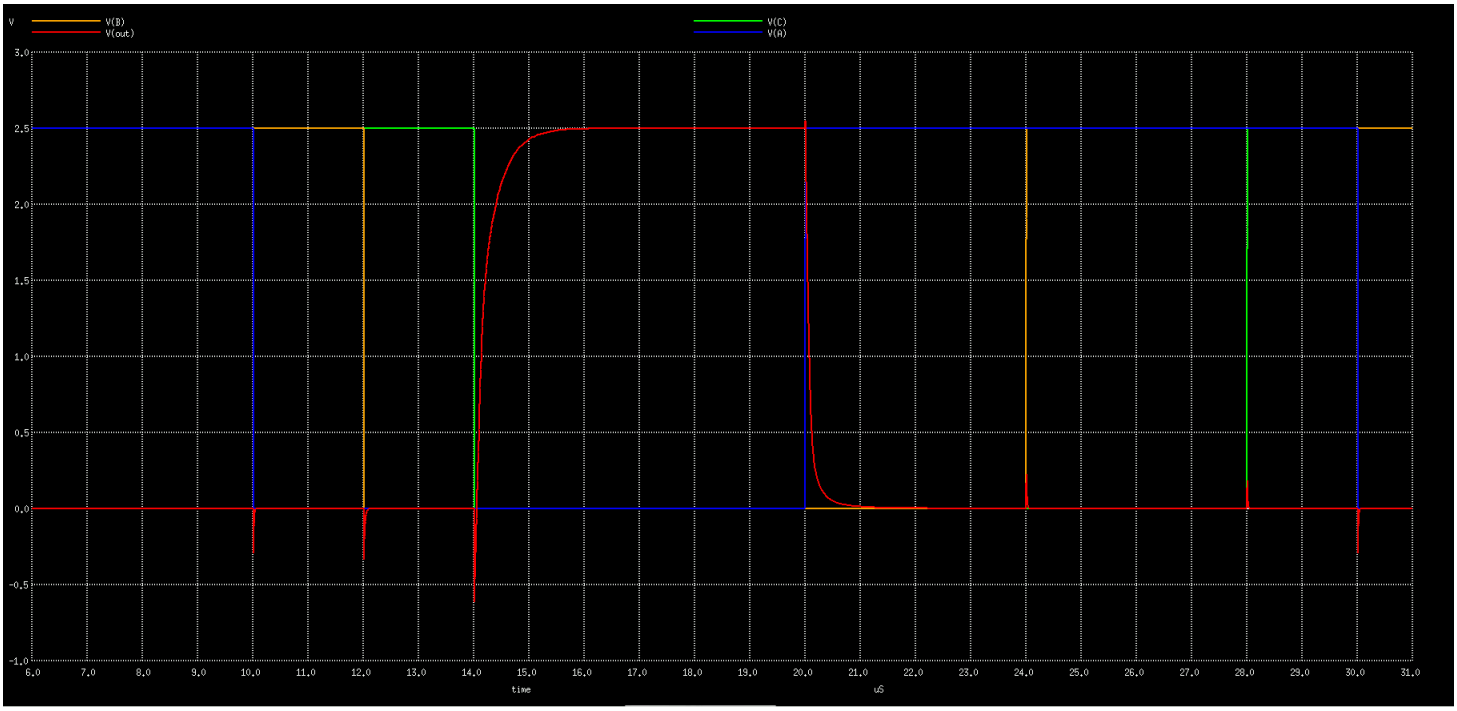

Figure 66: Functional simulation of NOR3X1

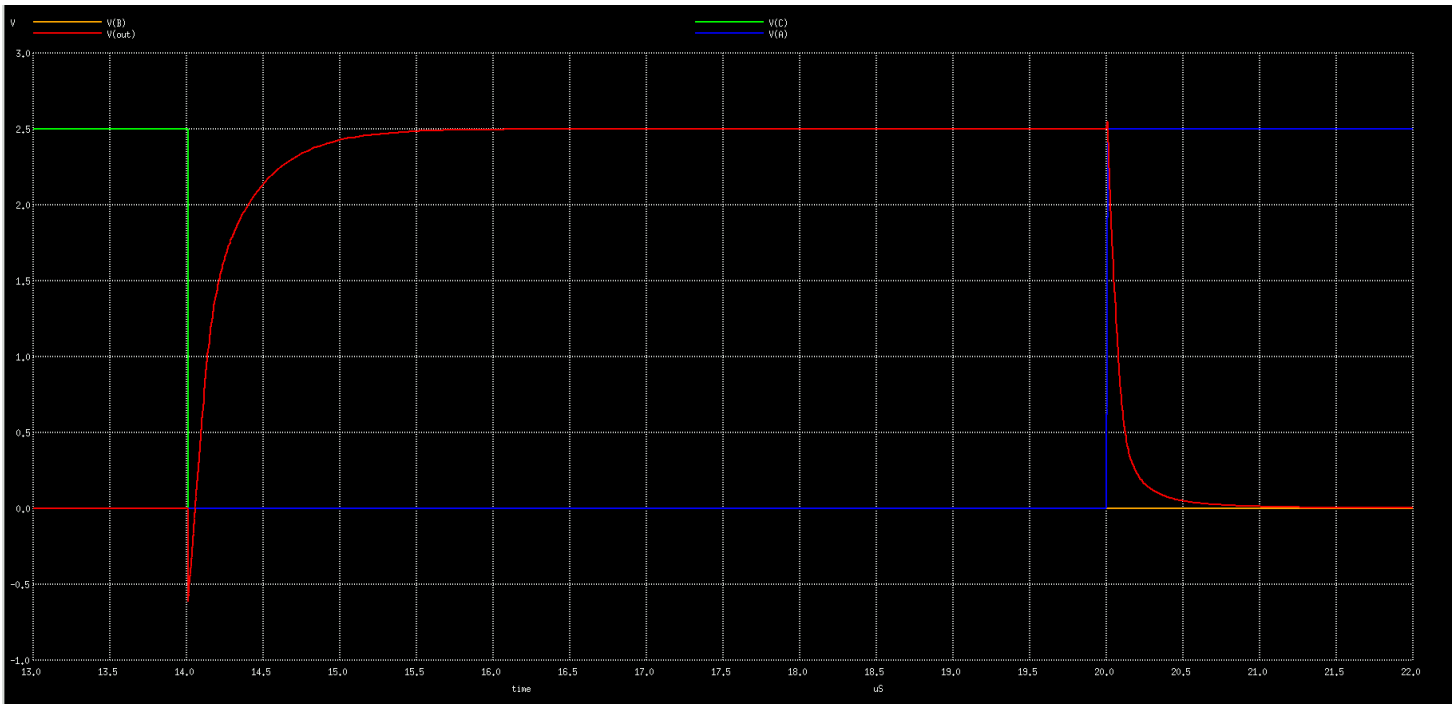

Figure 67: Fall/Rise time of NOR3X1

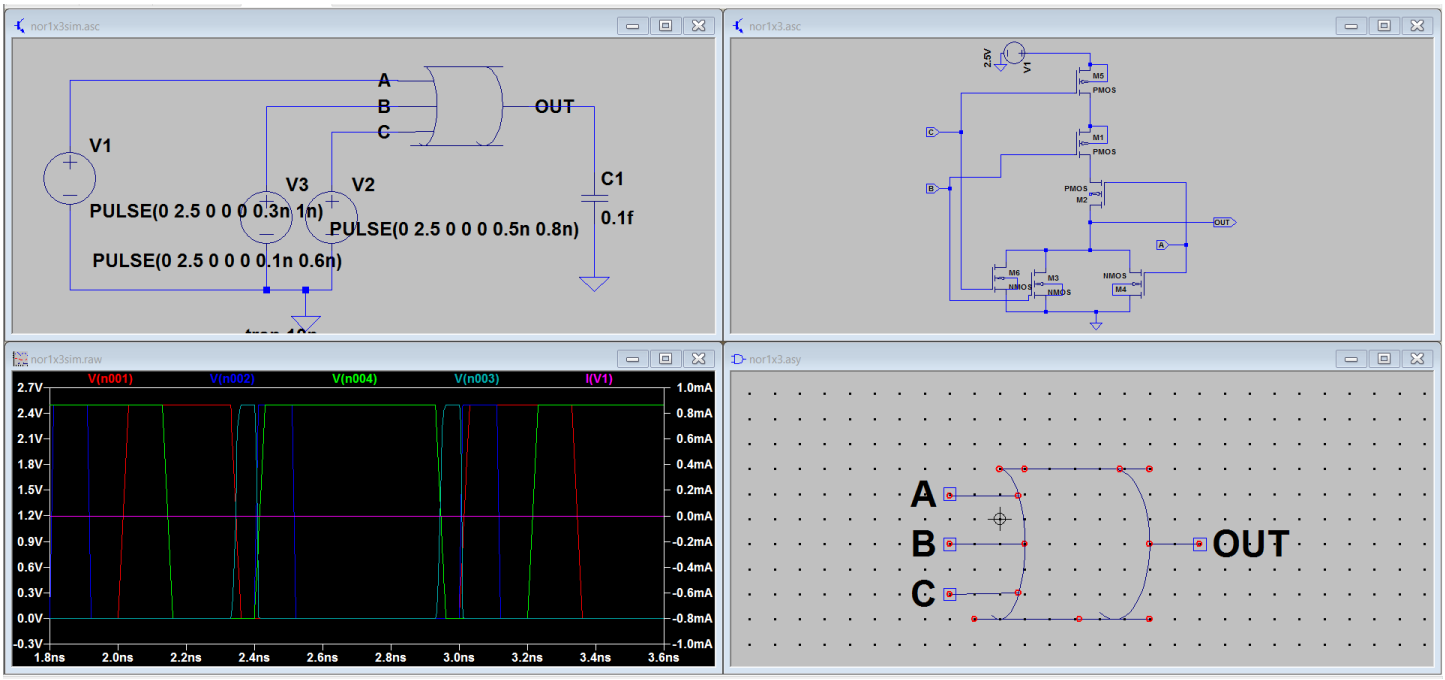

Figure 68: Symbol and circuit schematic of NOR3X1 with its functional simulation

NAND2X1

Note: Due to some problems i had in magic I did not have time for the simulation and even though I am doing the simulation part now I am sending so that we don't miss the deadline.

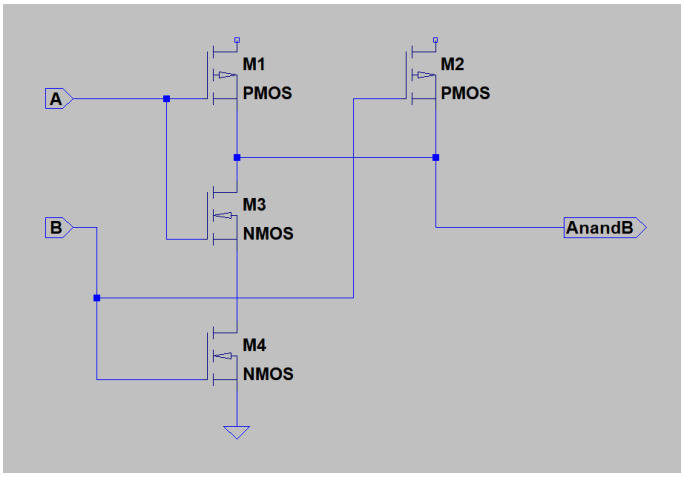

Figure 69: Circuit schematic of of NAND2X1

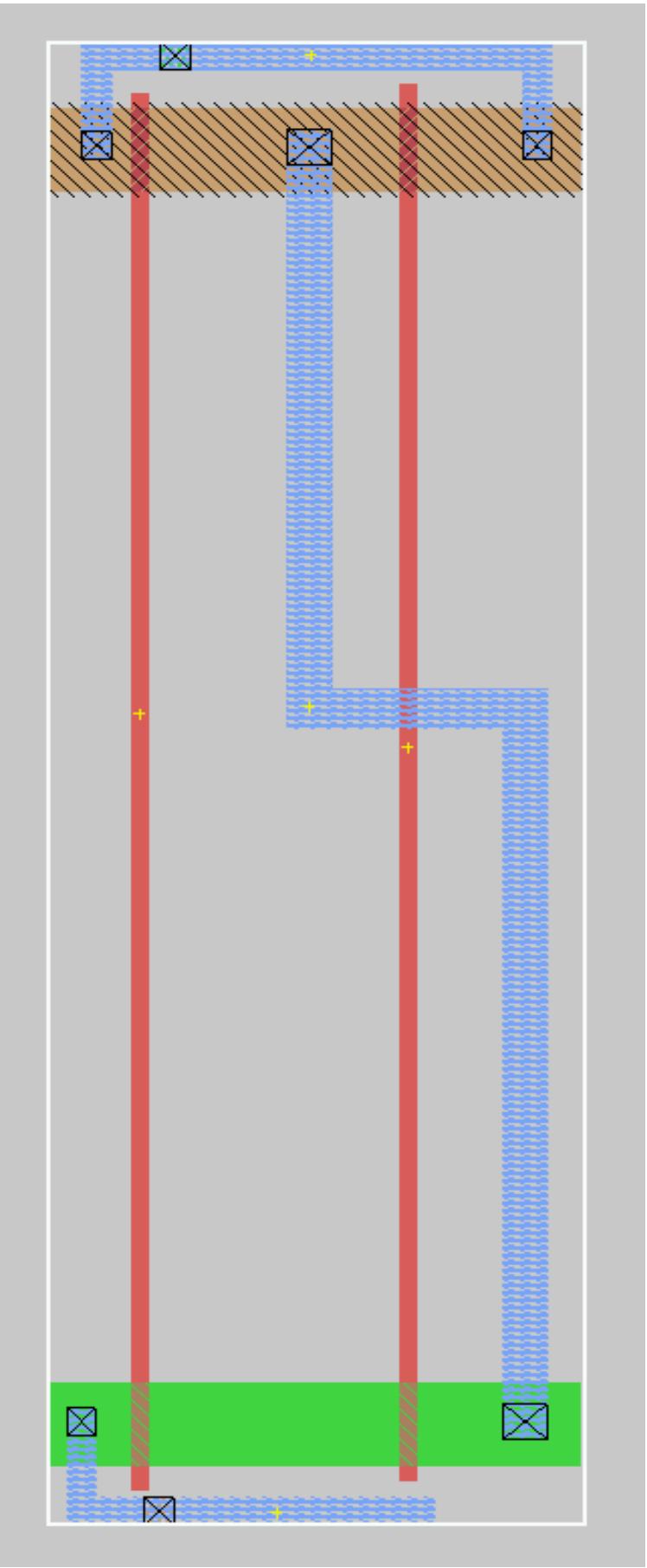

Figure 70: NAND2X1 VLSI design in Magic

NAND3X1

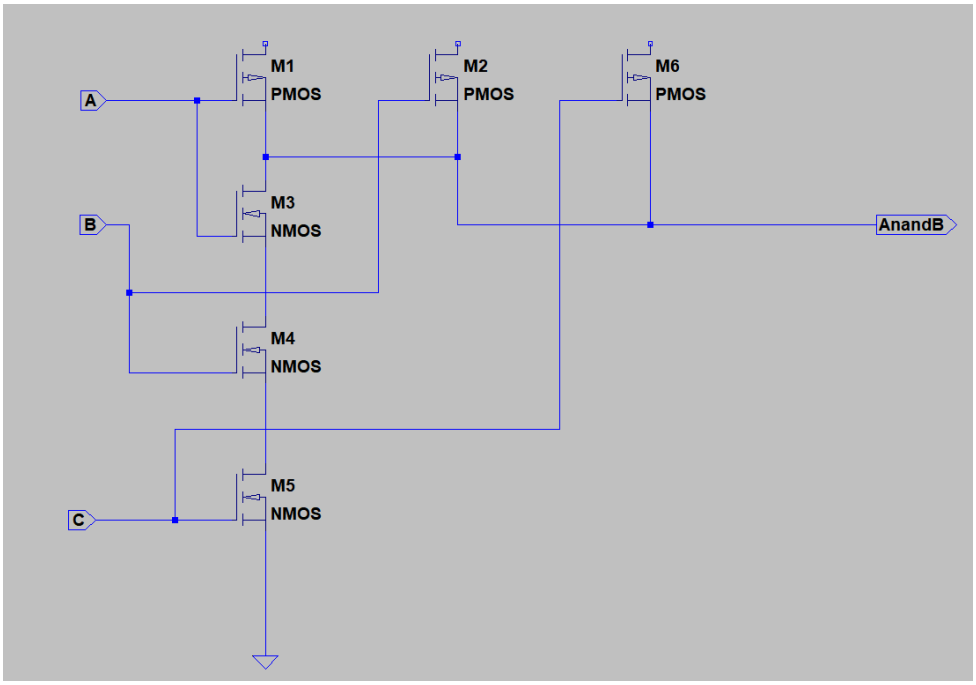

Figure 71: NAND3X1 circuit schematic

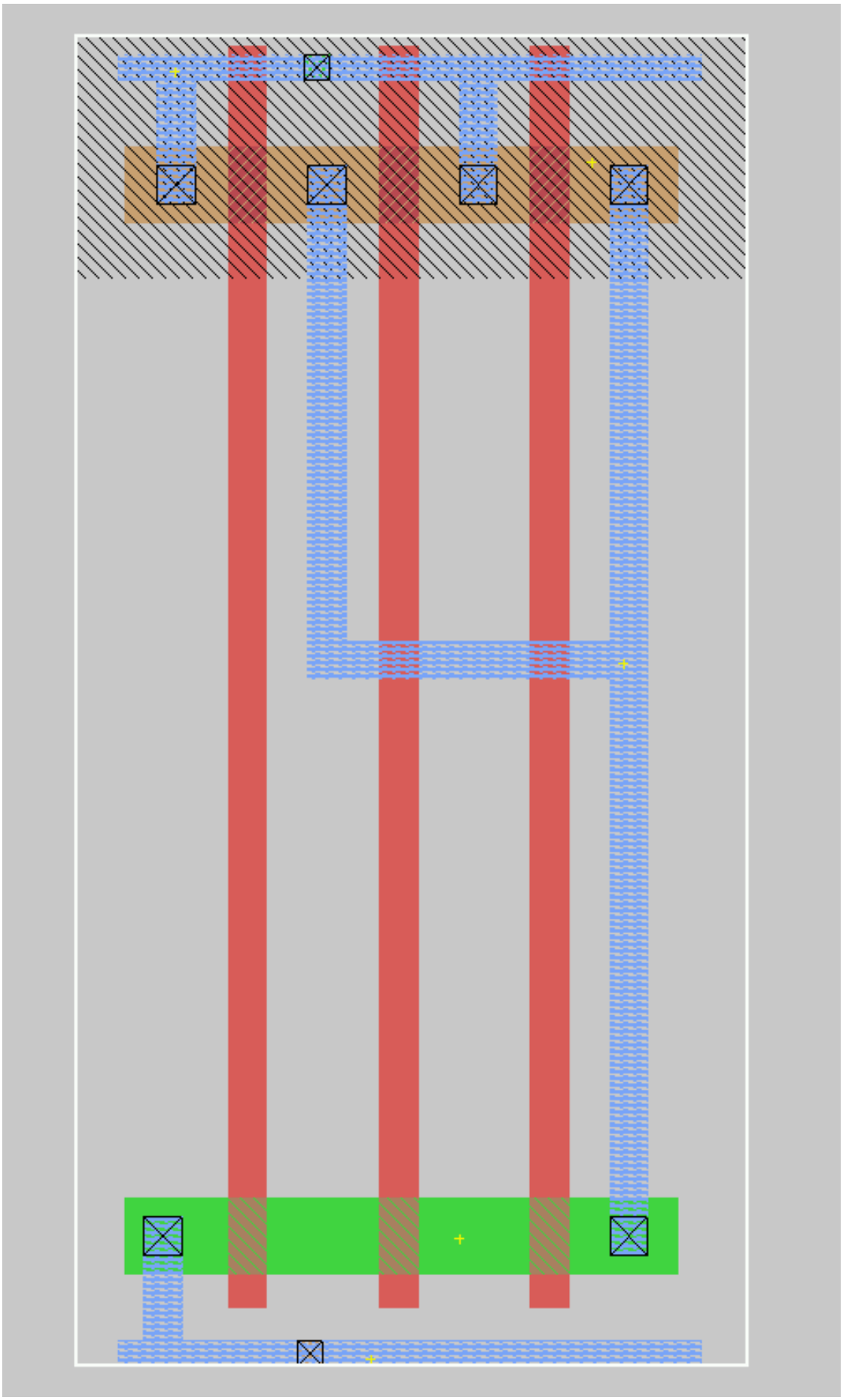

Figure 72: NAND3X1 VLSI design in Magic