Michael C. Kavcak
138 Buckthorn Dr.
Dripping Springs, TX 78620
Home: 512-266-3734
Email: sarge@kavcak.com
Website: www.kavcak.com

Job Objective: A consultant position which incorporates a mix of architecture, design, and verification of ASICs.

Work Experience:

1/01 to present

**President**, Sarge's Invincible Consulting, Austin, TX
-Self-employed consultant available for all facets of ASIC and/or micro-processor architecture, design, verification, and training.

8/21 to 7/22

**Consultant**, Alpha Omega Semiconductor, Austin, TX
-Responsible for all aspects of verification for the Digital Power group. Duties include creating and maintaining several digital and mixed-signal test benches in Specman for a new revision of a voltage regulator. Instructed remote verification team on all aspects of testbench. Updated AMS simulation environment. Ran and maintained full chip regression environment via vManager.

1/21 to 7/21

**Consultant**, Cruise, San Francisco, CA
-Responsible for integration of numerous peripheral IP blocks into a large scale SOC testbench for driverless vehicles. Required knowledge of typical peripheral protocols (SPI/UART/I2C), as well as C/UVM for system level testbench.

5/20 to present

**Consultant**, Ambiq Micro, Austin, TX
-Responsible for verification of USB 2.0 block on Apollo4 SoC, as well as flash memory interface. Duties included device driver development to move USB controller from boot through enumeration to responding to all types of transactions. Memory interface was verified against a number of commercially available flash and PSRAM devices.

4/18 to 9/19

**Consultant**, Alpha Omega Semiconductor, Austin, TX
-Responsible for all aspects of verification for the Digital Power group. Duties include creating and maintaining several digital and mixed-signal test benches in Specman for several voltage regulator products in the group. Created PMBus eVC for interfacing with parts more easily than what was previously available. Integrated with VRxx/PWM IP from Intel to help verify functionality.

1/18 to 4/18

**Student**, Cadence Connections Portable Stimulus Certification Program
-Completed training for the Perspec portable stimulus tool from Cadence over the course of several months. Online instruction from Cadence personnel, as well as lab and homework assignments to be completed for familiarization with the tool.

11/15 to 11/17

**Consultant**, Cirrus Logic, Austin, TX
-Helped create and maintain mixed-signal UVM testbenches for several digital amplifier projects. Required understanding of amplifier behavior and response to different parametric settings. Created self-checking monitors to

track proper voltage values throughout operation. Adapted testbenches for use in a Verilog-AMS simulation environment.

9/14 to 6/15

**Consultant**, Maxim Integrated, Austin, TX
-Created a self-checking mixed-signal UVM testbench using SystemVerilog for a voltage regulator. Required full understanding of chip to create reference model for all top level checking. Created sequences of PMBus commands to drive functionality of device, and implemented coverage to ensure completeness.

1/14 to 7/14

**Consultant**, Medtronic Inc., Minneapolis, MN
-Designed two block level UVM testbenches using Specman. One for an encryption module, and one for an SPI module. Both required creation of BFMs, monitors, scoreboards, and sequence libraries. Also helped integrate both environments into the top level test environment. Used vPlanner to create the test plan, as well as eManager to show completion metrics.

3/13 to 10/13

**VP Engineering**, Logic Refinery, Austin, TX
-Helped implement the Strategen verification tool. Responsibilities include customer interface, UVM-SV testbench integration, tool capability definition, and future roadmap planning.

11/12 to 1/13

**Consultant**, Maxim Integrated, Dallas, TX
-Helped create a Specman-Verilog AMS testbench for mixed-signal simulation of a battery charger. Main duties included creating an interrupt monitor/handler, along with sequences and testcases that would drive and monitor analog values at the device boundary.

11/11 to 10/12

**Consultant**, AMD, Austin, TX
-Member of core verification team. Responsible for debugging failing X86 testcases being run in regression on a wide variety of core configurations and modes. System level debug was also required on later assignment.

8/10 to 8/11

**Consultant**, Cisco Systems, Ottawa, Ontario, Canada
-Assisted with block level verification in Cisco's next generation router ASIC. Primary responsibilities include evaluating the testplan, inserting coverage primarily via System Verilog Assertions, and writing tests to fill that coverage. Work was done in System Verilog using VMM extensions.

8/09 to 7/10

**Consultant**, Texas Instruments, Dallas, TX
-Verification of memory sub-system portion of TI's flagship DSP product. Responsibilities include writing test plans, modifying the verification environment to adapt to new design changes, fixing broken portions of the environment, and eventual top-level verification closure. Also helped introduce the vPlanner tool into their Specman DV flow, which allowed for much better tracking of verification progress.

6/08 to 12/08

**Instructor**, Cadence Design Systems, Brazil
-Instructor for Cadence's IC-Brazil program. Taught theoretical digital architecture, design, and verification as well as several tools courses such as Specman and RTL Compiler to Brazilian nationals. Responsibilities included daily instruction, modifiying material as necessary, grading homework,

and directing lab exercises.

1/08 to 6/08

**Consultant**, Cisco Systems, Ottawa, Ontario, Canada
-Assisted with verification of several large ASICs. Primary responsibilities include writing tests, modifying verification environment, and meeting with designers to ensure proper RTL coverage.

4/07 to 1/08

**Verification Manager**, Coherent Logix, Austin, TX
-Responsible for all chip level verification. Put together a unit level testbench for one of the blocks and found several bugs in silicon shortly after arriving. Put together next generation chip level testbench, along with instruction generator. Used Specman and SystemVerilog verification languages.

6/06 to 8/06

**Consultant**, Boeing, Los Angeles, CA
-Assisted with verification of several FPGAs. Primary responsibilities included helping to improve the current Specman verification environment, building a new, faster Specman testbench for certain scenarios, writing tests and checks, and giving direction on Specman and verification methodology.

8/05 to 12/05

**Contract Engineer**, Volt Technical Services, Austin, TX
AMD
-Assisted the customer support division with the verification of a 3rd party ASIC using Specman. Duties include evaluating current test plan, adding to the current test environment, inserting coverage, and writing new tests.

9/04 to 3/05

**Contract Engineer**, Volt Technical Services, Austin, TX
Toshiba Cosimulation Team
-Co-lead of a verification team made up of STI (Sony, Toshiba, IBM) employees and contractors who are responsible for integrating and simulating the Cell chip's interaction with other ASICs.

10/01 to 7/04

**Design Manager**, SMSC, Austin, TX
-Responsible for all verification needs at Austin design center. Recent projects include leading a team of engineers in the verification of a USB 2.0 ASIC using Specman and the Verisity USB eVC, as well as charting future direction for the company and design center.

1/01 to 10/01

**Consultant**, Verisity, Mountain View, CA
-Trainer for the Specman verification product. Taught beginner and advanced Specman classes.

9/00 to 12/00

**Macintosh Development Manager**, 3dfx Interactive, Austin, TX
-Responsible for coordinating the engineering effort behind 3dfx's Macintosh products. Duties included organizing driver releases, interfacing with numerous other groups in 3dfx and Apple, and effectively understanding the 3dfx and Macintosh architectures.

2/00 to 9/00

**Senior Engineering Consultant**, Qualis Design Corporation, Austin, TX
-Team with ASIC design corporations to resolve all issues regarding the designs from architecture to verification. Duties also included learning new

verification languages (Vera, Specman), and teaching classes in Verilog and Specman.

8/96 to 11/99:

**PowerPC Architect**, Apple Computer, Austin, TX
Architect and Performance Group
-Responsible for system and processor architecture phases of numerous Power Macintosh computers. Duties included system modeling, performance evaluation, application analysis, and new product/processor definition.

-Responsible for lab debug phase of next generation PowerPC processors and systems. Duties included BootROM modifications, OpenFirmware coding, use of PowerPC JTAG debug tool, and general new silicon/system troubleshooting.

-Liaison between Apple and Motorola for all issues concerning the processors. Duties included communicating errata, conveying architecture details, and answering processor/system specific questions for both companies.

3/93 to 7/96:

**Product Development Engineer**, AMD, Austin, TX
K7 design team
-Responsible for all facets of design for integer core of next generation X86 microprocessor including architecture, RTL, logic design, circuit design, timing analysis, verification, and compatibility.

SLE486 design team
-Responsible for verification effort of SLE486. Duties included developing, verifying, and maintaining a test suite. Other duties included making design changes as necessary, and overseeing a group of contractors to assist in verification.

486FPU design team
-Responsible for logic and circuit design of several datapath blocks in 486FPU. Later duties included assisting in design of integer/fpu interface, and leading verification and debug effort.

1/92 to 1/93:

**Contract Engineer**, TAD Technical Services, Austin, TX
IBM 601 PowerPC design team
-Responsible for simulating bus protocol on 601 PowerPC. Duties included making behavioral level bus models and writing test cases to simulate the 601 PowerPC bus.

6/91 to 9/91:

**Contract Engineer**, TAD Technical Services, Austin, TX
AMD SONIC design team
-Responsible for porting AMD 8051 microcontroller design into SONIC chip. Duties included logic design and verification of microcontroller using Quicksim and Verilog.

5/90 to 8/90:

**Programmer**, IBM, Research Triangle Park, NC
IBM LAN test team
-Responsible for developing the initial parts of a program to perform exhaustive testing on IBM token ring networks. Used a modular design for program so that further additions would be easy to implement.

5/89 to 8/89:

**Programmer**, IBM, Research Triangle Park, NC

IBM LAN test team
-Responsible for developing a test program which would operate across a token ring remote bridge. Designed program to test bandwidth across the bridge.

Education:

University of Texas at Austin, Austin, TX, 78712
Master's Degree Program: Electrical Engineering
Thesis: Controller for Associative Memory
Graduated: May, 1992 G.P.A. 3.43

Pennsylvania State University, University Park, PA, 16802
Graduated with distinction, B.S. degree: May, 1990
Major: Computer Engineering
Cumulative G.P.A. 3.55 Major G.P.A. 3.60

Activities:

-Men's Senior Baseball League
-Handy Wheels volunteer