Kevin Chen

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EXPERIENCE

Apple | Design Verification Engineer (Silicon Engineering Group) | *Cupertino, CA* 2021 – Present

- Performed chip-level power aware verification, bringing up full-chip infrastructure, driving use case regressions with hundreds of tests to closure, and taping out 2-3 chips used in products such as iPhones and Macs every year
- Owned chip to power management unit co-simulation, enabling power rail sequencing when changing sleep states
- Converged supply state coverage flows, writing a single script used by dozens of IPs across 3 international sites

Penn Electric Racing | Electrical Lead | *University of Pennsylvania* 2017 – 2021

- Led a 25-member electrical team in designing custom electronics for racecars that place top three at FSAE Lincoln
- Designed a semi-distributed, 300V battery management system, consisting of daughter boards that monitor the temperature and voltage of lithium-ion batteries and a motherboard that analyzes and responds to the data
- Drove the PCB design timeline by documenting and reviewing 15 four-layer boards, including a power distribution unit and an LCD dashboard, that use STM32 microcontrollers, communicate over CAN, and total 2000 components

Relativity Space | Avionics Power Intern | *Los Angeles, CA* Summer 2020

- Accelerated the power architecture towards first flight readiness by designing a battery management system with short circuit protection for packs that supply over 1kW continuously and are used on both stages of the launch vehicle
- Co-routed a 16-layer power distribution board, shaving over half a month off the development timeline

Latch | Electrical Engineering Intern | *New York City, NY* Summer 2019

- Revamped the firmware prototyping and production line workflows by designing an interface board for all Latch devices, standardizing testing procedures across all products and making them take 50% less time
- Implemented a solution for characterizing the battery consumption of Latch devices in lifecycle testing

EDUCATION

University of Pennsylvania, School of Engineering & Applied Science Philadelphia, PA May 2021
MSE in Electrical Engineering | **BSE** in Computer Engineering **GPA:** 3.90/4.00
Minors: Mathematics, Engineering Entrepreneurship Summa Cum Laude ('21) | Tau Beta Pi ('20)

PROJECTS & ACTIVITIES

Novarcus | IoT Embedded Project | *C, Altium* Spring 2021

- Designed a IoT camera gimbal that had a bootloader and Wi-Fi for firmware updates and a command line interface

PennOS and PennShell | Operating Systems | *C, Linux* Fall 2020

- Built a UNIX-like operating system consisting of a priority scheduler, a FAT file system, and a bash-like shell
- Focused on the kernel side of the project, implementing kernel and user level functions as well as shell commands

Superscalar Pipelined Processor | Computer Architecture | *Verilog* Spring 2020

- Designed a fully bypassed CPU with two 5-stage superscalar pipelines and a basic branch prediction scheme
- Wrote a compiler and assembler in C for an ISA inspired by LC-3 and a language loosely inspired by Forth

Head Teaching Assistant | Discrete Mathematics for Computer Science 2018 – 2021

- Managed five TAs, wrote problem sets, and held office hours, assisting over 250 master students worldwide

SKILLS

- **Programming:** C | Python | Verilog/SystemVerilog (UVM) | Java | Tcl | Perforce+Git
- **Hardware:** PCB Design (Altium) | Electronics Lab Equipment | Soldering | Embedded Platforms (Atmel, mbed)