Kevin Chen

(856) 857 – 4373 | kevinchen929@gmail.com
linkedin.com/in/kevinchen929

EXPERIENCE

Apple | Design Verification Engineer (Silicon Engineering Group) | *Cupertino, CA* 2021 – Present

- Performed chip-level power-aware verification, working cross-functionally with design, architecture, and firmware teams to integrate over 25 subsystems and ship about 4 chips a year for use in products like iPhones, iPads, and Macs
- Developed new scripts and drove their adoption globally, left-shifting checks to subsystem-level verification in order to detect design bugs 2-3 months earlier; these scripts also bolstered coverage, for example, by parsing Excel and JSON databases to generate assertions that confirm the design never hits an invalid condition
- Owned chip to power management unit (PMU) co-simulation, delivering a library that let over 1000 functional tests interface with the PMU to verify accurate system-level behavior under real-world power rail sequencing events
- Spearheaded chip power state use cases, writing tests and debugging waveforms to validate accurate state machine transitions, a critical chip function; enhanced the CI/CD pipeline with integration tests and ensured comprehensive coverage through corner case testing and ad hoc regressions with random state changes
- Coordinated cross-functional discussions for a major architectural update to the chip and PMU state machines, contributing as my team's subject matter expert to help devise a thorough integration test plan
- Supported the DevOps/Tooling team's overhaul of our regression infrastructure, developing wrapper functions used by dozens of engineers to expedite their transition to the new framework

Penn Electric Racing | Electrical Lead | *University of Pennsylvania* 2017 – 2021

- Led a 25 member team, designing custom electronics for racecars that place top 3 internationally at FSAE Lincoln
- Oversaw the PCB development schedule, conducting design reviews, authorizing all board layouts, and ensuring timely procurement of about 15 complex four-layer boards with over 2000 components annually
- Engineered a semi-distributed 300V battery management system, equipped with daughter boards for precise battery monitoring and a central motherboard for response to the data, resulting in no injuries or battery failures

Relativity Space | Avionics Power Intern | *Los Angeles, CA* Summer 2020

- Advanced first flight readiness by engineering a battery management system critical to both stages of the final launch vehicle, featuring short circuit protection and support for over 1kW of continuous power
- Co-routed a 16-layer power distribution board, cutting the development timeline by over half a month

Latch | Electrical Engineering Intern | *New York City, NY* Summer 2019

- Revamped firmware prototyping and production line workflows by designing a universal interface board for Latch devices, standardizing testing procedures across all products and reducing setup time by 50%

EDUCATION

University of Pennsylvania, School of Engineering & Applied Science | Philadelphia, PA May 2021
MSE in Electrical Engineering | **BSE** in Computer Engineering **GPA:** 3.90/4.00
Minors: Mathematics, Engineering Entrepreneurship Summa Cum Laude ('21) | Tau Beta Pi ('20)
Course projects can be found at www.kevinjchen.me

SKILLS

- Motivated engineer, excelling at cross-functional communication (worked at a vertically integrated company), time management (aggressively shipped chips with overlapping timelines), and critical thinking (debugged complex issues)
- **Software**: C | Python | Version Control (Perforce, Git) | | *Working Knowledge*: Perl | Java | C++ | bash | SQL
- **Hardware:** Waveform Debug (Verisium, Verdi) | Verilog/SystemVerilog (UVM) | UPF | Tcl
- **Electrical Engineering:** PCB Design (Altium) | Electronics Lab Equipment | Soldering | Embedded Platforms