Kevin Chen

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EXPERIENCE

Apple | Design Verification Engineer (Silicon Engineering Group) | *Cupertino, CA* 2021 – Present

- Conducted chip-level power-aware verification, collaborating with design, architecture, firmware, and power teams to integrate over 25 IPs and tape out about 4 chips annually for use in products such as iPhones, iPads, and Macs
- Owned chip to power management unit (PMU) co-simulation, delivering power rail sequencing to hundreds of tests
- Developed new flows and led their adoption in 3 international sites, including a PMU model that left-shifted rail sequencing to IP-level testing and assertions generated to flag illegal power state pairs, thereby enhancing coverage
- Partnered with the CAD team to upgrade our regression infrastructure, improving usability for dozens of engineers
- Drove power state use cases, debugging waveforms and coordinating with IP owners to verify chip sleep transitions

Penn Electric Racing | Electrical Lead | *University of Pennsylvania* 2017 – 2021

- Led a 25 member team, developing custom electronics for racecars that place top 3 internationally at FSAE Lincoln
- Managed the PCB design timeline, reviewing and approving 15 four-layer boards totalling over 2000 components
- Designed a semi-distributed, 300V battery management system, consisting of daughter boards that monitor the temperature and voltage of lithium-ion batteries and a motherboard that reacts to the data to keep the batteries safe

Relativity Space | Avionics Power Intern | *Los Angeles, CA* Summer 2020

- Accelerated power architecture towards first flight readiness by engineering a battery management system with short circuit protection for packs that supply over 1kW continuously and are used on both stages of the launch vehicle
- Co-routed a 16-layer power distribution board, cutting the development timeline by over half a month

Latch | Electrical Engineering Intern | *New York City, NY* Summer 2019

- Revamped firmware prototyping and production line workflows by designing a universal interface board for Latch devices, standardizing testing procedures across all products and reducing setup time by 50%
- Implemented a solution for characterizing the battery consumption of Latch devices in lifecycle testing

EDUCATION

University of Pennsylvania, School of Engineering & Applied Science | Philadelphia, PA May 2021
MSE in Electrical Engineering | **BSE** in Computer Engineering **GPA:** 3.90/4.00
Minors: Mathematics, Engineering Entrepreneurship Summa Cum Laude ('21) | Tau Beta Pi ('20)

PROJECTS

Novarcus | IoT Embedded Project | *C, Altium* Spring 2021

- Designed an IoT camera gimbal that had a bootloader, Wi-Fi firmware updates, and a command line interface

PennOS and PennShell | Operating Systems | *C, Linux* Fall 2020

- Built a UNIX-like operating system consisting of a priority scheduler, a FAT file system, and a bash-like shell
- Focused on the kernel side of the project, implementing kernel and user level functions as well as shell commands

Superscalar Pipelined Processor | Computer Architecture | *Verilog* Spring 2020

- Designed a fully bypassed CPU with two 5-stage superscalar pipelines and a basic branch prediction scheme
- Wrote a compiler and assembler in C for an ISA inspired by LC-3 and a language loosely inspired by Forth

SKILLS

- **Programming:** C | Python | Verilog/SystemVerilog (UVM) | UPF | Tcl | Java | Perforce+Git
- **Hardware:** PCB Design (Altium) | Waveform Debug (Verisium, Verdi) | Electronics Lab Equipment | Soldering