Kevin Chen

(856) 857 – 4373 | kevinchen929@gmail.com
Relocating to New York Metropolitan Area | linkedin.com/in/kevinchen929

EXPERIENCE

Apple | Design Verification Engineer (Silicon Engineering Group) | *Cupertino, CA* 2021 – Present

Design Verification Engineer III (2023 – Present)

- Performed chip-level verification on 4 chips per year for use in products like iPhones, iPads, and Macs, working cross-functionally with design, architecture, and firmware teams to integrate over 25 subsystems
- Developed and drove the adoption of new scripts globally, introducing checks to subsystem-level verification that enabled the detection of design bugs 2-3 months earlier; the scripts also improved test coverage, parsing Excel and JSON design databases to automatically generate assertions enforcing design invariants
- Owned chip to power management unit (PMU) co-simulation, delivering a library that allowed over 1000 functional tests verify accurate system-level behavior under real-world power rail sequencing events
- Bolstered the CI/CD pipeline with integration tests that validated the chip's power state transitions and ad hoc regressions that cycled through random states to ensure comprehensive coverage

Design Verification Engineer II (2021 – 2023)

- Coordinated inter-team discussions for a major architectural update to the chip and PMU state machines, contributing as my team's subject matter expert to help devise a thorough integration test plan
- Implemented abstractions used by dozens of engineers to expedite their transition to the new framework, thereby playing a pivotal role in supporting the DevOps/Tooling team's overhaul of our regression infrastructure
- Drove the validation of chip power states, writing unit tests that simulate typical user behavior, engaging with firmware teams to receive sequence deliveries, and spearheading debugs to confirm the chip behaves as expected

Penn Electric Racing | Electrical Lead | *University of Pennsylvania* 2017 – 2021

- Led a 25 member team, designing custom electronics for racecars that place top 3 internationally at FSAE Lincoln
- Oversaw the printed circuit board (PCB) development schedule, conducting design reviews, authorizing all board layouts, and ensuring timely procurement of about 15 complex four-layer boards with over 2000 components annually
- Engineered a semi-distributed 300V battery management system, equipped with daughter boards for precise battery monitoring and a central motherboard that acts on the data, resulting in no injuries or battery failures

Relativity Space | Avionics Power Intern | *Los Angeles, CA* Summer 2020

- Advanced first flight readiness by engineering a battery management system critical to both stages of the final rocket
- Co-routed a 16-layer power distribution board, cutting the development timeline by over half a month

Latch | Electrical Engineering Intern | *New York City, NY* Summer 2019

- Revamped firmware prototyping and production line workflows by designing a universal interface board for Latch devices, standardizing testing procedures across all products and reducing setup time by 50%

EDUCATION

University of Pennsylvania, School of Engineering & Applied Science | Philadelphia, PA May 2021

MSE in Electrical Engineering | **BSE** in Computer Engineering **GPA:** 3.90/4.00

Minors: Mathematics, Engineering Entrepreneurship Summa Cum Laude ('21) | Tau Beta Pi ('20)

Course projects can be found at www.kevinjchen.me

SKILLS

- **Software**: C | Python | Version Control (Perforce, Git) | | *Working Knowledge*: Perl | Java | C++ | bash | SQL
- **Hardware:** Waveform Debug (Verisium, Verdi) | Verilog/SystemVerilog (UVM) | UPF | Tcl
- **Electrical Engineering:** PCB Design (Altium) | Electronics Lab Equipment | Soldering | Embedded Platforms