LPDDR3 PHY

LPDDR2/LPDDR3(L28, L32)

Revision 1.23

September 2012

User's Guide

SAMSUNG ELECTRONICS

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LPDDR3 PHY, LPDDR2/LPDDR3(L28, L32)**USER GUIDE**
User's Guide, Revision 1.23

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Revision History

Revision No.	Date	Description	Refer to	Author(s)
1.00	2011-10-20	LPDDR3 PHY initial Draft (Preliminary)	all	S.H. Kim
1.10	2012-01-19	Add power information about LN28LPP(p1) Remove DDR2 support(p1) Add layout guide about "clk_en"(p14)		
1.11	2012-03-20	Changed clk shielding guide. (p10)		Alex. Joo
1.21	2012-07-17	Add "Used Cell" information(p1) Add the jitter requirement(p13) Correct "Transmission line skew management"(p15)		S.H. Kim
1.22	2012-09-03	Correct "Transmission line skew management"(p15)		JH Oh
1.23	2013-01-28	Add "V5R2Rev1.32" information in Table 1-1(p1) Add "V5R2Rev1.32" scan information in Table 3-2(p4)		S.H. Kim

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Register RW Access Type Conventions

Type	Definition	Description
R	Read Only	The application has permission to read the Register field. Writes to read-only fields have no effect.
W	Write Only	The application has permission to write in the Register field.
RW	Read & Write	The application has permission to read and writes in the Register field. The application sets this field by writing 1'b1 and clears it by writing 1'b0.

Register Value Conventions

Expression	Description
x	Undefined bit
X	Undefined multiple bits
?	Undefined, but depends on the device or pin status
Device dependent	The value depends on the device
Pin value	The value depends on the pin status

Reset Value Conventions

Expression	Description
0	
1	
x	

Warning: Some bits of control registers are driven by hardware or write only. As a result the indicated reset value and the read value after reset might be different.

List of Acronyms

Acronyms	Descriptions
ACC	Adaptive Color Correction or Accurate Color Correction
BIST	Built In Self Test
GD	Gate Driver (Row Driver)
MB4	Mont Blanc 4 (GD Integration on LCD Panel)
SD	Source Driver (Column Driver)
CD	Column Driver (Source Driver)
SSCG	Spread Spectrum Clock Generation
TCON	Timing CONtroller
POR	Power On Reset
FRC	Frame Rate Control
DPRC	Data Processing
ATPG	Automatic Test Pattern Generation

1 OVERVIEW

Table shows the physical specification of PHY.

Table 1-1 Physical LPDDR3 PHY Specification

	Category	Description
LN32LP V5R1Rev2.7	Size	V5R1_LPDDR3_32b_PHY(4915X330um)
	Metal Option	6-metal
	Operation Frequency	≤ 533MHz (1066Mbps for LPDDR2) ≤ 800MHz (1600Mbps for LPDDR3/DDR3)
	Voltage	0.95V ~ 1.155V for 800MHz(LPDDR3 PHY)
	Dynamic Power	78.55mW(SS/-25C/0.95V), 126.3mW(FF/125C/1.155V)
	Static Power	0.012mW(SS/-25C/0.95V), 19.12mW(FF/125C/1.155V)
	Used Cell Type	RVT(1.29%), LVT(0.16%), LLP_RVT(97.77%), LLP_LVT(0.77%)
LN28LPP V5R2Rev0.4	Size	V5R2_LPDDR3_32b_PHY(4915X280um)
	Metal Option	6-metal
	Operation Frequency	≤ 533MHz (1066Mbps for LPDDR2) ≤ 800MHz (1600Mbps for LPDDR3/DDR3)
	Voltage	0.95V ~ 1.155V for 800MHz(LPDDR3 PHY)
	Dynamic Power	63.27mW(SS/-25C/0.95V), 107.594mW(FF/125C/1.155V)
	Static Power	0.012mW(SS/-25C/0.95V), 16.448mW(FF/125C/1.155V)
	Used Cell Type	RVT(0.00%), LVT(0.15%), LLP_RVT(98.43%), LLP_LVT(1.42%)
LN28LPP V5R2Rev1.32	Size	V5R2_LPDDR3_32b_PHY(4055X280um + 2200X70um)
	Metal Option	6-metal
	Operation Frequency	≤ 533MHz (1066Mbps for LPDDR2) ≤ 933MHz (1866Mbps for LPDDR3/DDR3)
	Voltage	1.0V±5%(800MHz), 1.1V±5%(933MHz)
	Dynamic Power	59.7mW(SS/-25C/0.95V), 112.426mW(FF/125C/1.155V)
	Static Power	0.008mW(SS/-25C/0.95V), 17.04mW(FF/125C/1.155V)
	Used Cell Type	

NOTE: "V5R2Rev1.32" has less power consumption (15~20%) than "V5R2Rev0.4" if applying to "wrapper clock gating" after leveling and calibration.

2 I/O SELECTION

The following I/Os should be selected as SEC LPDDR2/LPDDR3/DDR3 Combo I/O set that is electrically and physically tuned to the LN32LP low power process. This I/O uses 1.2V signaling when interfacing with LPDDR2 or LPDDR3 SDRAM and 1.5V signaling when interfacing with DDR3 SDRAM.

The following Combo I/Os can be also used as CMOS receiver by setting high at “CMOSRCV” pin. This can be used to interface with LPDDR/LPDDR2 SDRAM under 200MHz.

Table 2-1 LN32LP LPDDR2/LPDDR3/DDR3 Combo I/O Cell List

Cell Name	Type	Description	Size with PAD
pblpddr3_dds	I/O	Bi-direction PAD for DQ Only for LPDDR3 w/o ODT feature	30x236.95um
pblpddr3_dqs_dds	I/O	Differential bi-direction PAD for DQS Only for LPDDR3 w/o ODT feature	30x236.95um
pblpddr3	I/O	Bi-direction PAD for DQ	30x236.95um
pblpddr3_dqs	I/O	Differential bi-direction PAD for DQS	30x236.95um
polpddr3_cke	O	Output PAD for CKE(Clock Enable) Pin	30x236.95um
pvref_lpddr3	I/O	VREF supply PAD	30x236.95um
impcnt_new2_lpddr3	I/O	ZQ Calibration PAD	30x236.95um
pvddls_lpddr3	PWR	Power Pad for internal core & DDRx I/O’s logic	30x236.95um
pvssls_lpddr3	GND	Ground pad for core & DDRx I/O’s logic	30x236.95um
pdvdds_lpddr3	PWR	Power pad for DDRx I/O’s output driver	30x236.95um
pdvsss_lpddr3	GND	Ground pad for DDRx I/O’s output driver	30x236.95um
break_lpddr3_lpddr3	Slot	VDDQ/VSSQ Power separation in DDRx PHY	30x236.95um
pilpddr3_ckein	I	External retention mod control I/O	30x236.95um
decap_lpddr3	-	Filler cell with De-cap.	30x236.95um
impcnt_ext_lpddr3	-	Control cell for external impedance setting mode	30x236.95um
link_lpddr3_eg18	-	Link cell between DDR IOs and GPIOs, connect VDD/VSS/DVSS ring each other	30x236.95um
link_lpddr3_eg18_all	-	Link cell between DDR IOs and GPIOs, connect VDD/VSS/DVDD/DVSS ring each other	30x236.95um

3 DFT GUIDE

3.1 SCAN INSERTION

ctldb shoud be used for scan-insertion instead of netlist.

Example 3-1 SCAN Insertion

```
STEP:
# read ctldb instead of netlist. (model name is different according to PHY type and bit width)
read_test_model LPDDR3_32b_PHY_SCAN.ctldb (or LPDDR3_16b_PHY_SCAN.ctldb)
......

# stitch scan-chains of LPDDR3 PHY to top scan-chains.
set_scan_path "chain#0" { "LPDDR3 PHY Hierarchy"/c1 } -complete true
                          A                B                C
set_scan_path "chain#1" { "LPDDR3 PHY Hierarchy"/c2 } -complete true
set_scan_path "chain#2" { "LPDDR3 PHY Hierarchy"/c3 } -complete true
......
set_scan_path "chain#8" { "LPDDR3 PHY Hierarchy"/c8 } -complete true
set_scan_path "chain#9" { "LPDDR3 PHY Hierarchy"/9 } -complete true
set_scan_path "chain#10" { "LPDDR3 PHY Hierarchy"/10 } -complete true

*A : top scan chain name
*B : hierarchy of LPDDR3 PHY
*C : scan chain name of LPDDR3 PHY (refer to scanpath.rpt or table for scan chain information)

......
# remove black box design before write the final netlist.
remove_design LPDDR3_16b_PHY (or LPDDR3_32b_PHY)
```

Table 3-1 Scan-chain Information (V5R1Rev2.7, V5R2Rev0.4)

Scan Input	Scan Output	Scan Chain Name	Number of Chain
test_si[0]	test_so[0]	c1	382
test_si[1]	test_so[1]	c2	382
test_si[2]	test_so[2]	c3	382
test_si[3]	test_so[3]	c4	382
test_si[4]	test_so[4]	c5	382
test_si[5]	test_so[5]	c6	382
test_si[6]	test_so[6]	c7	382
test_si[7]	test_so[7]	c8	382
test_si[8]	test_so[8]	c9	382
test_si[9]	test_so[9]	c10	382
test_si[10]	test_so[10]	11	382
test_si[11]	test_so[11]	12	382
test_si[12]	test_so[12]	13	382
test_si[13]	test_so[13]	14	382
test_si[14]	test_so[14]	15	382
test_si[15]	test_so[15]	16	382
test_si[16]	test_so[16]	17	382
test_si[17]	test_so[17]	18	381
test_si[18]	test_so[18]	19	381
test_si[19]	test_so[19]	20	381

Table 3-2 Scan-chain Information (V5R2Rev1.32)

Scan Input	Scan Output	Scan Chain Name	Number of Chain
test_si[0]	test_so[0]	c1	239
test_si[1]	test_so[1]	c2	239
test_si[2]	test_so[2]	c3	239
test_si[3]	test_so[3]	c4	239
test_si[4]	test_so[4]	c5	239
test_si[5]	test_so[5]	c6	239
test_si[6]	test_so[6]	c7	239
test_si[7]	test_so[7]	c8	239
test_si[8]	test_so[8]	c9	239
test_si[9]	test_so[9]	c10	239
test_si[10]	test_so[10]	11	239
test_si[11]	test_so[11]	12	239
test_si[12]	test_so[12]	13	239

test_si[13]	test_so[13]	14	239
test_si[14]	test_so[14]	15	239
test_si[15]	test_so[15]	16	239
test_si[16]	test_so[16]	17	239
test_si[17]	test_so[17]	18	239
test_si[18]	test_so[18]	19	239
test_si[19]	test_so[19]	20	239
test_si[20]	test_so[20]	21	239
test_si[21]	test_so[21]	22	238
test_si[22]	test_so[22]	23	238
test_si[23]	test_so[23]	24	238
test_si[24]	test_so[24]	25	238
test_si[25]	test_so[25]	26	238
test_si[26]	test_so[26]	27	238
test_si[27]	test_so[27]	28	238
test_si[28]	test_so[28]	29	238
test_si[29]	test_so[29]	30	238
test_si[30]	test_so[30]	31	238
test_si[31]	test_so[31]	32	238

4 CKE CONTROL

4.1 CKE CONNECTION

CKE retention control input I/O(CKEIN I/O) should be connected internally to the retention control input of CKE[0]/CKE[1]/RESET. pilpddr3_ckein and polpddr3_cke are used for retention I/O. If you don't need to use pilpddr3_ckein as Figure 4-1, we recommend power or filler cell instead of pilpddr3_ckein.

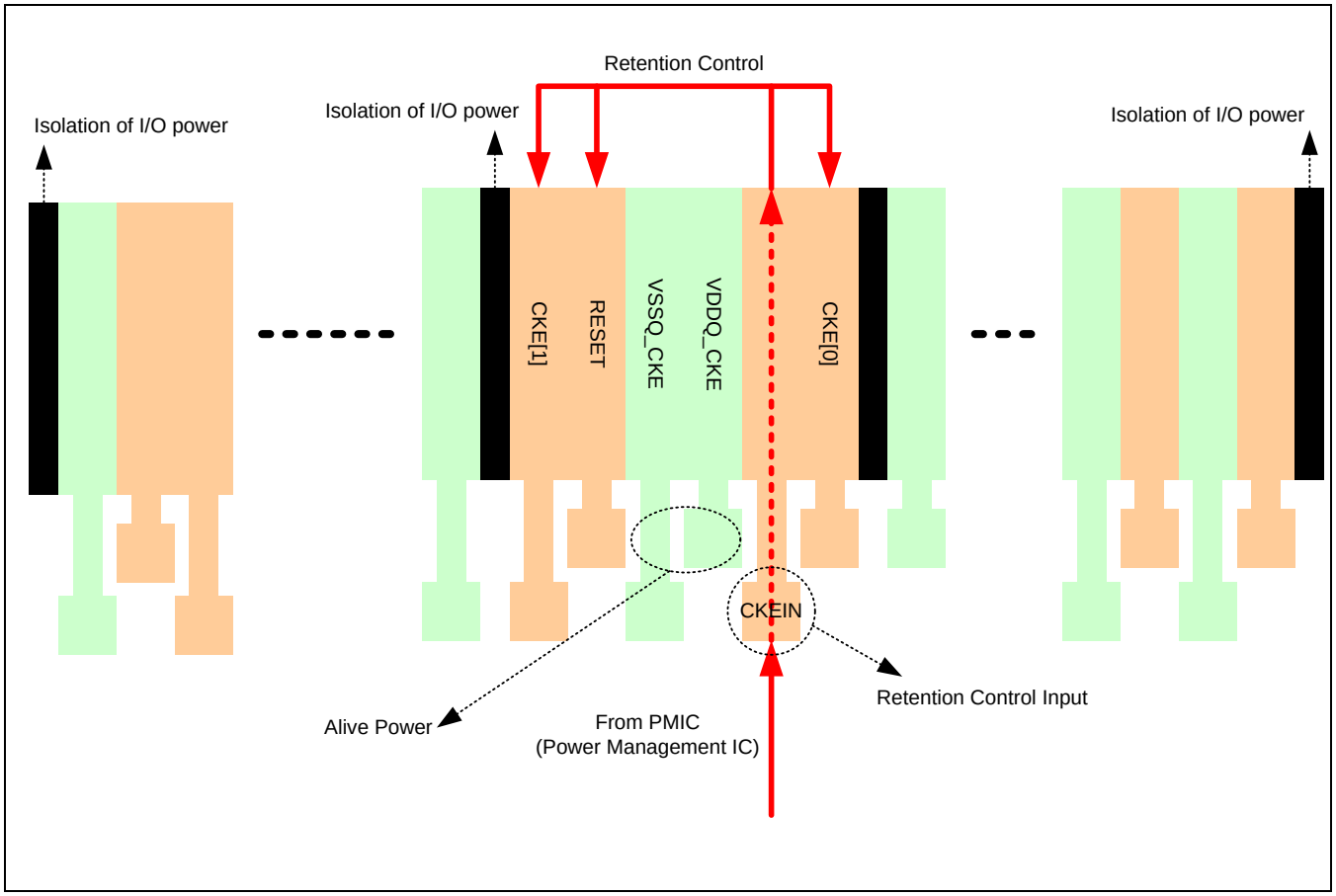

Figure 4-1 External CKE Retention Control

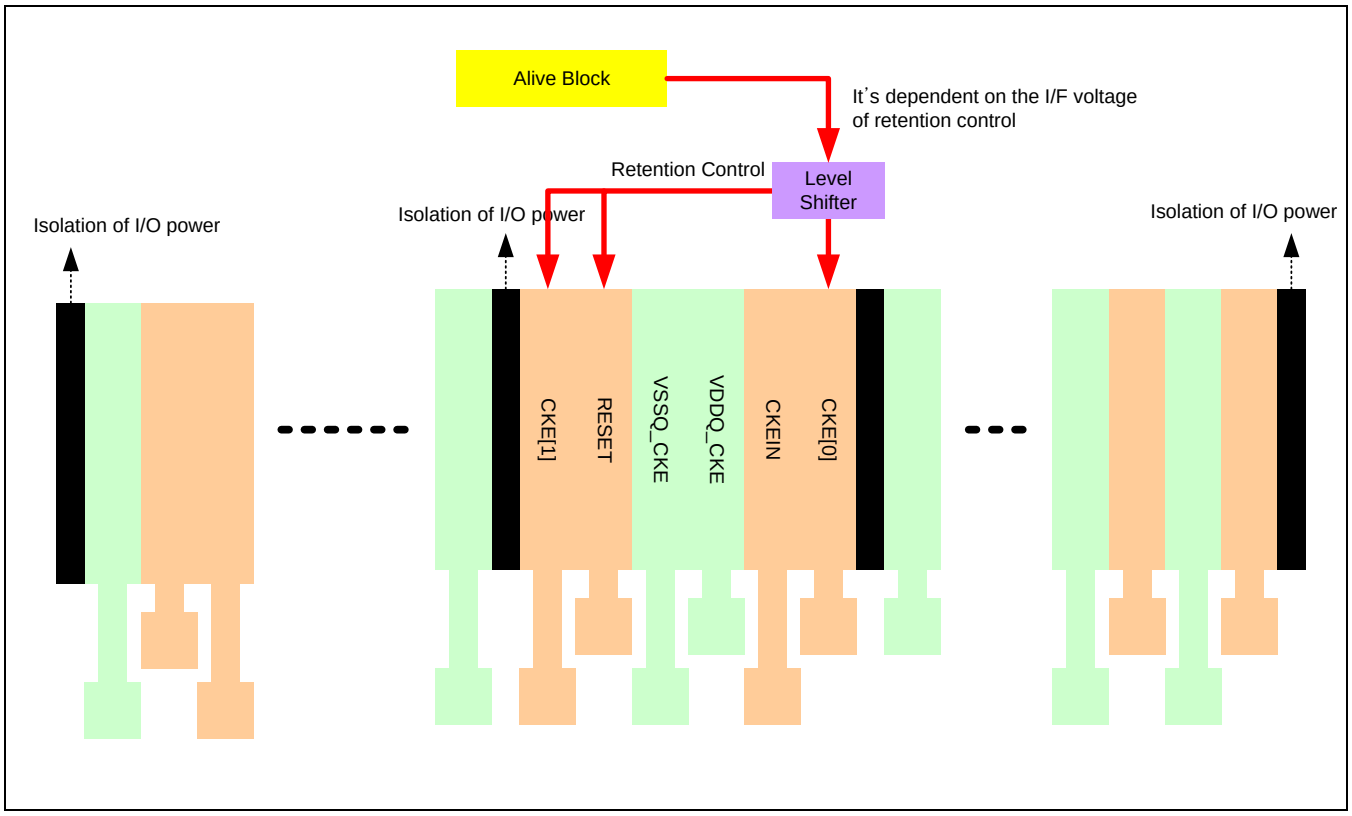

Figure 4-2 Internal CKE Retention Control

4.2 CKE CONTROL

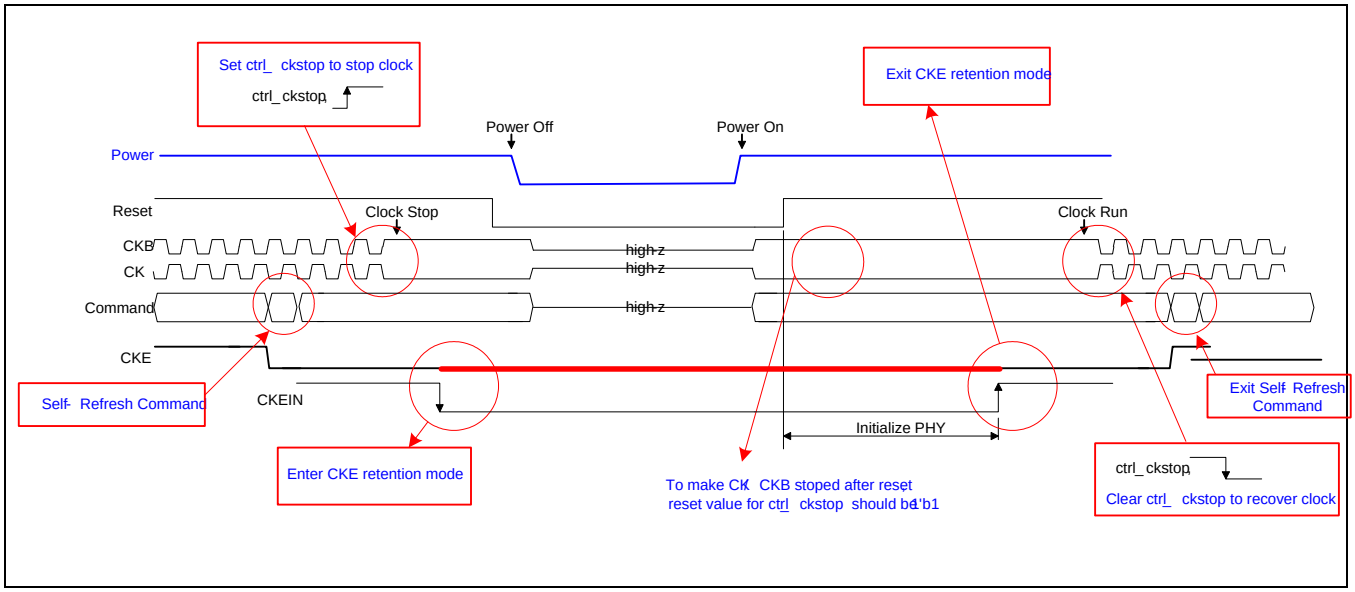

Figure 4-3 External CKE Retention Control Timing Example for LN32LP I/O

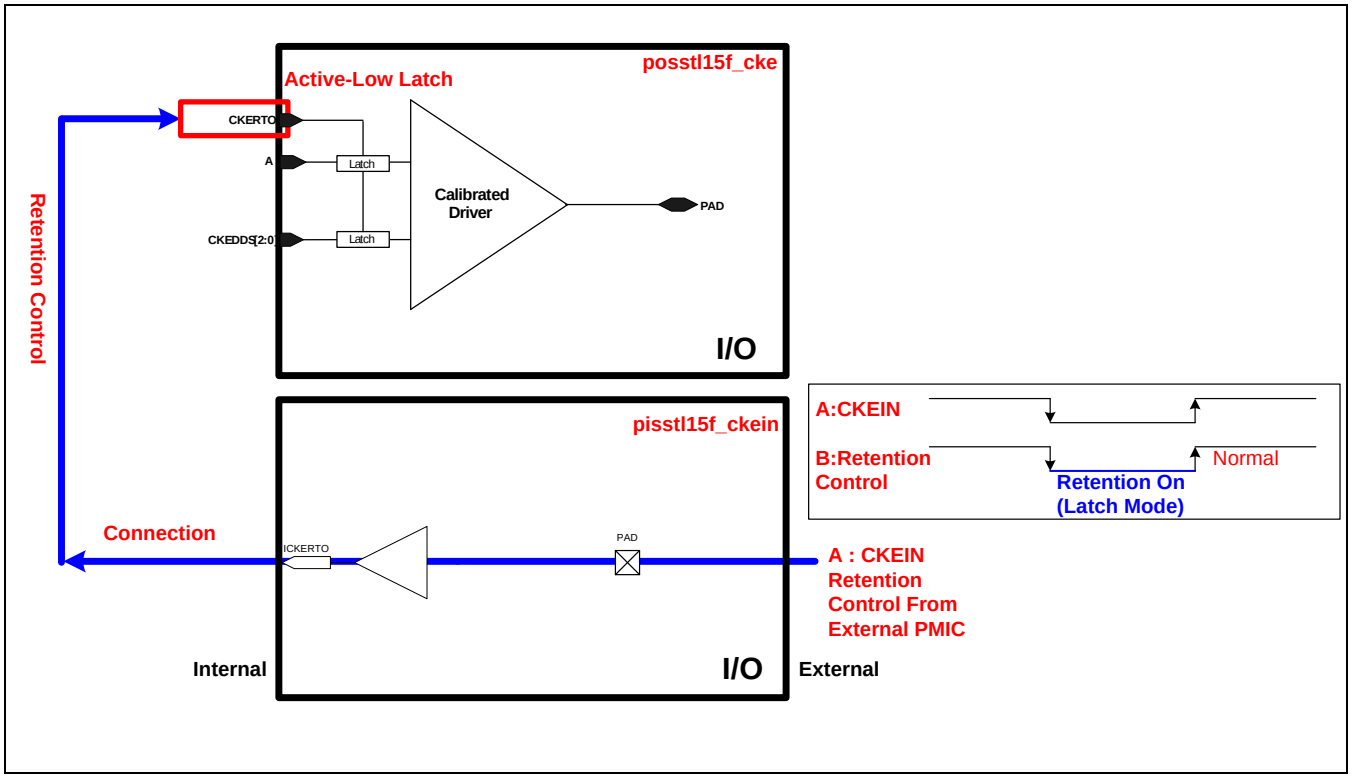

Figure 4-4 CKEIN Connection Example for LN32LP I/O

Figure shows the timing example of CKE retention control.

- Procedure
  - Enter Self-Refresh mode.
  - Set ctrl_ckstop to stop CK/CKB.
  - Set CKEIN to enter CKE retention mode.
  - Power-Off.
  - Power-On.
  - After reset is released, execute initialization.
  - Clear ctrl_ckstop to make clock run again.
  - Exit Self-Refresh mode.

5 LAYOUT

5.1 LAYOUT GUIDE

Layout guide is described in the table and figure.

Table 5-1 Layout Guide

Num	Item	Description
L0	Space between PHY and I/O	Should be less than 100um including routing channel.
L1	Signal Routing between PHY and I/O	PHY signals should be directly connected to I/O without any buffer.
L2	I/O placement	Place the I/O according to I/O allocation guide. * Sequence of I/O can be flipped. In this case, LPDDR2 PHY should also be flipped.
L3	Over-the-Cell Routing	Power: ≥ M7 Signal: ≥ Only DC signals can be routed with M7
L4	Power connection	Connect all power ports to the power ring.
L5	Clock Requirement	Clock should be generated by even-number division from PLL clock for almost 50:50 clock duty
L6	CTS buffer	"Clock Inverter Cell" should be used CTS buffer
L7	Clock Duty	Final duty of clock output I/O should be 47:53 ~ 53:47.
L8	Placement of clock source	PLL should not be placed in the opposite side of PHY. Should be placed near for low clock jitter.
L9	Clock Routing & Shielding	Should avoid noisy blocks like SRAM blocks and etc. Should not traverse the center of chip. Clock signal should be shielded with ground to prevent coupling noise and filled in de-coupling cell around clock cell on clock path (Figure 5-2)

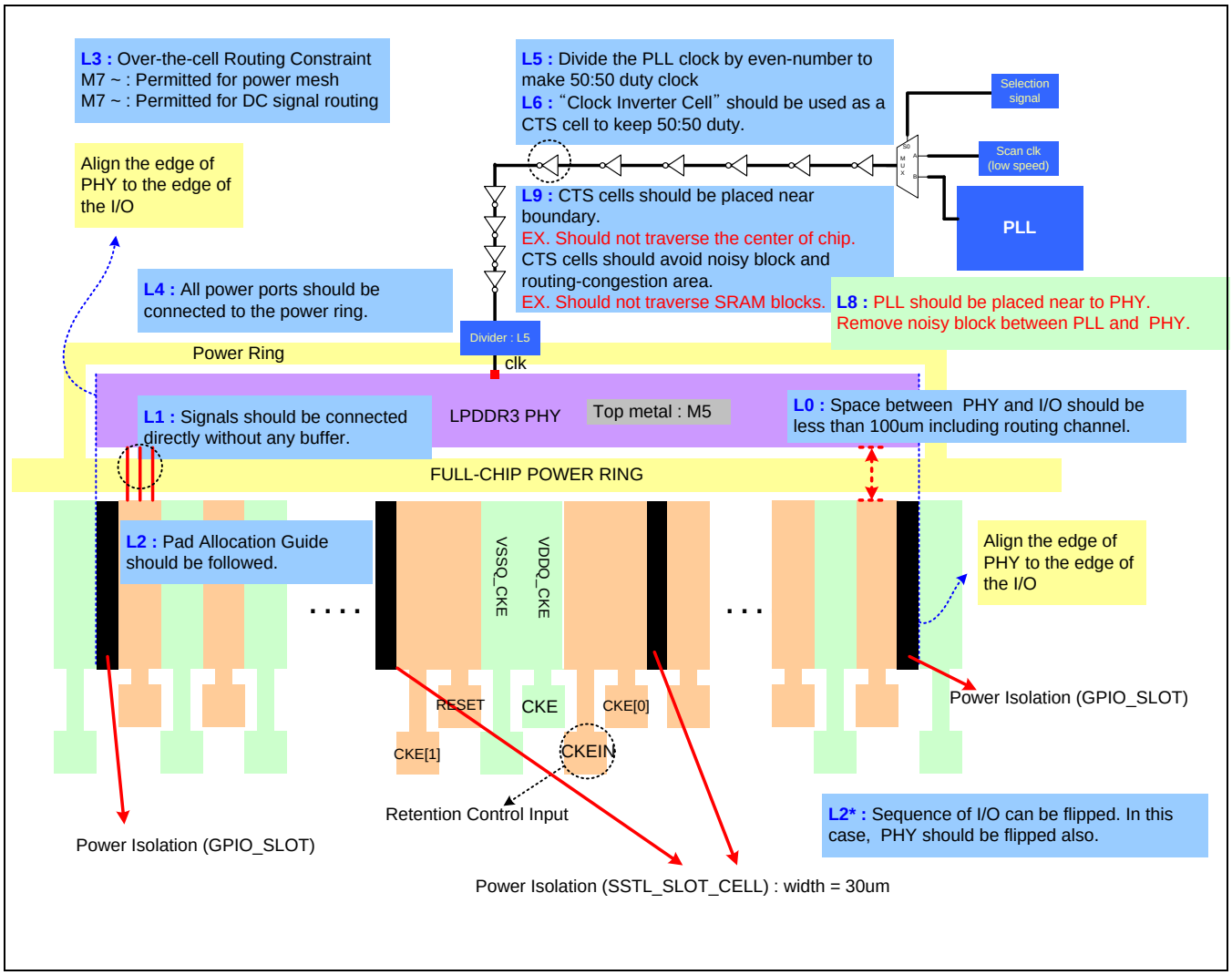

Figure 5-1 Layout Guide

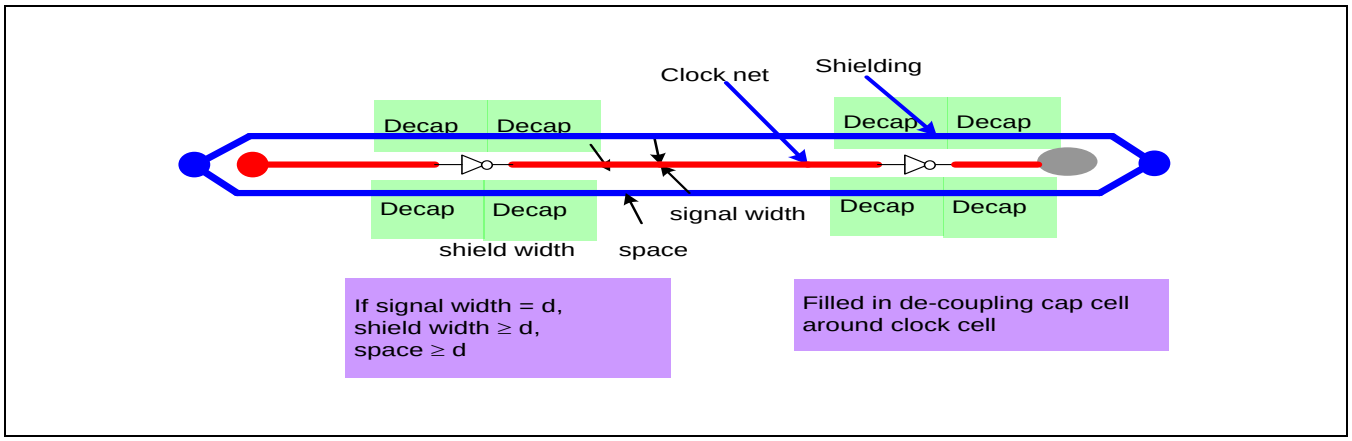

Figure 5-2 Clock shielding guide

5.2 PAD ALLOCATION

Additional excel file is provided for PAD allocation. Please, refer to the excel sheet.

5.3 CTS

CTS(Clock Tree Synthesis) depth should be considered in synthesis and CTS phase. CTS depth information is provided in the README file in the DK. Because the PHY includes the internal CTS depth(tPHYCTS), CTS depth from the clock source to the clock port of PHY should be tCTS – tPHYCTS (tCTS is the clock network delay). This early-point CTS should be considered in synthesis and layout. And to get 50:50 clock duty, even-number division is mandatory. At the same time, to maintain the 50:50 duty, clock-inverter cells should be used for CTS buffer.

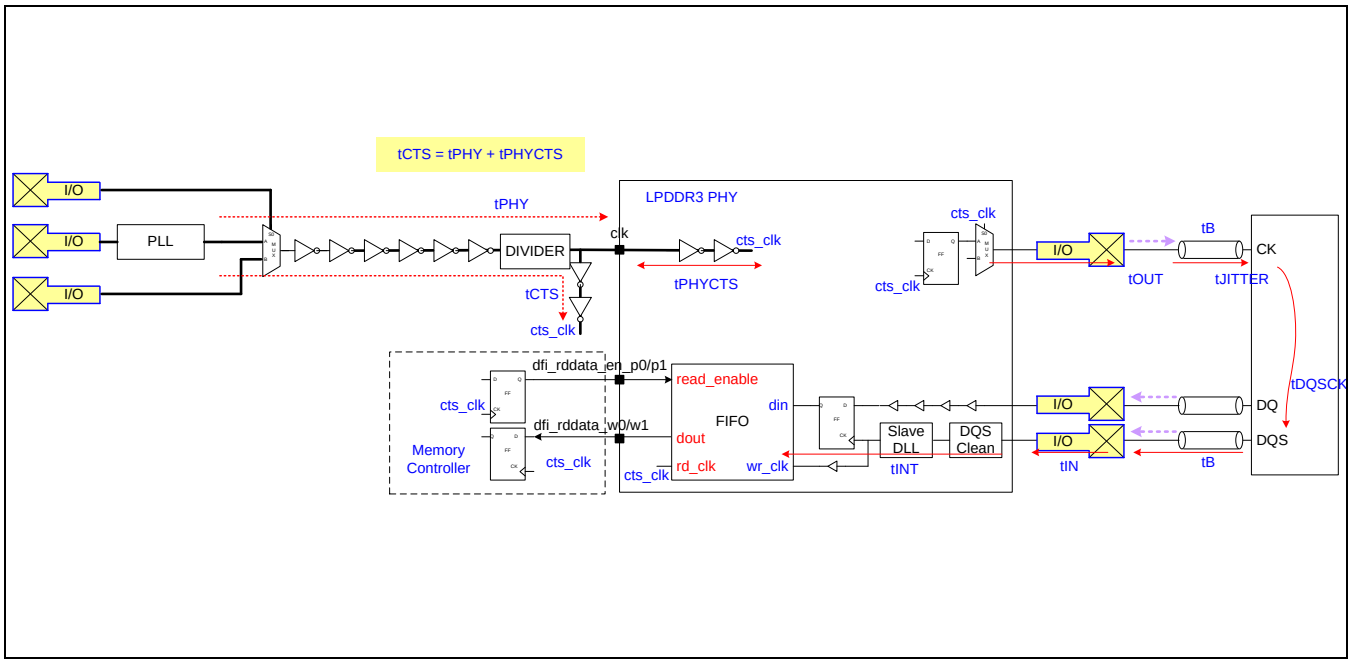

Figure 5-3 CTS

5.4 CLOCK DUTY AND JITTER

To meet the memory clock duty specification (45:55), right after the CTS phase, clock duty should be checked and corrected. Duty at the B point should be near to 50:50(at least, should be 49:51 ~ 51:49) to meet the 45:55 duty specification at the C and D point in any corner condition.

Output of divider is almost nearly 50:50 clock duty. So, divider location recommends most nearly the input clock port of PHY. (In this case PLL fout needs always double of target clock frequency.)

Caution: Clock Duty in feedback test mode should be also 49:51 ~ 51:49 to meet the duty requirement Please check Clock Duty by using "PSI Jitter" instead of STA.

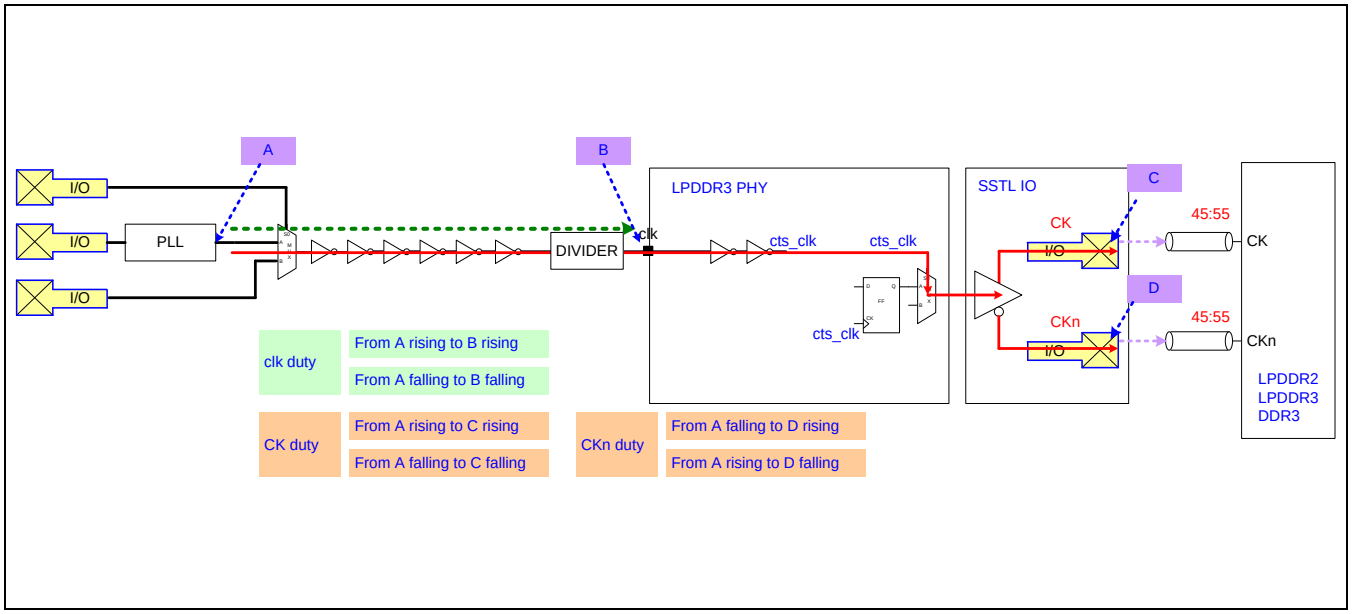

Figure 5-4 Clock Duty

The total on-chip jitter at "E" (including PLL, clock distribution network and DDRPHY jitter) should be under 3%. So please meet the following jitter margin for clock distribution network at 800MHz.

Table 5-2 The requirement for the total on-chip jitter

Clock Period	PLL(1%)	Clock Distribution Network	DDRPHY(1%)	Totall Jitter(RSS)
1250ps	12.5ps	33.1ps	12.5ps	37.5ps

5.5 CLK_EN

Because "clk_en" is the signal with 800MHz interface timing, it is very difficult to meet the timing requirement during PnR stage. So, please make sure to meet the following guide in Figure 5-5.

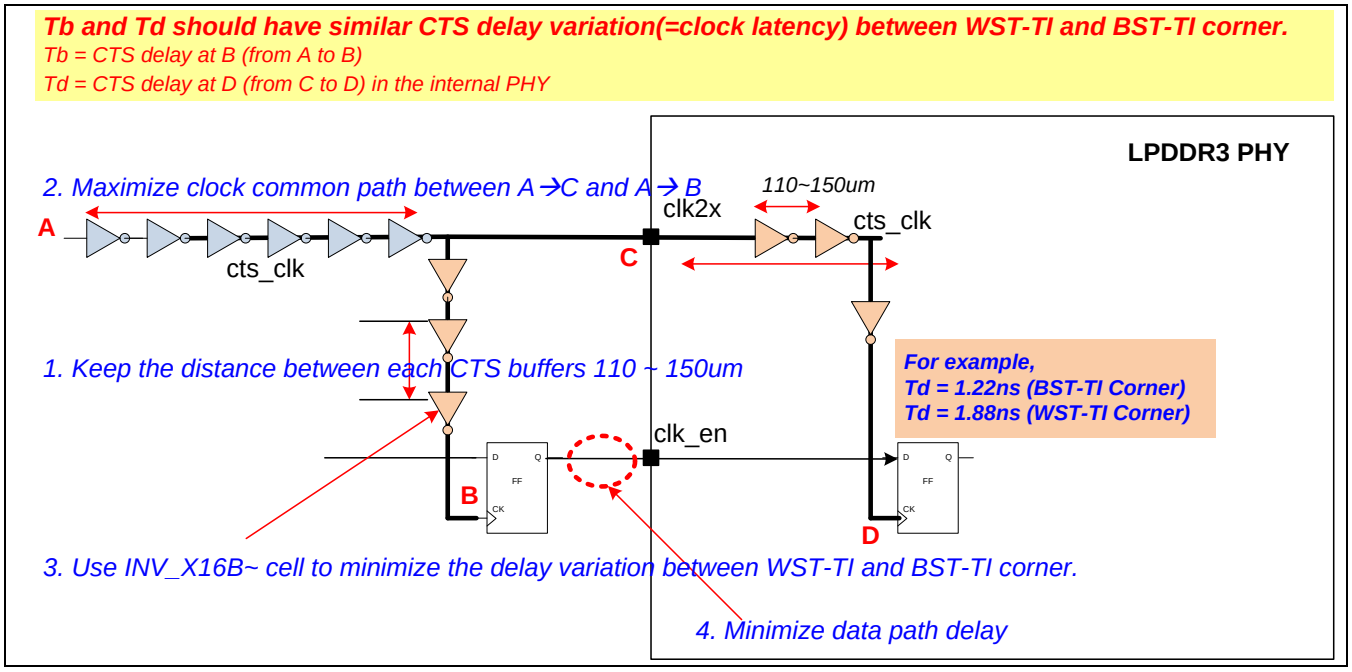

Figure 5-5 Guide to meet the timing requirement for "clk_en"

6 PACKAGE AND BOARD GUIDE

6.1 OFF-CHIP TIMING MARGIN

The off-chip timing margin should be maximized through the PI/SI analysis. Please contact Design Technology team for more details about PI/SI Flow.

6.2 TRANSMISSION LINE SKEW MANAGEMENT

In Table 6-1, Skew in picoseconds is translated to physical length on the PCB.

Table 6-1 Skew Including Package and Board

Group	Signals	Skew	From	To
G0_1	CK/CKB	±10ps	Pad	Memory Pin
G0_2	PDQS[N]/NDQS[N]	±10ps	Pad	Memory Pin
G1	PDQS[N]/NDQS[N] DQ[(N+1)*8-1:N*8] DM[N]	±25ps from PDQS[N]/NDQS[N]	Pad	Memory Pin
G2	CK/CKB, ADCT[15:0], RAS, CAS, CKE, WEN	±25ps from CK/CKB	Pad	Memory Pin
G3 (LPDDR2/LPDDR3)	CK/CKB, ADCT[9:0]	±25ps from CK/CKB	Pad	Memory Pin
G4	P/NDQS[NS-1:0], CK/CKB	-100ps from CK/CKB	Pad	Memory Pin

NOTE: N means 0,1 … NS-1, NS is the number of data_slice. For example if using 32bit PHY, NS will be 4.
CK/CKB should be delayed than P/NDQS[NS-1:0] (G4)

6.3 PACKAGE

VDDQ/VSSQ is power/ground for 1.2V I/O and VDD/VSS is power/ground for the core. Those power pads will be connected to power ring. And it's recommended that VREF pads should be connected to VREF ring as shown *Figure 6-1* to reduce the coupling noise between VREF and the other signals. Decoupling capacitor is recommended between power and ground to reduce SSN. VDDQZQ and VSSQZQ are analog power for ZQ IO. Thus, to isolate them from digital switching noise, they should not be connected to power ring but assigned to separate ballouts.

Wires of VREF, VDDQZQ, VSSQZQ and ZQ should have enough space away from adjacent signal wires to reduce the coupling noise

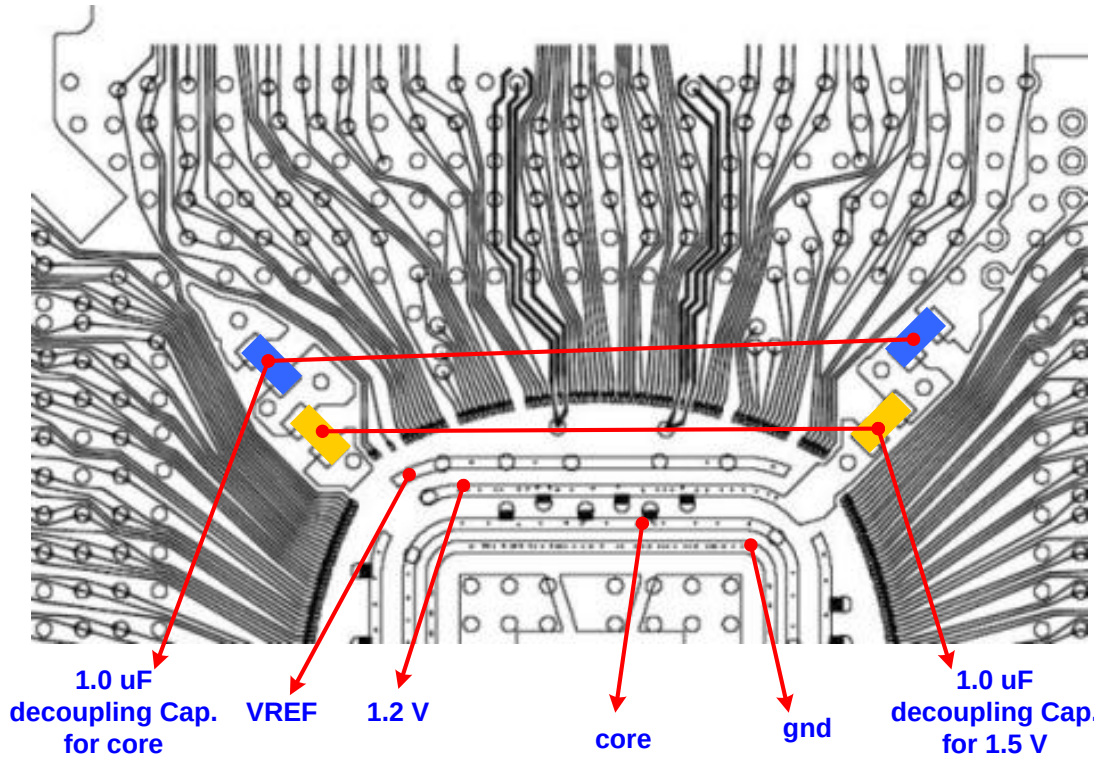

Figure 6-1 Connection between PADs and power ring

6.4 SHIELDING

Strobe and clock signals should be shielded with ground to prevent coupling noise.

Table 6-2 Signal List for Shielding

Signals	Description
PDQS/NDQS[0]	Ground shielding to prevent coupling noise
PDQS /NDQS[1]	Ground shielding to prevent coupling noise
PDQS /NDQS[2] (for 32-bit)	Ground shielding to prevent coupling noise
PDQS /NDQS[3] (for 32-bit)	Ground shielding to prevent coupling noise
CK/CKB	Ground shielding to prevent coupling noise
VREF	Ground shielding to prevent coupling noise
VDDQZQ, VSSQZQ	Ground shielding to prevent coupling noise
ZQ	Ground shielding to prevent coupling noise

If the signal width is d, the ground shielding width and space should be equal or more than d. On the package, ground shield should have two vias, which connects to ground plane, on the each end side.

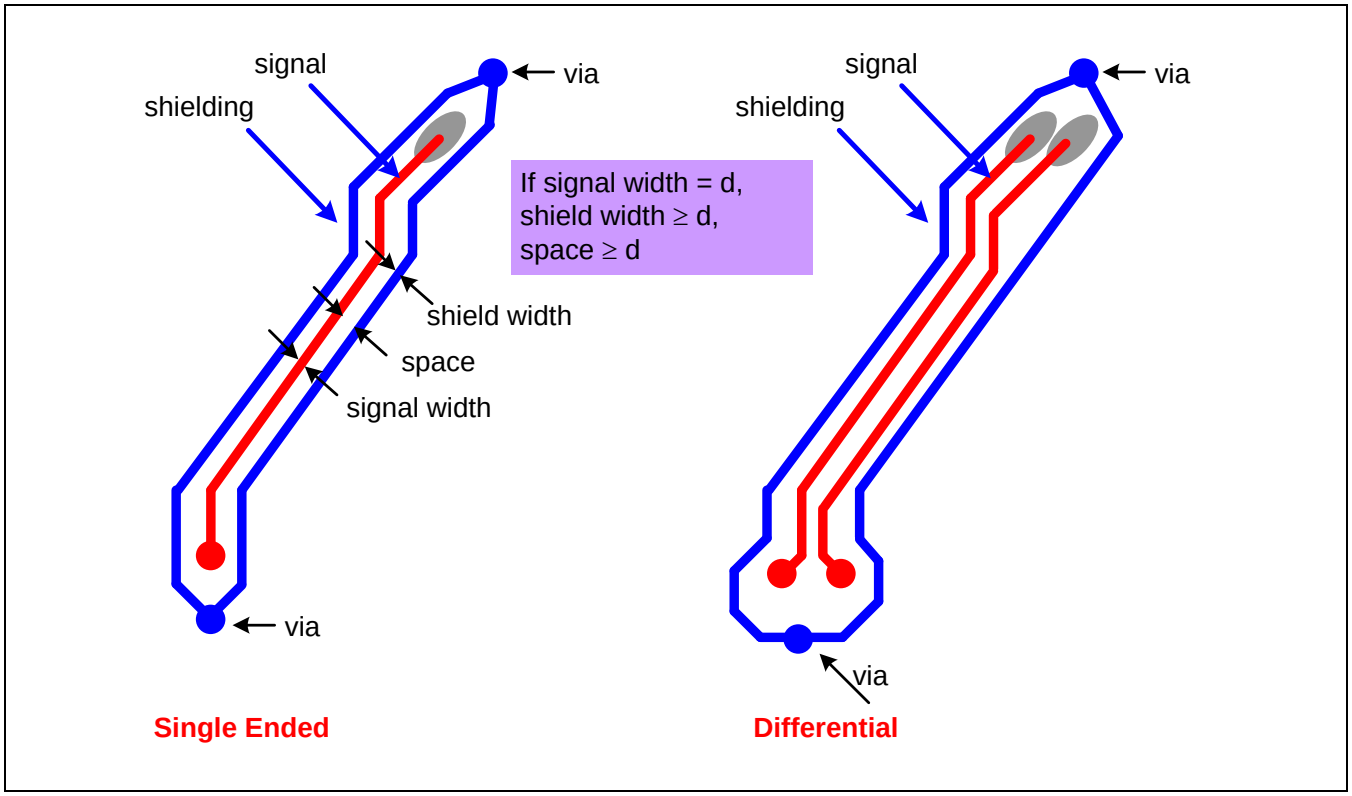

Figure 6-2 Package & Board Shielding Guide

6.5 GROUND PLANE OF THE PACKAGE

It is highly recommended to merge the ground plane to reduce the power and coupling noise.

6.6 SSN SIMULATION

6.6.1 SSN SIMULATION FOR LPDDR2/LPDDR3/DDR3

To prevent the power and signal integrity problem, package and board simulation should be conducted. For the worst write case, the input waveform pattern of the address, control and data should be input as shown in Figure 6-3.

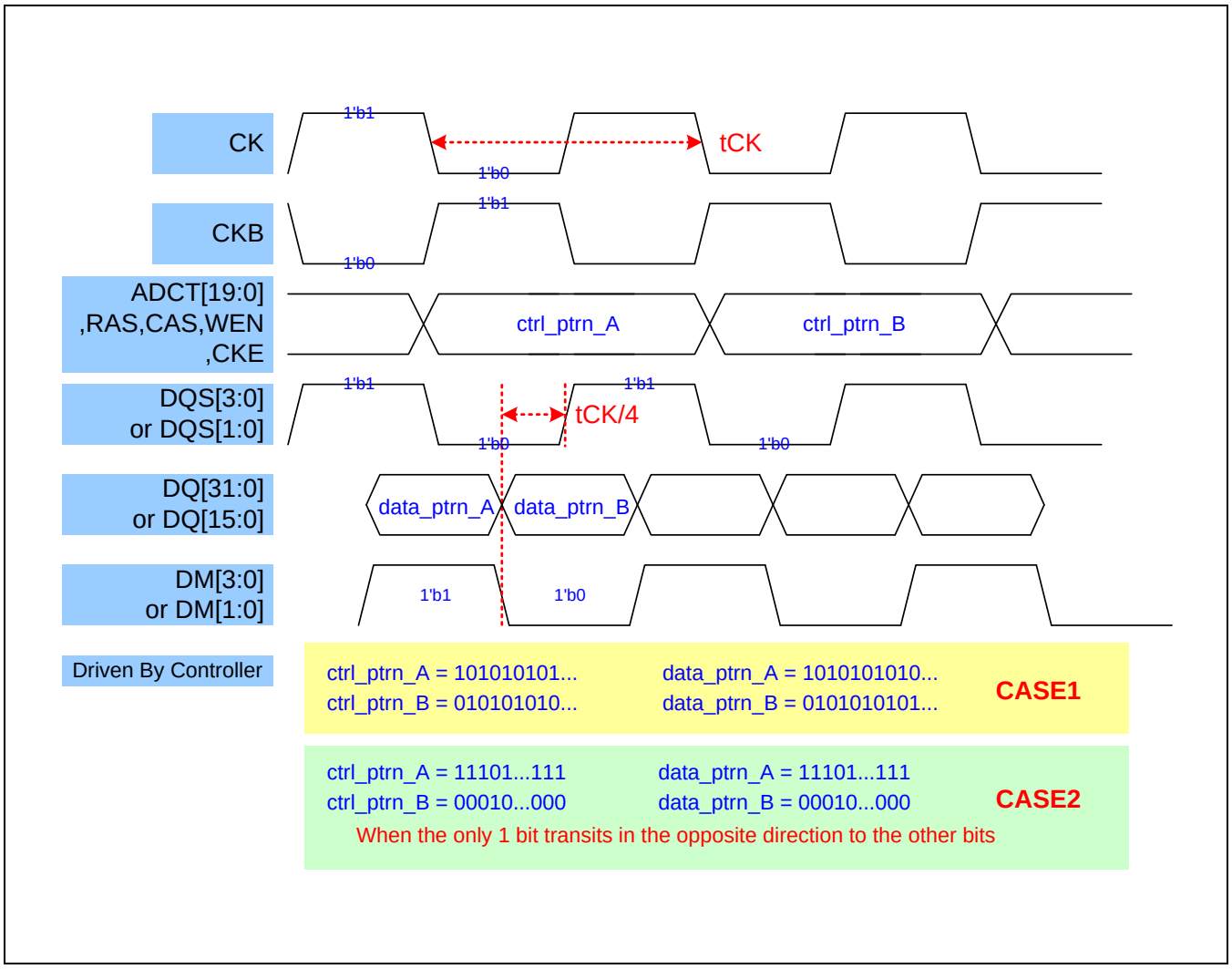

Figure 6-3 Spice Simulation Pattern for SSN Simulation for LPDDR2/LPDDR3/DDR3

With the guided input pattern, tSKEW_C(control signal skew) and tSKEW_D0~D3(data skew) should be checked whether they are less than 600ps and 300ps, respectively. And Vd/Vr(signal voltage drop/rise) should be checked whether they meet the VIL(AC)/VIH(AC) requirement as shown in Figure 6-4. Generally, they are caused by power/ground fluctuation and coupling noise.

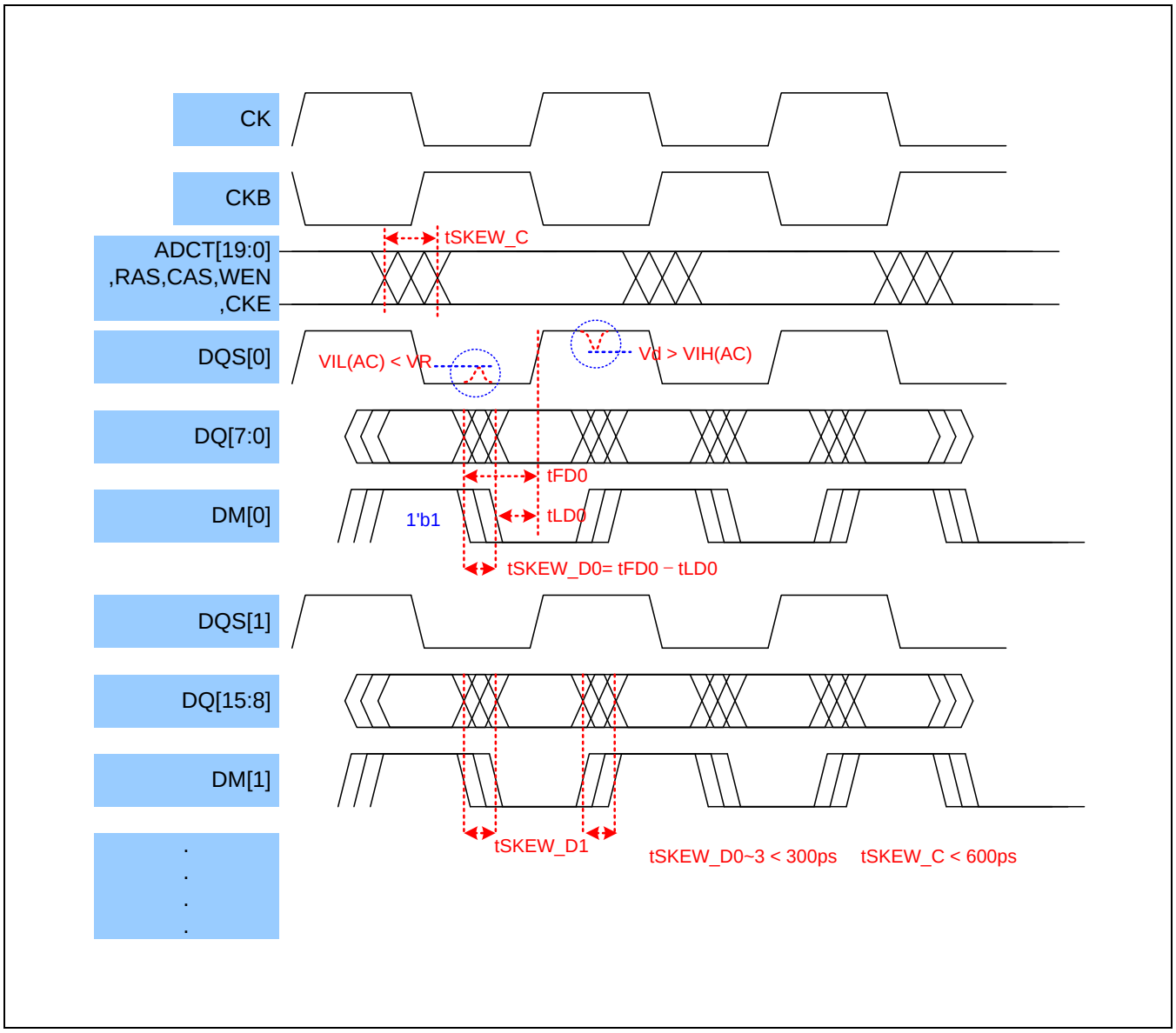

Figure 6-4 Check Points of SSN Simulation for LPDDR2/LPDDR3/DDR3

6.6.2 SSN SIMULATION FOR LPDDR3

For the worst write case, the input waveform pattern of LPDDR2 should be input as shown in Figure 6-5.

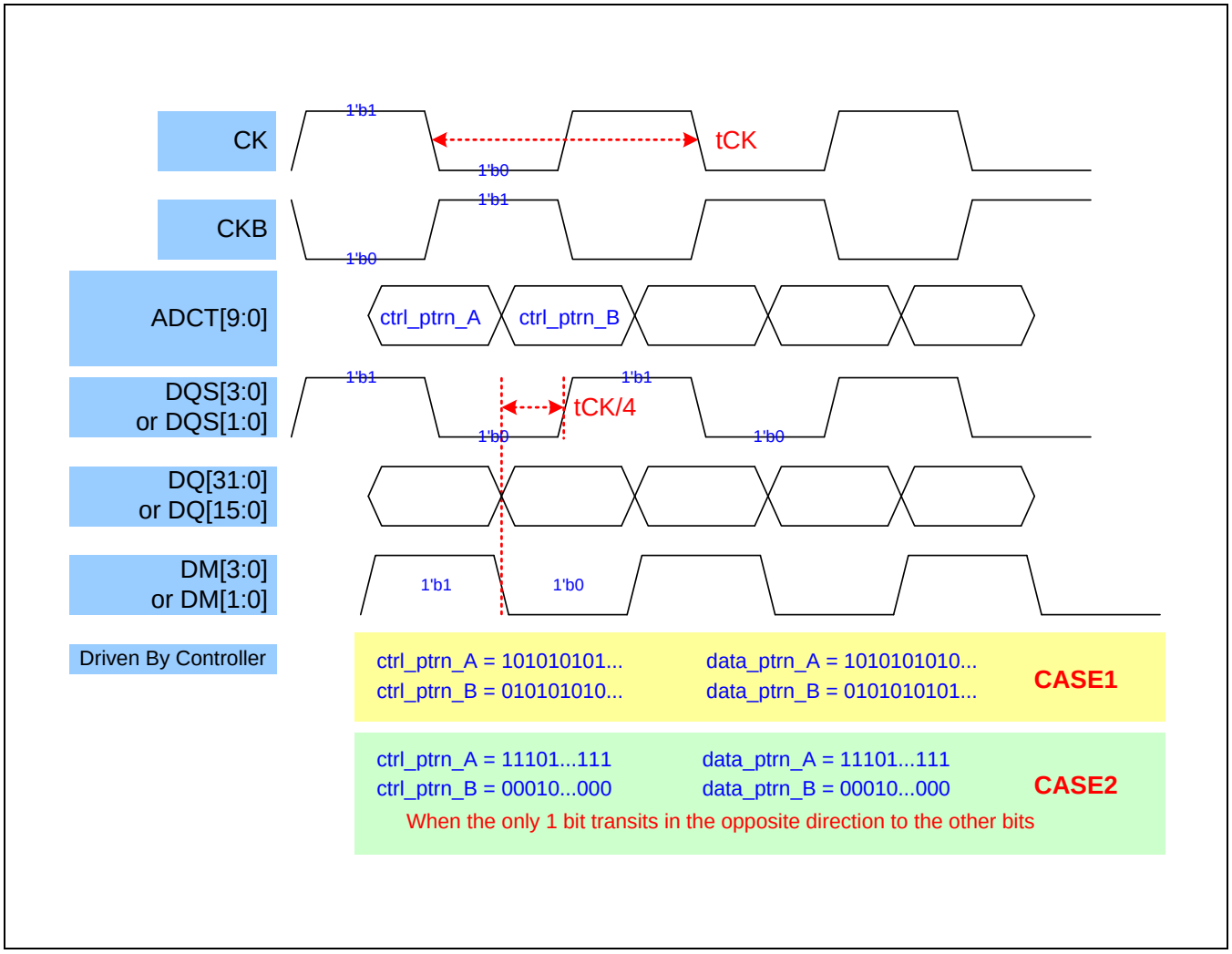

Figure 6-5 Spice Simulation Pattern for SSN Simulation for LPDDR3

With the guided input pattern, tSKEW_C(control signal skew) and tSKEW_D0~D3(data skew) should be checked whether they are less than 300ps. And Vd/Vr(signal voltage drop/rise) should be checked whether they meet the VIL(AC)/VIH(AC) requirement as shown in Figure 6-6. Generally, they are caused by power/ground fluctuation and coupling noise.

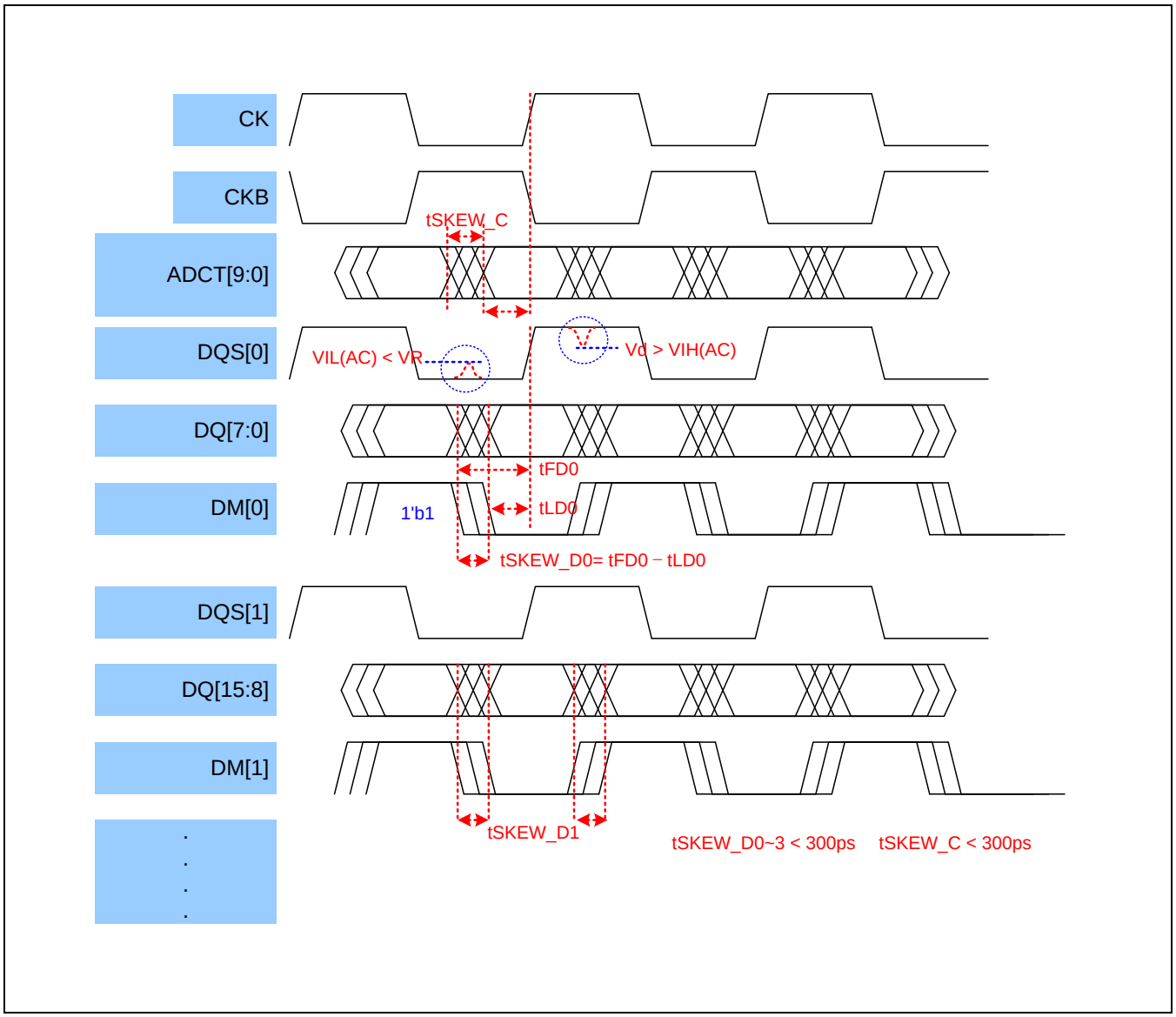

Figure 6-6 Check Points of SSN Simulation for LPDDR3