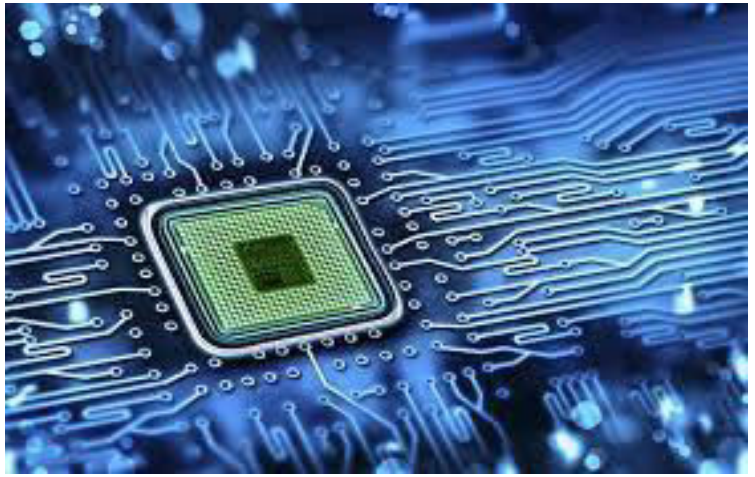
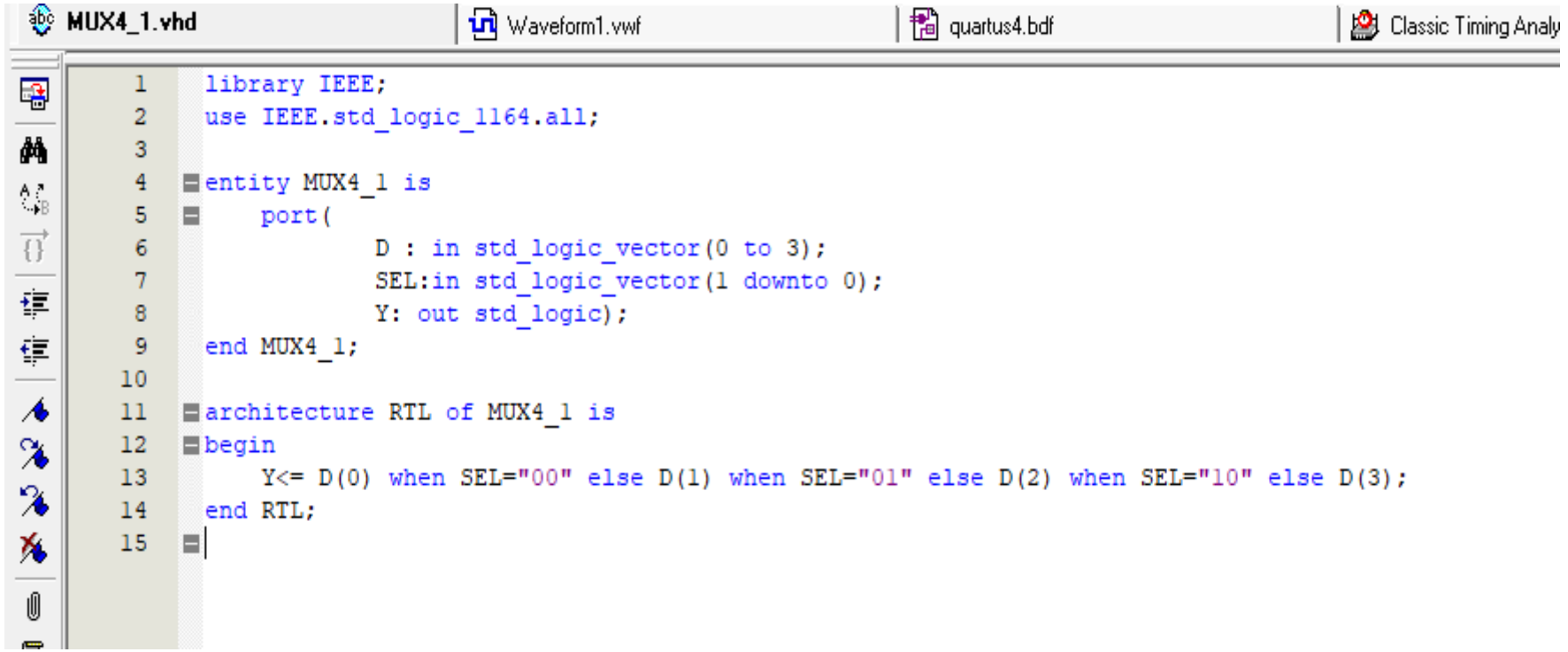
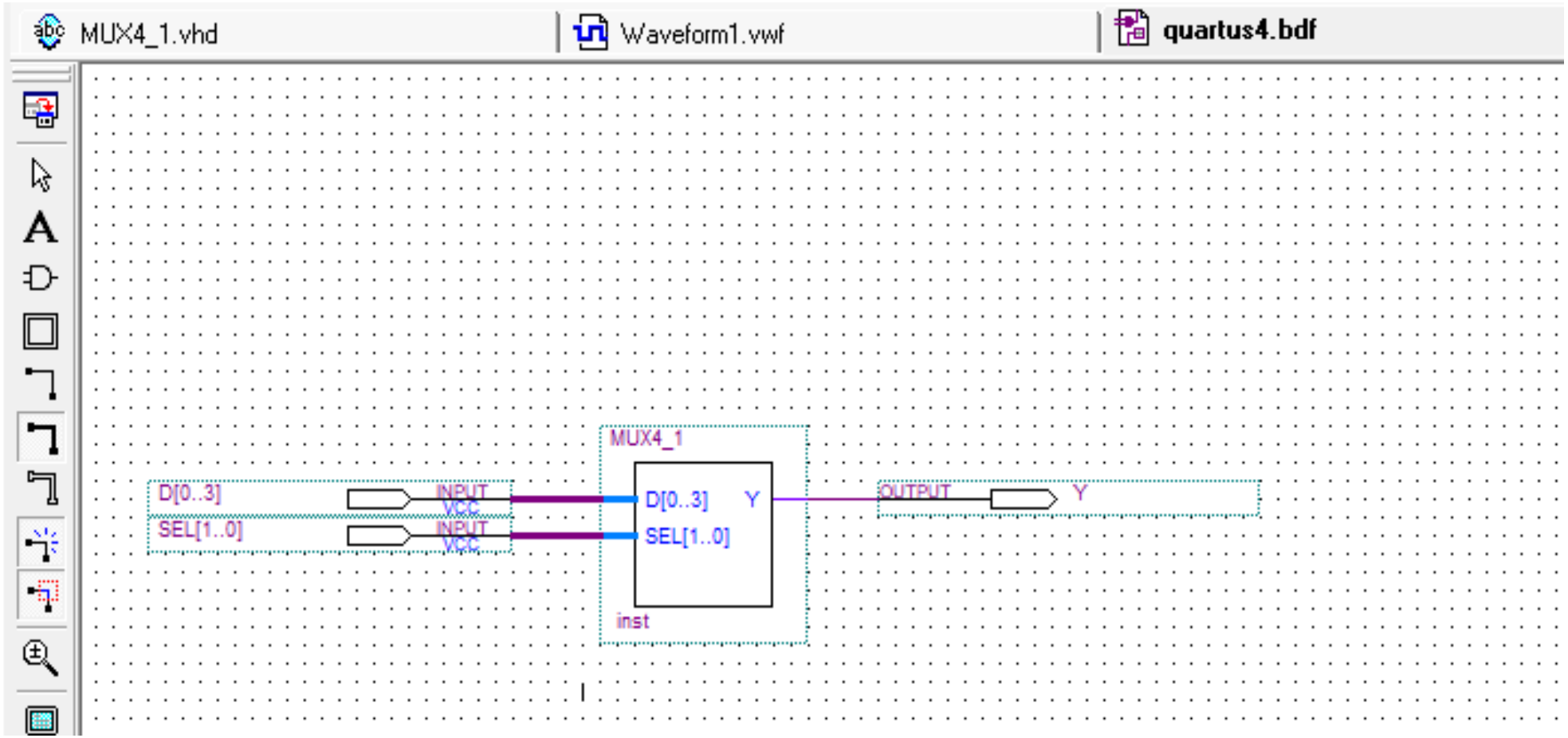
QUARTUS 4

ΧΡΗΣΤΟΣ ΚΑΡΑΓΙΑΝΝΙΔΗΣ ΑΜ 4375
ΜΥΡΩΝΑΣ ΚΟΥΦΟΠΟΥΛΟΣ ΑΜ 4398

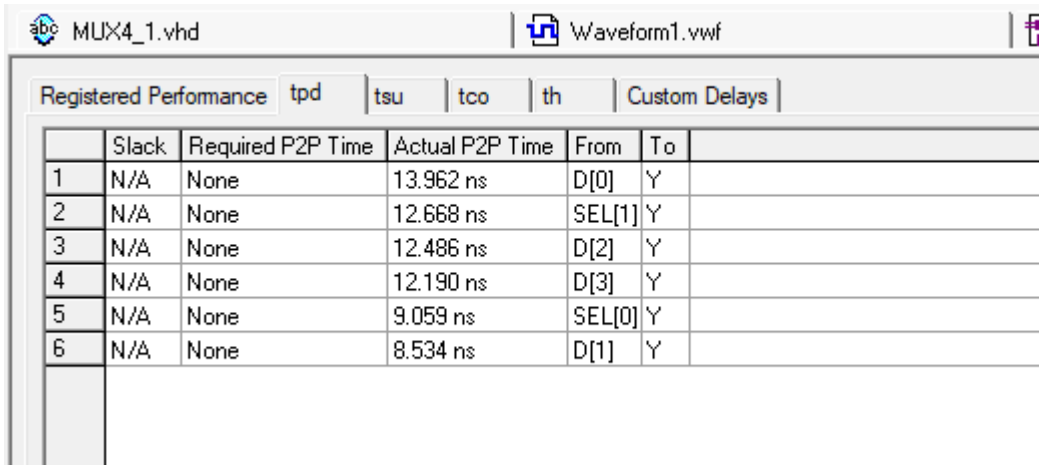


ΜΕΡΟΣ 1^{Ο} : Συνδιαστικά Κυκλώματα
Ερώτημα 1^{ο}



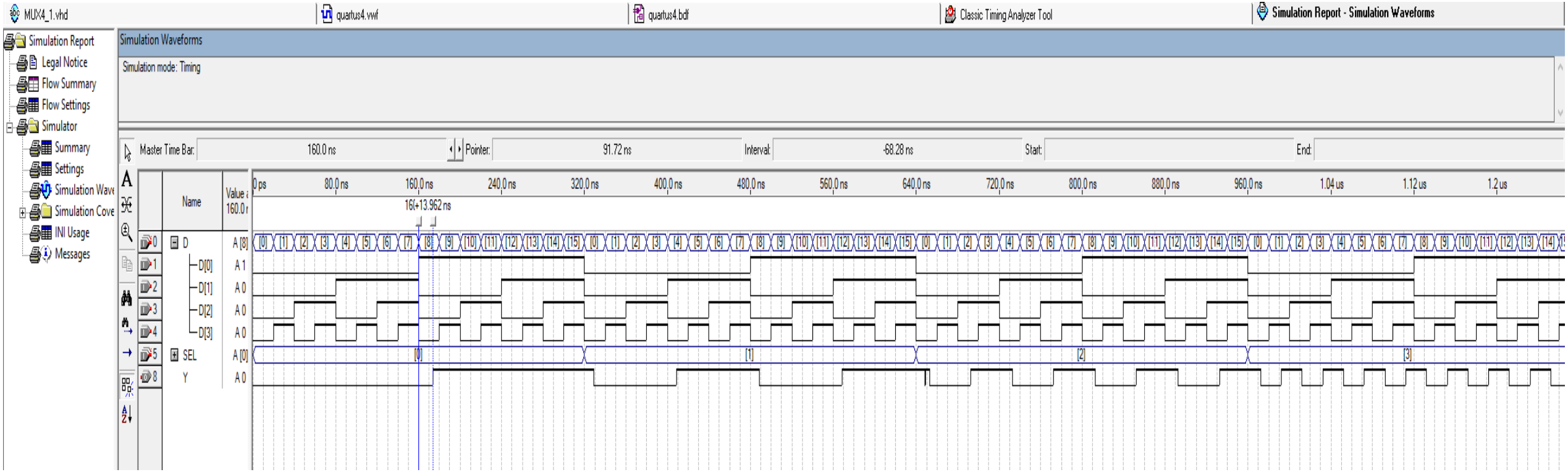

MUX4_1.vhd
Waveform1.vwf
quartus4.bdf
MUX4_1
D[0..3]
SEL[1..0]
INPUT
VCC
INPUT
VCC
D[0..3]
SEL[1..0]
Y
inst
OUTPUT
Y

ΣΤΑΤΙΚΗ ΧΡΟΝΙΚΉ ΑΝΑΛΥΣΗ



	Slack	Required P2P Time	Actual P2P Time	From	To
1	N/A	None	13.962 ns	D[0]	Y
2	N/A	None	12.668 ns	SEL[1]	Y
3	N/A	None	12.486 ns	D[2]	Y
4	N/A	None	12.190 ns	D[3]	Y
5	N/A	None	9.059 ns	SEL[0]	Y
6	N/A	None	8.534 ns	D[1]	Y

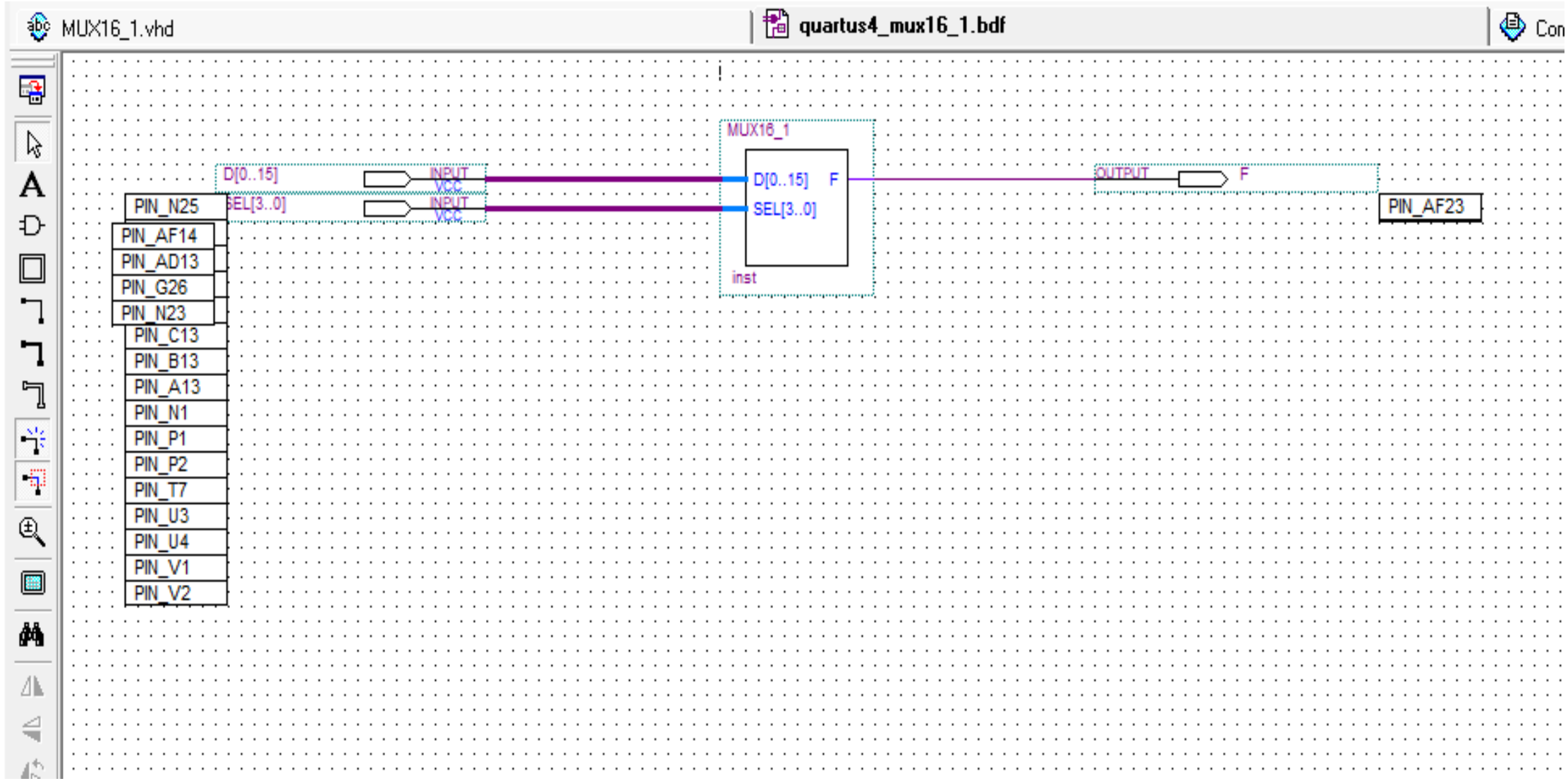
Η μέγιστη χρονική καθυστέρηση του κυκλώματος ειναι 13,962ns από το D[0] στο Y


MUX4_1.vhd
quartus4.vwf
quartus4.bdf
Classic Timing Analyzer Tool
Simulation Report - Simulation Waveforms
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Wave
Simulation Cove
INI Usage
Messages
Simulation Waveforms
Simulation mode: Timing
Master Time Bar: 160.0 ns
Pointer: 91.72 ns
Interval: -68.28 ns
Start:
End:
Name
Value a
160.0 r
0 ps
80.0 ns
160.0 ns
240.0 ns
320.0 ns
400.0 ns
480.0 ns
560.0 ns
640.0 ns
720.0 ns
800.0 ns
880.0 ns
960.0 ns
1.04 us
1.12 us
1.2 us
16(+13.962 ns
0
D
A [8]
1
D[0]
A 1
2
D[1]
A 0
3
D[2]
A 0
4
D[3]
A 0
5
SEL
A [0]
8
Y
A 0
[0]
[1]
[2]
[3]

ΜΕΡΟΣ 1^{Ο} : Συνδιαστικά Κυκλώματα
Ερώτημα 2^{ο}

MUX4_1.vhd | MUX16_1.vhd | quartus4.bdf

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  ENTITY MUX16_1 is port(
5          D : in std_logic_vector (0 to 15);
6          SEL: in std_logic_vector (3 downto 0);
7          F: out std_logic);
8  END MUX16_1;
9
10 ARCHITECTURE RTL OF MUX16_1 IS
11 COMPONENT MUX4_1
12     port(
13         D : in std_logic_vector (0 to 3);
14         SEL: in std_logic_vector (1 downto 0);
15         Y: out std_logic);
16 END COMPONENT;
17
18     SIGNAL Y: STD_LOGIC_VECTOR(0 to 3);
19
20 BEGIN
21
22 u0:MUX4_1 port map(D=>D(0 to 3), SEL=> Sel(1 downto 0), Y=>Y(0));
23 u1:MUX4_1 port map(D=>D(4 to 7), SEL=> Sel(1 downto 0), Y=>Y(1));
24 u2:MUX4_1 port map(D=>D(8 to 11), SEL=> Sel(1 downto 0), Y=>Y(2));
25 u3:MUX4_1 port map(D=>D(12 to 15), SEL=> Sel(1 downto 0), Y=>Y(3));
26 u4:MUX4_1 port map(D=>Y, SEL=> Sel(3 downto 2), Y=>F);
27
28 END RTL;
```


MUX16_1.vhd
quartus4_mux16_1.bdf
Con
MUX16_1
D[0..15]
INPUT
VCC
SEL[3..0]
INPUT
VCC
D[0..15]
F
SEL[3..0]
inst
OUTPUT
F
PIN_AF23
PIN_N25
PIN_AF14
PIN_AD13
PIN_G26
PIN_N23
PIN_C13
PIN_B13
PIN_A13
PIN_N1
PIN_P1
PIN_P2
PIN_T7
PIN_U3
PIN_U4
PIN_V1
PIN_V2

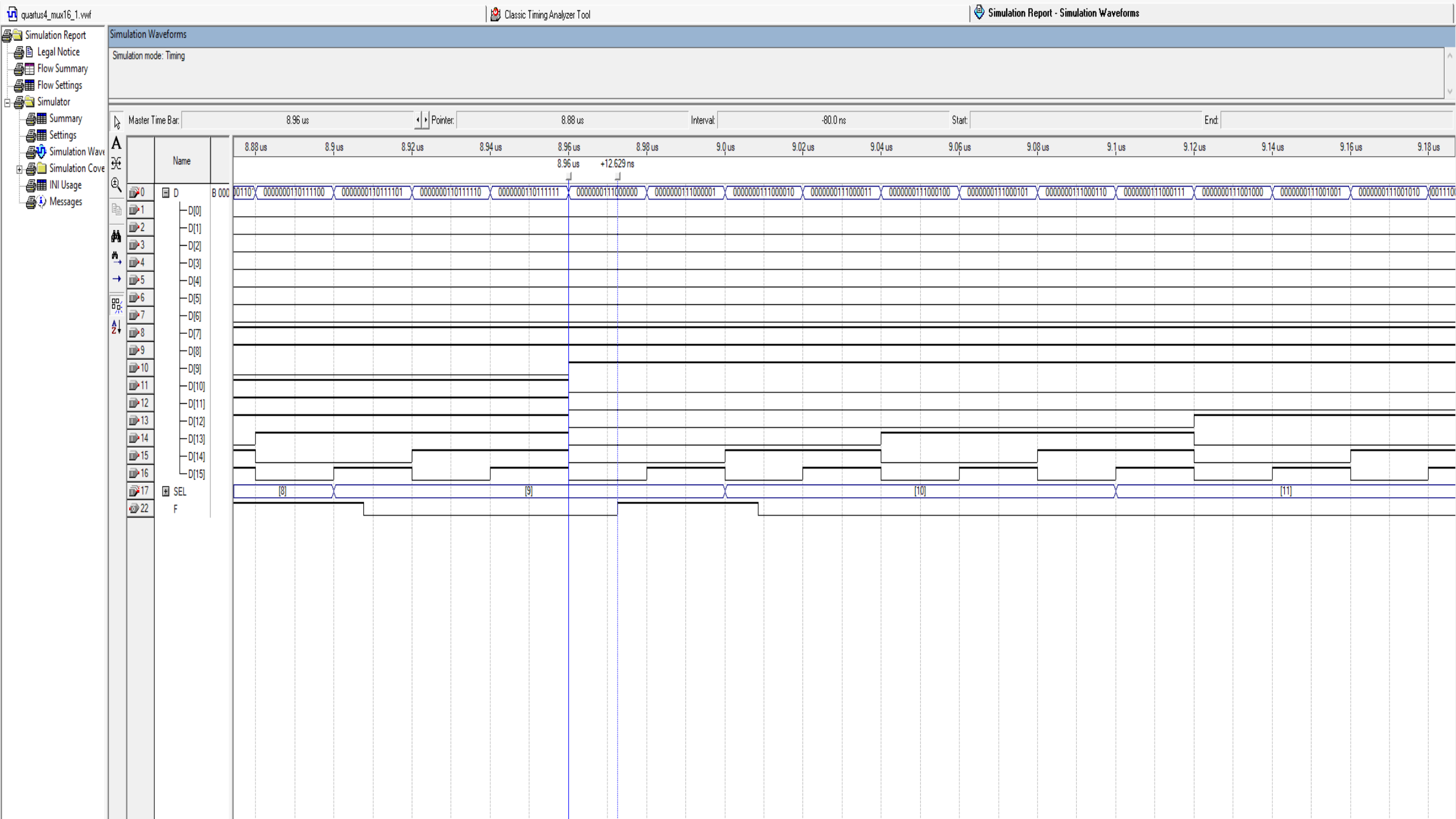
ΣΤΑΤΙΚΗ ΧΡΟΝΙΚΉ ΑΝΑΛΥΣΗ

MUX16_1.vhd | quartus4_mux16_1.bdf

Registered Performance | tpd | tsu | tco | th | Custom Delays

	Slack	Required P2P Time	Actual P2P Time	From	To
1	N/A	None	12.629 ns	D[9]	F
2	N/A	None	12.324 ns	D[14]	F
3	N/A	None	12.261 ns	D[4]	F
4	N/A	None	11.964 ns	D[13]	F
5	N/A	None	11.948 ns	D[6]	F
6	N/A	None	11.824 ns	D[10]	F
7	N/A	None	11.562 ns	D[11]	F
8	N/A	None	11.393 ns	D[8]	F
9	N/A	None	11.273 ns	D[15]	F
10	N/A	None	11.108 ns	SEL[2]	F
11	N/A	None	10.986 ns	D[12]	F
12	N/A	None	10.887 ns	D[7]	F
13	N/A	None	10.871 ns	D[5]	F
14	N/A	None	10.188 ns	SEL[3]	F
15	N/A	None	9.577 ns	D[1]	F
16	N/A	None	9.132 ns	D[0]	F
17	N/A	None	8.548 ns	SEL[0]	F
18	N/A	None	8.532 ns	SEL[1]	F
19	N/A	None	8.251 ns	D[2]	F
20	N/A	None	7.608 ns	D[3]	F

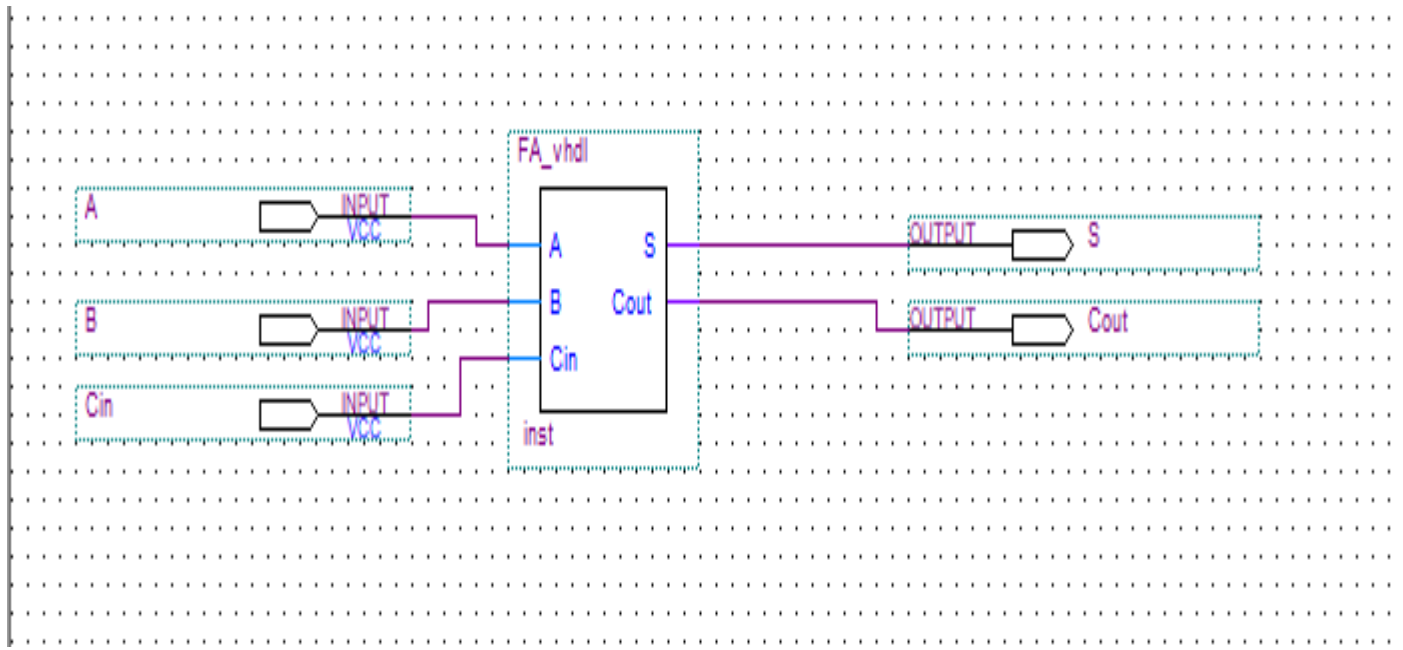
Η μέγιστη χρονική καθυστέρηση είναι 12,629ns από το D[9] στο F.


quartus4_mux16_1.vwf
Classic Timing Analyzer Tool
Simulation Report - Simulation Waveforms
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Wave
Simulation Cove
INI Usage
Messages
Simulation Waveforms
Simulation mode: Timing
Master Time Bar: 8.96 us
Pointer: 8.88 us
Interval: -80.0 ns
Start:
End:
Name
D
D[0]
D[1]
D[2]
D[3]
D[4]
D[5]
D[6]
D[7]
D[8]
D[9]
D[10]
D[11]
D[12]
D[13]
D[14]
D[15]
SEL
F
8.88 us
8.9 us
8.92 us
8.94 us
8.96 us
8.98 us
9.0 us
9.02 us
9.04 us
9.06 us
9.08 us
9.1 us
9.12 us
9.14 us
9.16 us
9.18 us
+12.629 ns
0000000110111100
0000000110111101
0000000110111110
0000000110111111
0000000111000000
0000000111000001
0000000111000010
0000000111000011
0000000111000100
0000000111000101
0000000111000110
0000000111000111
0000000111001000
0000000111001001
0000000111001010
[8]
[9]
[10]
[11]

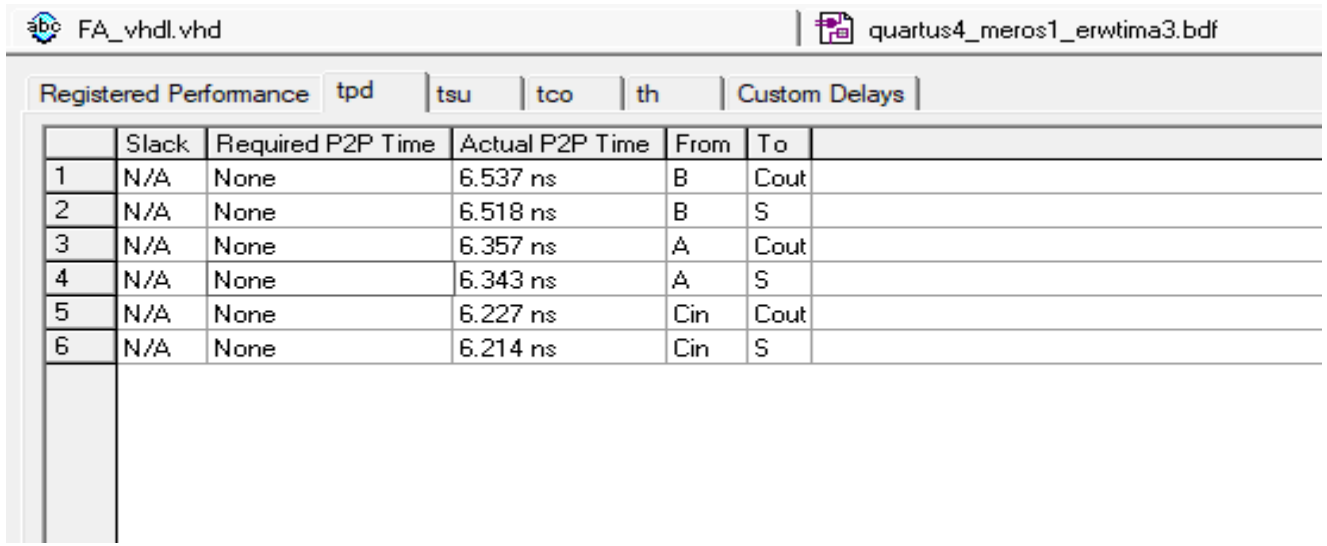
ΜΕΡΟΣ 1^{Ο} : Συνδιαστικά Κυκλώματα
Ερώτημα 3^{ο}

FA_vhdl.vhd | Compilation Report - Flow Summary

```
1   library IEEE;
2   use IEEE.STD_LOGIC_1164.ALL;
3
4   entity FA_vhdl is
5    port (
6    A : in STD_LOGIC;
7    B : in STD_LOGIC;
8    Cin : in STD_LOGIC;
9    S : out STD_LOGIC;
10   Cout : out STD_LOGIC);
11  end FA_vhdl;
12
13  architecture comp of FA_vhdl is
14
15  begin
16
17   S <= A XOR B XOR Cin ;
18   Cout <= (A AND B) OR (Cin AND A) OR (Cin AND B) ;
19
20  end comp;
21
```


FA_vhdl
A
INPUT
VCC
B
INPUT
VCC
Cin
INPUT
VCC
A
B
Cin
S
Cout
inst
OUTPUT
S
OUTPUT
Cout

ΣΤΑΤΙΚΗ ΧΡΟΝΙΚΗ ΑΝΑΛΥΣΗ


FA_vhdl.vhd

quartus4_meros1_erwtima3.bdf

Registered Performance | tpd | tsu | tco | th | Custom Delays

	Slack	Required P2P Time	Actual P2P Time	From	To
1	N/A	None	6.537 ns	B	Cout
2	N/A	None	6.518 ns	B	S
3	N/A	None	6.357 ns	A	Cout
4	N/A	None	6.343 ns	A	S
5	N/A	None	6.227 ns	Cin	Cout
6	N/A	None	6.214 ns	Cin	S

Η μέγιστη χρονική καθυστέρηση είναι 6,537ns απο το B στο Cout

FA_vhdl.vhd | quartus4_meros1_erwtima3.bdf | quartus4_meros1_erwtima3.vwf | Simulation Report - Simulation Wave

- Simulation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
- Simulator
  - Summary
  - Settings
  - Simulation Wave
  - Simulation Cove
  - INI Usage
  - Messages

Simulation Waveforms

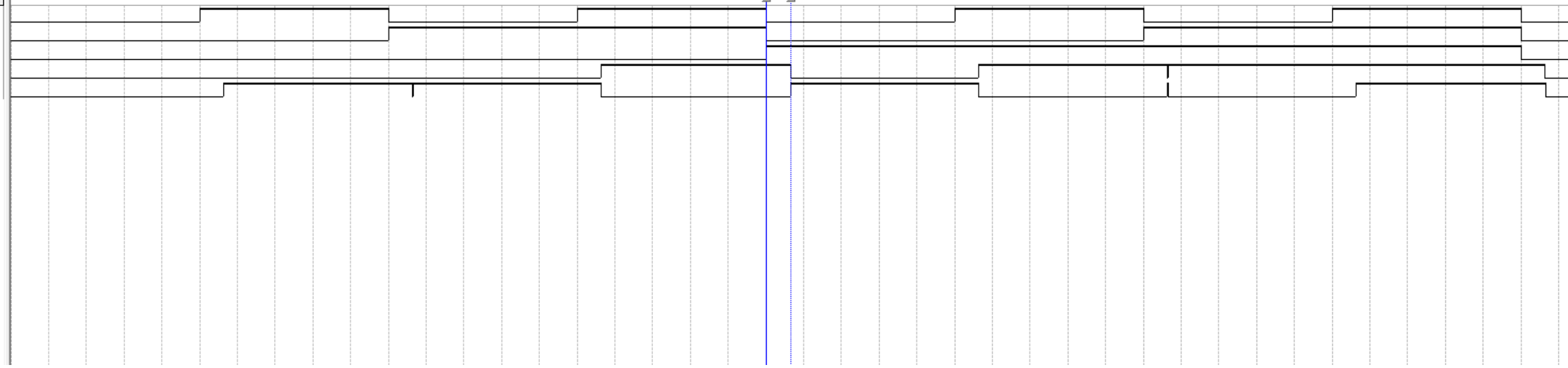
Simulation mode: Timing

Master Time Bar: 200.0 ns | Pointer: 0 ps | Interval: -200.0 ns | Start: | End:

	Name	Value at 200.0 ns
0	A	A 0
1	B	A 0
2	Cin	A 1
3	Cout	A 1
4	S	A 0

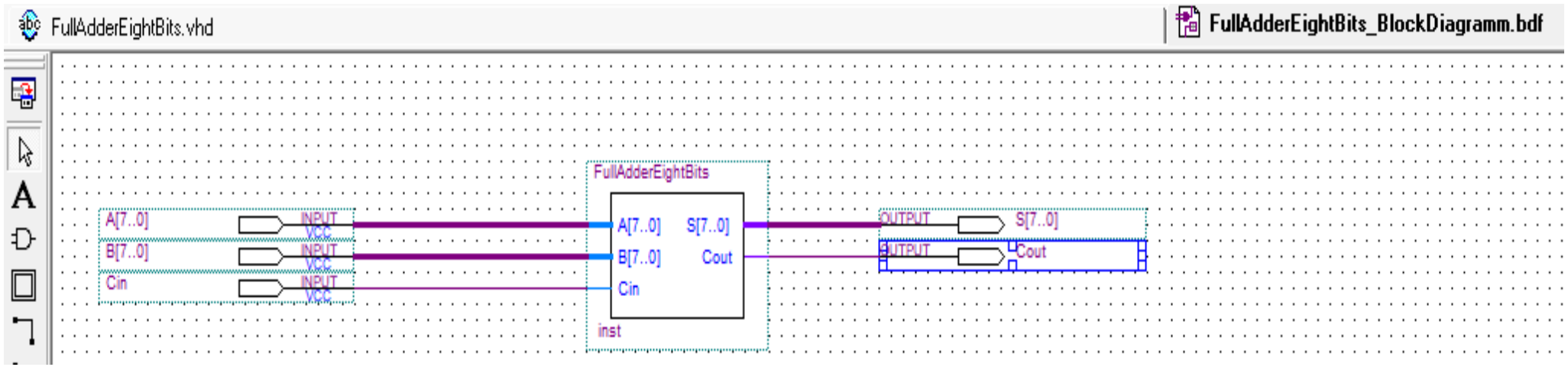
0 ps | 40.0 ns | 80.0 ns | 120.0 ns | 160.0 ns | 200.0 ns | 240.0 ns | 280.0 ns | 320.0 ns | 360.0 ns | 400.0 ns

200.+6.537 ns



FullAdderEightBits.vhd | quartus4_meros1_erwtima3.bdf | quartus4_meros1_erwtima3.vwf | Compilation Report - Flow Sum

```
 1  library IEEE;
 2  use IEEE.STD_LOGIC_1164.ALL;
 3
 4  ENTITY FullAdderEightBits is port(
 5          A : in std_logic_vector (7 downto 0);
 6          B : in std_logic_vector (7 downto 0);
 7          Cin : in std_logic;
 8          S : out std_logic_vector (7 downto 0);
 9          Cout : out std_logic);
10  END FullAdderEightBits;
11
12  ARCHITECTURE FAEB OF FullAdderEightBits IS
13  COMPONENT FA_vhdl
14      port(
15          A : in STD_LOGIC;
16          B : in STD_LOGIC;
17          Cin : in STD_LOGIC;
18          S : out STD_LOGIC;
19          Cout : out STD_LOGIC);
20  END COMPONENT;
21
22      SIGNAL M: STD_LOGIC_VECTOR(0 to 6);
23
24
25  BEGIN
26
27
28  u0: FA_vhdl port map(A=>A(0),B=>B(0),Cin=>Cin,  S=>S(0), Cout=>M(0));
29  u1: FA_vhdl port map(A=>A(1),B=>B(1),Cin=>M(0), S=>S(1), Cout=>M(1));
30  u2: FA_vhdl port map(A=>A(2),B=>B(2),Cin=>M(1), S=>S(2), Cout=>M(2));
31  u3: FA_vhdl port map(A=>A(3),B=>B(3),Cin=>M(2), S=>S(3), Cout=>M(3));
32  u4: FA_vhdl port map(A=>A(4),B=>B(4),Cin=>M(3), S=>S(4), Cout=>M(4));
33  u5: FA_vhdl port map(A=>A(5),B=>B(5),Cin=>M(4), S=>S(5), Cout=>M(5));
34  u6: FA_vhdl port map(A=>A(6),B=>B(6),Cin=>M(5), S=>S(6), Cout=>M(6));
35  u7: FA_vhdl port map(A=>A(7),B=>B(7),Cin=>M(6), S=>S(7), Cout=>Cout);
36
37  END FAEB;
```


FullAdderEightBits.vhd
FullAdderEightBits_BlockDiagramm.bdf
FullAdderEightBits
A[7..0]
B[7..0]
Cin
INPUT
INPUT
INPUT
A[7..0]
B[7..0]
Cin
S[7..0]
Cout
inst
OUTPUT
OUTPUT
S[7..0]
Cout

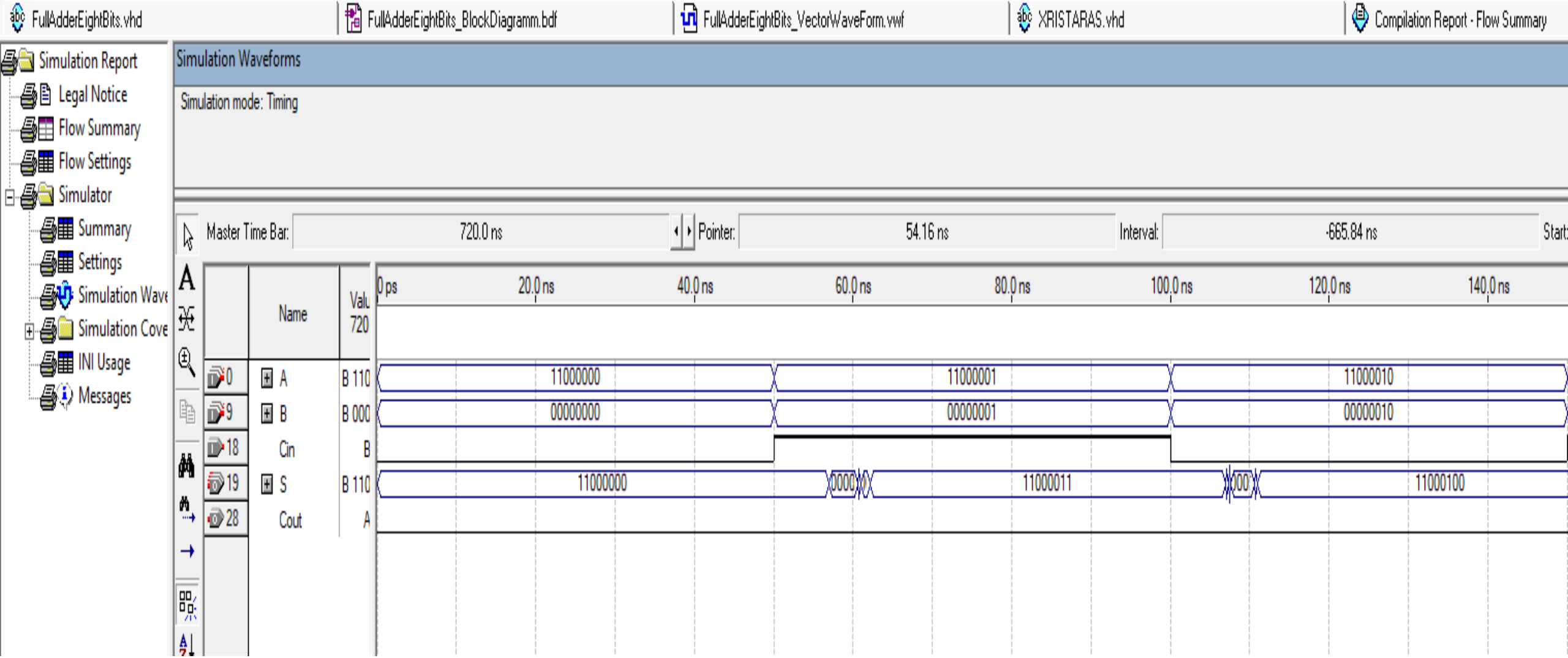
ΣΤΑΤΙΚΗ ΧΡΟΝΙΚΗ ΑΝΑΛΥΣΗ

FullAdderEightBits.vhd

Registered Performance | tpd | tsu | tco | th | Custom Delays

	Slack	Required P2P Time	Actual P2P Time	From	To
1	N/A	None	16.716 ns	B[1]	S[7]
2	N/A	None	16.532 ns	A[3]	S[7]
3	N/A	None	16.429 ns	Cin	S[7]
4	N/A	None	16.394 ns	B[3]	S[7]
5	N/A	None	16.177 ns	A[1]	S[7]
6	N/A	None	15.752 ns	B[2]	S[7]
7	N/A	None	15.740 ns	A[2]	S[7]
8	N/A	None	15.149 ns	B[1]	Cout
9	N/A	None	15.149 ns	B[4]	S[7]
10	N/A	None	14.965 ns	A[3]	Cout
11	N/A	None	14.862 ns	Cin	Cout
12	N/A	None	14.827 ns	B[3]	Cout
13	N/A	None	14.813 ns	A[4]	S[7]
14	N/A	None	14.610 ns	A[1]	Cout
15	N/A	None	14.328 ns	A[5]	S[7]
16	N/A	None	14.188 ns	B[5]	S[7]
17	N/A	None	14.185 ns	B[2]	Cout
18	N/A	None	14.173 ns	A[2]	Cout
19	N/A	None	13.582 ns	B[4]	Cout
20	N/A	None	13.576 ns	B[6]	S[7]
21	N/A	None	13.364 ns	A[6]	S[7]
22	N/A	None	13.251 ns	B[1]	S[6]
23	N/A	None	13.246 ns	A[4]	Cout
24	N/A	None	13.142 ns	A[0]	S[7]
25	N/A	None	13.067 ns	A[3]	S[6]

Η μέγιστη χρονική καθυστέρηση ειναι 16,716ns από το B[1] στο S[7].

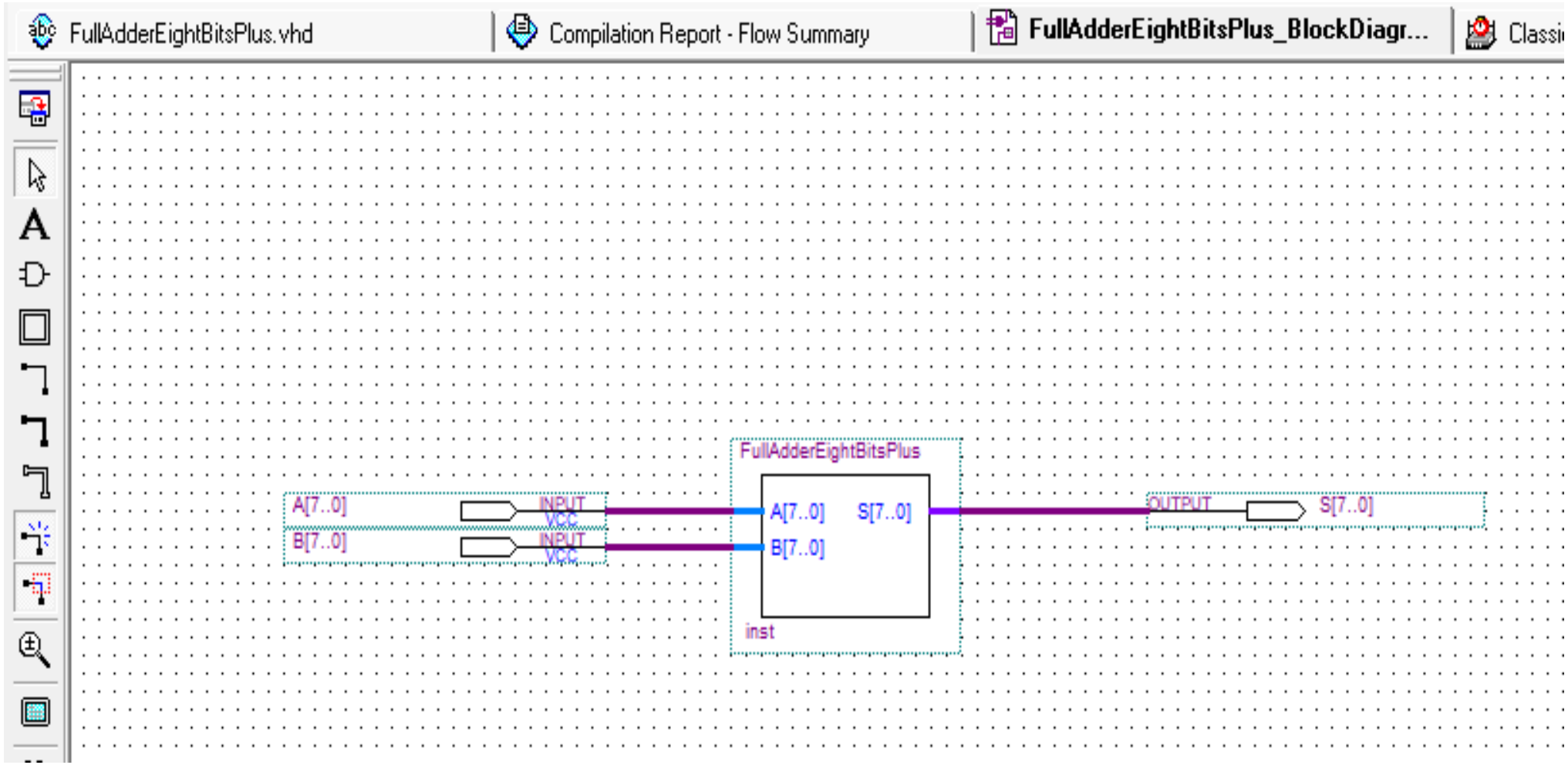


Στο παραπάνω vector waveform βάλαμε να αλλάζει η τιμή του Cin από 0 σε 1 για να δοκιμάσουμε αν λειτουργεί σωστά ενώ ξέρουμε οτι κανονικά θα έπρεπε να είναι μόνιμα στο 0 για να κάνει την κανονική πρόσθεση δύο 8-bit αριθμών .

ΜΕΡΟΣ 1^{Ο} : Συνδιαστικά Κυκλώματα
Ερώτημα 4^{ο}

FullAdderEightBitsPlus.vhd

```
 1  library IEEE;
 2  use IEEE.std_logic_1164.all;
 3  use IEEE.std_logic_unsigned.all;
 4
 5  entity FullAdderEightBitsPlus is port (
 6      A : in std_logic_vector (7 downto 0);
 7      B : in std_logic_vector (7 downto 0);
 8      S : out std_logic_vector (7 downto 0));
 9
10  end FullAdderEightBitsPlus;
11
12  architecture FAEBP of FullAdderEightBitsPlus is
13  begin
14      S<=A+B;
15  end FAEBP;
```


FullAdderEightBitsPlus.vhd
Compilation Report - Flow Summary
FullAdderEightBitsPlus_BlockDiagr...
FullAdderEightBitsPlus
A[7..0]
INPUT
VCC
B[7..0]
INPUT
VCC
A[7..0]
B[7..0]
S[7..0]
inst
OUTPUT
S[7..0]

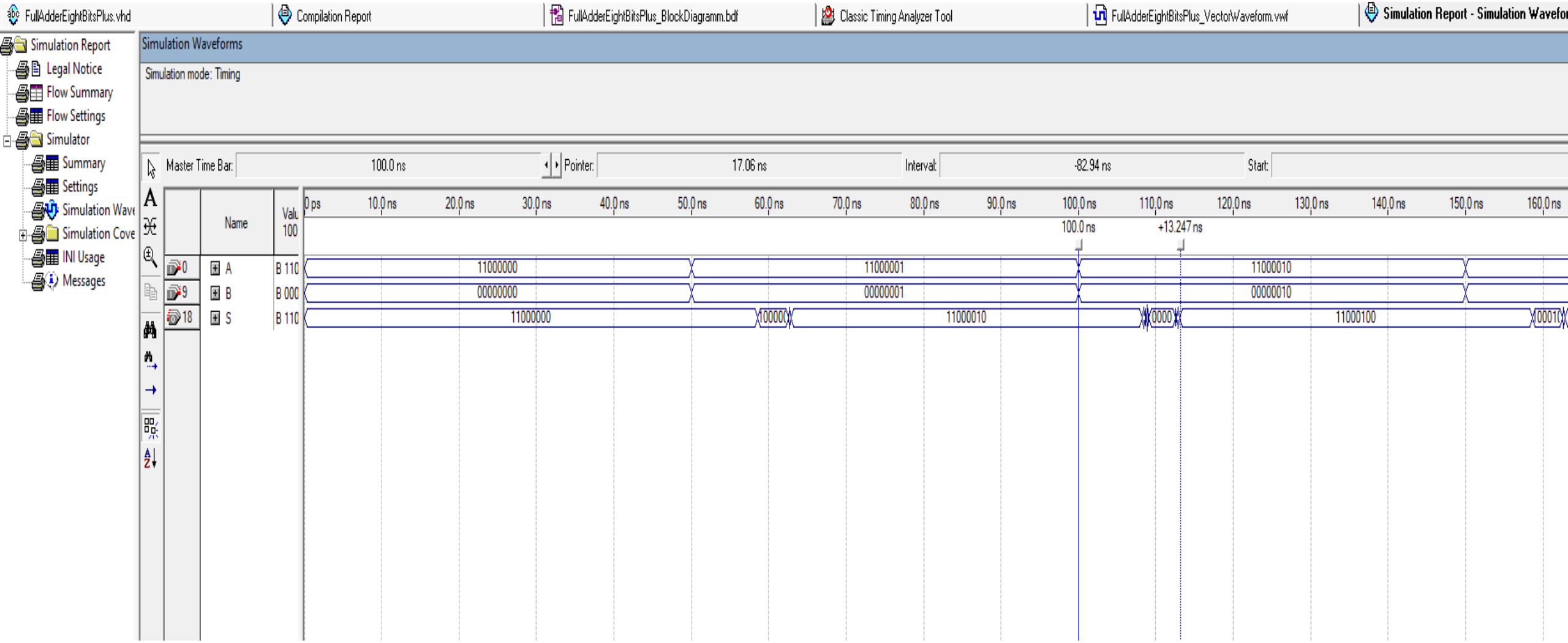
ΣΤΑΤΙΚΗ ΧΡΟΝΙΚΗ ΑΝΑΛΥΣΗ

FullAdderEightBitsPlus.vhd | Compilation Report - Flow Summary

Registered Performance | tpd | tsu | tco | th | Custom Delays

	Slack	Required P2P Time	Actual P2P Time	From	To
1	N/A	None	13.628 ns	B[1]	S[6]
2	N/A	None	13.580 ns	B[0]	S[6]
3	N/A	None	13.536 ns	B[1]	S[7]
4	N/A	None	13.488 ns	B[0]	S[7]
5	N/A	None	13.283 ns	B[1]	S[5]
6	N/A	None	13.235 ns	B[0]	S[5]
7	N/A	None	13.209 ns	B[1]	S[4]
8	N/A	None	13.161 ns	B[0]	S[4]
9	N/A	None	13.142 ns	B[2]	S[6]
10	N/A	None	13.102 ns	B[1]	S[3]
11	N/A	None	13.080 ns	B[1]	S[2]
12	N/A	None	13.054 ns	B[0]	S[3]
13	N/A	None	13.050 ns	B[2]	S[7]
14	N/A	None	13.032 ns	B[0]	S[2]
15	N/A	None	12.900 ns	B[0]	S[1]

Η μέγιστη χρονική καθυστέρηση είναι 13,628ns απο το B[1] στο S[6]


FullAdderEightBitsPlus.vhd
Compilation Report
FullAdderEightBitsPlus_BlockDiagramm.bdf
Classic Timing Analyzer Tool
FullAdderEightBitsPlus_VectorWaveform.vwf
Simulation Report - Simulation Wavefor
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Wave
Simulation Cove
INI Usage
Messages
Simulation Waveforms
Simulation mode: Timing
Master Time Bar: 100.0 ns
Pointer: 17.06 ns
Interval: -82.94 ns
Start:
Name
Valu
100
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
90.0 ns
100.0 ns
110.0 ns
120.0 ns
130.0 ns
140.0 ns
150.0 ns
160.0 ns
100.0 ns
+13.247 ns
0
A
B 110
11000000
11000001
11000010
9
B
B 000
00000000
00000001
00000010
18
S
B 110
11000000
11000010
11000100

Σύμφωνα με τη μέγιστη χρονική καθυστέρηση των δύο αθροιστών συμπεραίνουμε οτι ο αθροιστής του ερωτήματος 4 (με τη χρήση του «+») είναι ο πιο γρήγορος απο τους δύο.

FullAdderEightBits.vhd

Registered Performance | tpd | tsu | tco | th | Custom Delays

	Slack	Required P2P Time	Actual P2P Time	From	To
1	N/A	None	16.716 ns	B[1]	S[7]
2	N/A	None	16.532 ns	A[3]	S[7]
3	N/A	None	16.429 ns	Cin	S[7]
4	N/A	None	16.394 ns	B[3]	S[7]
5	N/A	None	16.177 ns	A[1]	S[7]
6	N/A	None	15.752 ns	B[2]	S[7]
7	N/A	None	15.740 ns	A[2]	S[7]
8	N/A	None	15.149 ns	B[1]	Cout
9	N/A	None	15.149 ns	B[4]	S[7]
10	N/A	None	14.965 ns	A[3]	Cout
11	N/A	None	14.862 ns	Cin	Cout
12	N/A	None	14.827 ns	B[3]	Cout
13	N/A	None	14.813 ns	A[4]	S[7]
14	N/A	None	14.610 ns	A[1]	Cout
15	N/A	None	14.328 ns	A[5]	S[7]
16	N/A	None	14.188 ns	B[5]	S[7]
17	N/A	None	14.185 ns	B[2]	Cout
18	N/A	None	14.173 ns	A[2]	Cout
19	N/A	None	13.582 ns	B[4]	Cout
20	N/A	None	13.576 ns	B[6]	S[7]
21	N/A	None	13.364 ns	A[6]	S[7]
22	N/A	None	13.251 ns	B[1]	S[6]
23	N/A	None	13.246 ns	A[4]	Cout
24	N/A	None	13.142 ns	A[0]	S[7]
25	N/A	None	13.067 ns	A[3]	S[6]

Ερώτημα 3

FullAdderEightBitsPlus.vhd | Compilation Report - Flow Summary

Registered Performance | tpd | tsu | tco | th | Custom Delays

	Slack	Required P2P Time	Actual P2P Time	From	To
1	N/A	None	13.628 ns	B[1]	S[6]
2	N/A	None	13.580 ns	B[0]	S[6]
3	N/A	None	13.536 ns	B[1]	S[7]
4	N/A	None	13.488 ns	B[0]	S[7]
5	N/A	None	13.283 ns	B[1]	S[5]
6	N/A	None	13.235 ns	B[0]	S[5]
7	N/A	None	13.209 ns	B[1]	S[4]
8	N/A	None	13.161 ns	B[0]	S[4]
9	N/A	None	13.142 ns	B[2]	S[6]
10	N/A	None	13.102 ns	B[1]	S[3]
11	N/A	None	13.080 ns	B[1]	S[2]
12	N/A	None	13.054 ns	B[0]	S[3]
13	N/A	None	13.050 ns	B[2]	S[7]
14	N/A	None	13.032 ns	B[0]	S[2]
15	N/A	None	12.900 ns	B[0]	S[1]

Ερώτημα 4

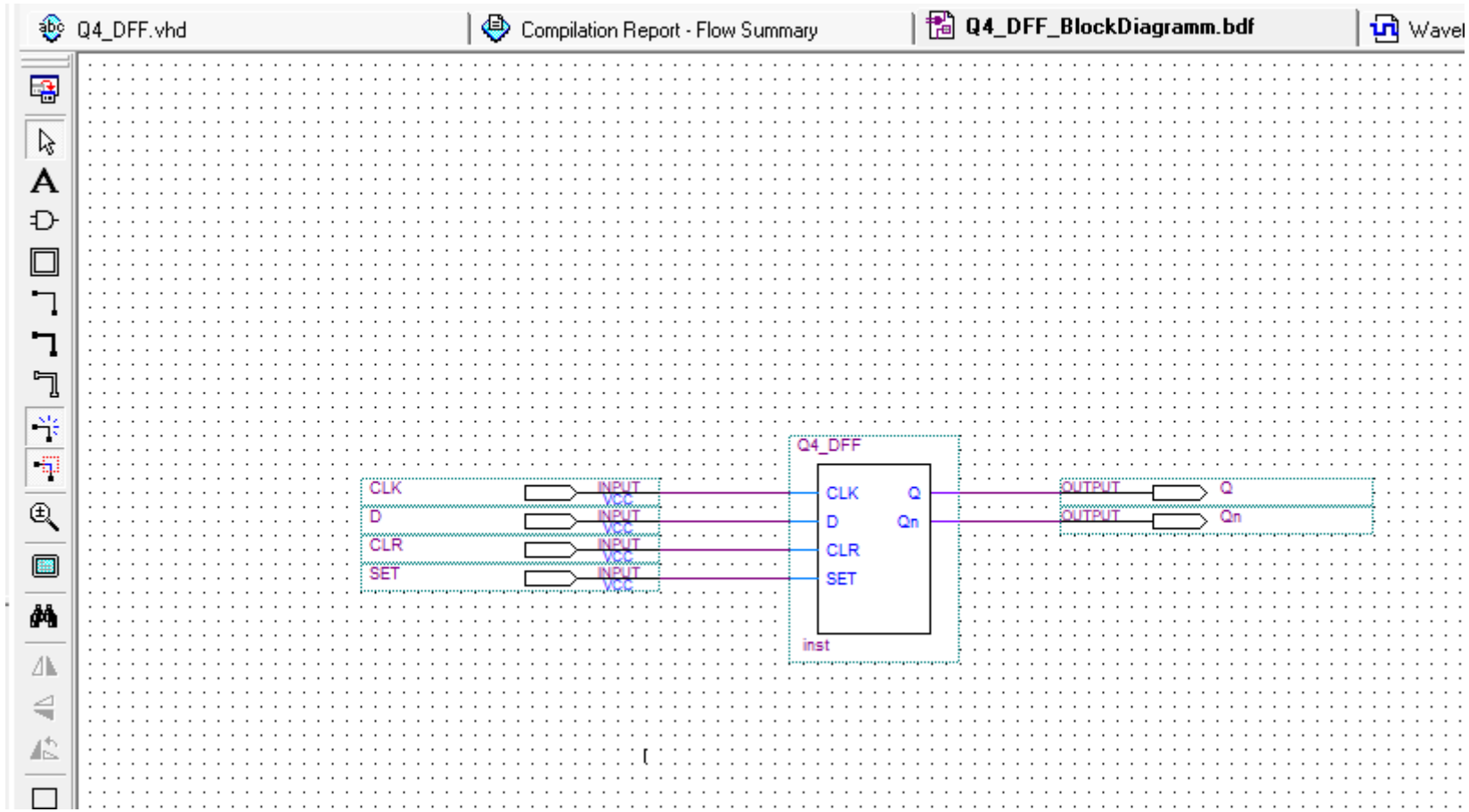
ΜΕΡΟΣ 2Ο

Ερώτημα 1ο

D Flip Flop

Q4_DFF.vhd | Compilation Report - Flow Summary | Q4_DFF_BlockDiagramm.bd

```
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3
4
5  entity Q4_DFF is port (
6      CLK,D,CLR,SET : in std_logic;
7      Q,Qn : out std_logic);
8  end Q4_DFF;
9
10 architecture RTL of Q4_DFF is
11     signal DFF : std_logic;
12 begin
13     seq0: process(CLK,CLR,SET)
14     begin
15         if(CLR='1') then DFF<='0';
16         elsif(SET='1') then DFF<='1';
17         elsif(CLK'event and CLK='1') then DFF<=D;
18         end if;
19     end process;
20     Q<=DFF;
21     Qn<= not DFF;
22 end RTL;
```


Q4_DFF.vhd
Compilation Report - Flow Summary
Q4_DFF_BlockDiagramm.bdf
Wavel
Q4_DFF
CLK
D
CLR
SET
INPUT
VCC
CLK
D
CLR
SET
Q
Qn
inst
OUTPUT
Q
OUTPUT
Qn

ΣΤΑΤΙΚΗ ΧΡΟΝΙΚΗ ΑΝΑΛΥΣΗ

Q4_DFF.vhd

Registered Performance | tpd | tsu | tco | th | Custom Delays

	Slack	Required P2P Time	Actual P2P Time	From	To
1	N/A	None	6.620 ns	SET	Qn
2	N/A	None	6.470 ns	CLR	Qn
3	N/A	None	6.215 ns	SET	Q
4	N/A	None	6.065 ns	CLR	Q

Η μέγιστη συχνότητα ρολογιού είναι που μπορεί να χρησιμοποιηθει ειναι:

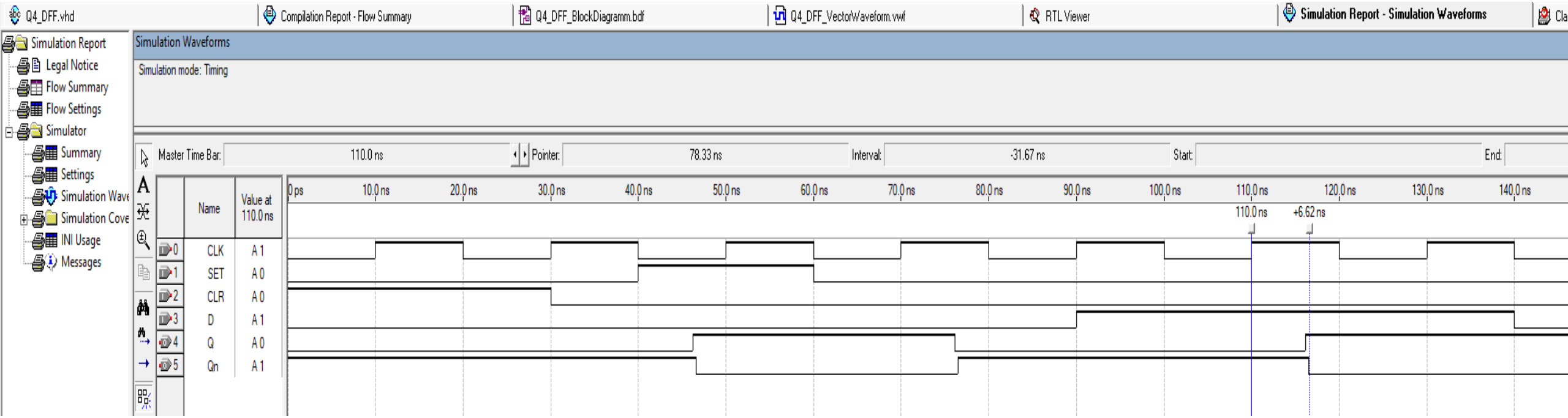
You are currently converting frequency units from nanosecond(period) to hertz

6.62 ns(p) = **151057401.81269** Hz

nanosecond(period)		**hertz**
6.62 ns(p)	→	**151057401.81269** Hz

Conversion base : 1 ns(p) = 1000000000 Hz

Conversion base : 1 Hz = 1000000000 ns(p)


Q4_DFF.vhd
Compilation Report - Flow Summary
Q4_DFF_BlockDiagramm.bdf
Q4_DFF_VectorWaveform.vwf
RTL Viewer
Simulation Report - Simulation Waveforms
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Wave
Simulation Cove
INI Usage
Messages
Simulation Waveforms
Simulation mode: Timing
Master Time Bar: 110.0 ns
Pointer: 78.33 ns
Interval: -31.67 ns
Start:
End:
Name
Value at 110.0 ns
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
90.0 ns
100.0 ns
110.0 ns
120.0 ns
130.0 ns
140.0 ns
110.0 ns
+6.62 ns
0 CLK A 1
1 SET A 0
2 CLR A 0
3 D A 1
4 Q A 0
5 Qn A 1

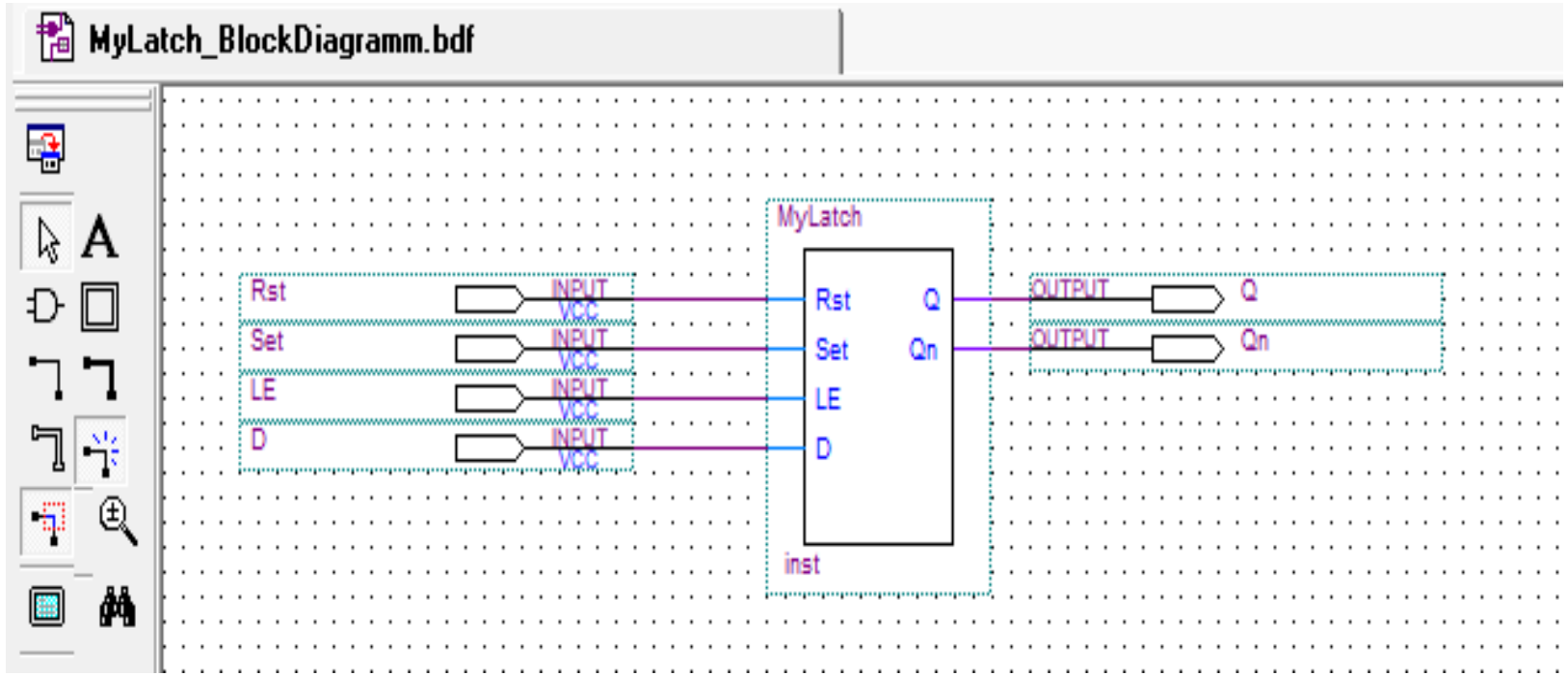
ΜΕΡΟΣ 2Ο

Ερώτημα 1ο

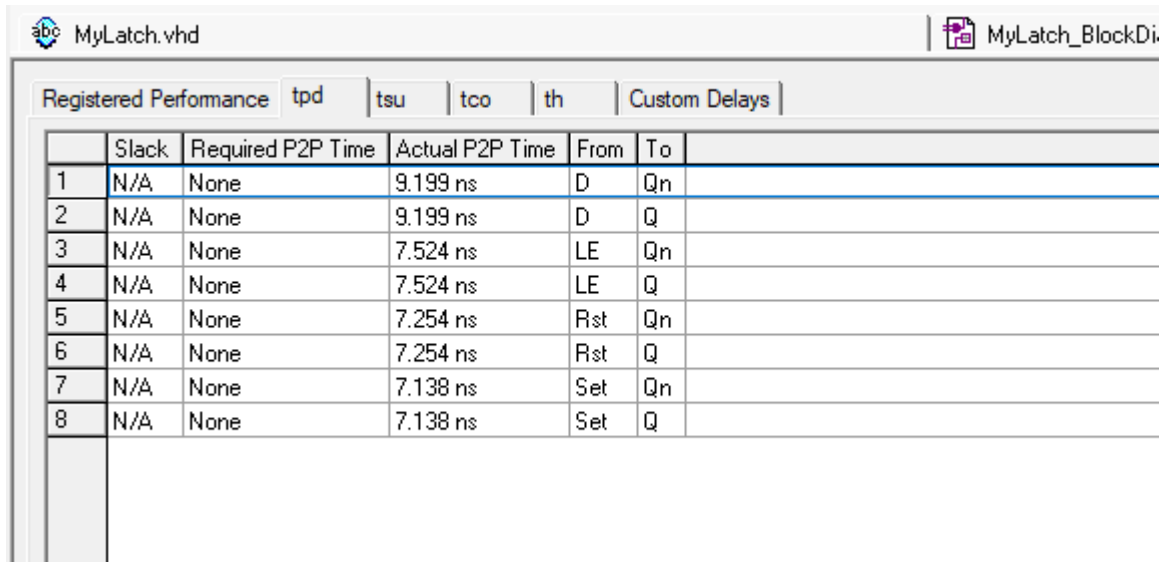
My Latch

MyLatch.vhd | Block1.bdf*

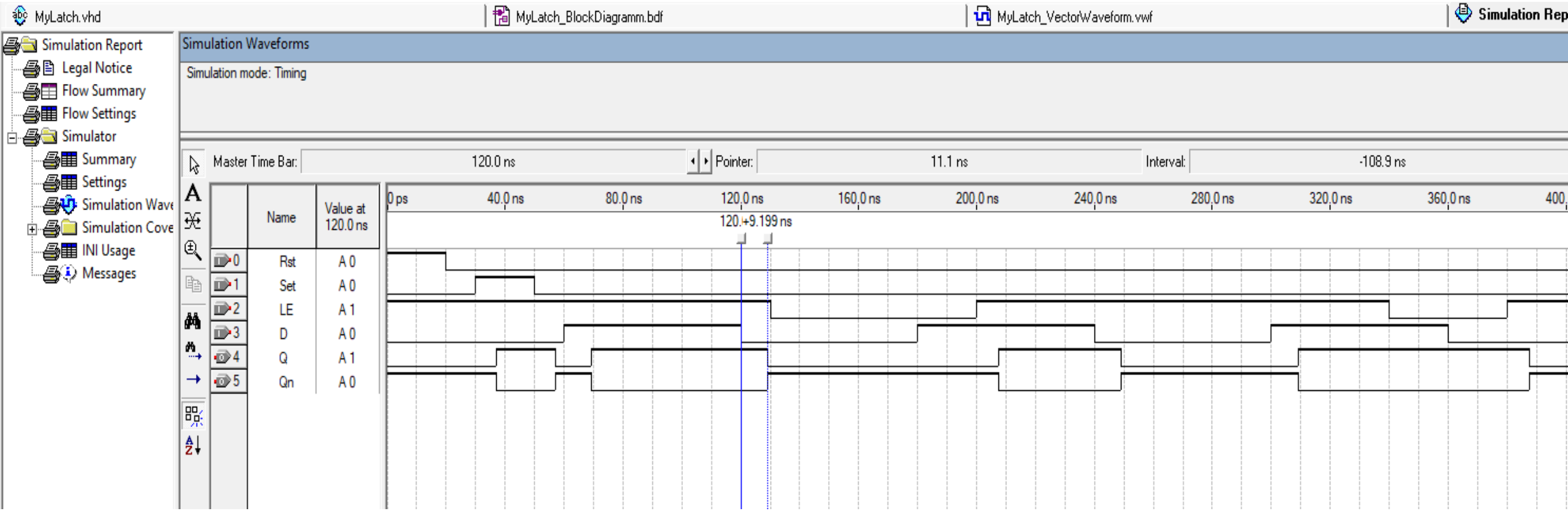
```
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  entity MyLatch is port(
5      Rst,Set,LE,D : in std_logic;
6      Q, Qn : out std_logic);
7  end MyLatch;
8
9  architecture RTL of MyLatch is
10 signal FF: std_logic;
11 begin
12 seq0 :process (Rst, Set, D , LE)
13 begin
14     if Rst = '1' then FF <= '0';
15     elsif Set = '1' then FF <= '1';
16     elsif LE = '1' then FF <= D;
17     end if;
18 end process;
19 Q <= FF;
20 Qn <= not FF;
21 end RTL;
```


MyLatch_BlockDiagramm.bdf
MyLatch
Rst
Set
LE
D
INPUT
VCC
Rst
Set
LE
D
Q
Qn
OUTPUT
Q
OUTPUT
Qn
inst

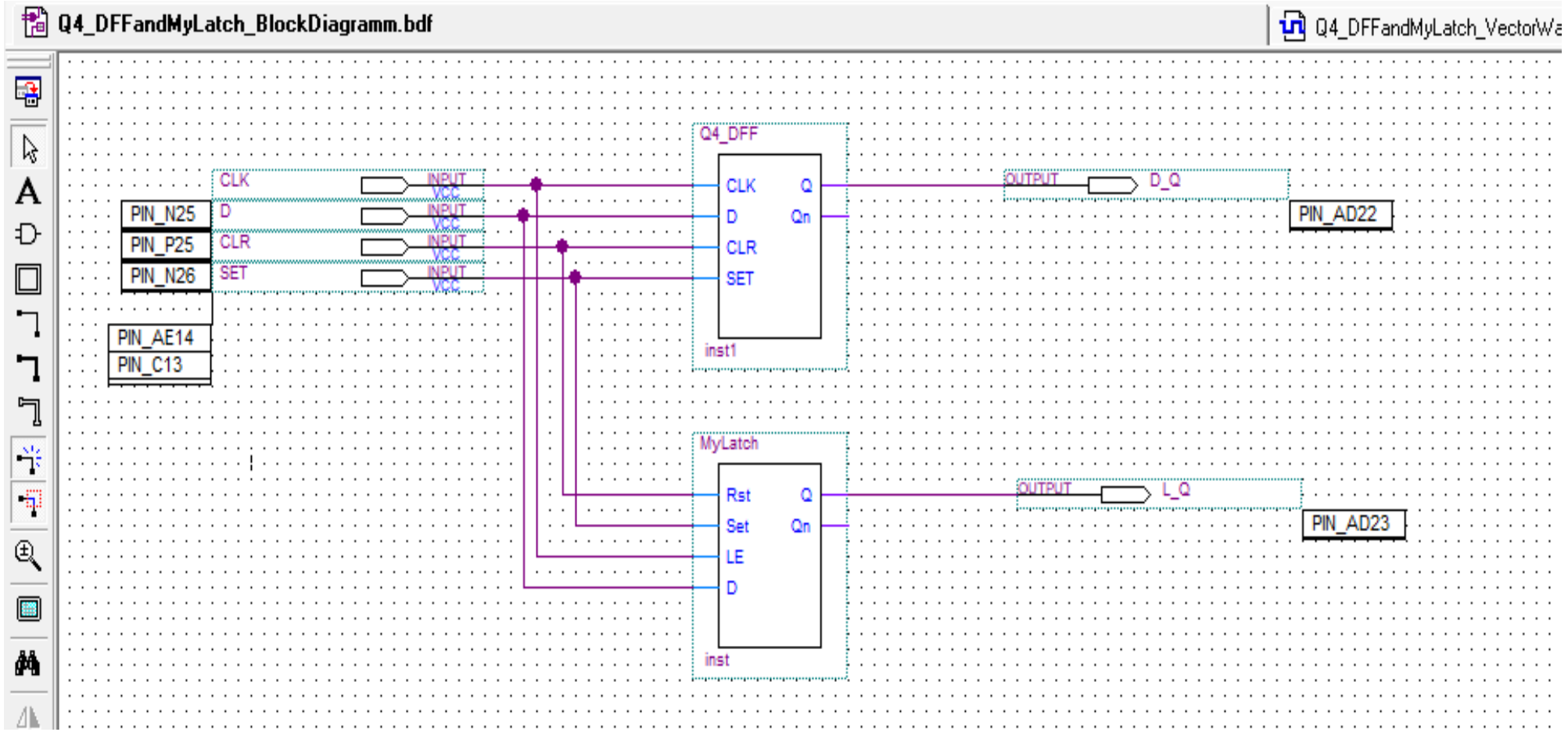
ΣΤΑΤΙΚΗ ΧΡΟΝΙΚΗ ΑΝΑΛΥΣΗ

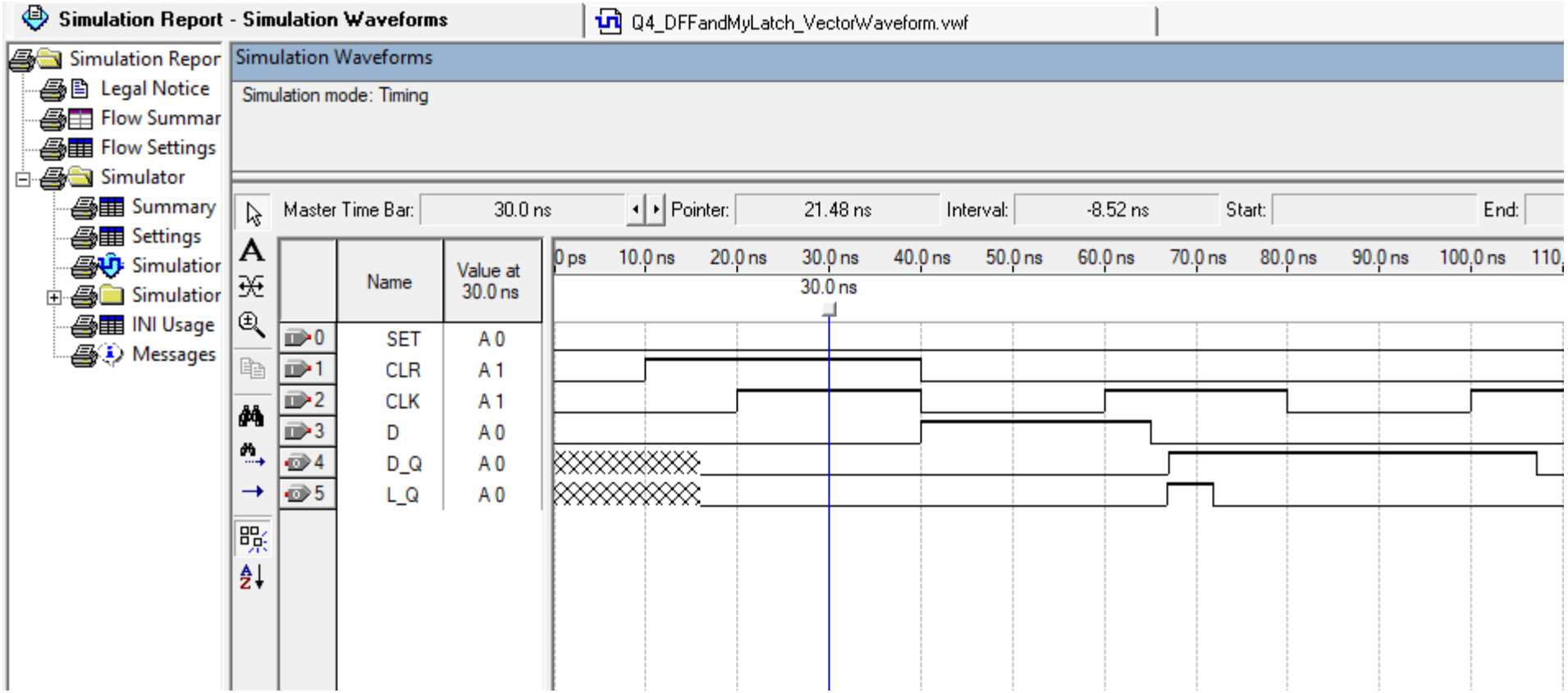


	Slack	Required P2P Time	Actual P2P Time	From	To
1	N/A	None	9.199 ns	D	Qn
2	N/A	None	9.199 ns	D	Q
3	N/A	None	7.524 ns	LE	Qn
4	N/A	None	7.524 ns	LE	Q
5	N/A	None	7.254 ns	Rst	Qn
6	N/A	None	7.254 ns	Rst	Q
7	N/A	None	7.138 ns	Set	Qn
8	N/A	None	7.138 ns	Set	Q


MyLatch.vhd
MyLatch_BlockDiagramm.bdf
MyLatch_VectorWaveform.vwf
Simulation Rep
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Wave
Simulation Cove
INI Usage
Messages
Simulation Waveforms
Simulation mode: Timing
Master Time Bar:
120.0 ns
Pointer:
11.1 ns
Interval:
-108.9 ns
Name
Value at 120.0 ns
0 ps
40.0 ns
80.0 ns
120.0 ns
160.0 ns
200.0 ns
240.0 ns
280.0 ns
320.0 ns
360.0 ns
120.+9.199 ns
0 Rst A 0
1 Set A 0
2 LE A 1
3 D A 0
4 Q A 1
5 Qn A 0

Σχηματικό DFF και Latch



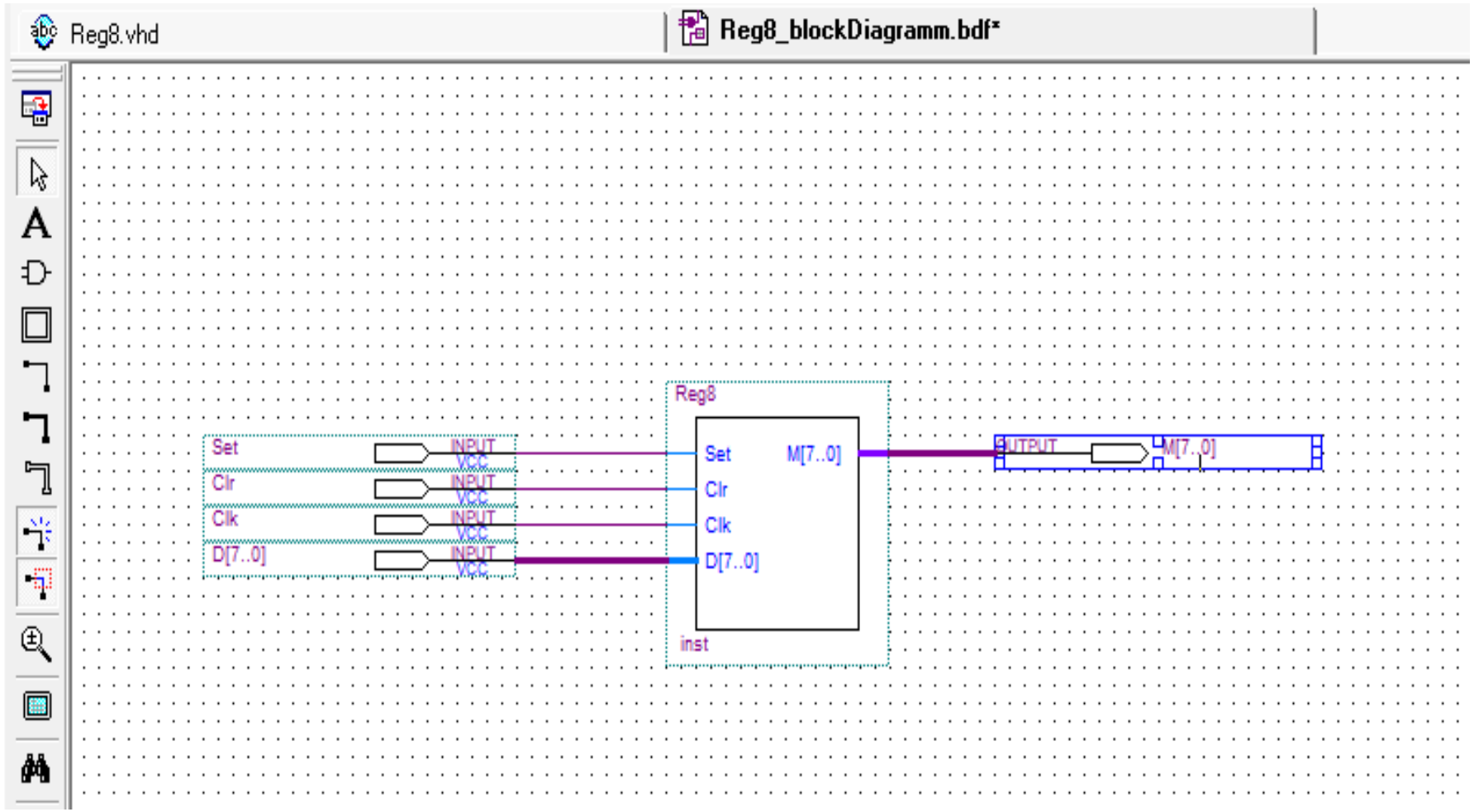

Simulation Report - Simulation Waveforms
Q4_DFFandMyLatch_VectorWaveform.vwf
Simulation Repor
Legal Notice
Flow Summar
Flow Settings
Simulator
Summary
Settings
Simulatior
Simulatior
INI Usage
Messages
Simulation Waveforms
Simulation mode: Timing
Master Time Bar: 30.0 ns
Pointer: 21.48 ns
Interval: -8.52 ns
Start:
End:
Name
Value at 30.0 ns
0 SET A 0
1 CLR A 1
2 CLK A 1
3 D A 0
4 D_Q A 0
5 L_Q A 0
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
90.0 ns
100.0 ns
30.0 ns

ΜΕΡΟΣ 2Ο

Ερώτημα 2ο

Reg8.vhd | CountToEightBits.vhd

```
1   library IEEE;
2   use IEEE.std_logic_1164.all;
3
4
5   entity Reg8 is port(
6       Set : in std_logic;
7       Clr : in std_logic;
8       Clk : in std_logic;
9       D :in std_logic_vector(7 downto 0);
10      M : out std_logic_vector(7 downto 0));
11  end Reg8;
12
13  architecture Regi8 of Reg8 is
14      signal temp : std_logic_vector(7 downto 0);
15  begin
16      seq0: process(Clr,Clk,Set,D)
17      begin
18          if (Clr='1') then
19                  temp<= "00000000";
20          elsif (Set='1') then
21                  temp<= "11111111";
22          elsif (Clk'event and Clk='1') then
23              temp<= D;
24          end if;
25      end process;
26      M<=temp;
27  end Regi8;
```


Reg8.vhd
Reg8_blockDiagramm.bdf*
Reg8
Set
Clr
Clk
D[7..0]
INPUT
VCC
Set
Clr
Clk
D[7..0]
M[7..0]
inst
OUTPUT
M[7..0]

ΣΤΑΤΙΚΗ ΧΡΟΝΙΚΗ ΑΝΑΛΥΣΗ

Reg8.vhd | Reg8_blockDiagramm.bd

Registered Performance | tpd | tsu | tco | th | Custom Delays

	Slack	Required P2P Time	Actual P2P Time	From	To
1	N/A	None	13.572 ns	Set	M[1]
2	N/A	None	13.094 ns	Set	M[2]
3	N/A	None	11.227 ns	Set	M[7]
4	N/A	None	11.172 ns	Set	M[6]
5	N/A	None	11.158 ns	Set	M[0]
6	N/A	None	10.955 ns	Set	M[4]
7	N/A	None	10.942 ns	Set	M[3]
8	N/A	None	10.919 ns	Set	M[5]
9	N/A	None	9.038 ns	Clr	M[1]
10	N/A	None	8.560 ns	Clr	M[2]
11	N/A	None	6.693 ns	Clr	M[7]
12	N/A	None	6.638 ns	Clr	M[6]
13	N/A	None	6.624 ns	Clr	M[0]
14	N/A	None	6.421 ns	Clr	M[4]
15	N/A	None	6.408 ns	Clr	M[3]
16	N/A	None	6.385 ns	Clr	M[5]

Μέγιστη συχνότητα ρολογιού που μπορεί να χρησιμοποιηθεί ειναι:

You are currently converting frequency units from nanosecond(period) to hertz

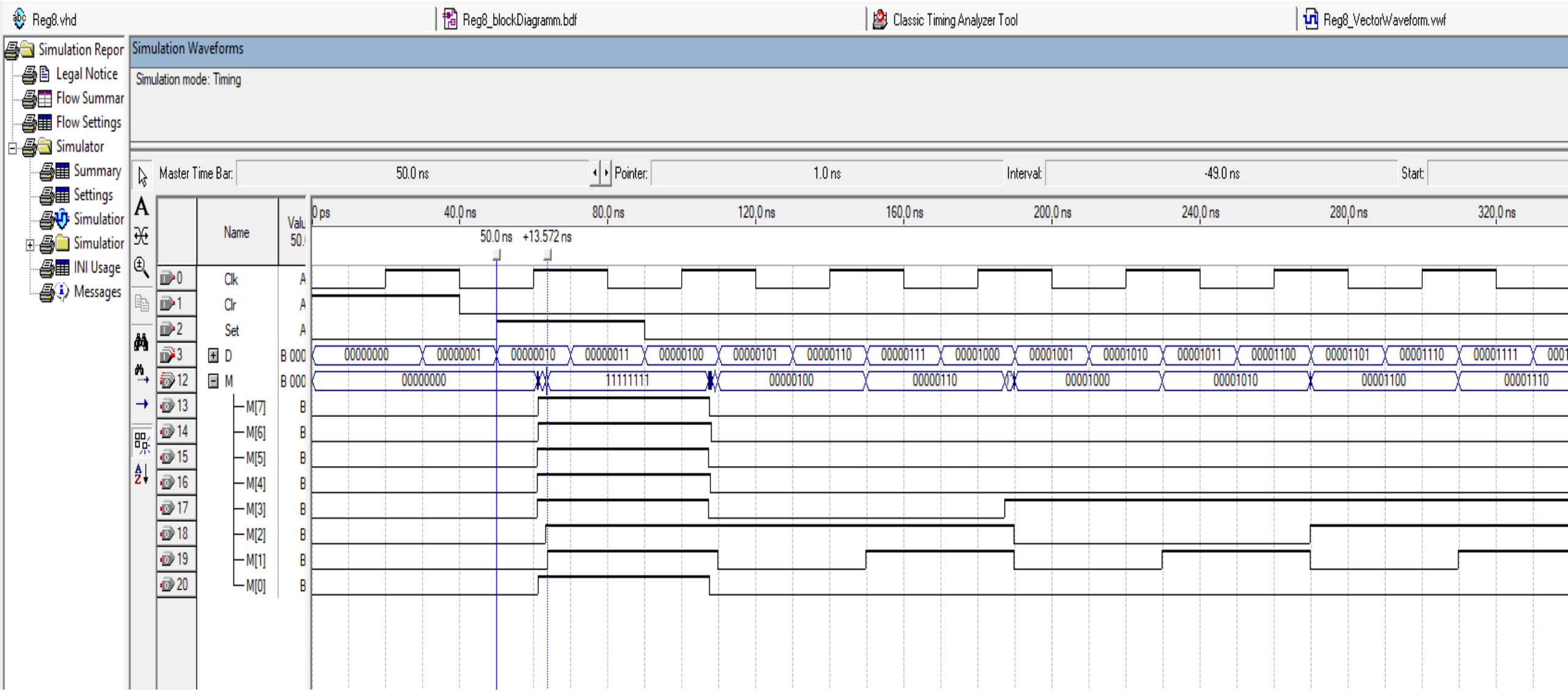
13.572 ns(p) = **73681108.163867** Hz

nanosecond(period) | **hertz**

13.572 ns(p) → **73681108.163867** Hz

Conversion base : 1 ns(p) = 1000000000 Hz

Conversion base : 1 Hz = 1000000000 ns(p)


Reg8.vhd
Reg8_blockDiagramm.bdf
Classic Timing Analyzer Tool
Reg8_VectorWaveform.vwf
Simulation Repor
Legal Notice
Flow Summar
Flow Settings
Simulator
Summary
Settings
Simulatior
Simulatior
INI Usage
Messages
Simulation Waveforms
Simulation mode: Timing
Master Time Bar: 50.0 ns
Pointer: 1.0 ns
Interval: -49.0 ns
Start:
Name
Valu
50.
0 ps
40.0 ns
80.0 ns
120.0 ns
160.0 ns
200.0 ns
240.0 ns
280.0 ns
320.0 ns
50.0 ns +13.572 ns
0 Clk A
1 Clr A
2 Set A
3 D B 000 00000000 00000001 00000010 00000011 00000100 00000101 00000110 00000111 00001000 00001001 00001010 00001011 00001100 00001101 00001110 00001111
12 M B 000 00000000 11111111 00000100 00000110 00001000 00001010 00001100 00001110
13 M[7] B
14 M[6] B
15 M[5] B
16 M[4] B
17 M[3] B
18 M[2] B
19 M[1] B
20 M[0] B

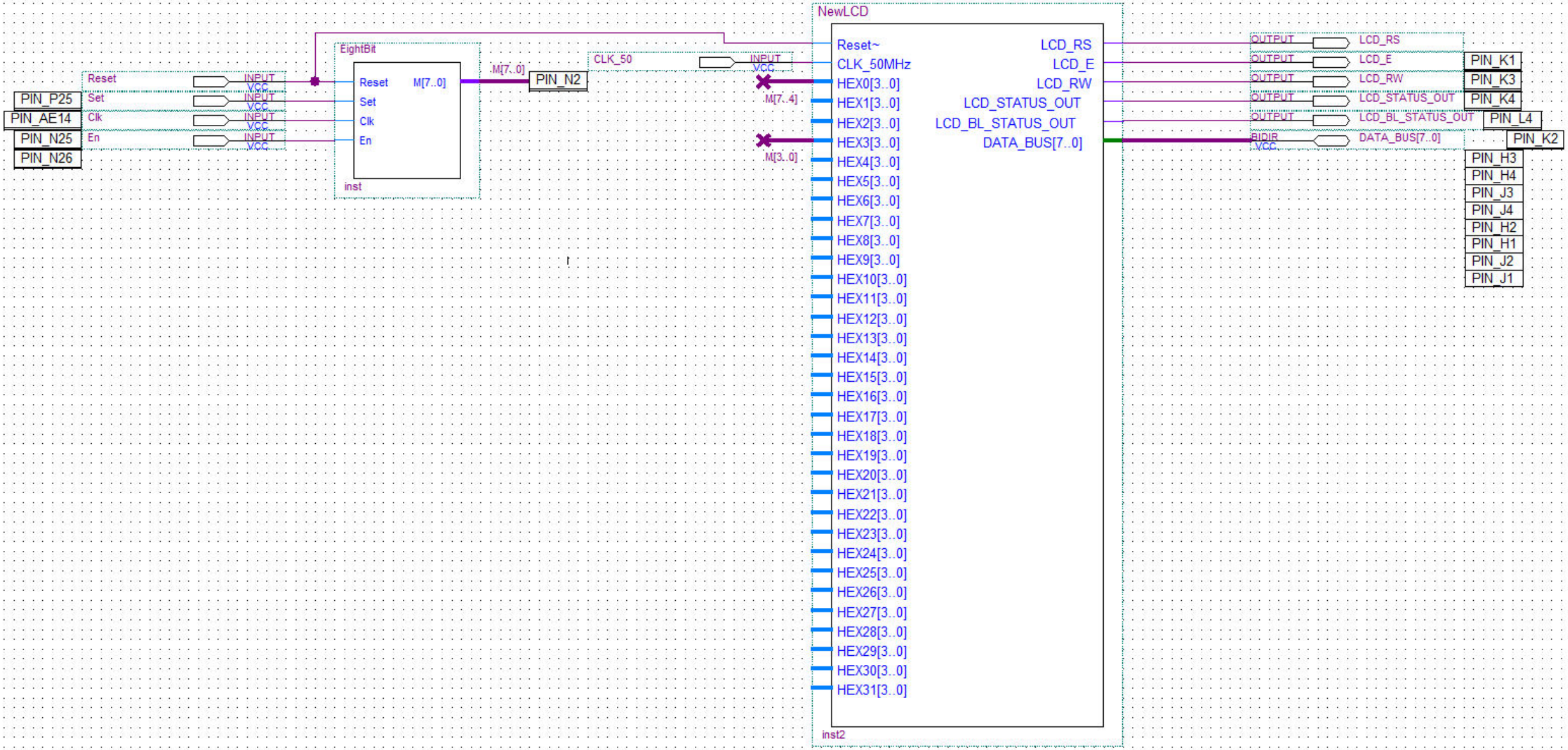
ΜΕΡΟΣ 3Ο

Ερώτημα 3ο

Classic Timing Analyzer Tool | EightBit.vhd

```
 1  library IEEE;
 2  use IEEE.std_logic_1164.all;
 3  use IEEE.std_logic_unsigned.all;
 4
 5
 6  entity EightBit is port(
 7       Reset : in std_logic;
 8       Set: in std_logic;
 9       Clk: in std_logic;
10       En: in std_logic;
11       M : out std_logic_vector(7 downto 0));
12  end EightBit;
13
14  architecture EB of EightBit is
15       signal  Y : std_logic_vector(7 downto 0);
16
17  begin
18       seq0 : process(Reset,Set,Clk,En)
19       begin
20            if (Reset='1') then
21                 Y<="00000000";
22            elsif (Set='1') then
23                 Y<="11111111";
24            elsif(Clk'event and Clk='1' and En='1') then
25                 Y<= Y + '1';
26            end if;
27       end process;
28       M<=Y;
29  end EB;
```

EightBit.vhd | Compilation Report - Flow Summary | EightBit_BlockDiagramm.bdf | ../../../Users/Mainframe/Documents/C

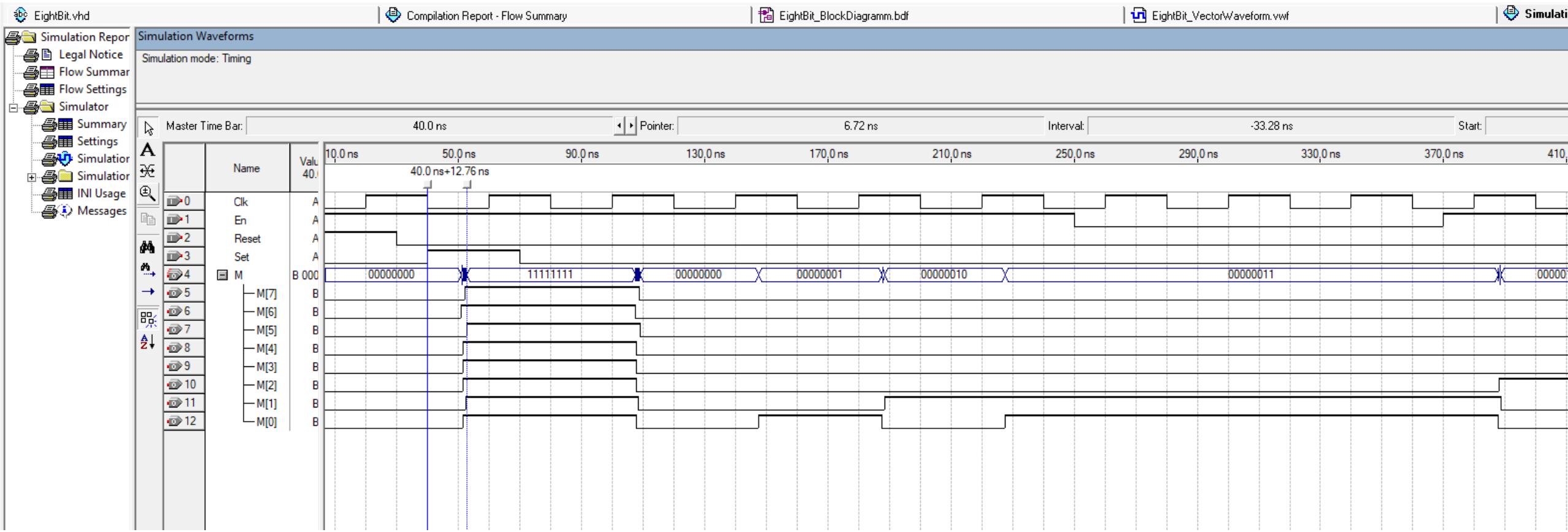


EightBit.vhd | Compilation Report - Flow Summary

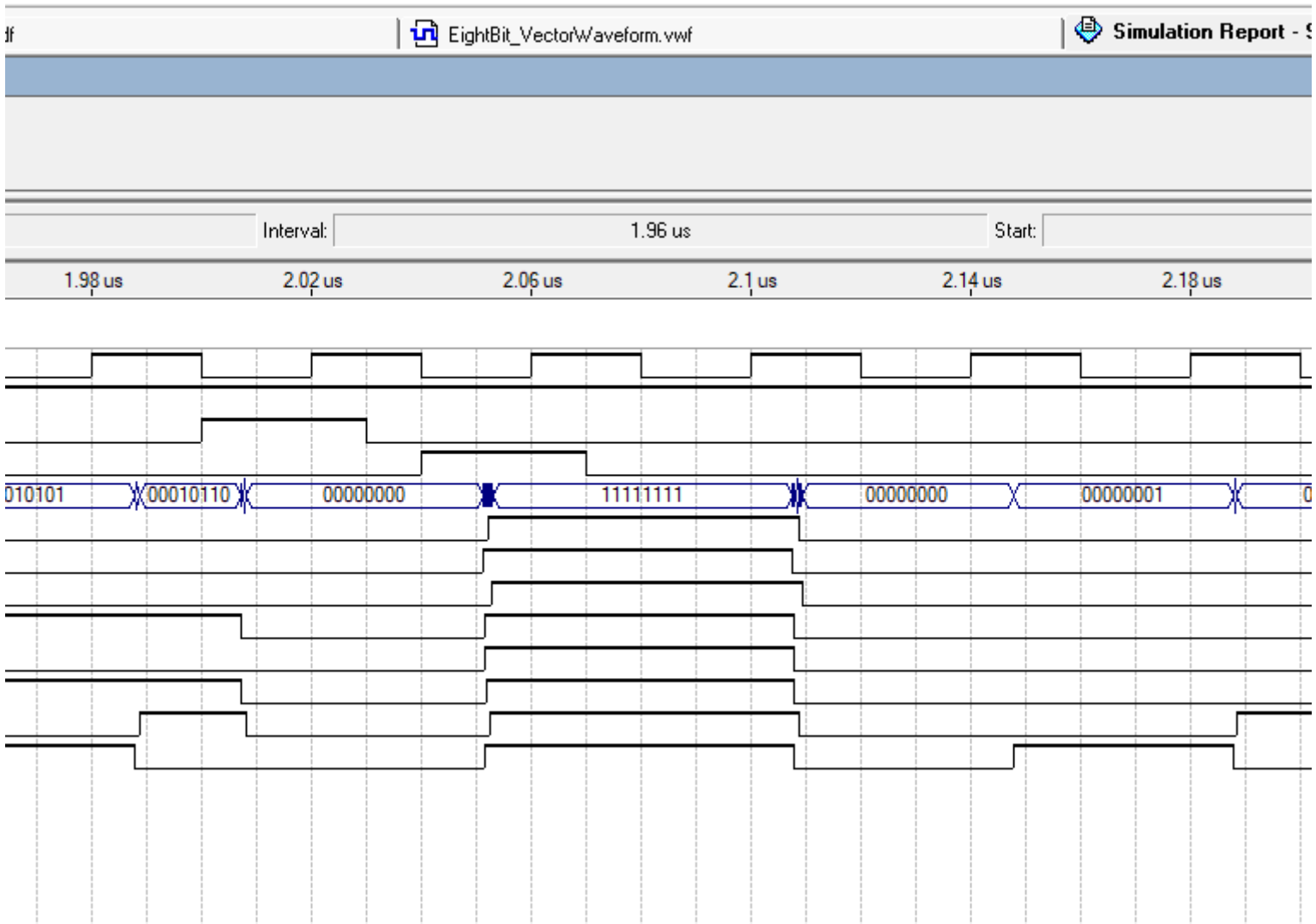
Registered Performance | tpd | tsu | tco | th | Custom Delays

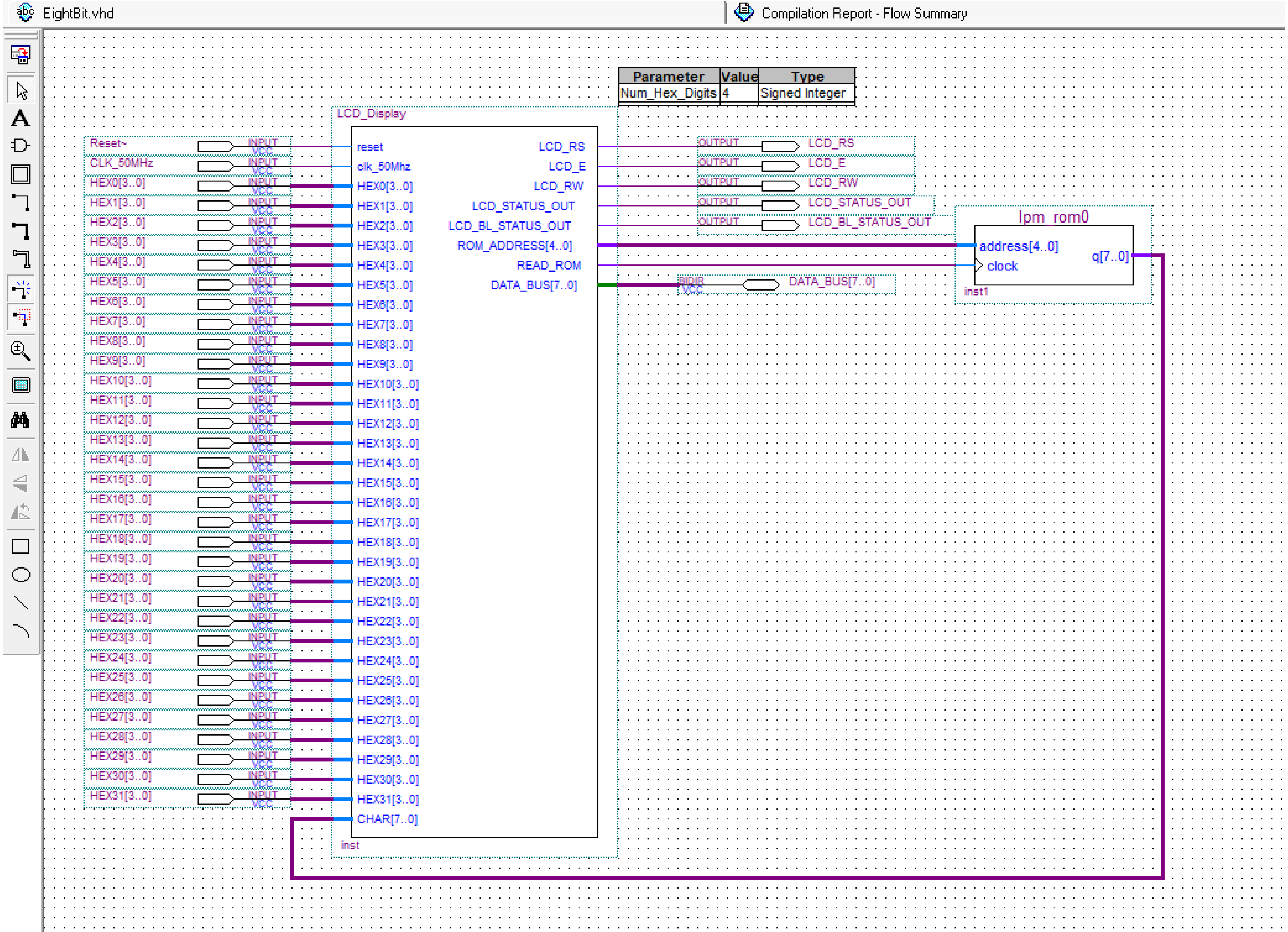
	Slack	Required P2P Time	Actual P2P Time	From	To
1	N/A	None	12.760 ns	Set	M[5]
2	N/A	None	12.467 ns	Set	M[1]
3	N/A	None	12.091 ns	Set	M[7]
4	N/A	None	11.724 ns	Set	M[2]
5	N/A	None	11.581 ns	Set	M[0]
6	N/A	None	11.481 ns	Set	M[4]
7	N/A	None	11.479 ns	Set	M[3]
8	N/A	None	11.055 ns	Set	M[6]
9	N/A	None	9.270 ns	Reset	M[5]
10	N/A	None	8.977 ns	Reset	M[1]
11	N/A	None	8.601 ns	Reset	M[7]
12	N/A	None	8.234 ns	Reset	M[2]
13	N/A	None	8.091 ns	Reset	M[0]
14	N/A	None	7.991 ns	Reset	M[4]
15	N/A	None	7.989 ns	Reset	M[3]
16	N/A	None	7.565 ns	Reset	M[6]

Η μέγιστη ταχύτητα λειτουργίας ειναι 12,76ns.


EightBit.vhd
Compilation Report - Flow Summary
EightBit_BlockDiagramm.bdf
EightBit_VectorWaveform.vwf
Simulati
Simulation Repor
Legal Notice
Flow Summar
Flow Settings
Simulator
Summary
Settings
Simulatior
Simulatior
INI Usage
Messages
Simulation Waveforms
Simulation mode: Timing
Master Time Bar:
40.0 ns
Pointer:
6.72 ns
Interval:
-33.28 ns
Start:
Name
Valu
40.
10.0 ns
50.0 ns
90.0 ns
130.0 ns
170.0 ns
210.0 ns
250.0 ns
290.0 ns
330.0 ns
370.0 ns
410.
40.0 ns+12.76 ns
0 Clk A
1 En A
2 Reset A
3 Set A
4 M B 000
5 M[7] B
6 M[6] B
7 M[5] B
8 M[4] B
9 M[3] B
10 M[2] B
11 M[1] B
12 M[0] B
00000000
11111111
00000000
00000001
00000010
00000011
00000

Και για να δειξουμε οτι οταν φτανει στην τιμη 11111111 παει μετα στην 00000000 :




EightBit.vhd
Compilation Report - Flow Summary
Parameter | Value | Type
Num_Hex_Digits | 4 | Signed Integer
LCD_Display
Reset~
CLK_50MHz
HEX0[3..0]
HEX1[3..0]
HEX2[3..0]
HEX3[3..0]
HEX4[3..0]
HEX5[3..0]
HEX6[3..0]
HEX7[3..0]
HEX8[3..0]
HEX9[3..0]
HEX10[3..0]
HEX11[3..0]
HEX12[3..0]
HEX13[3..0]
HEX14[3..0]
HEX15[3..0]
HEX16[3..0]
HEX17[3..0]
HEX18[3..0]
HEX19[3..0]
HEX20[3..0]
HEX21[3..0]
HEX22[3..0]
HEX23[3..0]
HEX24[3..0]
HEX25[3..0]
HEX26[3..0]
HEX27[3..0]
HEX28[3..0]
HEX29[3..0]
HEX30[3..0]
HEX31[3..0]
INPUT
VCC
reset
clk_50Mhz
CHAR[7..0]
inst
LCD_RS
LCD_E
LCD_RW
LCD_STATUS_OUT
LCD_BL_STATUS_OUT
ROM_ADDRESS[4..0]
READ_ROM
DATA_BUS[7..0]
OUTPUT
BIDIR
lpm_rom0
address[4..0]
clock
q[7..0]
inst1

Q4_ROM.hex

Addr	+0	+1	+2	+3	+4	+5	+6	+7
00	00	20	20	00	20	20	20	20
08	20	20	20	20	20	20	20	20
10	20	20	20	20	20	20	20	20
18	20	20	20	20	20	20	20	20

Οι θέσεις 00 και 03 είναι στην τιμή 00 αντί για 20 για να δέχονται τις 2 4bit εισόδους μας.
Χρησιμοποιούμε 2 θύρες γιατί δεν μπορούμε να βάλουμε 8bit σε μία