OSU ECEN 4233 HSCA, Spring 2023

HW 1: Introduction to SV Simulation

Instructor: James E. Stine, Jr.

Assigned: Wednesday, 1/25, 2023
Due **Friday 2/3, 2022** (midnight)
Handin: `http://canvas.okstate.edu`

- Using Structural Verilog, design a unit (using RTL) that computes the following for 64-bit computation:
  1. $Z = A \cdot B + C$. You can treat both A and B as unsigned values and use behavioral constructs to design your HDL. Make sure you adequately test your design with a testbench.
  2. Write an 8:1 multiplexer module called mux8 with inputs `s[2:0]`, `d0`, `d1`, `d2`, `d3`, `d4`, `d5`, `d6`, `d7`, and an output `y`.
  3. ECEN 5080 students: A sign extension unit extends a two's complement number from M to N ($N > M$) bits by copying the most significant bit of the input into the upper bits of the output. It receives an M-bit input A and produces an N-bit output Y. Sketch a circuit for a sign extension unit with a 32-bit input and an 64-bit output. Write the HDL for your design and test it..
- What to hand in? (3 things!) Each design should have the following. You are welcome to combine HDLs to produce simpler output waveforms for this assignment.
  - SystemVerilog files (SV and tb)
  - DO Files
  - Simulation Waveform

Please use our DLD text [1] as well as notes on Canvas to help you get started. The DLD text is on reserve in the library under ecen 3233. Do not Google anything as it just leads to problems!

References

[1] S. Harris and D. Harris, *Digital Design and Computer Architecture, RISC-V Edition.* Elsevier Science, 2021.