OSU ECEN 4233 HSCA, Spring 2023

HW 2: Carry-Lookahead Adders

Instructor: James E. Stine, Jr.

Assigned: Friday, 2/8, 2022
Due **Friday 2/17, 2022** (midnight)
Handin: `http://canvas.okstate.edu`

- Using SystemVerilog, design a 14-bit carry-lookahead adder with BCLGs and $r = 3$. Make sure you adequately test your design with a self-validating testbench.
- What to hand in? (3 things!)
  - SystemVerilog files (SV and tb)
  - DO Files
  - Simulation Waveform
  - Area/Delay analysis showing work on how you obtained result
- ECEN 5080 : repeat the problem using a Brent-Kung prefix adder [1, 2]. For the BK prefix adder, you can use the tools at the website and generate the HDL with the tool at the GitHub site: `https://github.com/tdene/synth_opt_adders`.

Please use our DLD text [3] as well as notes on Canvas to help you get started. The DLD text is on reserve in the library under ecen 3233. Do not Google anything as it just leads to problems!

References

[1] Brent and Kung, "A regular layout for parallel adders," *IEEE Transactions on Computers*, vol. C-31, no. 3, pp. 260–264, 1982.

[2] R. P. Brent and H. T. Kung, "A regular layout for parallel adders." `https://kilthub.cmu.edu/articles/journal_contribution/A_regular_layout_for_parallel_adders/6591290/1`, Jun 2018.

[3] S. Harris and D. Harris, *Digital Design and Computer Architecture, RISC-V Edition.* Elsevier Science, 2021.