C5X, 0.5μm Technology

Design Rules

Owner: Technology Research & Development

C5X (0.5 micron) Revision History

Revision	Release Date	Revision Detail
T	18-May-2005	• Added minimum metal density of 30% rule to Metal 1, Metal 2, and Metal 3 layout rules.
S	06-Apr-2005	• Removed all die seal ring rules and added notice that AMIS Reticle Data Prep groups will place the die seal ring. No customer variations will be allowed.
R	21-Dec-2004	• PISP - Min PI space from 0.6um to 0.7um • PLOSP - Min PLO space from 0.6um to 0.7um • Removed peripheral bus rules • Added Die Seal Rules • NIOPLO - NI over PLO not allowed - changed to: NIOPI - NI over PI not allowed
Q	04-Nov-2004	• Fix Design Rule conflicts by adding rules in sections: ○ NI Device (Rule: NIOPLO) ○ P+ (Rules: PEPI, PEPLO) ○ PI Device/PL Resistor (Rules: PIOPLO, PISNI) ○ PLO Device (Rules: NISPLO, PISPLO, PLOONI)
P	08-Sept-2004	• Centerline the Vtgm for: ○ N20X5ND Double Sided ○ N20X3ND Single Sided ○ N20X5ED Double Sided ○ N20X5ED Single Sided • Added the word "Mandatory" to the Layout rule descriptions for N40VTILE, P40VTILE, Schottky Devices • NI, PI, and PLO device IDSAT_5 adjusted to match wafer data
O	26-Sept-2003	• No nested vias over schottky contact • Schottky contact P+ spacing : 0.20 • Schottky contact length : 20.20 • Schottky requires poly 2 process • Schottky contact width : 0.70 • Via to metal line below with no other lower metal within 8 microns placed .7 micron of line end or corner
N	08-July-2003	• Layout design rules descriptions changed in 15/15V Ext-Drain Double Sided PCh, 15/20V Ext-Drain Single Sided PCh, 5/20V Ext-Drain PCh, BiPolar Devices, and External Connection sections.
M	20-Dec-2002	• Add design rule for Poly-2 ovl Cnt when Poly-2 is over Poly-1 to 0.3um • Change Poly-2 ovl of Poly-1 from 1um to 0.5 • Change Cnt to High-R spacing from 0.6um to 0.5um • Change Poly-Cnt spacing to Top Plate Poly-2 Spacing from 0.6 to 0.5

		• Change the N+ Poly-1 Sheet Resistance spec for Dbl Ply processes from 23-37 ohms/sq to 20-30 ohms/sq • Reduced the Cnt Resistance specs
L	05-Nov-2002	• Changed C5x parametric design rules N-Channel Electrical Parameters: Gamma, Idsat_5, Kprime_L, Leff_i, Vt_gm N20x0.6, Vt_gm N20x20, Weff_gm to better match process statistics at MAP. • Changed C5x parametric design rules P-Channel Electrical Parameters: Gamma, Idsat_5, Kprime_L, Leff_i, Vt_gm P20x0.6, Vt_gm P20x20, Weff_gm to better match process statistics at MAP. • Removed C5 Silicide rules per foundry request. • Changed description of MP40V and MN40V layout rules to make them easily understandable by layout engineers. Reduced drain area to follow minimum active overlap of contact. • Added NI Device, PI Device/PL Resistor, PLO Device layout rules and parametric specs. Required for transfer to Prototype phase. • Changed the name of Design rules in the double side extended-drain devices to be unique to the specific device. • Changed the drift region on the extended drain devices to mandatory from minimum. • Added design rules for small bipolar and clarified rule descriptions. • Clarified the description on the wide metal rule spacings. • Removed units from antenna rules.
K	09-Aug-2002	Added/updated layout rules for Bipolar, Schottky, ESD, and Nwell
J	13-Feb-2002	Added parametric specs and Layout rules for N40VTile and P40VTile devices. These devices run in C5R (AMI500 40 Volt) process. These devices are non-scalable. (Document Control release date: 03/27/2002)
I	15-Jan-2002	Top metal resistance decreased
H	21-Dec-2001	Added layout and parametric specs for Schottky diode.
G	04-May-2001	• added silicided resistance and temperature data • added the External Connection (ESD) rules • updated the P nested drain parameters • updated the P/N extended drain layout rules • updated the parametric symbol names and descriptions • removed the SOG Structural parameters • updated the Introduction to rename Research & Development group to Advanced Device Technology group
F	11-July-2000	• Capacitor Parametrics updated for CMP process • Kprime_S for N20x20 corrected to agree with MAP specs • Values for P0.8x0.6 and N0.8x0.6 Vt_gm added to Parametric Specs

		• Additional Notes added for High Voltage Layout Rules and Parametrics
E	09-Mar-2000	• Changes were made to the layout rules to obtain agreement between the Design Rules Web page and the ARG rules database. These changes were made to ensure that rules checked in the ARG database are detailed in the Web pages. • Nested Drain Devices were added, although, all High Voltage devices will only be released to inside customers unless a special license agreement has been signed. • Pad and Per-Bus rules where updated to match L5.
D	29-Nov-1999	• We are adding the C5 Design Rule Document to the Web. • We have updated the Metalization thicknesses to reflect where we are running. • We have added the C5 Extended Drain Document to the Design Rules. • We have added the Dual-Gate Extended Drain Devices to the Design Rules. • We have updated the Pad and PerBus rules.
C	12-May-1999	• Changed Parametric-Resistor M1,M2 and M3 sheet rho to 85+/-10 mohms/square per TRB 4/30/99
B	05-Nov-1998	• Referencing Double Poly. • Change diffusion rules to match new libraries, add high poly resistor for mixed signal, change pads and seal ring to use a mandatory contact sizes to aid manufacturing.
A	01-June-1998	• Initial Release

C5X (0.5 Micron) Design Rules

Introduction

AMIS 4500099 Rev: T, 18-May-2005

SCOPE:

- This website contains the layout design rules, parametric specifications and device models for the C5 process family.
- This website does not contain reticle biasing or data fracture information. Reticle biasing and data fracture information are controlled and documented by the RICE data base.
- This website does not contain reticle CD information. See the C5(X) CD reference guide (AMI document 4150143).
- This website does not contain parametric data extraction methodologies. See TIPS NOTES (AMI document 4510053).

PURPOSE:

- This website provides the layout design rules, electrical parametrics and device models required to design in the AMI C5 process family.
- The layout design rules provided are to be used for the electronic design check. All violations found should be fixed or waived by the Technology Research and Development Department.
- The parametric limits provided in this website are used when electrically testing the wafer at MAP. The wafer Pass/Fail criteria is based on meeting a subset of these specifications as outlined in the C5 Map Limits document (AMI 7100101).

RESPONSIBILITIES:

- AMIS' Technology Research and Development Department is responsible for maintaining this website. Questions concerning interpretation or clarification should be directed to the Technology Research and Development Department.

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C5X (0.5 Micron) Design Rules

Layout Rules' Notes

AMIS 4500099 Rev: T, 18-May-2005

The following tables consist of design rules to be adhered to during layout. To obtain reticle or final processing dimensions refer to the CD Reference Guide for the C5 process. These design rules were generated assuming a maximum supply operating voltage of 5.5V and a maximum absolute supply voltage of 6V. Operation at supply voltages greater than 5.5V will adversely affect reliability. Supply voltages exceeding 6V even for short periods may damage the circuit. The high voltage devices available in this process have voltage limits appropriate for each device. Refer to the layout rules and parametric specifications for more information.

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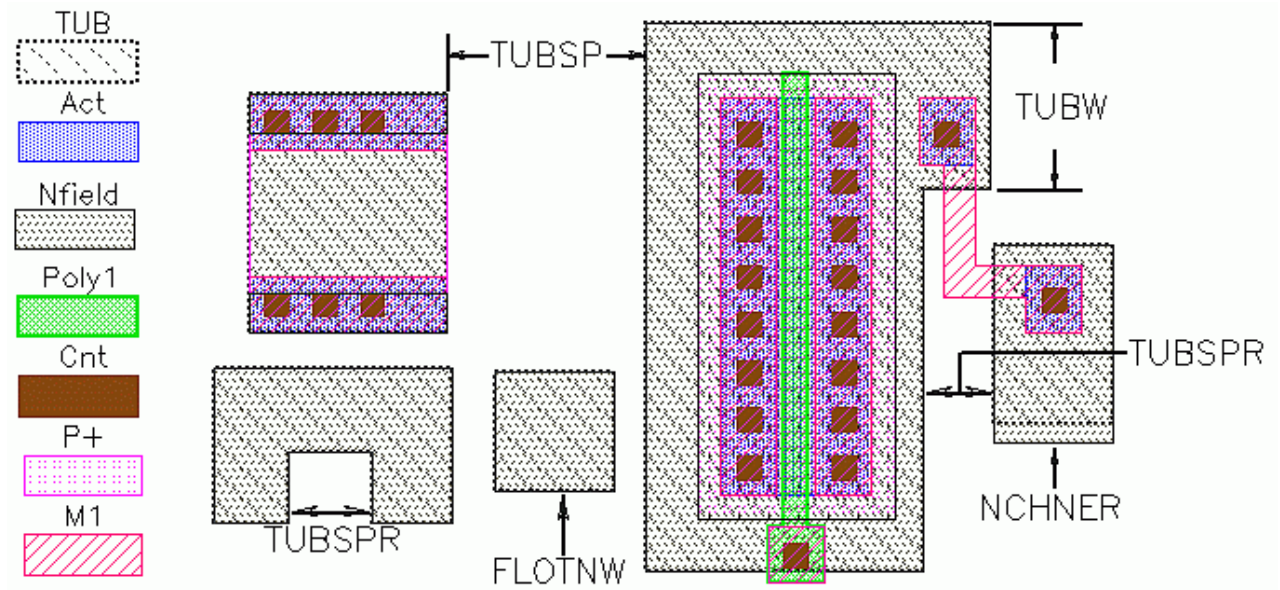
C5X (0.5 Micron) N-WELL Layout Rules

Layer/level #1 (TUB)



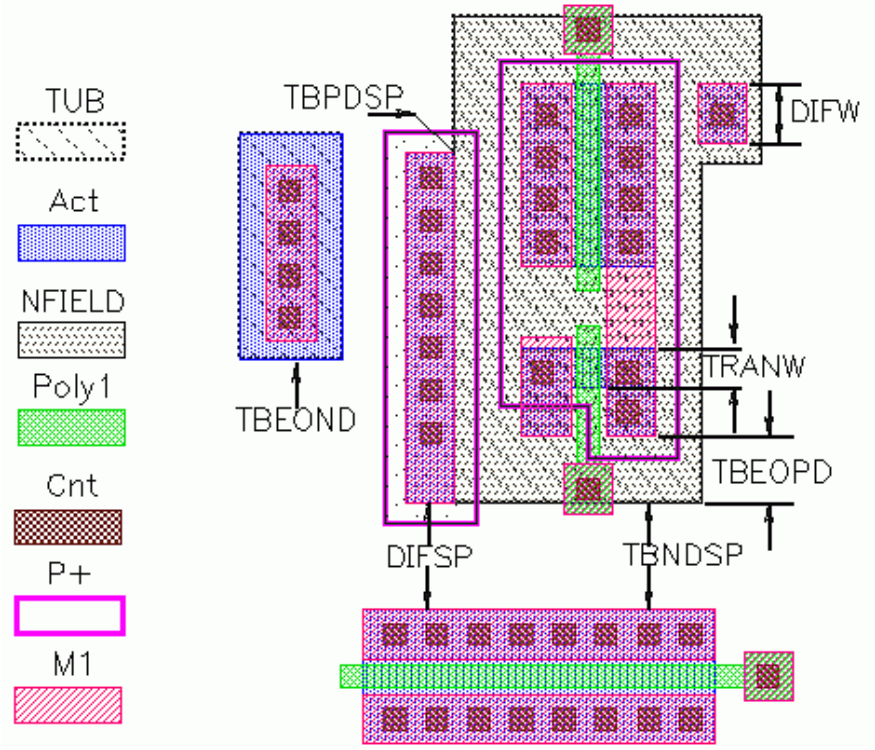
Note 1: TUB layer is drawn to define areas that will be implanted with n-tub implant. (ie N-Well is drawn and implanted over P-substrate).

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
FLOTNW	FLOaTing N-Wells			*	Floating N-Wells are those that contain P+ Active contacted to metal that do not have a corresponding N+ well-tie contacted to metal.
FLOTPW	FLOaTing P-Wells			*	A continuous N-Well ring or moat defines a separate island of P-Well, that is floating if it contains N+ active contacted to metal without a corresponding P+ well-tie contacted to metal. (Not shown in graphic above)
NCHNER	NCHaN ERror if nchan is not identical to tub			*	With the exception of the Extended drain devices and N-Field generated for NI Devices.
TUBSP	Min TUB SPacing	4.00	µm	*	
TUBSPR	Min TUB Spacing related	2.00	µm	*	
TUBW	Min TUB Width	2.50	µm	*	Resistor less than 5.00 µm wide do not meet models

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) ACTIVE Layout Rules

Layer/level #2 (DIF)



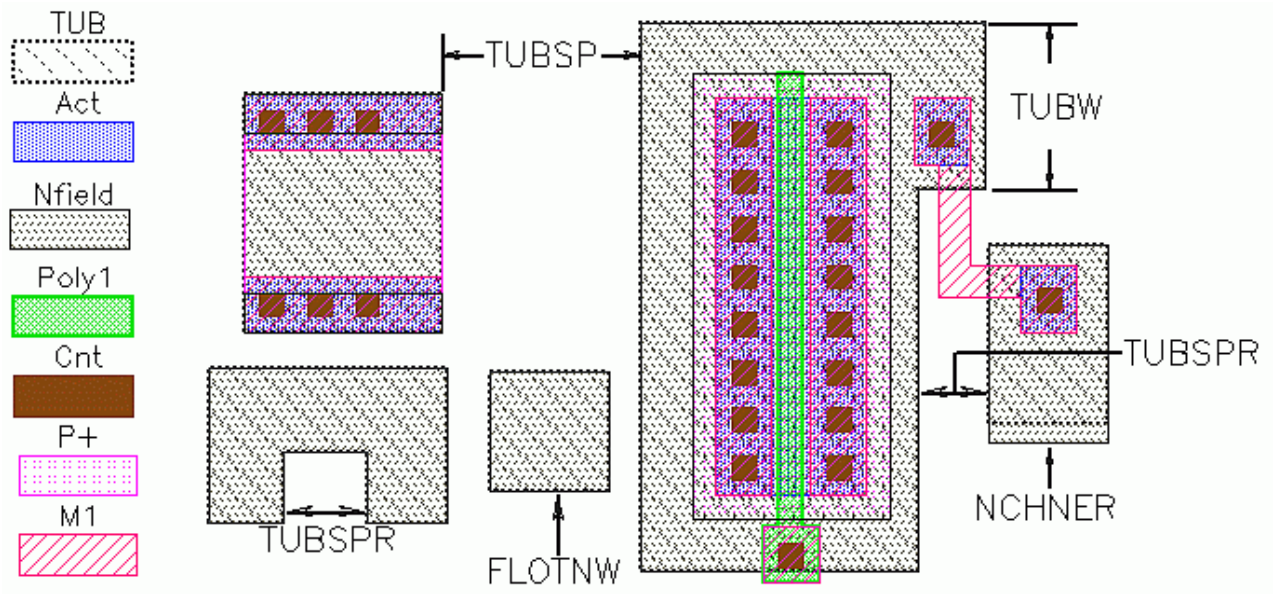
Note 1: Active Area (aka: DIF, Diffusion) or Field is used to define areas that will become diffusion (P,N,BN,etc.) as used in MOSFET source/drains,resistors, Bipolars and TUB/substrate tie downs (aka Guard Bars). In general Active refers to the drawn data, whereas Diffusion (N,P,BN,etc.) refers to implanted Active.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
DIFSP	Min DIFfusion SPacing	0.90	µm	*	
DIFW	Min DIFfusion Width	0.50	µm	*	Resistors less than 0.8 µm wide do not meet Parametric Specs and are not modeled accurately in simulation.
TBEOND	TuB Enclosure Of N-Diffusion	0.00	µm	*	Well Tie Only
TBEOPD	TuB Enclosure Of P-Diffusion	1.50	µm	*	
TBNDSP	TuB to N-Diffusion SPacing	1.50	µm	*	
TBPDSP	TuB to P-Diffusion SPacing	0.00	µm	*	Substrate Tie Only
TRANW	Minimum TRANsistor Width	0.80	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) NCH FLD Layout Rules

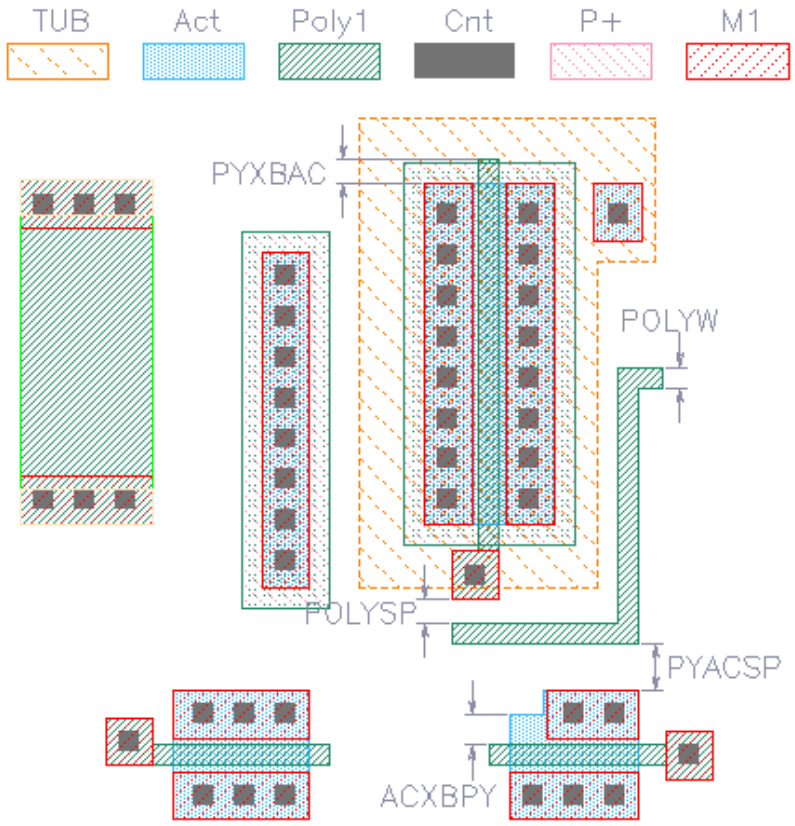
Layer/level #3 (NFIELD) Copy of Layer/level #1 (TUB or N-Well)



Note 1: N channel field is a copy of n-well except when extended drain devices are used. In this case, both layers must be drawn. For NI Device NCHFLD is not a copy of NWell and is generated at fracture.

C5X (0.5 Micron) POLY Layout Rules

Layer/level #4 (POLY1)



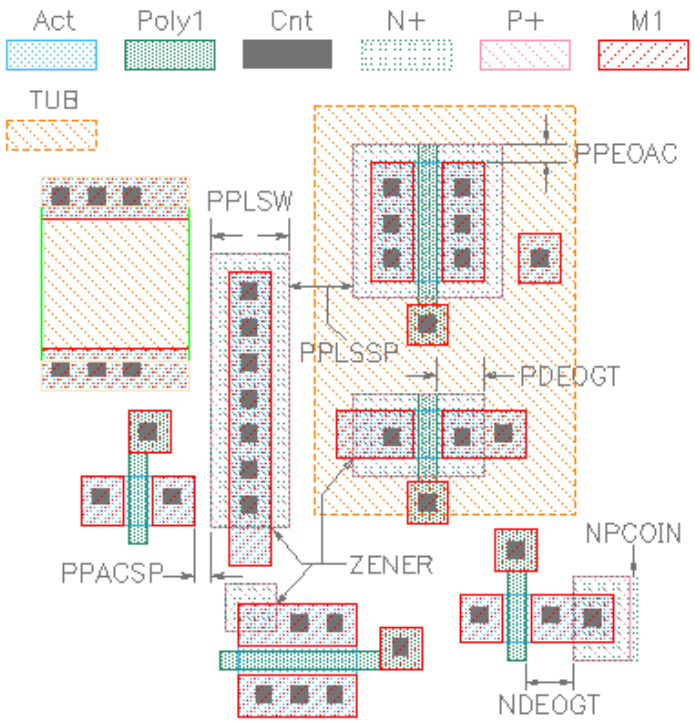
Note 1: Poly (aka: P1, PY1, Poly1 or Gate) layer is used to define interconnect, Poly(1) transistor gates, Floating gates in EE devices, resistors and Bottom Cap plates of double poly capacitors.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
ACXBPY	Min ACtive eXtension Beyond PolY	0.65	µm	*	S/D Dimension, must be checked when using butted contacts
POLYSP	Min POLY SPacing	0.60	µm	*	
POLYW	Min POLY Width	0.60	µm	*	
PY1ANT	PolY1 ANTenna check (100:1 ratio)	100.00		*	The ratio of Ply-not(Act) to Ply-Act for a single Poly polygon should not exceed 100:1. (not shown in graphic above)
PYACSP	Min PolY to ACtive SPacing	0.20	µm	*	
PYXBAC	Min PolY eXtension Beyond ACtive	0.50	µm	*	Poly End-Cap Rule

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) P+ Layout Rules

Layer/level #6 (PPLS) Copy of Layer/level #5 (NPLS)



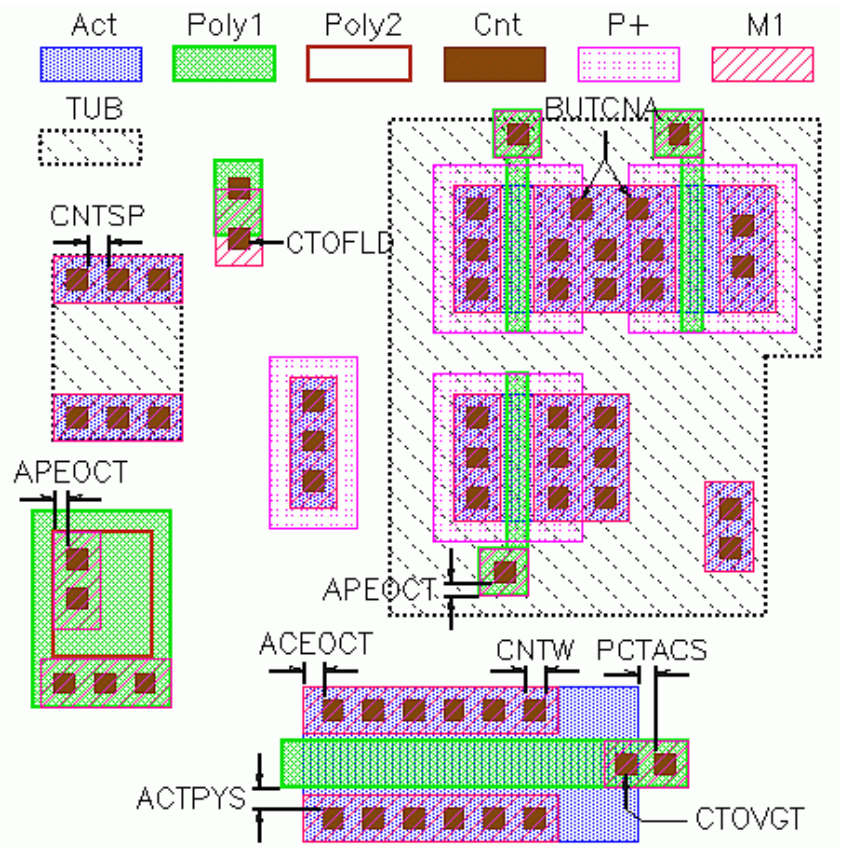
Note 1: P+ Implant (aka: PPLS or PPLUS) layer defines areas of Poly and Active that will receive a P+ implantation, resulting in P+ Diffusion and P-type Poly. N+ Implant (aka: NPLS or NPLUS) is a copy of P+ Implant, but its defined reticle will be a reverse image of P+.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
NDEOGT	Min N-Diffusion Enclosure Of GaTe	0.65	µm	*	N-Diffusion is defined as active regions not covered by N+
NPCOIN	Nplus/Pplus COINcide			*	N+ is a copy of P+ therefore must be coincident
PDEOGT	Min P-Diffusion Enclosure Of GaTe	0.65	µm	*	S/D Dimension, must be checked when using butted contacts
PEPI	Pplus enclosure of PI-Mandatory	0.00	µm	*	
PEPLO	Pplus enclosure of PLO-Mandatory	0.00	µm	*	
PPACSP	Min PPls to ACtive SPacing	0.30	µm	*	
PPEOAC	Min PPls Enclosure Of ACtive	0.30	µm	*	
PPLSSP	Min PPLS SPacing	0.70	µm	*	
PPLSW	Min PPLS Width	0.70	µm	*	
ZENER	P/N Active not at the same potential			*	not allowed

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) CONTACT Layout Rules

Layer/level #8 (CNT)



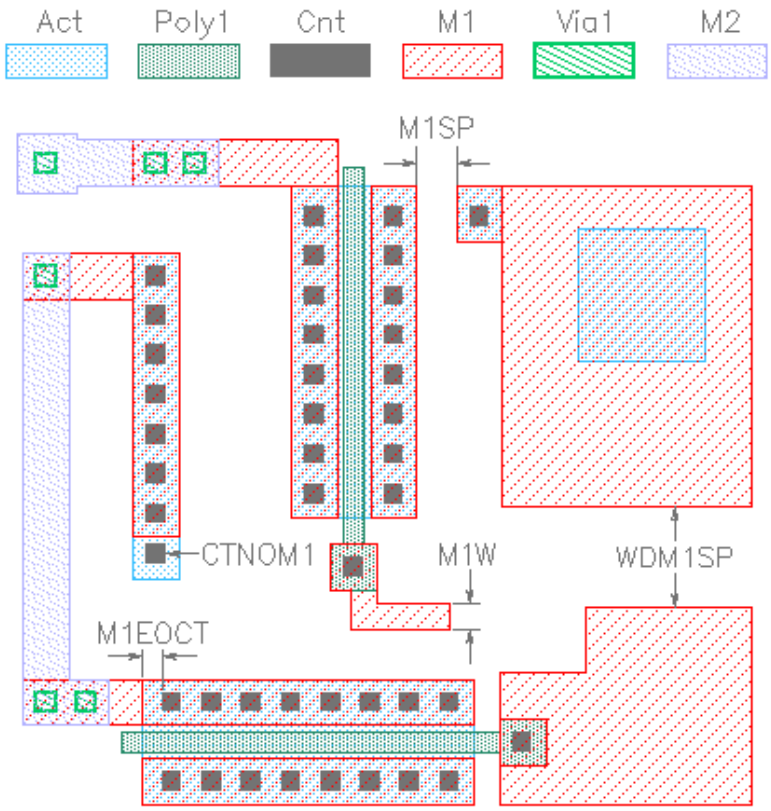
Note 1: Contact (aka: CT, CNT or Cont) layer is used to define connection points between Metal1 and Active or Poly(s).

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
ACEOCT	Min ACtive Enclosure Of CnT	0.30	µm	*	Internal Cell
ACTPYS	Min Active-ConTacts to any PolY Spacing	0.40	µm	*	Internal Cell (AMI gate arrays=0.35)
APEOCT	Min All-Poly Enclosure Of CnT	0.20	µm	*	
BUTCNA	BUTted Cnts Not Allowed			*	
CNTSP	Min CNT SPacing	0.50	µm	*	
CNTW	Man CNT Width	0.50	µm	*	Mandatory Cnt Size is 0.5x0.5 except for Schottky
CTOFLD	CnT Over FieLD			*	not allowed
CTOVGT	CnT OVer GaTe poly			*	not allowed
PCTACS	Min Poly-ConTacts to ACtive Spacing	0.40	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) METAL 1 Layout Rules

Layer/level #9 (M1)



Note 1: Metal 1 (aka: M1 or Met1) layer is used to define metal interconnect and supply bussing thru Contacts, to Active and Poly layers.

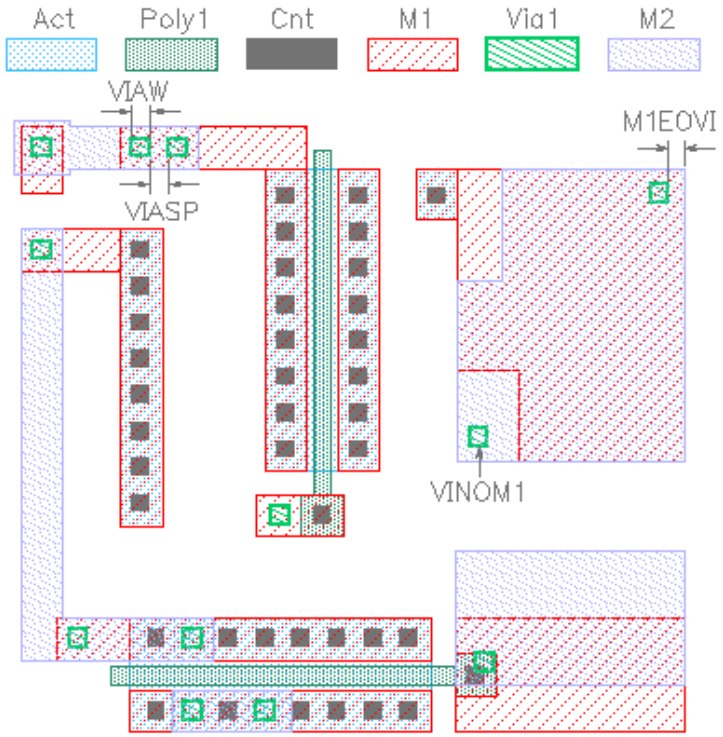
Rule Name	Rule Description	Rule	Units	Rule Type	Notes
CTNOM1	CnT with NO M1 cover			*	not allowed
M1DENS	Metal 1 minimum level density is 30%. If less, dummy structure should be added.	.3		*	Even if metal density rule is met, use of additional metal fill for all metal layers is encouraged to improve uniformity and yield. < 30% density is only allowed after the standard automated metal fill has been implemented on at least the non-analog sections of the circuit.
M1EOCT	Min M1 Enclosure Of CnT	0.20	µm	*	
M1PANT	Metal 1 to Poly gate ANTenna	1000.00		**	Max ratio of metal 1 area to poly transistor area when m1 is not contacting active area. Ratio=1000:1 (not shown in graphic above)
M1SP	Min M1 SPacing	0.60	µm	*	
M1W	Min M1 Width	0.60	µm	*	

WDM1SP	Min WiDe M1 to M1 SPacing	1.20	µm	*	Minimum spacing when either M1 width is greater than 10um.

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) VIA 1 Layout Rules

Layer/level #10 (VIA)

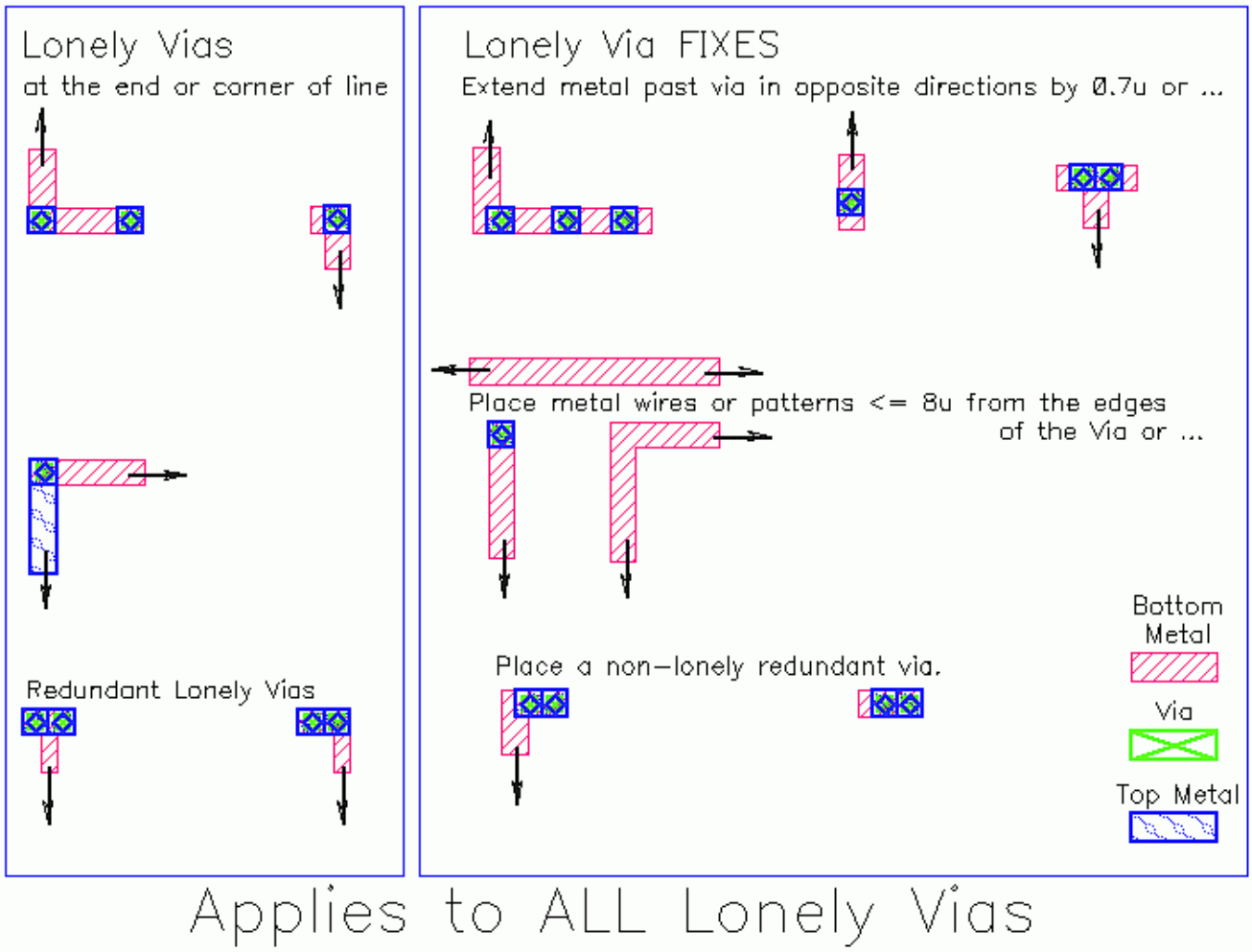


NOTE --->
More graphics to view!
See following page
for graphic # 2

Note 1: Via 1 (aka: Via or Via1) layer is used to define connection points between Metal1 and Metal2.

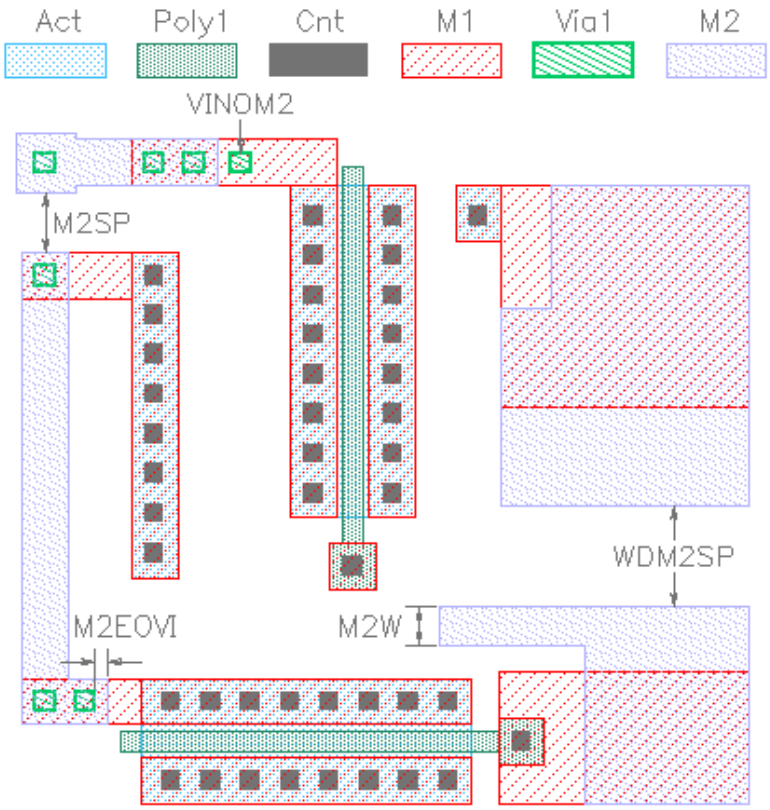
Rule Name	Rule Description	Rule	Units	Rule Type	Notes
LNLYVIA1	Lonely VIA1 needs redundancy, extra metal, or patterning			*	Defined as: Via in a corner or at the end of a wire with minimum metal surround, has no redundancy, has no metal patterns within 8u. Lonely Via rules are applied to the via and bottom connect layer only. (Solutions: extend metal past via in opposite directions by 0.7u or place metal wires or patterns <= 8u from the edges of the Via or place a non-lonely redundant via.) NOTE: Please see the following page for the Lonely Via graphic.
M1EOVI	Min M1 Enclosure Of VIa	0.20	µm	*	
VIASP	Min VIA SPacing	0.60	µm	*	
VIAW	Man VIA Width	0.50	µm	*	Mandatory Via 1 size is 0.5x0.5
VINOM1	VIa with NO M1 under			*	not allowed

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)


Lonely Vias
at the end or corner of line
Redundant Lonely Vias
Lonely Via FIXES
Extend metal past via in opposite directions by 0.7u or ...
Place metal wires or patterns <= 8u from the edges
of the Via or ...
Place a non-lonely redundant via.
Bottom Metal
Via
Top Metal
Applies to ALL Lonely Vias

C5X (0.5 Micron) METAL 2 Layout Rules

Layer/level #11 (M2)



Note 1: Metal 2 (aka: M2 or Met2) layer is used to define Metal2 interconnect and supply bussing thru Vias, to the Metal1 layer.

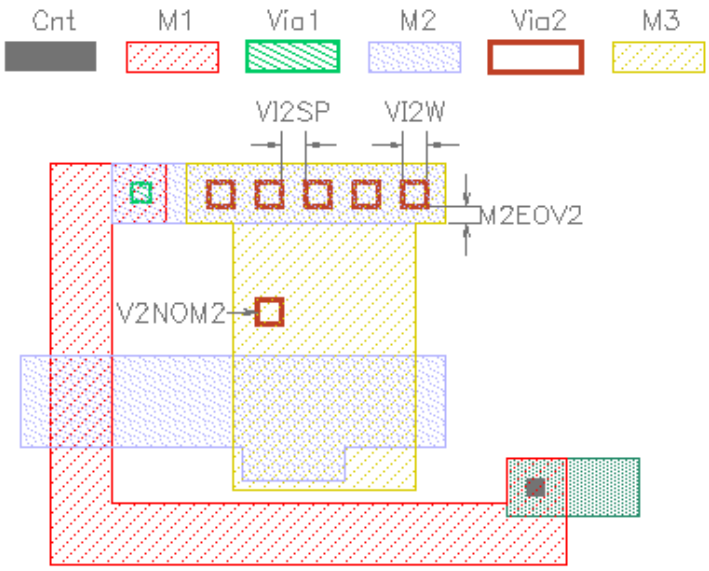
Rule Name	Rule Description	Rule	Units	Rule Type	Notes
M2DENS	Metal 2 minimum level density is 30%. If less, dummy structure should be added.	.3		*	Even if metal density rule is met, use of additional metal fill for all metal layers is encouraged to improve uniformity and yield. < 30% density is only allowed after the standard automated metal fill has been implemented on at least the non-analog sections of the circuit.
M2EOVI	Min M2 Enclosure Of VIa	0.20	µm	*	
M2PANT	Metal 2 to Poly gate ANTenna	1000.00		**	Max ratio of metal 1 area to poly transistor area when m1 is not contacting active area. Ratio=1000:1 (not shown in graphic above)
M2SP	Min M2 SPacing	0.70	µm	*	
M2W	Min M2 Width	0.70	µm	*	

VINOM2	VIa with NO M2 cover			*	not allowed
WDM2SP	Min WiDe M2 to M2 SPacing	1.20	µm	*	Minimum spacing when either M2 width is greater than 10um.

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) VIA 2 Layout Rules

Layer/level #12 (VIA2)

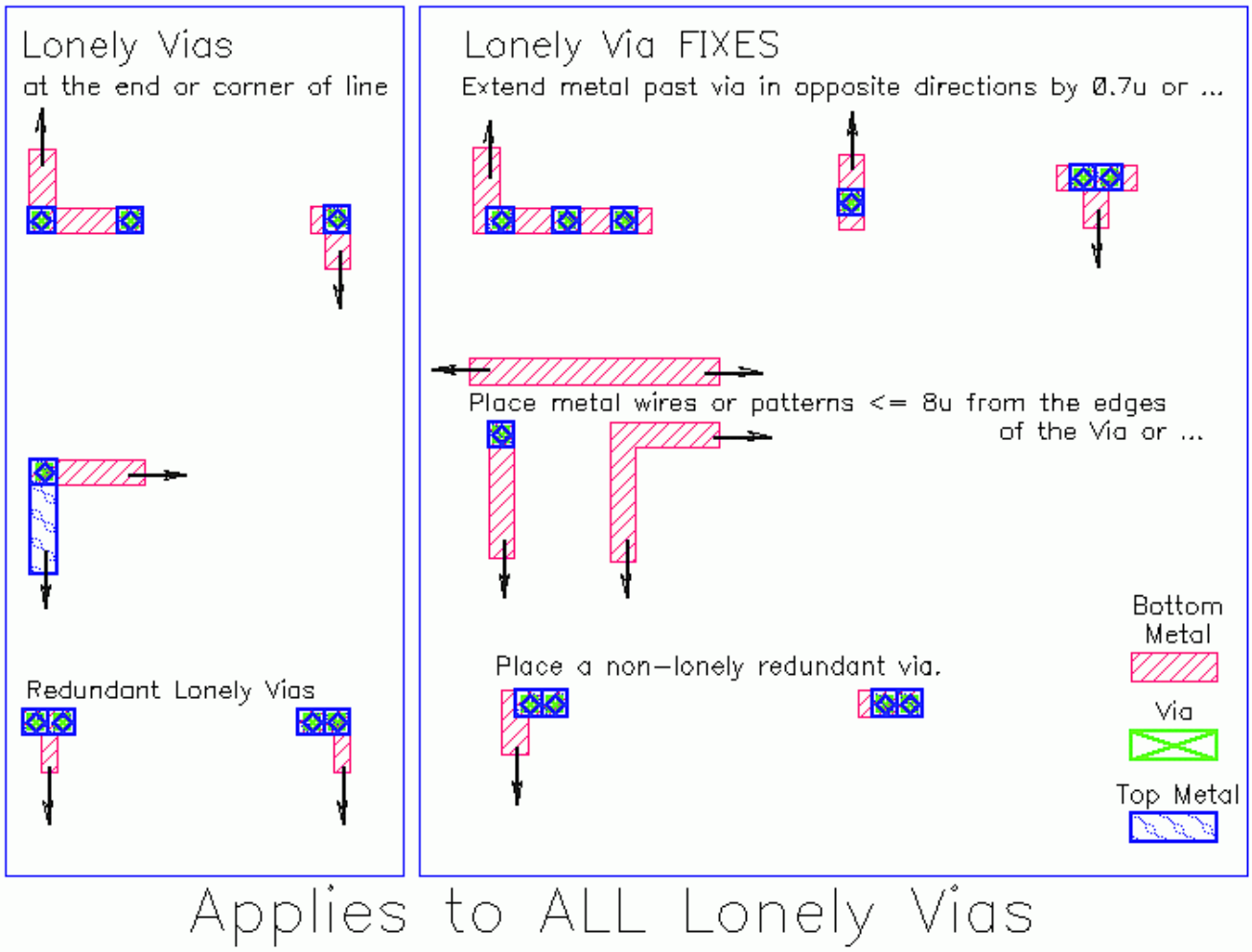


NOTE --->
More graphics to view!
See following page
for graphic # 2

Note 1: Via2 (aka: V2, VI2 or VIA2) layer is used to define connection points between Metal2 and Metal3.

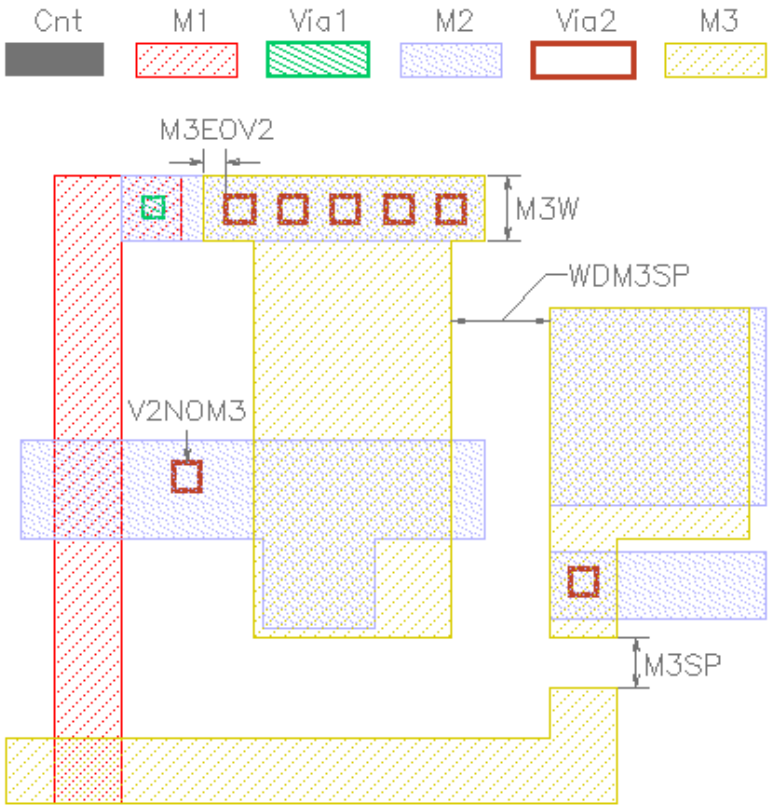
Rule Name	Rule Description	Rule	Units	Rule Type	Notes
LNLYVIA2	Lonely VIA2 needs redundancy, extra metal, or patterning			*	Defined as: Via in a corner or at the end of a wire with minimum metal surround, has no redundancy, has no metal patterns within 8u. Lonely Via rules are applied to the via and bottom connect layer only. (Solutions: extend metal past via in opposite directions by 0.7u or place metal wires or patterns <= 8u from the edges of the Via or place a non-lonely redundant via.) NOTE:Please see the following page for the Lonely Via graphic.
M2EOV2	Min M2 Enclosure Of Via2	0.20	µm	*	
V2NOM2	Via 2 with NO M2 under			*	not allowed
VI2SP	Min VI2 SPacing	0.80	µm	*	
VI2W	Man VI2 Width	0.50	µm	*	Mandatory Via 2 size 0.5x0.5

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)


Lonely Vias
at the end or corner of line
Redundant Lonely Vias
Lonely Via FIXES
Extend metal past via in opposite directions by 0.7u or ...
Place metal wires or patterns <= 8u from the edges
of the Via or ...
Place a non-lonely redundant via.
Bottom Metal
Via
Top Metal
Applies to ALL Lonely Vias

C5X (0.5 Micron) METAL 3 Layout Rules

Layer/level #13 (M3)



Note 1: Metal 3 (aka: M3 or Met3) layer is used to define Metal3 interconnect and supply bussing thru Via2, to Metal2.

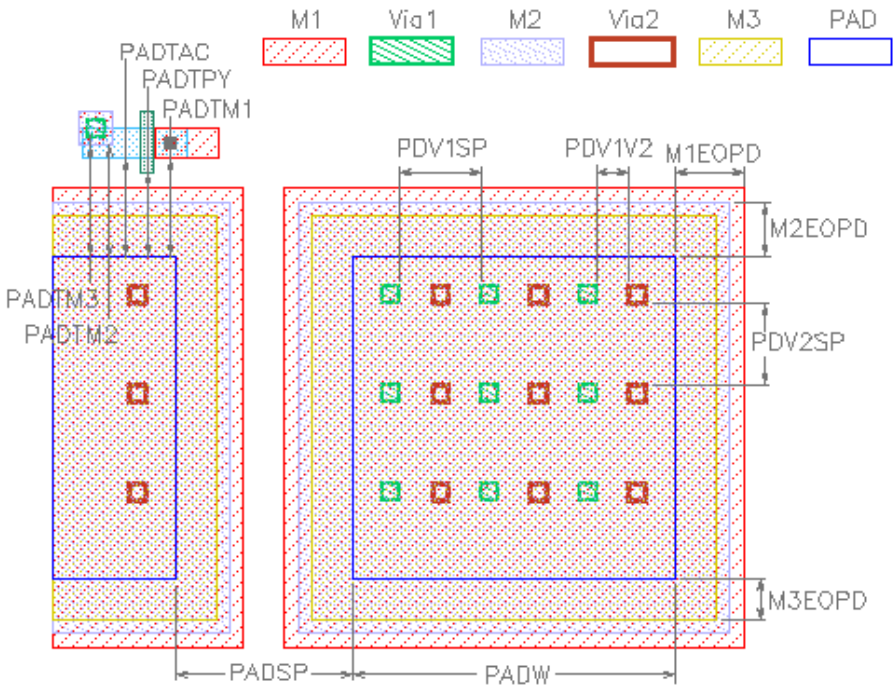
Rule Name	Rule Description	Rule	Units	Rule Type	Notes
M3DENS	Metal 3 minimum level density is 30%. If less, dummy structure should be added.	.3		*	Even if metal density rule is met, use of additional metal fill for all metal layers is encouraged to improve uniformity and yield. < 30% density is only allowed after the standard automated metal fill has been implemented on at least the non-analog sections of the circuit.
M3EOV2	Min M3 Enclosure Of Via2	0.20	µm	*	
M3PANT	Metal 3 to Poly gate ANTenna	1000.0		*	Max ratio of metal 1 area to poly transistor area when m1 is not contacting active area. Ratio=1000:1 (not shown in graphic above)
M3SP	Min M3 SPacing	0.70	µm	*	
M3W	Min M3 Width	0.80	µm	*	

V2NOM3	Via 2 with NO M3 covering			*	not allowed
WDM3SP	Min WiDe M3 to M3 Spacing	1.20	µm	*	Minimum spacing when either M3 width is greater than 10um.

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) PAD Layout Rules

Layer/level #14 (PAD)

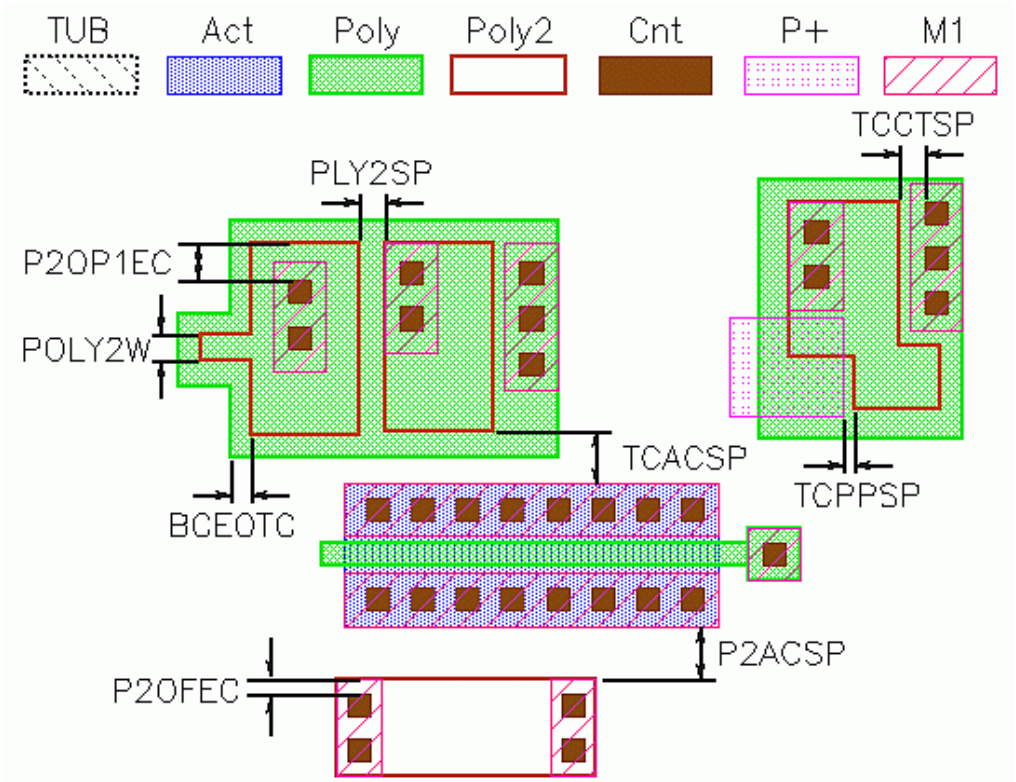


Note 1: PAD (aka Bond Pad or Passivation) layer is used to define areas for Top-side Passivation openings (PAD Windows) so the circuit can be connected to a Package or lead frame. PAD rules are generally governed by Packaging Vendors not necessarily by AMI. In tungsten-plug processes MANDATORY size and spacing for via layers in Pad windows will be enforced.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
M1EOPD	Min M1 Enclosure Of PaD	3.00	µm	*	
M2EOPD	Min M2 Enclosure Of PaD	2.40	µm	*	
M3EOPD	Min M3 Enclosure Of PaD	1.20	µm	*	
PADSP	Min PAD SPacing	12.00	µm	*	
PADTAC	PAD To ACtive spacing	10.00	µm	*	
PADTM1	PAD To unrelated M1	8.00	µm	*	
PADTM2	PAD To unrelated M2	8.00	µm	*	
PADTM3	PAD To unrelated M3	8.00	µm	*	
PADTPY	PAD To unrelated Poly	10.00	µm	*	
PADW	Min PAD Width	50.00	µm	*	Pad window and pitch should be drawn to accomodate bonding capability.
PDV1SP	Pad/Via1 SPacing	3.00	µm	*	Same layer Vias
PDV1V2	Pad/V1 to pad/V2 SPacing	1.00	µm	*	Stacked, adjacent layer Vias not allowed
PDV2SP	Pad/Via2 SPacing	3.00	µm	*	

C5X (0.5 Micron) POLY2 Layout Rules

Layer/level #26 (POLY2)



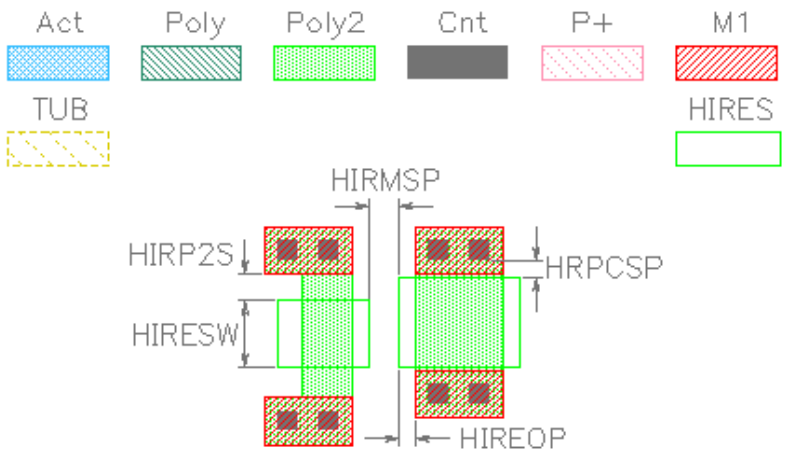
Note 1: Poly2 (aka: P2, PY2 or Cap Poly in some processes) layer is used to define interconnect, Top capacitor plate, resistors (HIRes), Control Gates for EE devices.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
BCEOTC	Min BotCap plate Enclosure Of TopCap plate	0.50	µm	*	
P2ACSP	Min Poly2 to ACtive SPacing	0.20	µm	*	
P2OFEC	Min Poly2 Over Field Enclosure of Contact	0.20	µm	*	
P2OP1EC	Min Poly2 Over Poly1 Enclosure of Contact	0.30	µm	*	
PLY2SP	Min POLY2 SPacing	0.80	µm	*	
POLY2W	Min POLY2 Width	2.00	µm	*	
TCACSP	Min TopCap plate to ACtive SPace	2.00	µm	*	
TCCTSP	Min TopCap plate to CnT SPacing	0.50	µm	*	
TCPPSP	Min TopCap to PPls SPace	2.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) HR POLY RESISTOR Layout Rules

Layer/level #27 (HIRES)



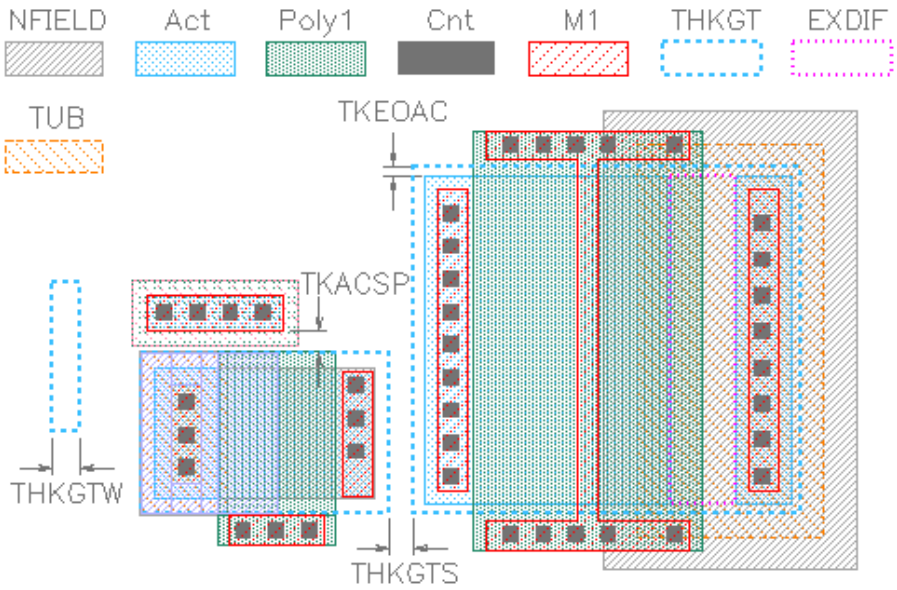
Note 1: HIRES Mask layer (aka: HIR or HIR-poly) blocks Poly2 doping, which results in Poly2 with much Higher Resistance.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
HIREOP	Min HIRes Enclosure Of Poly2	1.00	µm	*	
HIRESW	Min HIRES Width	2.00	µm	*	
HIRMSP	Min HIRes Mask SPace	1.00	µm	*	
HIRP2S	Min HIRes to Poly2 Space	1.00	µm	*	
HRPCSP	Min HiR over Poly2 to Cnt SPace	0.50	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) THICKGATE Layout Rules

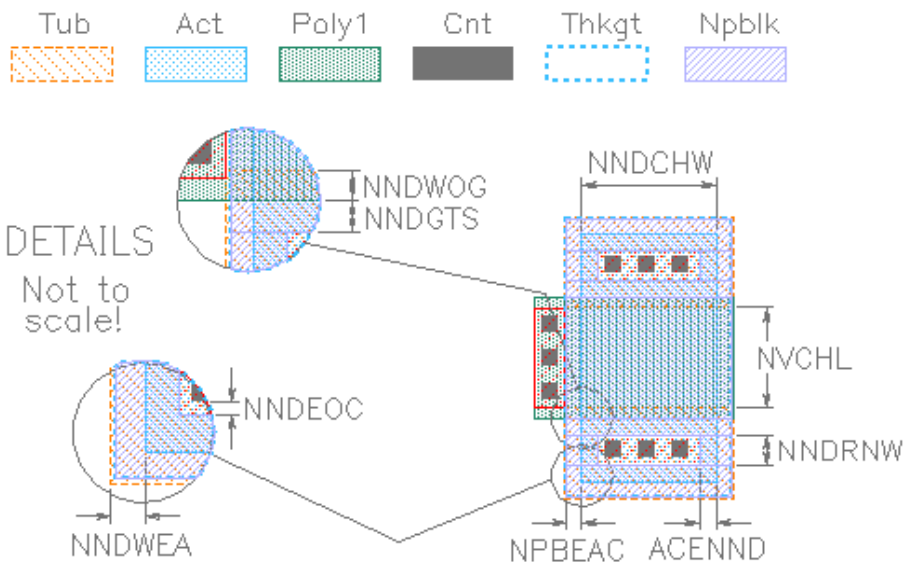
Layer/level #28 (THKGT)



Rule Name	Rule Description	Rule	Units	Rule Type	Notes
THKGTS	Min THKGT Spacing	0.70	µm	*	
THKGTW	Min THKGT Width	1.00	µm	*	
TKACSP	Min ThKgt to ACtive SPacing	0.30	µm	*	
TKEOAC	Min ThKgt Enclosure Of ACtive	0.30	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) 12V DOUBLE SIDED NESTED-DRAIN NCH Layout Rules



Note 1: Nested-N-Drain is the active region of an N-Ch Nested-Drain Transistor that is not covered by N+Blk mask. This region gets both the N-LDD and N+ implants.

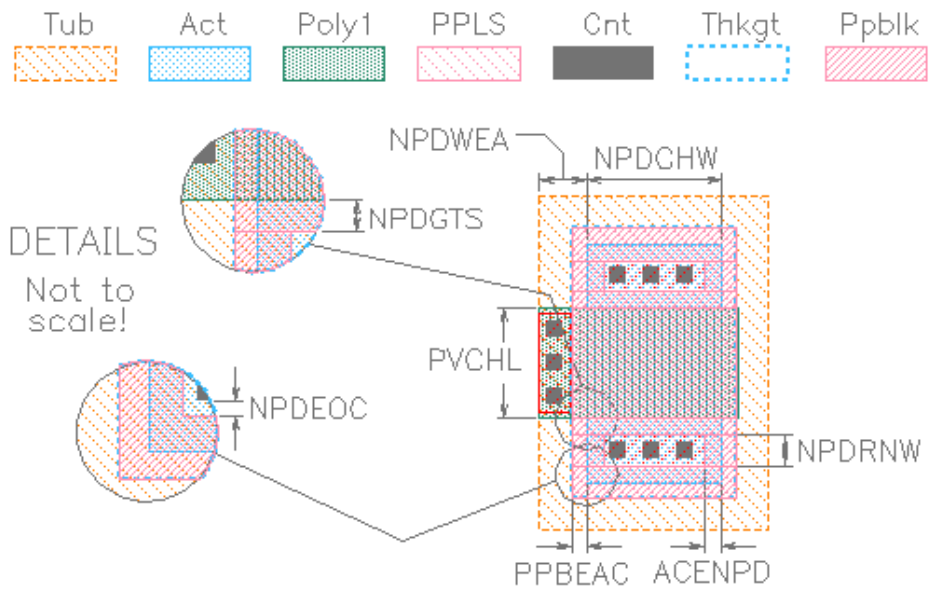
Note 2: Nested-N-Drain-Well is the well region below the Drain of a NCh Nested-Drain. For a Double-Sided NCh Nested-Drain device, the channel region starts from the N-Well Edge on the Drain side of the device and ends at the N-Well edge on the Source side. Note Source and Drain are interchangeable.

Note 3: NPBLK blocks the N+ implant but not the N-LDD implant from Active and Poly. NPBLK supersedes N+ drawn.

Note 4: This device will not be recognized if ThickGate does not cover the active region.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
ACENND	Man ACtive Enclosure of Nested-N-Drain	0.50	µm	*	
NNDCHW	Min Nested-N-Drain-CHannel Width	4.00	µm	*	
NNDEOC	Min Nested-N-Drain Enclosure Of Contact	0.20	µm	*	
NNDGTS	Man Nested-N-Drain to Gate Spacing	0.50	µm	*	
NNDRNW	Man Nested-N-DRaiN Width	0.90	µm	*	
NNDWEA	Man Nested-N-Drain-Well Enclosure of Active	0.50	µm	*	
NNDWOG	Man Nested-N-Drain-Well Overlap of Gate	0.50	µm	*	
NPBEAC	Min NPBlk Enclosure of ACtive	0.30	µm	*	
NVCHL	Min. NV-type nested-drain-CHannel-Length	5.00	µm	*	

C5X (0.5 Micron) 12V DOUBLE SIDED NESTED-DRAIN PCH Layout Rules



Note 1: Nested-P-Drain is the active region of an P-Ch Nested-Drain Transistor that is not covered by P+Blk mask. This region gets both the P-LDD and P+ implants.

Note 2: Nested-P-Drain-Well is the N-Well under the PCh Nested-Drain device.

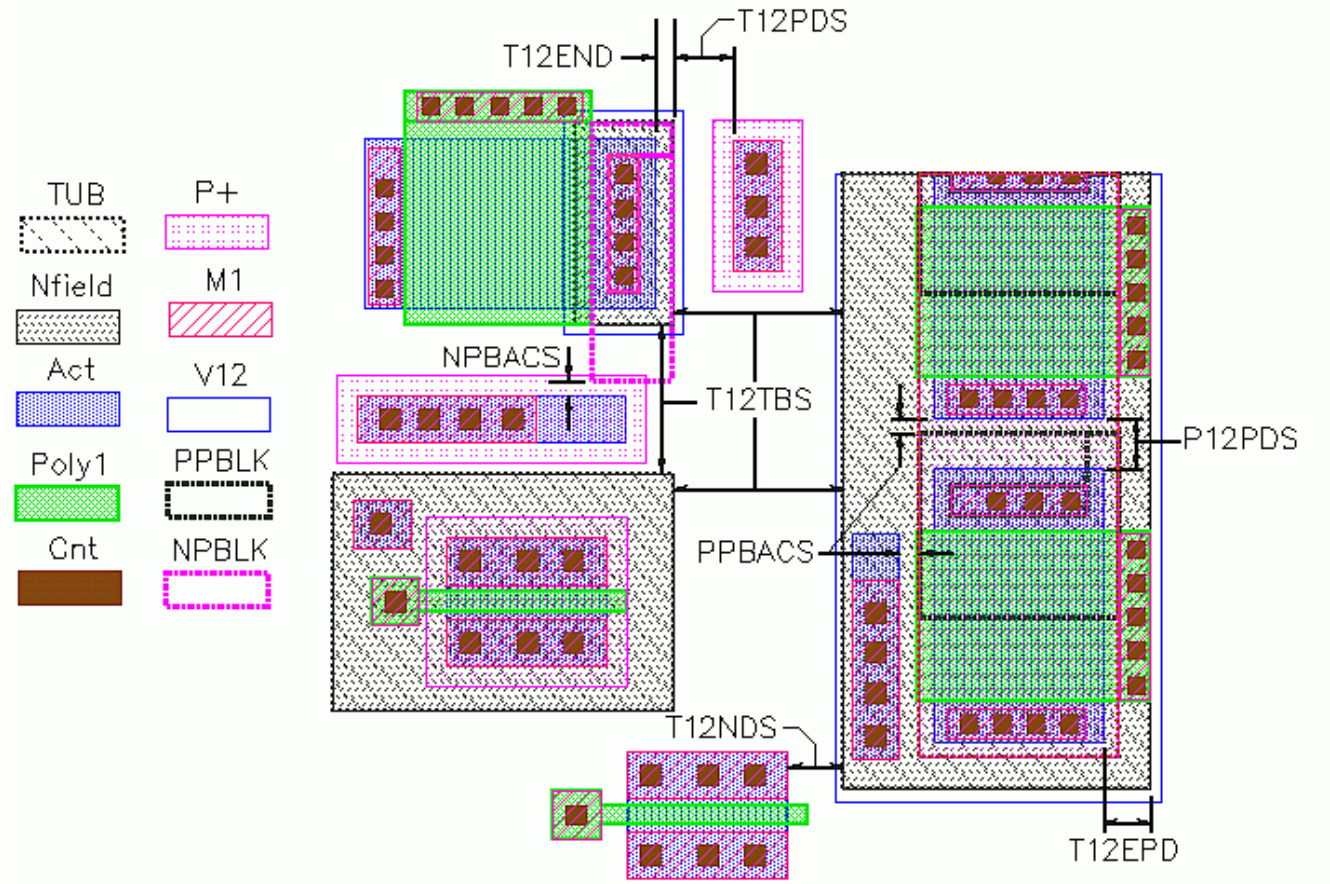
Note 3: PPBLK blocks the P+ implant but not the P-LDD implant from Active and Poly. PPBLK supersedes P+ drawn.

Note 4: This device will not be recognized if ThickGate does not cover the active region.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
ACENPD	Man ACtive Enclosure of Nested-P-Drain	0.70	µm	*	
NPDCHW	Min Nested-P-Drain CHannel Width	2.30	µm	*	
NPDEOC	Min Nested-P-Drain Enclosure Of Contact	0.20	µm	*	
NPDGTS	Man Nested-P-Drain to GaTe Spacing	0.70	µm	*	
NPDRNW	Man Nested-P-DRaiN Width	0.90	µm	*	
NPDWEA	Min Nested-P-Drain-Well Enclosure of Active	2.00	µm	*	
PPBEAC	Min PPBlk Enclosure of ACtive	0.30	µm	*	
PVCHL	Min. PV-type nested-drain CHannel-Length	3.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

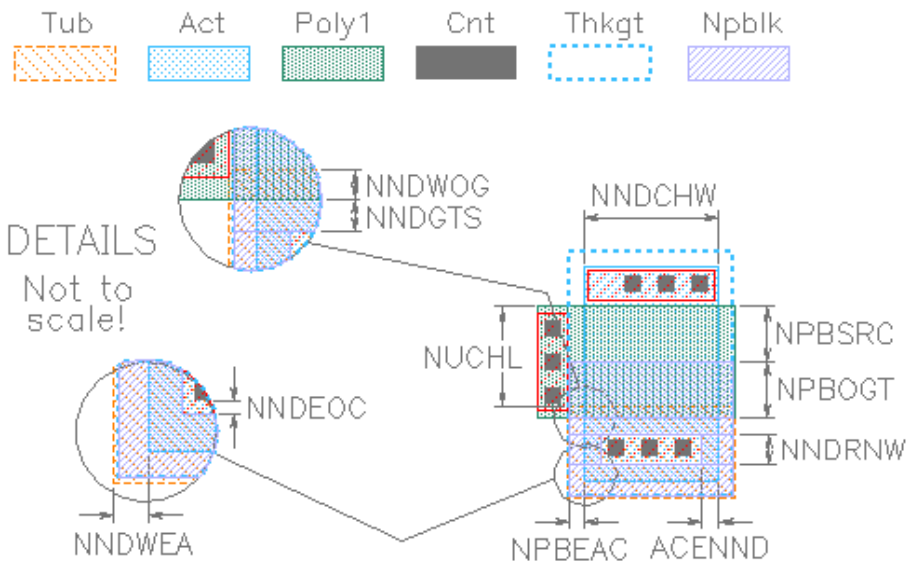
C5X (0.5 Micron) 12V ISOLATION Layout Rules



Rule Name	Rule Description	Rule	Units	Rule Type	Notes
NPBACS	Min NPBlk to ACtive Spacing	0.30	µm	*	
P12PDS	Min P-act-12v to P-Diffusion Spacing	2.00	µm	*	P-Act-12v is defined as active - AND - PPBLK
PPBACS	Min PPBlk to ACtive Spacing	0.30	µm	*	
T12END	Tub-12v Enclosure of N-Diffusion	0.50	µm	*	
T12EPD	Tub-12v Enclosure of P-Diffusion	2.00	µm	*	
T12NDS	Tub-12v to N-Diffusion Spacing	2.00	µm	*	
T12PDS	Tub-12v to P-Diffusion Spacing	0.50	µm	*	
T12TBS	Tub-12v to TuB Spacing	6.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) 12V SINGLE SIDED NESTED-DRAIN NCH Layout Rules



Note 1: Nested-N-Drain is the active region of an N-Ch Nested-Drain Transistor that is not covered by N+Blk mask. This region gets both the N-LDD and N+ implants.

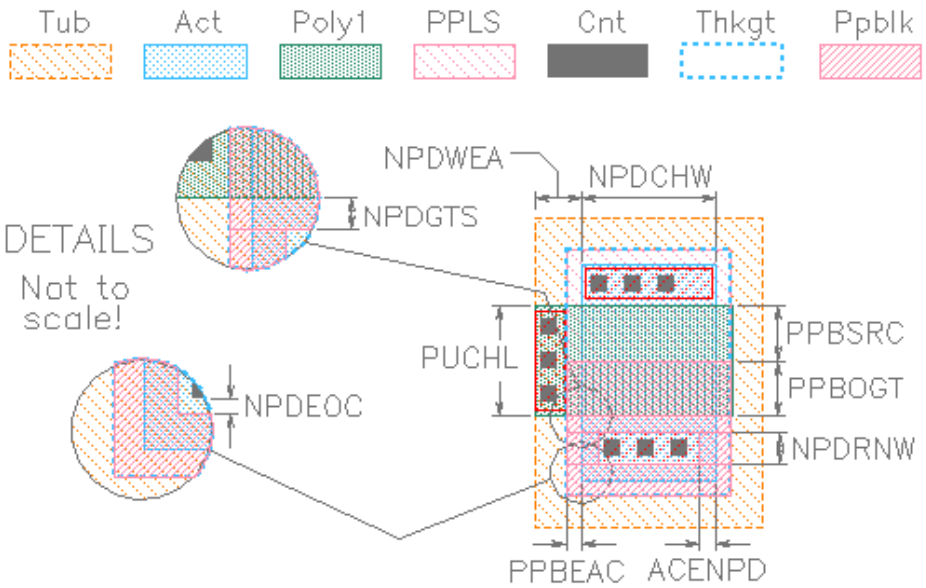
Note 2: Nested-N-Drain-Well is the well region below the Drain of a NCh Nested-Drain. For Single-Sided NCh-Nested Drain, the channel region of the device starts from the N-Well Edge on the Drain side of the device and ends at the poly edge on the Source side.

Note 3: NPBLK blocks the N+ implant but not the N-LDD implant from Active and Poly. NPBLK supersedes N+ drawn.

Note 4: This device will not be recognized if ThickGate does not cover the active region.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
ACENND	Man ACtive Enclosure of Nested-N-Drain	0.50	µm	*	
NNDCHW	Min Nested-N-Drain-CHannel Width	4.00	µm	*	
NNDEOC	Min Nested-N-Drain Enclosure Of Contact	0.20	µm	*	
NNDGTS	Man Nested-N-Drain to Gate Spacing	0.50	µm	*	
NNDRNW	Man Nested-N-DRaiN Width	0.90	µm	*	
NNDWEA	Man Nested-N-Drain-Well Enclosure of Active	0.50	µm	*	
NNDWOG	Man Nested-N-Drain-Well Overlap of Gate	0.50	µm	*	
NPBEAC	Min NPBlk Enclosure of ACtive	0.30	µm	*	
NPBOGT	Min NPBlk Overlap of GaTe	1.50	µm	*	
NPBSRC	Min NPBlk to SourRCe spacing	1.50	µm	*	
NUCHL	Min NU-type nested-drain CHannel Length	3.00	µm	*	

C5X (0.5 Micron) 12V SINGLE SIDED NESTED-DRAIN PCH Layout Rules



Note 1: Nested-P-Drain is the active region of an P-Ch Nested-Drain Transistor that is not covered by P+Blk mask. This region gets both the P-LDD and P+ implants.

Note 2: PPBLK blocks the P+ implant but not the P-LDD implant from Active and Poly. PPBLK supersedes P+ drawn.

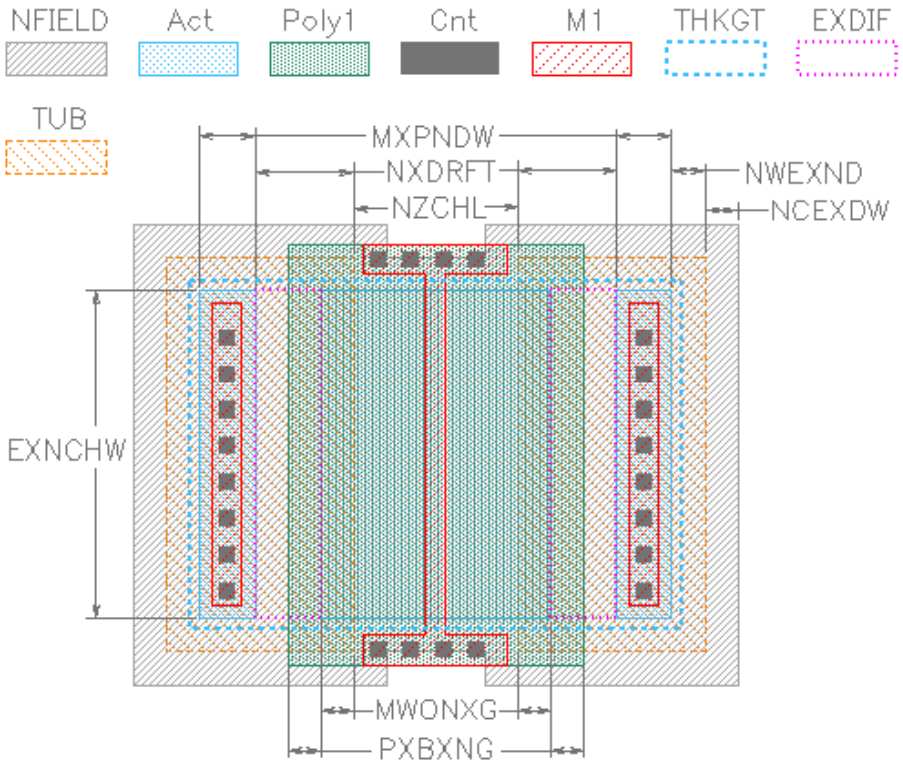
Note 3: This device will not be recognized if ThickGate does not cover the active region.

Note 4: Nested-P-Drain-Well is the N-Well under the PCh Nested-Drain device.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
ACENPD	Man ACtive Enclosure of Nested-P-Drain	0.70	µm	*	
NPDCHW	Min Nested-P-Drain CHannel Width	2.30	µm	*	
NPDEOC	Min Nested-P-Drain Enclosure Of Contact	0.20	µm	*	
NPDGTS	Man Nested-P-Drain to GaTe Spacing	0.70	µm	*	
NPDRNW	Man Nested-P-DRaiN Width	0.90	µm	*	
NPDWEA	Min Nested-P-Drain-Well Enclosure of Active	2.00	µm	*	
PPBEAC	Min PPBlk Enclosure of ACtive	0.30	µm	*	
PPBOGT	Min PPBlk Overlap of GaTe	1.50	µm	*	
PPBSRC	Min PPBlk to SouRCe spacing	1.50	µm	*	
PUCHL	Min PU-type nested-drain CHannel Length	3.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) 15/15V EXT-DRAIN DOUBLE SIDED NCH Layout Rules



Note 1: When Extended-Drain Devices are used both N-Well and NCh-Fld Must be drawn.

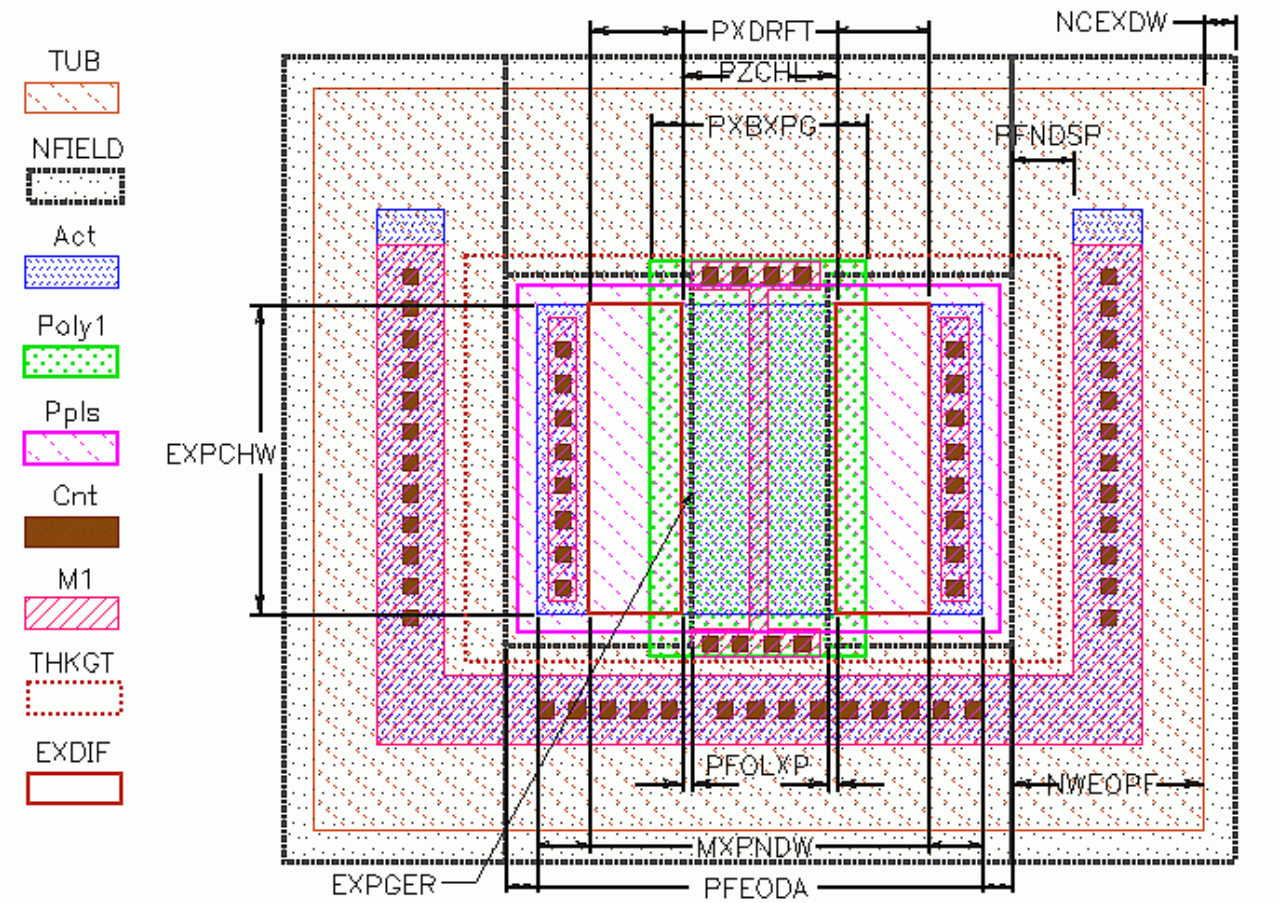
Note 2: This device will not be recognized if ThickGate does not cover the active region.

Note 3: EXDIF level 41 is used to fill the gap between source and drain active areas used in forming Extended-Drain Devices. This allows verification software to recognize separate s/d active areas as one Extended-Drain Device.

Note 4: For operating temperature greater than 70 degree C limit the gate to well operating voltage to 13.2V.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
EXNCHW	Min EXtended-N-drain CHannel Width	5.00	µm	*	
MWONXG	Man Well Overlaps NX-type Gate	0.50	µm	*	
MXPNDW	Man eXtended-P/N-Drain active Width	1.10	µm	*	
NCEXDW	Man N-Chan-field Enclosure of eXtended-Drain-Well	0.50	µm	*	
NWEXND	Min NWell Enclosure of eXtended-N-Drain region	1.00	µm	*	
NZCHL	Min NZ-type extended-drain CHannel Length	5.00	µm	*	
NZDRFT	Man NZ-type extended-drain DRiFT region length	3.00	µm	*	
PXBXNG	Min Poly eXtends Beyond eXtended-N-Gate	1.00	µm	*	

C5X (0.5 Micron) 15/15V EXT-DRAIN DOUBLE SIDED PCH Layout Rules



Note 1: P-Field is any region not(active) where N-Well is drawn and NCh-Fld is not drawn.

Note 2: When Extended-Drain Devices are used both N-Well and NCh-Fld Must be drawn.

Note 3: This device will not be recognized if ThickGate does not cover the active region.

Note 4: EXDIF level 41 is used to fill the gap between source and drain active areas used in forming Extended-Drain Devices. This allows verification software to recognize separate s/d active areas as one Extended-Drain Device.

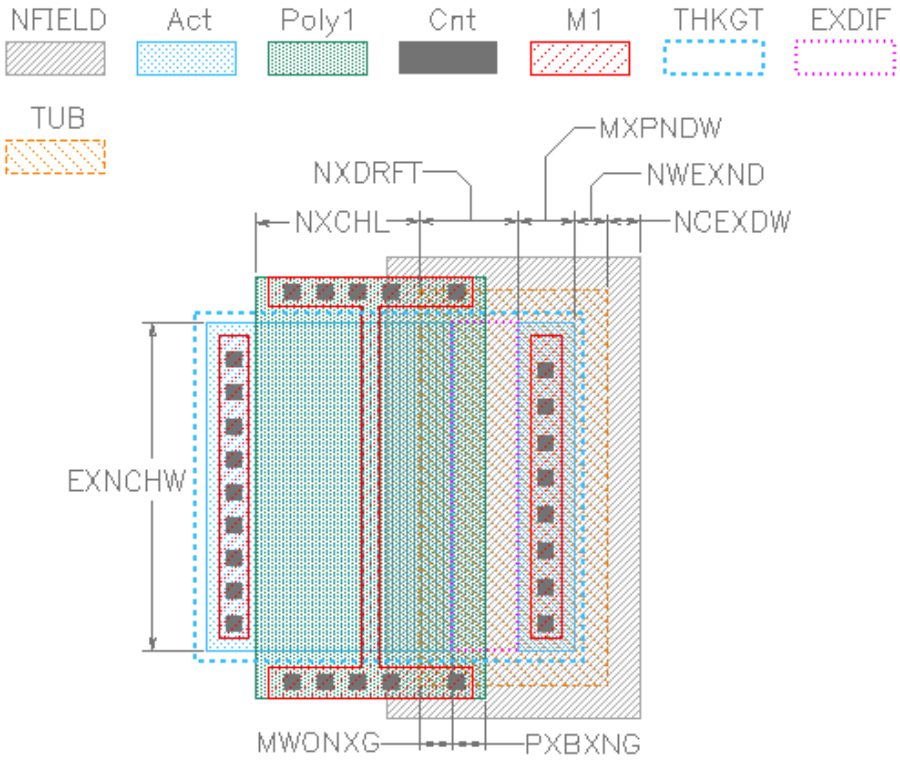
Note 5: For operating temperature greater than 70 degree C limit the gate to well operating voltage to 13.2V.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
EXPCHW	Min EXtended-P-drain CHannel Width	5.00	µm	*	
EXPGER	Extended P gate requires pfield			*	
MXPNDW	Man eXtended-P/N-Drain active Width	1.10	µm	*	
NCEXDW	Man N-Chan-field Enclosure of eXtended-Drain-Well	0.50	µm	*	

NWEOPF	Min NWell Enclosure Of PField	3.00	µm	*	
PFEODA	Min PField Enclosure of ext-Drain-Active	1.00	µm	*	
PFNDSP	Min P-Field to NDiff SPacing	1.00	µm	*	
PFOLXP	Man P-Field OverLap of eXtended-P-gate	0.30	µm	*	
PXBXPG	Min Poly eXtends Beyond eXtended-P-Gate	1.00	µm	*	
PZCHL	Min PZ-type extended-drain CHannel Length	5.00	µm	*	
PZDRFT	Man PZ-type extended-drain DRiFT region length	3.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) 15/20V EXT-DRAIN SINGLE SIDED NCH Layout Rules



Note 1: When Extended-Drain Devices are used both N-Well and NCh-Fld Must be drawn.

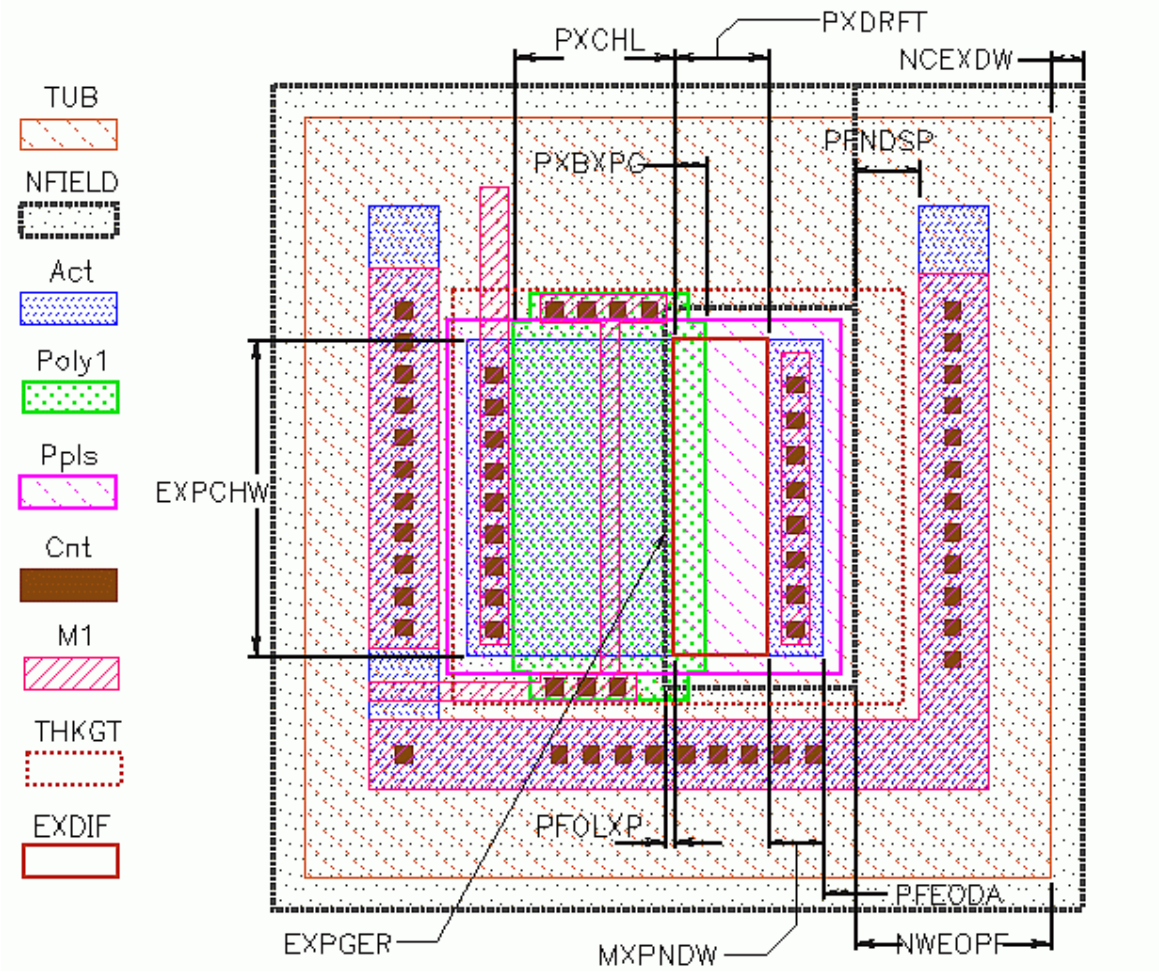
Note 2: This device will be recognized as a 5/20V Devices if ThickGate does not cover the active region.

Note 3: EXDIF level 41 is used to fill the gap between source and drain active areas used in forming Extended-Drain Devices. This allows verification software to recognize separate s/d active areas as one Extended-Drain Device.

Note 4: For operating temperature greater than 70 degree C limit the gate to well operating voltage to 13.2V.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
EXNCHW	Min EXtended-N-drain CHannel Width	5.00	µm	*	
MWONXG	Man Well Overlaps NX-type Gate	0.50	µm	*	
MXPNDW	Man eXtended-P/N-Drain active Width	1.10	µm	*	
NCEXDW	Man N-Chan-field Enclosure of eXtended-Drain-Well	0.50	µm	*	
NWEXND	Min NWell Enclosure of eXtended-N-Drain region	1.00	µm	*	
NXCHL	Min NX-type extended-drain CHannel Length	5.00	µm	*	
NXDRFT	Man NX-type extended-drain DRiFT region length	3.00	µm	*	
PXBXNG	Min Poly eXtends Beyond eXtended-N-Gate	1.00	µm	*	

C5X (0.5 Micron) 15/20V EXT-DRAIN SINGLE SIDED PCH Layout Rules



Note 1: P-Field is any region not(active) where N-Well is drawn and NCh-Fld is not drawn.

Note 2: This device will be recognized as a 5/20V Devices if ThickGate does not cover the active region.

Note 3: When Extended-Drain Devices are used both N-Well and NCh-Fld Must be drawn.

Note 4: EXDIF level 41 is used to fill the gap between source and drain active areas used in forming Extended-Drain Devices. This allows verification software to recognize separate s/d active areas as one Extended-Drain Device.

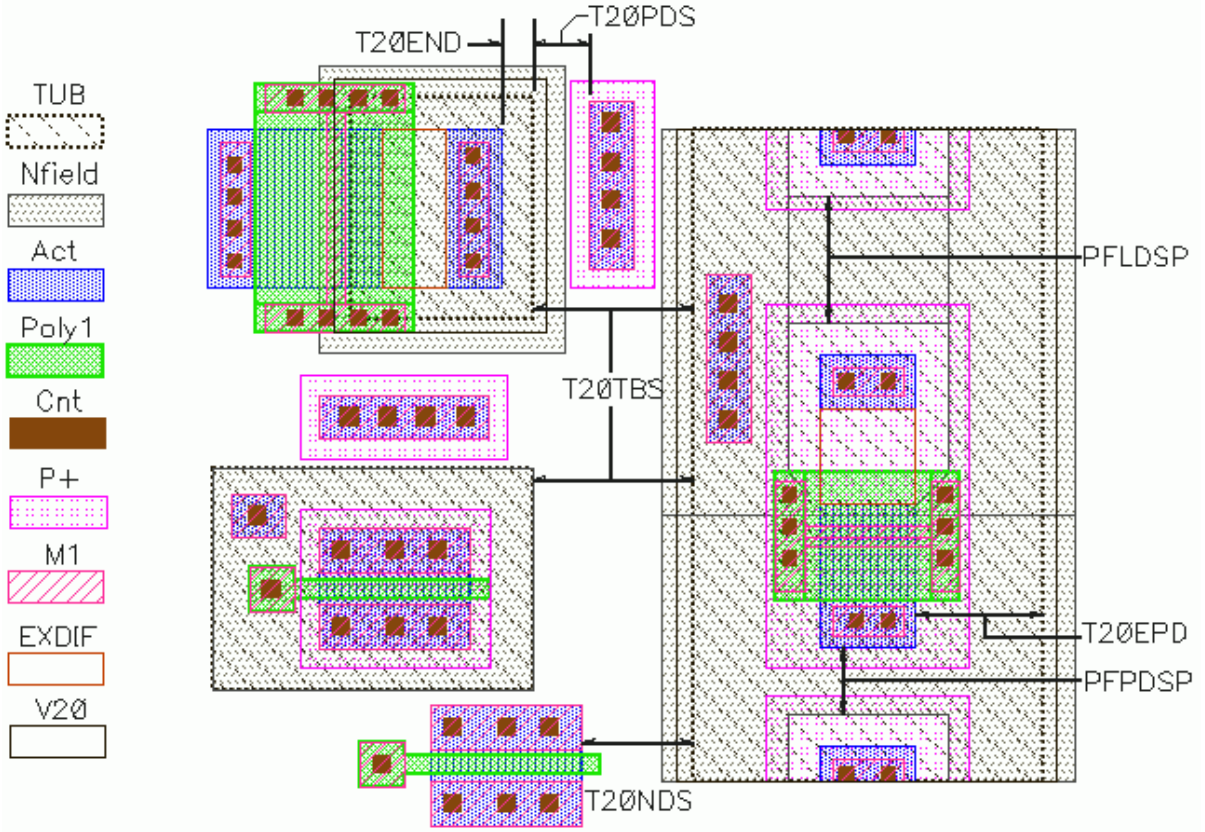
Note 5: For operating temperature greater than 70 degree C limit the gate to well operating voltage to 13.2V.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
EXPCHW	Min EXtended-P-drain CHannel Width	5.00	µm	*	
EXPGER	Extended P gate requires pfield			*	
MXPNDW	Man eXtended-P/N-Drain active Width	1.10	µm	*	

NCEXDW	Man N-Chan-field Enclosure of eXtended-Drain-Well	0.50	µm	*	
NWEOPF	Min NWell Enclosure Of PField	3.00	µm	*	
PFEODA	Min PField Enclosure of ext-Drain-Active	1.00	µm	*	
PFNDSP	Min P-Field to NDiff SPacing	1.00	µm	*	
PFOLXP	Man P-Field OverLap of eXtended-P-gate	0.30	µm	*	
PXBXPG	Min Poly eXtends Beyond eXtended-P-Gate	1.00	µm	*	
PXCHL	Min PX-type extended-drain CHannel Length	5.00	µm	*	
PXDRFT	Man PX-type extended-drain DRiFT region length	3.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) 20V ISOLATION Layout Rules

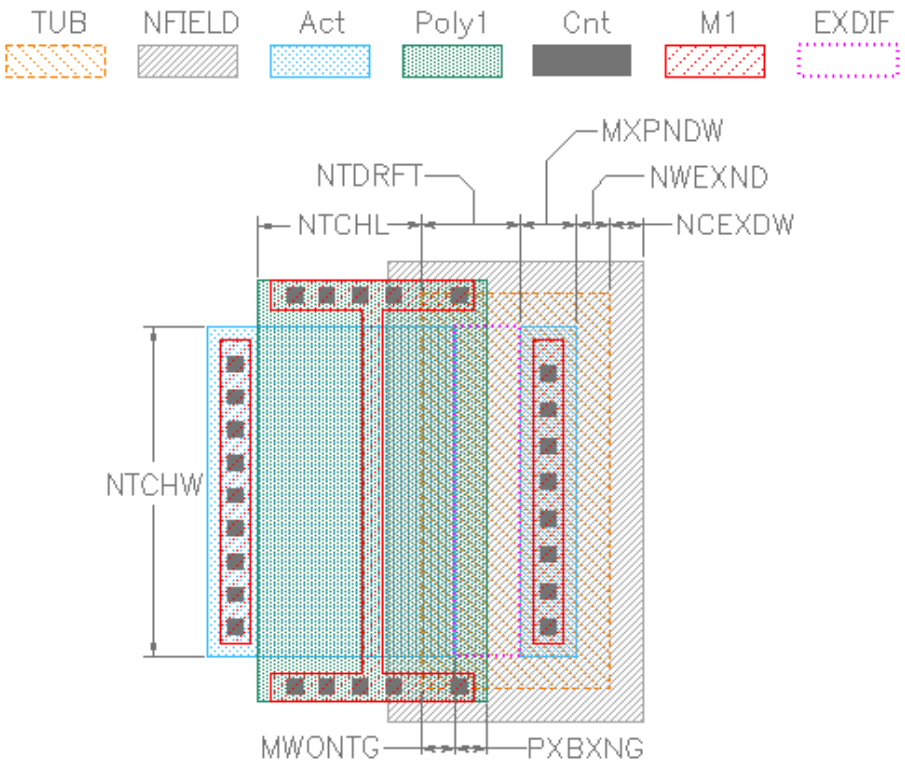


Note 1: P-Field is any region not(active) where N-Well is drawn and NCh-Fld is not drawn.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
PFLDSP	Min P-FieLD to P-FieLD SPacing	4.00	µm	*	
PFPDSP	Min P-Field to PDiffusion SPacing	3.00	µm	*	
T20END	Tub-20v Enclosure Of N-Diffusion	1.00	µm	*	
T20EPD	Tub-20v Enclosure Of P-Diffusion	3.00	µm	*	
T20NDS	Tub-20v to N-Diffusion Spacing	3.00	µm	*	
T20PDS	Tub-20v to P-Diffusion Spacing	1.00	µm	*	
T20TBS	Tub-20v to TuB Spacing	6.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) 5/20V EXT-DRAIN NCH Layout Rules

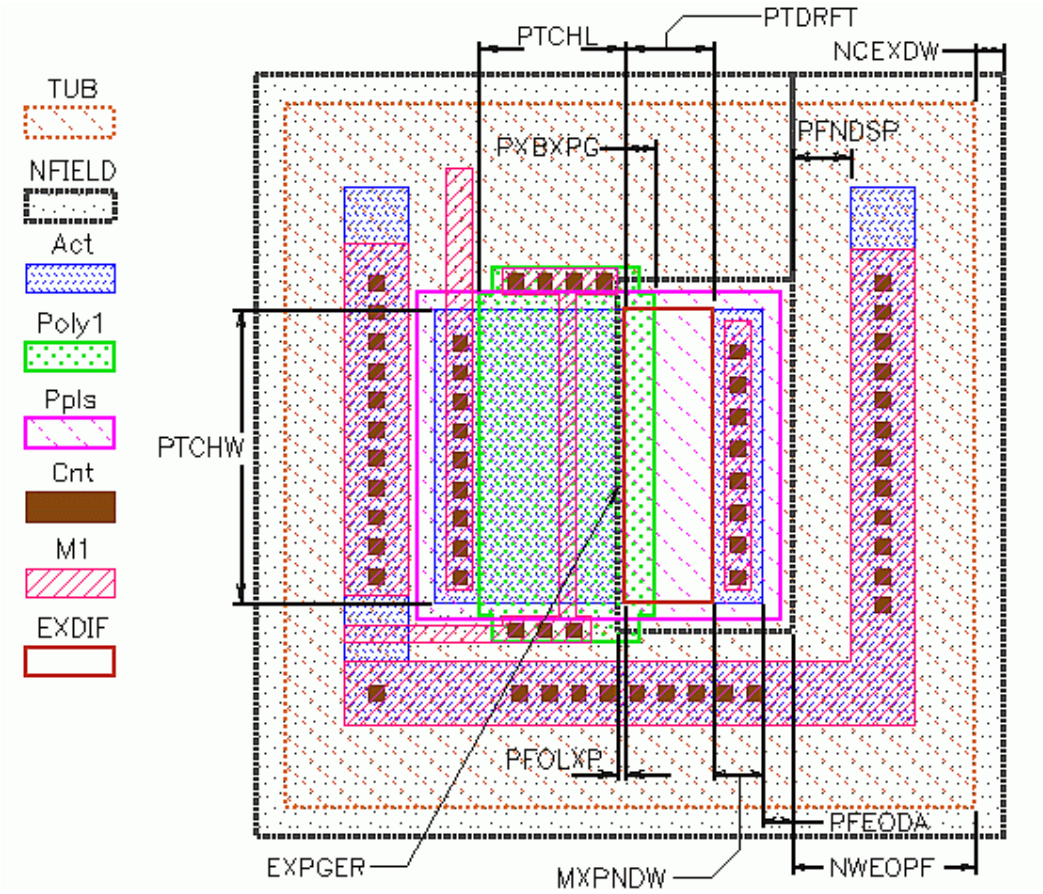


Note 1: When Extended-Drain Devices are used both N-Well and NCh-Fld Must be drawn.

Note 2: EXDIF level 41 is used to fill the gap between source and drain active areas used in forming Extended-Drain Devices. This allows verification software to recognize separate s/d active areas as one Extended-Drain Device.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
MWONTG	Man Well Overlaps NT-type Gate	0.50	µm	*	
MXPNDW	Man eXtended-P/N-Drain active Width	1.10	µm	*	
NCEXDW	Man N-Chan-field Enclosure of eXtended-Drain-Well	0.50	µm	*	
NTCHL	Min NT-type extended-drain CHannel Length	5.00	µm	*	
NTCHW	Min NT-type extended-drain CHannel Width	5.00	µm	*	
NTDRFT	Man NT-type ext-drain DRiFT region length for model accuracy only	3.00	µm	*	
NWEXND	Min NWell Enclosure of eXtended-N-Drain region	1.00	µm	*	
PXBXNG	Min Poly eXtends Beyond eXtended-N-Gate	1.00	µm	*	

C5X (0.5 Micron) 5/20V EXT-DRAIN PCH Layout Rules



Note 1: P-Field is any region not(active) where N-Well is drawn and NCh-Fld is not drawn.

Note 2: When Extended-Drain Devices are used both N-Well and NCh-Fld Must be drawn.

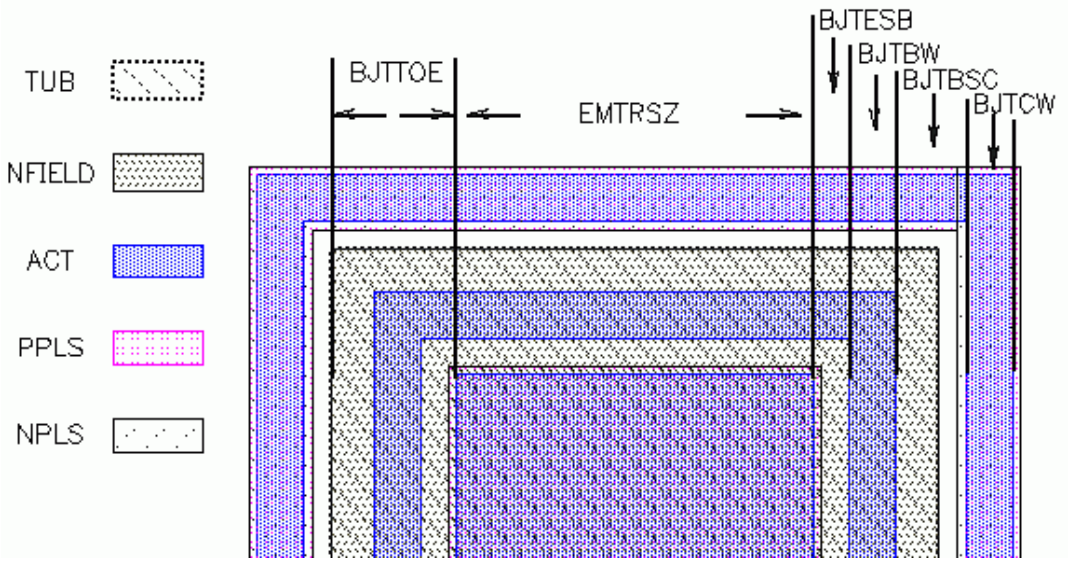
Note 3: EXDIF level 41 is used to fill the gap between source and drain active areas used in forming Extended-Drain Devices. This allows verification software to recognize separate s/d active areas as one Extended-Drain Device.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
EXPGER	Extended P gate requires pfield			*	
MXPNDW	Man eXtended-P/N-Drain active Width	1.10	µm	*	
NCEXDW	Man N-Chan-field Enclosure of eXtended-Drain-Well	0.50	µm	*	
NWEOPF	Min NWell Enclosure Of PField	3.00	µm	*	
PFEODA	Min PField Enclosure of ext-Drain-Active	1.00	µm	*	
PFNDSP	Min P-Field to NDiff SPacing	1.00	µm	*	
PFOLXP	Man P-Field OverLap of eXtended-P-gate	0.30	µm	*	

PTCHL	Min PT-type extended-drain CHannelLength	5.00	µm	*	
PTCHW	Min PT-dev-type extended-drain CHannel Width	5.00	µm	*	
PTDRFT	Man PT-type ext-drain DRiFT region length for model accuracy only	3.00	µm	*	
PXBXPG	Min Poly eXtends Beyond eXtended-P-Gate	1.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) BIPOLAR DEVICES Layout Rules



Note 1: BiPolar Junction Device rules below show 2 model sizes. The graphic representation above is valid for both sizes.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
BJTBSC	Man Base diffusion to Collector diffusion ensures model performance	3.90	µm	*	
BJTBSC_S	Man Base diffusion to Collector diffusion ensures model performance	.90	µm	*	Rule for smaller model size
BJTBW	Man Base diffusion Width ensures model performance	2.60	µm	*	
BJTBW_S	Man Base diffusion Width ensures model performance	1.10	µm	*	Rule for smaller model size
BJTCW	Min Collector diffusion Width	1.10	µm	*	
BJTESB	Man Emitter diffusion to Base diffusion ensures model performance	2.00	µm	*	
BJTESB_S	Man Emitter diffusion to Base diffusion ensures model performance	.90	µm	*	Rule for smaller model size
BJTTOE	Man Tub Overlap to Emitter diffusion ensures model performance	7.00	µm	*	
BJTTOE_S	Man Tub Overlap to Emitter diffusion ensures model performance	2.50	µm	*	Rule for smaller model size
EMTRSZ	Man Emitter diffusion Size ensures model performance	20.00	µm	*	Size=20x20 Area=400
EMTRSZ_S	Man Emitter diffusion Size ensures model performance	4.10	µm	*	Rule for smaller model size. Size=4.1x4.1 Area=16.81

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) EXTERNAL CONNECTION Layout Rules

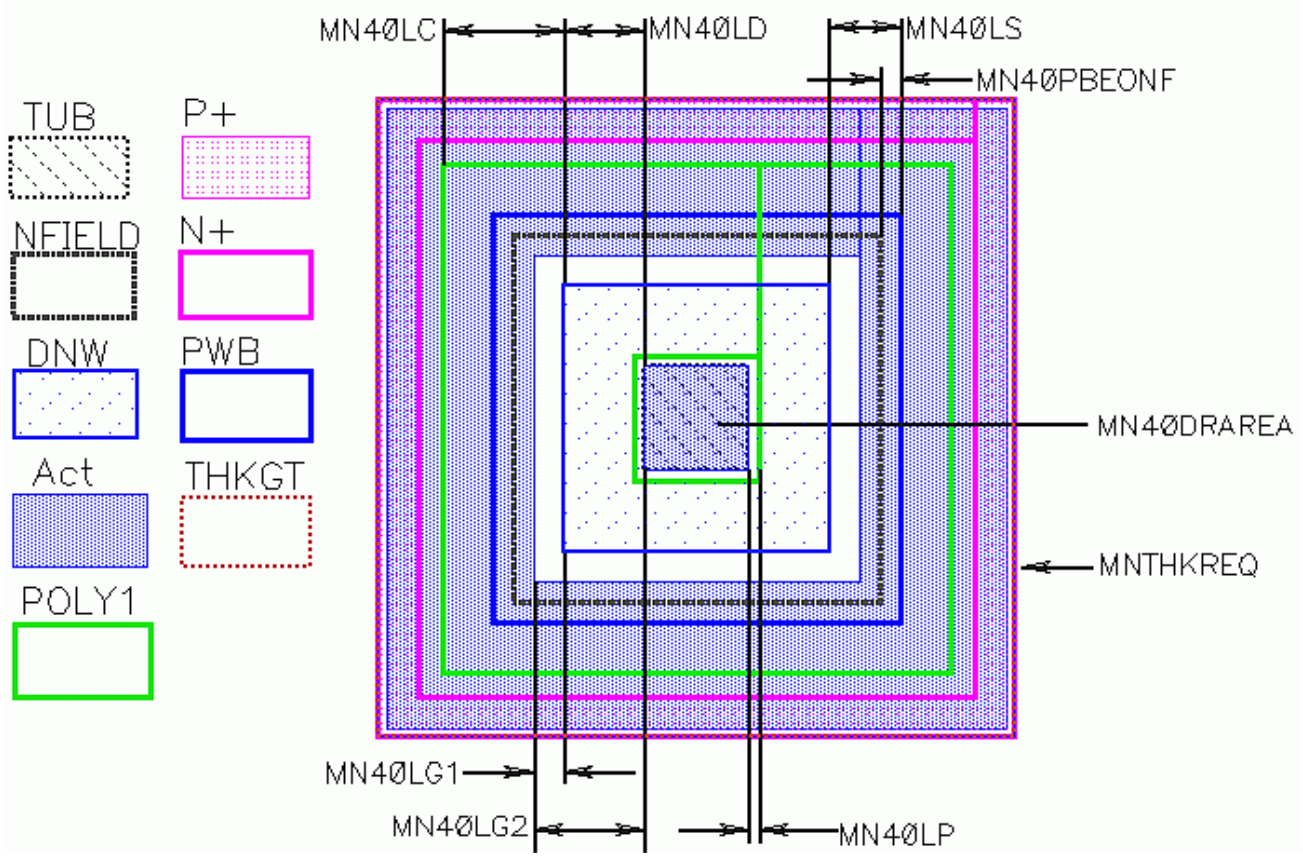
Note 1:
1) The AMI C5x digital I/O pad libraries have been drawn to these rules. ESD performance is dependent on chip layout and cell layout, so no specific level of ESD tolerance is guaranteed.
2) DRC rules can be made available that will not check these rules.

Note 2: All EC rules apply to Drain

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
EACEOC	EC ACtive Enclosure of Contact	2.00	µm	**	These are guidelines only and do not guarantee any particular level of ESD protection!
EACEOT	EC ACtive Overlap of Tub toward gate	1.50	µm	**	These are guidelines only and do not guarantee any particular level of ESD protection!
EACX	EC ACtive Spacing	1.20	µm	**	These are guidelines only and do not guarantee any particular level of ESD protection!
EDRCNT	Drain requires double row contact			**	These are guidelines only and do not guarantee any particular level of ESD protection!
ENCTGX	EC N-device drain Contact To Gate Spacing	6.20	µm	**	These are guidelines only and do not guarantee any particular level of ESD protection!
ENWUCT	EC NWell required under drain Contacts			**	These are guidelines only and do not guarantee any particular level of ESD protection!
EPCTGX	EC P-device drain Contact To Gate Spacing	4.60	µm	**	These are guidelines only and do not guarantee any particular level of ESD protection!
ESCTGX	EC Source Contact To Gate Spacing	1.90	µm	**	These are guidelines only and do not guarantee any particular level of ESD protection!
ETBEOC	EC NTuB Enclosure of Contact	1.00	µm	**	These are guidelines only and do not guarantee any particular level of ESD protection!
ETBGAX	EC TuB to GAte Spacing	1.50	µm	**	These are guidelines only and do not guarantee any particular level of ESD protection!

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

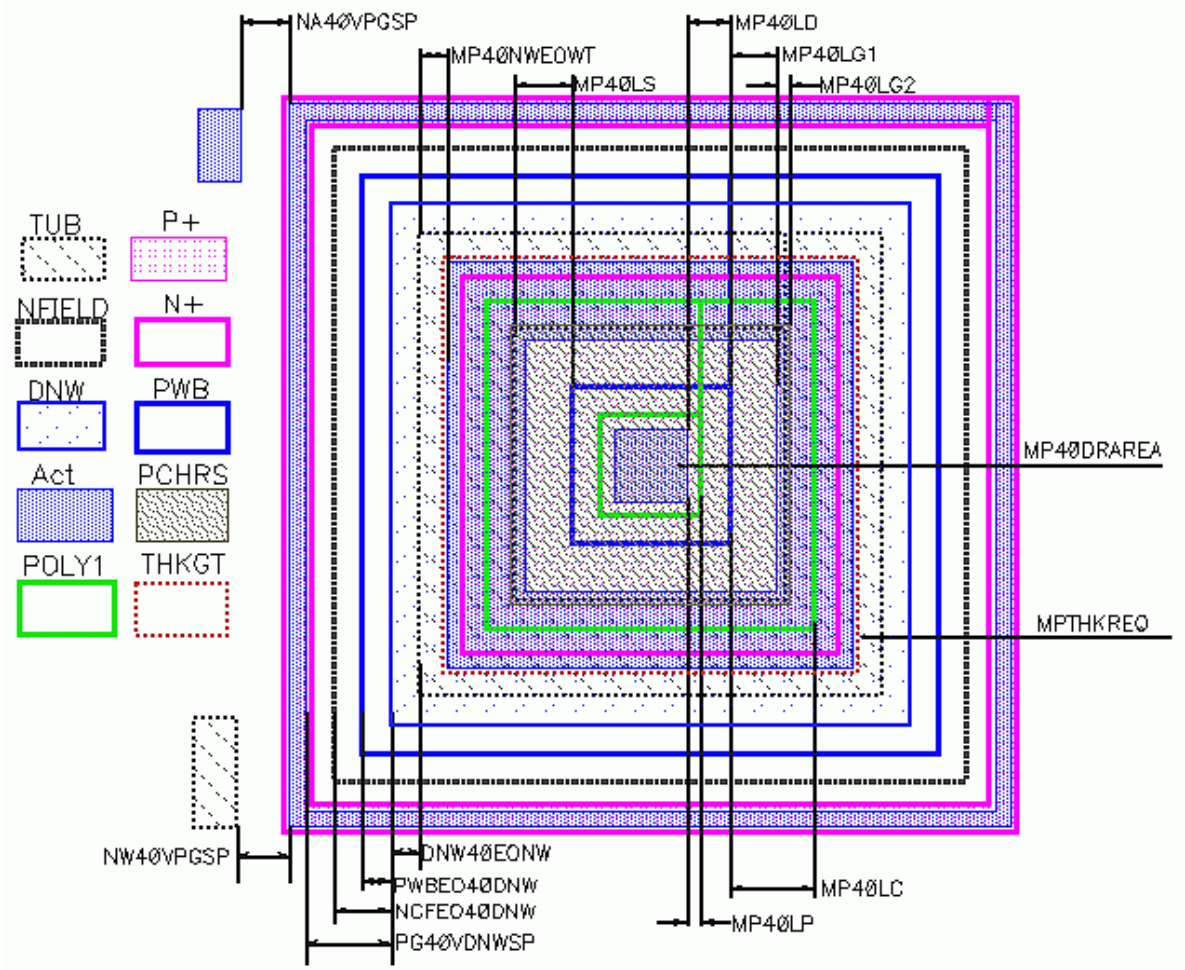
C5X (0.5 Micron) N40VTILE Layout Rules



Note 1: 40 Volt Nets can ONLY be connected to the drain of either 40V NMOS, the source of a 40V PMOS or the NWell of a 40V PMOS. All 40 Volt Nets must not be routed in Poly or Metal 1.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
MN40DRAREA	N-device Drain Area-Mandatory	26.01	µm²	*	Mandatory
MN40LC	Poly enclosure of Deep N Well towards source-Mandatory	6.0	µm	*	Mandatory
MN40LD	Deep N Well enclosure of drain active area-Mandatory	4.0	µm	*	Mandatory
MN40LG1	Deep N Well space of channel active-Mandatory	1.5	µm	*	Mandatory
MN40LG2	N Well space of channel active-Mandatory	5.5	µm	*	Mandatory
MN40LP	Poly space drain-Mandatory	0.5	µm	*	Mandatory
MN40LS	P Well Block enclosure of Deep N Well-Mandatory	3.5	µm	*	Mandatory
MN40PBEONF	P Well Block enclosure of N Channel Field-Mandatory	1.0	µm	*	Mandatory
MNTHKREQ	MN40V THicK gate REQuired-Mandatory			*	Mandatory

C5X (0.5 Micron) P40VTILE Layout Rules



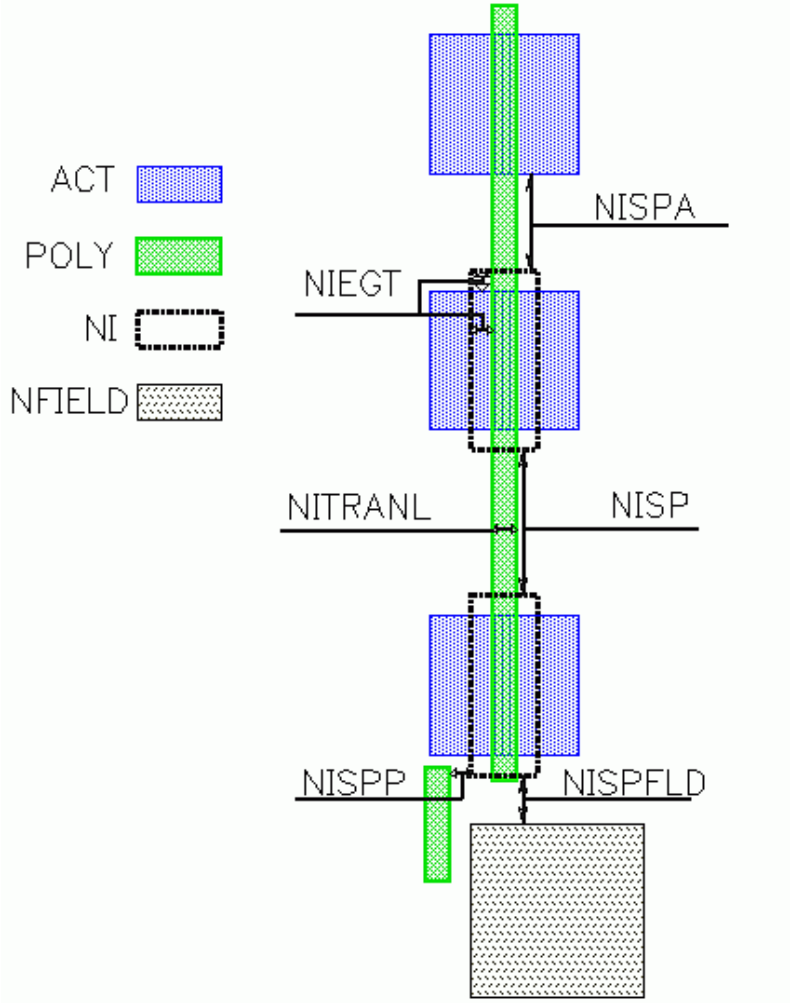
Note 1: 40 Volt Nets can ONLY be connected to the drain of either 40V NMOS, the source of a 40V PMOS or the NWell of a 40V PMOS. All 40 Volt Nets must not be routed in Poly or Metal 1.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
DNW40EONW	40 volt Deep N Well enclosure of N Well-Mandatory	2.0	µm	*	Mandatory
MP40DRAREA	P-device Drain Area-Mandatory	26.01	µm²	*	Mandatory
MP40LC	P Well Block enclosure of source poly edge towards drain-Mandatory	6.0	µm	*	Mandatory
MP40LD	P Well Block space to drain active-Mandatory	3.0	µm	*	Mandatory
MP40LG1	P Well Block Block enclosure of channel active towards drain-Mandatory	3.3	µm	*	Mandatory
MP40LG2	Pch Resurf overlap of channel active-Mandatory	1.0	µm	*	Mandatory
MP40LP	Poly space drain-Mandatory	1.0	µm	*	Mandatory
MP40LS	P Well Block overlap of nwell-	4.0	µm	*	Mandatory

	Mandatory				
MP40NWEOWT	N Well overlap of source-well active WellTie-Mandatory	2.0	µm	*	Mandatory
MPTHKREQ	MP40V THicK gate REQuired-Mandatory			*	Mandatory
NA40VPGSP	N+Active to Hard P+Guardbar of 40 Volt DeepNwell-Minimum	1.0	µm	*	Minimum
NCFEO40DNW	NchannelField overlap 40 Volt DeepNwell-Mandatory	4.0	µm	*	Mandatory
NW40VPGSP	Nwell to Hard P+Guardbar of 40 Volt DeepNwell-Minimum	2.0	µm	*	Minimum
PG40VDNWSP	P+Guardbar to 40 Volt DeepNwell-Mandatory	6.0	µm	*	Mandatory
PWBEO40DNW	PwellBlock overlap 40 Volt DeepNwell-Mandatory	2.0	µm	*	Mandatory

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) NI DEVICE Layout Rules

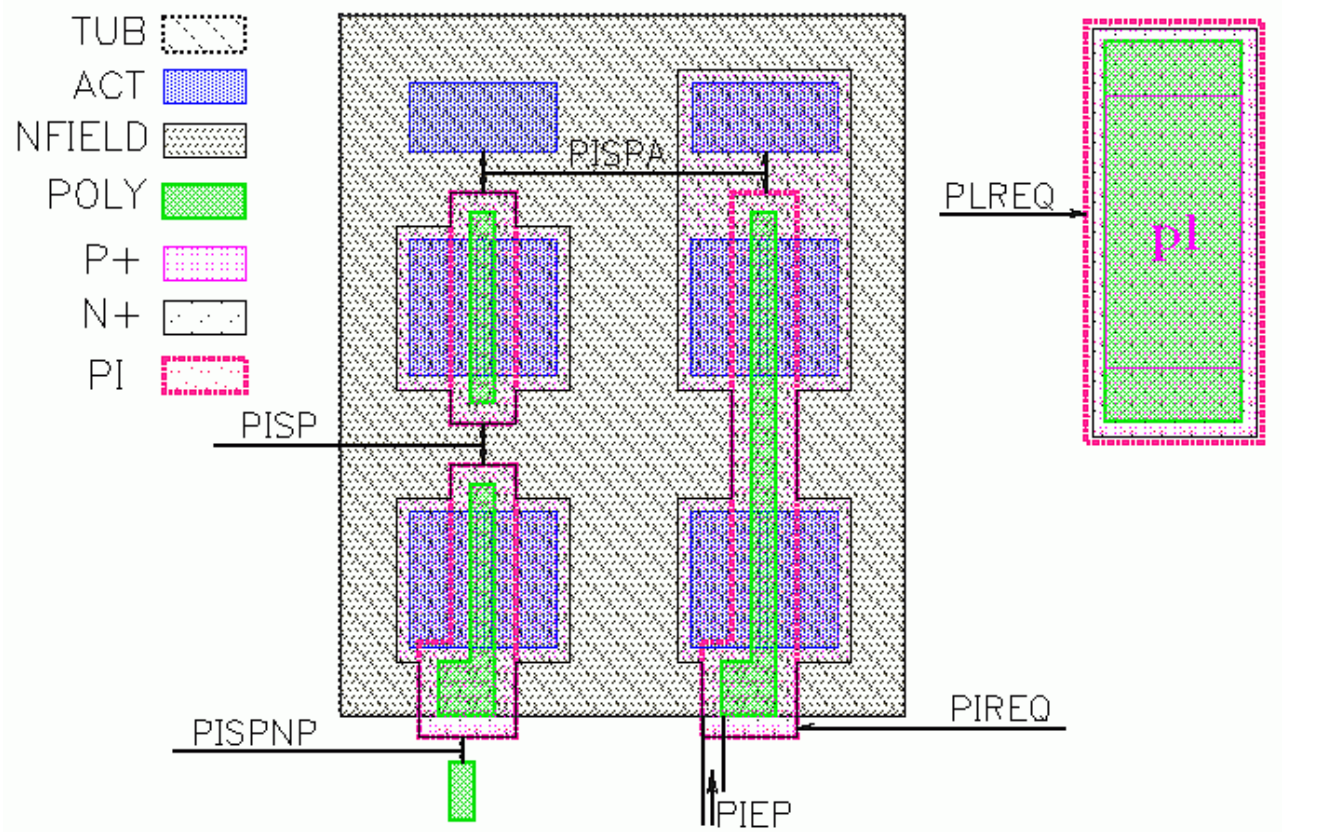


Note 1: N-Field is generated from NI layer by oversizing 0.7 microns.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
NIEGT	Man NI Enclosure of poly GaTe	0.30	µm	*	
NIOPI	NI over PI not allowed			*	
NISP	Min NI SPace	2.10	µm	*	NISP value is to allow adequate N-Field between NI devices.
NISPA	Min NI SPace to Active	1.40	µm	*	
NISPFLD	Min NI SPace to nchan FieLD	0.70	µm	*	
NISPLO	Minimum NI to PLO spacing	0.70	µm	*	
NISPP	Min NI to unrelated Poly	0.30	µm	*	
NITRANL	Min NI TRANSistor Length	0.80	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

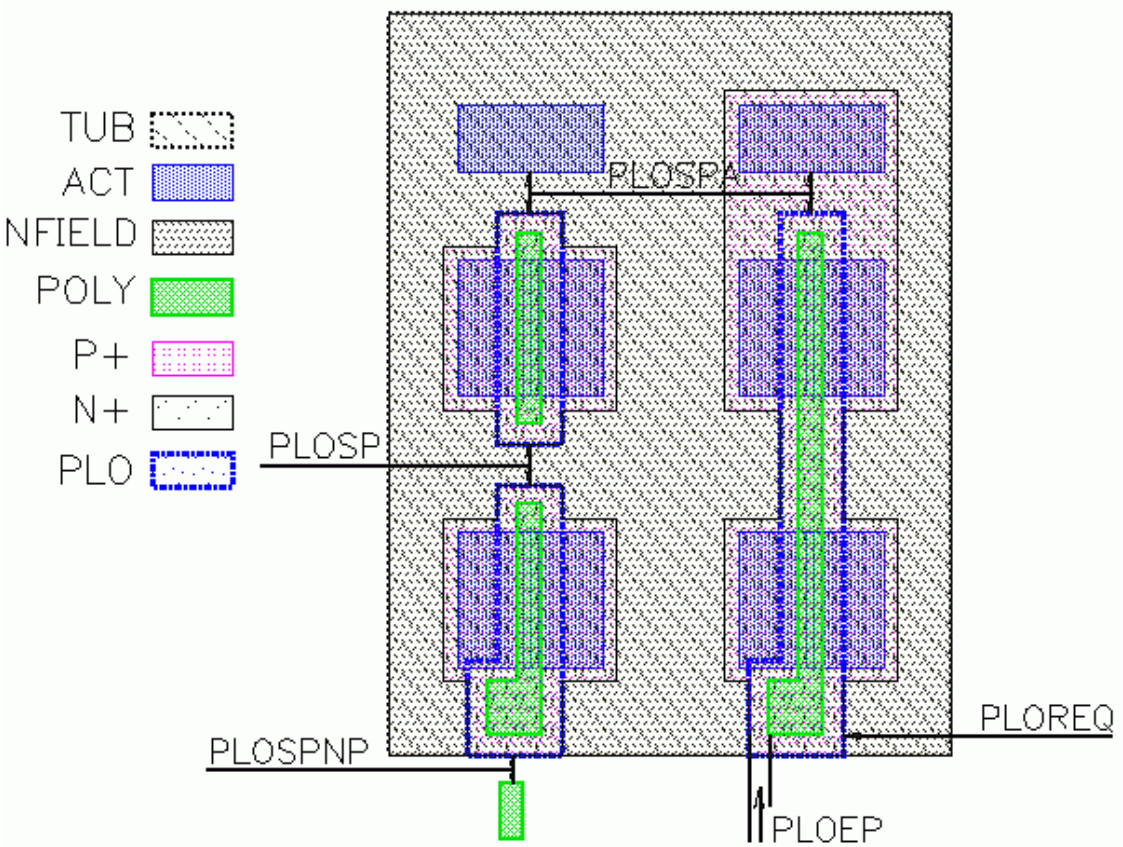
C5X (0.5 Micron) PI DEVICE/PL RESISTOR Layout Rules



Rule Name	Rule Description	Rule	Units	Rule Type	Notes
PIEP	Min PI Enclosure of Poly	0.30	µm	*	Poly cannot cross PI
PIOPLO	PI over PLO not allowed			*	
PIREQ	PI layer must enclose PI Poly			*	
PISNI	Minimum PI to NI spacing	0.70	µm	*	
PISP	Min PI SPace	0.70	µm	*	
PISPA	PI to Active SPace	0.30	µm	*	
PISPNP	Min PI to N+ Poly SPace	0.30	µm	*	
PLREQ	PI layer must enclose PL Resistor Poly			*	PI layer must be drawn to designate poly as PL resistor. PI device rules must be obeyed by PL Resistor. CAUTION: Metal1 to P+poly contact resistance is two orders of magnitude HIGHER than N+poly.

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

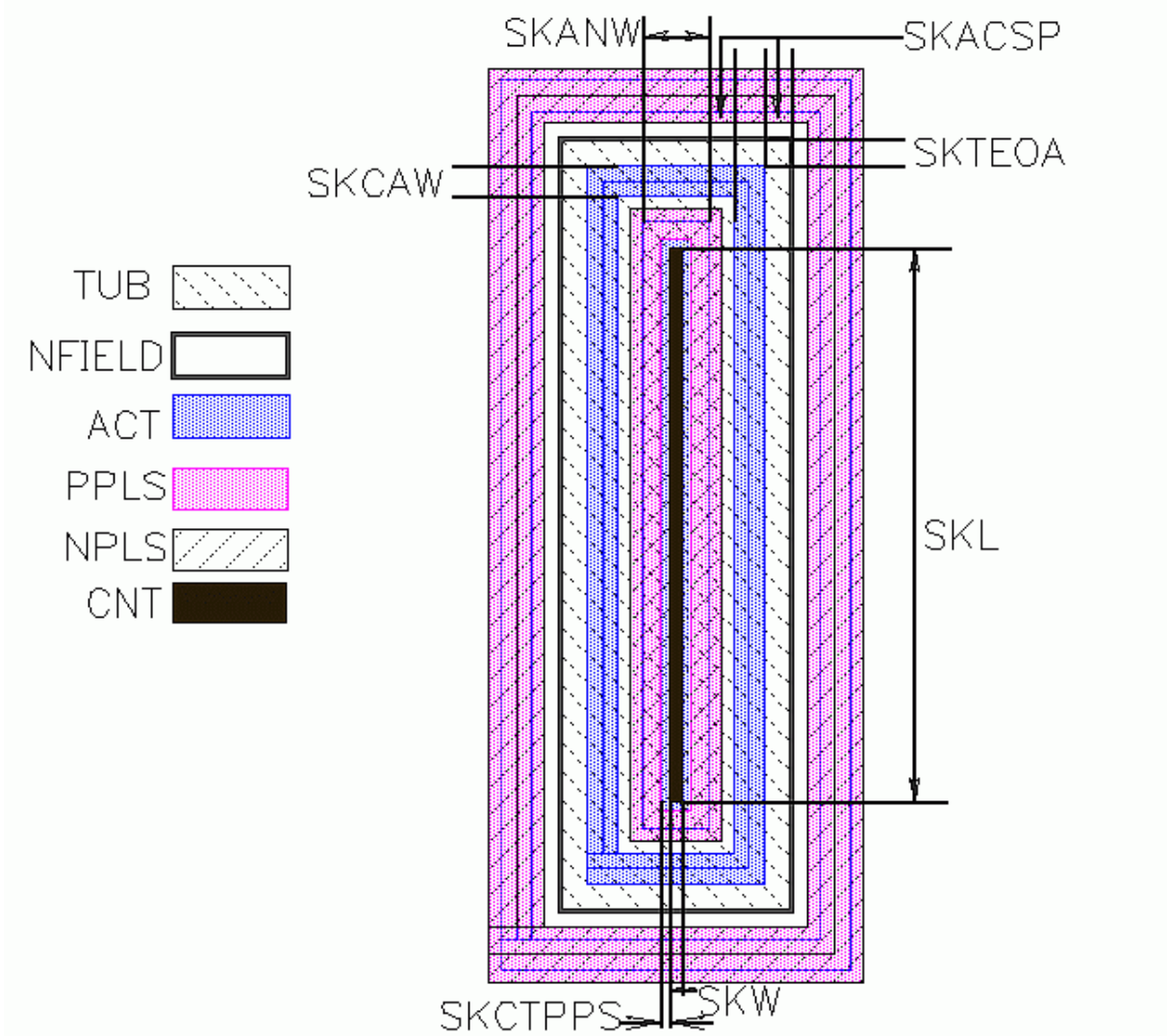
C5X (0.5 Micron) PLO DEVICE Layout Rules



Rule Name	Rule Description	Rule	Units	Rule Type	Notes
PISPLO	Minimum PI to PLO spacing	0.70	µm	*	
PLOEP	Min PLO Enclosure of Poly	0.30	µm	*	Poly cannot cross PLO
PLOONI	PLO over NI not allowed			*	
PLOREQ	PLO layer must enclose PLO Poly			*	
PLOSP	Min PLO SPace	0.70	µm	*	
PLOSPA	PLO to Active SPace	0.30	µm	*	
PLOSPNP	Min PLO to N+ Poly	0.30	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) SCHOTTKY DEVICES Layout Rules



Note 1: Model sensitive to layout design rules! Do not modify!

Note 2: The device layout can be obtained from the Pcell generator or the Schottky1 layout on the 10534 SLM. It is expected that these layouts will pass DRC. However, correct layout is defined by passing the DRC check, not by use of the particular cell.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
NVOSKCT	No nested vias over schottky contact-Mandatory			*	(not shown in graphic above)
SKACSP	Schottky ACtive SPacing-Mandatory	0.90	µm	*	Mandatory
SKANW	Schottky ANode Width-Mandatory	2.40	µm	*	Mandatory
SKCAW	Schottky CAthode Width-Mandatory	1.10	µm	*	Mandatory
SKCTPPS	Schottky ConTact P+ Spacing-Mandatory	0.20	µm	*	Mandatory. Schottky contact to P+ Spacing
SKL	Schottky contact Length-Mandatory	20.20	µm	*	Mandatory

SKRP2	Schottky requires Poly 2 process-Mandatory			*	(not shown in graphic above)
SKTEOA	Schottky Tub Enclosure Of Active-Mandatory	1.00	µm	*	Mandatory. Tub enclosure of the cathode ring
SKW	Schottky contact Width-Mandatory	0.70	µm	*	Mandatory

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C5X (0.5 Micron) Design Rules

Electromigration Rules

AMIS 4500099 Rev: T, 18-May-2005

AMIS Confidential

C5X (0.5 Micron) Metal Interconnects

Note: All electromigration design rules are based on 10 year life expentancy for DC operation.

Rule Description	85 Deg C	125 Deg C
Metal 1 allowed current density per width	2.2 mA/µm	0.85 mA/µm
Metal 2 allowed current density per width	2.2 mA/µm	0.85 mA/µm
Metal 3 allowed current density per width	2.2 mA/µm	0.85 mA/µm

C5X (0.5 Micron) Contacts & Vias

Note: All electromigration design rules are based on 10 year life expentancy for DC operation.

Rule Description	85 Deg C	125 Deg C
0.6µm x 0.6µm Via 1 allowed current density	1.6 mA/cnt	0.6 mA/cnt
0.6µm x 0.6µm Via 2 allowed current density	1.6 mA/cnt	0.6 mA/cnt
0.6µm x 0.6µm contact allowed current density	1.6 mA/cnt	0.6 mA/cnt

C5X (0.5 Micron) Design Rules

Parametric Specs

AMIS 4500099 Rev: T, 18-May-2005

AMIS Confidential

C5X (0.5 Micron) 12V Double Sided Nested-Drain NCh Electrical Parameters

Note: Maximum allowable operating voltage is 13.2V on drain, gate and source. This is the NV device in the model file.

Structure	Test	Min	Typ	Max	Units	Notes
N20x5ND	BVDSS	14	19	-	V	#13
N20x20ND	Gamma	0.8	1.0	1.2	sqrt(V)	#7
N20x5ND	Idsat	5	6	7	mA	#9
N20x20ND	KPrime_l	55	65	75	uA/V2	#4
N20x5ND	Lkg_13.2	-	-	0.5	nA/um	#23
N20x5ND	Vt	0.8	1.0	1.2	V	#3
NCAP_Thk	tox	260	290	320	angs	#1

C5X (0.5 Micron) 12V Double Sided Nested-Drain PCh Electrical Parameters

Note: Maximum allowable operating voltage is -13.2V on drain, gate and source, relative to N-Well. This is the PV device in the model file.

Structure	Test	Min	Typ	Max	Units	Notes
P20x3_ND	BVDSS	-	-14.5	-14.0	V	#13
P20x20_ND	Gamma	0.8	1.1	1.3	sqrt(V)	#7
P20x3_ND	Idsat	-2.7	-2.2	-1.7	mA	#9
P20x20_ND	KPrime_l	15	19	23	uA/V2	#4
P20x3_ND	Lkg_13.2	-0.5	-	-	nA/um	#23
P20x3_ND	Vt	-1.95	-1.65	-1.45	V	#3
PCAP_Thk	tox	260	290	320	angs	#1

C5X (0.5 Micron) 12V Single Sided Nested-Drain NCh Electrical Parameters

Note: Maximum allowable operating voltage is 13.2V on drain and gate, and 5.5V on source. This is the NU device in the model file.

Structure	Test	Min	Typ	Max	Units	Notes
N20x3_ND	BVDSS	14	19	-	V	#13
N20x3_ND	IDSAT_12	7.5	9.0	10.5	mA	#9
N20x3_ND	Lkg_13.2	-	-	0.5	nA/um	#23
N20x3_ND	Vt	0.8	1.0	1.2	V	#3

C5X (0.5 Micron) 12V Single Sided Nested-Drain PCh Electrical Parameters

Note: Maximum allowable operating voltage is -13.2V on drain and gate, and -5.5V on source, relative to N-Well. This is the PU device in the model file.

Structure	Test	Min	Typ	Max	Units	Notes
P20x3_ND	BVDSS	-	-14.5	-14.0	V	#13
P20x3_ND	Idsat	-2.7	-2.2	-1.7	mA	#9
P20x3_ND	Lkg_13.2	-0.5	-	-	nA/um	#23
P20x3_ND	Vt	-1.95	-1.65	-1.45	V	#3

C5X (0.5 Micron) 15/15V Ext-Drain Double Sided NCh Electrical Parameters

Note: Maximum allowable gate and source operating voltage is 15.5V.Maximum allowable drain operating voltage is 22.0V. This is the NZ device in the model file.

Note: For operating temperature greater than 70 degree C limit the gate to well operating voltage to 13.2V.

Structure	Test	Min	Typ	Max	Units	Notes
N20X5ED	BVDSS	24	28	-	V	#13
N20X5ED	IDSAT_15	6.5	8.0	9.5	mA	#9
N20X5ED	Isubpk_22	-100	-50	-	uA	#28
N20X5ED	Lkg_22	-	10	2000	pA	#23
N20X5ED	Vt_gm	0.8	1.0	1.2	Volts	#3

C5X (0.5 Micron) 15/15V Ext-Drain Double Sided PCh Electrical Parameters

Note: Maximum allowable gate and source operating voltage is -15.5V relative to N-Well. Maximum allowable drain operating voltage is -22.0V relative to N-Well. This is the PZ device in the model file.

Note: For operating temperature greater than 70 degree C limit the gate to well operating voltage to 13.2V.

Structure	Test	Min	Typ	Max	Units	Notes
P20X5ED	BVDSS	-	-28	-24	Volts	#13
P20X5ED	IDSAT_15	-3.2	-2.6	-2.0	mA	#9
P20X5ED	Isubpk_22	-	1	5	uA	#28
P20X5ED	Lkg_22	-2000	-10	-	pA	#23
P20X5ED	Vt_gm	-1.85	-1.65	-1.45	Volts	#3

C5X (0.5 Micron) 15/20V Ext-Drain Single Sided NCh Electrical Parameters

Note: Maximum allowable gate operating voltage is 15.5V.Maximum allowable drain operating voltage is 22.0V. Maximum allowable source operating Voltage is 5.5V. This is the NX device in the model file.

Note: For operating temperature greater than 70 degree C limit the gate to well operating voltage to 13.2V.

Structure	Test	Min	Typ	Max	Units	Notes
N20X5ED	BVDSS	24	28	-	Volts	#13
N20X5ED	IDSAT_15	6.5	8.0	9.5	mA	#9
N20X5ED	Isubpk_22	-100	-50	-	uA	#28
N20X5ED	LKG_22	-	10	2000	pA	#23
N20X5ED	Vt_gm	0.8	1.0	1.2	Volts	#3

C5X (0.5 Micron) 15/20V Ext-Drain Single Sided PCh Electrical Parameters

Note: Maximum allowable gate operating voltage is -15.5V relative to N-Well. Maximum allowable drain operating voltage is -22.0V relative to N-Well. Maximum allowable source operatiing voltage is -5.5V relative to N-Well. This is the PX device in the model file.

Note: For operating temperature greater than 70 degree C limit the gate to well operating voltage to 13.2V.

Structure	Test	Min	Typ	Max	Units	Notes
P20X5ED	BVDSS	-	-28	-24	Volts	#13
P20X5ED	IDSAT_15	-3.2	-2.6	-2.0	mA	#9
P20X5ED	Isubpk_22	-	1	5	uA	#28
P20X5ED	Lkg_22	-2000	-10	-	pA	#23
P20X5ED	Vt_gm	-1.85	-1.65	-1.45	V	#3

C5X (0.5 Micron) 5/20V Ext-Drain NCh Electrical Parameters

Note: Maximum allowable gate operating voltage is 5.5V.Maximum allowable drain operating voltage is 22.0V. This is the NT device in the model file.

Structure	Test	Min	Typ	Max	Units	Notes
N20X5ED	BVDSS	22.5	28.0	-	V	#13
N20X5ED	Idsat_5	2.2	2.9	3.6	mA	#9
N20X5ED	Lkg_22	-	20	6000	pA	TBD
N20X5ED	Vt_gm	0.5	0.75	1.0	V	#3

C5X (0.5 Micron) 5/20V Ext-Drain PCh Electrical Parameters

Note: Maximum allowable gate operating voltage relative to N-Wells -5.5V. Maximum allowable drain operating voltage is -22.0V, relative to N-Well. This is the PT device in the model file.

Structure	Test	Min	Typ	Max	Units	Notes
P20X5ED	BVdss	-	-28.0	-22.5	V	#13
P20X5ED	Idsat_5	-1.6	-1.1	-0.6	mA	#9
P20X5ED	Lkg_22	-6000	-20	-	pA	TBD
P20X5ED	Vt_gm	-1.3	-1.0	-0.7	V	#3

C5X (0.5 Micron) Diode Leakage Parameters

Parameter	Symbol	Min	Typ	Max	Units	Notes
N+P-_diode, D_Lkg, Area	DLNPPMA	-	-	10	fA/µm²	#26 D_Lkg_5.5
N+P-_diode, D_Lkg, Edge	DLNPPME	-	-	20	fA/µm	#26 D_Lkg_5.5
N-P-_diode, D_Lkg, Area	DLNMPMA	-	-	10	fA/µm²	#26 D_Lkg_5.5
N-P-_diode, D_Lkg, Edge	DLNMPME	-	-	20	fA/µm	#26 D_Lkg_5.5
P+N-_diode, D_Lkg, Area	DLPPNMA	-	-	10	fA/µm²	#26 D_Lkg_5.5
P+N-_diode, D_Lkg, Edge	DLPPNME	-	-	20	fA/µm	#26 D_Lkg_5.5

C5X (0.5 Micron) Intra-Line Capacitor Parameters

Note: All intra line capacitance is one-sided

Parameter	Symbol	Min	Typ	Max	Units	Notes
M1 to M1 on Field, Space	CM1M1	0.064	0.071	0.079	fF/µm	#43
M2 to M2 on Field, Space	CM2M2	0.063	0.068	0.075	fF/µm	#43
M3 to M3 on Field, Space	CM3M3	0.077	0.084	0.091	fF/µm	#43
Poly to Poly on Field, Space	CPP	0.031	0.037	0.039	fF/µm	#43
Poly2 to Poly2 on Field, Space	CP2P2	0.0031	0.0034	0.0037	fF/µm²	#43

C5X (0.5 Micron) Line to Plane Capacitor Parameters

Note: Capacitance parameters are for the ideal case shown above. All periphery caps are one-sided.

Parameter	Symbol	Min	Typ	Max	Units	Notes
M1 on Active, Area	CM1A	0.028	0.031	0.033	fF/µm²	#40
M1 on Active, Periphery	CM1AP	0.041	0.042	0.045	fF/µm	#40
M1 over Poly on Active, Area	CM1PA	0.044	0.049	0.053	fF/µm²	#41
M1 over Poly on Active, Periphery	CM1PAP	0.012	0.013	0.015	fF/um	#41
M1 over Poly on Field, Area	CM1P	0.047	0.055	0.064	fF/µm²	#40
M1 over Poly on Field, Periphery	CM1PP	0.016	0.019	0.026	fF/µm	#40
M1 over Poly2 on Active, Area	CM1P2A	0.040	0.044	0.048	fF/µm²	#41
M1 over Poly2 on Active, Periphery	CM1P2AP	0.0096	0.010	0.012	fF/um	#41
M1 over Poly2 on Field, Area	CM1P2	0.041	0.047	0.054	fF/µm²	#41
M1 over Poly2 on Field, Periphery	CM1P2P	0.015	0.016	0.022	fF/um	#41
M1 over Poly2 on Poly on Active, Area	CM1P2PA	0.064	0.072	0.078	fF/µm²	#42
M1 over Poly2 on Poly on Active, Periphery	CM1P2PAP	0.013	0.014	0.015	fF/µm²	#42
M1 over Poly2 on Poly on Field, Area	CM1P2PFA	0.089	0.098	0.109	fF/µm²	#42
M1 to Substrate on Field, Area	CM1S	0.024	0.027	0.030	fF/µm²	#41
M1 to Substrate on Field, Periphery	CM1SP	0.040	0.041	0.043	fF/µm	#40
M2 on Active, Area	CM2A	0.011	0.012	0.013	fF/µm²	#40
M2 on Active, Periphery	CM2AP	0.032	0.033	0.033	fF/µm	#40
M2 over M1 on Field, Area	CM2M1	0.029	0.032	0.035	fF/µm²	#41
M2 over M1 on Field, Periphery	CM2M1P	0.020	0.023	0.025	fF/µm	#41
M2 over Poly on Active, Area	CM2PA	0.013	0.014	0.016	fF/µm²	#41
M2 over Poly on Active, Periphery	CM2PAP	0.0036	0.0040	0.0044	fF/um	#41
M2 over Poly on Field, Area	CM2P	0.013	0.015	0.016	fF/µm²	#41
M2 over Poly on Field, Periphery	CM2PP	0.0057	0.0064	0.0070	fF/µm	#41
M2 over Poly2 on Active, Area	CM2P2A	0.012	0.014	0.015	fF/µm²	#41
M2 over Poly2 on Active, Periphery	CM2P2AP	0.0042	0.0047	0.0051	fF/um	#41
M2 over Poly2 on Field, Area	CM2P2	0.013	0.014	0.016	fF/µm²	#41
M2 over Poly2 on Field, Periphery	CM2P2P	0.0052	0.0057	0.0063	fF/um	#41
M2 over Poly2 on Poly on Active, Periphery	CM2P2PAP	0.0047	0.0053	0.0058	fF/µm²	#42
M2 over Poly2 on Poly on Field, Area	CM2P2PF	0.015	0.017	0.018	fF/µm²	#42
M2 over Poly2 on Poly on Field, Periphery	CM2P2PFP	0.0039	0.0044	0.0048	fF/um	#42
M2 to Substrate on Field, Area	CM2S	0.010	0.011	0.012	fF/µm²	#40
M2 to Substrate on Field, Periphery	CM2SP	0.032	0.033	0.034	fF/µm	#40
M3 on Active, Area	CM3A	0.0068	0.0075	0.0079	fF/µm²	#40
M3 on Active, Periphery	CM3AP	0.029	0.030	0.031	fF/µm	#40
M3 over M1 on Field, Area	CM3M1	0.011	0.013	0.014	fF/µm²	#41
M3 over M1 on Field, Periphery	CM3M1P	0.009	0.010	0.011	fF/µm	#41
M3 over M2 on Field, Area	CM3M2	0.029	0.032	0.035	fF/µm²	#41
M3 over M2 on Field, Periphery	CM3M2P	0.024	0.027	0.029	fF/µm	#41

M3 over Poly on Active, Area	CM3PA	0.0074	0.0082	0.0091	fF/µm²	#41
M3 over Poly on Active, Periphery	CM3PAP	0.0018	0.0020	0.0022	fF/µm²	#41
M3 over Poly on Field, Area	CM3P	0.0077	0.0085	0.0093	fF/µm²	#41
M3 over Poly on Field, Periphery	CM3PP	0.0031	0.0035	0.0038	fF/um	#41
M3 over Poly2 on Active, Area	CM3P2A	0.0073	0.0081	0.0089	fF/µm²	#41
M3 over Poly2 on Active, Periphery	CM3P2AP	0.0026	0.0028	0.0032	fF/um	#41
M3 over Poly2 on Field, Area	CM3P2	0.0075	0.0083	0.0091	fF/µm²	#41
M3 over Poly2 on Field, Periphery	CM3P2P	0.0028	0.0031	0.0034	fF/um	#41
M3 over Poly2 on Poly on Active, Area	CM3P2PA	0.0080	0.0088	0.0097	fF/µm²	#42
M3 over Poly2 on Poly on Field, Area	CM3P2PF	0.0083	0.0092	0.0010	fF/µm²	#42
M3 over Poly2 on Poly on Field, Periphery	CM3P2PFP	0.0018	0.0020	0.0022	fF/um	#42
M3 to Substrate on Field, Area	CM3S	0.0066	0.0073	0.0077	fF/µm²	#40
M3 to Substrate on Field, Periphery	CM3SP	0.029	0.030	0.031	fF/um	#41
Poly on Field, Area	CPS	0.098	0.12	0.13	fF/µm²	#40
Poly on Field, Periphery	CPSP	0.049	0.053	0.066	fF/um	#40
Poly2 on Active, Area	CP2A	0.82	0.91	1.00	fF/µm²	#40
Poly2 on Active, Periphery	CP2AP	0.076	0.085	0.093	fF/µm²	#40
Poly2 on Field, Area	CP2S	0.086	0.10	0.11	fF/µm²	#41
Poly2 on Field, Periphery	CP2SP	0.052	0.056	0.068	fF/um	#40
Poly2 over Poly on Field, Area	CP2P	0.8	0.9	0.96	fF/µm²	#41
Poly2 over Poly on Field, Periphery	CP2PP	0.04	0.065	0.127	fF/µm	#41

C5X (0.5 Micron) N-Channel Electrical Parameters

Structure	Test	Min	Typ	Max	Units	Notes
N20x0.6	BVdss	8	14	18	V	#13
N20x0.6	BVnp	8	14	18	V	#12
N20x20	BVnpg	8	14	18	V	#12
N20x20	Gamma	0.49	0.54	0.635	V½	#7
N20x0.6	Idsat_5	0.38	0.45	0.52	mA/µM	#9
N20x20	Kprime_L	100	116	127	µA/V²	#4-A
N20x20	Kprime_S	54	84	114	µA/V²	#4-B
N20x0.6	Leff_i	0.45	0.54	0.65	µM	#5-B
N20x0.6	Lkg_5.5	-	1.0	100	pA/µM	#23
N20x5	Out_con	-	2.0	-	µA/V	#36
N20x0.6	Sub_SL	85	92	100	mV/dec	#8
N20x20	Sub_SL	85	90	95	mV/dec	#8
N20x0.6	VBII	7.0	8.0	-	V	#32
N_Met	Vt_fld	25	-	-	V	#10
N_PSI	Vt_fld	8	15	18	V	#10
N0.8x0.6	Vt_gm	0.80	1.10	1.40	V	#3
N20x0.6	Vt_gm	0.525	0.696	0.813	V	#3
N20x20	Vt_gm	0.612	0.752	0.82	V	#3
N0.8x20	Weff_gm	0.448	0.572	0.708	µM	#6

C5X (0.5 Micron) P-Channel Electrical Parameters

Structure	Test	Min	Typ	Max	Units	Notes
P20x0.6	BVdss	-15	-12	-8	V	#13
P20x0.6	BVpn	-15	-12	-8	V	#12
P20x20	BVpng	-15	-12	-8	V	#12
P20x20	Gamma	0.5	0.555	0.58	V½	#7
P20x0.6	Idsat_5	-0.32	-0.26	-0.18	mA/µM	#9
P20x20	Kprime_L	32	37	40	µA/V²	#4-A
P20x20	Kprime_S	18	23	28	µA/V²	#4-B
P20x0.6	Leff_i	0.45	0.534	0.65	µm	#5-B
P20x0.6	Lkg_5.5	-	1	100	pA/µM	#23
P20x5	Out_con	-	0.5	-	µA/V	#36
P20x0.6	Sub_SL	80	90	100	mV/dec	#8
P20x20	Sub_SL	80	85	90	mV/dec	#8
P_Met	Vt-fld	-	-	-25	V	#10
P_PSI	Vt-fld	-15	-12	-8	V	#10
P0.8x0.6	Vt_gm	-1.15	-0.95	-0.75	V	#3
P20x0.6	Vt_gm	-1.035	-0.905	-0.805	V	#3
P20x20	Vt_gm	-1.085	-0.959	-0.861	V	#3
P0.8x20	Weff_gm	0.444	0.584	0.744	µm	#6

C5X (0.5 Micron) N40VTile Device

Structure	Test	Min	Typ	Max	Units	Notes
N40VTile	BVdss	75	>80	-	Volts	#13
N40VTile	BVnpg	-	>80	-	Volts	#12
N40VTile	Idsat_12_30	-	10.2	-	mA	#9-F
N40VTile	Idsat_12_40	7.8	10	12.2	mA	#9-F
N40VTile	Isub_pk44	0	-7.5	-13	uA	#28-G
N40VTile	Kprime_L	-	825	-	uA/V2	#4-A
N40VTile	Lkg_44	0	18	500	pA	#23-E
N40VTile	Ron	-	535	-	ohms	
N40VTile	Vt_gm	0.7	0.9	1.1	Volts	#3

C5X (0.5 Micron) P40VTile Device

Structure	Test	Min	Typ	Max	Units	Notes
P40VTile	BVdss	-	-72	-60	Volts	#13
P40VTile	BVpng	-	<-72	-	Volts	#12
P40VTile	Idsat_12_30	-	-7.7	-	mA	#9-F
P40VTile	Idsat_12_40	-10	-8	-6	mA	#9-F
P40VTile	Isub_pk44	0	2.6	10	uA	#28-G
P40VTile	Kprime_L	-	380	-	uA/V2	#4-A
P40VTile	Lkg_44	0	79	500	pA	#23-E
P40VTile	Ron	-	1400	-	ohms	
P40VTile	Vt_gm	-2.1	-1.75	-1.4	Volts	#3

C5X (0.5 Micron) NI Device

Note: NI Device is only available in C5S and C5T. C5S is a double poly, high R, double metal, complementary poly low threshold process which has all flavors of MOSFETS in C5 family except 40 volt and includes new intrinsic NMOS (NI), complementary poly intrinsic PMOS (PI), complementary poly low threshold PMOS (PLO), and P+ Poly resistor (PL). NI is not a true native device. NI DEVICE HAS A MINIMUM ALLOWED GATE LENGTH OF 0.8 MICRON. C5T is C5S with triple metal.

Structure	Test	Min	Typ	Max	Units	Notes
NI20x0.8	BVdss	8	11	14	V	#13
NI20x20	BVnpg	-	11	-	V	#12
NI20x20	Gamma	0.33	0.48	0.63	V½	#7
NI20x0.8	Idsat_5	0.33	0.43	0.53	mA/µM	#9
NI20x0.8	Isub_5.5	0	-1	-10	uA/um	#28-C
NI20x20	Kprime_L	104	124	144	µA/V²	#4-A
NI20x0.8	Leff_i	-	0.7	-	µm	#5-B
NI20x0.8	Lkg_5.5	-	3	200	pA/µM	#23
NI0.8x0.8	Vt_gm	-	TBD	-	V	#3
NI20x0.8	Vt_gm	0.28	0.43	0.58	V	#3
NI20x20	Vt_gm	0.29	0.44	0.59	V	#3
NI0.8x20	Weff_gm	-	0.58	-	µm	#6

C5X (0.5 Micron) PI Device

Note: PI Device is only available in C5S and C5T. C5S is a double poly, high R, double metal, complementary poly low threshold process which has all flavors of MOSFETS in C5 family except 40 volt and includes new intrinsic NMOS (NI), complementary poly intrinsic PMOS (PI), complementary poly low threshold PMOS (PLO), and P+ Poly resistor (PL). PI is a true native device. C5T is C5S with triple metal.

Structure	Test	Min	Typ	Max	Units	Notes
PI20x0.6	BVdss	-14	-11	-8	V	#13
PI20x20	BVpng	-	-11	-	V	#12
PI20x20	Gamma	0.5	0.65	0.8	V½	#7
PI20x0.6	Idsat_5	-0.305	-0.245	-0.185	mA/µM	#9
PI20x20	Kprime_L	22	30	38	µA/V²	#4-A
PI20x0.6	Leff_i	-	0.53	-	µm	#5-B
PI20x0.6	Lkg_5.5	-	8.9	200	pA/µM	#23
PI0.8x0.6	Vt_gm	-	-0.46	-	V	#3
PI20x0.6	Vt_gm	-0.58	-0.38	-0.18	V	#3
PI20x20	Vt_gm	-0.61	-0.41	-0.21	V	#3
PI0.8x20	Weff_gm	-	0.62	-	µm	#6

C5X (0.5 Micron) PLO Device

Note: PLO Device is only available in C5S and C5T. C5S is a double poly, high R, double metal, complementary poly low threshold process which has all flavors of MOSFETS in C5 family except 40 volt and includes new intrinsic NMOS (NI), complementary poly intrinsic PMOS (PI), complementary poly low threshold PMOS (PLO), and P+ Poly resistor (PL). PLO is a ~0.6 volts threshold device. C5T is C5S with triple metal.

Structure	Test	Min	Typ	Max	Units	Notes
PLO20x0.6	BVdss	-14	-11	-8	V	#13
PLO20x20	BVpng	-	-11	-	V	#12
PLO20x20	Gamma	0.54	0.69	0.84	V½	#7
PLO20x0.6	Idsat_5	-0.265	-0.205	-0.145	mA/µM	#9
PLO20x20	Kprime_L	19.5	27.5	35.5	µA/V²	#4-A
PLO20x0.6	Leff_i	-	0.53	-	µm	#5-B
PLO20x0.6	Lkg_5.5	-	1	100	pA/µM	#23
PLO0.8x0.6	Vt_gm	-	-0.66	-	V	#3
PLO20x0.6	Vt_gm	-0.72	-0.6	-0.48	V	#3
PLO20x20	Vt_gm	-0.75	-0.65	-0.55	V	#3
PLO0.8x20	Weff_gm	-	0.67	-	µm	#6

C5X (0.5 Micron) Resistor Parameters

Structure	Test	Min	Typ	Max	Units	Notes
Capacitor Poly Res 40x200 - Standard	Res_2	40	50	60	ohms/sq	#14
Capacitor Poly Res 40x200 - Under HR Mask	Res_2	800	1000	1200	ohms/sq	#14
M1 Sheet Res	Res_2	75	85	95	m-ohms/sq	#14
M2 Sheet Res	Res_2	75	85	95	m-ohms/sq	#14 double metal use M3
M3 Sheet Res	Res_2	33	40	47	m-ohms/sq	#14
N+ Poly Sheet Res 20x100 (double poly processes)	Res_2	20	25	30	ohms/sq	#14
N+ Poly Sheet Res 20x100 (single poly processes)	Res_2	23	30	37	ohms/sq	#14
N+ sheet Res 40x200	Res_2	60	90	120	ohms/sq	#14
N-Tub Res (Fld) 10x200	Res_2	10000	16000	22000	ohms	_
N-Tub Res (Fld) 5x200	Res_2	16000	32000	48000	ohms	_
N-Tub Sheet Res (Act) 40x200	Res_2	500	750	1000	ohms/sq	#14
N-Tub Sheet Res 40x200, (Fld)	Res_2	500	800	1100	ohms/sq	#14
P+ Poly 20x100	Res_2	200	375	500	Ohms/sq	#14 C5S/T Complementary Poly Process Only.
P+ Sheet Res 40x200	Res_2	70	115	160	ohms/sq	#14
M1-N+ Cnt Res 0.5 µM²	Res_Cnt	-	30	60	ohms/Cnt	#24
M1-P+ Cnt Res 0.5 µM²	Res_Cnt	-	100	200	ohms/Cnt	#24
M1-P+ Poly 0.5x0.5	Res_Cnt	200	350	750	ohms/cnt	#24 C5S/T Complementary Poly Process Only. CAUTION: High Value.
M1-Poly 0.5 µM²	Res_Cnt	-	7	15	ohms/Cnt	#24
M1-M2 Via Res 0.5 µM²	Res_Via	-	1.0	3.0	ohms/Cnt	#24
M2-M3 Via Res 0.5 µM²	Res_Via	0	1.0	3.0	ohms/Cnt	#24

C5X (0.5 Micron) Schottky Diode Device

Structure	Test	Min	Typ	Max	Units	Notes
Schottky.3	DIODE_BV	-	-12.1	-11.6	volt	#44
Schottky.3	D_Lkg-5.5	-	3.6	10	nA	#44
Schottky.3	ID.25	2.3	7.0	11.7	uA	#44
Schottky.3	ID.6	1.35	1.65	1.95	mA	#44
Schottky.3	Isub.6	-70	-38	-	nA	#44

C5X (0.5 Micron) Structural Parameters

Parameter	Symbol	Min	Typ	Max	Units	Notes
CMP BPSG Thickness, Over Flat Area	TBPSGF	8500	9500	10500	A	#1
CMP BPSG Thickness, Over Poly on Fox	TBPSGP	3850	4850	5850	A	#1
CMP M1 Thickness	TM1	5700	6400	7100	A	#2
CMP M2 Thickness	TM2	5000	5700	6400	A	#2 double metal use M3
CMP M2 to M1 Dielectric	TM2M1	10000	11000	12000	A	#1
CMP M3 Thickness	TM3	7000	7700	8400	A	#2
CMP M3 to M1 Dielectric	TM3M1	25000	27700	30400	A	#1
CMP M3 to M2 Dielectric	TM3M2	10000	11000	12000	A	#1
Field Ox Thickness Grown	TFOX	4000	4500	5000	A	#1
Field Ox Under M1	TFOXM	3250	3750	4250	A	#1
Field Ox Under Poly	TFOXP	3500	4000	4500	A	#1
Gate Ox Thickness	TGOX	125	135	145	A	#1
N+ Junction Depth	XJN	0.15	0.25	0.35	µm	#2
N-LDD Junction Depth	XJNLDD	0.15	0.20	0.25	µm	#2
N-Tub Depth	XJNT	2.5	3.0	3.5	µm	#2
P+ Junction Depth	XJP	0.20	0.30	0.40	µm	#2
Poly Thickness	TPOLY	3000	3500	4000	A	#2
Poly2 to Poly Ox Thickness	TP2P	335	390	445	A	#1
Scratch Protection, Ox/Nit Thickness	TPROT	15700	17000	18700	A	#2
Thick Gate Ox Thickness	TTHGOX	260	290	320	A	#1

C5X (0.5 Micron) Temperature Coefficients

Parameter	Symbol	Min	Typ	Max	Units	Notes
Dbl-Fact N+/P- Leakage	DFNPPM	-	10	-	°c-1	#22
Dbl-Fact N-/P-. Leakage	DFNMPM	-	11	-	°c-1	#22
Dbl-Fact N-Ch Lkg	DFLKGN	-	10	-	°c-1	#22 Lkg_5.5(20x0.6)
Dbl-Fact P+/N- Leakage	DFPPNM	-	10	-	°c-1	#22
Dbl-Fact P-Ch Lkg	DFLKGP	-	10	-	°c-1	#22 Lkg_5.5(20x0.6)
Dbl-Fact Schottky Metal/N- Leakage	DFSMNM	-	13.2	-	°C-1	#22
TC N+ Poly Res	TCNPPR	-	0.00065	-	°c-1	#21
TC N+ Res	TCNPR	-	0.0015	-	°c-1	#21
TC N-Ch Threshold	TCVTON	-	-1.5	-	mV/°C	#17
TC N-M1-Field Threshold	TCVTFMN	-	TBD	-	mV/°C	#17
TC N-Tub Field Res	TCNMR	-	0.0075	-	°c-1	#21
TC P+ Res	TCPPR	-	0.0016	-	°c-1	#21
TC P-Ch Threshold	TCVTOP	-	1.8	-	mV/°C	#17
TC P-M1-Field Threshold	TCVTFMP	-	TBD	-	mV/°C	#17
TC P-Poly-Field Threshold	TCVTFPP	-	15	-	mV/°C	#17

C5X (0.5 Micron) Transistor Capacitor Parameters

Parameter	Symbol	Min	Typ	Max	Units	Notes
Gate to S/D Overlap N-CH	CGOXNP	0.25	0.30	0.35	fF/µm	#20
Gate to S/D Overlap P-CH	CGOXPP	0.30	0.35	0.40	fF/µm	#20
Gate to Substrate, Area	CGOX	2.28	2.56	2.84	fF/µm²	#1

C5X (0.5 Micron) Design Rules

Die Seal Ring Rules

AMIS 4500099 Rev: T

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Die Seal Ring Rules

Introduction

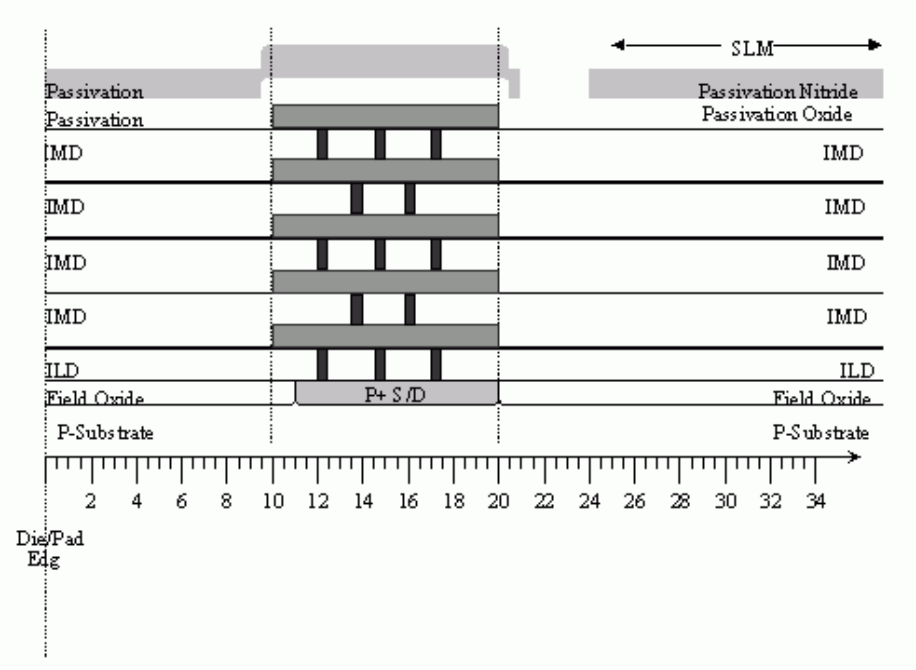
This section covers the AMI's methodology for placement of a die seal for moisture protection and edge of die to scribe lane layout..

Purpose

The purpose of this section is to define a scribe lane and an edge of die, which will give a moisture resistant die, without the possibility that cracks generated during sawing can propagate into the die.

Guidelines

The AMI Data Preparation Groups will place a standard 10µ wide die seal ring 10µ from the outermost data of the die. A cross-sectional view of this design is provided below. No variations of this design are allowed. AMI cannot guarantee any customer-placed die seal ring, so these will not be allowed.



Glossary - Notations and Definitions

Layout

"-" - Logical "and", e.f. P+-Act is a region having both P+ and Act digitized.

Butted Contacts - Contacts crossing over N+ and P+ regions used to tie the source and well to the same potential. **Butted contacts are not allowed in the C5 process. However, butted diffusions are allowed, but should be used with care in analog and/or matching applications.**

Fld - Field Oxide regions, i.e. where Active is "not" digitized.

Internal Cell - Internal circuitry buffered by protection circuitry.

Min. Dim. - Minimum Dimension.

Min. Enc. - Minimum Enclosure.

Min. Ext. - Minimum Extension (assumes directionality).

Min. Sp. - Minimum Space.

N+ - Regions to be opened at N+ and N- implant mask, i.e. regions where P+ is not digitized

not() - Logical "not", e.f. not(Act) is all regions not digitized with Act.

Peripheral - Circuitry related to protection circuitry and I/O Cells.

Per-Bus - Peripheral Bus, used as seal ring and substrate tie surrounding the circuit.

Per-Bus St - Peripheral-Bus Start, defined at edge of active area of Per-Bus in the direction of die center.

PW - P-Well, regions where N-Well is "not" digitized.

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Electromigration

Electromigration - A process which metal in interconnects or contacts migrate over time when current is applied. This can result in the interconnect or contact failing if the current density of the structure is too high for a given temperature.

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Parametric

Bvdss - Drain to source breakdown measurement as described in TIPS Notes document 4510053.

Bvnp - N+/P- junction breakdown measurement as described in TIPS Notes document 4510053.

Bvnpg - Gated N+/p- junction breakdown measurement as described in TIPS Notes document 4510053.

Bvpn - P+/N- junction breakdown measurement as described in TIPS Notes document 4510053.

Bvpng - Gated P+/N- junction breakdown measurement as described in TIPS Notes document 4510053.

Gamma - Body factor measurement as described in TIPS Notes document 4510053.

D_Lkg - Diode leakage measurement as described in TIPS Notes document 4510053.

IDSAT_5 - P+/N- Saturation current measurement as described in TIPS Notes document 4510053.

Kprime_L - Linear gain factor measurement as described in TIPS Notes document 4510053.

Kprime_S - Saturation gain factor measurement as described in TIPS Notes document 4510053.

Leff_I - Electrical channel length measurement as described in TIPS Notes document 4510053.

Lkg_5.5 - Drain to source leakage measurement as described in TIPS Notes document 4510053.

Out_con - Drain to source conductance measurement as described in TIPS Notes document 4510053.

Res_2 - Sheet resistance measurement as described in TIP Notes document 4510053.

Res_Cnt - Contact resistance measurement as described in TIP Notes document 4510053

Res_Via - Via resistance measurement as described in TIP Notes document 4510053.

Structure - Device structure used for test. The structure notation used often, but not exclusively, contains the polarity, width and length of the structure, e.f. P20x0.6 refers to a P-channel transistor with a drawn width of 20μ m and a drawn length of 0.6μ m. Further descriptions of the structures are given in the TIPS Notes AMI document 4510053.

Sub_SL - Sub-threshold slope measurement as described in TIPS Notes document 4510053.

TC - Temperature Coefficient measurement as described in TIP Notes document 4510053.

VBII - Voltage breakdown from impact ionization measurement as described in TIPS Notes document 4510053.

Vt_gm - Extrapolated threshold measurement as described in TIPS Notes document 4510053.

Weff_gm - Electrical channel width measurement as described in TIPS Notes document 4510053.

Vt_fld - Field threshold measurement as described in TIPS Notes document 4510053.

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Model

BSIM - Berkeley Short Channel IGFET Model.

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ESD Notation and Definition

Contact Spiking - The migration of contact metal into the Silicon below and/or Silicon into the contact metal caused by excessive heat or current through the contact. When the contact metal migrates into the surrounding junction, the metal will short the junction.

Secondary Breakdown - An event where current passing under the gate of a MOS transistor or through the Base of a Bipolar transistor heats a localized region which in turn causes additional current to flow through that region. The positive feedback system generated causes damage to the silicon and oxide in the region.

Latch-Up Notation and Definition

SCR - Semiconductor Controlled Rectifier.

VDD - Highest potential supplied on a integrated circuit.

VSS - Lowest potential supplied on a integrated circuit.

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C5X (0.5 Micron) Design Rules

Technical Information

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AMIS Confidential

General ESD Guidelines

These guidelines are intended to be used in conjunction with the preceding rule set. The layout considerations are intended to provide guidance in optimizing ESD performance for I/O cells and may reduce the electrical performance of the cells. Actual I/O cells with ESD data may be licensed from AMI.

If you need a glossary, please see Glossary - Notations and Definitions.

Failure Modes

- Snapback and Secondary Breakdown of the N-Channel output driver devices.
- Contact Spiking.

Recommendations

- Provide for uniform distribution of the current along the width of the N-Channel output devices.
- Provide adequate diffusion overlap of contacts in the output structures.

Layout Considerations

- Use multi-fingered layout configuration for output devices.
- Use metal interconnect to minimize impedance to fingered drain regions to insure uniform current distribution.
- Maximize the number of contacts used for connection to output structures.
- Maximize diffusion overlap of contacts
- Maximize the drain contact to gate edge spacing.
- Maximize the metal overlap of contact on output structures.
- Maximize the width of the output transistors.
- Where possible use a wide and short N-Well resistor in series with drain to assist in uniform current flow through the drain.
- Use minimum channel length output devices.
- Maximize the diode/clamp area to VDD and VSS and between VDD and VSS.
- Use Guard rings and good layout practices to protect output structures from SCR latchup conditions.

General Latch-Up Guidelines

Latch-up is the condition when a parasitic SCR is triggered on a CMOS circuit. The PNPN SCR is often described as a coupled pair of bipolar transistors consisting of a PNP and a NPN. The base of the PNP is the collector of the NPN which physically is the N-Well. The base of the NPN is the collector of the PNP which physically is the substrate. The emitter of the PNP is a P+ region in the N-Well. The emitter of the NPN is a N+ region in the substrate in close proximity to the N-Well. For latch-up to occur the P+ region must be at a higher potential than the N+ region. In addition, the base/emitter junction of the PNP and/or the NPN must be forward biased. Biasing either the NPN or the PNP will in turn bias the other. As the base emitter currents are increased, the beta of the bipolars are increased. At the point when the product of the PNP beta and the NPN beta becomes greater than one the SCR is triggered. Once the SCR is triggered it is self biasing and will continue to allow current flow as long as the potential on the P+ emitter is higher than the N+ emitter. Triggering one SCR will trigger other SCRs in the circuit forcing the resistance from VDD to VSS to approach zero causing excessive power supply current.

The maximum beta of the parasitic bipolar is a function of the base-width and base doping level. The base-width of the lateral NPN is defined by the N-Well to N+ spacing. The base-width of the PNP is defined by the N-Well overlap of the P+ active area. As these design rules are reduced with each new technology the circuits become more susceptible to Latch-up if adequate design techniques are not used.

If you need a glossary, please see Glossary - Notations and Definitions.

Failure Modes

- Substrate current raises the local P- substrate potential of an SCR structure above VSS.
- Local N-Well potential of an SCR structure falls below VDD.

Recommendations

- Guardbar large drivers and I/O cells.
- Add substrate and well contacts as often as possible. For bulk starting material, substrate contacts should be placed every 45 μ m.
- N-Well Contact should be placed such that the resistance between any two N-Well contacts does not exceed 50KΩ .