

**EE143 Microfabrication Technology**  
**Midterm Exam 1**

**Name:** Solutions

**Signature:** \_\_\_\_\_

**SID:** \_\_\_\_\_

CLOSED BOOK. ONE 8 1/2" X 11" SHEET OF NOTES, AND SCIENTIFIC POCKET CALCULATOR PERMITTED.

*TIME ALLOTTED: 80 MINUTES*

1. Lithography

- a. Give three of the important performance parameters that determine the usefulness of a photoresist.

Any of the following:

1. sensitivity
2. resolution
3. etch resistance
4. contrast
5. edge slope
6. resist type (positive or negative)

- b. Why is contact printing unsuitable for high-volume manufacturing of complex integrated circuits?

- resist sticking causes defects
- resolution is limited to  $> 1\mu\text{m}$

- c. What is the purpose of the postexposure bake for chemically amplified photoresist?

activate the photo acid generator and  
the catalytic reaction of photo acid to  
deprotect the resist.

- d. Give two advantages of projection lithography over proximity printing

- Higher resolution
- Reducitn in imaging allows larger mask features

2. Safety

- a. Why do you add acid to water as opposed to adding water to acid when preparing a diluted acid solution?

Concentrated acid diluting with water is exothermic. The solution gets hot and may spit and bubble.

Adding acid to water dilutes acid and slowly increases concentration. Acid sinks causing heat to dissipate in bulk of water.

- b. While etching a wafer in piranha solution, you accidentally pick up a beaker of the solution. It is hot! You drop the beaker, it splashes the solution on your lab coat, which soaks through and you feel a burning sensation on the skin of your chest. What do you do? Answer specifically and fully to get full credit.

strip off clothes,  
Wash off in safety shower for 15 mins.

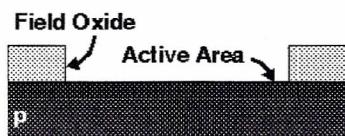
### 3. Lab related

So far, you have finished gate oxidation step. The ideal lab process flow is the following:

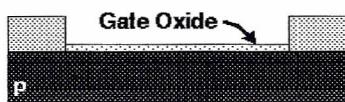
Week 2: Field Oxidation - 5200 Å



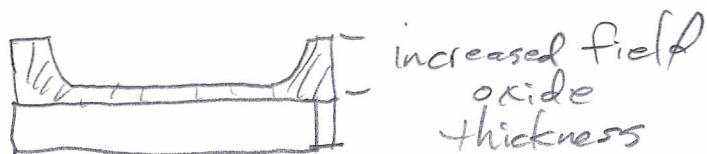
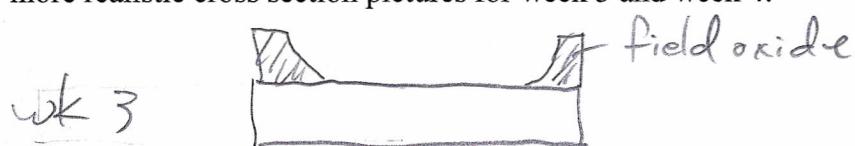
Week 3: Active Area Photolithography



Week 4: Gate Oxidation - 800 Å



- a. Draw more realistic cross section pictures for week 3 and week 4.



- b. What is the function of gate oxide and field oxide? What oxidation methods are used for them? Why?

gate oxide is insulator for MOSFET  
Dry oxidation: slower, more controlled, higher quality  
low trapped charge and interface trap density  
field oxide isolates adjacent transistors  
wet oxidizer: faster growth

- c. The channel doping concentration (p-Si doping concentration) is a critical parameter for MOSFETs. This parameter usually changes after high-temperature steps due to dopants diffusion. In week 4, the whole wafer is covered with either field oxide or gate oxide, and thus no electrical measurement can be performed on the wafer. How did you measure the doping concentration in week 4?

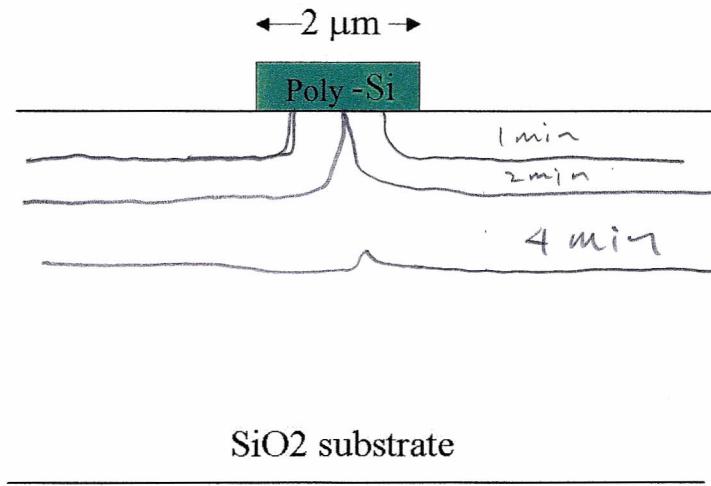
A control wafer is used. After oxidation, the control wafer oxide is stripped in HF and 4 point probe measures sheet resistance. Doping concentration is calculated from sheet resistance.

- d. At the end of the active region lithography step, you measured the linewidth under microscope. The linewidth is larger than the design value in the etched region. List three possible reasons that might cause this.

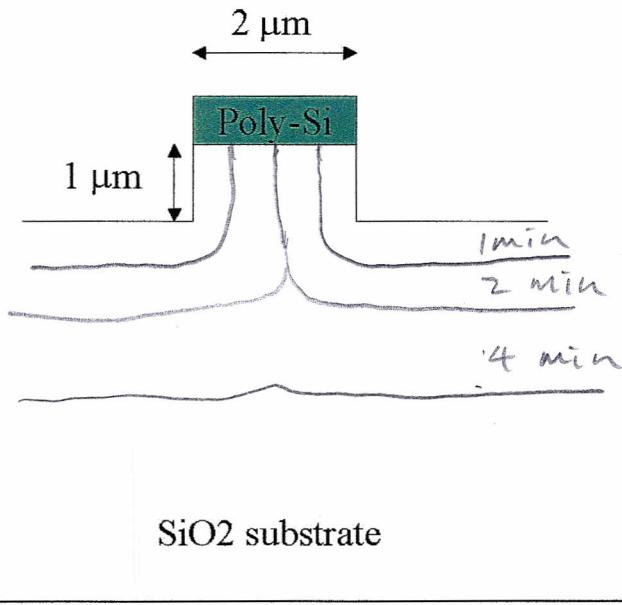
1. Over exposure
2. over development
3. over etch

4. Etching

- a. A poly-Si line is patterned on top of a SiO<sub>2</sub> substrate. We will release it from the oxide substrate to form a cantilever beam by etching the oxide underneath with buffered HF solution. The etching recipe has a vertical etching rate of 0.5 micron/minute and the degree of anisotropy is 0 (i.e. completely isotropic). Sketch the cross sections of the oxide after HF etching times = 1 min, 2 min, and 4 min.



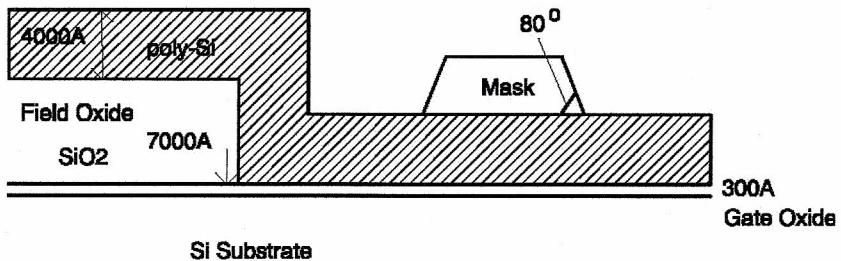
- b. A better way to release the Poly-Si beam is to use an anisotropic RIE process to etch the oxide first to a depth of 1  $\mu\text{m}$ . The same buffer HF solution recipe in part (i) is then used to release the poly-Si beam. Sketch the cross sections of the oxide after HF etching times = 1 min, 2 min, and 4 min.



c. Comment on why Method (b) is better than Method (a).

- at release time 2 min method b has a larger gap
- method b takes less etch time to clear a given gap under the beam

- d. The following cross-section shows a 4000 Å-thick poly-Si deposited over a field oxide of step height of 7000 Å which lies on top of a gate oxide with thickness 300 Å.



Given:

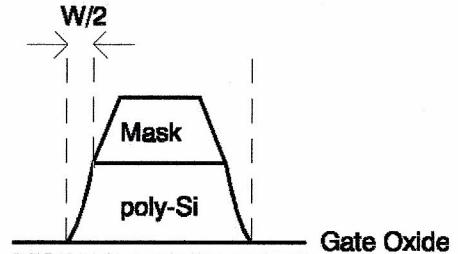
Poly etch degree of anisotropy anisotropy  $A_f = 1$

Poly-Si thickness variation factor  $\delta = 0.03$

Poly-Si etch rate variation factor  $\phi_f = 0.05$

Mask slope angle  $\theta = 80^\circ$

Mask etch degree of anisotropy  $A_m = 1$



The worst-case design goal is to control the poly-gate linewidth reduction on the top to less than 0.1 μm (*i.e.*  $W < 0.1 \mu\text{m}$ ) when the poly-Si is just cleared. [See schematic figure shown above]

**Find the required minimum etching selectivity between the poly and mask ( $S_{fm}$ ).**

$$A \equiv \frac{h_1}{h_2} = \frac{7000}{4000} = 1.75 \quad h_f = 0.4 \mu\text{m}$$

$$\frac{W}{2} = \frac{v_{m\perp}}{J_c} h_f \frac{(1+\delta)(1+A)}{1-\phi_f} \left[ \cot \theta + \frac{v_{m\parallel}}{v_{m\perp}} \right]$$

$$0.05 \mu\text{m} = S \cdot 0.4 \frac{(1+0.03)(2.75)}{0.95} \left[ \cot 80^\circ + \right]$$

$$0.05 = 0.174 S^{-1}$$

$$S > \frac{1}{17.4} \mu\text{m}^{-1}$$

5. Oxidation

A furnace with the following A and B parameters is used for the following oxidation steps.

$$B = 0.529 \text{ } \mu\text{m}^2/\text{hr}$$

$$B/A = 2.90 \text{ } \mu\text{m}/\text{hr}$$

$$\text{Temperature} = 1100 \text{ C}$$

- a. A Si wafer is placed in this furnace for 3 hrs. What is the thickness of the oxide grown? Assume there is no oxide present before the oxidation.

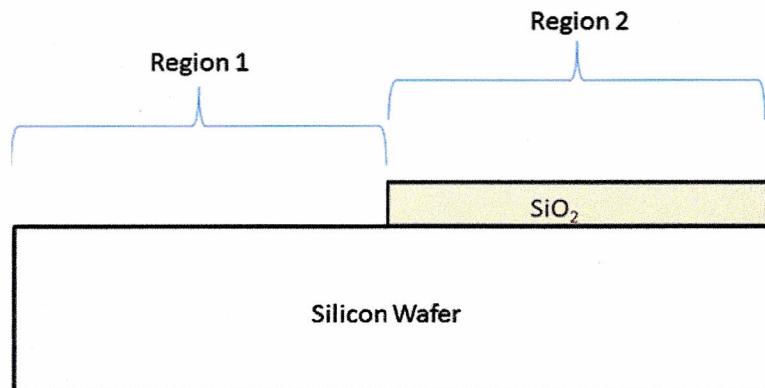
$$X = \frac{A}{2} \left\{ \left[ 1 + \frac{4B}{A^2} (t + \tau) \right]^{1/2} - 1 \right\}$$

$$A = \frac{0.529}{2.9} = 0.1824$$

$$t = 3 \quad \tau = 0$$

$$X = 1.172 \text{ } \mu\text{m}$$

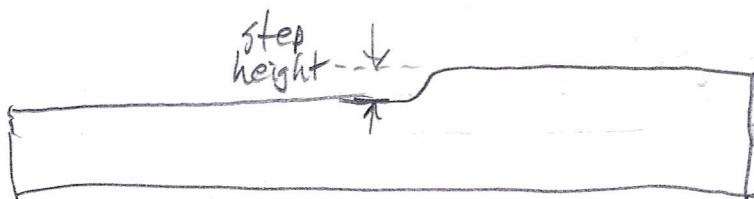
- b. Half of the wafer (Region 1) is stripped of the oxide grown in the previous step, resulting in a structure shown below. The wafer is then placed back into the furnace with the same growth conditions for 30mins. What is the resulting oxide thickness in Region 1 and Region 2?



Region 1:  $t = 0.5 \text{ } \mu\text{m}$   $\lambda = 0.43 \mu\text{m}$

Region 2:  $t = 3.5 \text{ } \mu\text{m}$   $\lambda = 1.27 \mu\text{m}$

- c. After the oxidation, the oxide is stripped from both regions of the wafer using an HF etch. Sketch the profile that results and calculate the step height.



From lecture  
for every  $1\mu\text{m}$  of Si oxidized,  
 $2.17\mu\text{m}$  of oxide is grown.  
So for  $1\mu\text{m}$  of oxide,  $0.46\mu\text{m}$   
silicon is consumed. Region 2: additional  $0.1\mu\text{m}$   
oxide is grown

$$\text{Region 1 } 0.46 \cdot 0.43\mu\text{m} = 0.198\mu\text{m}$$

$$\text{Region 2 } 0.46 \cdot 0.1\mu\text{m} = 0.046\mu\text{m}$$

$$\text{Step is then } 0.198 - 0.046 = \underline{\underline{0.152\mu\text{m}}}$$