

NTS4409N, NVS4409N

**MOSFET – Single,
N-Channel, Small Signal,
ESD Protection,
SC-70/SOT-323
25 V, 0.75 A**

Features

- Advance Planar Technology for Fast Switching, Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- AEC-Q101 Qualified and PPAP Capable – NVS4409N
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Boost and Buck Converter
- Load Switch
- Battery Protection

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	25	V
Gate-to-Source Voltage			V_{GS}	± 8.0	V
Drain Current	$t < 5 \text{ s}$	$T_A = 25^\circ\text{C}$	I_D	0.75	A
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	0.7	A
		$T_A = 75^\circ\text{C}$		0.6	
Power Dissipation (Note 1)	Steady State		P_D	0.28	W
Power Dissipation (Note 1)	$t \leq 5 \text{ s}$		P_D	0.33	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$		I_{DM}	3.0	A
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode) (Note 1)	I_S		I_S	0.3	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L		T_L	260	$^\circ\text{C}$
ESD Rating – Machine Model				25	V

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	450	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 5 \text{ s}$ (Note 1)	$R_{\theta JA}$	375	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 in sq pad size
(Cu area = 1.127 in sq [1 oz] including traces).

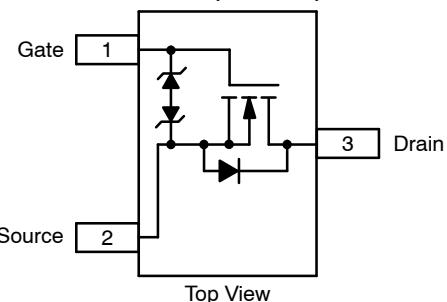


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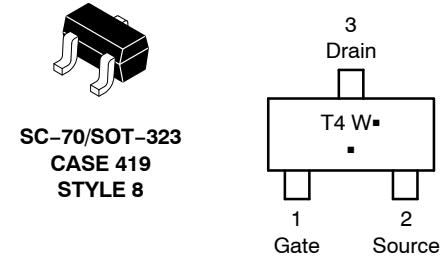
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)} \text{ Typ}$	$I_D \text{ Max}$
25 V	249 mΩ @ 4.5 V	0.75 A
	299 mΩ @ 2.7 V	

SC-70 (3-Leads)



MARKING DIAGRAM & PIN ASSIGNMENT



T4 = Device Code
W = Work Week
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NTS4409NT1G	SOT-323 (Pb-Free)	3000 / Tape & Reel
NVS4409NT1G	SOT-323 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit	
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}, I_D = 250 \mu\text{A}$	25			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(\text{BR})\text{DSS}}/T_J$			30		$\text{mV}/^\circ\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 20 \text{ V}$	$T_J = 25^\circ\text{C}$		0.5	μA	
			$T_J = 70^\circ\text{C}$		2.0		
			$T_J = 125^\circ\text{C}$		5.0		
Gate-to-Source Leakage Current	I_{GSS}	$V_{\text{DS}} = 0 \text{ V}, V_{\text{GS}} = 8.0 \text{ V}$			100	nA	
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{\text{GS}(\text{TH})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250 \mu\text{A}$	0.65		1.5	V	
Negative Threshold Temperature Coefficient	$V_{\text{GS}(\text{TH})}/T_J$			-2.0		$\text{mV}/^\circ\text{C}$	
Drain-to-Source On Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 4.5 \text{ V}, I_D = 0.6 \text{ A}$		249	350	$\text{m}\Omega$	
		$V_{\text{GS}} = 2.7 \text{ V}, I_D = 0.2 \text{ A}$		299	400		
		$V_{\text{GS}} = 4.5 \text{ V}, I_D = 1.2 \text{ A}$		260			
Forward Transconductance	g_{FS}	$V_{\text{DS}} = 5.0 \text{ V}, I_D = 0.5 \text{ A}$		0.5		S	
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	$V_{\text{GS}} = 0 \text{ V}, f = 1.0 \text{ MHz}, V_{\text{DS}} = 10 \text{ V}$		49	60	pF	
Output Capacitance	C_{OSS}			22.4	30		
Reverse Transfer Capacitance	C_{RSS}			8.0	12		
Total Gate Charge	$Q_{\text{G}(\text{TOT})}$	$V_{\text{GS}} = 4.5 \text{ V}, V_{\text{DS}} = 15 \text{ V}, I_D = 0.8 \text{ A}$		1.2	1.5	nC	
Threshold Gate Charge	$Q_{\text{G}(\text{TH})}$			0.2			
Gate-to-Source Charge	Q_{GS}			0.28	0.50		
Gate-to-Drain Charge	Q_{GD}			0.3	0.40		
SWITCHING CHARACTERISTICS (Note 3)							
Turn-On Delay Time	$t_{\text{d}(\text{ON})}$	$V_{\text{GS}} = 4.5 \text{ V}, V_{\text{DS}} = 15 \text{ V}, I_D = 0.7 \text{ A}, R_G = 51 \Omega$		5.0	12	ns	
Rise Time	t_r			8.2	8.0		
Turn-Off Delay Time	$t_{\text{d}(\text{OFF})}$			23	35		
Fall Time	t_f			41	60		
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	$V_{\text{GS}} = 0 \text{ V}, I_S = 0.6 \text{ A}$	$T_J = 25^\circ\text{C}$		0.82	1.20	V

2. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

3. Switching characteristics are independent of operating junction temperatures.

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

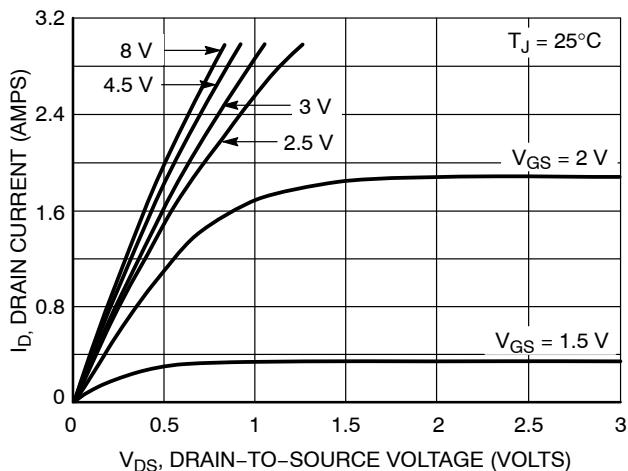


Figure 1. On-Region Characteristics

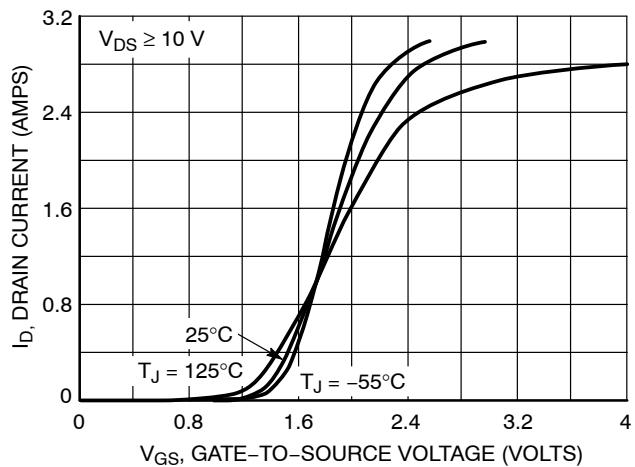


Figure 2. Transfer Characteristics

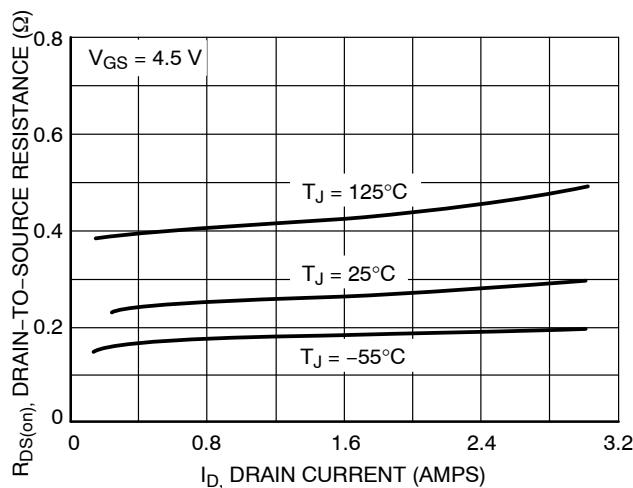


Figure 3. On-Resistance vs. Drain Current and Temperature

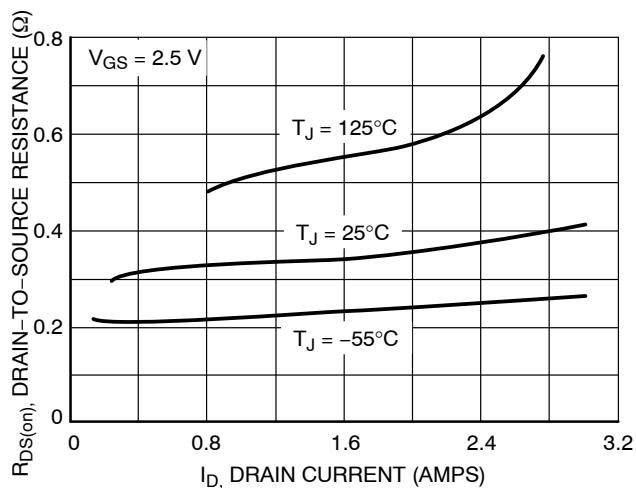


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

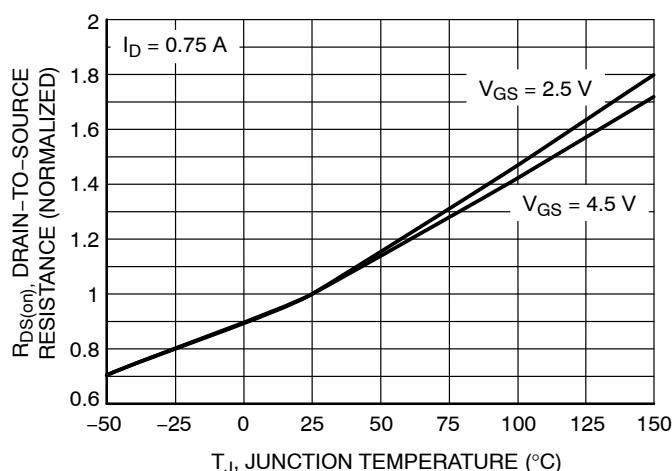


Figure 5. On-Resistance Variation with Temperature

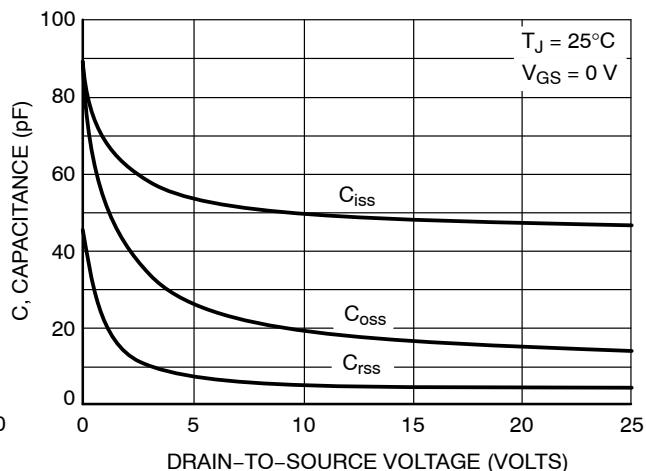


Figure 6. Capacitance Variation

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

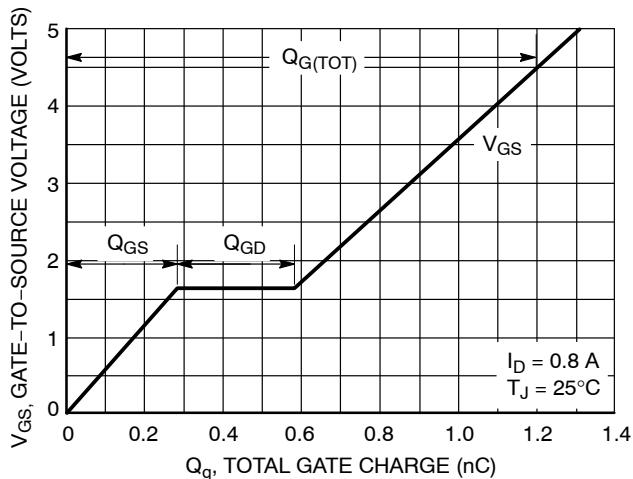


Figure 7. Gate-to-Source and
Drain-to-Source Voltage vs. Total Charge

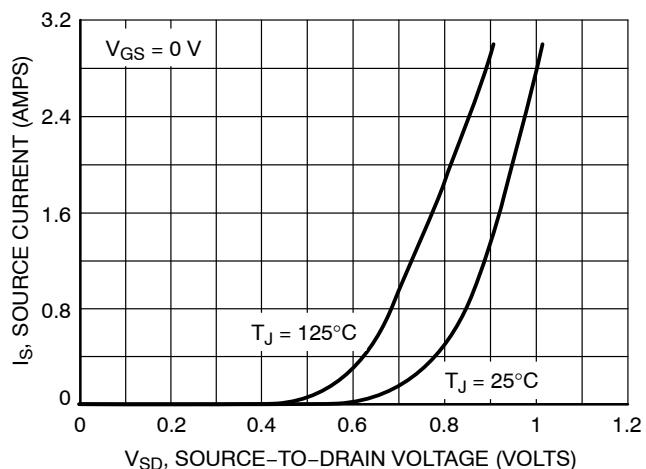
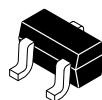


Figure 8. Diode Forward Voltage vs. Current

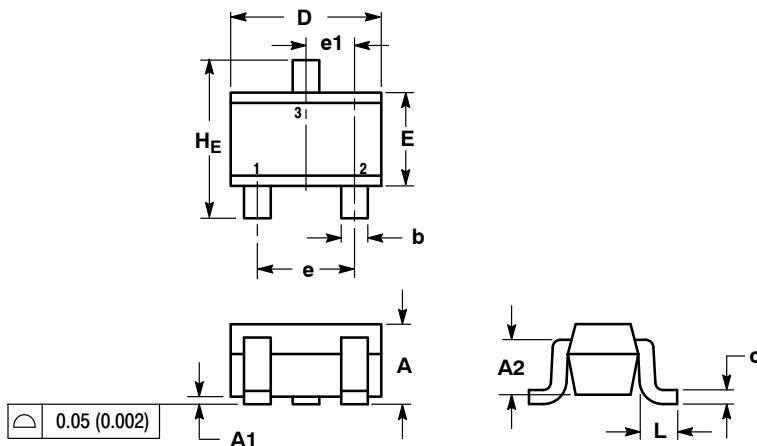
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 4:1



SC-70 (SOT-323)
CASE 419-04
ISSUE N

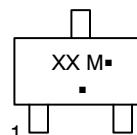
DATE 11 NOV 2008

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70 REF			0.028 REF		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.20	0.38	0.56	0.008	0.015	0.022
H_E	2.00	2.10	2.40	0.079	0.083	0.095

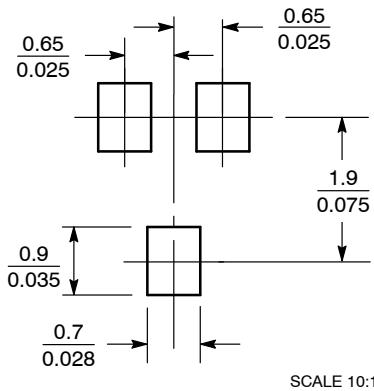
**GENERIC
MARKING DIAGRAM**



XX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*



SCALE 10:1 (mm)
(inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:
CANCELLED

STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE

STYLE 3:
PIN 1. BASE
2. Emitter
3. Collector

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 6:
PIN 1. Emitter
2. Base
3. Collector

STYLE 7:
PIN 1. BASE
2. Emitter
3. Collector

STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE-ANODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE-CATHODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

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DESCRIPTION:	SC-70 (SOT-323)	PAGE 1 OF 1

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