Analog voltage adder circuit using Op amp in 28 nm CMOS technology

Koushik Datta, National Institute of Technology, Agartala

Abstract

In this paper a design of analog voltage adder circuit adder circuit using Op amp has been shown. Besides, the circuit diagram, theoretical proof and estimated waveform has been shown. The adder circuit is used in different signal processing application in communication engineering.

Circuit details

First of all, a tow stage opamp has been designed, which is shown below.

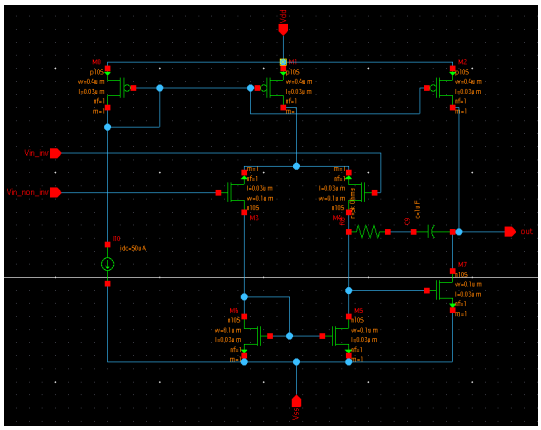

Fig. Two state Op amp designed using MOSFET

Practically the virtual ground concept isn't dominant. Thats why the calculations that we have done theoretically doesn't hold error free. The changes in the waveform show the same.

It is estimated that the current through the inverting and non inverting terminal of the op amp as zero, but in simulation there is non zero value exist.

Besided, in the circuit, Iref has 40uA current, the PMOS has total width of 0.4Um and length is 0.03um. And the NMOS has the total width of 0.1um and length of 0.03um. Vdd applied is 1.8V and Vss applied is -1.8V. In the complete circuit the Rf=R1=R2= 100K Ohm and at the output the 1pF capacitor is used. For the input, two constant voltage sources are used, one of 0.5V and other of 0.2V. The output was estimated at 0.7V. But the obtained output voltage is 0.74V.

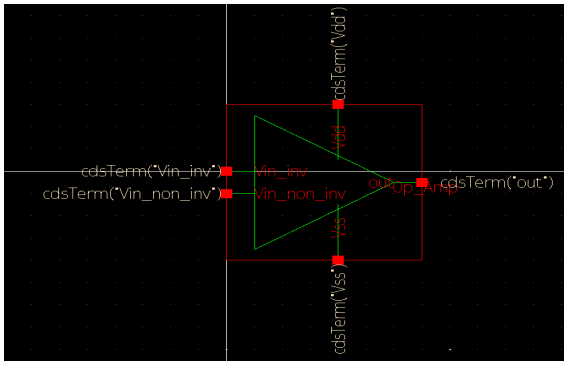

Fig. Symbol of Op amp created

Circuit design

The complete circuit is shown below.

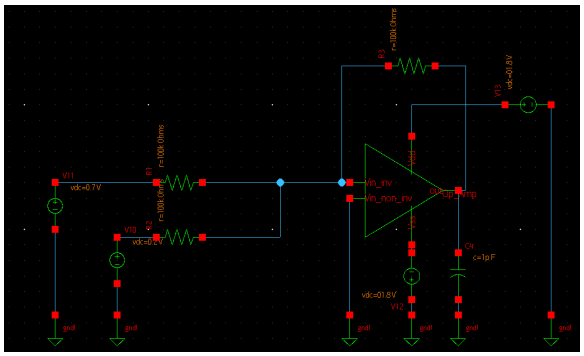

Fig Designed Circuit

Waveform

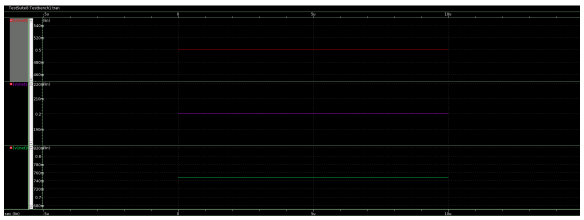

Fig Obtained Waveform

References

1. https://www.tutorialspoint.com/linear_integrated_circuits_applications/linear_integrated_circuits_applications_arithmetic_circuits.htm
2. Optimal Design of a CMOS Op-Amp via Geometric Programming - Maria del Mar Hershenson et al.