Western University
Faculty of Engineering
Department of Electrical and Computer Engineering

ECE 2277A: Digital Logic Systems

Course Outline 2024-2025

Course Description: This course introduces students to design and analysis of digital electronic devices. Students will learn fundamental concepts of digital systems and apply those concepts to design problems. Three themes are emphasized: representation of digital processes using algorithms, a modular approach to design by partitioning complex systems into subsystem hierarchies, and hardware implementation and use of programmable devices.

Academic Calendar: Theory of Boolean algebra, switching circuits, Venn diagrams; Karnaugh maps; logic and memory systems, design of combinational and sequential switching machines; electronic switching circuits; data coding, storage, transmission; basic design of digital computers.

Antirequisite: the former ECE3339A/B

Prerequisites: Physics 1302 A/B or Physics 1402A/B or the former Physics 1026.

Corequisite(s): ECE 2205A/B or registration in Integrated Engineering or Software Engineering Program.

Unless you have either the requisites for this course or written special permission from your Dean to enroll in it, you will be removed from this course and it will be deleted from your record. This decision may not be appealed. You will receive no adjustment to your fees if you are dropped from a course for failing to have the necessary prerequisites.

CEAB Academic Units: Engineering Science 75%, Engineering Design 25%.

Instructors: Dr. Anestis Dounavis (Section 1)
TEB 253, 519-661-2111 ext. 81255, adounavi@uwo.ca
Consultation hours: By appointment, in person or via Zoom

Dr. Arash Reyhani-Masoleh (Section 2)
TEB 243, 519-661-2111 ext. 81253, areyhani@uwo.ca
Consultation hours: By appointment, in person or via Zoom.

Dr. Raveendra K. Rao (Section 3)
ACEB 4457, 519-661-2111 ext. 88231, rrao@uwo.ca
Consultation hours: By appointment, in person or via Zoom

Contact Hours:

Timetable information is available at https://draftmyschedule.uwo.ca/.

LECTURE:	3 lecture hours per week
LABORATORY:	3 laboratory exercises and 1 project: each of duration 3 hours
TUTORIAL:	1 tutorial hour per week

Required Textbook: M.M. Mano and M.D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog*, 6th ed., Pearson, 2018, ISBN: 9780134549897.
Please note that there are three options for purchasing the textbook from Western's bookstore:

- A traditional printed copy (ISBN 9780134549897).
- An electronic copy with a perpetual digital license (ISBN 9780134529578). This provides you with electronic access to the textbook for the rest of your life.
- An electronic copy with a subscription digital license (ISBN 9780134529561). This is the least expensive option and provides you with electronic access to the textbook for 180 days. (Longer if you renew your subscription.)

It is only required to purchase the textbook using **one** of these options.

Other Required References: Laboratory manuals and relevant documents will be made available on the course website.

Recommended References: Links would be provided on the course website.

General Learning Objectives (CEAB Graduate Attributes)

Knowledge Base	I	Use of Engineering Tools	I	Impact on Society and the Environment	
Problem Analysis	I	Individual and Team Work		Ethics and Equity	
Investigation		Communication Skills		Economics and Project Management	
Design	D	Professionalism		Life-Long Learning	

Notation*: I: Introductory, D: Intermediate, A: Advanced, or empty*. I – The instructor will introduce the topic at the level required. It is not necessary for the student to have seen the material before. D – There may be a reminder or review, but the student is expected to have seen and been tested on the material before taking the course. A – It is expected that the student can apply the knowledge without prompting (e.g. no review).

Course Material: All course material including lecture slides by instructors, laboratory exercises and guides and supplementary material will be posted to the course website.

Course Topics and Specific Learning Outcomes	CEAB Graduate Attributes Indicators
1. Digital Number Systems	
At the end of this section, students will be able to:	
a. Express numbers in binary, octal, and hexadecimal representations and convert between those number systems and the decimal system.	**PA 1**
b. Obtain signed magnitude, one's-complement, and two's-complement representations of signed numbers and perform arithmetic in each of those formats.	**PA 1**
2. Boolean Algebra and Logic Gates	
At the end of this section, students will be able to:	
a. Use the postulates of Boolean algebra to verify complex Boolean expressions.	**PA 1**
b. Derive a Boolean expression for a logic function given a schematic diagram of a digital circuit that implements the expression.	**PA 1, KB 3**
3. Gate-Level Minimization	
At the end of this section, students will be able to:	
a. Use Karnaugh maps and postulates of Boolean algebra to derive optimal implementations of digital logic circuits.	**PA 2, KB 3**
b. Implement logic functions using a constrained set of logic gates.	**PA 2, PA 3**
4. Combinational Circuits	
At the end of this section, students will be able to:	
a. Define the logic functions performed by fundamental combinational circuits (multiplexers, encoders, decoders, etc.).	**PA 1, KB 3**
b. Use fundamental combinational circuit blocks to design and implement circuits that realize more complex functions.	**PA 2, PA 3**
5. Synchronous Sequential Circuits	
At the end of this section, students will be able to:	
a. Define three types of synchronous flip-flop (D, T, and JK) and give their characteristic and excitation tables.	**PA 1**
b. Differentiate between Mealy- and Moore-model sequential circuits.	**PA 1, KB 3**
c. Design and implement a synchronous state machine to perform a sequential logic function given a word description, block diagram, and/or timing diagram of the function.	**PA 2, PA 3, KB 3, D 2, D 4**
d. Minimize the number of states realized by a synchronous state machine.	**PA 2, KB 3**
6. Registers and Counters	
At the end of this section, students will be able to:	

a. Define the purpose and function of fundamental sequential circuits (counters, registers, shift registers, etc.).	**PA 1**
b. Design and implement synchronous sequential circuits using state machine methods and fundamental sequential circuit blocks.	**PA 2, PA 3, KB 3**
7. Implementation of Digital Circuits (Laboratory Exercise)	
At the end of the laboratory exercises, students will be able to:	
a. Create and verify digital circuit designs using industry-standard design software.	**PA 2, ET 2, D 2, D 4**
b. Implement and test digital circuits using an FPGA-based development board.	**PA 3, ET 2, D 2, D 4**

Evaluation:

Course Component	Weight	CEAB GAs ASSESSED
Laboratory Exercises (3)	20%	PA1, PA2, PA3, KB3, ET2
Project	10%	PA1, PA2, PA3, ET2, D2, D4
Midterm	25% / 0%	PA1, PA2, PA3, KB3
Final examination	45% / 70%	PA1, PA2, PA3, KB3

To obtain a passing grade in the course, a mark of 50% or more must be achieved on the final examination, laboratory exercises, and project components of the course. A final examination or laboratory exercises or project mark of < 50% will result in a final course grade of 48% or less.

For the midterm test and final examination, the **greater** (25% midterm + 45% final) or (0% midterm + 70% final) will be used to evaluate each student's grade.

Laboratory: Three laboratory experiments are to be performed in this course. Information will be posted to the course website well in advance of the laboratory sessions. Laboratory exercises consist of designing logic circuits in software, which can be done prior to attending the laboratory session, and then implementing and testing that circuit on a FPGA development board during the laboratory session. Students must submit a laboratory report by the end of the laboratory session. Attendance in the laboratory and project sessions is mandatory.

Project: Students will be required to design, build, and test a logic circuit on the FPGA development board and write a report. The details of the design requirements for this project will be distributed in class, at least two weeks before the report and circuit demonstration is due.

Midterm Test: The midterm test will be held on Friday the November 1st, 2024, from 3:45 to 5:15 PM. The midterm test is expected to be an **in-person** and a **closed-book** test. A non-programmable calculator may be used, but use of any other electronic devices is not permitted during the test. The midterm test is **optional** and if students do not complete the midterm, the weight of midterm will be added to the weight of the final examination. If students do complete the midterm but achieve a higher grade on the final examination than on the midterm, the final examination grade will be used instead.

Final Examination: The final examination will take place during the regular examination period. The final examination is expected to be an **in-person** and a **closed-book** exam. A non-programmable calculator may be used, but use of any other electronic devices is not permitted during the examination.

Late Submission Policy: Laboratory reports should be submitted before leaving the laboratory session, and project reports should be submitted after demonstrating the circuit. Late submission of these reports is not accepted.

Use of English: In accordance with Senate and Faculty Policy, students may be penalized up to 10% of the marks on all assignments, tests, and examinations for improper use of English. Additionally, poorly written work except for the final examination may be returned without grading. If resubmission of the work is permitted, it may be graded with marks deducted for poor English and/or late submission.

Attendance: All laboratories are mandatory unless otherwise stated. Any student who, in the opinion of the instructor, is absent too frequently from class or laboratory periods will be reported to the Dean (after due warning has been given). On the recommendation of the department, and with the permission of the Dean, the student will be debarred from taking the regular final examination in the course.

Online Activities: The course website will be extensively used in delivering course content including announcements, and lesson slides. Some pre-recorded video lessons from previous years' remote course delivery may be made available as learning aids and to supplement in-class activities. Public distribution of lecture materials including course notes, slides, and video lessons is not permitted.

COVID-19 Contingency Clause: In the event of a COVID-19 resurgence during the course that necessitates the course delivery moving away from face-to-face interaction, all remaining course content will be delivered entirely online, either synchronously (i.e., at the times indicated in the timetable) or asynchronously (e.g., posted on OWL for students to view at their convenience). The grading scheme will not change. Any remaining assessments will also be conducted online at the discretion of the course instructor.

Absence Due to Illness or Other Circumstances: Students should immediately consult with the instructor or department Chair if they have any problems that could affect their performance in the course. Where appropriate, the problems should be documented (see the attached "Instructions for Students Unable to Write Tests or Examinations or Submit Assignments as Scheduled"). The student should seek advice from the instructor or department Chair regarding how best to deal with the problem. Failure to notify the instructor or department Chair immediately (or as soon as possible thereafter) will have a negative effect on any appeal.

For more information concerning medical accommodations, see the relevant section of the Academic Handbook:
http://www.uwo.ca/univsec/pdf/academic_policies/appeals/accommodation_medical.pdf

For more information concerning accommodations for religious holidays, see the relevant section of the Academic Handbook:
http://www.uwo.ca/univsec/pdf/academic_policies/appeals/accommodation_religious.pdf

Cheating and Plagiarism: Students must write their essays and assignments in their own words. Whenever students take an idea or a passage from another author, they must acknowledge their debt both by using quotation marks where appropriate and by proper referencing such as footnotes or citations. University policy states that cheating, including plagiarism, is a scholastic offence. The commission of a scholastic offence is attended by academic penalties, which might include expulsion from the program. If you are caught cheating, there will be no second warning.

All required papers may be subject to submission for textual similarity review to commercial plagiarism-detection software under license to the University for the detection of plagiarism. All papers submitted will be included as source documents on the reference database for the purpose of detecting plagiarism of papers subsequently submitted to the system. Use of the service is subject to the licensing agreement, currently between the University of Western Ontario and Turnitin.com (http://www.turnitin.com).

Scholastic offences are taken seriously and students are directed to read the appropriate policy, specifically, the definition of what constitutes a Scholastic Offence, in the relevant section of the Academic Handbook:
http://www.uwo.ca/univsec/pdf/academic_policies/appeals/scholastic_discipline_undergrad.pdf

Use of Electronic Devices: Not applicable.

Use of Personal Response Devices ("Clickers"): Not applicable.

Policy on Repeating All Components of a Course: Students who are required to repeat an Engineering course must repeat all components of the course. No special permissions will be granted enabling a student to retain laboratory, assignment, or test marks from previous years. Previously completed assignments and laboratories cannot be resubmitted by the student for grading in subsequent years.

Internet and Electronic Mail: Students are responsible for regularly checking their Western e-mail and the course web site (https://owl.uwo.ca/portal/) and making themselves aware of any information that is posted about the course.

Accessibility: Please contact the course instructor if you require material in an alternate format or if any other arrangements can make this course more accessible to you. You may also wish to contact Services for Students with Disabilities (SSD) at 519-661-2111 ext. 82147 for any specific question regarding an accommodation.

Support Services: Office of the Registrar, http://www.registrar.uwo.ca/
Student Development Centre, http://www.sdc.uwo.ca/
Engineering Undergraduate Services, http://www.eng.uwo.ca/undergraduate/
USC Student Support Services, http://westernusc.ca/services/

Students who are in emotional/mental distress should refer to Mental Health @ Western, http://www.health.uwo.ca/mental_health/, for a complete list of options about how to obtain help.