VL-731 VLSI Design Architecture

Paper Presentation

Low Power 19 Transistor Single True Phase Clocking Flip-Flop Design based on Logic Structure Reduction Techniques

Team Members

Kedar Deshpande IMT2020523

Aakash Khot IMT2020512

Anshul Madurwar IMT2020554

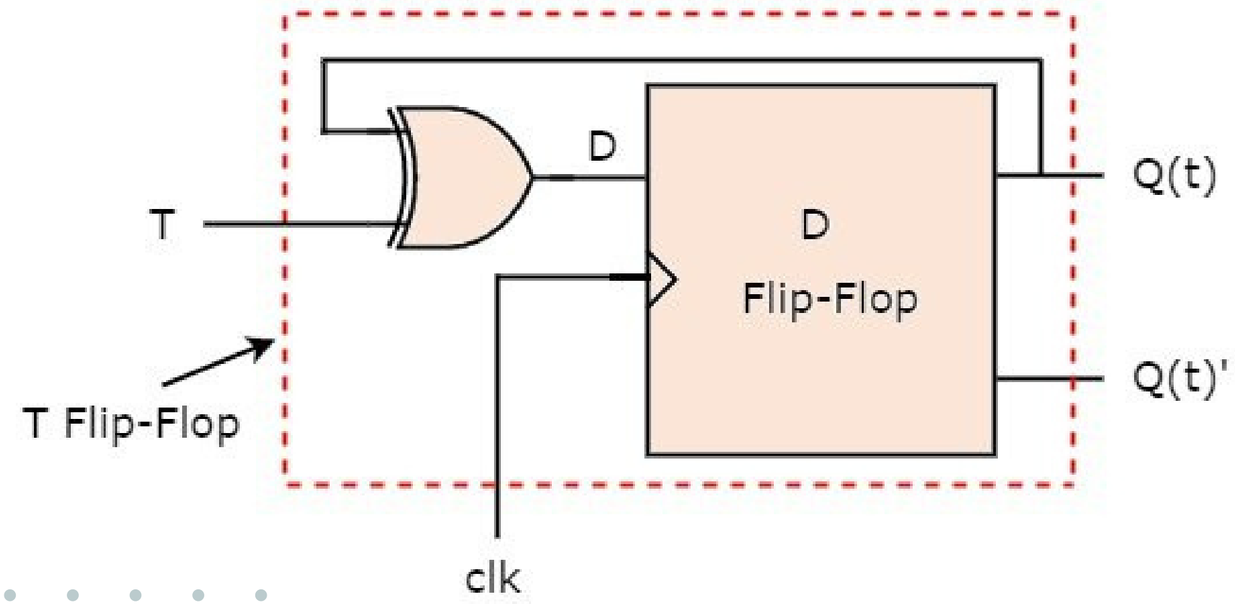
Anmol Shetty IMT2020551

TABLE OF CONTENTS

INTRODUCTION

THE FLIP-FLOP

Flip-flops are digital circuits used to store binary information. They are made up of logic gates for data transfer and storage. The output of a flip-flop depends on its current state and the state of its inputs. They are often used in combination with other digital circuits to implement more complex functions such as counters, shift registers, and memory elements.



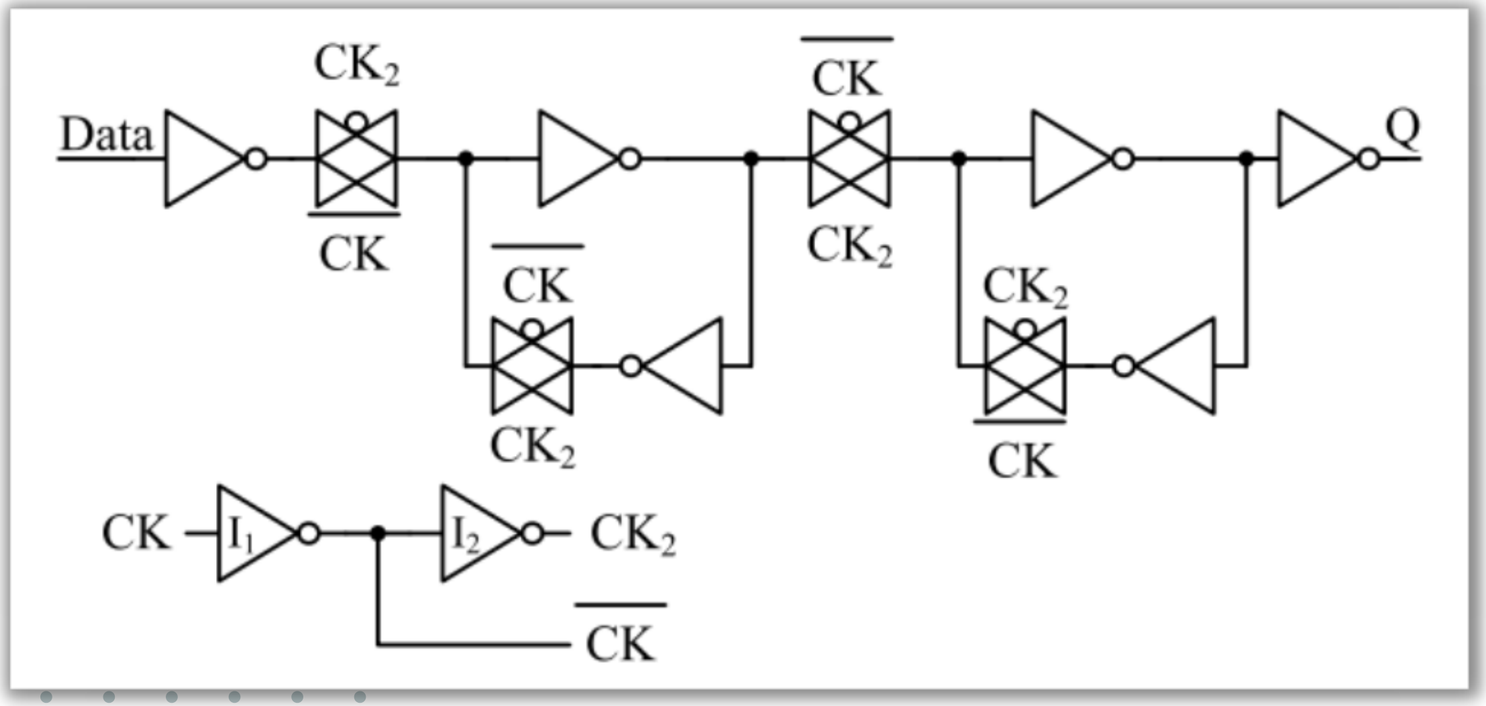
THE NEED FOR BETTER FLIP-FLOP DESIGNS

- FFs along with Clock Distribution Networks constitute as high as 20-45% of the total system power.
- Switch from Ultra High-Speed toggling to extremely Low-Power applications.
- Reduction of Switching and Leakage Power.
- Design must also function for voltage settings below the nominal voltage.
- Reduction of Layout Area
- Better Performance Metrics such as delay, PDP, etc.
- Reliable FF outputs that are not subjected to noise.

GENERIC FLIP-FLOP DESIGNS

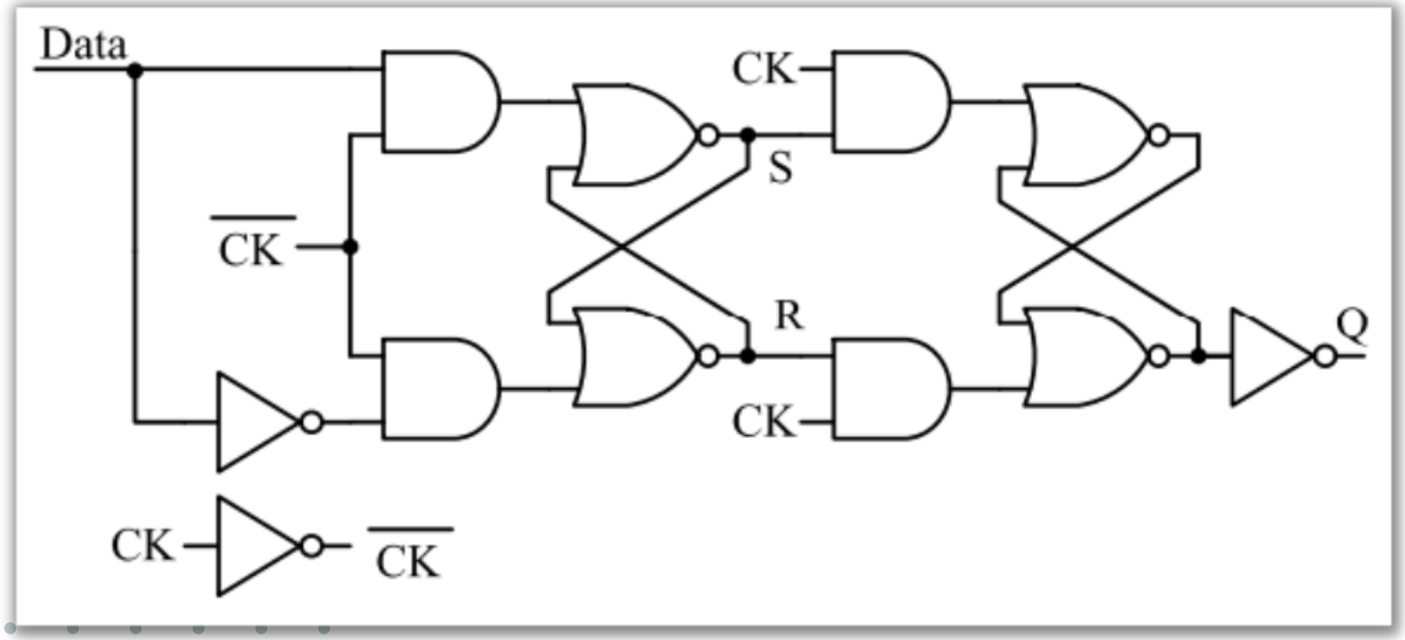
TRANSMISSION GATE FLIP–FLOP (TGFF)

- A master–slave-type design comprising of two TG-based latch designs.
- Excessive workload on CK signal.
- High dynamic power even when data-switching activity is low.
- Shorter setup time compared to their TSPC counterparts.



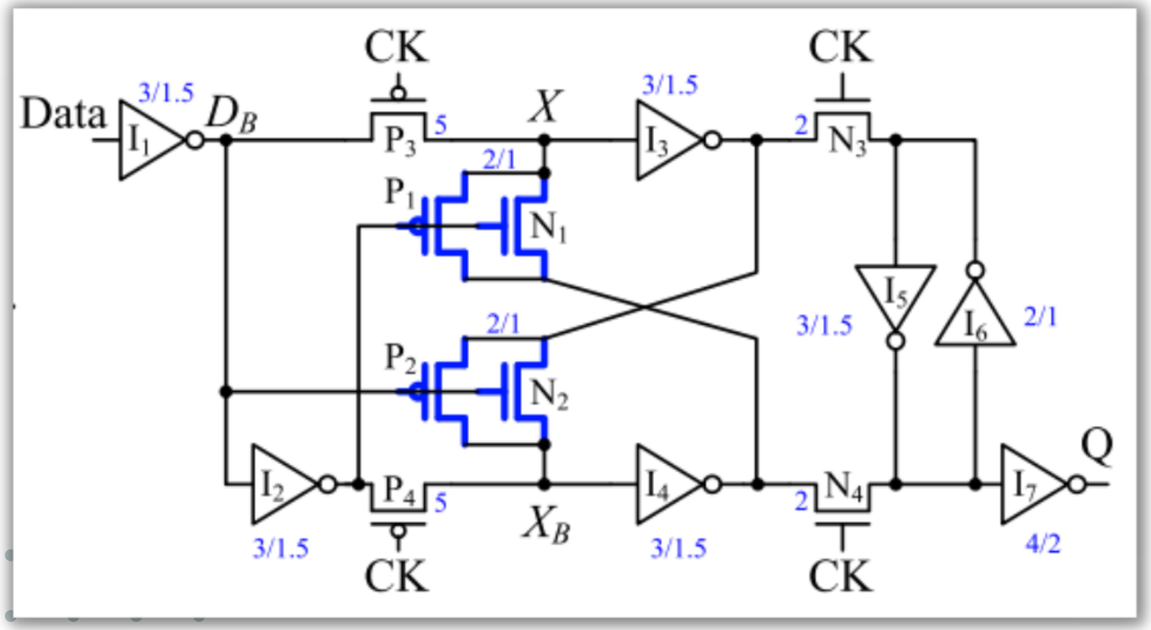
SET–RESET LATCH FLIP–FLOP (SRFF)

- A master–slave type circuit comprising SR-Latch-based design.
- Cross-coupled set-reset (SR) latches are used instead of the TG-based latch to support single-clock-phase operations to reduce clock signal loading.
- Shorter setup time compared to their TSPC counterparts.



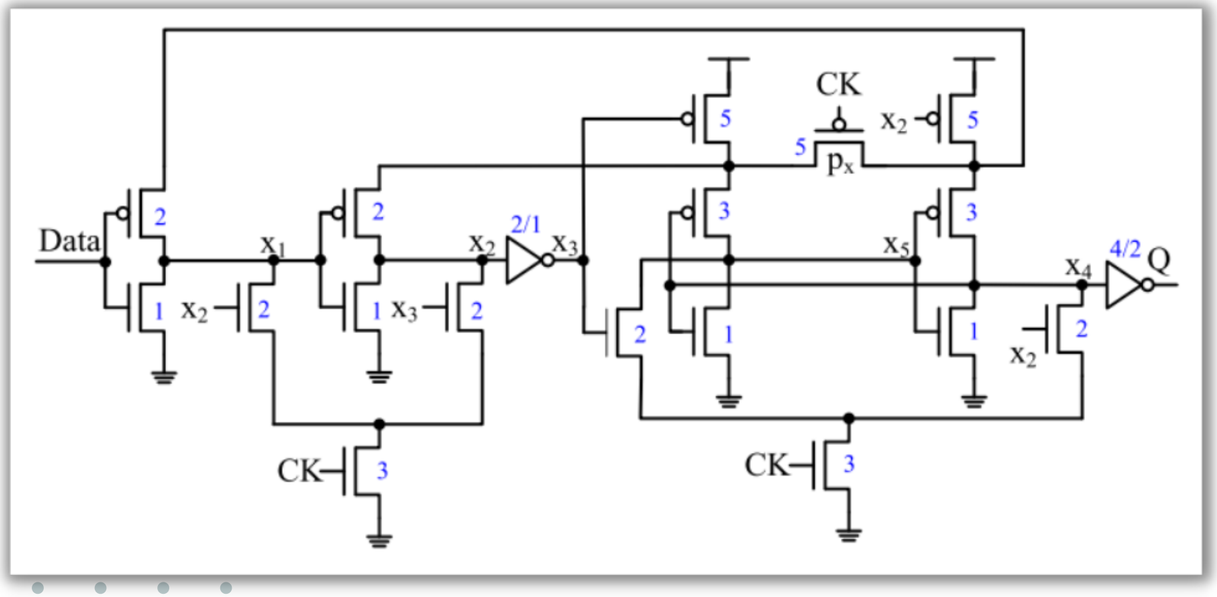
ADAPTIVE COUPLING FLIP–FLOP (ACFF)

- A differential latch structure with pass-transistor logic to achieve TSPC operation.
- A single channel TG with an additional dynamic circuit has been used for the data line in order to reduce clock-related transistor count.
- Level restoring circuits to avoid process variations. But they result in longer setup time.
- Power Leakage during certain input node combinations.

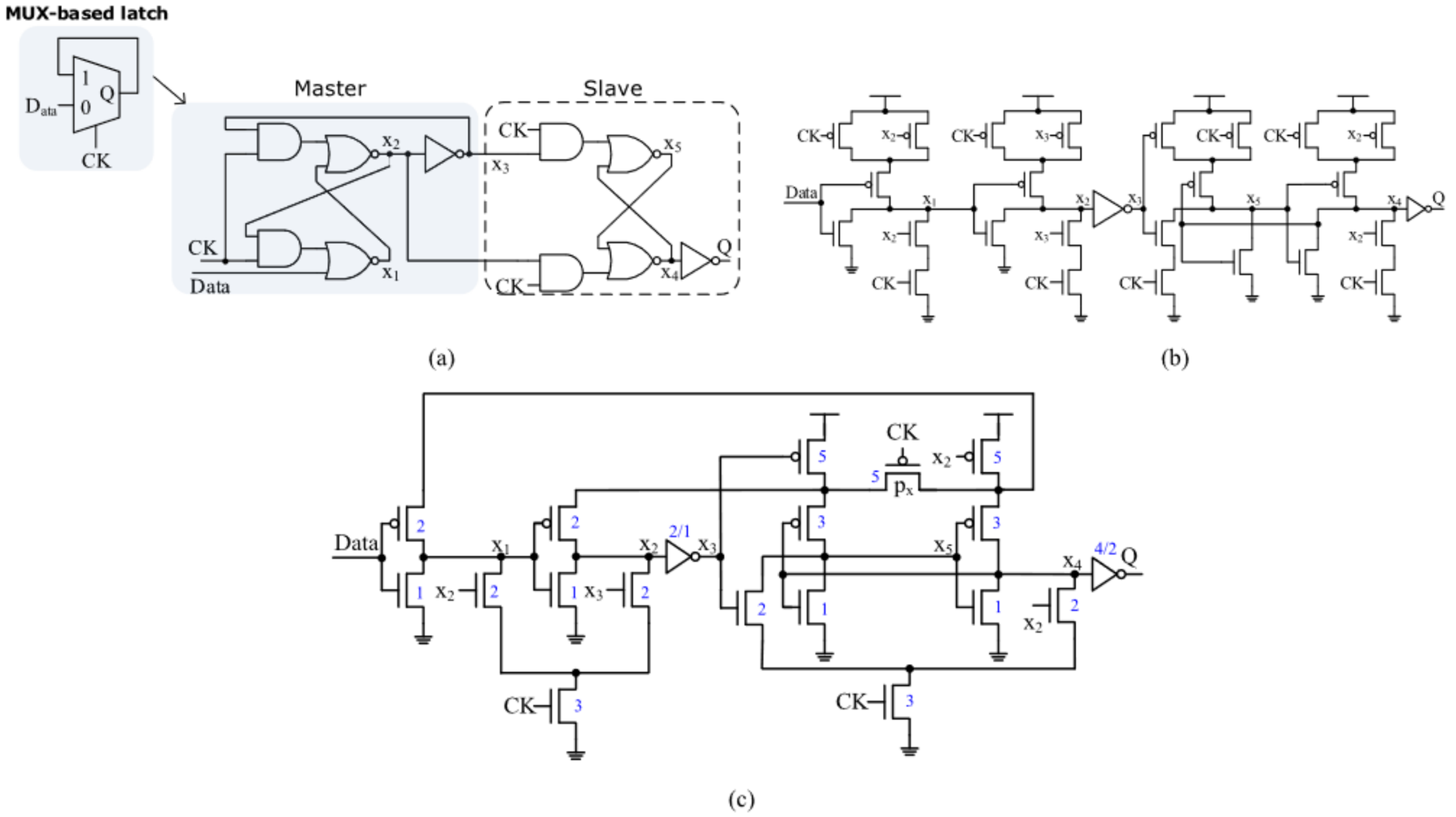


TOPOLOGICALLY COMPRESSED FLIP-FLOP (TCFF)

- The Master and the Slave Latches have a MUX configuration with feedback which is mapped to two AND-OR-Invert (AOI) gates and an inverter.
- Fully static design despite aggressive simplifying of logic.
- Longer setup time from a weakened pull-up network. The critical path consists of three pMOS transistors connected in series.
- Showed one of the highest performance in terms of the CQ delay.



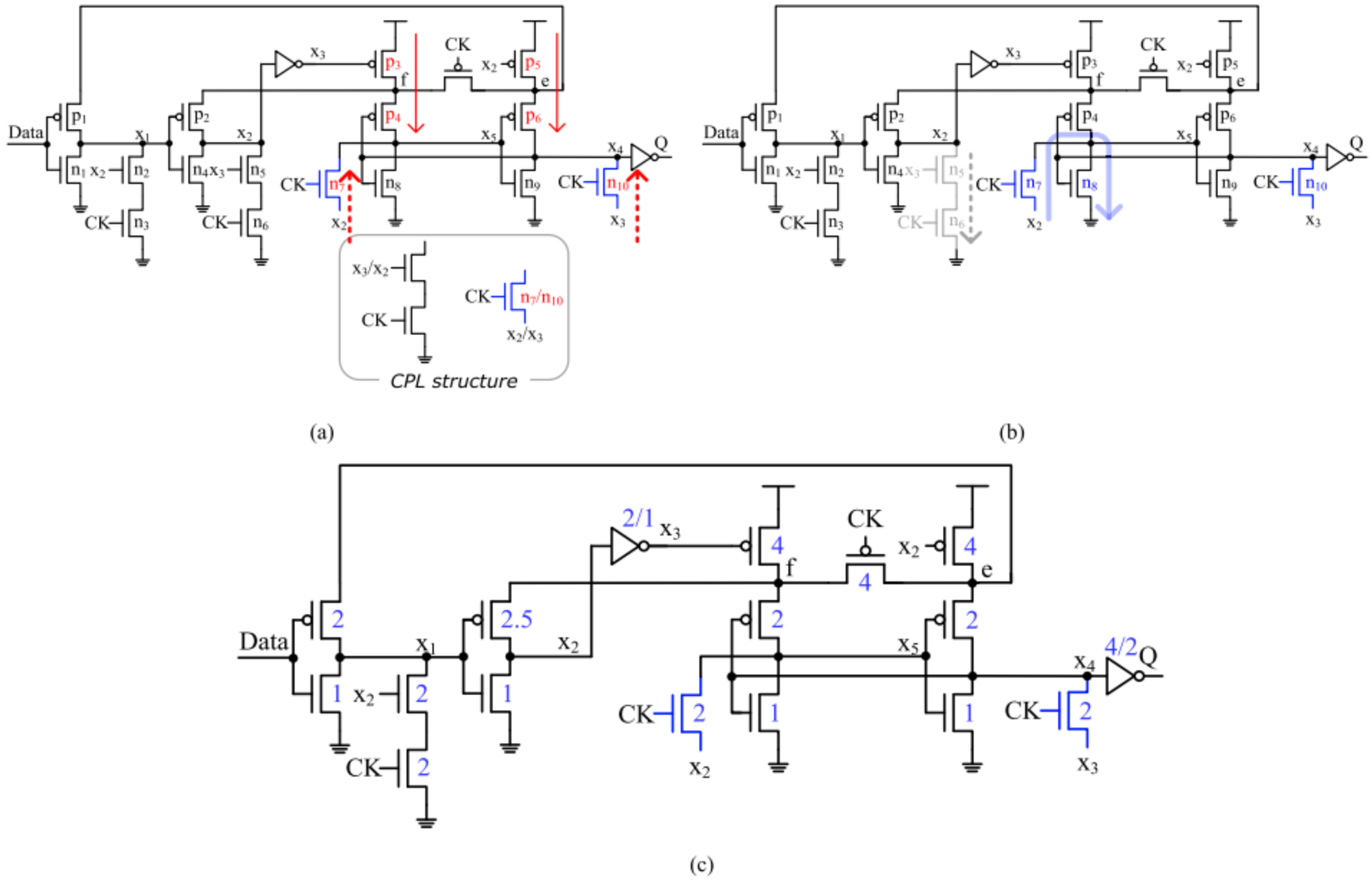
CIRCUIT OPTIMIZATION OF TCFF



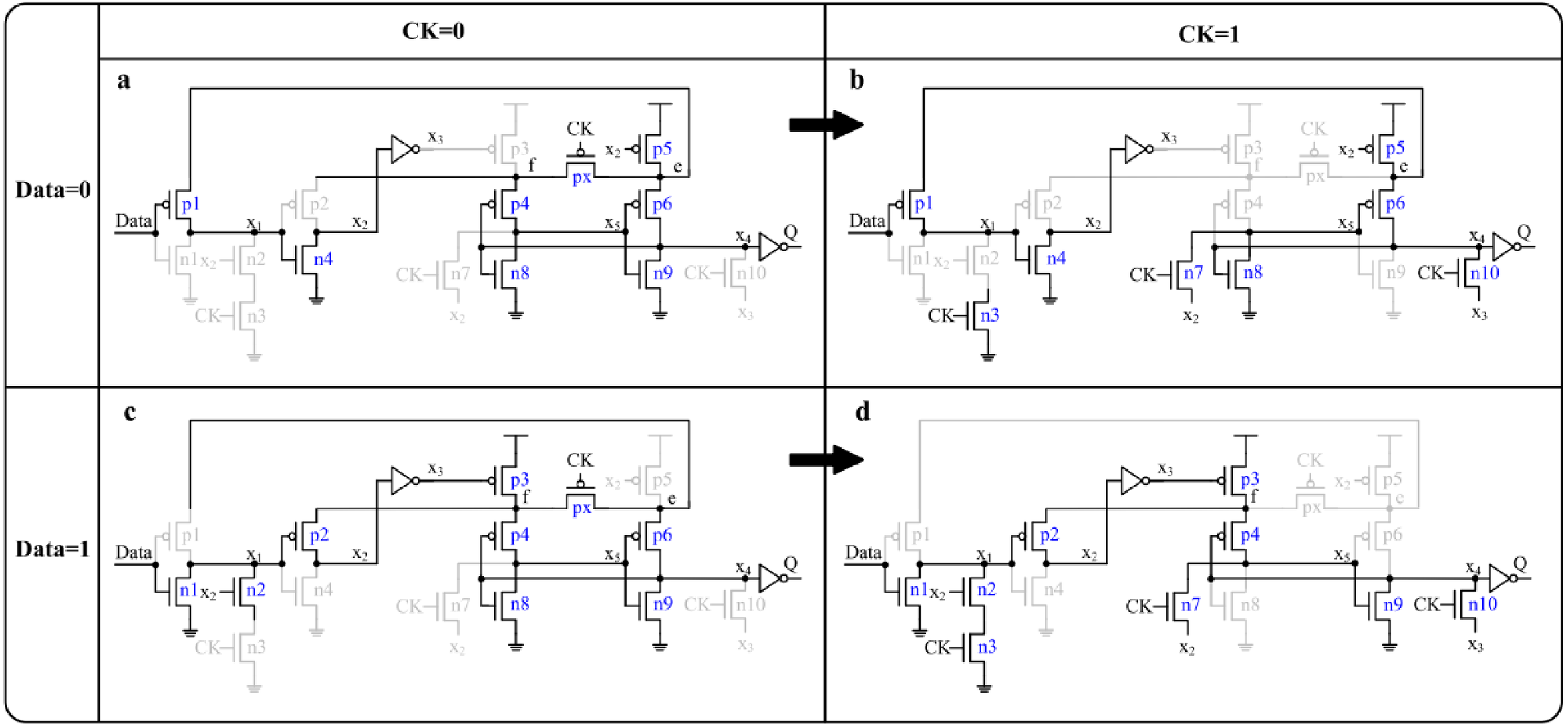
PROPOSED DESIGN

LOGIC STRUCTURE REDUCTION FLIP-FLOP (LRFF)

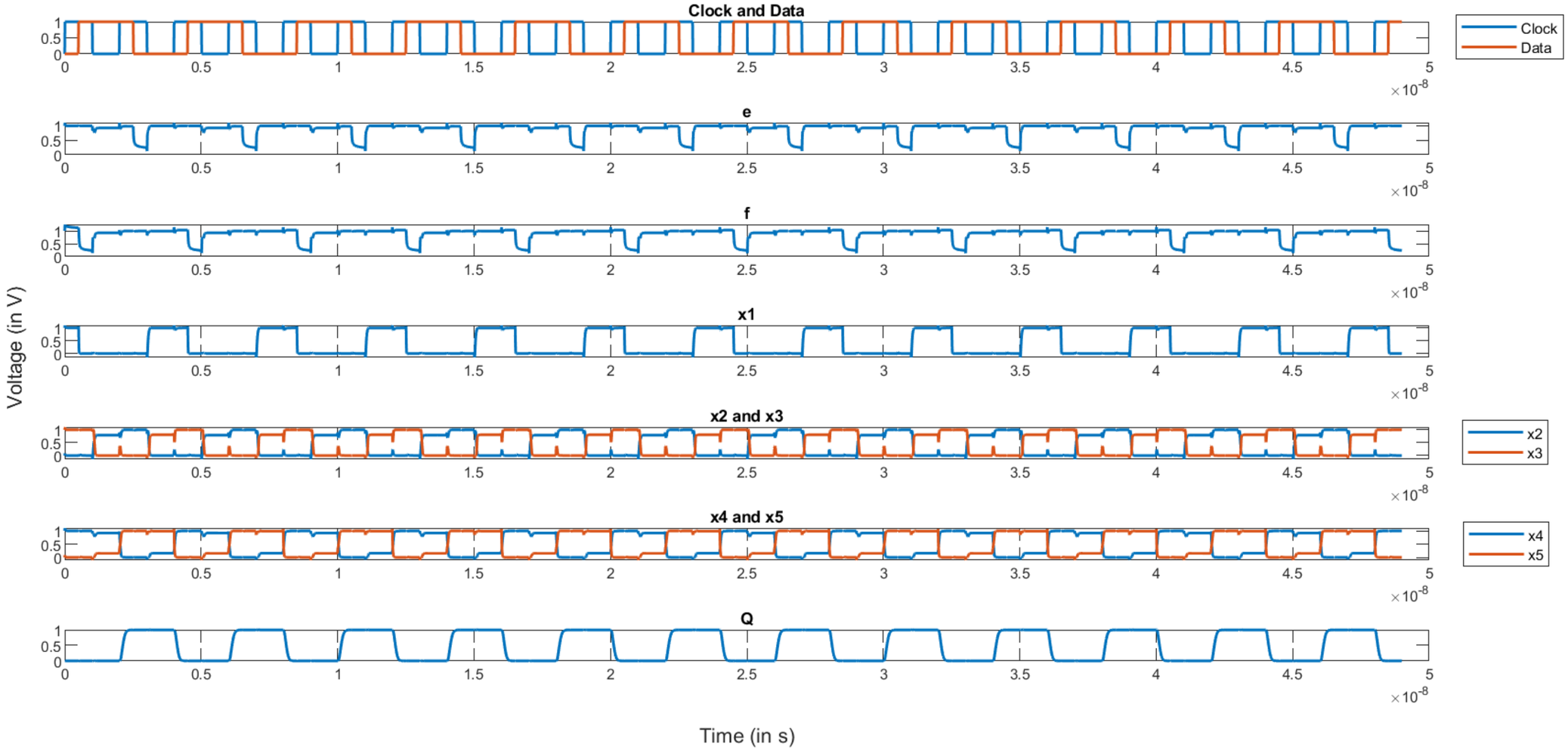
Design Derivation of LRFF from TCFF



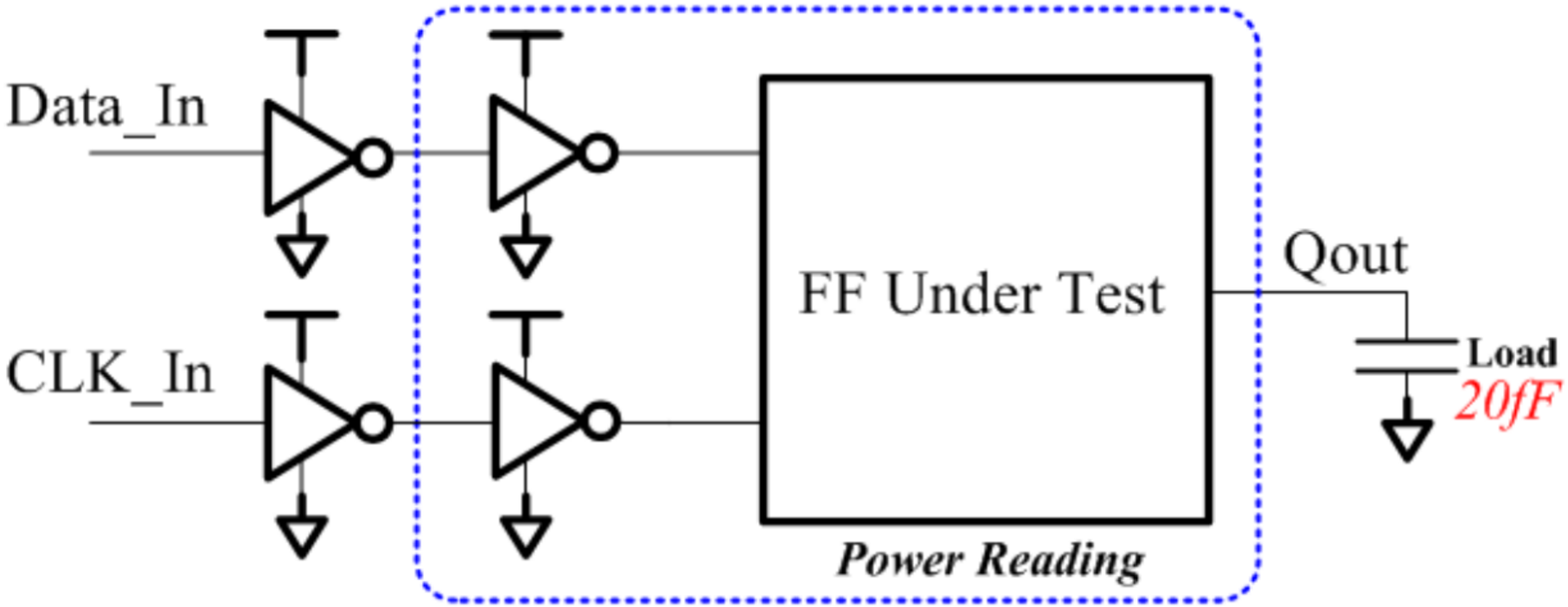
DATA LATCHING PROCESS OF LRFF



LRFF WAVEFORM SIMULATION

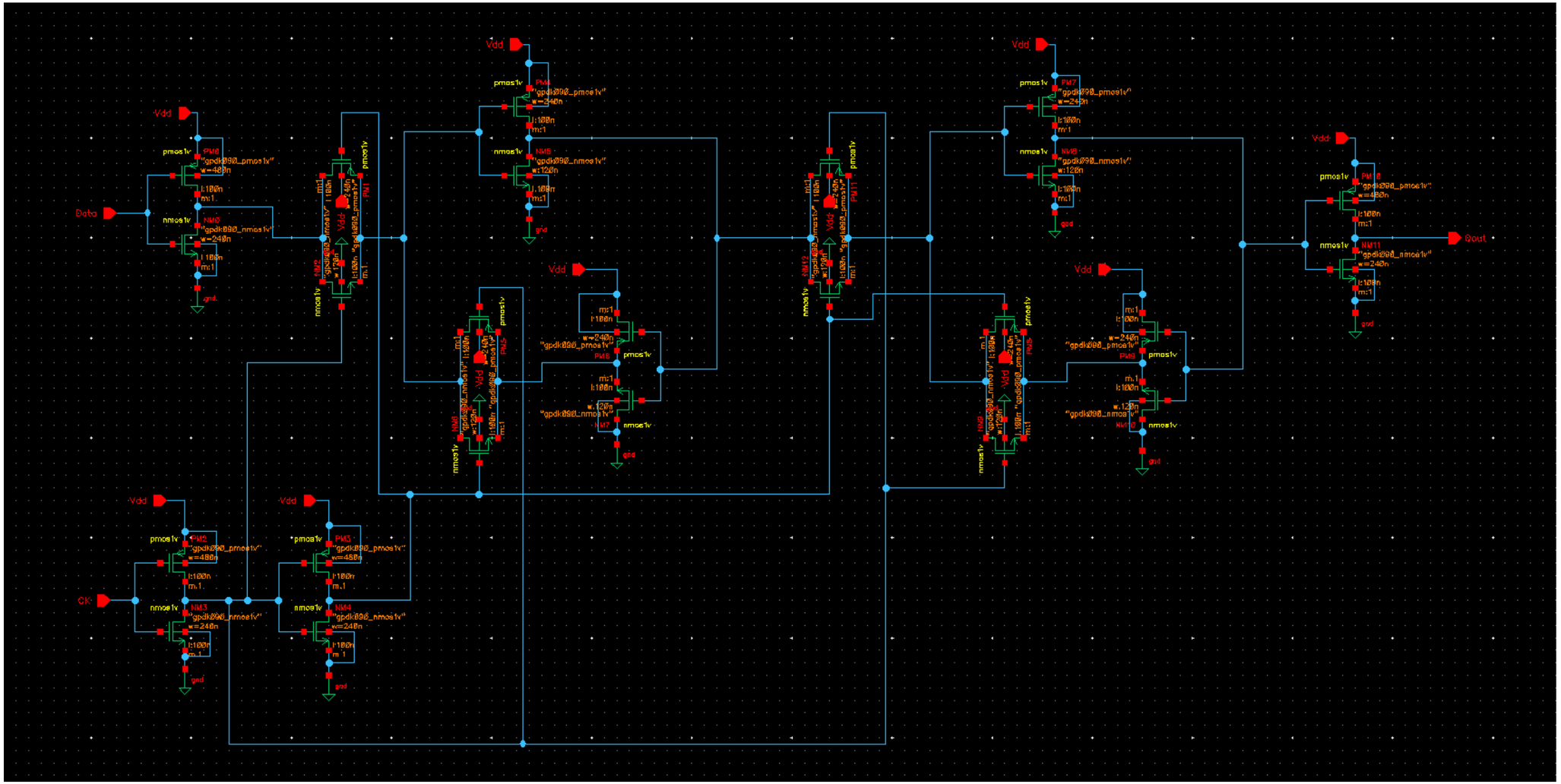


MODEL SETUP FOR FF SIMULATION

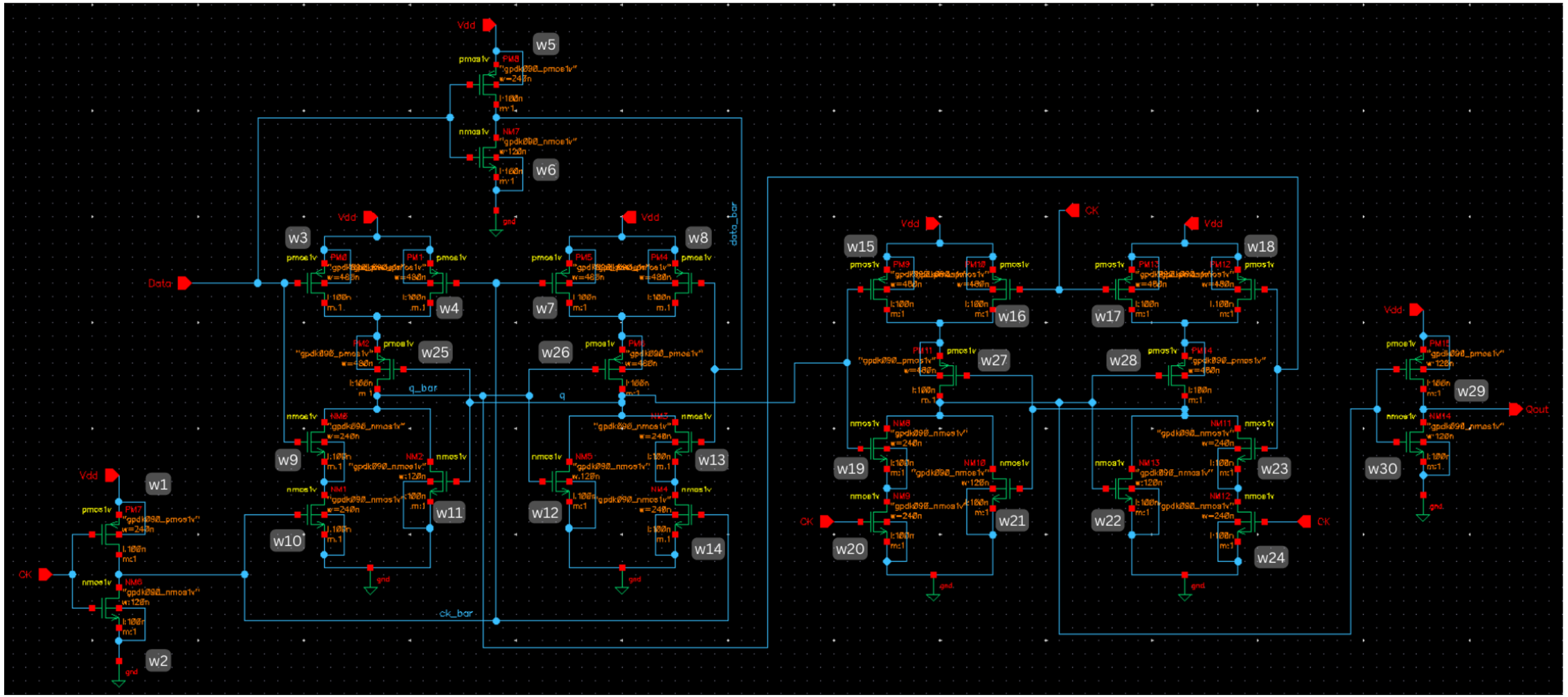


SIMULATIONS

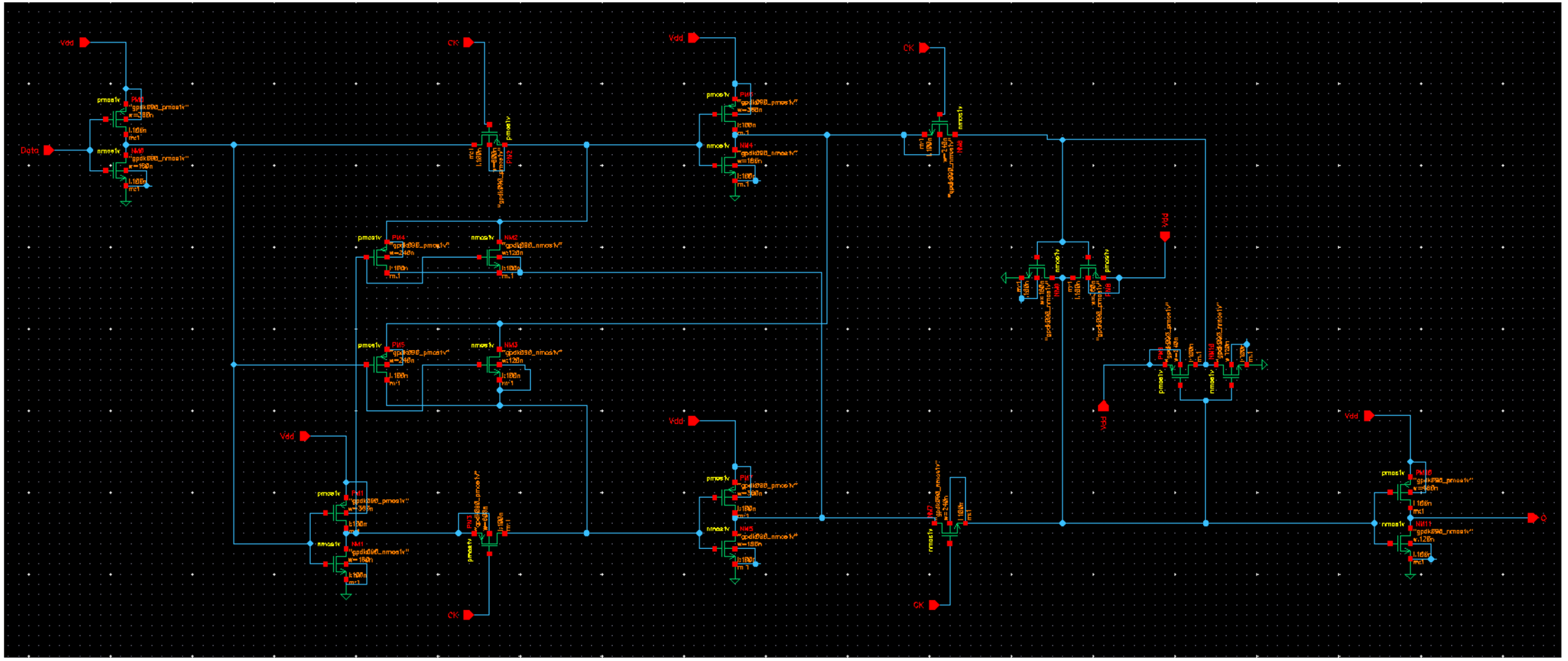
VIRTUOSO IMPLEMENTATION OF TGFF



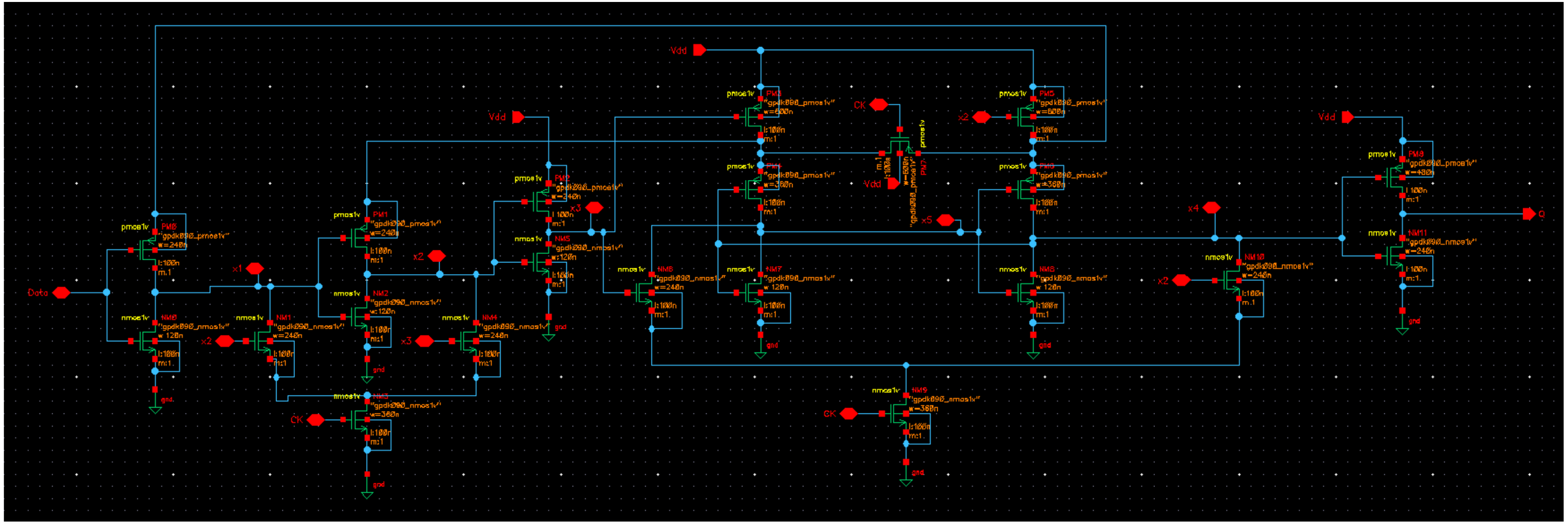
VIRTUOSO IMPLEMENTATION OF SRFF



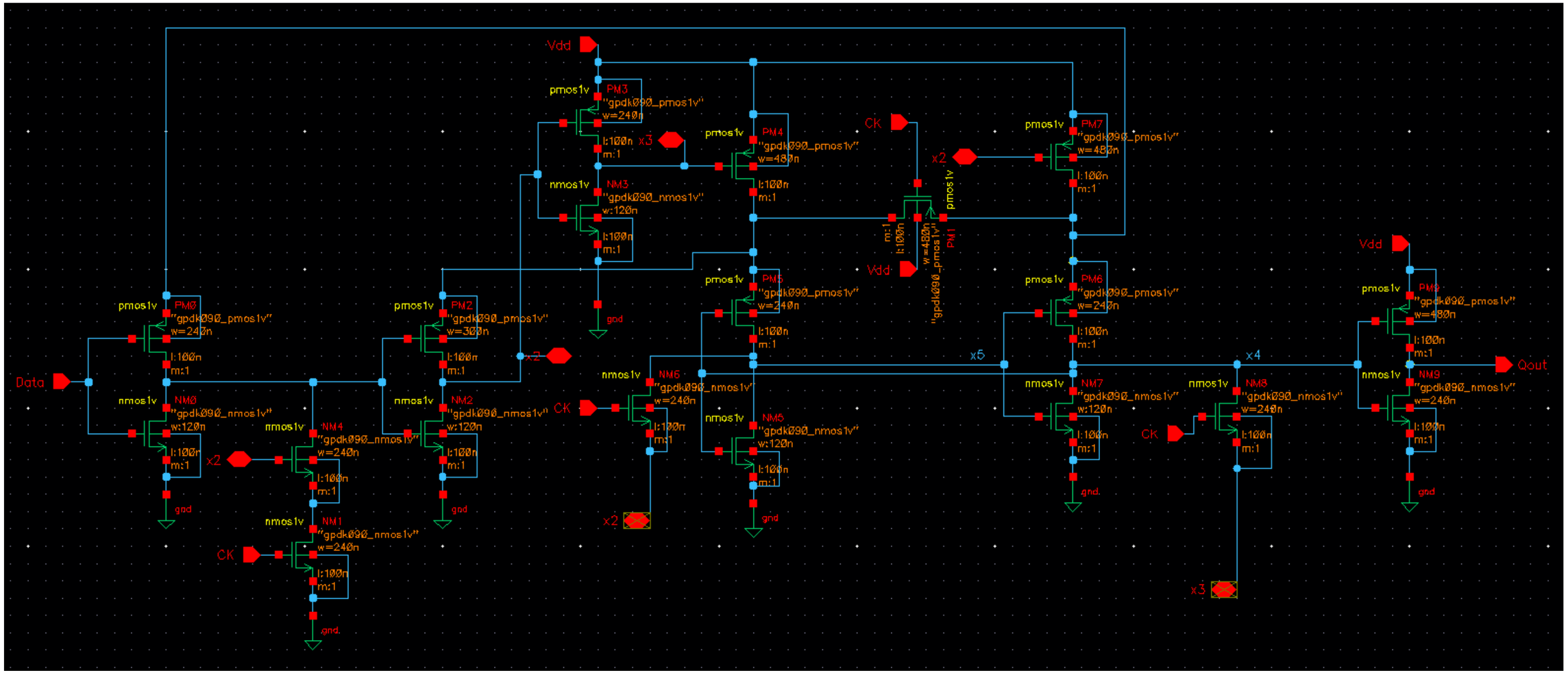
VIRTUOSO IMPLEMENTATION OF ACFF



VIRTUOSO IMPLEMENTATION OF TCFF



VIRTUOSO IMPLEMENTATION OF LRFF



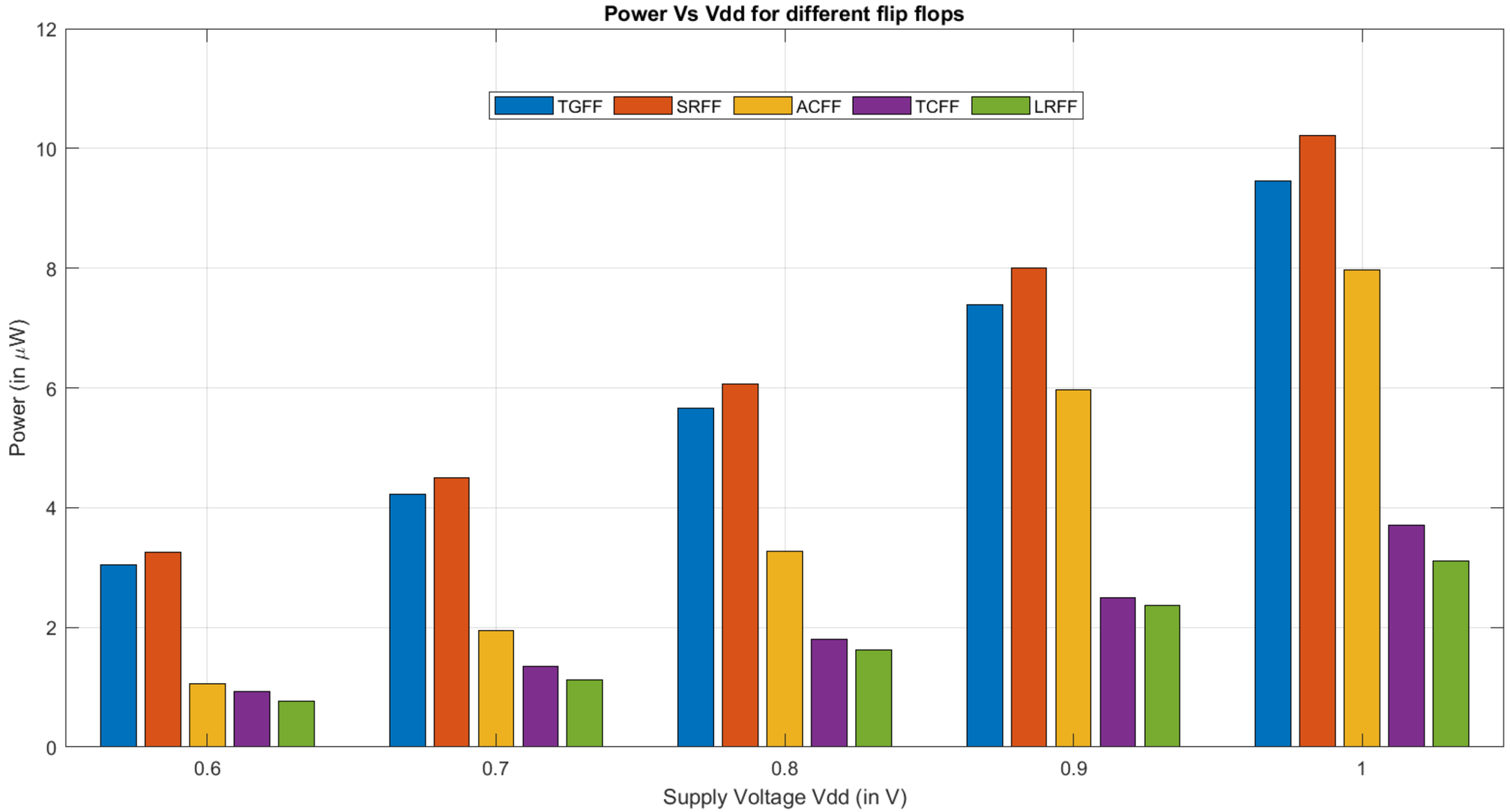
RESULT ANALYSIS

TIMING PARAMETER EVALUATION

Feature Comparison of FF designs at 500 MHz/1 V					
FF Designs	**TGFF**	**SRFF**	**ACFF**	**TCFF**	**LRFF**
No. of Transistors	24	30	22	21	19
Setup Time (ps)	35.73	30.11	113	110	76.7
Hold Time (ps)	-16	-11.11	-74	-38	9
Clock-to-Q delay (ps)	205.01	252	160	171	166
Data-to-Q delay (ps)	240.74	282.11	273	281	242.7
Average Power(12.5%) µW	7.15	7.54	4.84	3.71	3.11
PDP CQ (12.5%) fJ	1.46	1.90	0.77	0.63	0.516
PDP DQ (12.5%) fJ	1.72	2.12	1.32	1.04	0.75

The FFs were tested at Clock Frequency of 500 MHz with the supply voltage (Vdd) fixed at 1V and the Data Switching Activity of 12.5%.

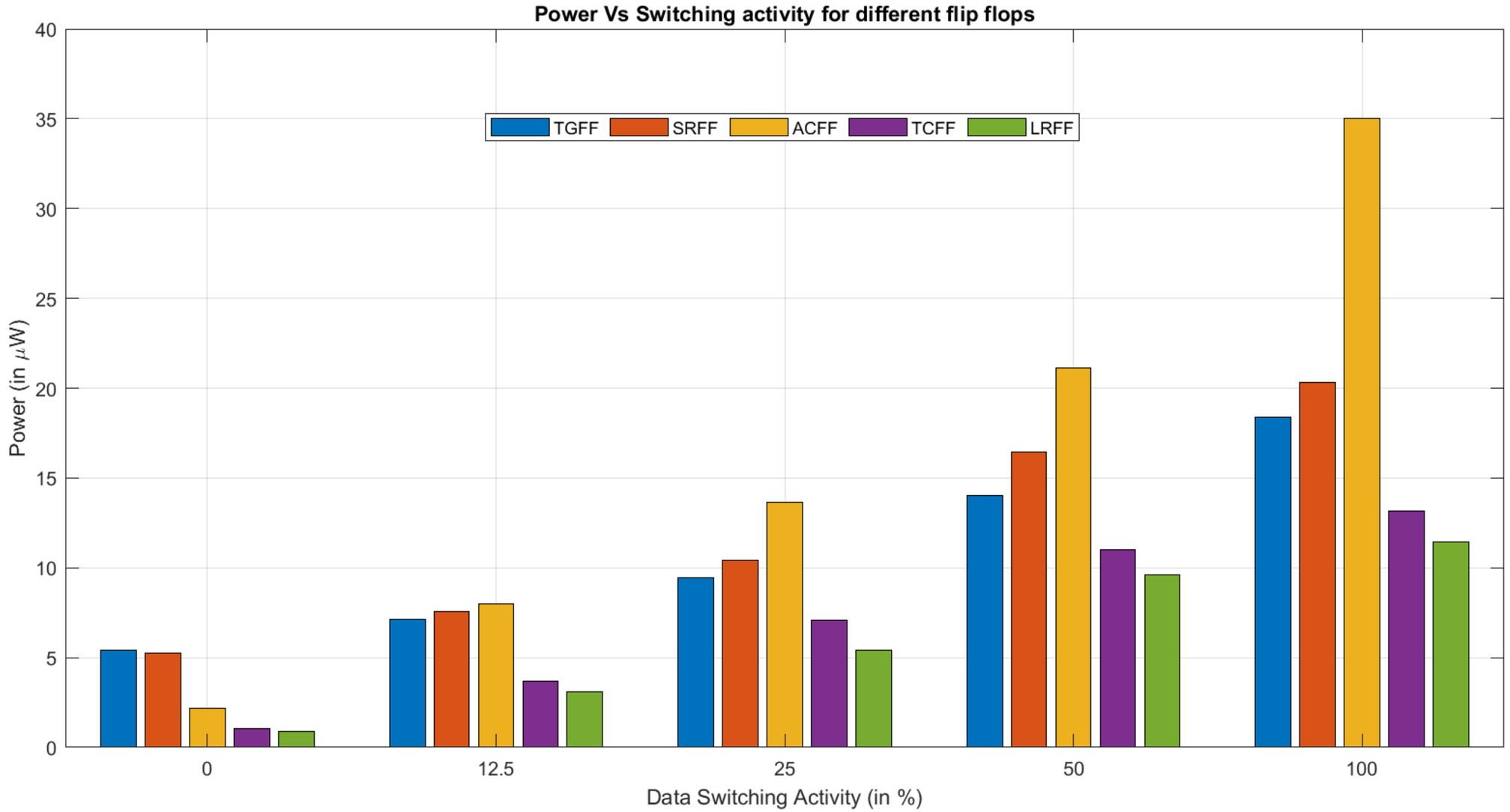
POWER VS VDD



Clock Frequency of 500 MHz

Data Switching Activity of 25%.

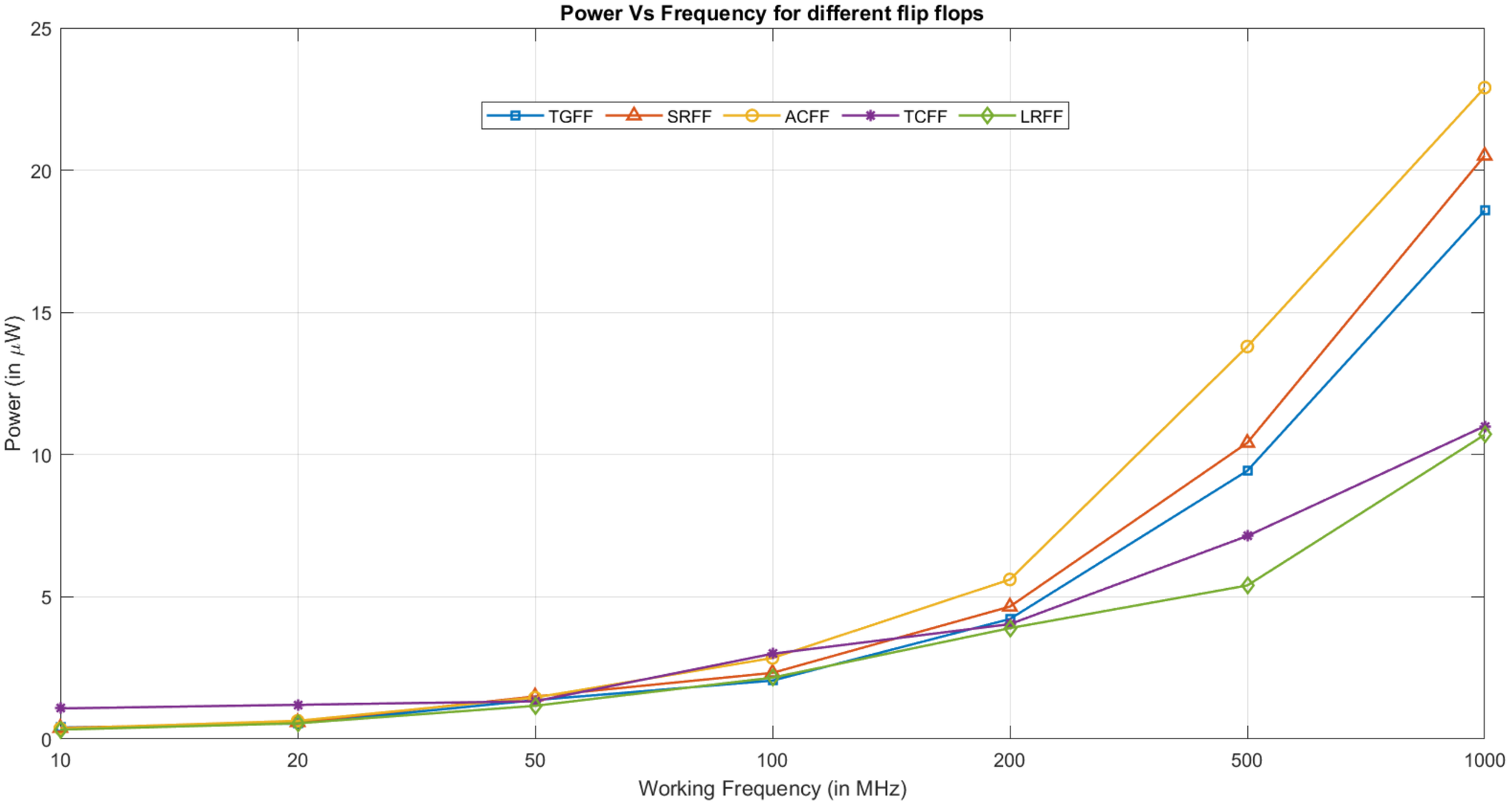
POWER VS DATA SWITCHING ACTIVITY



Clock Frequency of 500 MHz

Supply Voltage of 1 V

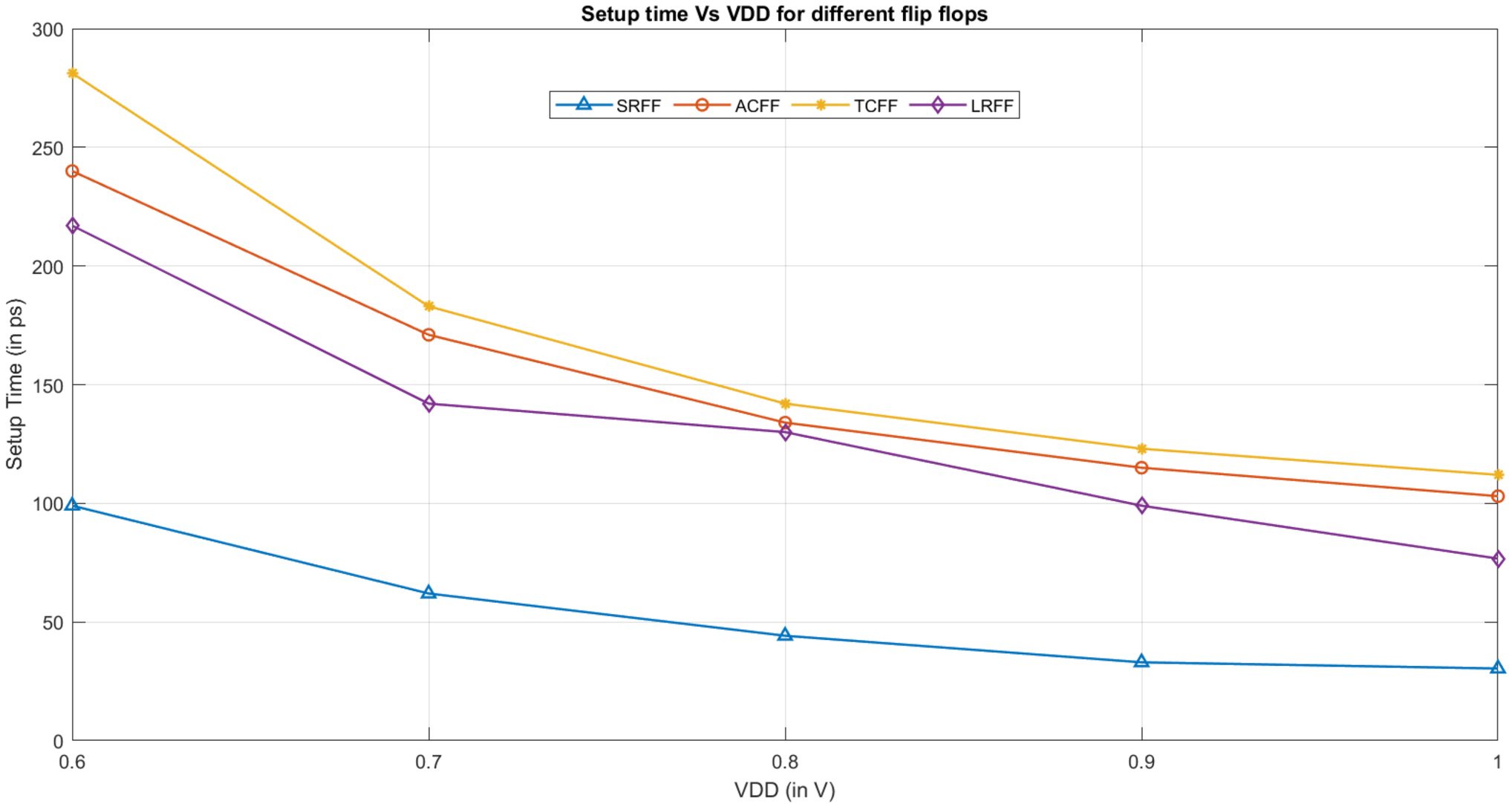
POWER VS WORKING FREQUENCY



Data Switching Activity of 12.5%

Supply Voltage of 1 V

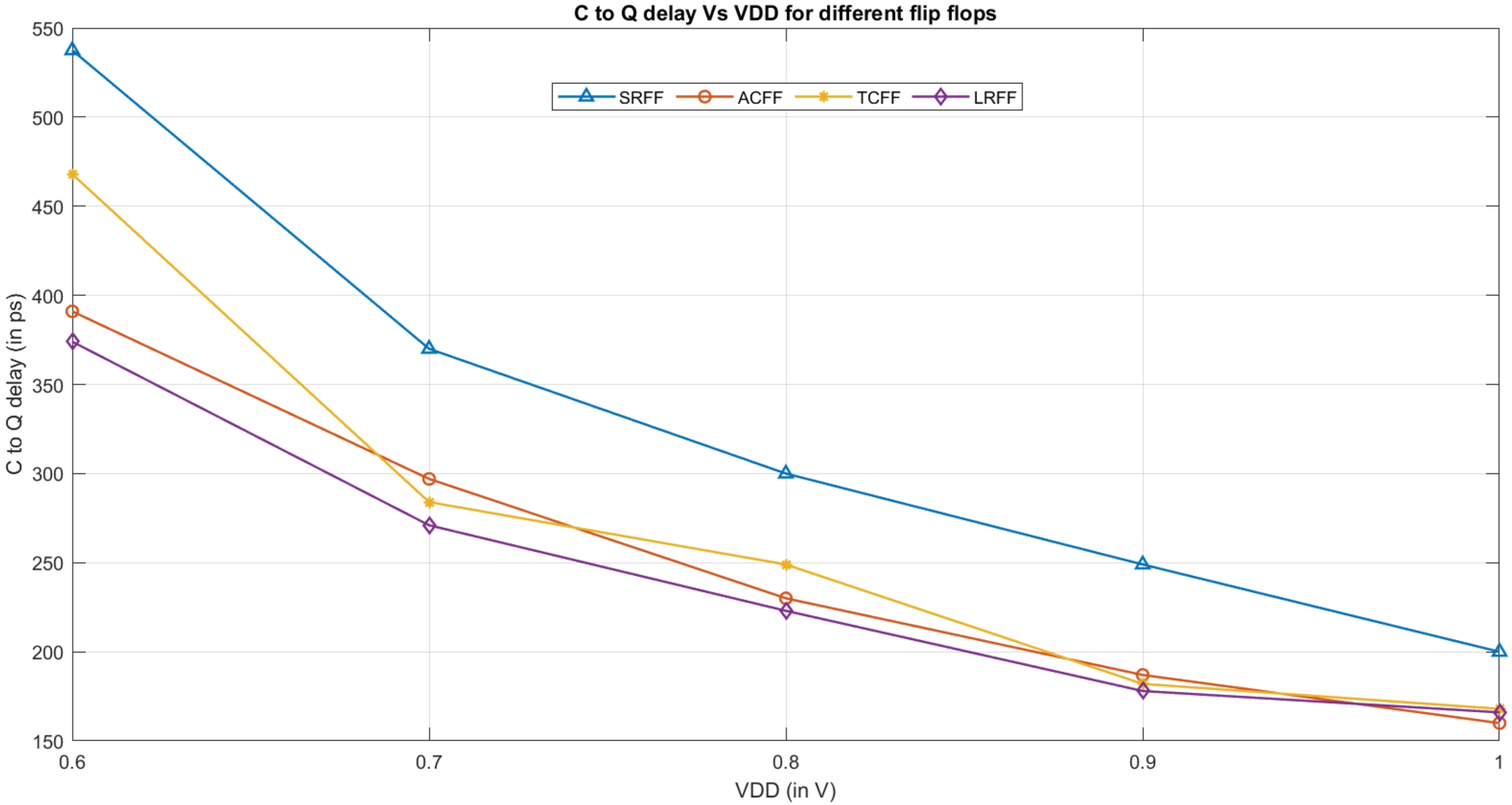
SETUP TIME VS VDD



Clock Frequency of 100 MHz

Data Switching Activity of 12.5%.

CLK TO Q DELAY VS VDD



Clock Frequency of 100 MHz

Data Switching Activity of 12.5%.

LRFF – 45NM TECHNOLOGY NODE

Results obtained at 500MHz, 1V	
Setup time	84.69 ps
Clock to Q delay	175 ps
Avg Power (@ 12.5%)	1.64 uW
PDP CQ	0.287 fJ

CONCLUSIONS

CONCLUSIONS

- In this paper, a novel FF design was achieved by modifying an SR Latch-based structure consisting of static-CMOS logic and CPL.
- Better timing parameters due to additional discharge paths between master and slave latches, improving performance and reducing circuit complexity.
- The proposed design performed better in terms of PDP, CQ delay, and setup time delay. In particular, the proposed design consistently outperformed other designs under different voltage and switching activity settings. This thus proves the efficiency of the proposed FF design
- Moreover from our analysis, we observed that we could go up to a maximum working frequency of 5.5 GHz, beyond which the input was not replicated by the output signal.

REFERENCES

REFERENCES

- N. Kawai, “A fully static topologically-compressed 21-transistor flip-flop with 75% power saving,” IEEE J. Solid-State Circuits, vol. 49, no. 11, pp. 2526–2533, Nov. 2014.
- V. Stojanovic and V. G. Oklobdzija, “Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems,” IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 536–548, Apr. 1999.
- C. K. Teh, T. Fujita, H. Hara, and M. Hamada, “A 77% energy-saving 22-transistor single-phase-clocking D-flip-flop with adaptive-coupling configuration in 40 nm CMOS,” in ISSCC Dig. Tech. Papers, Feb. 2011, pp. 338–339.
- B.-S. Kong, S.-S. Kim, and Y.-H. Jun, “Conditional-capture flip-flop for statistical power reduction,” IEEE J. Solid-State Circuits, vol. 36, no. 8, pp. 1263–1271, Aug. 2001.
- V. G. Oklobdzija, “Clocking and clocked storage elements in a multi-gigahertz environment,” IBM J. Res. Develop., vol. 47, pp. 567–584, Sep. 2003.


thank you