Digital Design Lab

ECE 315

Lab/Project #4

BCD and Seven Segment Display

Group #7

Karysse Hay, Nikeem

Dunkelly-Allen and Dibyanshi Mishra

Zeinab Ramezani, TA

University of Miami

3/10/2022

Overview

The purpose of the lab is to implement a fully functional 4-bit Adder/ Subtractor with a display circuit and BCD attached to it. With this, the algorithm was able to be tested and displayed on the DE1 board. The seven segment display on the board displays the input and output numbers. This was done by using a top level circuit that contains sign display, magnitude display, BCD block diagram, display circuit and a 4 bit Adder-Subtractor.

A BCD is a binary system that is used to represent a decimal number using four binary numbers. The maximum binary number that the circuit can decode is 99. Any positive result can be directly displayed from BCD to the seven segment display on the DE1 board, whereas a negative result must be converted to binary value in order to display a minus sign to the front of the number (magnitude). The top level circuit was created by combining the circuits listed above and was successfully able to display an addition/ subtraction equation using decimal numbers. The inputs traveled through the 4 bit adder/subtractor, sign display circuit or magnitude display circuit (depending on the operation), the BCD circuit and display circuit to then display the output value on the seven segment display on the DE1 board.

Equipment

- Quartus Prime Software
- AND gates
- OR gates
- XNOR gates
- NOT gates
- ModelSim
- Input Pins
- Output Pins
- Orthogonal Node
- Diagonal Node
- DE1 Board

Description

To begin, a truth table was constructed for the inputs, X_3,X_2, X_1, $X_0$with outputs P_3, P_2, P_1, and P_0. Four K-maps were constructed for each output value respectively and the boolean equations were derived from each K-maps. P_0equaled $\bar{X_3}\,\bar{X_2}\,X_0 + X_2X_1\overline{X_0} + X_3\overline{X_0}$, P_1equaled

$X_1X_0 + X_3\overline{X_0} + \overline{X_2}X_1$, P_2equaled $X_2\,\bar{X}_1\,\bar{X}_0 + X_3X_0$ and P_3equaled $X_3 + X_2X_0 + X_2X_1$. The simplest circuit was designed based on these equations and was implemented on Quartus Prime.

Quartus Prime was opened and a new project was created, named "Lab_4_ECE_315", and saved into our USB drive. A new file was created in the project and the block diagram/schematic file option was chosen. The new file was saved and the file with the 4 bit adder/subtractor from Lab 3 was opened on Quartus Prime. This circuit was copied into Lab 4.

The 4 bit Adder/Subtractor was modified to introduce a $A/\overline{S}$ control input. When the control was set to 1, it performed addition using the equation (X+Y) = $X_3X_2X_1X_0 + Y_3\,Y_2\,Y_1\,Y_0$ + 0000 while 0 performed subtraction using the equation X+(-Y) = $X_3X_2X_1X_0 + Y_3$' Y_2' Y_1' Y_0' + 0001. The 2:1 mux was found in Quartus Prime and added to the symbol window; and four of these Muxs and the 4 bit adder were used to implement the 4 bit adder/subtractor. The A/$\overline{S}$ input was connected to these 2:1 Mux inputs and the Cin of the 4 bit adder was set to 0. The circuit was set to the top level hierarchy and compiled on Quartus Prime.

In the University Program, a vector wave file was created and the node was clocked. All the input and output pins were selected and added to the nodes window and Quartus 1 stimulator was chosen. The end time for each input was set by overwriting the clock. X_3 was set to 16 microseconds, $X_2$was set to 8 microseconds, $X_1$was set to 4 microseconds and $X_0$was set to 2 microseconds. The grid size was set to 1 microsecond and the simulation was run by clicking the icon, run functional simulation. The inputs were grouped by selecting the inputs, right clicking and selecting the option to group. A screenshot of the simulation was taken and has been attached in the results section. This was converted into a symbol by right clicking, selecting insert and then selecting symbol.

Using the logic developed previously, a sign display circuit was constructed on Quartus Prime. There were two input signs, 0 and 1 with six output values, S_6, S_5, S_4, S_3, S_2, S_1, and S_0. The sign display circuit was compiled and saved. Furthermore, a magnitude display circuit was constructed using 5 inputs and a sign bit. The magnitude display circuit was a combinational circuit with 4 outputs - R_1, R_2, $R_3$and R_0. If the input was positive, the input was equal to the output. whereas if the input value was negative, the circuit would obtain its 2s complement.

Next, the BCD block diagram was created. The BCD block diagram was created using several Add 3 Circuits. The Add 3 circuit was designed with 3 inputs and 3 output values. The input

values were connected to NOR gates, AND gates and OR gates with outputs =H_4 G_5F_5 E_4D_3 C_2 B_1 A. The Add 3 circuit was compiled and simulated. The Add 3 Circuit was then converted into a block symbol (bsf).
These Add 3 circuits were combined together to create the BCD Block Diagram. The BCD block diagram consisted of 7 add 3 circuits, inputs A, B, C, D, E, F, G, H and outputs U_0, U_1, U_2, U_3, L_0, L_1, L_2, L_3 and overflow. The BDC circuit was compiled and simulated. The BDC Block diagram was converted into a block symbol as well.

Next, a BCD circuit with 7 segment display was created using the BCD circuit and display circuits constructed in Lab 2. The display circuit from Lab 2 was copied into a new file and the BCD circuit with inputs A-H was added. The outputs of the circuit, U_0, U_1, $U_2$and U_3 was fed into the first display circuit inputs X_0, X_1, $X_2$and X_3 while the remaining outputs L_0, L_1, $L_2$and L_3 were fed into the inputs of the second display circuit. Outputs of Display 1 were inputted into the 7 segment display from D10-D16 while remaining outputs of Display 2 were imputed to D00-D06 of the segment display. This circuit was compiled and simulated and was converted into a block symbol.

All the circuits were combined to create a Top level circuit- a 4 bit adder/subtractor with display circuit. The circuit started with the modified 4 bit Adder/Subtractor with inputs X_0, X_1, X_2, X_3, Y_0, Y_1, $Y_2$and Y_3. The circuit was connected to the sign display circuit and magnitude display circuit. The sign display circuit had outputs S_6, S_5, S_4, S_3, S_2, S_1, S_0 connected to the 7 segment display. The outputs Q_3, Q_2, $Q_1$and $Q_0$of the 4 bit adder subtractor were assigned to the LEDs and were fed to the magnitude display circuit. The outputs of the magnitude display circuit were sent to the BCD circuit which was connected to the two display circuits from Lab 2. The circuit was compiled and simulated. However, when the circuit was stimulated, the results showed errors. The 4 bit adder/subtractor was modified to include an XNOR gate that took Cout and A/$\overline{S}$ as inputs. The circuit was compiled and simulated again and it showed correct results. This new and improved circuit was converted into a symbol.

Lastly, the circuit was downloaded and displayed on the DE1 board. The Quartus Prime window was opened and the assignments tab was clicked. The pin planner was selected, after which a window opened. The pins were assigned to the DE1 board. Input pins X_0, X_1, $X_2$and X_3, Y_0, Y_1, Y_2, Y_3 and Cin were assigned to PIN_AB12, PIN_AC12, PIN_AF9, PIN_AF10, PIN_AD11,

PIN_AD12, PIN_AE11, PIN_AC9, PIN_AD10. The Program Device and hardware output was opened and the DE1-SoC board was selected as Hardware output and Auto-detect was selected. The file was uploaded to 5CSEBA5 device and the start button was clicked to test the circuit design. The circuit was tested with multiple combinations of numbers. For example: 4-3=2, 6-8=-2 etc.

Design Synthesis

1. **Truth Tables**

Input X3X2X1X0	Output P3P2P1P0
0000	0000
0001	0001
0010	0010
0011	0011
0100	0100
0101	1000
0110	1001
0111	1010
1000	1011
1001	1100
1010	xxxx
.	.
.	.
1111	xxxx

Figure 1: Truth Table for Add 3 circuit

This truth table (Figure 1) was given to us partially done, our task was to finish it. If an input was greater than 4, the output would be 3 + the input, hence the name Add 3. For numbers greater than 9 the output was don't cares, using these don't cares proved to be essential in our boolean equations. Karnaugh maps were constructed based on each output from P0-P3.

2. KMAPS

	X_3X_2 00	01	11	10
X_1X_0 00	0	0	X	1
01	1	0	X	0
11	1	0	X	X
10	0	1	X	X

Table 1: K-map for P0

	X_3X_2 00	01	11	10
X_1X_0 00	0	0	X	1
01	0	0	X	0
11	1	1	X	X
10	1	0	X	X

Table 2: K-map for P1

	X_3X_2 00	01	11	10
X_1X_0 00	0	1	X	0
01	0	0	X	1
11	0	0	X	X
10	0	0	X	X

Table 3: K-map for P2

	X_3X_2 00	01	11	10
X_1X_0 00	0	0	X	1
01	0	1	X	1
11	0	1	X	X
10	0	1	X	X

Table 4: K-map for P3

3. **Boolean Equations:**

P0: $\bar{X}_3 \bar{X}_2 X_0 + X_2 X_1 \overline{X_0} + X_3 \overline{X_0}$

P1: $X_1 X_0 + X_3 \overline{X_0} + \overline{X_2} X_1$

P2: $X_2 \bar{X}_1 \bar{X}_0 + X_3 X_0$

P3: $X_3 + X_2 X_0 + X_2 X_1$

Complete Logic Diagram

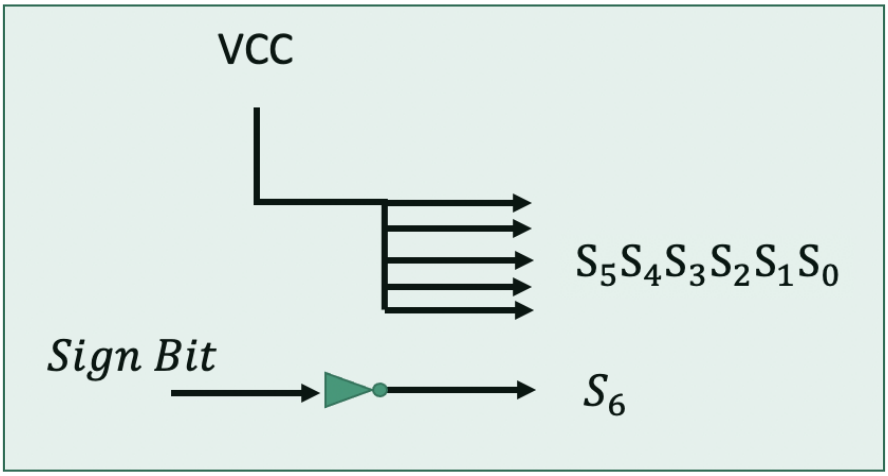

Figure 2:Block Diagram for Sign Display Circuit

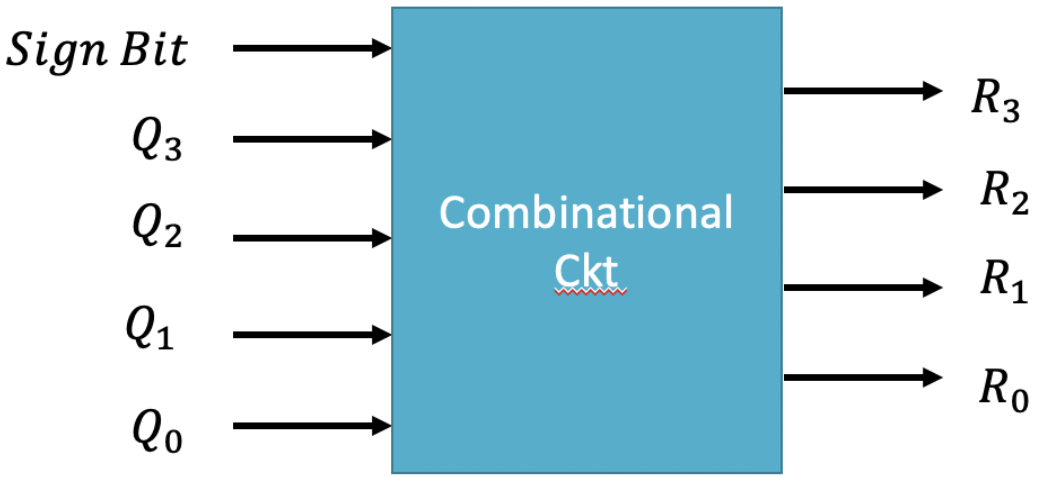

Figure 3: Block Diagram for Magnitude Circuit

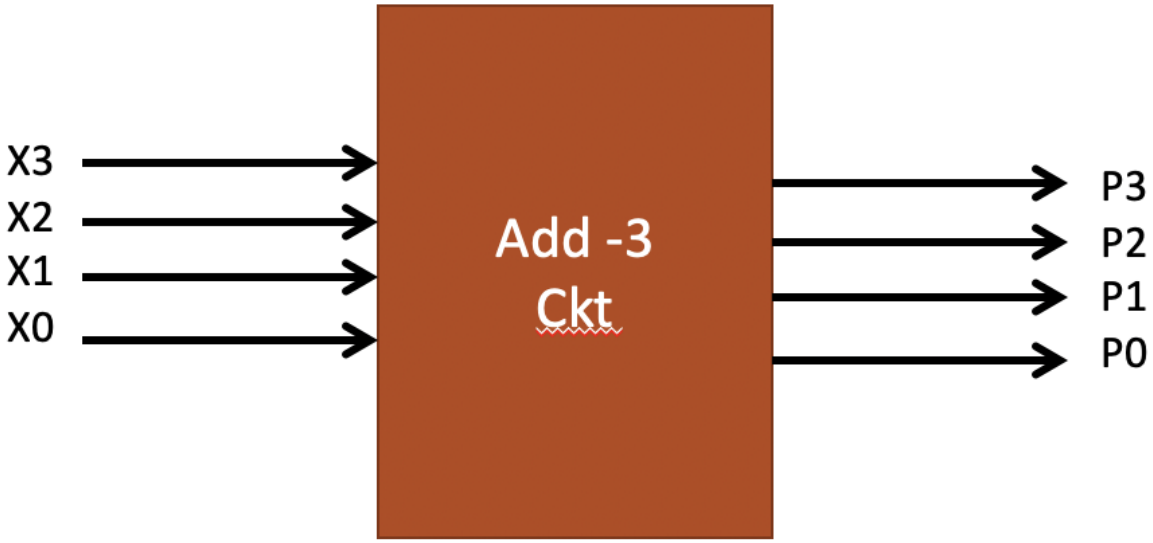

Figure 4: Block Diagram for Add 3 Circuit Simplified

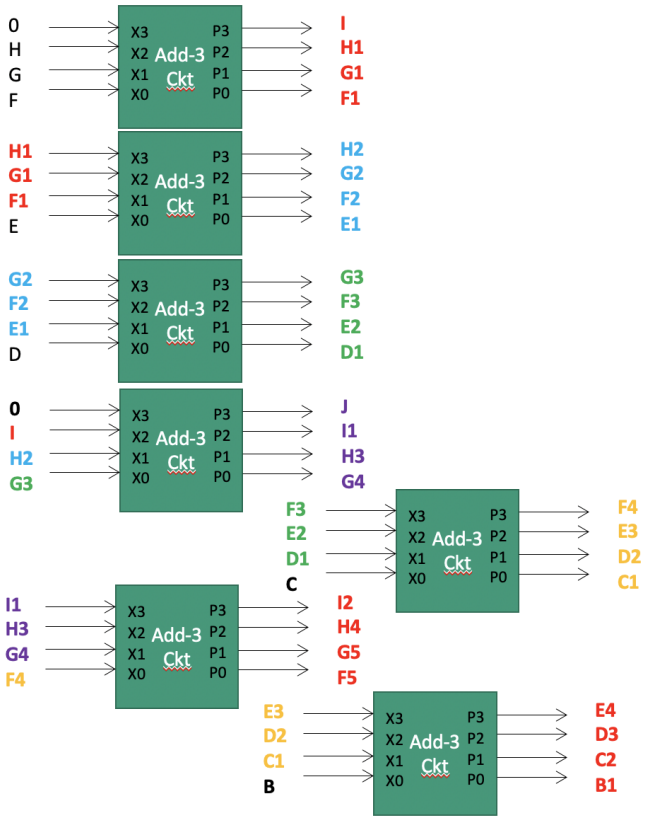

Figure 5: Block Diagram for BCD Circuit

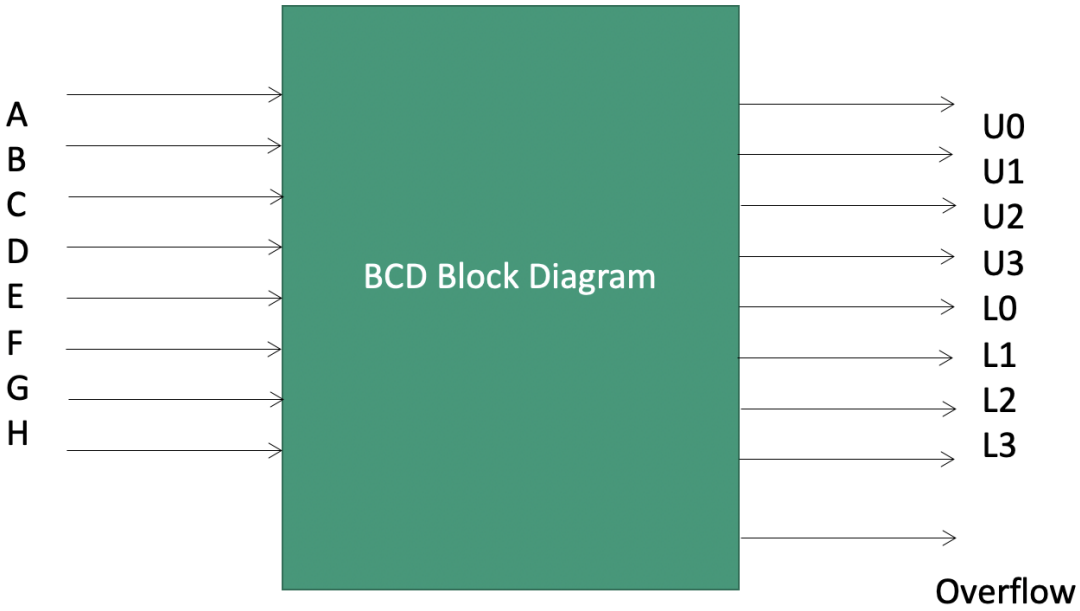

Figure 6: Block Diagram for BCD Circuit Simplified

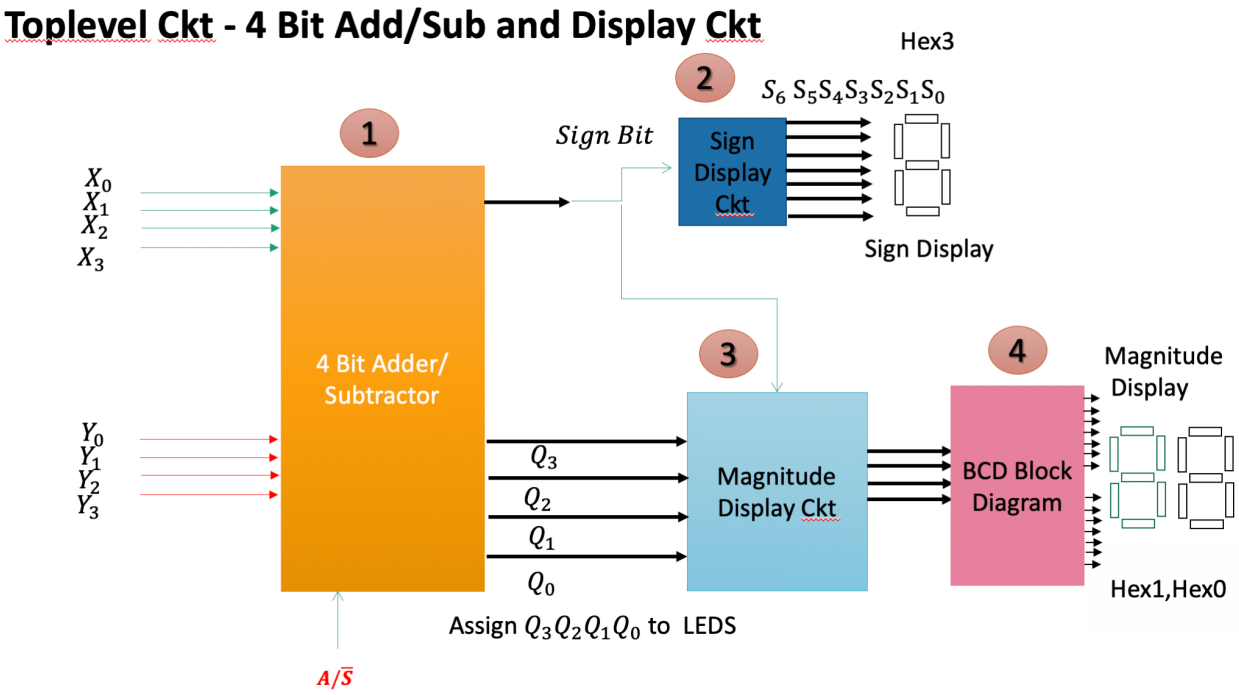

Figure 7: Block Diagram for Top Level Circuit Simplified

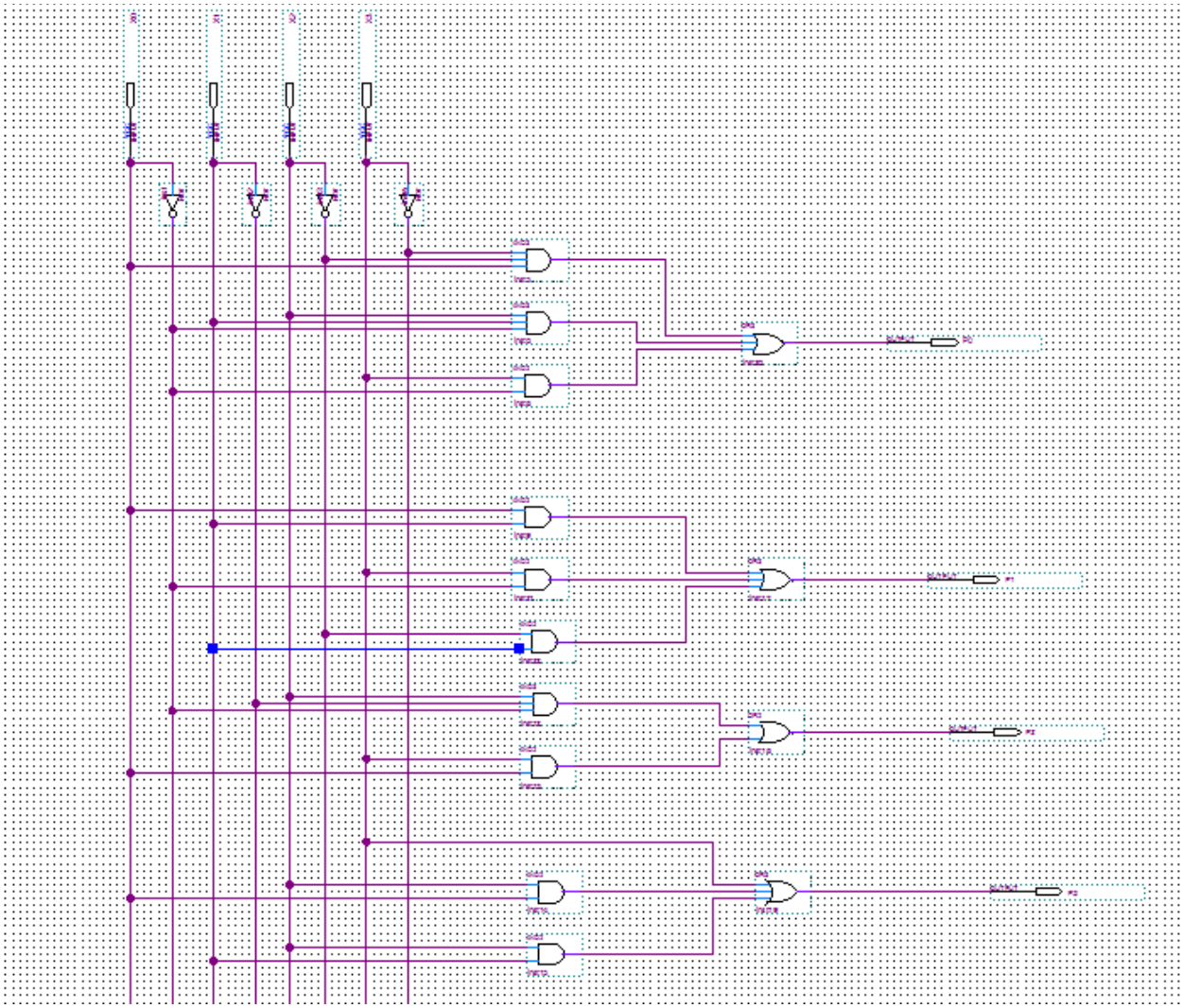

Figure 8: Complete Logic Diagram for Add 3 circuit on Quartus Prime

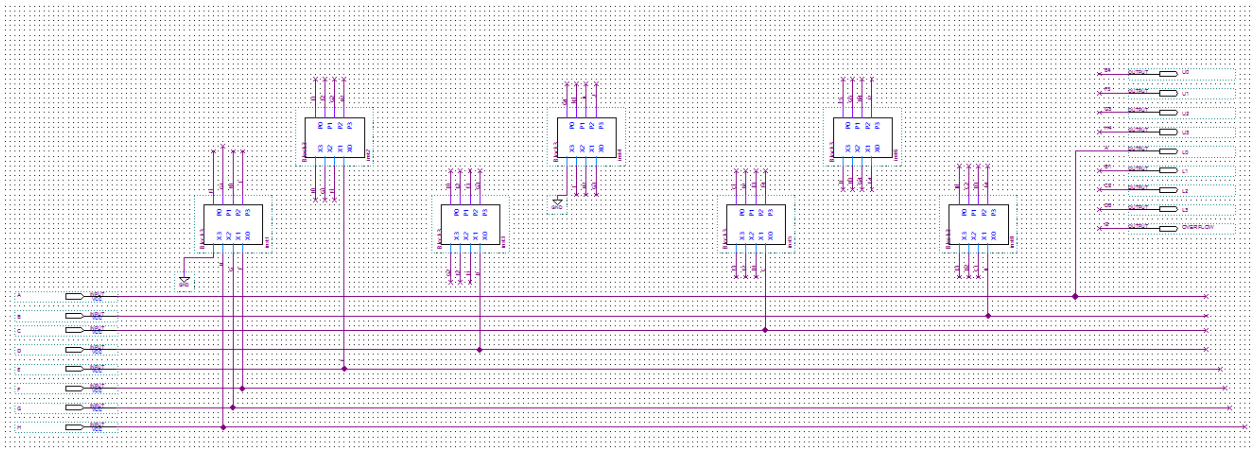

Figure 9: Complete Logic Diagram of BCD circuit on Quartus Prime

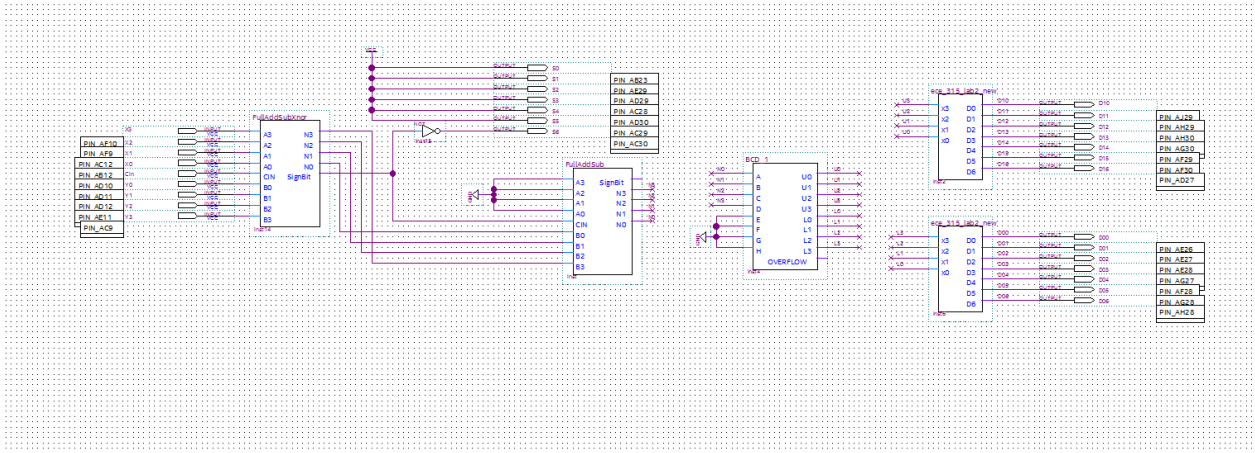

Figure 10: Top Level Complete Logic Diagram on Quartus Prime

Results and Simulations

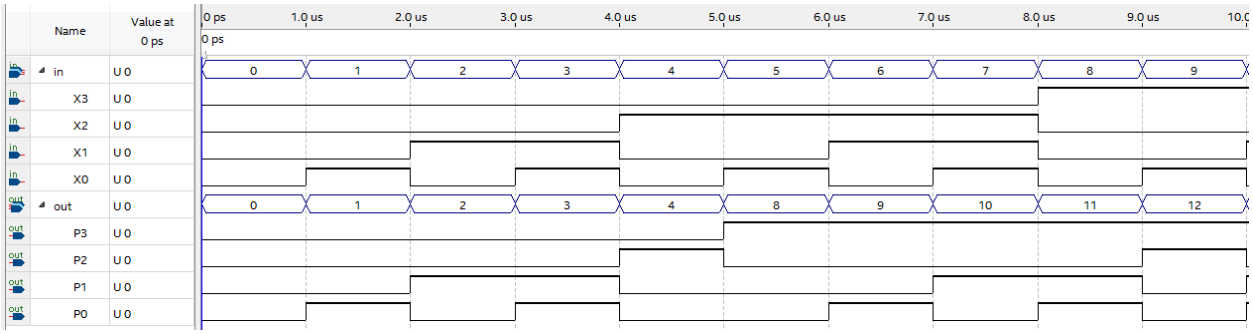

Figure 11: Add 3 Circuit Simulation

Figure 11 shows the simulation results for the Add 3 Circuit. This circuit adds a value of 3 to an input greater than 4. For example: the input number (first line) is 5 in binary which is 0101 and the output number (second line) is 8 in binary which is 1000. This algorithm allows for a binary number to be converted to BCD - Binary Converted Decimal.

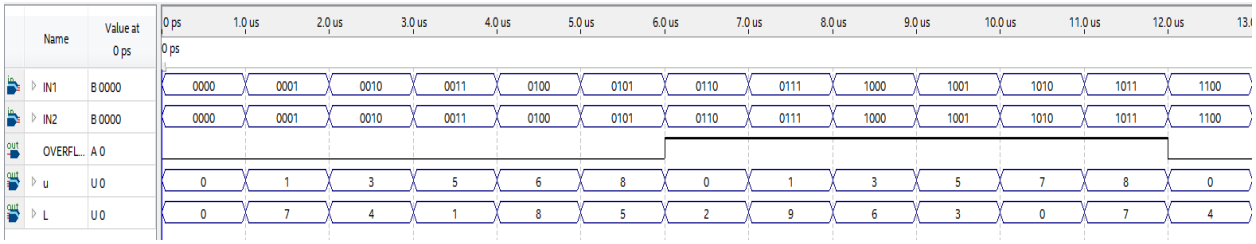

Figure 12: BCD Circuit Simulation

Figure 12 shows the simulation for the BCD circuit. This circuit combines two 4-bit binary numbers to one 8-bit binary number. It then displays this number as a whole amongst two decimal values. For instance: 0100 and 0100 are both 4 (decimal) individually but 0100 0100 is 68 (decimal). This can be seen in the U and L segment in the simulation. U=6 and L=8. These two numbers would then be displayed on the seven segment display.

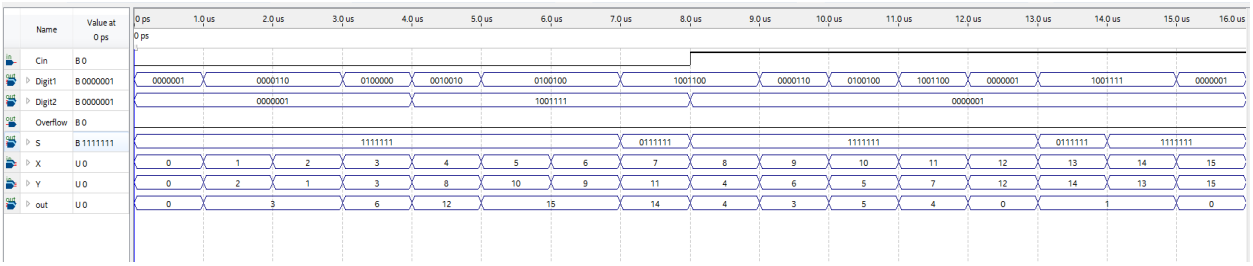

Figure 13: Top Level Circuit Simulation

Figure 13 shows the final simulation of the entire lab. This circuit was able to perform addition and subtraction of positive numbers of range (0-15). It displayed both positive and negative outputs depending on the inputs given. When the Cin input was 0, addition was performed whereas when it was 1, subtraction was performed. This can be seen above. (E.g.) 1+2 = 3 and 8-4=4.

The Digit 1 and Digit 2 portion of the simulation represented the seven segment display for each number. A 0 meant that that segment was on and a 1 meant that it was on. This can be further seen in the pictures below.

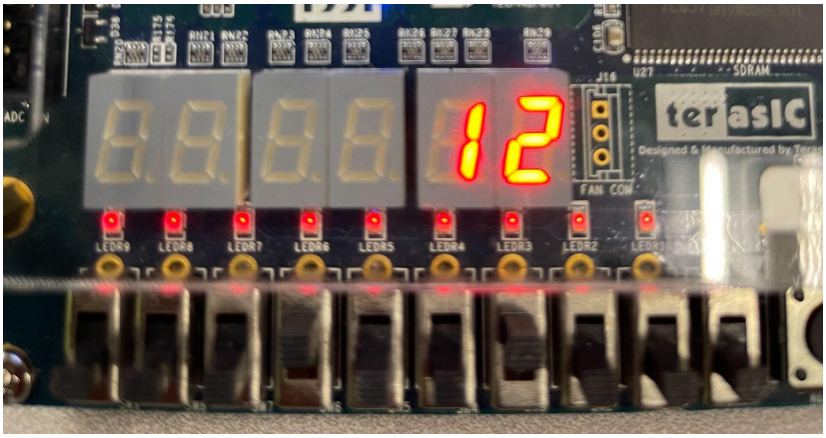

Figure 14: Addition performed on the DE1 board

In Figure 14, it can be seen that 8 (rightmost four switches) add 4 (second four switches from the right) gave an output of 12 which was displayed on the seven segment displays. Also, it should be noted that the second switch from the left indicates whether addition or subtraction will be performed. ‘0’ suggests addition and ‘1’ suggests subtraction.

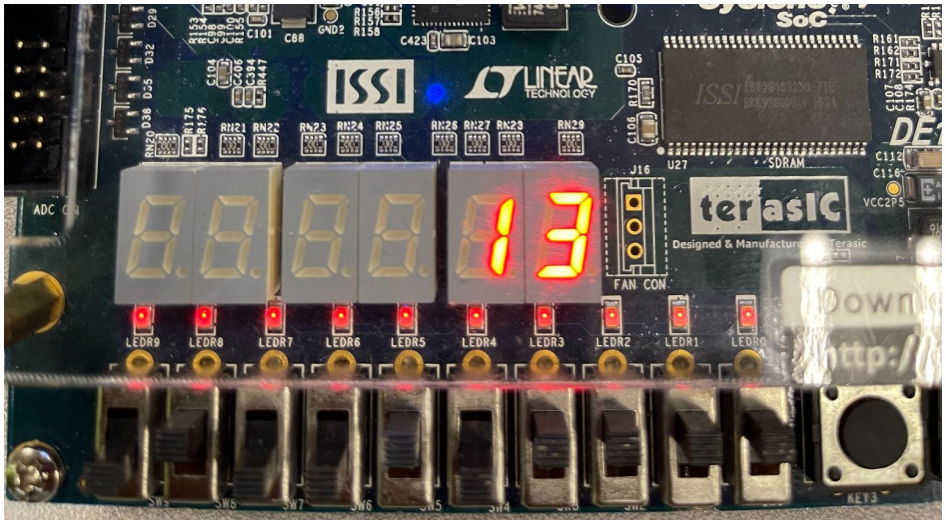

Figure 15: Subtraction performed on the DE1 board

In Figure 15, it can be seen that 15 (rightmost four switches) subtract 2 (second four switches from the right) gave an output of 13 which was displayed on the seven segment displays. Also, the addition/ subtraction switch is flipped up indicating a 1 for subtraction.

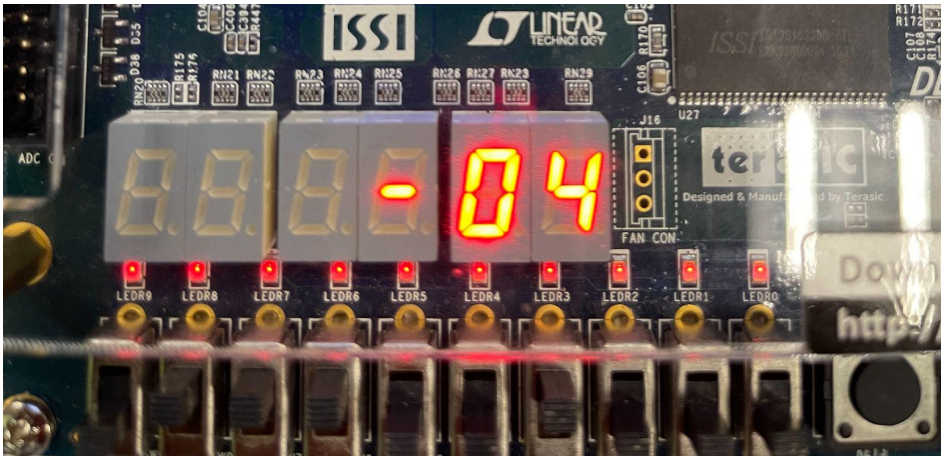

Figure 15: Display of Negative Numbers on the DE1 board

IIn Figure 15, it can be seen that 8 (rightmost four switches) subtract 12 (second four switches from the right) gave an output of -04 which was displayed on the seven segment displays.

Conclusion

The 4 Bit Adder/ Subtarctor from the previous lab was already implemented and working completely. This circuit was combined with other logical circuits to create a fully functioning 4 Bit Adder/ Subtractor that was able to display its inputs and outputs on the seven segment display of the DE1 board.

A sign display circuit was created which allowed for the numbers to be displayed with a negative sign and the magnitude of the numbers were obtained by creating a magnitude display circuit. The BCD circuit was a combination of seven add-3 circuits which allowed for a single decimal number (4-bits) to be displayed with 8 bits in binary.

At first, the Adder part of the circuit was giving the wrong output values. The circuit had to be revised and after many trials with different gates, it was decided that an XNOR gate should be incorporated. This gate took the Cout and $A/\overline{S}$ signal as inputs and gave the Sign Bit as the new output. This fixed the errors.

The seven segment display from another previous lab was connected to the BCD to allow for the displaying of the decimal numbers. After the entire top level circuit was compiled and simulated, it was downloaded to the board and tested. The circuit worked perfectly and displayed the correct numbers.

The extra credit portion of the lab proved to be very difficult. Our group was unable to put forward a logical solution that would have allowed our circuit to accept negative decimal inputs. Many combinations of gates and logic were tested but all failed.