

# Register map

---

Created with [Corsair](#) v1.0.4.

## Conventions

Access mode	Description
rw	Read and Write
rw1c	Read and Write 1 to Clear
rw1s	Read and Write 1 to Set
ro	Read Only
roc	Read Only to Clear
roll	Read Only / Latch Low
rolh	Read Only / Latch High
wo	Write only
wosc	Write Only / Self Clear

## Register map summary

Base address: 0x00000000

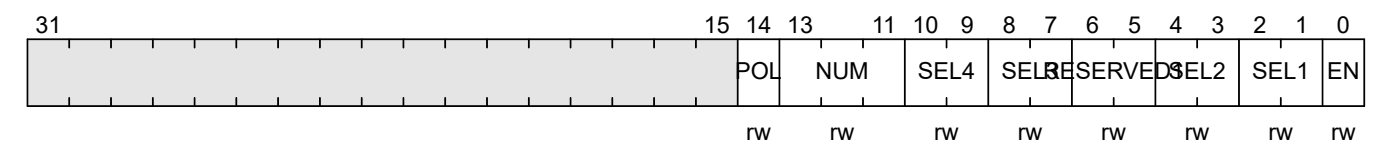
Name	Address	Description
<a href="#">TPWM_config</a>	0x00000000	PWM configuration register
<a href="#">TPWM_prescaler</a>	0x00000004	PWM clock divider
<a href="#">TPWM_period1</a>	0x00000008	PWM1 and PWM2 period register
<a href="#">TPWM_period2</a>	0x0000000c	PWM3 and PWM4 period register
<a href="#">TPWM_compare1</a>	0x00000010	Compare values for PWM1 and PWM2
<a href="#">TPWM_compare2</a>	0x00000014	Compare values for PWM3 and PWM4
<a href="#">TPWM_counter1</a>	0x00000018	PWM counters for PWM1 and PWM2
<a href="#">TPWM_counter2</a>	0x0000001c	PWM counters for PWM3 and PWM4

## TPWM\_config

PWM configuration register

Address offset: 0x00000000

Reset value: 0x00000000



Name	Bits	Mode	Reset	Description
-	31:15	-	0x0000	Reserved
POL	14	rw	0x0	Polarity of the PWM signal
NUM	13:11	rw	0x0	Number of PWM signals selected
SEL4	10:9	rw	0x0	Output selection for PWM4
SEL3	8:7	rw	0x0	Output selection for PWM3
RESERVED1	6:5	rw	0x0	Reserved for future use
SEL2	4:3	rw	0x0	Output selection for PWM2
SEL1	2:1	rw	0x0	Output selection for PWM1
EN	0	rw	0x0	Enable PWM operation

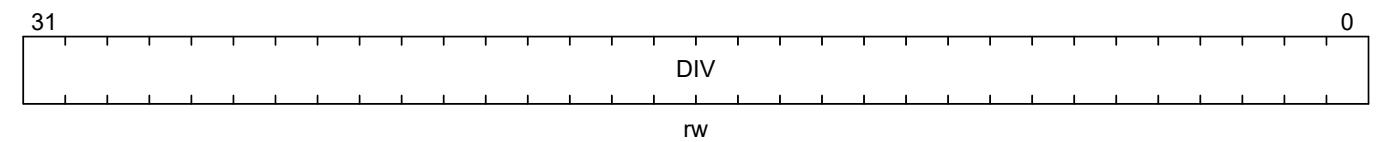
Back to [Register map](#).

## TPWM\_prescaler

PWM clock divider

Address offset: 0x00000004

Reset value: 0x0000001b



Name	Bits	Mode	Reset	Description
DIV	31:0	rw	0x0000001b	Clock divider value for PWM

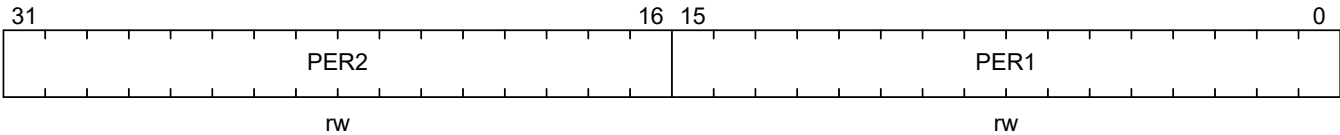
Back to [Register map](#).

## TPWM\_period1

PWM1 and PWM2 period register

Address offset: 0x00000008

Reset value: 0xffffffff



Name	Bits	Mode	Reset	Description
PER2	31:16	rw	0xffff	Period value for PWM2
PER1	15:0	rw	0xffff	Period value for PWM1

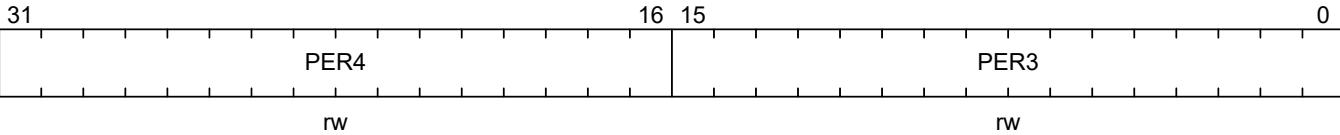
Back to [Register map](#).

## TPWM\_period2

PWM3 and PWM4 period register

Address offset: 0x0000000c

Reset value: 0xffffffff



Name	Bits	Mode	Reset	Description
PER4	31:16	rw	0xffff	Period value for PWM4
PER3	15:0	rw	0xffff	Period value for PWM3

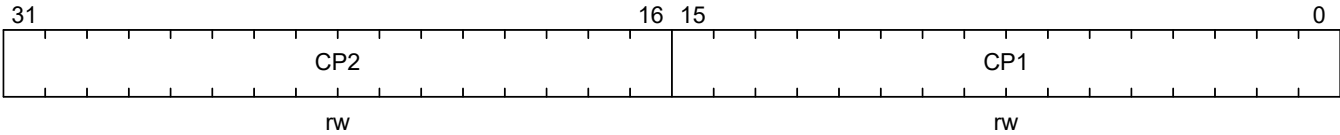
Back to [Register map](#).

## TPWM\_compare1

Compare values for PWM1 and PWM2

Address offset: 0x00000010

Reset value: 0xffffffff



Name	Bits	Mode	Reset	Description
CP2	31:16	rw	0xffff	Compare value for PWM2
CP1	15:0	rw	0xffff	Compare value for PWM1

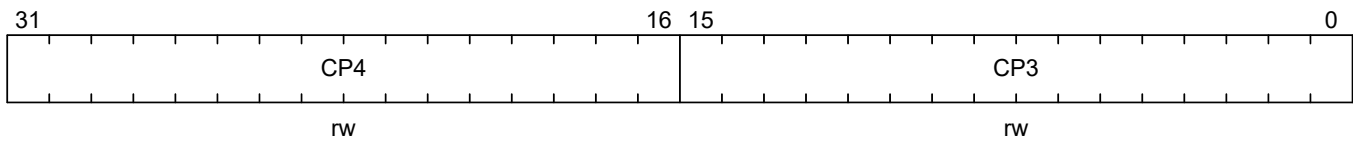
Back to [Register map](#).

# TPWM\_compare2

Compare values for PWM3 and PWM4

Address offset: 0x00000014

Reset value: 0xffffffff



Name	Bits	Mode	Reset	Description
CP4	31:16	rw	0xffff	Compare value for PWM4
CP3	15:0	rw	0xffff	Compare value for PWM3

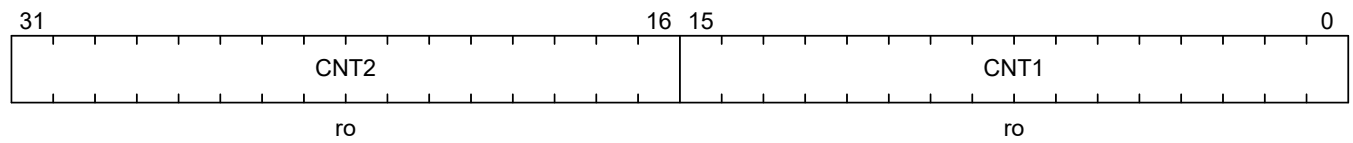
Back to [Register map](#).

# TPWM\_counter1

PWM counters for PWM1 and PWM2

Address offset: 0x00000018

Reset value: 0x00000000



Name	Bits	Mode	Reset	Description
CNT2	31:16	ro	0x0000	Current counter value for PWM2
CNT1	15:0	ro	0x0000	Current counter value for PWM1

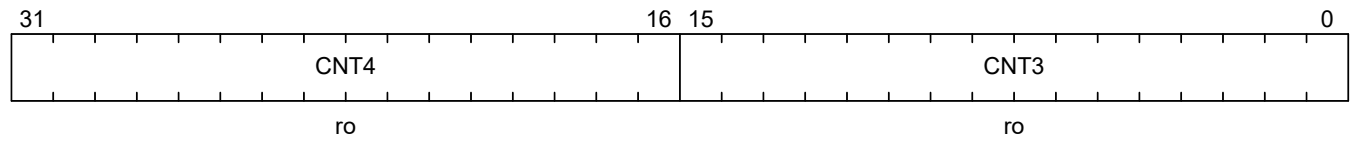
Back to [Register map](#).

# TPWM\_counter2

PWM counters for PWM3 and PWM4

Address offset: 0x0000001c

Reset value: 0x00000000



Name	Bits	Mode	Reset	Description
CNT4	31:16	ro	0x0000	Current counter value for PWM4
CNT3	15:0	ro	0x0000	Current counter value for PWM3

Back to [Register map](#).