

Um Breve Estudo da Adição de um Quarto Nível de Cache em Processadores Multicore

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Abstract

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1. Introdução

Nos últimos anos, a frequência de relógio dos processadores tem aumentado bastante. Paralelamente a isso, e devido a uma certa estagnação da velocidade dos cores [FIXME:ref], os fabricantes têm optado pela produção de processadores com vários núcleos de processamento (processadores *multicore*, com diversos *cores*). Exemplos disso são as arquitetura da Intel (*Dunnington* [FIXME:ref], *Nehalem* [FIXME:ref] etc.), AMD (*Barcelona* [FIXME:ref], *Budapest* [FIXME:ref], *Deneb* [FIXME:ref] etc.) e Sun (*Niagara* [FIXME:ref], *Victoria Falls* [FIXME:ref] etc.).

As memórias cache servem para reduzir o número de ciclos de latência que um processador deve esperar para acessar um determinado dado na memória. Reduzindo o número de ciclos, reduz-se o tempo necessário para acessar um dado. Por esta razão, o tempo de acesso a dados na memória cache é consideravelmente menor do que o tempo necessário para acessar a memória principal, por exemplo.

Contudo, ultimamente as aplicações têm cada vez um volume maior de dados a processar. Essa quantidade maior de dados, se não puderem ser acessados rapidamente pela unidade de processamento, podem implicar um pior desempenho do sistema. Além disso,

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References

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