6.2.8.2 Changes required to port to new multicore device

To map this code to additional CPUs, the only change required to this code is in the constant definitions for node and port numbers in the creation of endpoints.

6.3 Remote memory use cases

Use case 1 – accelerator core accesses host core's memory randomly using DMA and/or software cache

This use case aims to capture a common programming pattern for the Cell Broadband Engine processor. On the Cell processor the PPE (host) may launch a thread on an SPE (accelerator). The SPE can access (all of) PPE memory via DMA.

For certain kinds of access, particularly access to contiguous arrays in main memory, it is convenient to use DMA directly, using double or triple buffering to overlap communication with computation. This requires the use of *non-blocking* read and write operations on host memory.

For less regular types of access, but where there is likely to be some locality, it is common to use a software cache, which fetches data from main memory via DMA, but caches chunks of data locally to avoid repeated fetches. With a software cache, read and write calls are blocking.

The following use case illustrates these scenarios: we have two nodes, Node 1 and Node 2. Node 1 has a linked list data structure in memory, which Node 2 is going to process. For each element in the list, Node 2 will compute a score. The scores will be written back via DMA, as they are to be stored contiguously in Node 1's memory. The list elements will be read via a software cache as, we assume, they are relatively close together (e.g. perhaps the linked list elements are stored as an array, but are chained together in a non-contiguous order).

```
/*------------------------------------------------*/
/* Definitions common to Node 1 and Node 2        */
/*------------------------------------------------*/

typedef struct Entity_s {
      // DATA FIELDS (not specified here)
      struct Entity_s * next;
} Entity;

#define AGREED_ID_FOR_SW_CACHE 0 /* In a real application these IDs would
more likely be obtained */
#define AGREED_ID_FOR_DMA 1      /* by one node via MRAPI, and communicated
to the other node.    */




/*------------------------------------------------*/
/* Node 1 side of use case                        */
/*------------------------------------------------*/
```