6.2.2 Key functionality requirements

6.2.2.1 Control Task

There must be a control task collecting all data and calculating updates; this task must update engine parameters continuously; Updates to engine parameters must occur when the engine crankshaft is at a particular angle, so the faster the engine is running, the more frequently this task must run.

6.2.2.2 Angle Task

There must be a data task to monitor engine RPM and schedule the control task.

6.2.2.3 Data Tasks

There must be a set of tens to hundreds of task to poll sensors; the task must communicate this data to the control task.

6.2.3 Context/Constraints

6.2.3.1 Operating System

Often there is no commercial operating system involved, although the notion of time critical tasks and task scheduling must be supported by some type of executive; however this may be changing; possible candidates are OSEK, or other RTOS.

6.2.3.2 Polling/Interrupts

Sensor inputs may be polled and/or associated with interrupts.

6.2.3.3 Reliability

Sensors assumed to be reliable; interconnect assumed to be reliable; task completion within scheduled deadline is assumed to be reliable for the control task, and less reliable for the data tasks.

6.2.4 Metrics

6.2.4.1 Latency of the control task

Dependent on engine RPM. At 1800 RPM the task must complete every 33.33ms, and at 9000 RPM the task must complete every 6.667ms.

6.2.4.2 # dropped sensor readings

Ideally zero.

6.2.4.3 Latencies of data tasks

Ideally the sum of the latencies plus message send/receive times should be < latency of the control loop given current engine RPM. In general, individual tasks are expected to complete in times varying from 1ms up to 1600ms, depending on the nature of the sensor and the type of processing required for its data.

6.2.4.4 Code size

Automotive customers expect their code to fit into on chip SRAM. Current generation of chips often has 1Mb of SRAM, with 2Mb on the near horizon.

6.2.5 Possible Factorings

- 1 gp core for control, 1 gp core for data
- 1 gp core for control/data, dedicated SIMD core for signal processing, other SP cores for remainder of data processing
- 1 core per cylinder, or 1 core per group of cylinders