5 FAQ

Q: Is a reference implementation available? What is the intended purpose of the reference implementation?

A: A reference implementation is planned in the future. The current plan is to receive feedback on the draft specification and make modifications based upon the feedback. When the specification is near finalization, the MRAPI working group will announce the plans and schedule for such an implementation. The reference implementation models the functionality of the specification and does not intend to be a high performance implementation.

Q: Can you elaborate on how a hardware accelerators will interact with embedded processors using MRAPI? An API is a library of C/C++ functions, but it is not clear to me how an API can be used with a hardware accelerator, which can be very application specific.

A: The API can be implemented on top of a hardware accelerator. For example, an SoC may have hardware acceleration for mutexes, in which case an MRAPI implementation could utilize that hardware accelerator without the programmer needing to know how to interact with it directly.

Q: Does the API have testcases?

A: The API itself does not have testcases. However, as with the MCAPI example implementation which is available from the Multicore Association we would expect an MRAPI example implementation to contain testcases.

Q: Do you have implementations of the API that can be tested by the reviewers?

A: We are hoping to publish a simple POSIX implementation along with the spec.

Q: I assume MRAPI relies upon a "local" resource manager ? That is MRAPI must store state, and so needs a way to allocate state storage ?

A: It is up to the MRAPI implementation as to how resources are managed. Our simple initial implementation stores state in shared memory protected with a semaphore.

Q: I saw a statement that other solutions are too heavyweight because they target distributed systems. Does it mean that your goal is not to target the distributed system? What happens when we have a multi-chip multi-core? Isn't this the same distributed system?

A: To be clear, MRAPI targets cores on a chip, and chips on a board. MRAPI is not intended to scale beyond that scope.

Q: Is it possible to hide the differences between local and remote memory by just different properties of these memories? Remote memory will have higher latency, some access restrictions, etc.