Dashboard

Announcements

No announcements

Schedule: March 21-27,

Monday, Mar 24

Lecture

Microcontroller circuits

Lab 10 (Sec 1)

Assignments

Homework 10

Wednesday, Mar 26

Lecture

Serial Interfaces, I2C, SPI,

Interfacing Sensors, Pulse

Thursday, Mar 27

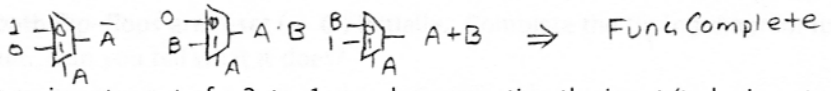
Lecture

Lab 10 (Sec 2)

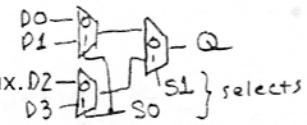
Assignment Details

Homework 10

Mar 24 Due: Monday at 4:30 pm Key

Multiplexers  ⇒ Func Complete

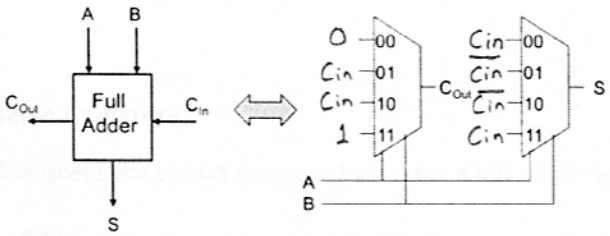
1. You can make an inverter out of a 2-to-1 mux by connecting the input (to be inverted) to the mux select input, connecting the mux data0 input to logical '1', and connecting the mux data1 input to logical '0'. Show that the 2-to-1 mux is functionally complete by showing it can be used to compute 'A and B' and 'A or B' as well.
[*Hint*: Try connecting A to the mux select input, and connecting the two data inputs to different combinations of B, B', '0', or '1'.]



2. Draw a circuit that uses three 2-to-1 muxes to make a 4-to-1 mux.

3. How many mux select inputs would a 32-to-1 multiplexer need to have? 5

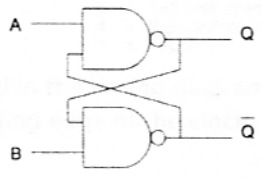
4. Below is a partial complete implementation of a full adder with two 4-to-1 muxes.



Complete the circuit diagram by connecting the data inputs of the two muxes to different combinatons of C_{in}, C'_{in}, '0', or '1', so that the muxes correctly compute C_{out} and S.

Set-Reset Flip-Flops

1. In class, we showed how a set-reset flip-flop could be made from two cross-coupled NOR gates. You can also make a set-reset flip-flop from two cross-coupled NAND gates, as shown below:



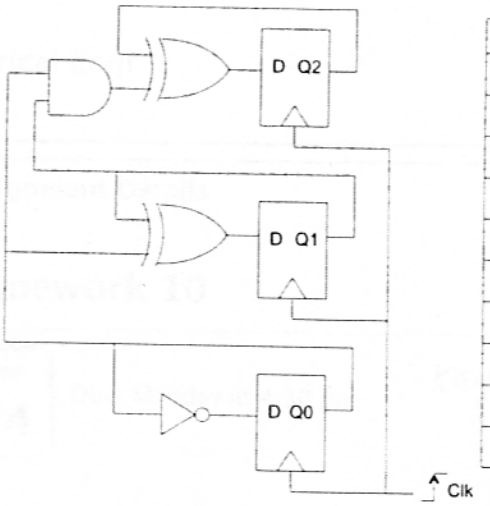
AB	Q
00	Illegal
01	1 (set)
10	0 (reset)
11	hold

(Set, Reset, Hold, Illegal)

Analyze this circuit and complete the truth table above that describes what happens to Q for each combination of A and B, The choices are set, reset, hold, or illegal.

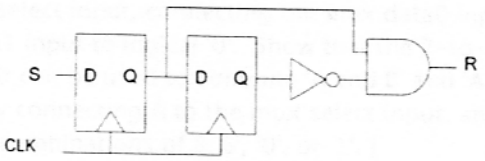
Counters and Timing Diagrams

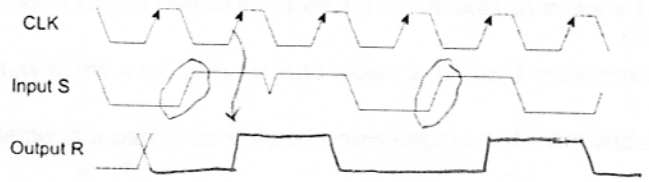
1. The counter below changes state on the rising edge of the clock. Fill in the table below showing the count sequence of this counter starting at 000.



Q2 Q1 Q0
0 0 0
0 0 1
0 1 0
0 1 1
1 0 0
1 0 1
1 1 0
1 1 1
0 0 0
0 0 1

2. Assume that both flip-flops are reset (= 0) initially. Complete the timing diagram for the following circuit. Can you tell what it does?

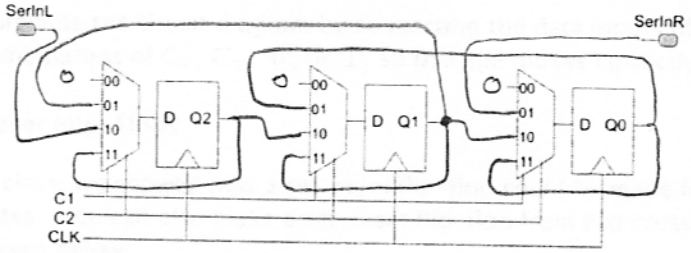




Output R goes high for 1 cycle anytime anytime input S has a rising edge.

Loadable Registers

1. Complete the circuit diagram below for a left-shift right-shift register.



C1	C2	Q
0	0	Clear
0	1	Left Shift (SerInR to Q0)
1	0	Right Shift (SerInL to Q3)
1	1	Hold

Fill in the timing diagram below for the above circuit by filling in the values of Q after each rising edge of the clock.