

## Quiz #37 – Counter Fun

The diagram shows a 3-bit shift register. It consists of three D flip-flops labeled Q2, Q1, and Q0 from left to right. The output of Q2 is connected to the input of Q1, and the output of Q1 is connected to the input of Q0. The output of Q0 is connected to an OR gate. The output of the OR gate is connected to the input of Q2. A common clock signal, labeled 'Clk', is connected to the clock input of all three flip-flops.

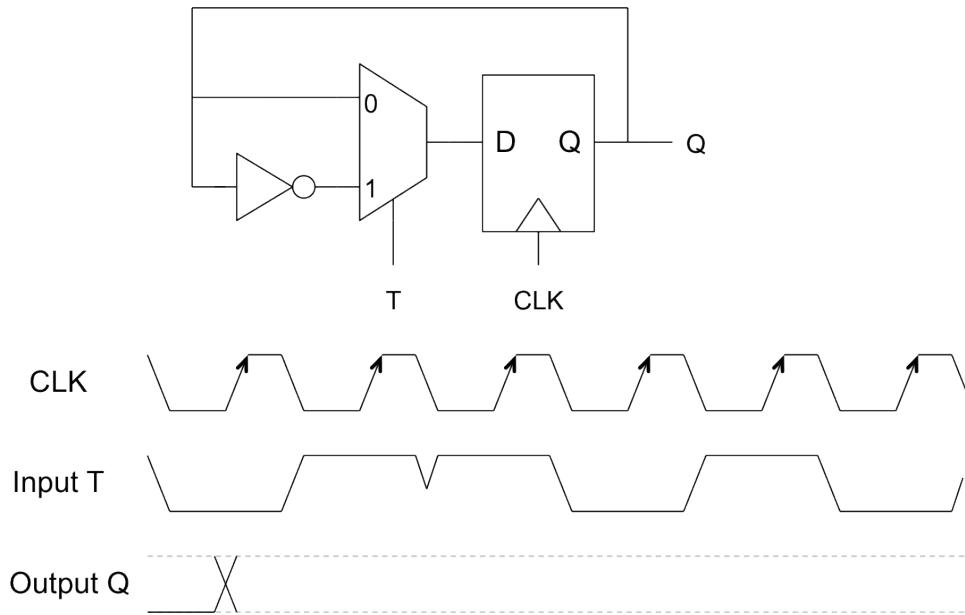
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ECEn 301

Quiz #38 – Timing Diagram

Name: \_\_\_\_\_

Fill in the timing diagram for the circuit below.

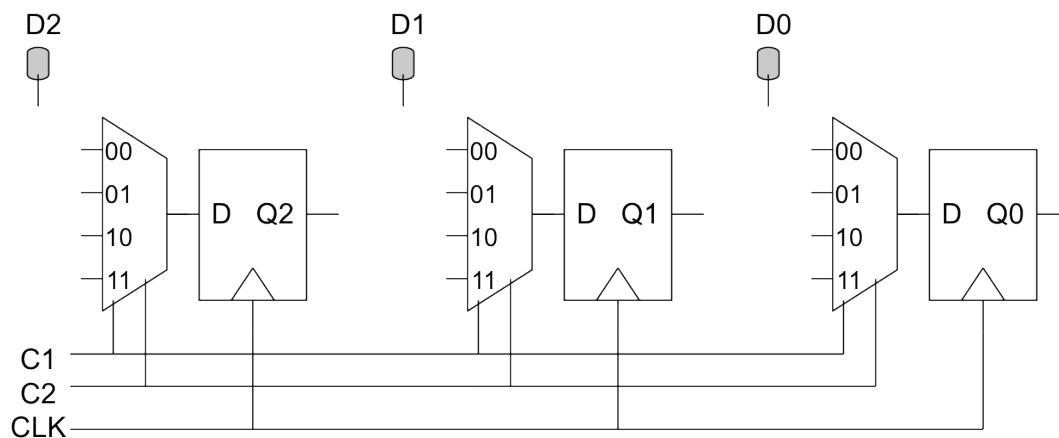


# ECEn 301

## Quiz #39 – Loadable Register

Name: \_\_\_\_\_

Complete the loadable register circuit below.



C1	C2	Q
0	0	Hold
0	1	$\sim Q$
1	0	Rotate Left ( $Q2 \leftarrow Q1 \leftarrow Q0 \leftarrow Q2$ )
1	1	Load D

Fill in the timing diagram below for the above circuit by filling in the values of Q after each rising edge of the clock.

