**CS2100 Computer Organisation**

# Lab #9: Decoder

(Week 11: 30 October – 3 November 2023)

[ This document is available on Canvas and course website https://www.comp.nus.edu.sg/~cs2100 ]

***Remember to bring this along to your lab!***

Name: _____ Student No: _____

Lab Group: _____

**Important:** You should complete the report before you come for your lab or you may not have enough time to complete it.

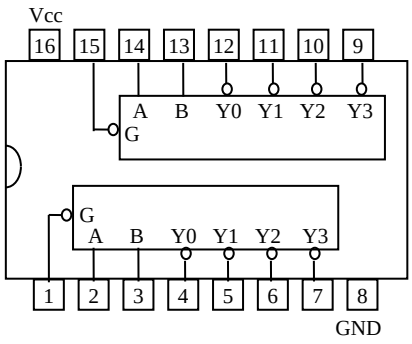
## Objective:

In this experiment, you will use the decoder to implement some logic functions.

## IC chips:

1. One **74LS139** chip (DUAL 2×4 decoder with negated output and zero-enable).
2. One **74LS20** chip (DUAL 4-input NAND gates).

The decoder chip you will use in this lab is the 74LS139, which contains two sets of 2×4 decoder with *negated outputs* and *zero-enable*. The pin configuration and the function table are given below.




Function Table of 74LS139

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| Enable | Select | | | | | |
| G | B | A | Y0 | Y1 | Y2 | Y3 |
| 1 | X | X | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 |

1 = High, 0 = Low, X = don't care

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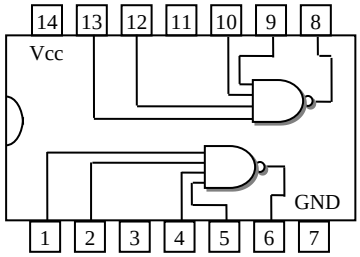
The 74LS20 chip contains two 4-input NAND gates. The pin configurations are shown below.




74LS20

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## Propagation delay:

Assume that the propagation delay for every NAND gate in 74LS20 is 15 ns (nano-seconds), and the propagation delay for each decoder in 74LS139 is 35 ns.

**Procedure:**

1. Given a 3-variable function ***S(P,Q,R) = (P + Q + R)·(P + Q')·(P' + R)***, write this function in the **product-of-maxterms** form, using the Π*M* notation. [1 mark]

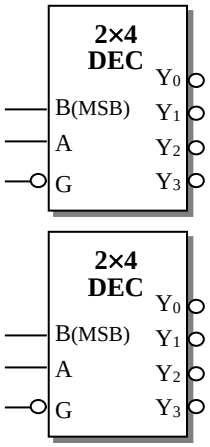
   $S(P,Q,R) = \Pi\ M\ ($ _____ $)$

2. Complete the truth table for *S* below. [1 mark]

| ***P*** | ***Q*** | ***R*** | ***S*** |
|---|---|---|---|
| 0 | 0 | 0 | **0** |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

3. With the truth table above, implement function *S* using the 2×4 decoders in the 74LS139 chip, and NAND gates in the 74LS20 chip. Connect the inputs *P*, *Q*, and *R* to SW7, SW6 and SW5 on your logic trainer respectively.

   Complete the following logic diagram. [5 marks]




4. Show your implementation implementation of the above circuit to your labTA before dismantling the circuit and moving on to another circuit in step 7. [5 marks]

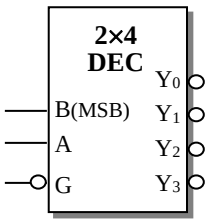
5. What is the propagation delay of your circuit above? _____ ns. [1 mark]

6. Given a 4-variable function $F(W,X,Y,Z) = \Pi M(3, 7)$, write out the simplified SOP expression for *F* below. [2 marks]

   Simplified SOP expression: $F =$ _____

7. Use the block diagram below to illustrate how you might implement *F* using only **ONE** such 2×4 decoder (with negated output and zero-enable), without any additional logic gate. Due to time constraint, you are NOT required to actually implement this circuit on the logic trainer.

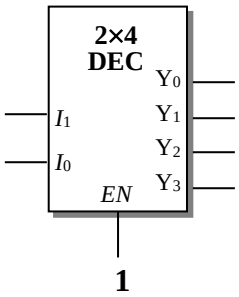
   Complete the diagram below. [2 marks]

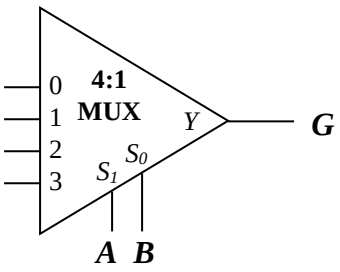



8. Using one 4:1 multiplexer and one 2×4 decoder with 1-enable as shown below, show how you might implement function $G(A,B,C,D) = \Sigma m(0, 6, 9, 15)$ without using any additional logic gate. Complete the diagram below. [3 marks]

   Note that the selector lines for the 4:1 multiplexer have been fixed to *AB*, and you must not change it.

   You do not need to implement this since you are not given any multiplexer in this lab.




Marking Scheme: Report (15 marks), Circuit (5 marks); Total: 20 marks.
Your graded report will be returned to you at the next lab.