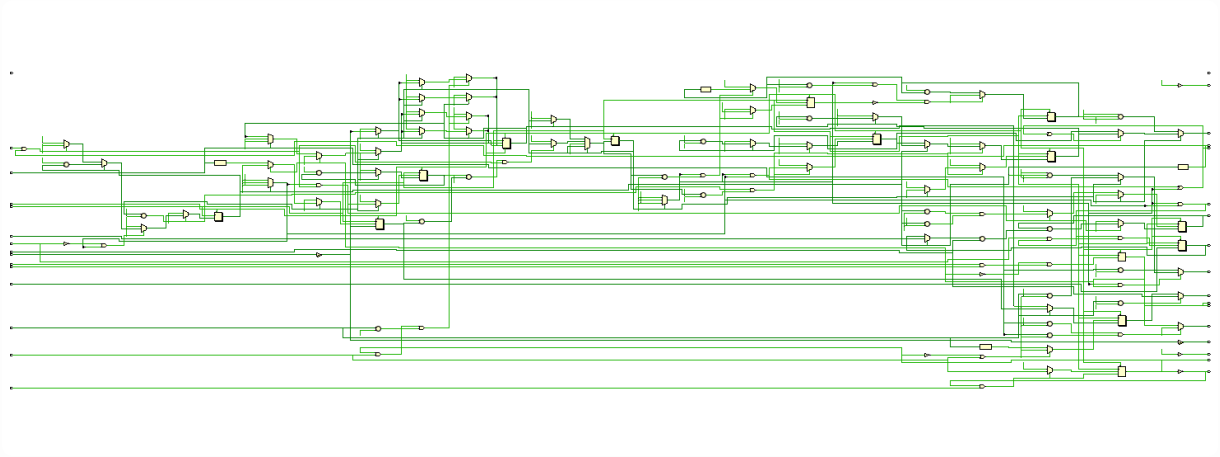
1.



2.operation

Write:

In the next cycle when AW_valid and W_valid are both 1, AWR_ready and W_ready are pulled high at the same time, and the value of awaddr is read and tap_RAM is written in this cycle.

Read:

When AR_valid and AR_Ready are read as High at the same time, the value of Tap_RAM is put into the Data of R channel in the next cycle, and R_valid is also pulled high.

Idle: In the Idle stage, each value in Data_Mem will be cleared to 0 first, and wait for ap_start to be pulled to 1. During this phase, the transmission of AXI_Lite continues, and the external Master will pass the Tap parameters and ap_start into the FIR using AXI_Lite.

Start: In Start, FIR starts to process the Data from AXI_Stream. After each piece of Data is processed, fir_data_cnt will be increased by 1 until it is added to fir_data_cnt == length – 1. At this time, if the final Data is calculated and transmitted, it will enter the Done State.

Done: This cycle sets ap_done and ap_idle to 1 and enters the Idle phase.

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3 Resource usage

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	282	0	53200	0.53
LUT as Logic	282	0	53200	0.53
LUT as Memory	0	0	17400	0.00
Slice Registers	180	0	106400	0.17
Register as Flip Flop	180	0	106400	0.17
Register as Latch	0	0	106400	0.00
F7 Muxes	0	0	26600	0.00
F8 Muxes	0	0	13300	0.00

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	140	0.00
RAMB36/FIFO*	0	0	140	0.00
RAMB18	0	0	280	0.00

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	3	0	220	1.36
DSP48E1 only	3			

Bonded IOB	329	0	125	263.20
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	4	0.00
PHASER_REF	0	0	4	0.00
OUT_FIFO	0	0	16	0.00
IN_FIFO	0	0	16	0.00
IDELAYCTRL	0	0	4	0.00
IBUFDS	0	0	121	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	16	0.00
PHASER_IN/PHASER_IN_PHY	0	0	16	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	200	0.00
ILOGIC	0	0	125	0.00
OLOGIC	0	0	125	0.00

4 Time

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	685	Total Number of Endpoints:	685	Total Number of Endpoints:	NA

5 waveform