BLDC Closed-Loop Speed Control Based on CY8C24x33

AN42102

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Application Note Abstract

This application note details the implementation of Brushless DC motor (BLDC) closed-loop speed control using the PSoC® device CY8C24x33. Hardware over-current protection in BLDC control application is also explained.

Introduction

Brushless DC motor is now replacing the traditional brushed DC motor which has higher reliability, higher efficiency, and lower noise. BLDC is popular in almost every field such as consumer electronics, home appliances, and industrial controls.

Development of high performance BLDC control systems requires higher accuracy. This is achieved by using closed-loop control in a majority of BLDC control systems.

This application note describes BLDC closed-loop speed control based on the Cypress PSoC chip CY8C24x33. This chip can be used in BLDC motor control applications such as E-bike.

BLDC

The advantages of BLDC motors over brushed DC motors are:

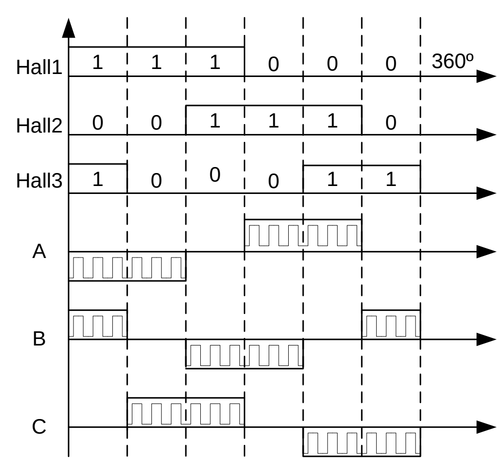
- High efficiency
- Reliable and no arcing on commutation – no brushes to maintain
- Higher speed and power-to-size ratio
- Heat is generated in stator – easy to remove
- Lower inertia – no commutator
- Higher acceleration rate

BLDC motors are considered more efficient than brushed DC motors. For the same input power, a BLDC motor converts more electrical power into mechanical power than a brushed motor because of the absence of friction due to brushes.

In BLDC motors, the commutation is controlled electronically. The motor requires the stator windings be energized in a particular sequence. To implement this sequence, it is important to know the rotor position. This is done by using sensors such as Hall-Effect sensors (sensored control), or by sensing back EMF (sensorless control). Hall-Effect sensors are embedded in the stator. When the rotor magnetic poles pass near the hall sensors, they supply a high or low signal, indicating that the north or south poles are passing near. The position of the rotor is derived with the exact combination of the three hall sensor signals.

This application introduces the sensored BLDC. Three position sensors provide current position of motor. Position sensors output high or low level. Position sensors toggle each 180 electrical degrees of electrical rotation. A timing diagram of sensor outputs and the required motor driving voltages is shown in Figure 1.

Figure 1. BLDC Sensor Output vs. Commutation Timing



Refer to AN2227 and AN2228 for more details on BLDC.

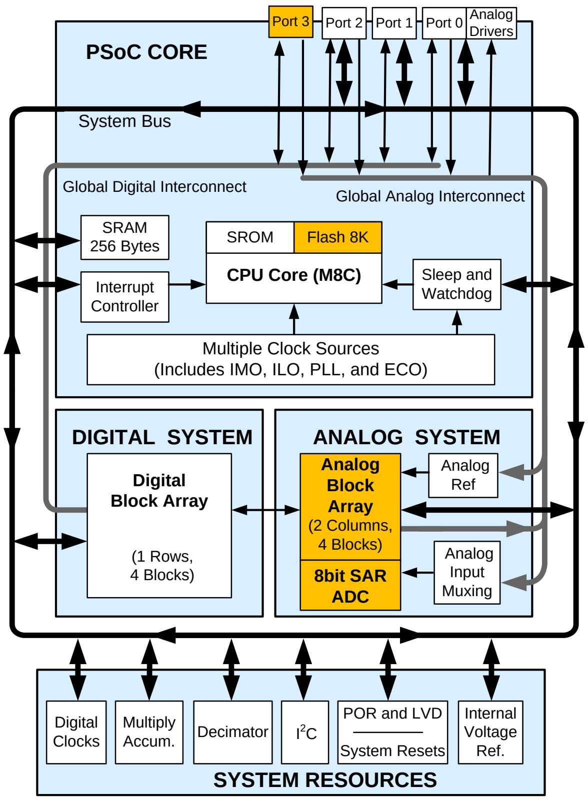
CY8C24x33 Introduction

CY8C24x33 derives from the CY8C24x23A family, which has the following improvements:

- Flash memory is doubled from 4K in CY8C24X23 to 8K in CY8C24x33;
- SC blocks of Column 0 in CY8C24x23A are replaced with a SAR (Successive Approximation Register) ADC with a higher sample rate of 300 Ksps;
- GPIO increases from 24 I/Os in CY8C24x23A up to 26 I/Os.

A block diagram of the features is shown in Figure 2. The difference between CY8C24x33 and CY8C24x23 is marked with yellow or a darker gray when printing to a black and white printer.

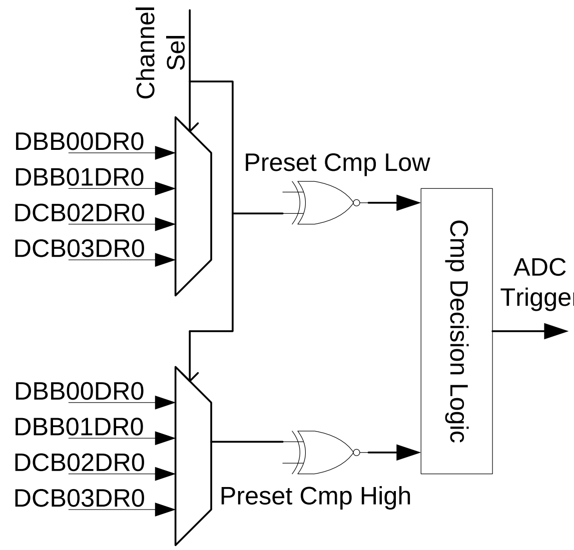
Figure 2. Block Diagram of CY8C24x33



The ADC in CY8C24x33 is an optimized SAR ADC, which has a conversion time of 3.33 µS. A high conversion rate is critical in some applications. A typical application is motor control, in which an ADC with a high sample rate is used to sample the motor current for over-current protection and back EMF detection.

Another feature of the optimzed ADC is the auto aligned trigger function. The block diagram of this feature is shown in Figure 3.

Figure 3. ADC Auto-Trigger Function



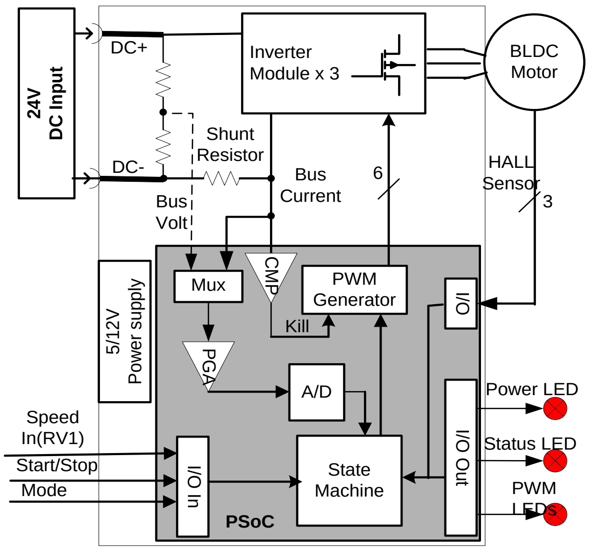
A description of auto-align functions are as follows:

- There are two channels, trigger compare high and low, which are used for ADC auto-triggering.
- Each or both channels can be selected to trigger ADC.
- Both channels can act as two separate 8-bit trigger sources or can be combined as a 16-bit trigger source.
- For each compare channel, one of the four digital modules can be selected as compare input.
- If two compare channels are combined as a 16-bit trigger source, then the high and low channels' compare input is combined together as a 16-bit input.

BLDC Control Based on PSoC

The block diagram of BLDC motor control based on PSoC is shown in Figure 4.

Figure 4. BLDC Motor PSoC Controller



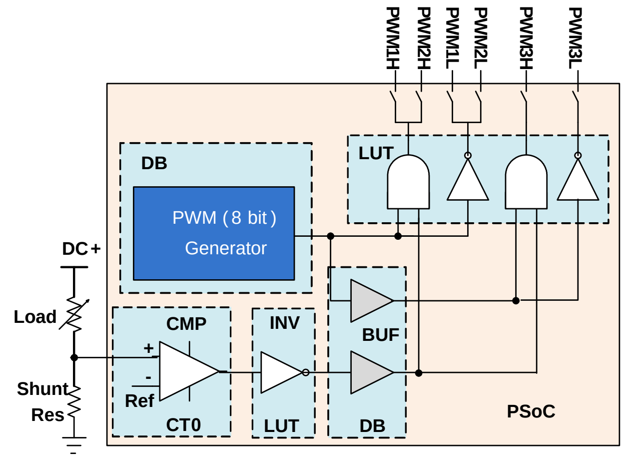
The input signals and its functions are as follows:

- Speed command (RV1).
- Motor current detection: Cut off power device driver to protect motor when over-current.
- Battery voltage: System low battery protection.
- Hall sensor: Output of hall sensors provide position of motor. This is used for commutation.
- Other inputs: Start/Stop motor button (SW1) and Mode button (SW2).

Outputs from PSoC are power device driver signals. The high sides of power device driver signal are PWM output. The low sides of power device driver signal is the invert of PWM output of high side.

The highlight of the E-Bike implementation is over-current protection of PSoC hardware implementation. Figure 5 shows a block diagram of PSoC over-current protection.

Figure 5. Block Diagram of Over-current Protection



The PSoC resources used in BLDC over-current protection are:

- A digital block is placed with PWM8; its output is the driving signal of a power device.
- A Continuous Time block (ACB00) is placed with a comparator (CMPPRG). The first input of the comparator is the voltage of the shunt resistor, which is proportional to the current flowing into the motor. The second input is the reference voltage set according to the application. Comparator outputs are high when the shunt voltage is higher than the reference voltage, else the outputs are low.
- Another digital block is placed with a digital buffer (DigBuf). It has two simple two-input two-output digital buffers. PWM and comparator outputs route through the DigBuf module.
- The PWM output is also routed through Input1 of DigBuf to Row Output Bus.
- The over-current signal and comparator output are routed through Input2 of DigBuf to Row Output Bus.
- The over-current signal and the PWM output logically cuts off the PWM output when over-current occurs.

The over-current protection mechanism is an on-chip low cost solution.

CY8C24x33 PI Closed-Loop Speed Control

PSoC system resources include an on-chip register based Multiply Accumulate (MAC). The MAC block is a fast 8-bit multiplier or a fast 8-bit multiplier with 32-bit accumulator. To execute a multiply, write the value to any internal multiplicand register. Immediately after the write of the multiplicand, the product is available at product registers. The Multiply Accumulate calculation has the same operation. The MAC block is a very useful resource for the PI algorithm.

The PI control algorithm is very useful in a continuous control system. There are two basic PI control algorithms: position mode and increment mode PI control algorithm. The following equation is a discrete expression of position mode of the PI algorithm.

$$u_{\mathrm{k}} = K_{\mathrm{P}} * e_{\mathrm{k}} + K_{\mathrm{I}} * \sum_{i=1}^{k-1} e_i + u_0 \qquad \text{Equation 1}$$

The disadvantages of the position mode PI algorithm are:

- Switching between closed-loop and open loop has system impulsive force, which results in an unstable motor.
- Output of position mode PI control is related to all status in the past. So simulating an error is unavoidable because of the accuracy of MCU calculation.

The disadvantages can be solved by using the increment mode PI algorithm. The formula is shown in the following equation.

$$\Delta u_{\mathrm{k}} = u_{\mathrm{k}} - u_{\mathrm{k-1}} = K_{\mathrm{P}} * (e_{\mathrm{k}} - e_{\mathrm{k-1}}) + K_{\mathrm{I}} e_{\mathrm{k}} \qquad \text{Equation 2}$$

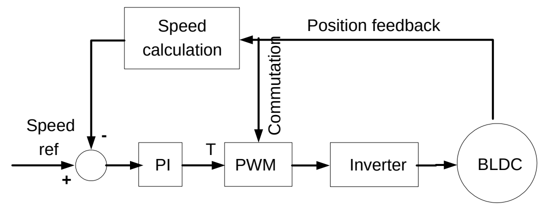
The control increment is output, which is added to the current control input. MCU implementation also becomes easier.

In closed-loop speed PI control system:

e_k is speed error.

Figure 6 is the block diagram of PSoC PI closed-loop speed control.

Figure 6. PSoC PI Closed-Loop Speed Control



Summary

Cypress BLDC closed-loop speed control based on the CY8C24x33 is an optimized solution. It implements on-chip hardware over-current protection, which is very important in BLDC control to avoid over-current damage. The PSoC BLDC motor control solution also has low total system cost.

Appendix A

Schematic

Figure 7. Main Control Schematic

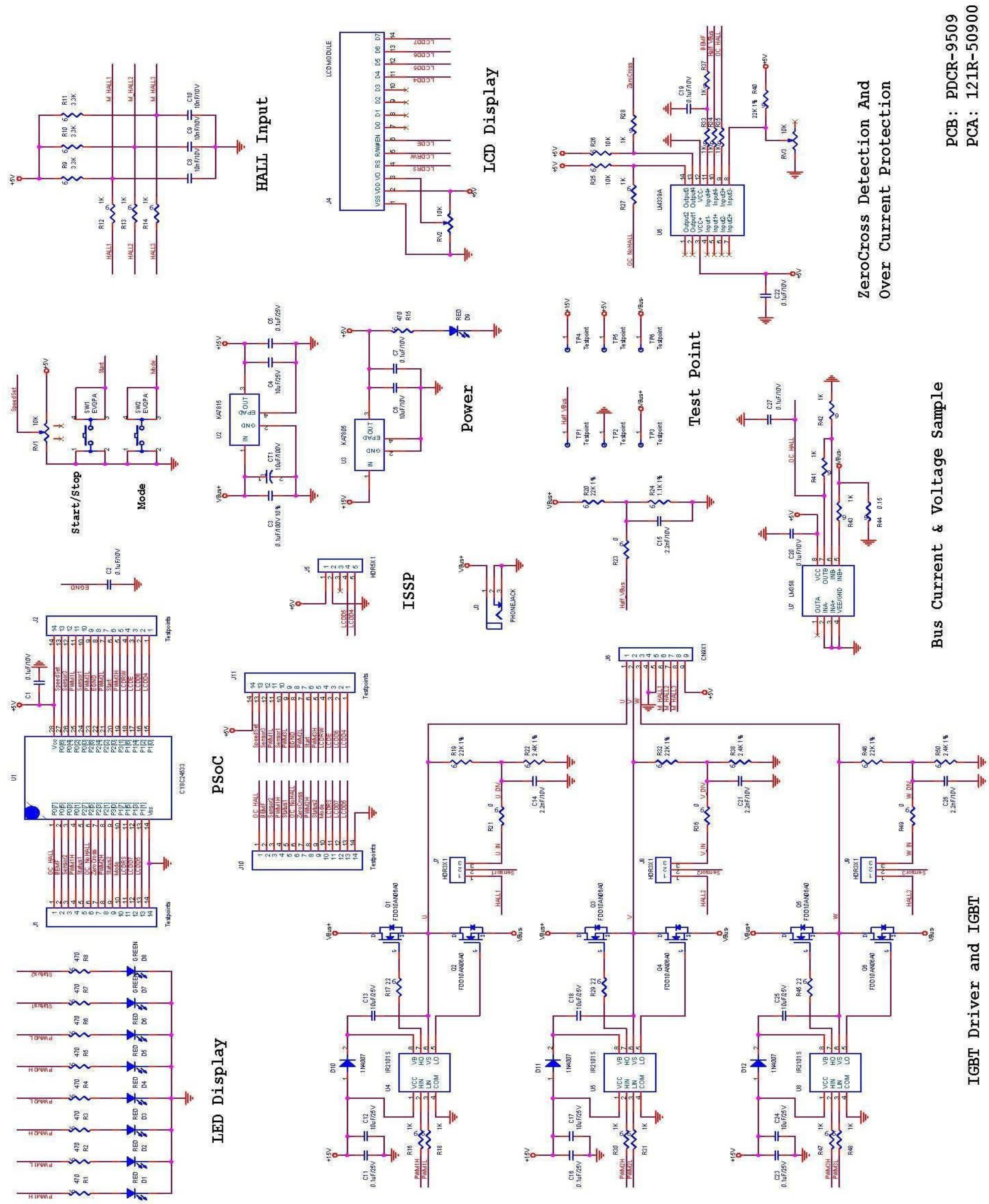
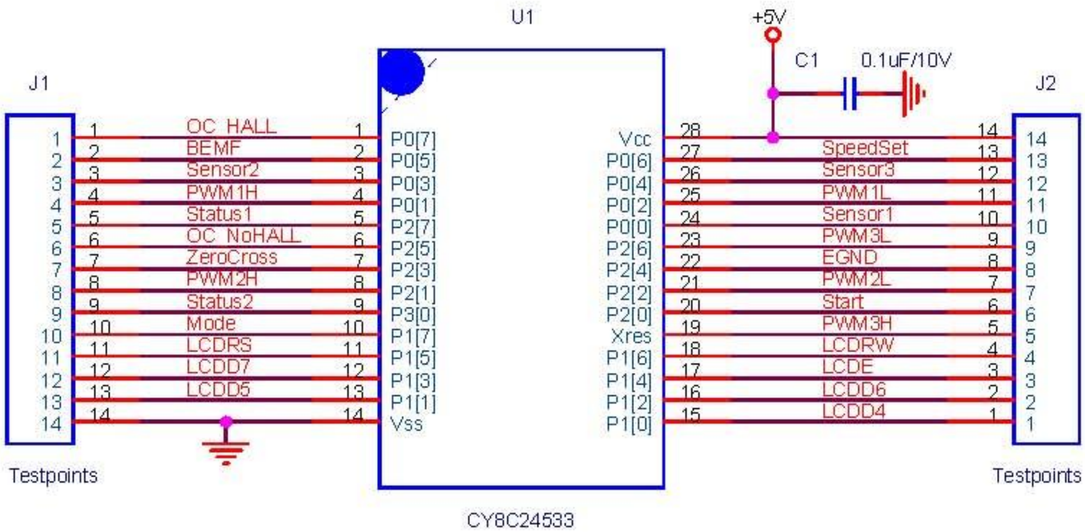
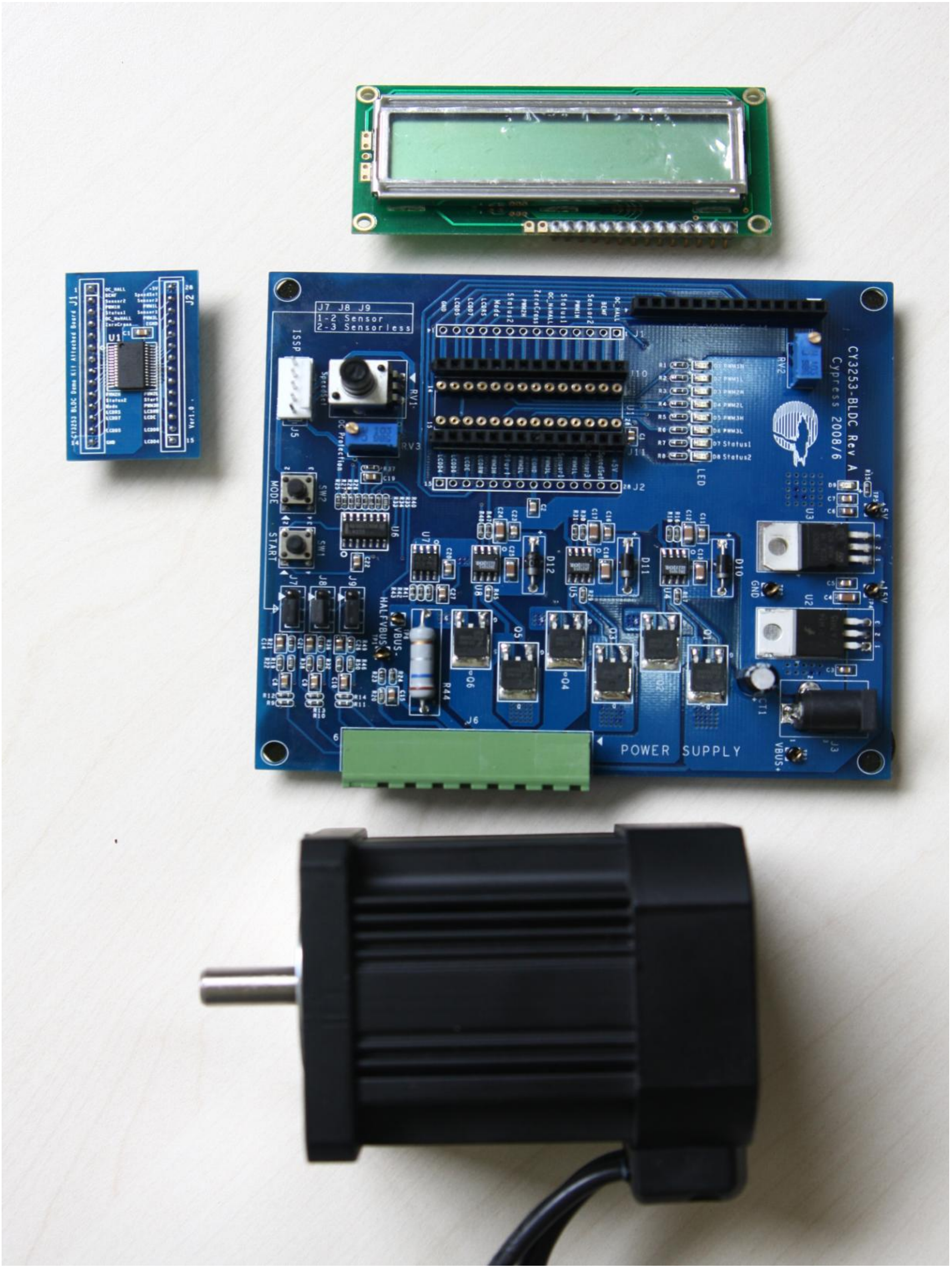


Figure 8. Daughter Board Schematic



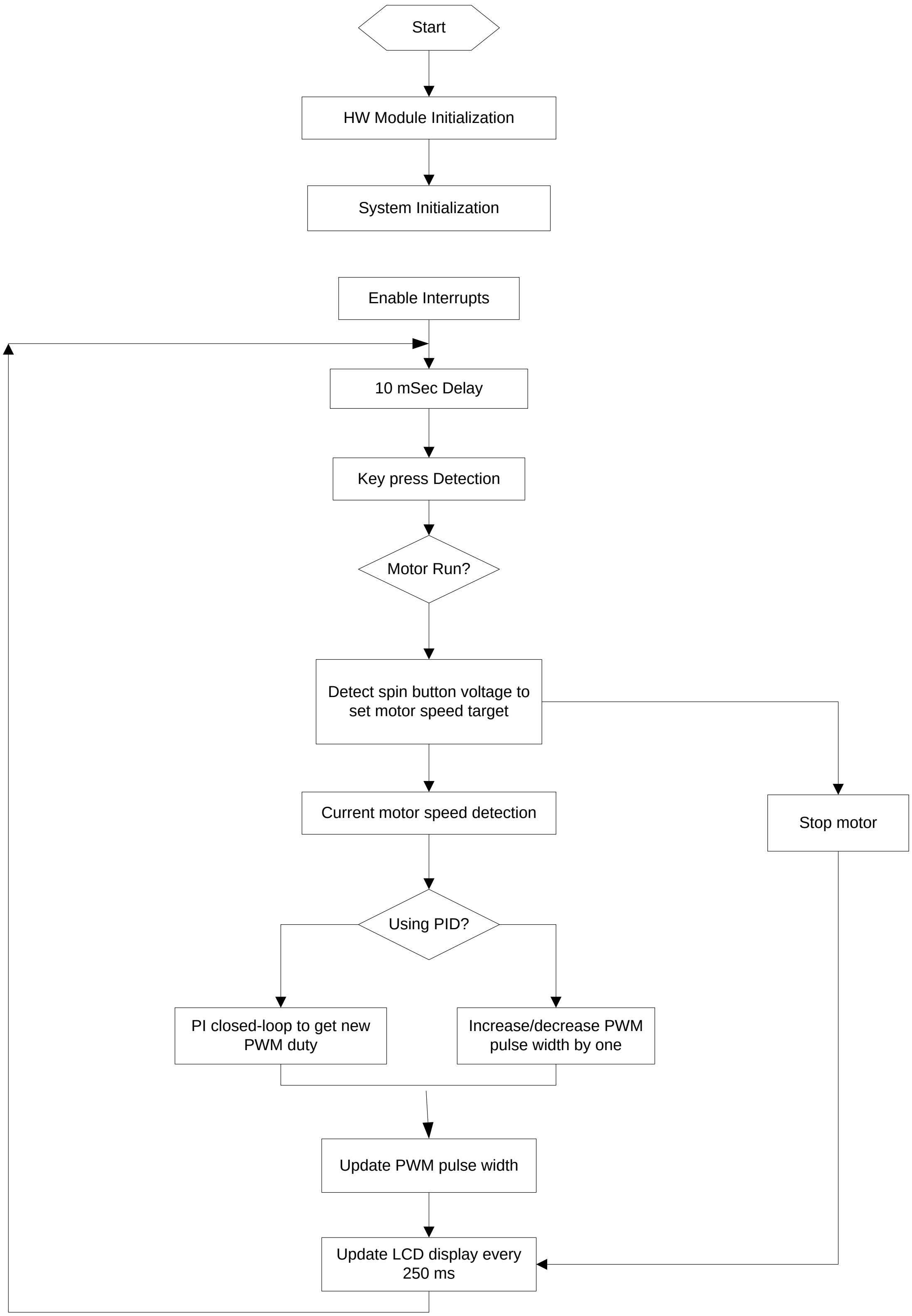
Appendix B

Figure 9. Demo Board



Appendix C

Figure 10. Main Flowchart



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