Report

I want to use two late tokens for lab6

In this experiment, we implemented two jumps, namely conditional jump and unconditional jump. And we implemented the flush function. First, it is predicted that the branch does not jump. If we detect that the rd signal is 0, that is, when we need to perform a branch jump, the flush signal is 1. At this time, the written instruction signal needs to be returned to 0. So as to realize the flushing function.

Compilation order:

The PC part outputs the address to the imem part, and the imem part outputs the instruction signal to the IF/ID part. Under normal circumstances, IF/ID will transmit instructions to registers and Hazarddetect, as well as CPU, ID/EX part. The command signal output from the IF/ID will enter the hazard part,When the ifflush signal is 1, the command signal and the pc signal that should be output by the ifid part will be changed to 0.

In the ID/EX part, the signals output by the register and cpucontrol will enter the ID/EX, and the ID/EX will transmit the signal to enter the two selectors of three options and the Forwarding unit. These two multiplexers are composed of forwardA and forwardB Controlled, transmitted to the ALU component after multiple operations.

MEMWB, and finally write back to the corresponding register to change the value of the corresponding register

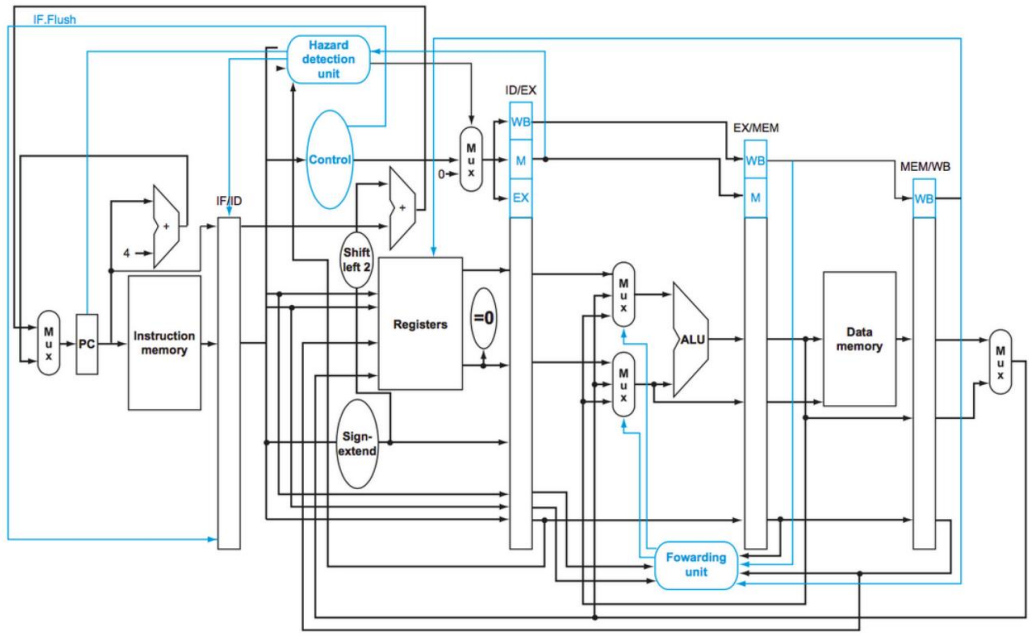


Figure 1: the circuit of assignment 6

```
SUB X23, X20, X19     11001011000100110000001010010111
CBZ X23, 5            10110100000000000000000010110111
ADD X9,  X9, X9       10001011000010010000000100101001
SUB X24, X22, X21     11001011000101010000001011011000
CBZ X24, 3            10110100000000000000000001111000
ADD X10, X10, X10     10001011000010100000000101001010
ADD X11, X11, X11     10001011000010110000000101101011
ADD X12, X12, X12     10001011000011000000000110001100
B 2                   00010100000000000000000000000010
ADD X19, X19, X19     10001011000100110000001001110011
ADD X20, X20, X20     10001011000101000000001010010100
nop
nop
nop
nop
```

Figure 2: the instruction sequences

following is the waveform diagram of lab6. During the operation of the instruction, in this experiment, I advance some signals such as signextend to the Ifid stage. And because I perform the jump whether to execute the jump instruction in the ifid stage, therefore, In my opinion, the processor will execute the CBZ 23, 5 branch instruction, because the value of x23 is still 0 at this time (ifid stage).

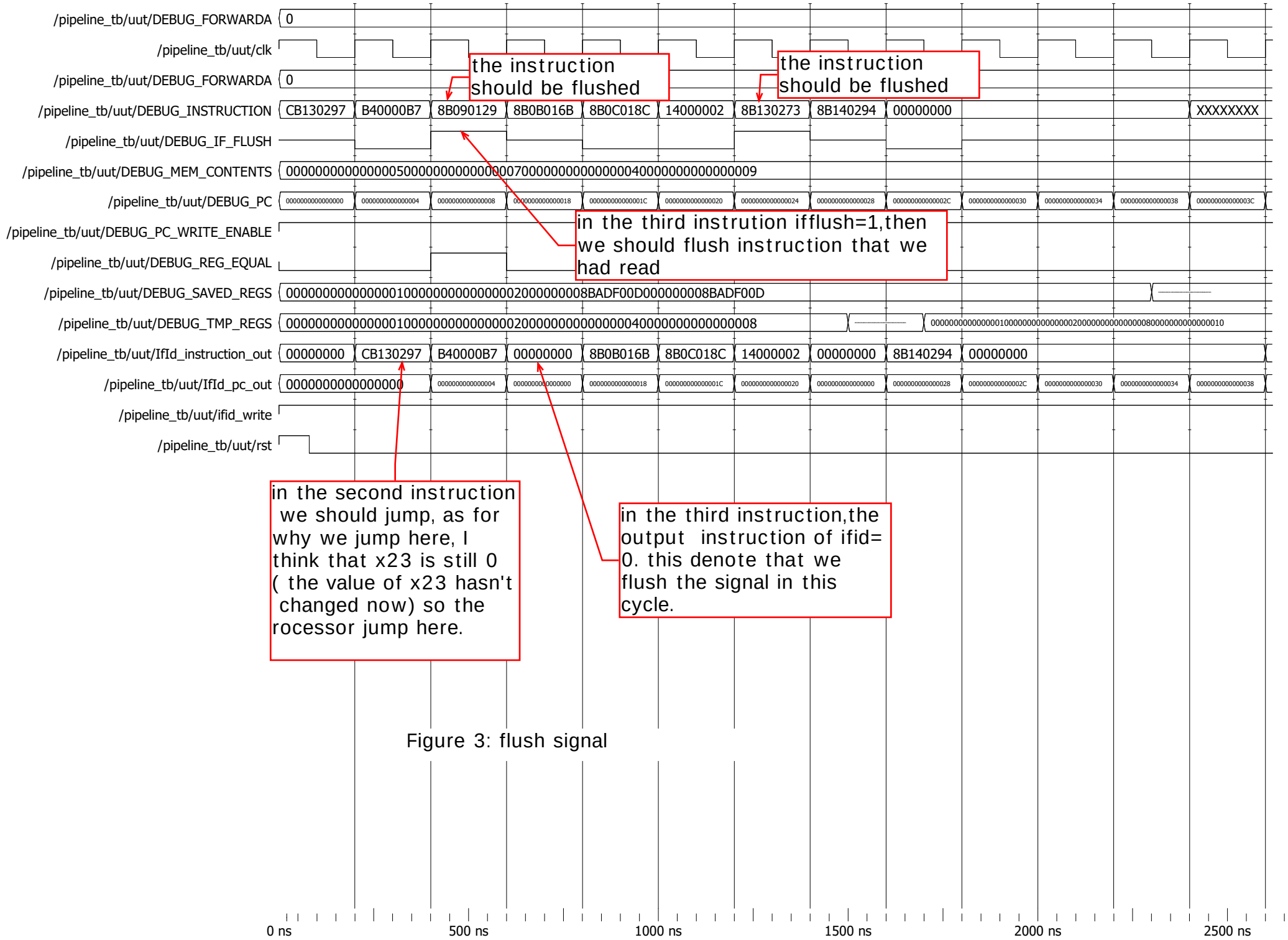


Figure 3: flush signal

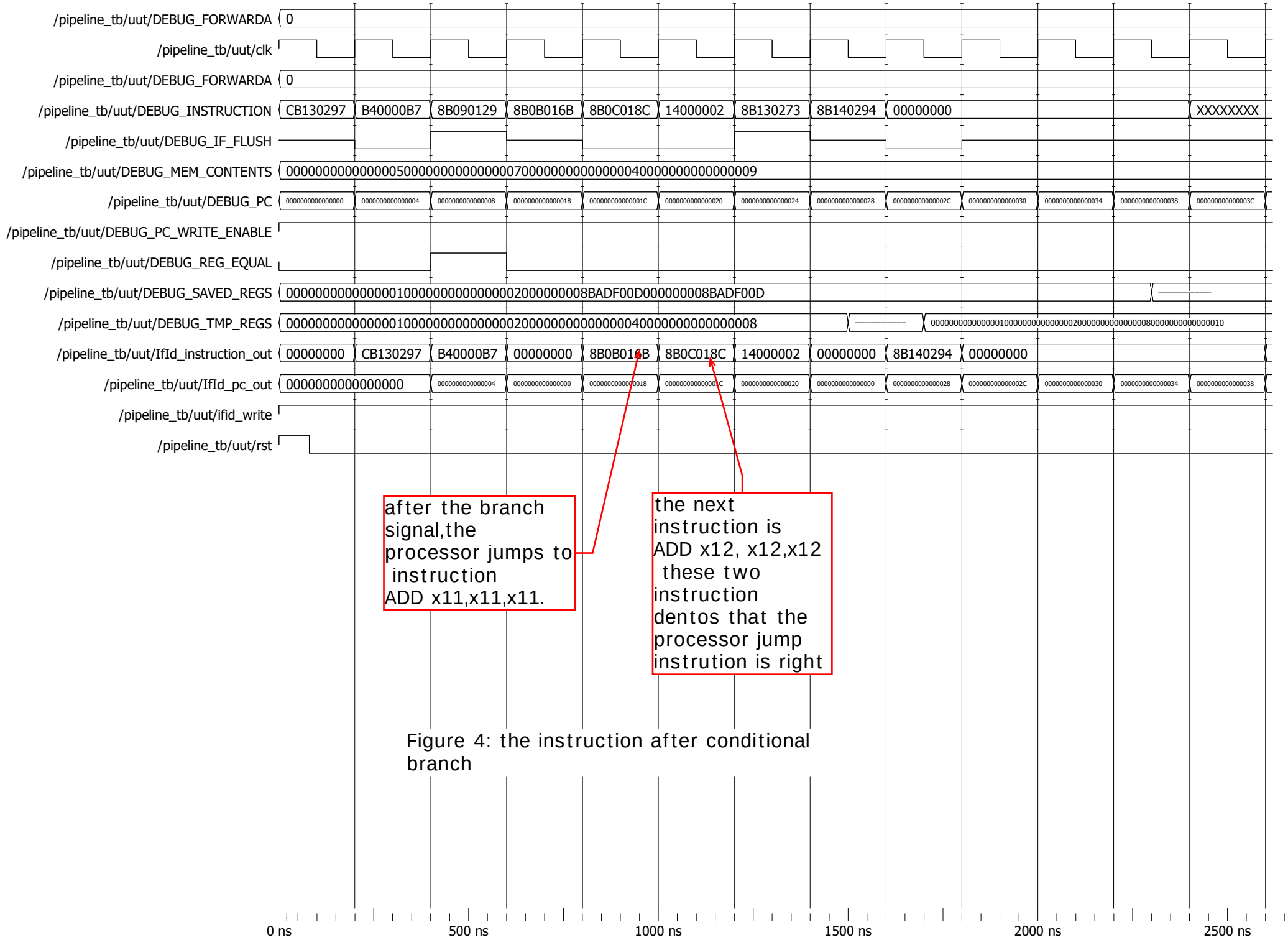


Figure 4: the instruction after conditional branch

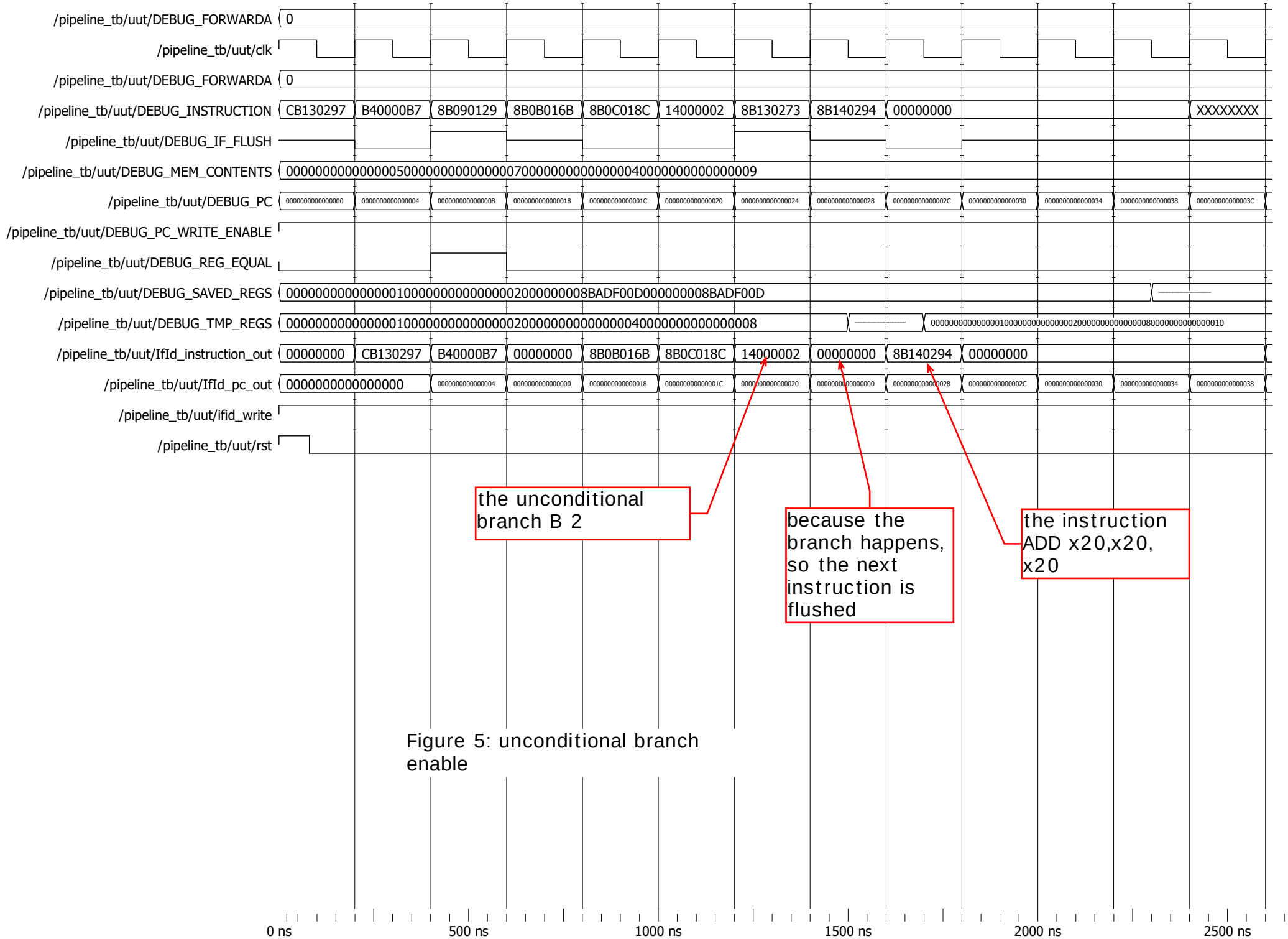
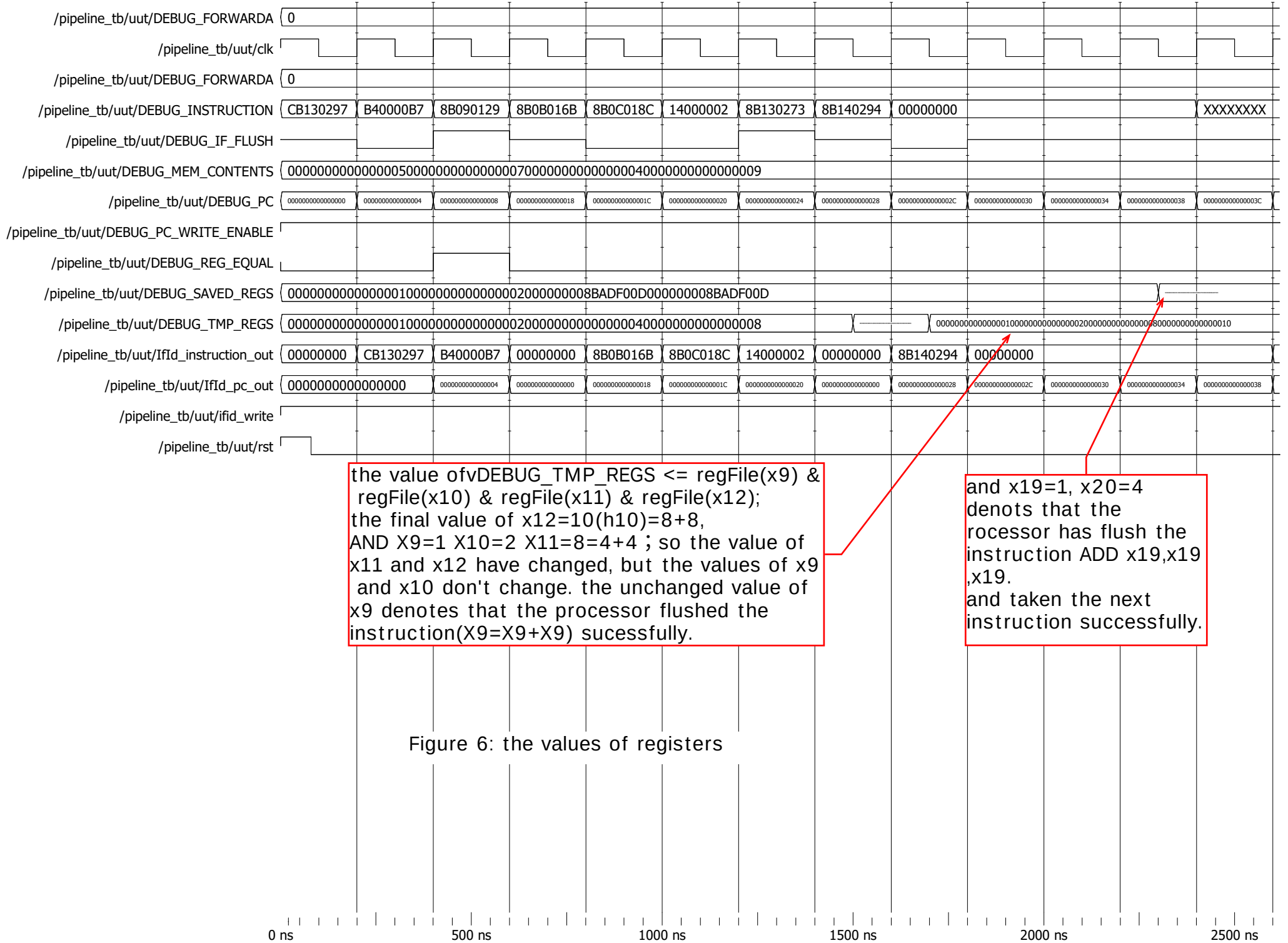


Figure 5: unconditional branch enable



the value ofvDEBUG_TMP_REGS <= regFile(x9) & regFile(x10) & regFile(x11) & regFile(x12);
the final value of x12=10(h10)=8+8,
AND X9=1 X10=2 X11=8=4+4 ; so the value of x11 and x12 have changed, but the values of x9 and x10 don't change. the unchanged value of x9 denotes that the processor flushed the instruction(X9=X9+X9) sucessfully.

and x19=1, x20=4 denots that the rocessor has flush the instruction ADD x19,x19 ,x19.
and taken the next instruction successfully.

Figure 6: the values of registers

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