Digital Design and Computer Organisation Laboratory

UE22CS251A

3rd Semester, Academic Year 2023-24

Date: 04/09/2024

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Week:4 Program Number:1

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A 2: 1 MULTIPLEXER. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE

I. Verilog Code and Test Bench Code

1.mux.v

```
module mux2 (
    input wire i0, i1, j,
    output wire o
);
assign o = (j == 0) ? i0 : i1;

endmodule
```

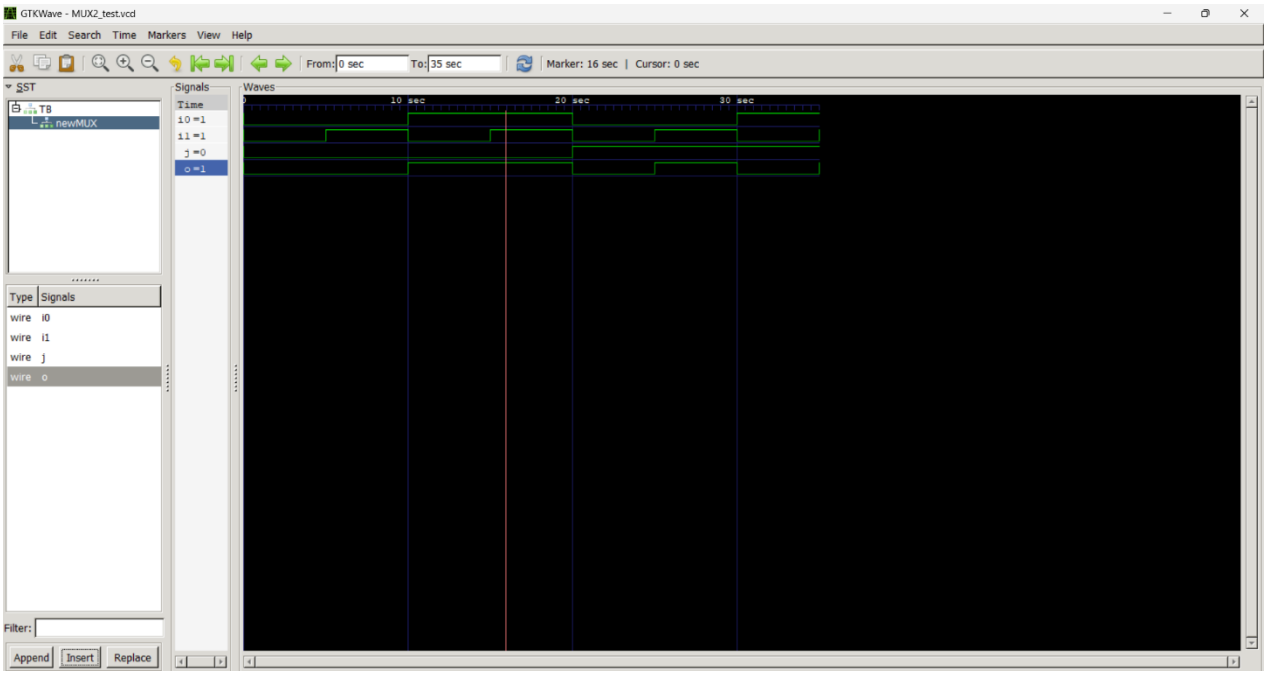
2.mux_tb.v

```
module TB;
    reg A, B, S;
    wire X;
    mux2 newMUX(.i0(A), .i1(B), .j(S), .o(X));

    initial begin
        S = 1'b0; A = 1'b0; B = 1'b0;
        #5 S = 1'b0; A = 1'b0; B = 1'b1;
        #5 S = 1'b0; A = 1'b1; B = 1'b0;
        #5 S = 1'b0; A = 1'b1; B = 1'b1;
        #5 S = 1'b1; A = 1'b0; B = 1'b0;
        #5 S = 1'b1; A = 1'b0; B = 1'b1;
        #5 S = 1'b1; A = 1'b1; B = 1'b0;
        #5 S = 1'b1; A = 1'b1; B = 1'b1;
    end
    initial begin
        $monitor("Time = %0t: A = %b, B = %b, S = %b, X = %b", $time, A, B, S, X);
    end
    initial begin
        $dumpfile("MUX2_test.vcd");
        $dumpvars(0,TB);
    end
endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>vvp test
VCD info: dumpfile MUX2_test.vcd opened for output.
Time = 0: A = 0, B = 0, S = 0, X = 0
Time = 5: A = 0, B = 1, S = 0, X = 0
Time = 10: A = 1, B = 0, S = 0, X = 1
Time = 15: A = 1, B = 1, S = 0, X = 1
Time = 20: A = 0, B = 0, S = 1, X = 0
Time = 25: A = 0, B = 1, S = 1, X = 1
Time = 30: A = 1, B = 0, S = 1, X = 0
Time = 35: A = 1, B = 1, S = 1, X = 1
```

III. GTKWAVE Screenshot



Week:4 Program Number:2

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A 4:1 MULTIPLEXER USING 2:1 MULTIPLEXERS. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE

I. Verilog Code and Test Bench Code

1.mux4.v

```
module mux4(input wire [0:3] i, input wire j0, j1, output wire o);
    wire [0:1] s;
    assign s = j1 ? {j0, 1'b1} : {j0, 1'b0};

    assign o = (s == 2'b00) ? i[0] :
               (s == 2'b01) ? i[1] :
               (s == 2'b10) ? i[2] :
                              i[3];
endmodule
```

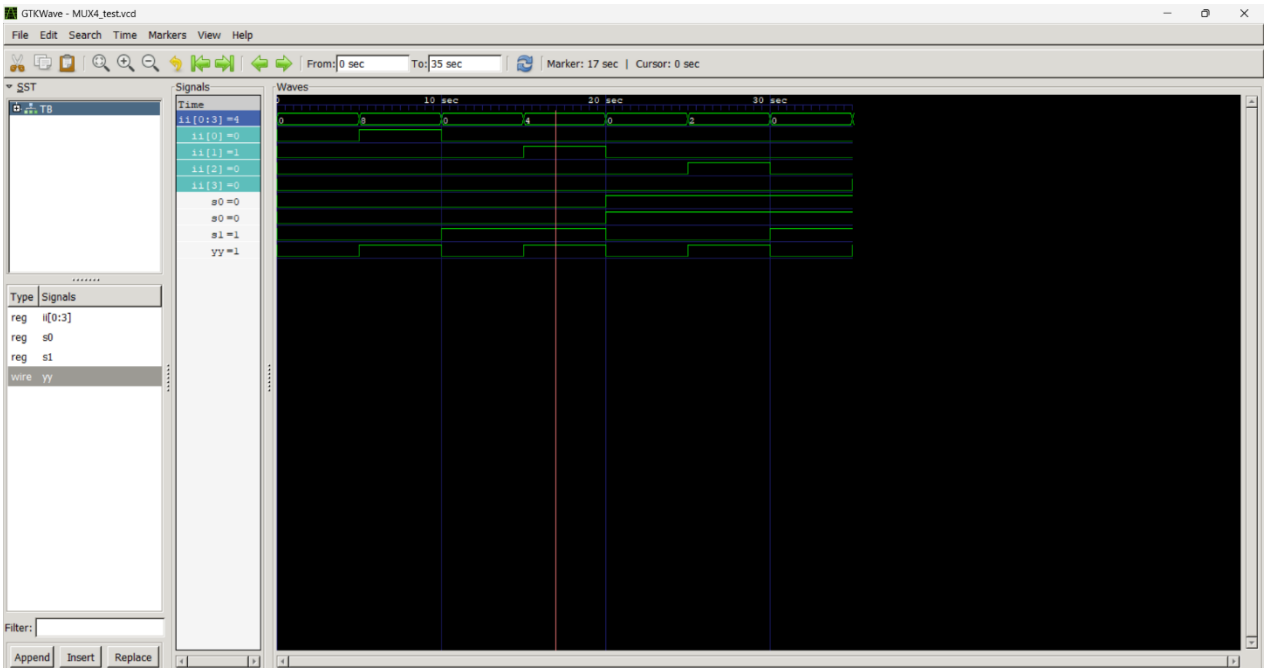
2.mux4_tb.v

```
module TB;
    reg [0:3]ii;
    reg s0;reg s1;
    wire yy;
    mux4 newMUX(.i(ii), .j0(s0),.j1(s1),.o(yy));
    initial begin
        ii = 4'b0000;s0=1'b0;s1=1'b0;
        #5      ii = 4'b1000;s0=1'b0;s1=1'b0;
        #5      ii = 4'b0000;s0=1'b0;s1=1'b1;
        #5      ii = 4'b0100;s0=1'b0;s1=1'b1;
        #5      ii = 4'b0000;s0=1'b1;s1=1'b0;
        #5      ii = 4'b0010;s0=1'b1;s1=1'b0;
        #5      ii = 4'b0000;s0=1'b1;s1=1'b1;
        #5      ii = 4'b0001;s0=1'b1;s1=1'b1;
    end
    initial begin
        $monitor("Time = %0t: ii = %b, s0 = %b, s1 = %b, yy = %b", $time, ii, s0, s1, yy);
    end
    initial begin
        $dumpfile("MUX4_test.vcd");
        $dumpvars(0, TB);
    end
endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>vvp test
VCD info: dumpfile MUX4_test.vcd opened for output.
Time = 0: ii = 0000, s0 = 0, s1 = 0, yy = 0
Time = 5: ii = 1000, s0 = 0, s1 = 0, yy = 1
Time = 10: ii = 0000, s0 = 0, s1 = 1, yy = 0
Time = 15: ii = 0100, s0 = 0, s1 = 1, yy = 1
Time = 20: ii = 0000, s0 = 1, s1 = 0, yy = 0
Time = 25: ii = 0010, s0 = 1, s1 = 0, yy = 1
Time = 30: ii = 0000, s0 = 1, s1 = 1, yy = 0
Time = 35: ii = 0001, s0 = 1, s1 = 1, yy = 1
```

III. GTKWAVE Screenshot



Week:4 Program Number:3

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A 1:2 DEMULTIPLEXER.GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE

I. Verilog Code and Test Bench Code

1.demux21.v

```
module demux2 (
    input wire in, sel,
    output wire y0, y1
);
assign y0 = (sel == 0) ? in : 0;
assign y1 = (sel == 1) ? in : 0;

endmodule
```

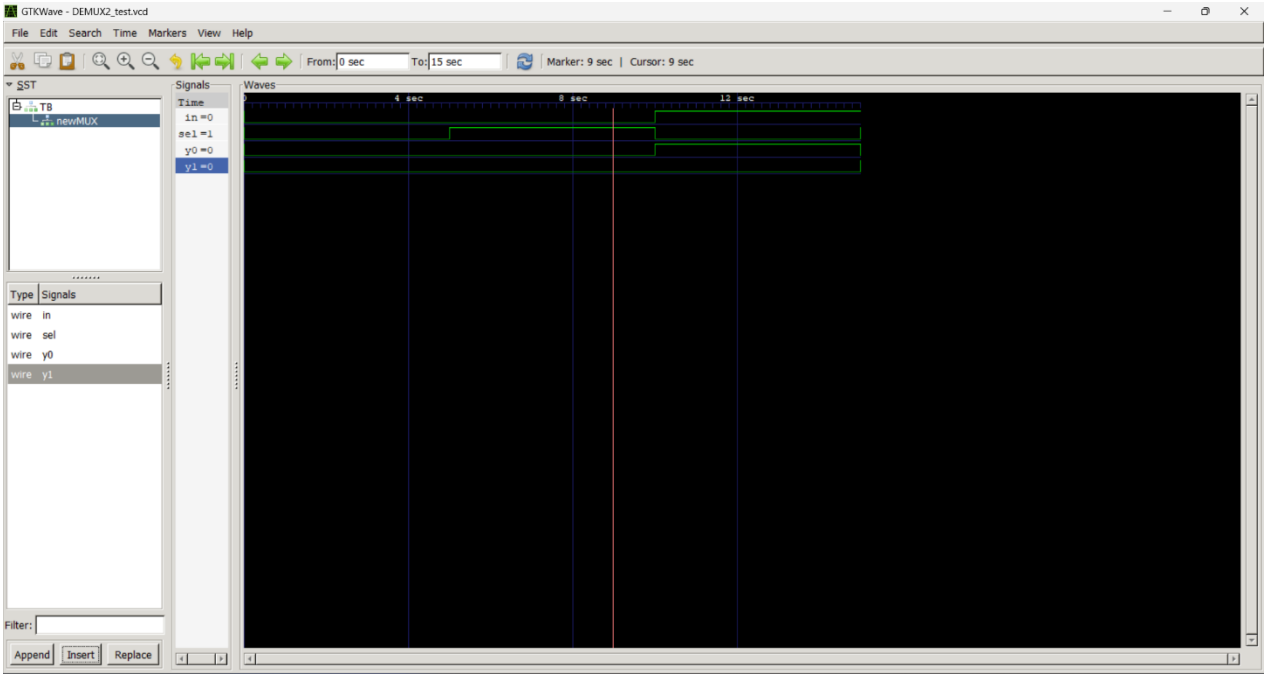
2.demux21_tb.v

```
module TB;
reg i,s;
wire y0,y1;
demux2 newMUX(.in(i), .sel(s), .y0(y0), .y1(y1));

    initial begin
        i = 1'b0; s = 1'b0;
        #5 i = 1'b0; s = 1'b1;
        #5 i = 1'b1; s = 1'b0;
        #5 i = 1'b1; s = 1'b1;
    end
    initial begin
        $monitor("Time = %0t: in = %b, sel = %b, y0 = %b, y1 = %b", $time, i, s, y0, y1);
    end
    initial begin
        $dumpfile("DEMUX2_test.vcd");
        $dumpvars(0,TB);
    end
endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>vvp test
VCD info: dumpfile DEMUX2_test.vcd opened for output.
Time = 0: in = 0, sel = 0, y0 = 0, y1 = 0
Time = 5: in = 0, sel = 1, y0 = 0, y1 = 0
Time = 10: in = 1, sel = 0, y0 = 1, y1 = 0
Time = 15: in = 1, sel = 1, y0 = 0, y1 = 1
```

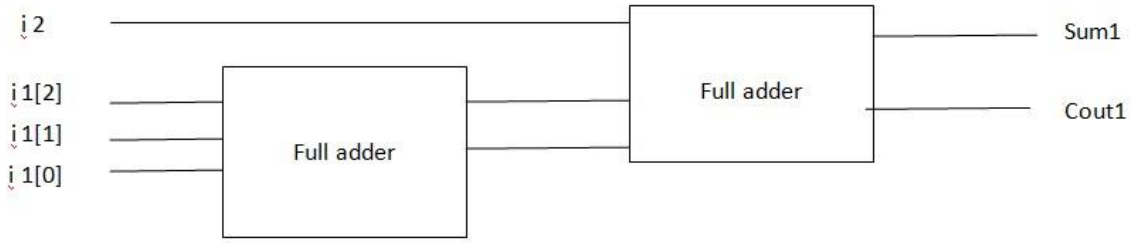
III. GTKWAVE Screenshot



Week:4 Program Number:4

TITLE:

WRITE A VERILOG PROGRAM TO MODEL THE GIVEN CIRCUIT 3.GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE



I. Verilog Code and Test Bench Code

1.circuit4.v

```
module fa(input wire i0,i1,cin,output wire sum, cout);
wire t0,t1,t2;
xor3 _i0 (i0,i1,cin,sum);
and2 _i1 (i0,i1,t0);
and2 _i2 (i1,cin,t1);
and2 _i3 (cin,i0,t2);
or3 _i4 (t0,t1,t2,cout);
endmodule

module circuit3(input wire [0:2] i1, input wire i2, output wire sum1, cout1);
wire x1,x2;
fa fa_1(i1[0],i1[1],i1[2],x1,x2);
fa fa_2(x1,x2,i2,sum1,cout1);
endmodule
```

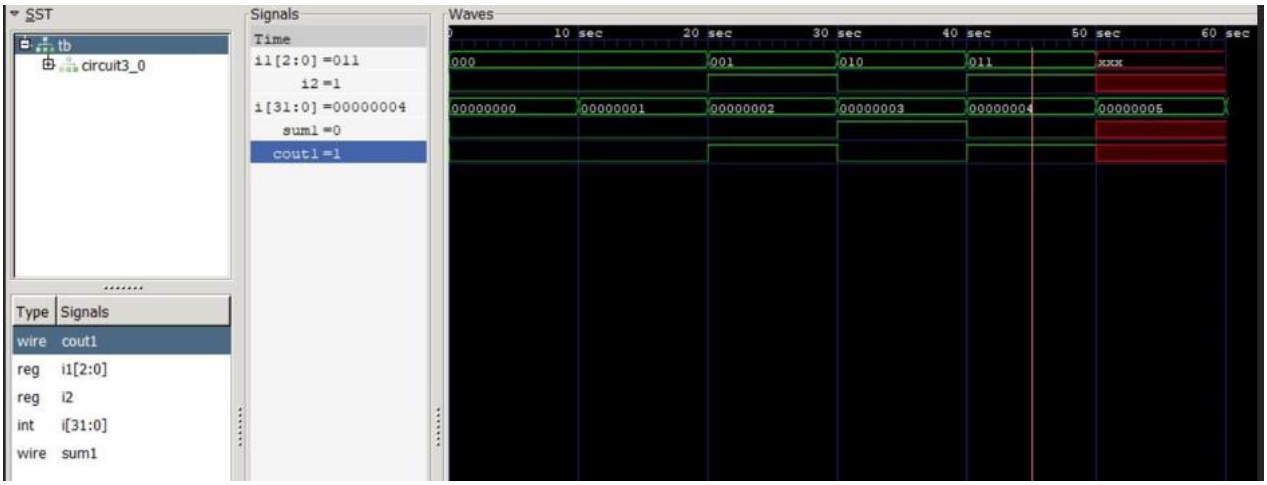
2.circuit4_tb.v

```
`define TESTVECS 6

module tb;
  reg [2:0] i1;
  reg i2;
  wire sum1,cout1;

  reg [3:0] test_vecs [0:(`TESTVECS-1)];
  integer i;
  initial begin
  $dumpfile("circuit_3.vcd");
  $dumpvars(0,tb);
  end


  initial begin
    test_vecs[0][3:1] = 3'b000;test_vecs[0][0:0] = 1'b0;
    test_vecs[1][3:1] = 3'b001;test_vecs[1][0:0] = 1'b1;
    test_vecs[2][3:1] = 3'b010;test_vecs[2][0:0] = 1'b0;
    test_vecs[3][3:1] = 3'b011;test_vecs[3][0:0] = 1'b1;
    end
initial begin
       $monitor("Time = %0t: i1 = %b, i2 = %b, sum1 = %b, cout1 = %b", $time, i1, i2, sum1, cout1);
    end
  initial {i1, i2} = 0;
  circuit3 circuit3_0 (i1,i2,sum1, cout1);
  initial begin
  for(i=0;i<`TESTVECS;i=i+1)
      begin #10 {i1,i2}=test_vecs[i];
      end

  end
endmodule
```

II. Verilog VVP Output Screen Shot

```
Time = 0: i1 = 000, i2 = 0, sum1 = 0, cout1 = 0
Time = 20: i1 = 001, i2 = 1, sum1 = 0, cout1 = 1
Time = 30: i1 = 010, i2 = 0, sum1 = 1, cout1 = 0
Time = 40: i1 = 011, i2 = 1, sum1 = 0, cout1 = 1
Time = 50: i1 = xxx, i2 = x, sum1 = x, cout1 = x
```

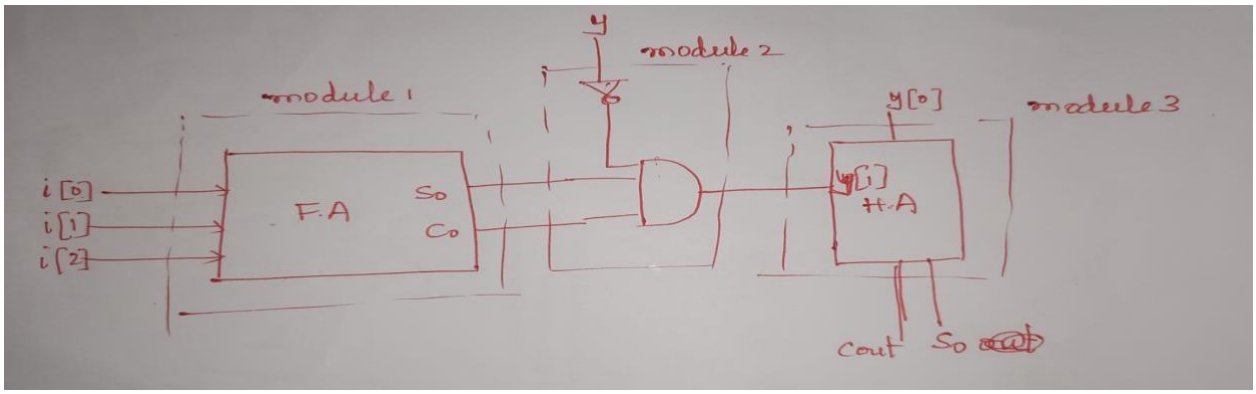
III. GTKWAVE Screenshot



Week:4 Program Number:5

TITLE:

WRITE A VERILOG PROGRAM TO MODEL THE GIVEN CIRCUIT 4.GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE



I. Verilog Code and Test Bench Code

1.circuit5.v

```
module fa (input wire i0, i1, cin, output wire sum, cout);   wire t0, t1, t2;
 xor3 _i0 (i0, i1, cin, sum);
  and2 _i1 (i0, i1, t0);
 and2 _i2 (i1, cin, t1);
and2 _i3 (cin, i0, t2);
 or3 _i4 (t0, t1, t2, cout);
endmodule


module circuit3 (input wire [0:2] i1,input wire i2,output wire sum1,cout1);
wire x1,x2;
fa fa_1(i1[0],i1[1],i1[2],x1,x2);
fa fa_2(x1,x2,i2,sum1,cout1);
endmodule
```

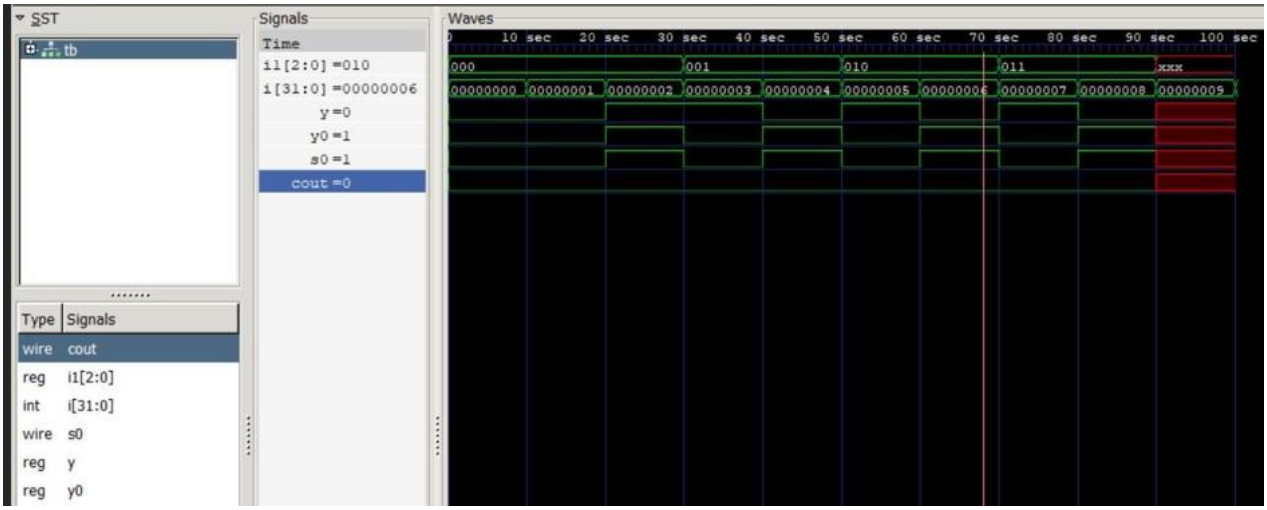
2.circuit5_tb.v

```
`define TESTVECS 10

module tb;
 reg [2:0] i1;
 reg y,y0;
 wire s0,cout;

 reg [4:0] test_vecs [0:(`TESTVECS-1)];
 integer i;
 initial begin
 $dumpfile("circuit_4.vcd");
 $dumpvars(0,tb);
 end


 initial begin
   test_vecs[0][4:2] = 3'b000;test_vecs[0][1:1] = 1'b0;test_vecs[0][0:0] = 1'b0;
   test_vecs[1][4:2] = 3'b000;test_vecs[1][1:1] = 1'b1;test_vecs[1][0:0] = 1'b1;
   test_vecs[2][4:2] = 3'b001;test_vecs[2][1:1] = 1'b1;test_vecs[2][0:0] = 1'b0;
   test_vecs[3][4:2] = 3'b001;test_vecs[3][1:1] = 1'b0;test_vecs[3][0:0] = 1'b1;
   test_vecs[4][4:2] = 3'b010;test_vecs[4][1:1] = 1'b1; test_vecs[4][0:0] = 1'b0;
   test_vecs[5][4:2] = 3'b010;test_vecs[5][1:1] = 1'b0;test_vecs[5][0:0] = 1'b1;
   test_vecs[6][4:2] = 3'b011;test_vecs[6][1:1] = 1'b1;test_vecs[6][0:0] = 1'b0;
   test_vecs[7][4:2] = 3'b011;test_vecs[7][1:1] = 1'b0; test_vecs[7][0:0] = 1'b1;
   end
initial begin
      $monitor("Time = %0t: i1 = %b, y = %b, y0 = %b, s0 = %b, cout = %b", $time, i1, y,y0,s0, cout);
   end
 initial {i1, y, y0} = 0;
 circuit4 circuit4_0 (i1,y,y0,s0, cout);
 initial begin
 for(i=0;i<`TESTVECS;i=i+1)
     begin #10 {i1,y,y0}=test_vecs[i];
     end

 end
endmodule
```

II. Verilog VVP Output Screen Shot

```
Time = 0: i1 = 000, y = 0, y0 = 0, s0 = 0, cout = 0
Time = 20: i1 = 000, y = 1, y0 = 1, s0 = 1, cout = 0
Time = 30: i1 = 001, y = 1, y0 = 0, s0 = 0, cout = 0
Time = 40: i1 = 001, y = 0, y0 = 1, s0 = 1, cout = 0
Time = 50: i1 = 010, y = 1, y0 = 0, s0 = 0, cout = 0
Time = 60: i1 = 010, y = 0, y0 = 1, s0 = 1, cout = 0
Time = 70: i1 = 011, y = 1, y0 = 0, s0 = 0, cout = 0
Time = 80: i1 = 011, y = 0, y0 = 1, s0 = 1, cout = 0
Time = 90: i1 = xxx, y = x, y0 = x, s0 = x, cout = x
```

III. GTKWAVE Screenshot



Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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