Digital Design and Computer Organisation Laboratory

UE23CS251A

3rd Semester, Academic Year 2024-2025

Date:12/08/2024

Name: Keerthan P.V.	SRN: PES2UG23CS272	Section E

Week:1 Program Number: 1

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT AND GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

I. Verilog Code Screenshot

1.and1.v

```
module and2(c,a,b);
input a,b;
output c;
assign c=a&b;
endmodule
```

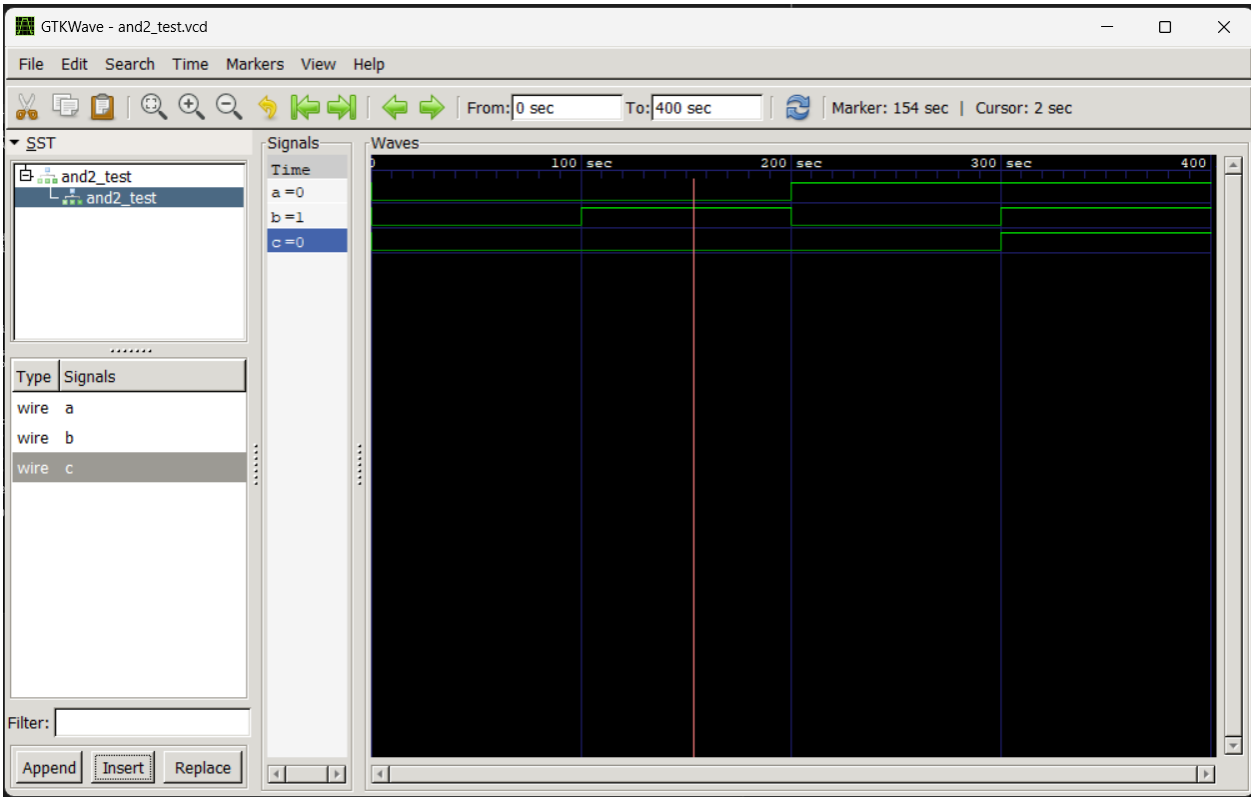
2.and2_tb.v

```
module and2_test;
reg a,b;
wire c;
and2 and2_test(c,a,b);
initial
begin
#000 a=0;b=0;
#100 a=0;b=1;
#100 a=1;b=0;
#100 a=1;b=1;
#100;
end
initial
begin
$monitor($time,"a=%b,b=%b,c=%b",a,b,c);
end
initial
begin
$dumpfile("and2_test.vcd");
$dumpvars(0,and2_test);
end
endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>vvp test
VCD info: dumpfile and2_test.vcd opened for output.
                   0a=0,b=0,c=0
                 100a=0,b=1,c=0
                 200a=1,b=0,c=0
                 300a=1,b=1,c=1
```

III. GTKWAVE Screenshot



Week:1 Program Number: 2

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT OR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE OR GATE TRUTH TABLE

I. Verilog Code Screenshot

1.or2.v

```
module or2(c,a,b);
input a,b;
output c;
assign c=a|b;
endmodule
```

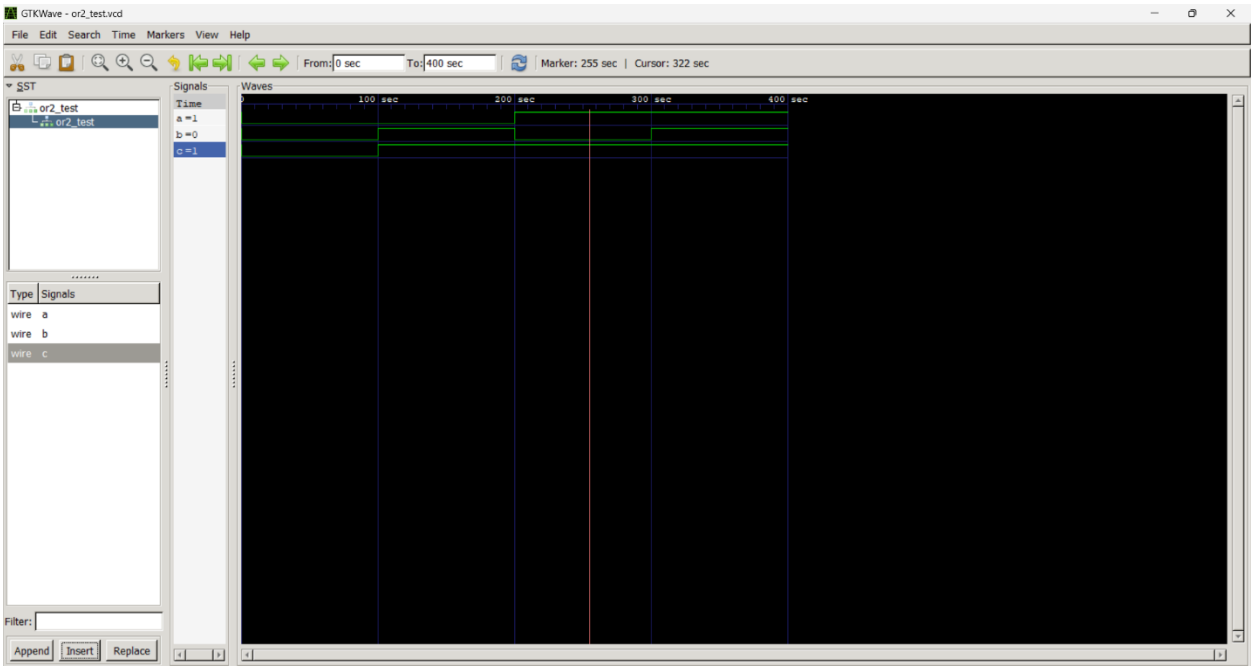
2.or2_tb.v

```
module or2_test;
reg a,b;
wire c;
or2 or2_test(c,a,b);
initial
begin
#000 a=0;b=0;
#100 a=0;b=1;
#100 a=1;b=0;
#100 a=1;b=1;
#100;
end
initial
begin
$monitor($time,"a=%b,b=%b,c=%b",a,b,c);
end
initial
begin
$dumpfile("or2_test.vcd");
$dumpvars(0,or2_test);
end
endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>vvp test
VCD info: dumpfile or2_test.vcd opened for output.
                    0a=0,b=0,c=0
                  100a=0,b=1,c=1
                  200a=1,b=0,c=1
                  300a=1,b=1,c=1
```

III. GTKWAVE Screenshot



Week:1 Program Number: 3

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A NOT GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NOT GATE TRUTH TABLE

I. Verilog Code Screenshot

1.not1.v

```
module not1(a,b);
input a;
output b;
assign b=!a;
endmodule
```

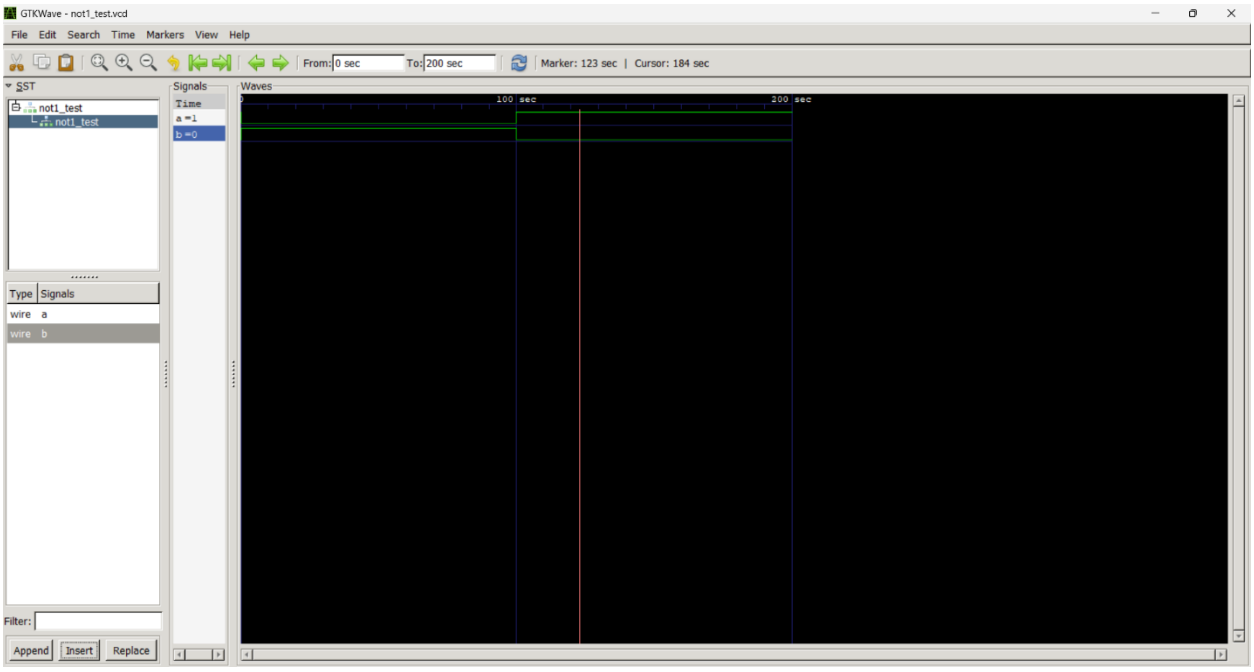
2.not1_tb.v

```
module not1_test;
reg a;
wire b;
not1 not1_test(a,b);
initial
begin
#000 a=0;
#100 a=1;
#100;
end
initial
begin
$monitor($time,"a=%b, b=%b",a,b,);
end
initial
begin
$dumpfile("not1_test.vcd");
$dumpvars(0,not1_test);
end
endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>vvp test
VCD info: dumpfile not1_test.vcd opened for output.
                   0a=0, b=1
                 100a=1, b=0
```

III. GTKWAVE Screenshot



Week:1 Program Number: 4

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT NAND GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NAND GATE TRUTH TABLE

I. Verilog Code Screenshot

1.nand2.v

```
module nand2(c,a,b);
input a,b;
output c;
assign c=!(a&b);
endmodule
```

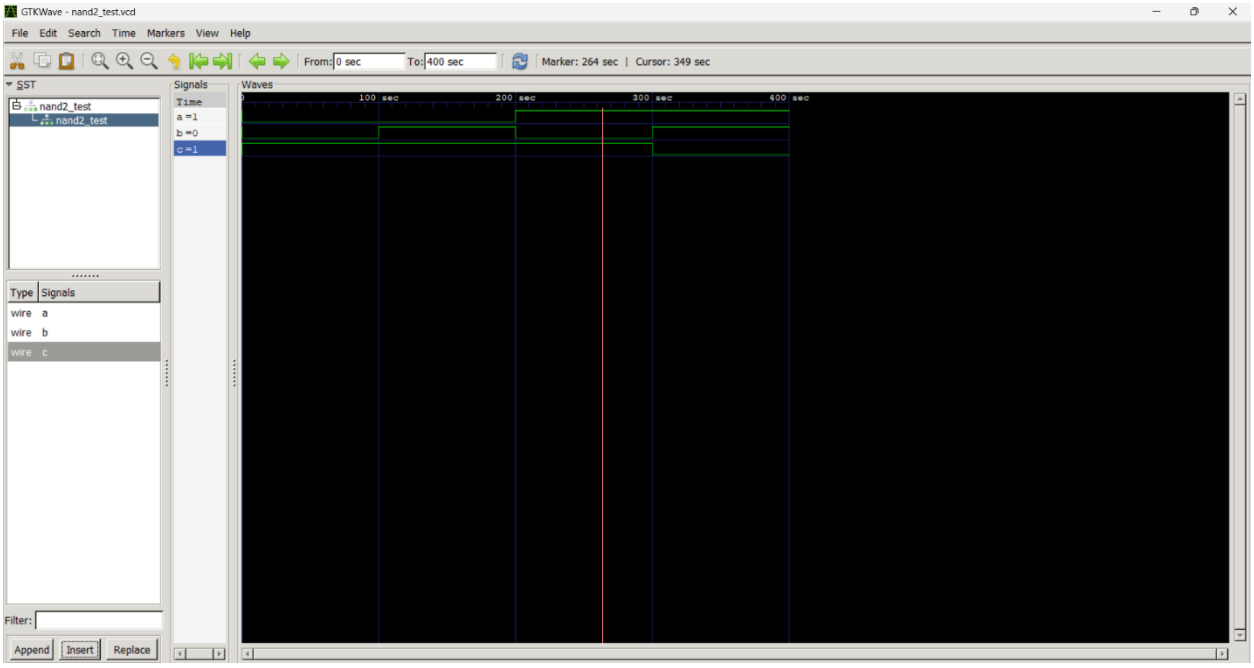
2.nand2_tb.v

```
module nand2_test;
reg a,b;
wire c;
nand2 nand2_test(c,a,b);
initial
begin
#000 a=0;b=0;
#100 a=0;b=1;
#100 a=1;b=0;
#100 a=1;b=1;
#100;
end
initial
begin
$monitor($time,"a=%b,b=%b,c=%b",a,b,c);
end
initial
begin
$dumpfile("nand2_test.vcd");
$dumpvars(0,nand2_test);
end
endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>vvp test
VCD info: dumpfile nand2_test.vcd opened for output.
                    0a=0,b=0,c=1
                  100a=0,b=1,c=1
                  200a=1,b=0,c=1
                  300a=1,b=1,c=0
```

III. GTKWAVE Screenshot



Week:1 Program Number: 5

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT NOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NOR GATE TRUTH TABLE

I. Verilog Code Screenshot

1.nor2.v

```
module nor2(c,a,b);
input a,b;
output c;
assign c=!(a | b);
endmodule
```

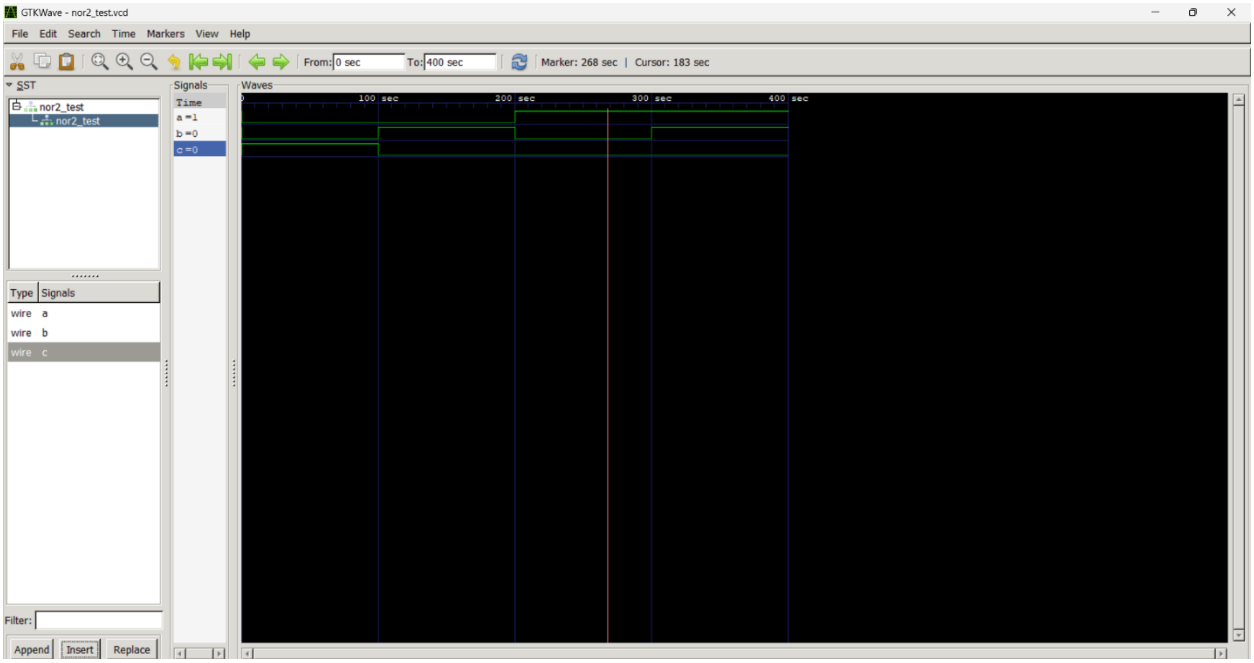
2.nor2_tb.v

```
module nor2_test;
reg a,b;
wire c;
nor2 nor2_test(c,a,b);
initial
begin
#000 a=0;b=0;
#100 a=0;b=1;
#100 a=1;b=0;
#100 a=1;b=1;
#100;
end
initial
begin
$monitor($time,"a=%b,b=%b,c=%b",a,b,c);
end
initial
begin
$dumpfile("nor2_test.vcd");
$dumpvars(0,nor2_test);
end
endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>vvp test
VCD info: dumpfile nor2_test.vcd opened for output.
                   0a=0,b=0,c=1
                 100a=0,b=1,c=0
                 200a=1,b=0,c=0
                 300a=1,b=1,c=0
```

III. GTKWAVE Screenshot



Week:1 Program Number: 6

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT XOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

I. Verilog Code Screenshot

1.xor2.v

```
module xor2(c,a,b);
input a,b;
output c;
assign c=a^b;
endmodule
```

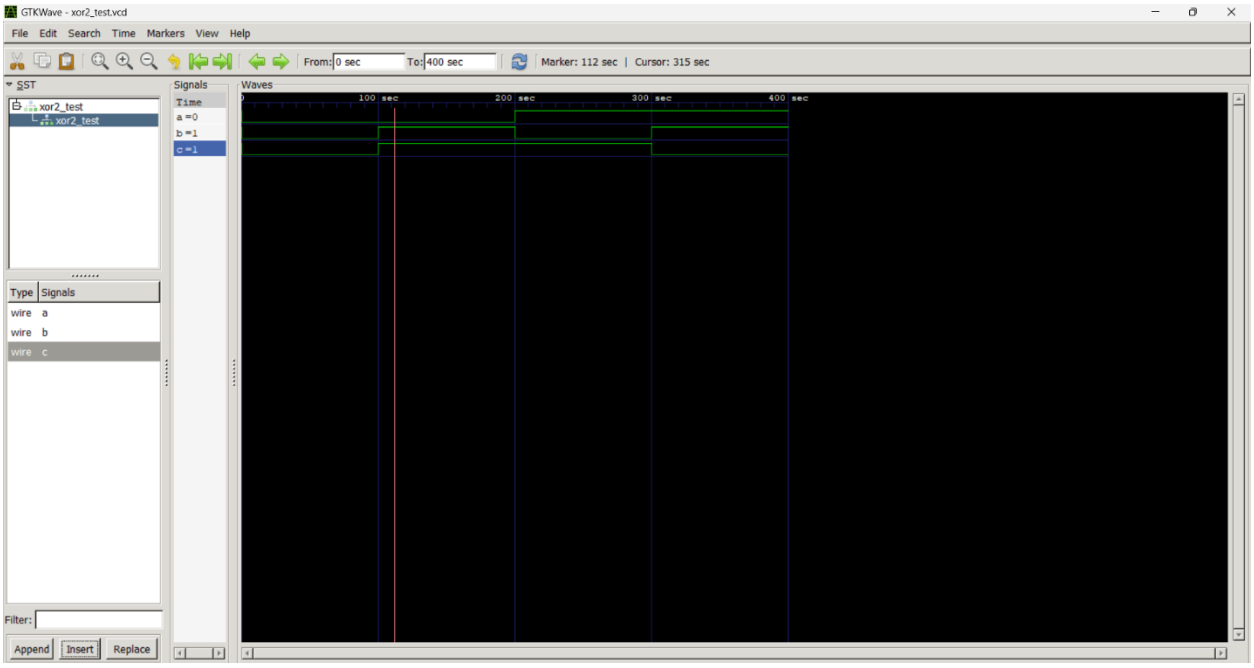
2.xor2_tb.v

```
module xor2_test;
reg a,b;
wire c;
xor2 xor2_test(c,a,b);
initial
begin
#000 a=0;b=0;
#100 a=0;b=1;
#100 a=1;b=0;
#100 a=1;b=1;
#100;
end
initial
begin
$monitor($time,"a=%b,b=%b,c=%b",a,b,c);
end
initial
begin
$dumpfile("xor2_test.vcd");
$dumpvars(0,xor2_test);
end
endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>vvp test
VCD info: dumpfile xor2_test.vcd opened for output.
                   0a=0,b=0,c=0
                 100a=0,b=1,c=1
                 200a=1,b=0,c=1
                 300a=1,b=1,c=0
```

III. GTKWAVE Screenshot



Week:1 Program Number: 7

TITLE :

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT XNOR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

I. Verilog Code Screenshot

1.xnor2.v

```
module xnor2(c,a,b);
input a,b;
output c;
assign c=!(a ^ b);
endmodule
```

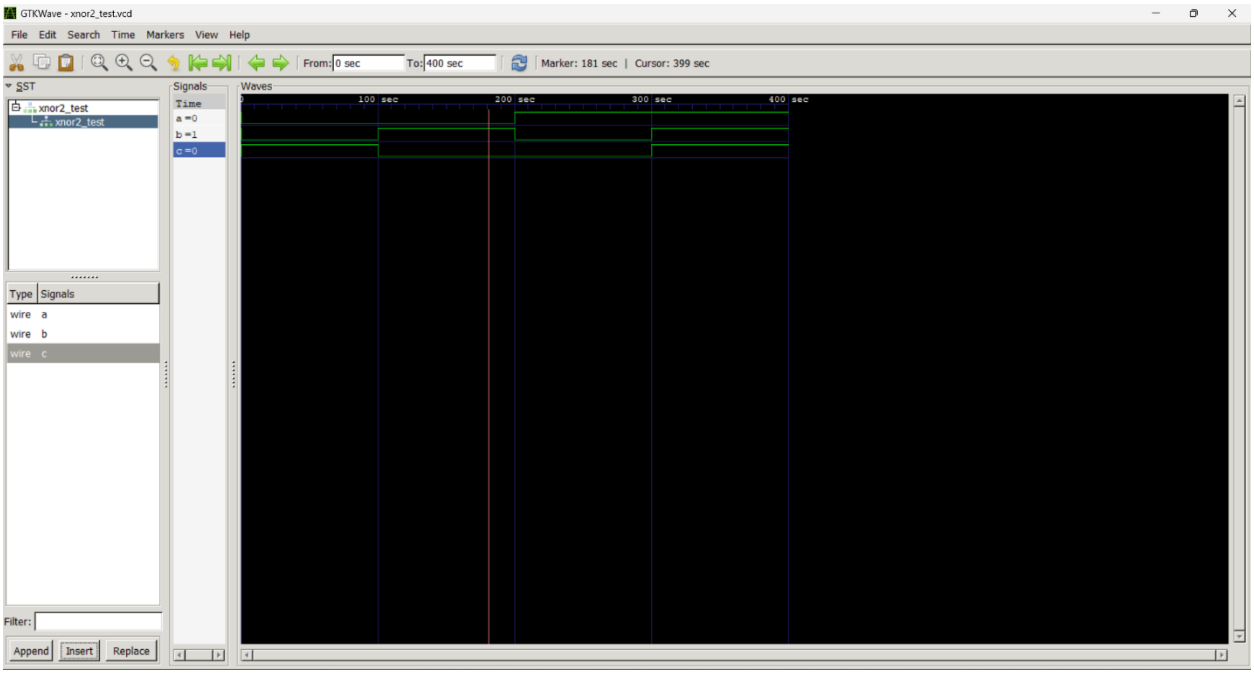
2.xnor2_tb.v

```
module xnor2_test;
reg a,b;
wire c;
xnor2 xnor2_test(c,a,b);
initial
begin
#000 a=0;b=0;
#100 a=0;b=1;
#100 a=1;b=0;
#100 a=1;b=1;
#100;
end
initial
begin
$monitor($time,"a=%b,b=%b,c=%b",a,b,c);
end
initial
begin
$dumpfile("xnor2_test.vcd");
$dumpvars(0,xnor2_test);
end
endmodule
```

II. Verilog VVP Output Screen Shot

```
C:\iverilog\bin>vvp test
VCD info: dumpfile xnor2_test.vcd opened for output.
                   0a=0,b=0,c=1
                 100a=0,b=1,c=0
                 200a=1,b=0,c=0
                 300a=1,b=1,c=1
```

III. GTKWAVE Screenshot



Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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