Digital Design and Computer Organization Laboratory

3rd Semester, Academic Year 2024-25

Date:19/08/2024

Name: Keerthan P.V.	SRN: PES2UG23CS272	Section 3E

Week:2 Program Number :1

Title of the Program

SIMPLE_CIRCUIT

Aim:

WRITE A VERILOG PROGRAM TO MODEL THE GIVEN SIMPLE CIRCUIT.GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE

1. Paste the Screen Shot of the source code

1.simplecircuit.v

```
module simple_circuit (A, B, C, D, E);
output D,E;
input A, B, C;
wire w1;
and G1 (w1,A,B);
not G2(E,C);
or G3(D,w1,E);
endmodule
```

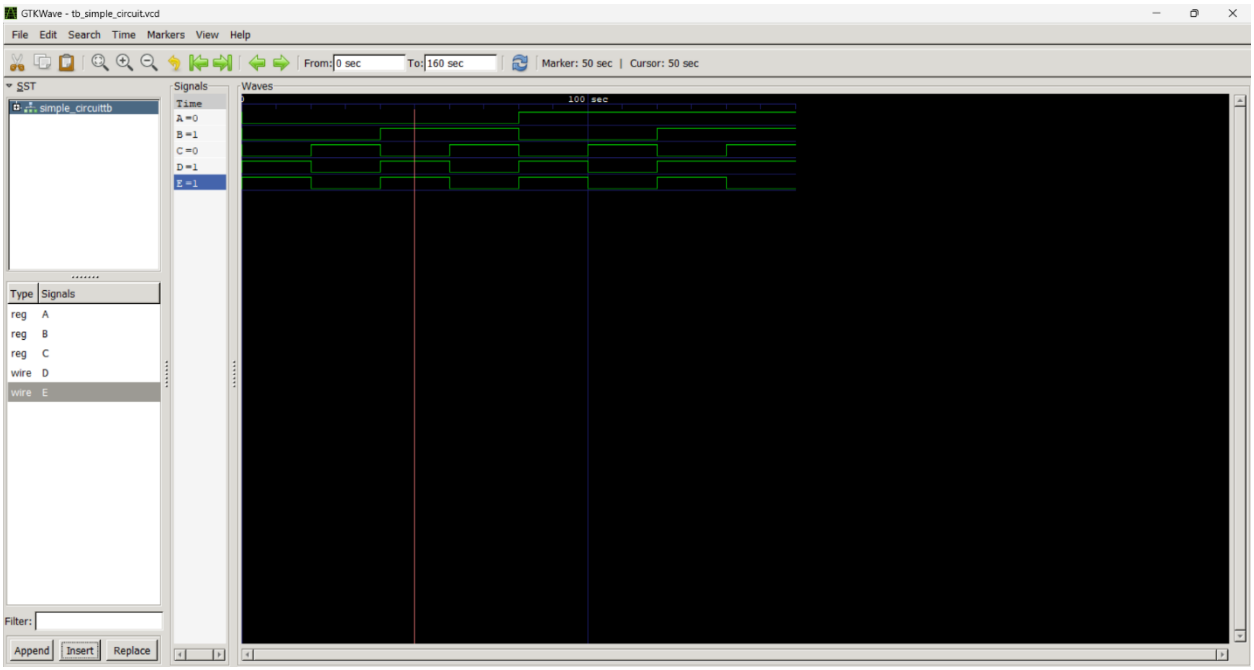
2.tb_simple_circuit.v

```
module simple_circuittb;
    wire D, E;
    reg A, B, C;

    // Instantiate the simple_circuit module
    simple_circuit M1 (A, B, C, D, E);

    initial
    begin
        // Initialize the dump file for waveform generation
        $dumpfile("tb_simple_circuit.vcd");
        $dumpvars(0, simple_circuittb);

        // Apply stimulus to the inputs
        A = 1'b0; B = 1'b0; C = 1'b0;
        #20;
        A = 1'b0; B = 1'b0; C = 1'b1;
        #20;
        A = 1'b0; B = 1'b1; C = 1'b0;
        #20;
        A = 1'b0; B = 1'b1; C = 1'b1;
        #20;
        A = 1'b1; B = 1'b0; C = 1'b0;
        #20;
        A = 1'b1; B = 1'b0; C = 1'b1;
        #20;
        A = 1'b1; B = 1'b1; C = 1'b0;
        #20;
        A = 1'b1; B = 1'b1; C = 1'b1;
        #20;
    end

    initial
    begin
        // Monitor the changes in signals
        $monitor($time, " A=%b B=%b C=%b D=%b E=%b", A, B, C, D, E);
    end
endmodule
```

2. Paste the Screen Shot of the VVP command output

```
C:\iverilog\bin>vvp test
VCD info: dumpfile tb_simple_circuit.vcd opened for output.
                   0 A=0 B=0 C=0 D=1 E=1
                  20 A=0 B=0 C=1 D=0 E=0
                  40 A=0 B=1 C=0 D=1 E=1
                  60 A=0 B=1 C=1 D=0 E=0
                  80 A=1 B=0 C=0 D=1 E=1
                 100 A=1 B=0 C=1 D=0 E=0
                 120 A=1 B=1 C=0 D=1 E=1
                 140 A=1 B=1 C=1 D=1 E=0
```

3. Paste the Screen shot of the GTKWave form



4. Include relevant Truth Table

Time (in ms)	Inputs			Outputs	
	A	B	C	D	E
0	0	0	0	1	1
20	0	0	1	0	0
40	0	1	0	1	1
60	0	1	1	0	0
80	1	0	0	1	1
100	1	0	1	0	0
120	1	1	0	1	1
140	1	1	1	1	0

Week:2 Program Number: 2

Title of the Program

CIRCUIT1

Aim:

WRITE A VERILOG PROGRAM TO MODEL THE GIVEN CIRCUIT1. GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE

1. Paste the Screen Shot of the source code

1.circuit1.v

```
module circuit1 (A, B, C, Y);
    input A, B, C;  // Declare inputs
    output Y;       // Declare output
    wire w1;        // Intermediate wire to hold the output of the AND gate

    // AND gate: ANDs inputs B and C
    assign w1 = B & C;

    // OR gate: ORs input A with the output of the AND gate
    assign Y = A | w1;

endmodule
```

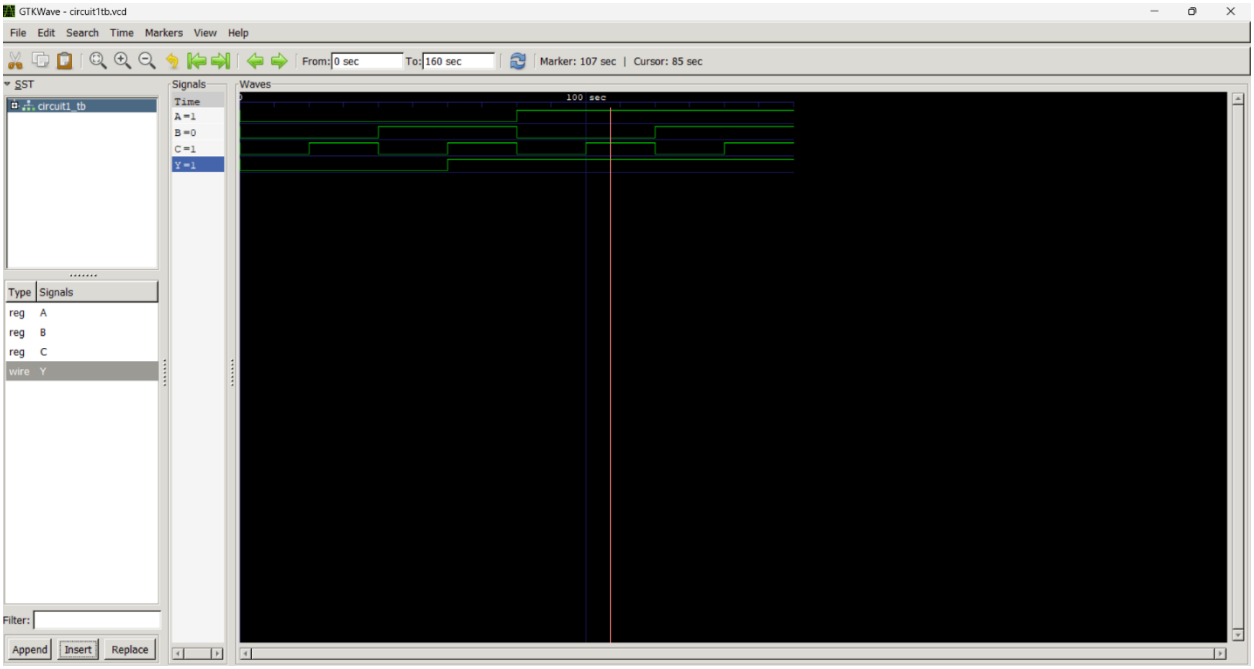
2.circuit1tb.v

```
module circuit1_tb;
    wire D, E;
    reg A, B, C;

    // Instantiate the simple_circuit module
    circuit1 M1 (A, B, C, Y);

    initial
    begin
        // Initialize the dump file for waveform generation
        $dumpfile("circuit1tb.vcd");
        $dumpvars(0, circuit1_tb);

        // Apply stimulus to the inputs
        A = 1'b0; B = 1'b0; C = 1'b0;
        #20;
        A = 1'b0; B = 1'b0; C = 1'b1;
        #20;
        A = 1'b0; B = 1'b1; C = 1'b0;
        #20;
        A = 1'b0; B = 1'b1; C = 1'b1;
        #20;
        A = 1'b1; B = 1'b0; C = 1'b0;
        #20;
        A = 1'b1; B = 1'b0; C = 1'b1;
        #20;
        A = 1'b1; B = 1'b1; C = 1'b0;
        #20;
        A = 1'b1; B = 1'b1; C = 1'b1;
        #20;
    end

    initial
    begin
        // Monitor the changes in signals
        $monitor($time, " A=%b B=%b C=%b Y=%b ", A, B, C, Y);
    end
endmodule
```

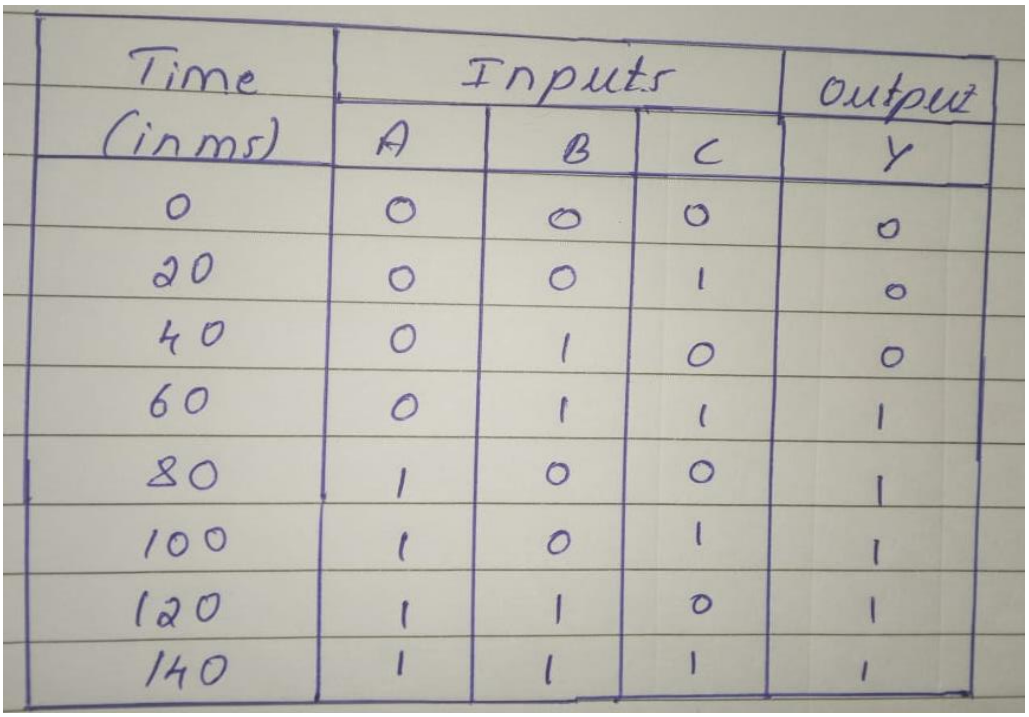
2. Paste the Screen Shot of the VVP command output

```
C:\iverilog\bin>vvp test
VCD info: dumpfile circuit1tb.vcd opened for output.
                   0 A=0 B=0 C=0 Y=0
                  20 A=0 B=0 C=1 Y=0
                  40 A=0 B=1 C=0 Y=0
                  60 A=0 B=1 C=1 Y=1
                  80 A=1 B=0 C=0 Y=1
                 100 A=1 B=0 C=1 Y=1
                 120 A=1 B=1 C=0 Y=1
                 140 A=1 B=1 C=1 Y=1
```

3. Paste the Screen shot of the GTKWave form



4. Include relevant Truth Table



Time (in ms)	Inputs			Output
	A	B	C	Y
0	0	0	0	0
20	0	0	1	0
40	0	1	0	0
60	0	1	1	1
80	1	0	0	1
100	1	0	1	1
120	1	1	0	1
140	1	1	1	1

Week:2 Program Number:3

Title of the Program

CIRCUIT2

Aim:

WRITE A VERILOG PROGRAM TO MODEL THE GIVEN CIRCUIT2. GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE

1. Paste the Screen Shot of the source code

1.circuit2.v

```
// Define the circuit2 module (DUT)
module circuit2 (
    input A2, B2, C2,
    output Z
);
    wire w1, w2, w3;

    // First AND gate: w1 = C2 AND B2
    assign w1 = C2 & B2;

    // First OR gate: w2 = A2 OR w1
    assign w2 = A2 | w1;

    // Second AND gate: w3 = B2 AND A2
    assign w3 = B2 & A2;

    // Second OR gate: Z = w2 OR w3
    assign Z = w2 | w3;

endmodule
```

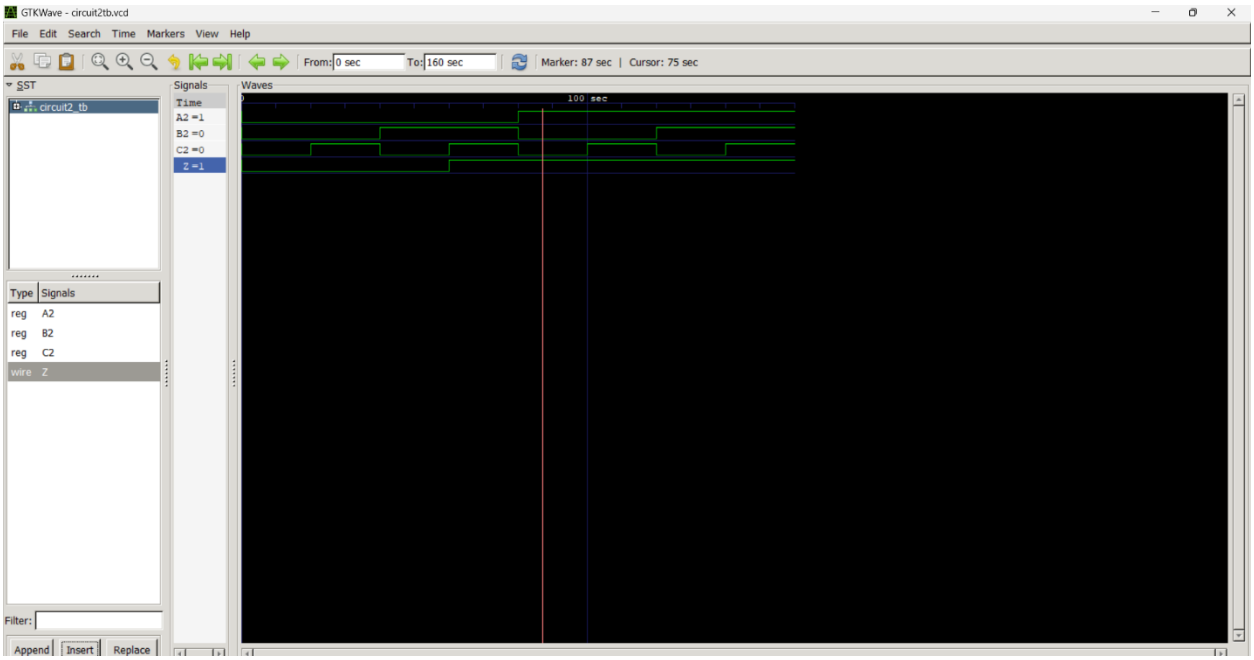
2.circuit2tb.v

```
module circuit2_tb;
    reg A2, B2, C2;
    wire Z;

    // Instantiate the circuit2 module (DUT)
    circuit2 uut (
        .A2(A2),
        .B2(B2),
        .C2(C2),
        .Z(Z)
    );

    initial
    begin
        // Initialize the dump file for waveform generation
        $dumpfile("circuit2tb.vcd");
        $dumpvars(0, circuit2_tb);

        // Apply stimulus to the inputs
        A2 = 1'b0; B2 = 1'b0; C2 = 1'b0;
        #20;
        A2 = 1'b0; B2 = 1'b0; C2 = 1'b1;
        #20;
        A2 = 1'b0; B2 = 1'b1; C2 = 1'b0;
        #20;
        A2 = 1'b0; B2 = 1'b1; C2 = 1'b1;
        #20;
        A2 = 1'b1; B2 = 1'b0; C2 = 1'b0;
        #20;
        A2 = 1'b1; B2 = 1'b0; C2 = 1'b1;
        #20;
        A2 = 1'b1; B2 = 1'b1; C2 = 1'b0;
        #20;
        A2 = 1'b1; B2 = 1'b1; C2 = 1'b1;
        #20;
    end

    initial
    begin
        // Monitor the changes in signals
        $monitor($time, " A2=%b B2=%b C2=%b Z=%b", A2, B2, C2, Z);
    end
endmodule
```

2. Paste the Screen Shot of the VVP command output

```
C:\iverilog\bin>vvp test
VCD info: dumpfile circuit2tb.vcd opened for output.
                   0 A2=0 B2=0 C2=0 Z=0
                  20 A2=0 B2=0 C2=1 Z=0
                  40 A2=0 B2=1 C2=0 Z=0
                  60 A2=0 B2=1 C2=1 Z=1
                  80 A2=1 B2=0 C2=0 Z=1
                 100 A2=1 B2=0 C2=1 Z=1
                 120 A2=1 B2=1 C2=0 Z=1
                 140 A2=1 B2=1 C2=1 Z=1
```

3. Paste the Screen shot of the GTKWave form



4. Include relevant Truth Table

Time (in ms)	Inputs			Output
	A2	B2	C2	Z
0	0	0	0	0
20	0	0	1	0
40	0	1	0	0
60	0	1	1	1
80	1	0	0	1
100	1	0	1	1
120	1	1	0	1
140	1	1	1	1

Disclaimer:

- The programs and output submitted is duly written, verified and executed my me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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