

Microprocessor and Computer Architecture Laboratory

UE23CS251B

4th Semester, Academic Year 2024-25

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Week# 8 Exercise: 1

1. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

Consider a direct mapped cache of size 16 bytes with block size 4 bytes. The size of main memory is 256 bytes. Find Number of bits in tag, index and offset.

The processor generates requests as follows

1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11.

Find hit rate and miss rate.

Include One Screenshot(for Write Back Cache) with

- i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor
- ii) Screenshot showing the Cache Table
- iii) Screenshot showing hit and miss rates

Write Policies

☒ Write Back
 ☐ Write Through
 ☒ Write On Allocate
 ☐ Write Around

Cache Size (power of 2): 16
 Memory Size (power of 2): 256
 Offset Bits: 2

Instruction:

Information
 The cycle has been completed.
 Please submit another instructions

Statistics
 Hit Rate: 33%
 Miss Rate: 67%

List of Previous Instructions:

- Load 0 (Miss)
- Load 4 (Miss)
- Load 8 (Miss)
- Load 12 (Miss)
- Load 16 (Miss)
- Load 20 (Miss)
- Load 24 (Miss)
- Load 28 (Miss)
- Load 32 (Miss)
- Load 36 (Miss)
- Load 40 (Miss)
- Load 44 (Miss)
- Load 48 (Miss)
- Load 52 (Miss)
- Load 56 (Miss)
- Load 60 (Miss)
- Load 64 (Miss)

Instruction Breakdown

0001	00	01
4 bit	2 bit	2 bit

Memory Block

B 4 W 0	B 4 W 1	B 4 W 2	B 4 W 3
B 5 W 0	B 5 W 1	B 5 W 2	B 5 W 3
B 6 W 0	B 6 W 1	B 6 W 2	B 6 W 3
B 7 W 0	B 7 W 1	B 7 W 2	B 7 W 3
B 8 W 0	B 8 W 1	B 8 W 2	B 8 W 3
B 9 W 0	B 9 W 1	B 9 W 2	B 9 W 3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0001	BLOCK 4 WORD 0-3	0
1	1	0000	BLOCK 1 WORD 0-3	0
2	1	0000	BLOCK 2 WORD 0-3	0
3	0	-	0	0

2. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

Include One Screenshot(for Write Back Cache) with

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

ii) Screenshot showing the Cache Table

iii) Screenshot showing hit and miss rates

(c)When a program is executed, the processor reads data sequentially from the following word addresses: .(One Screenshot)

128, 144, 2176, 2180, 128, 2176

All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

ParaCache

Write Policies: ☒ Write Back, ☐ Write Through, ☒ Write On Allocate, ☐ Write Around

Cache Size (power of 2): 2048
Memory Size (power of 2): 65536
Offset Bits: 6

Reset Submit

Instruction: Load [0x128] [hex]
List of next 10 instructions: [Submit]

Information: The cycle has been completed. Please submit another instructions.

Next Fast Forward

Statistics:
Hit Rate: 50%
Miss Rate: 50%
List of Previous Instructions:
• Load 128 [Hex]
• Load 144 [Hex]
• Load 2176 [Hex]
• Load 2180 [Hex]
• Load 128 [Hex]
• Load 2176 [Hex]

DIRECT MAPPED CACHE

Instruction Breakdown:
00100 5 DE
00101 5 DE
110110 6 DE

Memory Block:
0 00100 0 00100 1 0 00100 2 0 00100 3 0 00100 4 0 00100 5 0 00100 6 0 00100 7 0 00100 8 0 00100 9 0 00100 A 0 00100 B 0 00100 C 0 00100 D 0 00100 E 0 00100 F 0 00100 10 0 00100 11 0 00100 12 0 00100 13 0 00100 14 0 00100 15 0 00100 16 0 00100 17 0 00100 18 0 00100 19 0 00100 20 0 00100 21 0 00100 22 0 00100 23 0 00100 24 0 00100 25 0 00100 26 0 00100 27 0 00100 28 0 00100 29 0 00100 30 0 00100 31 0

Cache Table:

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	1	00000	BLOCK 4 WORD 0 - 63	0
5	1	00100	BLOCK 85 WORD 0 - 63	0
6	1	00100	BLOCK 86 WORD 0 - 63	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

Week# ____8____ Exercise: ____4__

4. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

- a. Direct Mapped Cache Size: 32 words
- b. Memory Size: 131072 words[main memory].
- c. Block Size: 4 words.

Use Write back policy

Also, repeat the exercise for Write through policy.

Include One Screenshot(for Write Back Cache) with

- i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor**
- ii) Screenshot showing the Cache Table**
- iii) Screenshot showing hit and miss rates**

Include One Screenshot(for Write Through Cache) with

- i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor**

a. Write back cache

Week# ____8____ Exercise: ____5__

5. Try using PARACACHE SIMULATOR for the exercise for the following configuration .

Cache Size(Direct Mapped): 32 words

Memory Size: 16-bit memory address

Block Size: 16 words.

Use Write back policy

Also, repeat the exercise for Write through policy.

Include One Screenshot for each case with

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

ii) Screenshot showing the Cache Table

iii) Screenshot showing hit and miss rates

a. Write Back cache

ParaCache

Direct Mapped CacheFully Associative Cache2-Way SA4-Way SACache Type AnalysisVirtual MemoryKnowledge Base

Write Policies

☒ Write Back

☐ Write Through

☒ Write On Allocate

☐ Write Around

Cache Size (power of 2)

32

Memory Size (power of 2)

65536

Offset Bits

4

Reset

Submit

Instruction

Load

pc=hex#

List of next 10 instructions

Submit

Information

The cycle has been completed.
Please submit another instructions

Next

Fast Forward

Statistics

Hit Rate : 0%

Miss Rate : 100%

List of Previous Instructions

Load R218 (Miss)

Load R80 (Miss)

Load R407 (Miss)

Load C872 (Miss)

Load C200 (Miss)

Load R44A (Miss)

Load P40F (Miss)

Load R4A2 (Miss)

Load R0B1 (Miss)

Load R0Y1 (Miss)

DIRECT MAPPED CACHE

Instruction Breakdown

Memory Block

Cache Table

010110100000

0

0001

11 bit

1 bit

4 bit

0

1

01011010000

BLOCK 508 WORD 0 - 15

0

1

1

0100000101

BLOCK 408 WORD 0 - 15

0

0

1

01011010000

BLOCK 508 WORD 0 - 15

0

1

1

0100000101

BLOCK 408 WORD 0 - 15

0

0

1

01011010000

BLOCK 508 WORD 0 - 15

0

1

1

0100000101

BLOCK 408 WORD 0 - 15

0

115

1

01011010000

BLOCK 508 WORD 0 - 15

0

1

1

0100000101

BLOCK 408 WORD 0 - 15

0

0

1

01011010000

BLOCK 508 WORD 0 - 15

0

1

1

0100000101

BLOCK 408 WORD 0 - 15

0

b. write Through cache

ParaCache

Direct Mapped CacheFully Associative Cache2-Way SA4-Way SACache Type AnalysisVirtual MemoryKnowledge Base

Write Policies

☐ Write Back

☒ Write Through

☒ Write On Allocate

☐ Write Around

Cache Size (power of 2)

32

Memory Size (power of 2)

65536

Offset Bits

4

Reset

Submit

Instruction

Load

pc=hex#

List of next 10 instructions

Submit

Information

The cycle has been completed.
Please submit another instructions

Next

Fast Forward

Statistics

Hit Rate : 0%

Miss Rate : 100%

List of Previous Instructions

Load R218 (Miss)

Load C43 (Miss)

Load R219 (Miss)

Load R80 (Miss)

Load R27A (Miss)

Load C202 (Miss)

Load R20B (Miss)

Load C22A (Miss)

Load R40F (Miss)

DIRECT MAPPED CACHE

Instruction Breakdown

Memory Block

Cache Table

00100100001

0

1111

11 bit

1 bit

4 bit

0

1

00100100001

BLOCK 242 WORD 0 - 15

0

1

1

0010011011

BLOCK 237 WORD 0 - 15

0

0

1

00100100001

BLOCK 242 WORD 0 - 15

0

1

1

0010011011

BLOCK 237 WORD 0 - 15

0

0

1

00100100001

BLOCK 242 WORD 0 - 15

0

1

1

0010011011

BLOCK 237 WORD 0 - 15

0

Week# 8

Exercise: 6

6. Try using PARACACHE SIMULATOR for the exercise for the following configuration .

Consider a fully associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find number of tag bits.

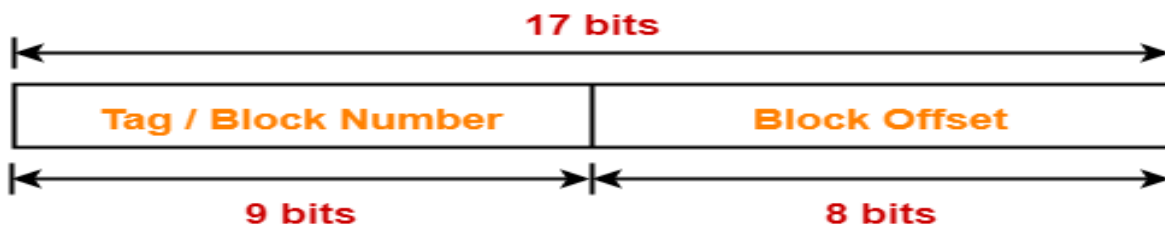
a)Use LRU replacement policy calculate the hit ratio and miss ratio for the following sequence:

0,1,2,3,4,5,6,7,0,1,2,8,10,15,15,12

b)Use FIFO replacement policy calculate the hit ratio and miss ratio for the following sequence:

0,1,2,3,4,5,6,7,0,1,2,8,10,15,15,12

Solution



a.LRU Replacement Policy:

Week# 8 Exercise: 7

7. Try using PARACACHE SIMULATOR for the exercise for the following configuration .

Consider the following cache design: main memory having 32 bytes, cache memory of 8 bytes, block size is 1 byte. Use LRU replacement policy

Using fully associative cache calculate the hit ratio and miss ratio for the following sequence:

0,1,2,3,4,5,6,7,0,1,2,8,10,15,15,12

ParaCache

Replacement Policies: ☐ FIFO ☒ LRU ☐ Random

Write Policies: ☒ Write Back ☐ Write Through ☐ Write Around

Cache Size (word x bit): 8 x 32

Memory Size (word x bit): 32 x 32

Offset Bits: 0

Instruction Breakdown: 0, 1, 2, 3, 4, 5, 6, 7, 0, 1, 2, 8, 10, 15, 15, 12

Cache Table:

Index	Value	Tag	Data Field	Dirty Bit
0	1	00000	BLOCK WORD 0-0	0
1	1	00001	BLOCK WORD 0-1	0
2	1	00010	BLOCK WORD 0-2	0
3	1	01000	BLOCK WORD 0-3	0
4	1	10000	BLOCK WORD 0-4	0
5	1	10101	BLOCK WORD 0-5	0
6	1	10010	BLOCK WORD 0-6	0
7	1	00111	BLOCK WORD 0-7	0

Memory Block:

Block	Value	Tag	Dirty Bit
0	0	00000	0
1	0	00001	0
2	0	00010	0
3	0	01000	0
4	0	10000	0
5	0	10101	0
6	0	10010	0
7	0	00111	0

Statistics:

Hit Ratio: 87.5%

Miss Ratio: 12.5%

Instruction List:

- Load 0 (0x0)
- Load 1 (0x1)
- Load 2 (0x2)
- Load 3 (0x3)
- Load 4 (0x4)
- Load 5 (0x5)
- Load 6 (0x6)
- Load 7 (0x7)
- Load 0 (0x0)
- Load 1 (0x1)
- Load 2 (0x2)
- Load 8 (0x8)
- Load 10 (0xA)
- Load 15 (0xF)
- Load 15 (0xF)
- Load 12 (0xC)

Used Index: 7

Load Index: 6

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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