

Microprocessor and Computer Architecture Laboratory

UE23CS251B

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Week#____9_____ Exercise: ____1__

1. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag.

Randomly generate 10 addresses and find hit rate and miss rate.

Include One Screenshot(for Write Back Cache) with

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

ii) Screenshot showing the Cache Table

iii) Screenshot showing hit and miss rates

Replacement Policies
☒ FIFO ☐ LRU ☐ Random

Write Policies
☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2) 16384
Memory Size (power of 2) 131072
Offset Bits 8

Reset Submit

Instruction Load

Information
The cycle has been completed.
Please submit another instructions

Next Fast Forward

Statistics
Hit Rate : 100%
Miss Rate : 90%

List of Previous Instructions :

- Load 40F3 (Miss)
- Load 33F3 (Miss)
- Load 89E7 (Miss)
- Load 05F2 (Miss)
- Load 2670 (Miss)
- Load 32C5 (Hit)
- Load 7049 (Miss)
- Load 150C2 (Miss)
- Load 8F7 (Miss)
- Load 5487 (Miss)

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown
0010 4 bit 10100 5 bit 10000111 8 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	3	B: 60 W: 0 - 255	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	1	1	B: 26 W: 0 - 255	0
7	0	-	0	0
8	0	-	0	0
9	1	0	B: 9 W: 0 - 255	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	1	c	B: 192 W: 0 - 255	0
19	1	1	B: 33 W: 0 - 255	0
20	1	2	B: 54 W: 0 - 255	0
21	1	4	B: 95 W: 0 - 255	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	1	6	B: 08 W: 0 - 255	0
28	0	-	0	0
29	1	3	B: 70 W: 0 - 255	0

Memory Block

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0

Week# 9 Exercise: 2

2. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

Consider a main memory having 64-byte capacity and cache memory of 8 bytes initially empty

The following addresses are generated by the CPU. All values in hexadecimal

0,3,4,1,2,5,7,6,0,3,1,11,5,15,9,4,0,4,3

Clearly label data that is replaced in cache lines. Show the cache memory table and filled data in the cache lines of block size 1 byte. LRU Policy is used. The cache is mapped as a) Two way set Associative b) Four Way Set associative

Include Two Screenshots, one for Two way Set Associative(for Write Back Cache), One for four way Set Associative (for Write

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

ii) Screenshot showing the Cache Table

iii) Screenshot showing hit and miss rates

Replacement Policies

☐ FIFO ☒ LRU ☐ Random

Write Policies

☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

Reset	Submit
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Instruction

Load ☒ jn null

List of next 10 instructions:

	Submit
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Information

The cycle has been completed.
Please submit another instructions.

Next	Fast Forward
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2-WAY SET ASSOCIATIVE CACHE

➤ Instruction Breakdown

0000	11	0
4 bit	2 bit	0 bit

🗄️ Memory Cache

B 5 W 0
B 4 W 0
B 3 W 0
B 2 W 0
B 1 W 0
A 0 W 0

🗃️ Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B 5 W 0 - 0	0
1	1	2	BLOCK 9 WORD 0 - 0	0
2	1	0	B 2 W 0 - 0	0
3	1	0	B 3 W 0 - 0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	BLOCK 4 WORD 0 - 0	0
1	1	5	BLOCK 15 WORD 0 - 0	0
2	1	1	BLOCK 6 WORD 0 - 0	0
3	1	1	BLOCK 7 WORD 0 - 0	0

Statistics

Hit Rate : 37%

Miss Rate : 63%

List of Previous Instructions :

- Load 3 [Miss]
- Load 3 [Miss]
- Load 4 [Miss]
- Load 1 [Miss]
- Load 3 [Miss]
- Load 5 [Miss]
- Load 7 [Miss]
- Load 5 [Miss]
- Load 0 [Hit]
- Load 0 [Hit]
- Load 1 [Hit]
- Load 5 [Miss]
- Load 3 [Miss]
- Load 5 [Miss]
- Load 4 [Hit]
- Load 0 [Hit]
- Load 4 [Hit]
- Load 0 [Hit]

Replacement Policies

☐ FIFO
☒ LRU
☐ Random

Write Policies

☐ Write Back
☐ Write Through

☒ Write On Allocate
☐ Write Around

Cache Size (power of 2)

8

Memory Size (power of 2)

64

Offset Bits

0

Reset

Submit

Instruction

Load

in reg1

List of next 10 instructions

Submit

Information

The cycle has been completed.
Please submit another instructions

Next

Fast Forward

Statistics

Hit Rate: 100%

Miss Rate: 00%

List of Previous Instructions

Load 0 (Miss)

Load 1 (Miss)

Load 2 (Miss)

Load 3 (Miss)

Load 4 (Miss)

Load 5 (Miss)

Load 6 (Miss)

Load 7 (Miss)

Load 8 (Miss)

Load 9 (Hit)

Load 0 (Hit)

Load 1 (Hit)

Load 2 (Miss)

Load 3 (Miss)

Load 4 (Hit)

Load 5 (Hit)

Load 6 (Hit)

Load 7 (Hit)

Load 8 (Hit)

Load 9 (Hit)

Load 0 (Hit)

4-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

0001

1

0

5 bit

1 bit

0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B: 0 W: 0-0	0
1	1	a	B: 15 W: 0-0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	B: 4 W: 0-0	0
1	1	4	B: 9 W: 0-0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B: 2 W: 0-0	0
1	1	1	B: 3 W: 0-0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	3	B: 6 W: 0-0	0
1	1	2	B: 5 W: 0-0	0

Memory Block

B: 3 W: 0

B: 4 W: 0

B: 5 W: 0

B: 6 W: 0

B: 7 W: 0

B: 8 W: 0

Week# ____9____

Exercise: ____3__

3. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

Consider 2 way set associative mapping with following design :
cache memory is 16 bytes and main memory is 256 bytes. The offset bits is 2 . calculate the hit ratio and miss ratio for the following sequence:

3,6,0,8,5,1C,14,15,2,1D,11

Use LRU and FIFO as replacement policy

Include Two Screenshots(for LRU with Write Back Cache, FIFO with Write Back cache) with

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

ii) Screenshot showing the Cache Table

iii) Screenshot showing hit and miss rates

a) LRU with Write Back Cache:

Replacement Policies: ☐ FIFO ☒ LRU ☐ Random

Write Policies: ☒ Write Back ☐ Write Through ☐ Write On Allocate ☐ Write Around

Cache Size (power of 2): 16
Memory Size (power of 2): 256
Offset Bits: 2

Reset Submit

Instruction: Load (in hex) []
List of next 10 instructions: [] Submit

Information: The cycle has been completed. Please submit another instructions.

Next Fast Forward

Statistics:
Hit Rate : 45%
Miss Rate : 55%
List of Previous Instructions :
• Load 3 (Miss)
• Load 6 (Miss)
• Load 0 (Hit)
• Load 8 (Miss)
• Load 5 (Hit)
• Load 1C (Miss)
• Load 14 (Miss)
• Load 15 (Hit)
• Load 2 (Hit)
• Load 1D (Hit)
• Load 11 (Miss)

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

00010	0	01
5 bit	1 bit	2 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B 0 W 0 - 3	0
1	1	2	BLOCK 5 WORD 0 - 3	0

Memory Block

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	BLOCK 4 WORD 0 - 3	0
1	1	3	BLOCK 7 WORD 0 - 3	0

b) FIFO with Write Back Cache:

Replacement Policies: ☒ FIFO ☐ LRU ☐ Random

Write Policies: ☒ Write Back ☐ Write Through ☐ Write On Allocate ☐ Write Around

Cache Size (power of 2): 16
Memory Size (power of 2): 256
Offset Bits: 2

Reset Submit

Instruction: Load (in hex) []
List of next 10 instructions: [] Submit

Information: The cycle has been completed. Please submit another instructions.

Next Fast Forward

Statistics:
Hit Rate : 45%
Miss Rate : 55%
List of Previous Instructions :
• Load 3 (Miss)
• Load 6 (Miss)
• Load 0 (Hit)
• Load 8 (Miss)
• Load 5 (Hit)
• Load 1C (Miss)
• Load 14 (Miss)
• Load 15 (Hit)
• Load 2 (Hit)
• Load 1D (Hit)
• Load 11 (Miss)

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

00010	0	01
5 bit	1 bit	2 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	BLOCK 4 WORD 0 - 3	0
1	1	2	BLOCK 5 WORD 0 - 3	0

Memory Block

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	BLOCK 2 WORD 0 - 3	0
1	1	3	BLOCK 7 WORD 0 - 3	0

4. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

Consider 4 way set associative mapping with following design :
 cache memory is 16bytes and main memory is 256 bytes. The offset bits is 2 . calculate the hit ratio and miss ratio for the following sequence:

3,6,0,8,5,1c,14,15,2,1D,11

Use replacement algorithm as LRU and FIFO.

Include Two Screenshots(LRU with Write Back Cache, FIFO with Write Back cache)

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

ii) Screenshot showing the Cache Table

iii) Screenshot showing hit and miss rates

a) LRU with Write Back Cache:

The screenshot displays the PARACACHE SIMULATOR interface for a 4-WAY SET ASSOCIATIVE CACHE. The configuration is set to LRU replacement policy and Write Back cache policy. The cache size is 16 bytes (power of 2), memory size is 256 bytes (power of 2), and offset bits are 2. The instruction breakdown shows a sequence of 11 instructions: 000100 (6 bits), 0 (0 bit), 01 (2 bit), and 0 (0 bit). The memory block shows 16 blocks (B.4 W.0 to B.9 W.3). The cache table shows 4 sets, each with 4 ways. The statistics show a Hit Rate of 36% and a Miss Rate of 64%. The list of previous instructions shows 11 instructions, all of which are misses.

Replacement Policies
☐ FIFO ☒ LRU ☐ Random

Write Policies
☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2): 16
Memory Size (power of 2): 256
Offset Bits: 2

Instruction Breakdown

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	5	B.5 W.0-3	0
1	1	4	B.4 W.0-3	0
2	1	0	B.0 W.0-3	0
3	1	7	B.7 W.0-3	0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	5	B.5 W.0-3	0
1	1	4	B.4 W.0-3	0
2	1	0	B.0 W.0-3	0
3	1	7	B.7 W.0-3	0

Statistics
 Hit Rate : 36%
 Miss Rate : 64%

List of Previous Instructions :

- Load 3 (Miss)
- Load 6 (Miss)
- Load 0 (Hit)
- Load 8 (Miss)
- Load 5 (Hit)
- Load 1C (Miss)
- Load 14 (Miss)
- Load 15 (Hit)
- Load 2 (Miss)
- Load 1D (Hit)
- Load 11 (Miss)

b) FIFO with Write Back Cache:

Replacement Policies
☒ FIFO ☐ LRU ☐ Random

Write Policies
☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2): 16
Memory Size (power of 2): 256
Offset Bits: 2

Instruction
 Load [in hex]
 List of next 10 Instructions

Information
 The cycle has been completed.
 Please submit another instructions

Statistics
 Hit Rate : 36%
 Miss Rate : 64%

List of Previous Instructions :

- Load 3 (Miss)
- Load 6 (Miss)
- Load 9 (Hit)
- Load 8 (Miss)
- Load 5 (Hit)
- Load 10 (Miss)
- Load 14 (Miss)
- Load 13 (Hit)
- Load 2 (Miss)
- Load 11 (Hit)
- Load 11 (Miss)

4-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

000100	0	01
6 bit	0 bit	2 bit

Memory Block

B.4 W.0	B.4 W.1	B.4 W.2	B.4 W.3
B.5 W.0	B.5 W.1	B.5 W.2	B.5 W.3
B.6 W.0	B.6 W.1	B.6 W.2	B.6 W.3
B.7 W.0	B.7 W.1	B.7 W.2	B.7 W.3
B.8 W.0	B.8 W.1	B.8 W.2	B.8 W.3
B.9 W.0	B.9 W.1	B.9 W.2	B.9 W.3

Cache Table

Index/Valid	Tag	Data (Hex)	Dirty Bit
0	1	5	B.5 W.0-3
0	1	0	B.0 W.0-3
0	1	4	B.4 W.0-3
0	1	7	B.7 W.0-3

Week# 9 Exercise: 5

5. Use PARACACHE SIMULATOR for the exercise for the following configuration. (Cache Analysis)

Problem 1) Consider the following Design

FIFO, Write Back, Write Allocate

Main Memory = 128 Offset/word = 3 Cache size (Each) = 32

Cache 1 Direct Mapped Cache Cache 2 Fully associative Cache

Cache 3 2 Way Set Associative Cache Cache 4 4 Way Set Associative

List of Instructions

Input L-20, L-6, L-19, L-5E, L-29, L-20, L-1A, L-4B, L-20, L-1, L-F, L-5E

Include

i) One Screenshot of Cache Address Table showing the splitup of the address fields for each level of cache

Cache Comparison

1. Direct Mapped Cache[4] HIT 0 MISS 4 || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	INDEX	OFFSET
2 bit	2 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

2. Fully Associative Cache[4] HIT 0 MISS 4 || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	OFFSET
4 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

3. 2-Way Set Associative Cache[2] HIT 0 MISS 4 || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	INDEX	OFFSET
3 bit	1 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

4. 4-Way Set Associative Cache[1] HIT 0 MISS 4 || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	INDEX	OFFSET
4 bit	0 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0

ii) 2 Screenshots showing hit and miss rates for each cache level wrt the requests generated by the processor

CACHE TYPE ANALYSIS

Current Instruction (in Hex): 5E

List of Instructions (in Hex) | Split by comma

Gen. 88 Random Instructions Submit Next Instruction Fast Forward Reset

Cache Comparison

1. Direct Mapped Cache[4] HIT 8% MISS 92% || ADD. RESOURCES 36 NAND

Instruction Breakdown

10	11	110
2 bit	2 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	BLOCK 0 WORD 0 - 7	0
1	1	0	BLOCK 1 WORD 0 - 7	0
2	0	-	0	0
3	1	10	BLOCK B WORD 0 - 7	0

2. Fully Associative Cache[4] HIT 17% MISS 83% || ADD. RESOURCES 400 NAND

Instruction Breakdown

1011	110
4 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	BLOCK 1 WORD 0 - 7	0
1	1	11	BLOCK B WORD 0 - 7	0
2	1	9	BLOCK 9 WORD 0 - 7	0
3	1	0	BLOCK 0 WORD 0 - 7	0

3. 2-Way Set Associative Cache[2] HIT 26% MISS 74% || ADD. RESOURCES 144 NAND

Instruction Breakdown

101	1	110
3 bit	1 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	B 4 W 0 - 7	0
1	1	5	B 5 W 0 - 7	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
1	1	0	B 1 W 0 - 7	0

4. 4-Way Set Associative Cache[1] HIT 17% MISS 83% || ADD. RESOURCES 272 NAND

Instruction Breakdown

1011	0	110
4 bit	0 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B 1 W 0 - 7	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	11	B 8 W 0 - 7	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	9	B 9 W 0 - 7	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B 0 W 0 - 7	0

Week# 9 Exercise: 6

6. Try using PARACACHE SIMULATOR for the exercise for the following configuration .

Consider the following Design

FIFO, Write Back, Write Allocate

Main Memory= 2048 Offset/word=3 Cache size(Each)= 64

Cache 1 Direct Mapped Cache Cache 2 Fully associative Cache

Cache 3 2 Way Set Associative Cache Cache 4 4 Way Set Associative

List of Instructions

Input L-20,L-6,L-19,L-5E,L-29,L-20,L-1A,L-4B,L-20,L-1,L-F,L-5E

Include

i) **One Screenshot of Cache Address Table showing the splitup of the address fields for each level of cache**

Cache Comparison

1. Direct Mapped Cache[8]

HIT MISS WADO. RESOURCES NAND

Instruction Breakdown

TAG			INDEX		OFF SET	
5 bit			3 bit		3 bit	

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0

2. Fully Associative Cache[8]

HIT MISS WADO. RESOURCES NAND

Instruction Breakdown

TAG			OFF SET	
8 bit			3 bit	

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0

3. 2-Way Set Associative Cache[4]

HIT MISS WADO. RESOURCES NAND

Instruction Breakdown

TAG			INDEX		OFF SET	
8 bit			2 bit		3 bit	

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

4. 4-Way Set Associative Cache[2]

HIT MISS WADO. RESOURCES NAND

Instruction Breakdown

TAG			INDEX		OFF SET	
7 bit			1 bit		3 bit	

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

ii) 2 Screenshots showing hit and miss rates for each cache level wrt the requests generated by the processor

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

☒ FIFO ☐ LRU

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Memory Size (power of 2) 2048

Offset Bits 3

Cache 1 ☐ Direct Mapped Cache

Size (in hex) # 64

Cache 2 ☐ Fully Associative Cache

Size (in hex) # 64

Cache 3 ☐ 2-Way Set Associative Cache

Size (in hex) # 64

Cache 4 ☐ 4-Way Set Associative Cache

Size (in hex) # 64

Gen. Random Configuration

Reset Submit

List of Previous Instructions :

- Load 20 [M] [M] [M] [M]
- Load 6 [M] [M] [M] [M]
- Load 19 [M] [M] [M] [M]
- Load 5C [M] [M] [M] [M]
- Load 29 [M] [M] [M] [M]
- Load 20 [H] [H] [H] [H]
- Load 1A [M] [H] [H] [H]
- Load 4B [M] [M] [M] [M]
- Load 20 [H] [H] [H] [H]
- Load 5 [H] [H] [H] [H]
- Load 7 [M] [M] [M] [M]
- Load 5E [M] [H] [H] [H]

CACHE TYPE ANALYSIS

List of instructions (in Hex) | Split by comma

Gen. 88 Random Instructions Submit Next Instruction Fast Forward Reset

Current Instruction (in Hex) 5E

Cache Comparison

1. Direct Mapped Cache[8] HIT 25% MISS 75% (1) ADD. RESOURCES 164 NAND

Instruction Breakdown

00001	011	110
5 bit	3 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	BLOCK 0 WORD 0 - 7	0
1	1	0	BLOCK 1 WORD 0 - 7	0
2	0	-	0	0
3	1	00001	BLOCK 8 WORD 0 - 7	0
4	1	0	BLOCK 4 WORD 0 - 7	0
5	1	0	BLOCK 5 WORD 0 - 7	0
6	0	-	0	0
7	0	-	0	0

2. Fully Associative Cache[8] HIT 42% MISS 58% (1) ADD. RESOURCES 1192 NAND

Instruction Breakdown

00001011	110
8 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	4	BLOCK 4 WORD 0 - 7	0
1	1	0	BLOCK 0 WORD 0 - 7	0
2	1	3	BLOCK 3 WORD 0 - 7	0
3	1	11	BLOCK 8 WORD 0 - 7	0
4	1	5	BLOCK 5 WORD 0 - 7	0
5	1	9	BLOCK 9 WORD 0 - 7	0
6	1	1	BLOCK 1 WORD 0 - 7	0
7	0	-	0	0

3. 2-Way Set Associative Cache[4] HIT 42% MISS 58% (1) ADD. RESOURCES 264 NAND

Instruction Breakdown

000010	11	110
6 bit	2 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B. 4 W. 0 - 7	0
1	1	0	B. 1 W. 0 - 7	0
2	0	-	0	0
3	1	0	B. 3 W. 0 - 7	0

4. 4-Way Set Associative Cache[2] HIT 42% MISS 58% (1) ADD. RESOURCES 376 NAND

Instruction Breakdown

0000101	1	110
7 bit	1 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	B. 4 W. 0 - 7	0
1	1	0	B. 1 W. 0 - 7	0

Week# 9 Exercise: 7

7. Use PARACACHE SIMULATOR for the exercise for the following configuration .Consider the following Design

FIFO, Write Back, Write Allocate

Main Memory= 2048 Offset/word=2

Cache size(Each)= 32

Cache 1 Direct Mapped Cache Cache 2 Fully associative Cache

Cache 3 2 Way Set Associative Cache Cache 4 4 Way Set Associative

List of Instructions

Input L-20,L-6,L-19,L-5E,L-29,L-20,L-1A,L-4B,L-20,L-1,L-F,L-5E

Include

i) One Screenshot of Cache Address Table showing the splitup of the address fields for each level of cache

Cache Comparison

1. Direct Mapped Cache[8]

Instruction Breakdown

HIT MISS ADD. RESOURCES NAND

TAG				INDEX				OFF SET			
9 bit				3 bit				2 bit			
Index	Valid	Tag		Data (Hex)		Dirty Bit					
0	0	-		0		0					
1	0	-		0		0					
2	0	-		0		0					
3	0	-		0		0					
4	0	-		0		0					
5	0	-		0		0					
6	0	-		0		0					
7	0	-		0		0					

2. Fully Associative Cache[8]

Instruction Breakdown

HIT MISS ADD. RESOURCES NAND

TAG				OFF SET			
9 bit				2 bit			
Index	Valid	Tag		Data (Hex)		Dirty Bit	
0	0	-		0		0	
1	0	-		0		0	
2	0	-		0		0	
3	0	-		0		0	
4	0	-		0		0	
5	0	-		0		0	
6	0	-		0		0	
7	0	-		0		0	

3. 2-Way Set Associative Cache[4]

Instruction Breakdown

HIT MISS ADD. RESOURCES NAND

TAG				INDEX				OFF SET					
7 bit				2 bit				2 bit					
Index	Valid	Tag		Data (Hex)		Dirty Bit	Index	Valid	Tag		Data (Hex)		Dirty Bit
0	0	-		0		0	0	0	-		0		0
1	0	-		0		0	1	0	-		0		0
2	0	-		0		0	2	0	-		0		0
3	0	-		0		0	3	0	-		0		0

4. 4-Way Set Associative Cache[2]

Instruction Breakdown

HIT MISS ADD. RESOURCES NAND

TAG				INDEX				OFF SET					
8 bit				1 bit				2 bit					
Index	Valid	Tag		Data (Hex)		Dirty Bit	Index	Valid	Tag		Data (Hex)		Dirty Bit
0	0	-		0		0	0	0	-		0		0
1	0	-		0		0	1	0	-		0		0

ii) 2 Screenshots showing hit and miss rates for each cache level wrt the requests generated by the processor

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

☒ FIFO ☐ LRU

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Memory Size (power of 2) 2048

Offset Bits 2

Cache 1 ☐ Direct Mapped Cache

Size (in hex) # 32

Cache 2 ☐ Fully Associative Cache

Size (in hex) # 32

Cache 3 ☐ 2-Way Set Associative Cache

Size (in hex) # 32

Cache 4 ☐ 4-Way Set Associative Cache

Size (in hex) # 32

Gen Random Configuration

Reset Submit

List of Previous Instructions:

- Load 29 [M] [M] [M]
- Load 6 [M] [M] [M]
- Load 19 [M] [M] [M]
- Load 62 [M] [M] [M]
- Load 29 [M] [M] [M]
- Load 29 [H] [H] [H]
- Load 16 [H] [H] [H]
- Load 48 [M] [M] [M]
- Load 29 [H] [H] [H]
- Load 1 [M] [M] [M]
- Load 52 [H] [H] [H]

Current Instruction (in Hex) 5E

Cache Type Analysis

List of instructions (in Hex) | Split by comma

Gen 88 Random Instructions Submit Next Instruction Fast Forward Reset

Cache Comparison

1. Direct Mapped Cache[8] HIT 33% MISS 67% (1 ADD, RESOURCES 148) NAND

Instruction Breakdown

000010		111		10	
6 bit		3 bit		2 bit	
Index	Valid	Tag	Data (Hex)	Dirty Bit	
0	1	0	BLOCK 0 WORD 0-3	0	
1	1	0	BLOCK 1 WORD 0-3	0	
2	1	000010	BLOCK 12 WORD 0-3	0	
3	1	0	BLOCK 3 WORD 0-3	0	
4	0	-	0	0	
5	0	-	0	0	
6	0	0	BLOCK 6 WORD 0-3	0	
7	1	000010	BLOCK 17 WORD 0-3	0	

2. Fully Associative Cache[8] HIT 33% MISS 67% (1 ADD, RESOURCES 148) NAND

Instruction Breakdown

000010111		10		
9 bit		2 bit		
Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	8	BLOCK 8 WORD 0-3	0
1	1	1	BLOCK 1 WORD 0-3	0
2	1	6	BLOCK 6 WORD 0-3	0
3	1	23	BLOCK 17 WORD 0-3	0
4	1	10	BLOCK A WORD 0-3	0
5	1	18	BLOCK 12 WORD 0-3	0
6	1	0	BLOCK 0 WORD 0-3	0
7	1	3	BLOCK 3 WORD 0-3	0

3. 2-Way Set Associative Cache[4] HIT 33% MISS 67% (1 ADD, RESOURCES 272) NAND

Instruction Breakdown

0000101		11		10	
7 bit		2 bit		2 bit	
Index	Valid	Tag	Data (Hex)	Dirty Bit	
0	1	2	B. 8 W. 0-3	0	
1	1	0	B. 1 W. 0-3	0	
2	1	4	B. 12 W. 0-3	0	
3	1	5	B. 17 W. 0-3	0	

4. 4-Way Set Associative Cache[2] HIT 33% MISS 67% (1 ADD, RESOURCES 416) NAND

Instruction Breakdown

00001011		1		10	
8 bit		1 bit		2 bit	
Index	Valid	Tag	Data (Hex)	Dirty Bit	
0	1	0	B. 0 W. 0-3	0	
1	1	0	B. 1 W. 0-3	0	

Week# 9 Exercise: 8

Try using PARACACHE SIMULATOR for the exercise for the following configuration .Consider the following Design

FIFO, Write Back, Write Allocate

Memory size: 64 Offset:0 Cache size:8

Cache 1 Direct Mapped Cache Cache 2 Fully associative Cache

Cache 3 2 Way Set Associative Cache Cache 4 4 Way Set Associative

Input=L-0,L-3,L-4,L-1,L-2,L-5,L-7,S-6,L-0,L-3,L-1,L-11,L-5,L-15,L-9,S-4,L-0,L-4,S-3,L-12

Include

i) One Screenshot of Cache Address Table showing the splitup of the address fields for each level of cache

Cache Comparison

1. Direct Mapped Cache[8]

Instruction Breakdown

TAG

INDEX

OFF SET

3 bit

3 bit

0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0

HIT MISS !ADD. RESOURCES NAND

2. Fully Associative Cache[8]

Instruction Breakdown

TAG

OFF SET

6 bit

0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0

HIT MISS !ADD. RESOURCES NAND

3. 2-Way Set Associative Cache[4]

Instruction Breakdown

TAG

INDEX

OFF SET

4 bit

2 bit

0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

HIT MISS !ADD. RESOURCES NAND

4. 4-Way Set Associative Cache[2]

Instruction Breakdown

TAG

INDEX

OFF SET

5 bit

1 bit

0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

HIT MISS !ADD. RESOURCES NAND

ii) 2 Screenshots showing hit and miss rates for each cache level wrt the requests generated by the processor

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

☒ FIFO ☐ LRU

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Memory Size (power of 2) 64

Offset Bits 0

Cache 1 ☐ Direct Mapped Cache

Size (in hex) # 8

Cache 2 ☐ Fully Associative Cache

Size (in hex) # 8

Cache 3 ☐ 2-Way Set Associative Cache

Size (in hex) # 8

Cache 4 ☐ 4-Way Set Associative Cache

Size (in hex) # 8

Gen. Random Configuration

Reset Submit

List of Previous Instructions :

- Load 0 (M | M | M | M)
- Load 3 (M | M | M | M)
- Load 0 (M | M | M | M)
- Load 1 (M | M | M | M)
- Load 2 (M | M | M | M)
- Load 5 (M | M | M | M)
- Load 7 (M | M | M | M)
- Store 6 (M | M | M | M)
- Load 0 (H | H | H | H)
- Load 2 (H | H | H | H)
- Load 1 (H | H | H | H)
- Load 1 (M | M | M | M)
- Load 5 (H | H | H | H)
- Load 0 (M | M | M | M)
- Store 4 (H | H | H | H)
- Load 0 (H | M | H | H)
- Load 0 (H | H | H | H)
- Store 3 (H | H | H | M)
- Load 12 (M | M | M | M)

CACHE TYPE ANALYSIS

Current Instruction (in Hex) 12

List of instructions (in Hex) | Split by comma

Gen. 88 Random Instructions Submit Next Instruction Fast Forward Reset

Cache Comparison

1. Direct Mapped Cache[8] HIT 40% MISS 60% (ADD. RESOURCES 184) NAND

Instruction Breakdown

010		010		0	
3 bit		3 bit		0 bit	
Index	Valid	Tag	Data (Hex)	Dirty Bit	
0	1	0	BLOCK 0 WORD 0 - 0	0	
1	1	001	BLOCK 9 WORD 0 - 0	0	
2	1	010	BLOCK 12 WORD 0 - 0	0	
3	1	0	BLOCK 3 WORD 0 - 0	1	
4	1	0	BLOCK 4 WORD 0 - 0	1	
5	1	010	BLOCK 15 WORD 0 - 0	0	
6	1	0	BLOCK 6 WORD 0 - 0	0	
7	1	0	BLOCK 7 WORD 0 - 0	0	

2. Fully Associative Cache[8] HIT 25% MISS 75% (ADD. RESOURCES 1808) NAND

Instruction Breakdown

010010		0		
6 bit		0 bit		
Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	17	BLOCK 11 WORD 0 - 0	0
1	1	21	BLOCK 15 WORD 0 - 0	0
2	1	9	BLOCK 9 WORD 0 - 0	0
3	1	4	BLOCK 4 WORD 0 - 0	0
4	1	0	BLOCK 0 WORD 0 - 0	0
5	1	3	BLOCK 3 WORD 0 - 0	0
6	1	18	BLOCK 12 WORD 0 - 0	0
7	1	6	BLOCK 6 WORD 0 - 0	0

3. 2-Way Set Associative Cache[4] HIT 40% MISS 60% (ADD. RESOURCES 336) NAND

Instruction Breakdown

0100		10		0	
4 bit		2 bit		0 bit	
Index	Valid	Tag	Data (Hex)	Dirty Bit	
0	1	0	B. 0 W. 0 - 0	0	
1	1	2	B. 9 W. 0 - 0	0	
2	1	4	B. 12 W. 0 - 0	0	
3	1	0	B. 3 W. 0 - 0	1	

4. 4-Way Set Associative Cache[2] HIT 35% MISS 65% (ADD. RESOURCES 320) NAND

Instruction Breakdown

01001		0		0	
5 bit		1 bit		0 bit	
Index	Valid	Tag	Data (Hex)	Dirty Bit	
0	1	9	B. 12 W. 0 - 0	0	
1	1	6	B. 11 W. 0 - 0	0	

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- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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