Microprocessor and Computer Architecture Laboratory

UE23CS251B

4th Semester, Academic Year 2024-25

Date:12/04/2025

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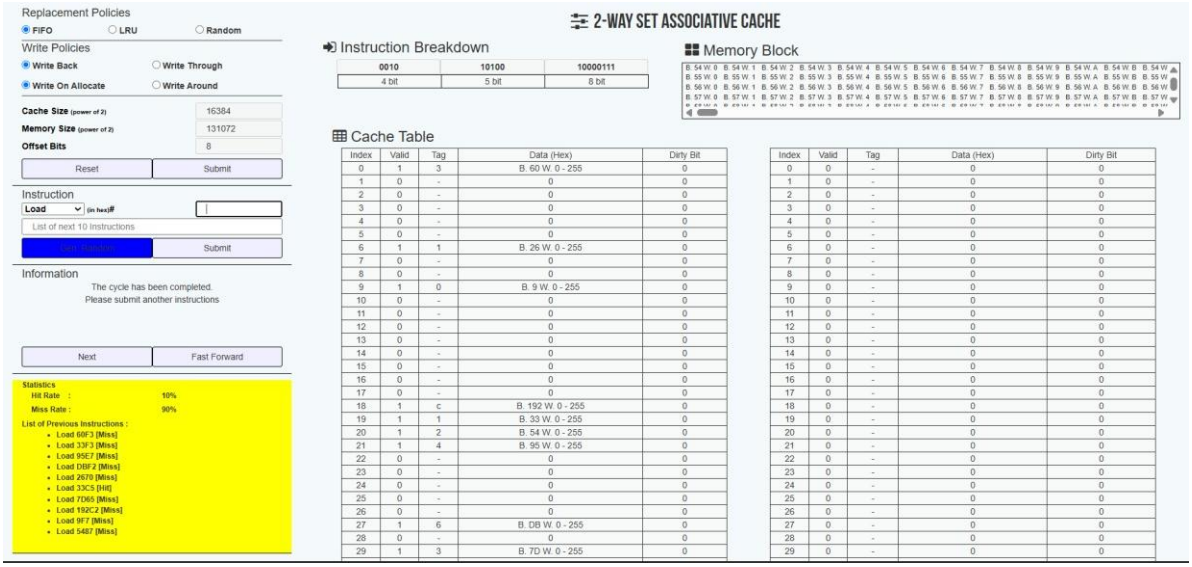
Week#____9_____ Exercise: ____1__

1. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag.
Randomly generate 10 addresses and find hit rate and miss rate.

Include One Screenshot(for Write Back Cache) with
i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor
ii) Screenshot showing the Cache Table
iii) Screenshot showing hit and miss rates



Week#____9_____ Exercise: ____2_

2. Use PARACACHE SIMULATOR for the exercise below given the following configuration .
   Consider a main memory having 64-byte capacity and cache memory of 8 bytes initially empty

The following addresses are generated by the CPU. All values in hexadecimal
0,3,4,1,2,5,7,6,0,3,1,11,5,15,9,4,0,4,3

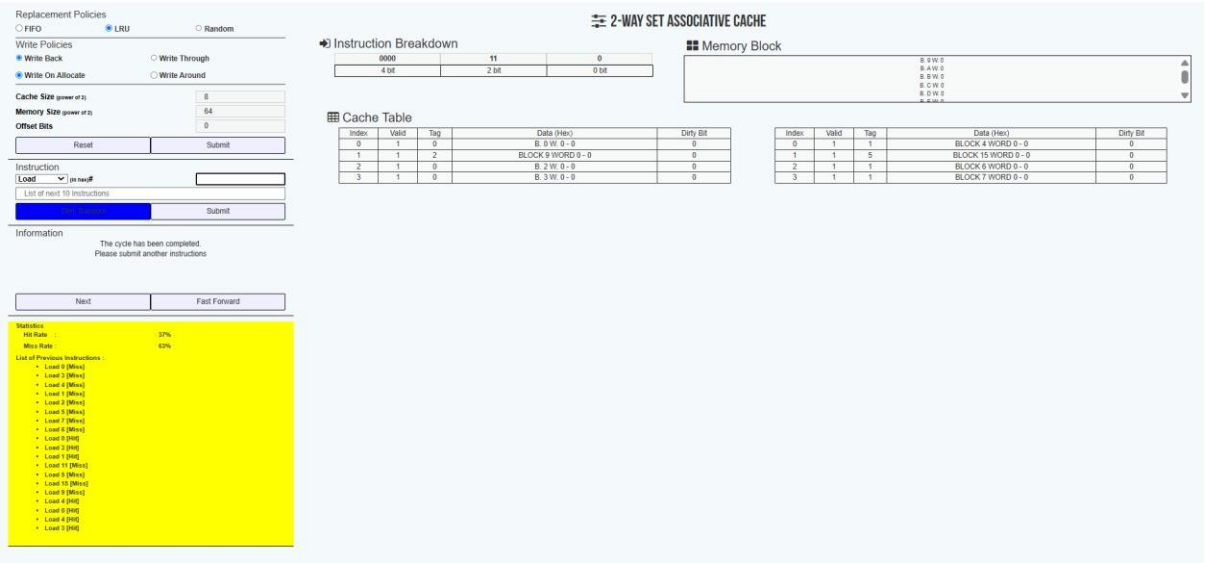
Clearly label data that is replaced in cache lines. Show the cache memory table and filled data in the cache lines of block size 1 byte. LRU Policy is used. The cache is mapped as a)Two way set Associative b)Four Way Set associative

Include Two Screenshots, one for Two way Set Associative(for Write Back Cache), One for four way Set Associative (for Write

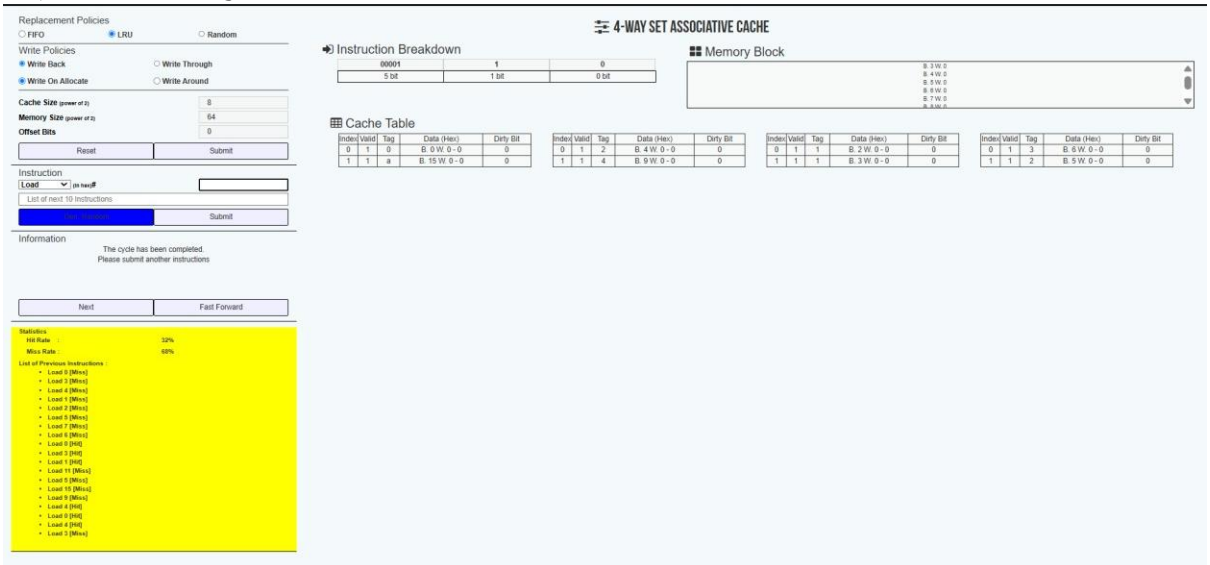
Back Cache) with

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor ii) Screenshot showing the Cache Table iii) Screenshot showing hit and miss rates

a)Two way set Associative



b)Four Way Set associative



Week#____9_____ Exercise: ____3_

3. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

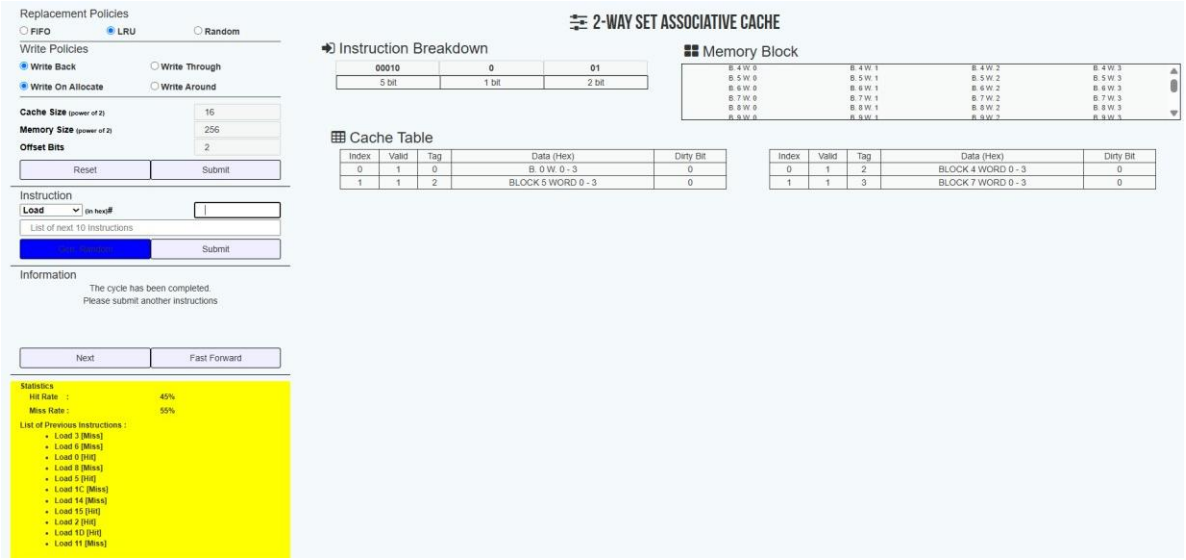
Consider 2 way set associative mapping with following design : cache memory is 16 bytes and main memory is 256 bytes. The offset bits is 2 . calculate the hit ratio and miss ratio for the following sequence:

3,6,0,8,5,1C,14,15,2,1D,11

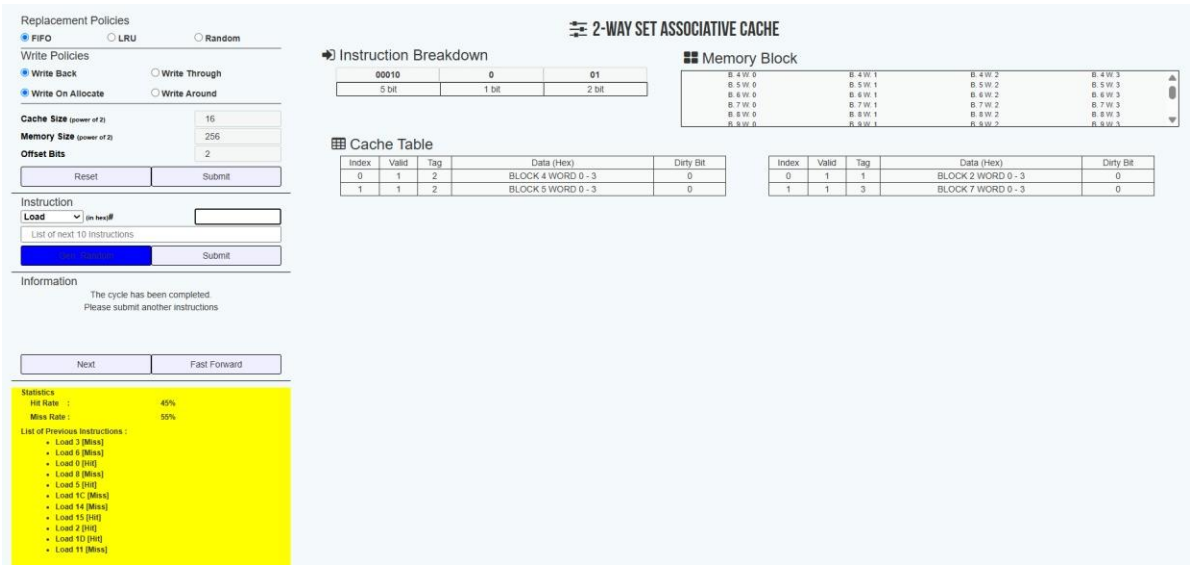
Use LRU and FIFO as replacement policy

Include Two Screenshots(for LRU with Write Back Cache, FIFO with Write Back cache) with
i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor
ii) Screenshot showing the Cache Table
iii) Screenshot showing hit and miss rates

a) LRU with Write Back Cache:



b) FIFO with Write Back Cache:



4.Use PARACACHE SIMULATOR for the exercise below given the following configuration .

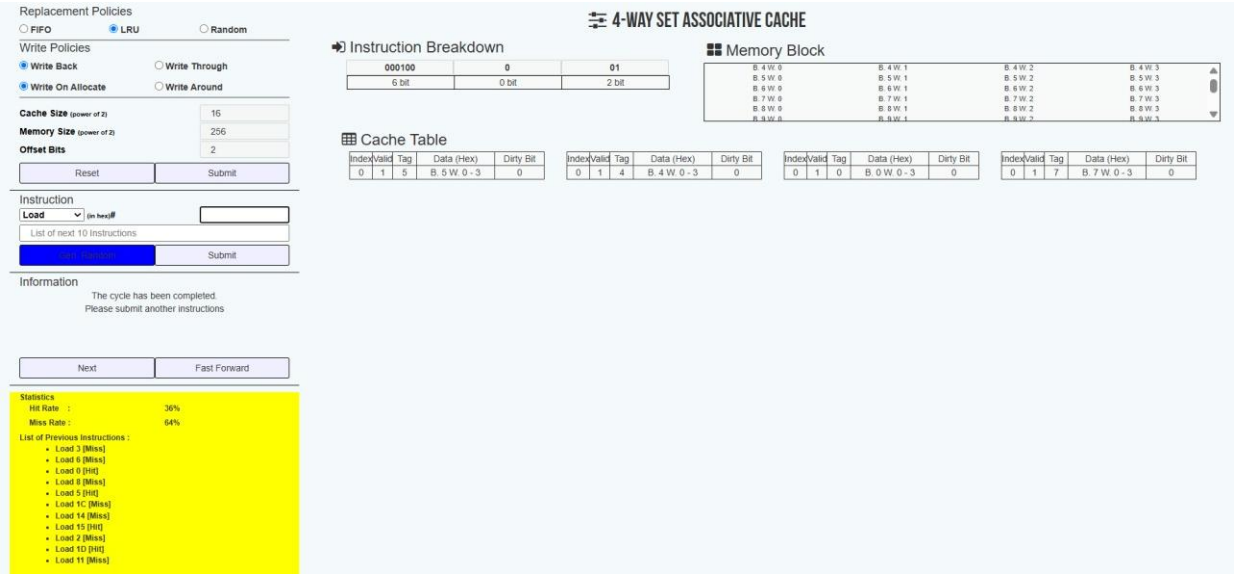
Consider 4 way set associative mapping with following design : cache memory is 16bytes and main memory is 256 bytes. The offset bits is 2 . calculate the hit ratio and miss ratio for the following sequence:

3,6,0,8,5,1c,14,15,2,1D,11

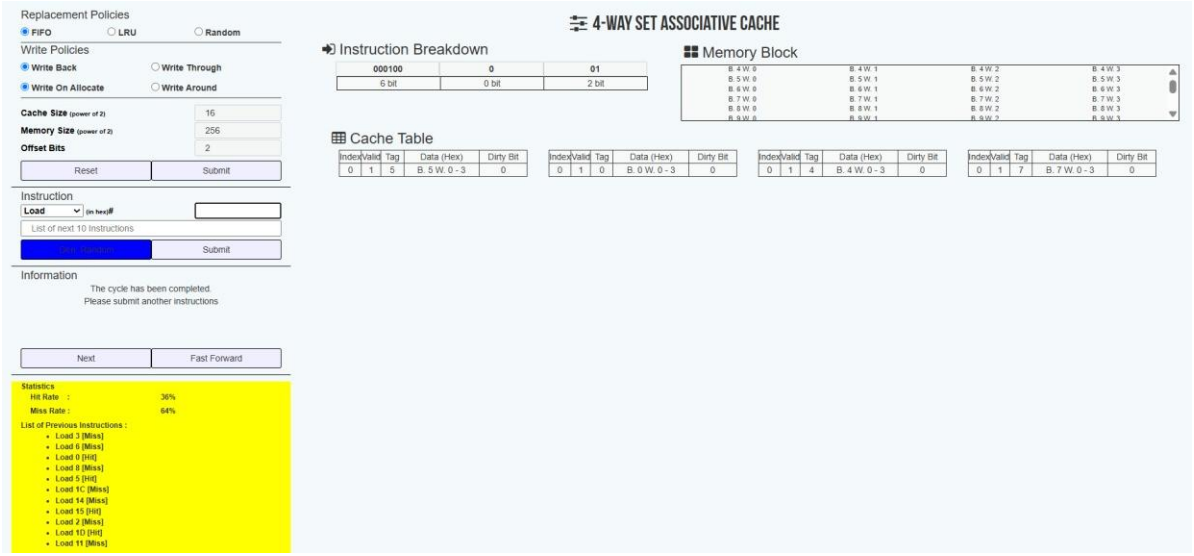
Use replacement algorithm as LRU and FIFO.

Include Two Screenshots(LRU with Write Back Cache, FIFO with Write Back cache)
i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor
ii) Screenshot showing the Cache Table
iii) Screenshot showing hit and miss rates

a) LRU with Write Back Cache:



b) FIFO with Write Back Cache:



Week#____9_____ Exercise: ____5__

5.Use PARACACHE SIMULATOR for the exercise for the following configuration .(Cache Analysis)

Problem 1)Consider the following Design

FIFO, Write Back, Write Allocate

Main Memory= 128 Offset/word=3 Cache size(Each)= 32

Cache 1 Direct Mapped Cache Cache 2 Fully associative Cache

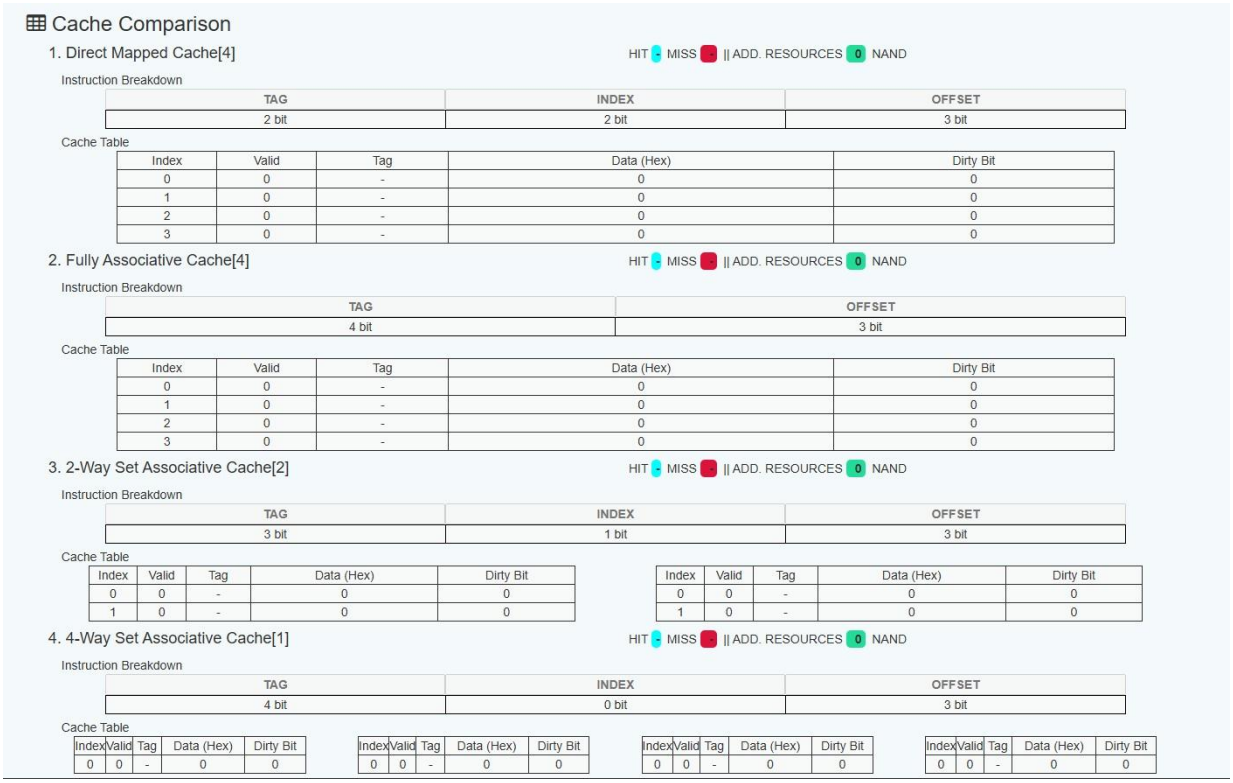
Cache 3 2 Way Set Associative Cache Cache 4 4 Way Set Associative

List of Instructions

Input L-20,L-6,L-19,L-5E,L-29,L-20,L-1A,L-4B,L-20,L-1,L-F,L-5E

Include

i) One Screenshot of Cache Address Table showing the splitup of the address fields for each level of cache



Cache Comparison

1. Direct Mapped Cache[4]

HIT - MISS - || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	INDEX	OFFSET
2 bit	2 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

2. Fully Associative Cache[4]

HIT - MISS - || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	OFFSET
4 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

3. 2-Way Set Associative Cache[2]

HIT - MISS - || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	INDEX	OFFSET
3 bit	1 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

4. 4-Way Set Associative Cache[1]

HIT - MISS - || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	INDEX	OFFSET
4 bit	0 bit	3 bit

Cache Table

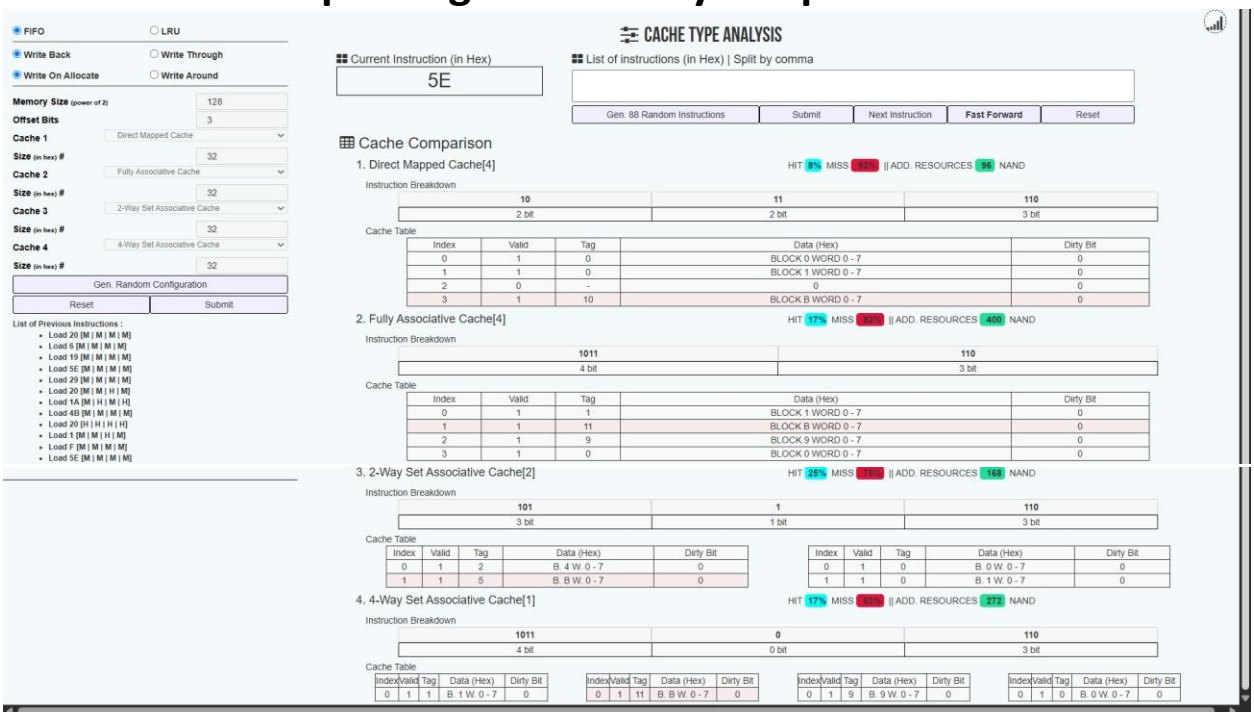
Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0

ii) 2 Screenshots showing hit and miss rates for each cache level wrt the requests generated by the processor



FIFO LRU

Write Back Write Through

Write On Allocate Write Around

Memory Size (power of 2) 128

Offset Bits 3

Cache 1 Direct Mapped Cache

Size (in hex) # 32

Cache 2 Fully Associative Cache

Size (in hex) # 32

Cache 3 2-Way Set Associative Cache

Size (in hex) # 32

Cache 4 4-Way Set Associative Cache

Size (in hex) # 32

Gen. Random Configuration

Reset Submit

List of Previous Instructions :

- Load 20 [M | M | M | M]
- Load 6 [M | M | M | M]
- Load 19 [M | M | M | M]
- Load 5E [M | M | M | M]
- Load 29 [M | M | M | M]
- Load 20 [M | M | H | M]
- Load 1A [M | H | M | H]
- Load 4B [M | M | M | M]
- Load 20 [H | H | H | H]
- Load 1 [M | M | H | M]
- Load F [M | M | M | M]
- Load 5E [M | M | M | M]

CACHE TYPE ANALYSIS

Current Instruction (in Hex)

5E

List of instructions (in Hex) | Split by comma

Gen. 88 Random Instructions | Submit | Next Instruction | Fast Forward | Reset

Cache Comparison

1. Direct Mapped Cache[4]

HIT 8% MISS 92% || ADD. RESOURCES 96 NAND

Instruction Breakdown

10	11	110
2 bit	2 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	BLOCK 0 WORD 0 - 7	0
1	1	0	BLOCK 1 WORD 0 - 7	0
2	0	-	0	0
3	1	10	BLOCK B WORD 0 - 7	0

2. Fully Associative Cache[4]

HIT 17% MISS 83% || ADD. RESOURCES 400 NAND

Instruction Breakdown

1011	110
4 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	BLOCK 1 WORD 0 - 7	0
1	1	11	BLOCK B WORD 0 - 7	0
2	1	9	BLOCK 9 WORD 0 - 7	0
3	1	0	BLOCK 0 WORD 0 - 7	0

3. 2-Way Set Associative Cache[2]

HIT 25% MISS 75% || ADD. RESOURCES 168 NAND

Instruction Breakdown

101	1	110
3 bit	1 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	B. 4 W. 0 - 7	0
1	1	5	B. B W. 0 - 7	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B. 0 W. 0 - 7	0
1	1	0	B. 1 W. 0 - 7	0

4. 4-Way Set Associative Cache[1]

HIT 17% MISS 83% || ADD. RESOURCES 272 NAND

Instruction Breakdown

1011	0	110
4 bit	0 bit	3 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B. 1 W. 0 - 7	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	11	B. B W. 0 - 7	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	9	B. 9 W. 0 - 7	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B. 0 W. 0 - 7	0

Week#____9_____ Exercise: ____6__

6. Try using PARACACHE SIMULATOR for the exercise for the following configuration .

Consider the following Design

FIFO, Write Back, Write Allocate

Main Memory= 2048 Offset/word=3 Cache size(Each)= 64

Cache 1 Direct Mapped Cache Cache 2 Fully associative Cache

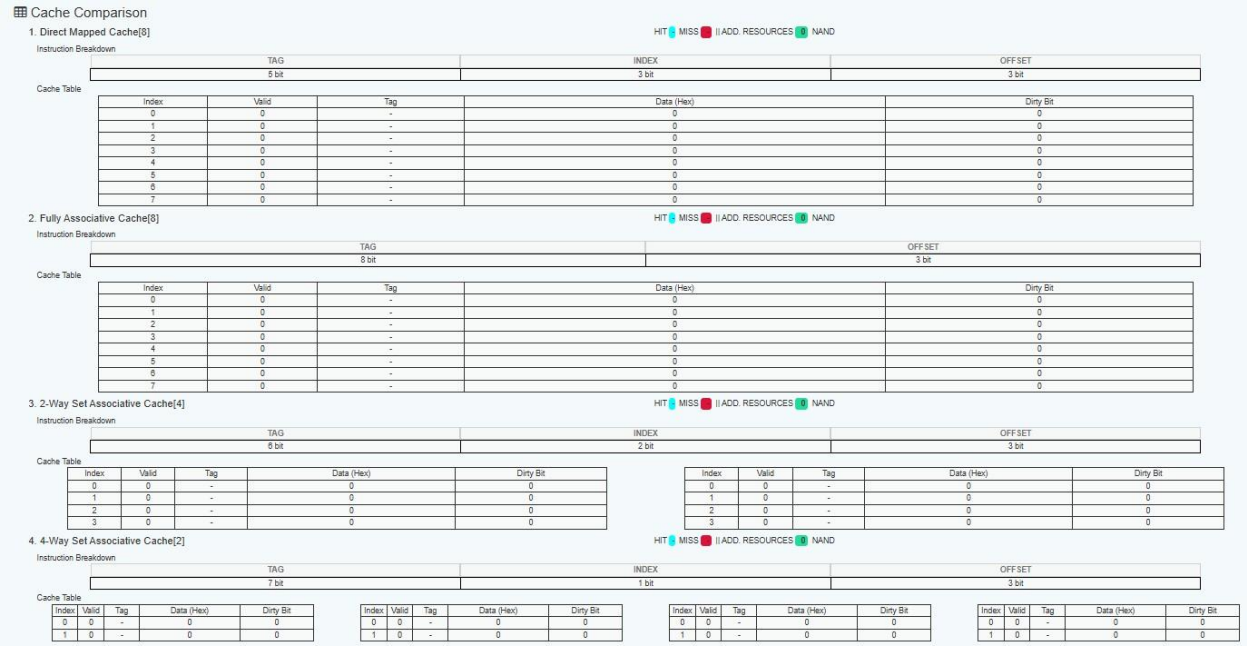
Cache 3 2 Way Set Associative Cache Cache 4 4 Way Set Associative

List of Instructions

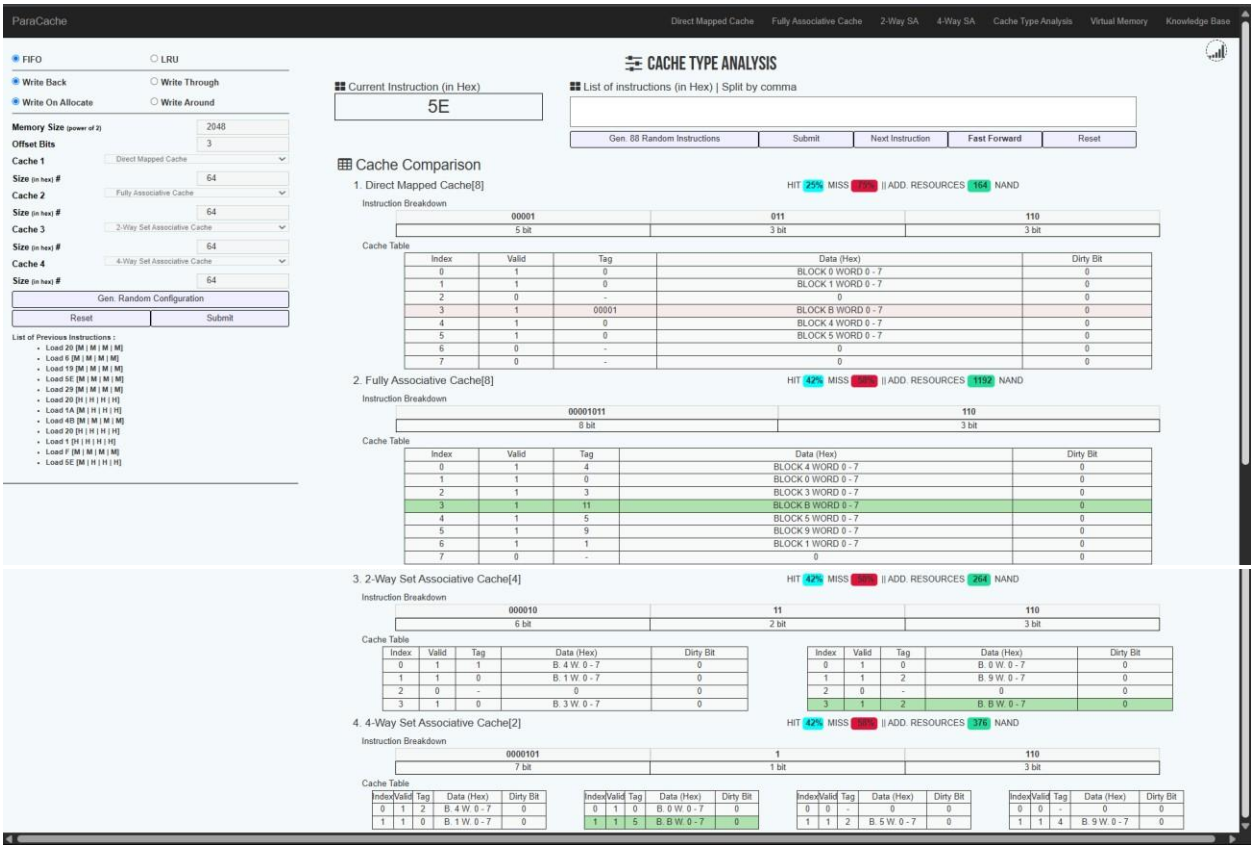
Input L-20,L-6,L-19,L-5E,L-29,L-20,L-1A,L-4B,L-20,L-1,L-F,L-5E

Include

i) **One Screenshot of Cache Address Table showing the splitup of the address fields for each level of cache**



ii) 2 Screenshots showing hit and miss rates for each cache level wrt the requests generated by the processor



Week#____9_____ Exercise: ____7__

7. Use PARACACHE SIMULATOR for the exercise for the following configuration .Consider the following Design

FIFO, Write Back, Write Allocate

Main Memory= 2048 Offset/word=2

Cache size(Each)= 32

Cache 1 Direct Mapped Cache Cache 2 Fully associative Cache

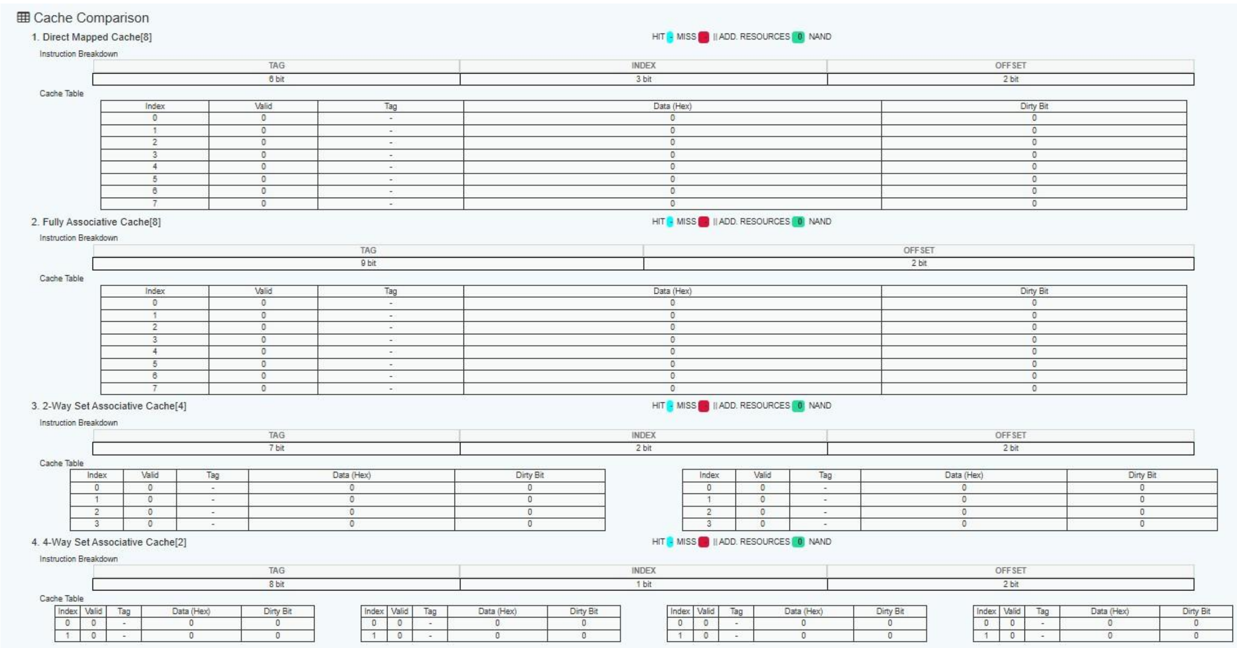
Cache 3 2 Way Set Associative Cache Cache 4 4 Way Set Associative

List of Instructions

Input L-20,L-6,L-19,L-5E,L-29,L-20,L-1A,L-4B,L-20,L-1,L-F,L-5E

Include

i) One Screenshot of Cache Address Table showing the splitup of the address fields for each level of cache



Cache Comparison

1. Direct Mapped Cache[8]

HIT - MISS || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	INDEX	OFFSET
6 bit	3 bit	2 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0

2. Fully Associative Cache[8]

HIT - MISS || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	OFFSET
9 bit	2 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0

3. 2-Way Set Associative Cache[4]

HIT - MISS || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	INDEX	OFFSET
7 bit	2 bit	2 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

4. 4-Way Set Associative Cache[2]

HIT - MISS || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	INDEX	OFFSET
8 bit	1 bit	2 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

ii) 2 Screenshots showing hit and miss rates for each cache level wrt the requests generated by the processor

Week#____9_____ Exercise: ____8__

Try using PARACACHE SIMULATOR for the exercise for the following configuration .Consider the following Design

FIFO, Write Back, Write Allocate

Memory size: 64 Offset:0 Cache size:8

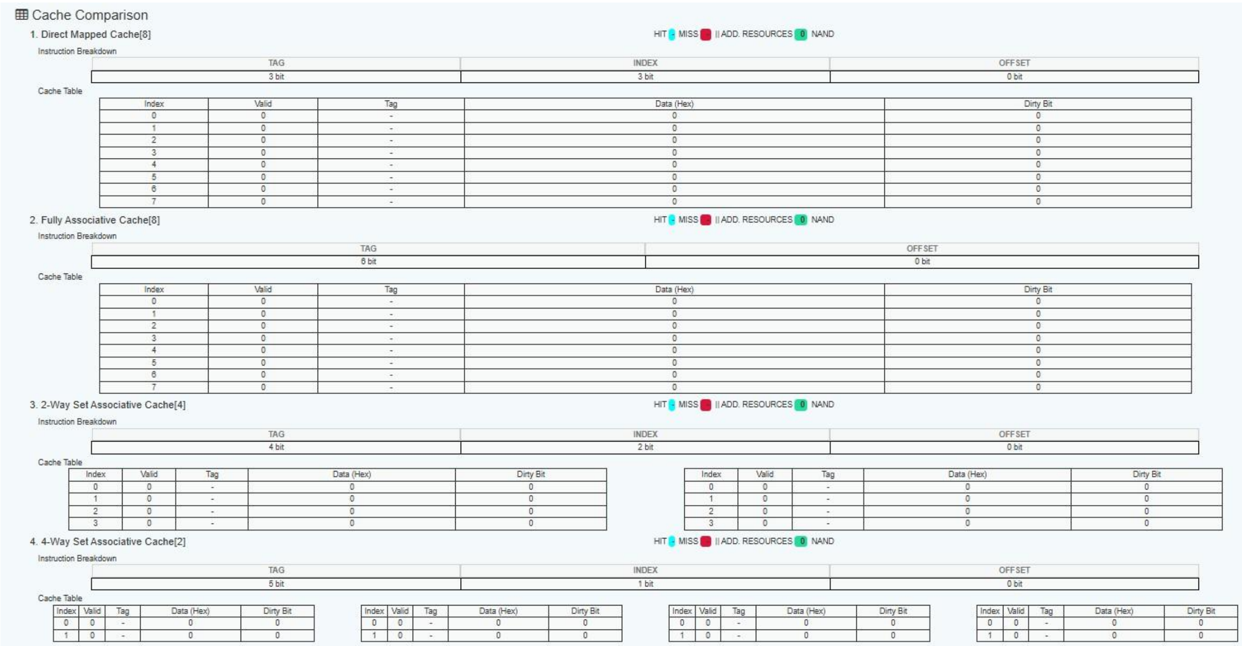
Cache 1 Direct Mapped Cache Cache 2 Fully associative Cache

Cache 3 2 Way Set Associative Cache Cache 4 4 Way Set Associative

Input=L-0,L-3,L-4,L-1,L-2,L-5,L-7,S-6,L-0,L-3,L-1,L-11,L-5,L-15,L-9,S-4,L-0,L-4,S-3,L-12

Include

i) One Screenshot of Cache Address Table showing the splitup of the address fields for each level of cache



Cache Comparison

1. Direct Mapped Cache[8]

HIT - MISS - || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	INDEX	OFFSET
3 bit	3 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0

2. Fully Associative Cache[8]

HIT - MISS - || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	OFFSET
6 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0

3. 2-Way Set Associative Cache[4]

HIT - MISS - || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	INDEX	OFFSET
4 bit	2 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0

4. 4-Way Set Associative Cache[2]

HIT - MISS - || ADD. RESOURCES 0 NAND

Instruction Breakdown

TAG	INDEX	OFFSET
5 bit	1 bit	0 bit

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0

ii) 2 Screenshots showing hit and miss rates for each cache level wrt the requests generated by the processor

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature: Keerthan P.V

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Section: 4E
Date: 12/04/2025