## Microprocessor and Computer Architecture Laboratory UE23CS251B

#### 4th Semester, Academic Year 2024-25

Date:12/04/2025

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Week#9	Exercise:1	

1. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag.

Randomly generate 10 addresses and find hit rate and miss rate.

Include One Screenshot(for Write Back Cache) with

- i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor
- ii) Screenshot showing the Cache Table
- iii) Screenshot showing hit and miss rates

Replacement Policies	Random	₹ 2-WAY SET ASSOCIATIVE CACHE												
Vrite Policies	Random	◆ Instruction Breakdown					• Mem	■ Memory Block						
Write Back		0010 10100 10000111					B 54W 0 B 54W 1 B 54W 2 B 54W 3 B 54W 4 B 54W 5 B 54W 6 B 54W 7 B 54W 8 B 54W 9 B 54W A B 54W B B							
(	Write Through		4 bit	-	5 bit	10000111					V.5 B.55 W.6 B.55 W.7 B.55 W.8 B.55 V.5 B.55 W.6 B.55 W.7 B.55 W.8 B.55			
Write On Allocate	O Write Around		4 DIL		5 DIL	8 Dil		W.1 B.56 W.2 B.	56 W. 3 B.	56 W. 4 B. 56 V	V.5 B.56 W.6 B.56 W.7 B.56 W.8 B.56 V.5 B.57 W.6 B.57 W.7 B.57 W.8 B.57	W.9 B.56W.A B.56W.B W.9 B.57W.A B.57W.B		
ache Size (power of 2)	16384										1.2 8 25 W 6 8 37 W 7 8 25 W 6 8 31			
Memory Size (power of 2) 131072			MATANA SELECTIONS											
		⊞ Cache Table												
Offset Bits	8	Index	Valid	Tag	Data (	Hex)	Dirty Bit	Index	Valid	Tag	Data (Hex)	Dirty Bit		
Reset	Submit	0	1	3	B. 60 W.	0 - 255	0	0	0		0	0		
2,10,171		1	0		0		0	1	0	-	0	0		
Instruction	A2 0	2	0	1 -	0		0	2	0		0	0		
Load V (in hex)#		3	0	. 2	0		0	3	0	-	0	0		
List of next 10 Instructions		4	0	- 26	0		0	4	0.		0	0		
List of next 10 instructions		5	0		0		0	5	0	-	0	0		
	Submit	6	- 1	. 1	B. 26 W.	0 - 255	0	6	0	-	0	0		
	- As	7	0	. 9	0		0	7	0		0	0		
nformation		8	0	100	0		0	8	0		0	0		
The cycle ha	s been completed.	9	1	0	B. 9 W. I	- 255	0	9	0	-	0	0		
Please submit	t another instructions	10	0	12	0		0	10	0	2.5	0	0		
		11	0	-	.0		0	11	0	*	0	0		
		12	0		0		0	12	0	-	0	0		
		13	0	3	0		0	13	0	-	0	0		
Next	Fast Forward	14	0		0		0	14	0	- 1	0	0		
0.00000	100000000000000000000000000000000000000	15	0	35	0		0	15	0		0	0		
Statistics		16	0		0		0	16	0	-	0	0		
Hit Rate :	10%	17	0		0		0	17	0		0	0		
Miss Rate :	90%	18	1	C	B. 192 W.		0	18	0		0	0		
ist of Previous Instructions :		19	- 1	1	B. 33 W.		0	19	0	-	0	0		
<ul> <li>Load 60F3 [Miss]</li> </ul>		20	1	2	B. 54 W.		0	20	0		0	0		
<ul> <li>Load 33F3 [Miss]</li> </ul>		21	1	4	B. 95 W.		0	21	0	- 2	0	0		
<ul> <li>Load 95E7 [Miss]</li> <li>Load DBF2 [Miss]</li> </ul>		22	0	-	0		0	22	0	-	0	0		
Load 2670 [Miss]		23	0		0		0	23	0	-	0	0		
<ul> <li>Load 33C5 [Hit]</li> </ul>		24	0		0		0	24	0	-	0	0		
<ul> <li>Load 7D65 [Miss]</li> </ul>		25	0	196	0		.0	25	0	-	0	0		
<ul> <li>Load 192C2 [Miss]</li> <li>Load 9F7 [Miss]</li> </ul>		26	0	-	0		0	26	0	-	0	0		
Load 9F7 [Miss]     Load 5487 [Miss]		27	- 1	6	B. DB W.		0	27	0		0	0		
		28	0	-	0		0	28	0	- 1	0	0		
		29	1	3	B. 7D W.	0 - 255	0	29	0	-	0	0		

Week#	9	Exercise:	2

2. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

Consider a main memory having 64-byte capacity and cache memory of 8 bytes initially empty

The following addresses are generated by the CPU. All values in hexadecimal

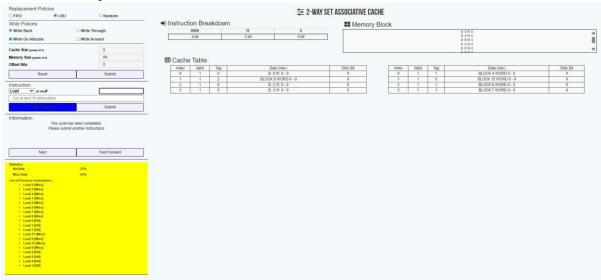
Clearly label data that is replaced in cache lines. Show the cache memory table and filled data in the cache lines of block size 1 byte. LRU Policy is used. The cache is mapped as a)Two way set Associative b)Four Way Set associative

Include Two Screenshots, one for Two way Set Associative(for Write Back Cache), One for four way Set Associative (for Write

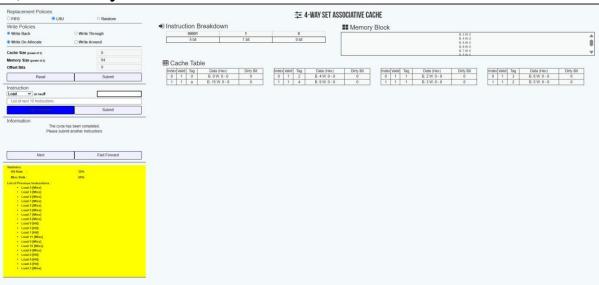
#### Back Cache) with

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor ii) Screenshot showing the Cache Table iii) Screenshot showing hit and miss rates





#### b)Four Way Set associative



Week#	9	Exercise:	3

3. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

Consider 2 way set associative mapping with following design: cache memory is 16 bytes and main memory is 256 bytes. The offset bits is 2 . calculate the hit ratio and miss ratio for the following sequence:

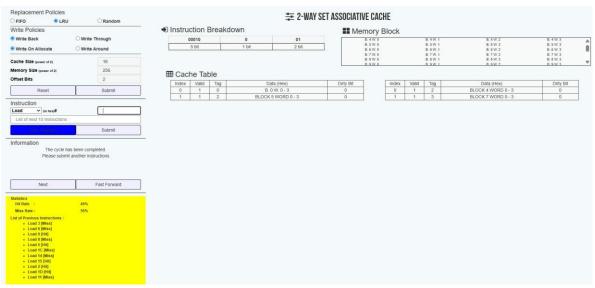
3,6,0,8,5,1C,14,15,2,1D,11

Use LRU and FIFO as replacement policy

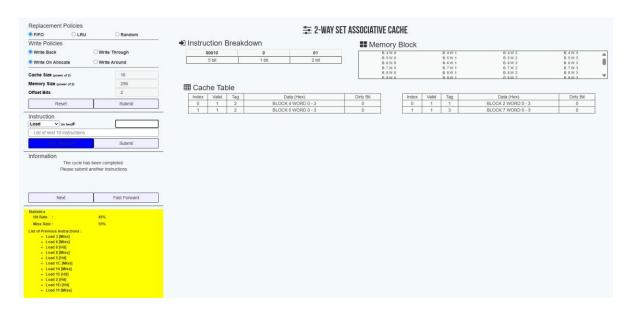
Include Two Screenshots(for LRU with Write Back Cache, FIFO with Write Back cache) with

- i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor
- ii) Screenshot showing the Cache Table
- iii) Screenshot showing hit and miss rates

a) LRU with Write Back Cache:



b) FIFO with Write Back Cache:



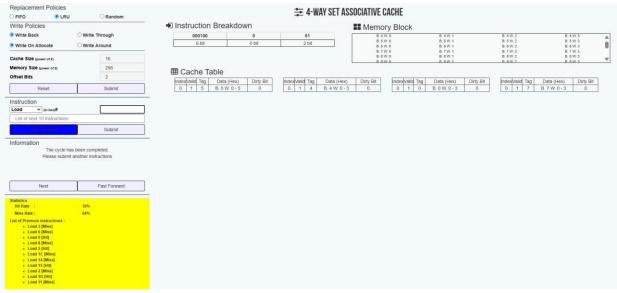
4.Use PARACACHE SIMULATOR for the exercise below given the following configuration .

Consider 4 way set associative mapping with following design: cache memory is 16bytes and main memory is 256 bytes. The offset bits is 2 . calculate the hit ratio and miss ratio for the following sequence:

Use replacement algorithm as LRU and FIFO.

Include Two Screenshots(LRU with Write Back Cache, FIFO with Write Back cache)

- i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor
- ii) Screenshot showing the Cache Table
- iii) Screenshot showing hit and miss rates
- a) LRU with Write Back Cache:



#### b) FIFO with Write Back Cache:

● FIFO ○ LRU	○ Random			₹ 4-WAY SET AS	SOCIATIVE CACHE			
Write Policies		◆ Instruction Breakdown	n		<b>SE</b> Memory Block			
<ul> <li>Write Back</li> </ul>	○ Write Through	000100	0	01	B.4W.0	8.4W.1	B. 4 W. 2	B.4W.3
<ul> <li>Write On Allocate</li> </ul>	O Write Around	6 bit	0 bit	2 bit	B. 5 W. 0 B. 6 W. 0	B. 5 W. 1 B. 6 W. 1	B. 5 W. 2 B. 6 W. 2	B. 5 W. 3 B. 6 W. 3
Cache Size (power of 2)	16				8.7 W.0 8.8 W.0 8.9 W.0	8.7 W.1 8.8 W.1 8.9 W.1	B. 7 W. 2 B. 8 W. 2 B. 9 W. 2	B.7 W.3 B.6 W.3 B.9 W.3
Memory Size (power of 2)	256				L RAWS	N. W. Y.	B NW 2	H WW J
Offset Bits	2	■ Cache Table			Telegraph Called		L. Luda I	
Reset	Submit	Index Valid Tag		Valid Tag Data (Hex) 1 0 B. 0 W. 0 - 3	Dirty Bit IndexValid 0 0 1	Tag Data (Hex) Dirty Bit 4 B. 4 W. 0 - 3 0	0 1 7	Data (Hex) Dirty Bit B. 7 W. 0 - 3 0
Instruction Load   Gin bex)#								
List of next 10 Instructions								
Est of Heat To Histocoons								
Tech veneration	Submit							
	s been completed.							
The cycle ha	is been completed. another instructions Fast Forward							
The cycle has Please submit	another instructions Fast Forward							
The cycle has Please submit	another instructions							

Week#\_\_\_\_9\_\_\_ Exercise: \_\_\_\_5\_\_

5.Use PARACACHE SIMULATOR for the exercise for the following configuration .(Cache Analysis)

Problem 1)Consider the following Design

FIFO, Write Back, Write Allocate

Main Memory= 128 Offset/word=3 Cache size(Each)= 32

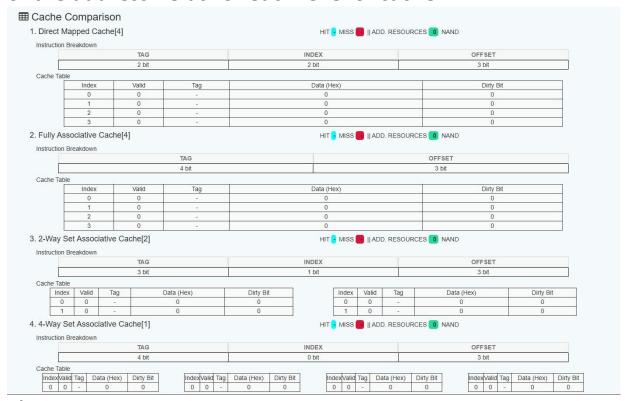
Cache 1 Direct Mapped Cache Cache 2 Fully associative Cache

Cache 3 2 Way Set Associative Cache Cache 4 4 Way Set Associative List of Instructions

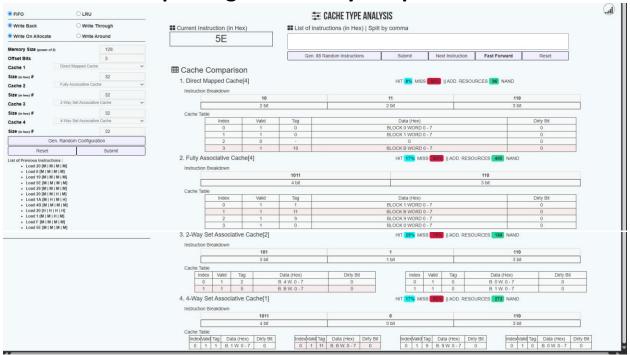
Input L-20,L-6,L-19,L-5E,L-29,L-20,L-1A,L-4B,L-20,L-1,L-F,L-5E

#### Include

### i) One Screenshot of Cache Address Table showing the splitup of the address fields for each level of cache



ii) 2 Screenshots showing hit and miss rates for each cache level wrt the requests generated by the processor



Week#\_\_\_\_9\_\_\_ Exercise: \_\_\_\_6\_\_

6. Try using PARACACHE SIMULATOR for the exercise for the following configuration .

Consider the following Design

FIFO, Write Back, Write Allocate

Main Memory= 2048 Offset/word=3 Cache size(Each)= 64

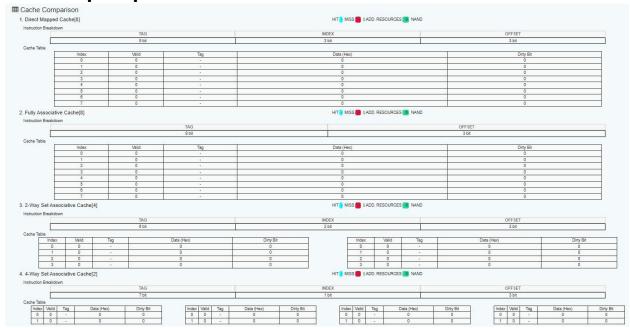
Cache 1 Direct Mapped Cache Cache 2 Fully associative Cache

Cache 3 2 Way Set Associative Cache Cache 4 4 Way Set Associative List of Instructions

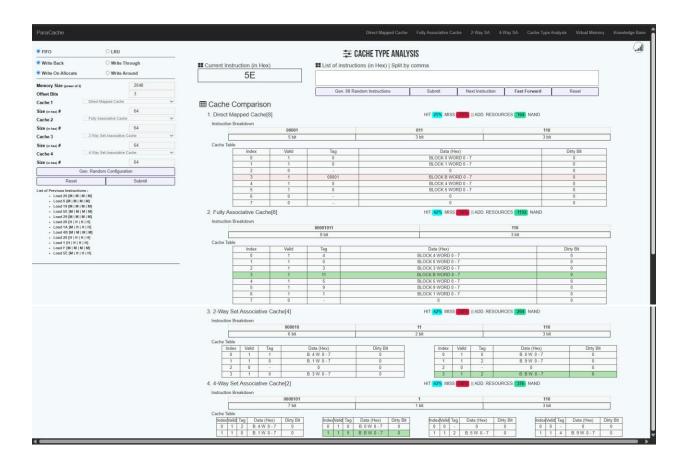
Input L-20,L-6,L-19,L-5E,L-29,L-20,L-1A,L-4B,L-20,L-1,L-F,L-5E

#### Include

i) One Screenshot of Cache Address Table showing the splitup of the address fields for each level of cache



# ii) 2 Screenshots showing hit and miss rates for each cache level wrt the requests generated by the processor



Week#\_\_\_\_\_9\_\_\_\_ Exercise: \_\_\_\_\_7\_\_

7. Use PARACACHE SIMULATOR for the exercise for the following configuration .Consider the following Design

FIFO, Write Back, Write Allocate

Main Memory= 2048 Offset/word=2

Cache size(Each)= 32

Cache 1 Direct Mapped Cache Cache 2 Fully associative Cache

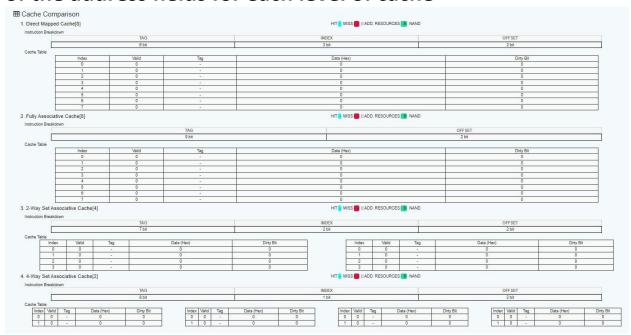
Cache 3 2 Way Set Associative Cache Cache 4 4 Way Set Associative

#### List of Instructions

Input L-20,L-6,L-19,L-5E,L-29,L-20,L-1A,L-4B,L-20,L-1,L-F,L-5E

#### Include

i) One Screenshot of Cache Address Table showing the splitup of the address fields for each level of cache



ii) 2 Screenshots showing hit and miss rates for each cache level wrt the requests generated by the processor

FIFO	OLRU	_		<b>‡</b>	CACHE TYPE ANALY	'SIS			
Write Back	O Write Through	Current Instruction (	■ List of instructions (in Hex)   Split by comma						
Write On Allocate	○ Write Around	5E							
emory Size (power of 2)	2048								
fset Bits	2			Gen. 88	Random Instructions	Submit Ne:	xt Instruction	Fast Forward	Reset
nche 1 Direct M	apped Cache		rison						
ZO (in hex) #	32	Direct Mapped C				HIT 33% MISS MISS	IANN DESCUID	CES TES NAND	
nche 2 Fully Ass	ociative Cache	Instruction Breakdown	Market Control			THE SAME MILES SHEET	II ADD. NEDOUN	CLO LINE HAND	
ZO (in hox) #	32	manucaum Greaksonn	000010			111		10	
iche 3 2-Way S	et Associative Cache		6 bit			3 bit		2 bit	
(in hex) III	32	Cache Table				Data (Hex)			01 - 01
ne 4	et Associative Cache 🕓	Inde 0		Tag 0		BLOCK 0 WORD 0	- 3		Dirty Bit 0
(in hex) #	32	1	1	0		BLOCK 1 WORD 0	- 3		0
Gen. Rando	m Configuration	2	1 1	000010		BLOCK 12 WORD 0			0
Reset	Submit	] 3		0		BLOCK 3 WORD 0	- 3		0
of Previous Instructions :	-00:	5	0	-		0			0
<ul> <li>Load 20 [M   M   M   M]</li> <li>Load 6 [M   M   M   M]</li> </ul>		6	1	000010		BLOCK 6 WORD 0 BLOCK 17 WORD 0			0
- Load 19 [M   M   M   M]				000010					0
<ul> <li>Load 5E [M   M   M   M]</li> <li>Load 29 [M   M   M   M]</li> </ul>		<ol><li>Fully Associative</li></ol>				HIT 33% MISS MAN	ADD. RESOUR	CES 1440 NAND	
<ul> <li>Load 20 [H   H   H   H]</li> <li>Load 1A [H   H   H   H]</li> </ul>		Instruction Breakdown		000010111				10	
- Load 4B [M   M   M   M]		<u> </u>		9 bit		-		2 bit	
<ul> <li>Load 20 [H   H   H   H]</li> <li>Load 1 [M   M   M   M]</li> </ul>		Cache Table		7.70					
- Load F [M   M   M   M] - Load 5E [H   H   H   H]		Inde		Tag		Data (Hex)		8	Dirty Bit
· rosmacfulululul		0	1	8		BLOCK 8 WORD 0 - 3 BLOCK 1 WORD 0 - 3			0
		- 1	1 1	6		BLOCK 6 WORD 0 - 3			0
		3	1	23		BLOCK 17 WORD 0 - 3			0
		4 5	1 1	10		BLOCK A WORD 0 - 3 BLOCK 12 WORD 0 - 3			0
		5		0		BLOCK 0 WORD 0 - 3			0
		7	1	3		BLOCK 3 WORD 0 - 3			0
		3. 2-Way Set Assoc	ciative Cache[4]			HIT 33% MISS 66/50	I ADD RESOUR	CES 272 NAND	
		Instruction Breakdown						00 00 00 00 00 00 00 00 00 00 00 00 00	
		monagem Dronkoviii	0000101			11		10	
			7 bit			2 bit		2 bit	
		Cache Table			Dia 20	C Lwn I	-	2 - 2 -	Dia Bi
		Index Valid	Tag 2	Data (Hex) B. 8 W. 0 - 3	Dirty Bit	Index Valid	Tag 0	Data (Hex) B. 0 W. 0 - 3	Dirty Bit
		1 1	0	B. 1 W. 0 - 3	0	1 0	-	0	0
		2 1	4	B. 12 W. 0 - 3	0	2 1	2	B. A.W. 0 - 3	0
		3 1	5	B. 17 W. 0 - 3	0	3 1	0	B. 3 W. 0 - 3	0
		4. 4-Way Set Assoc				HIT 33% MISS 667%	ADD RESOUR	CES 416 NAND	
		Instruction Breakdown				1		46	
			00001011 8 bit			1 bit		10 2 bit	
			- U.M.				_	2.00	
		Cache Table							

Week#\_\_\_\_9\_\_\_ Exercise: \_\_\_\_8\_\_

Try using PARACACHE SIMULATOR for the exercise for the following configuration .Consider the following Design

FIFO, Write Back, Write Allocate

Memory size: 64 Offset:0 Cache size:8

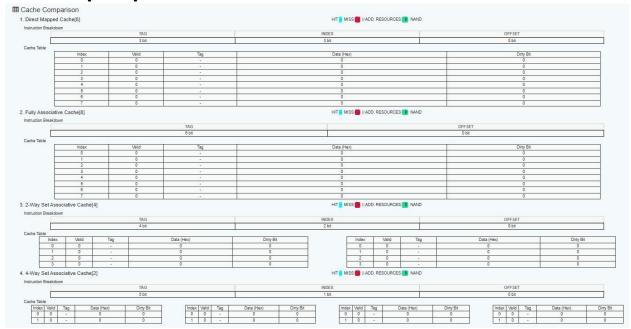
Cache 1 Direct Mapped Cache Cache 2 Fully associative Cache

Cache 3 2 Way Set Associative Cache Cache 4 4 Way Set Associative

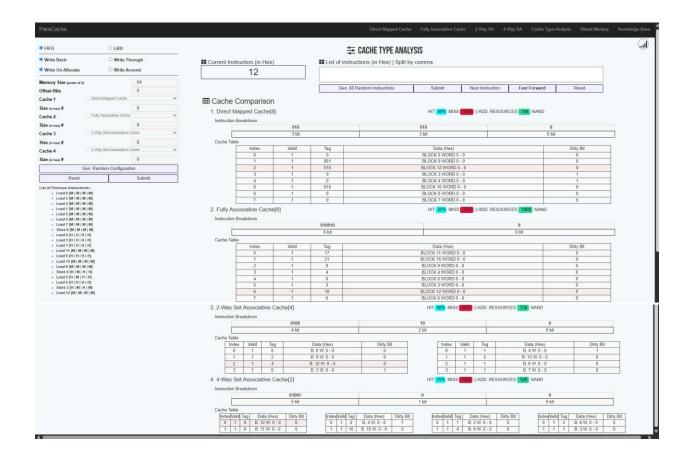
Input=L-0,L-3,L-4,L-1,L-2,L-5,L-7,S-6,L-0,L-3,L-1,L-11,L-5,L-15,L-9,S-4,L-0,L-4,S-3,L-12

#### Include

i) One Screenshot of Cache Address Table showing the splitup of the address fields for each level of cache



ii) 2 Screenshots showing hit and miss rates for each cache level wrt the requests generated by the processor



#### **Disclaimer:**

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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