Microprocessor and Computer Architecture Laboratory

UE23CS251B

4th Semester, Academic Year 2024-25

Date: 29/03/2025

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Week#____8_____ Exercise: ____1__

1. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

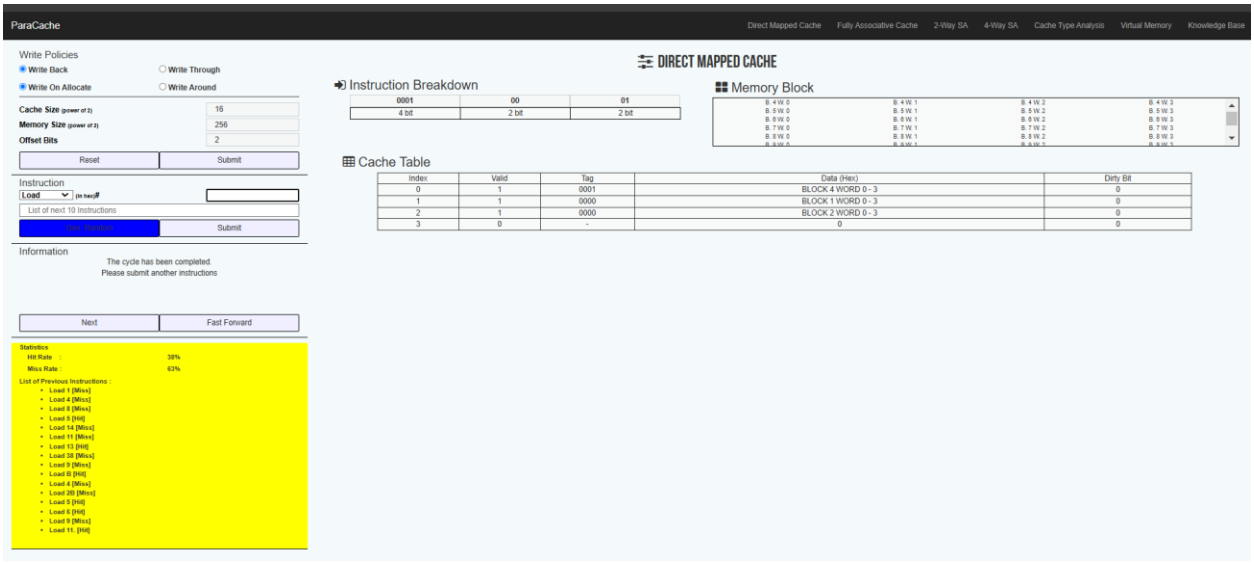
Consider a direct mapped cache of size 16 bytes with block size 4 bytes. The size of main memory is 256 bytes. Find Number of bits in tag, index and offset.

The processor generates requests as follows

1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11.

Find hit rate and miss rate.

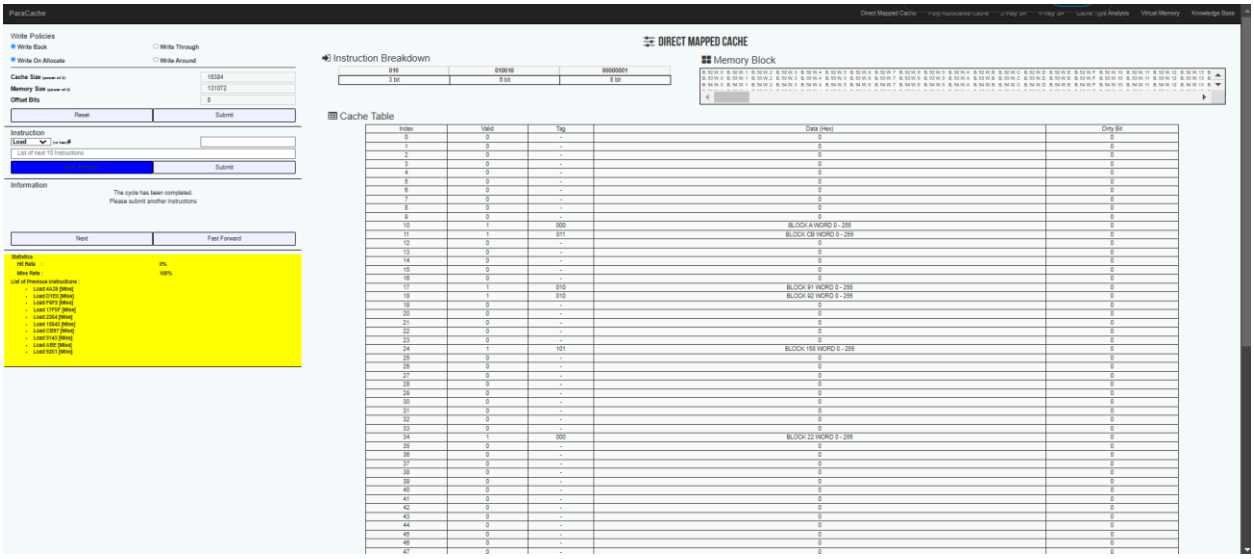
Include One Screenshot(for Write Back Cache) with
i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor
ii) Screenshot showing the Cache Table
iii) Screenshot showing hit and miss rates



2. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

Include One Screenshot(for Write Back Cache) with
i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor
ii) Screenshot showing the Cache Table
iii) Screenshot showing hit and miss rates

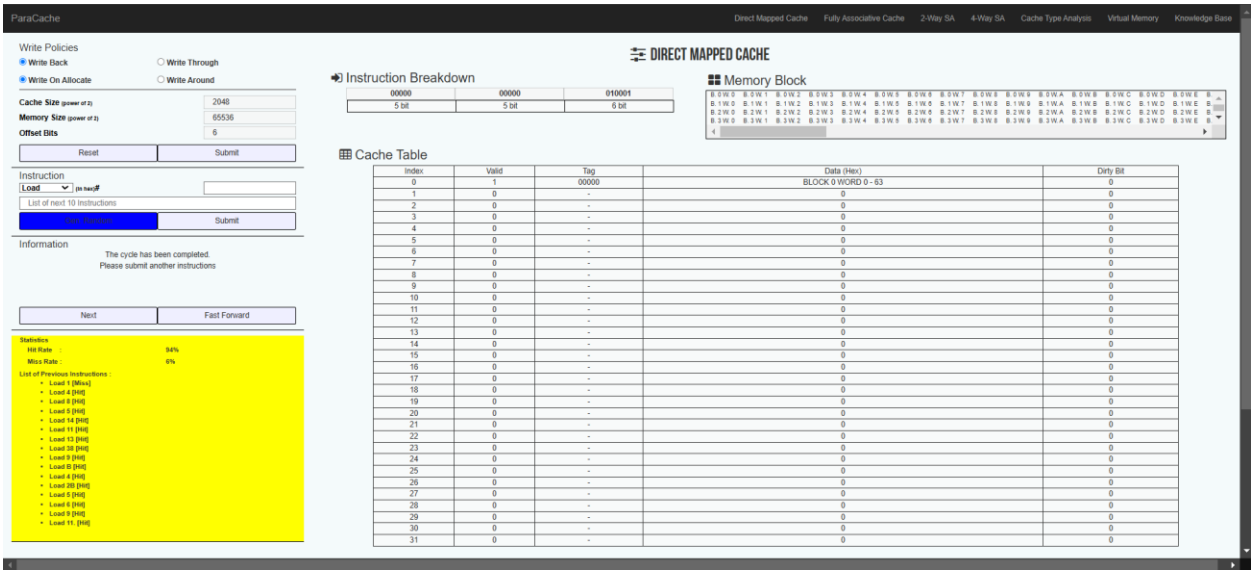


Week#____8_____ Exercise: ____3_

3. Use PARACACHE SIMULATOR for the exercise below given the following configuration .

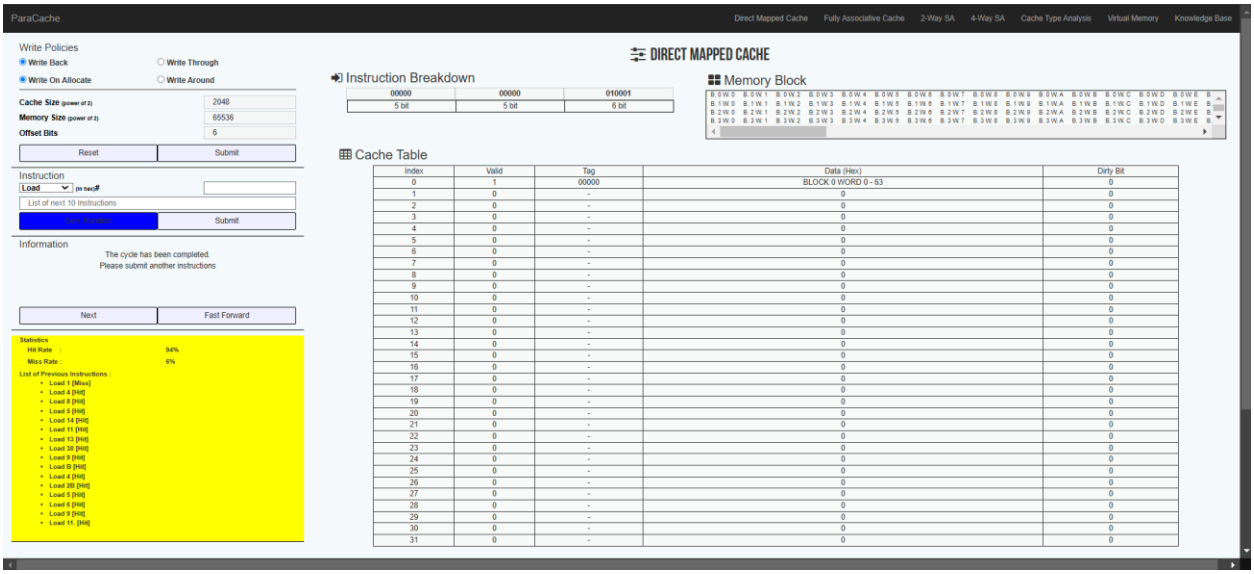
A computer system uses 16-bit memory addresses. It has a 2K-byte cache(Write Back) organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.(One Screenshot)



(b) When a program is executed, the processor reads data sequentially from the following word addresses: .(One Screenshot)

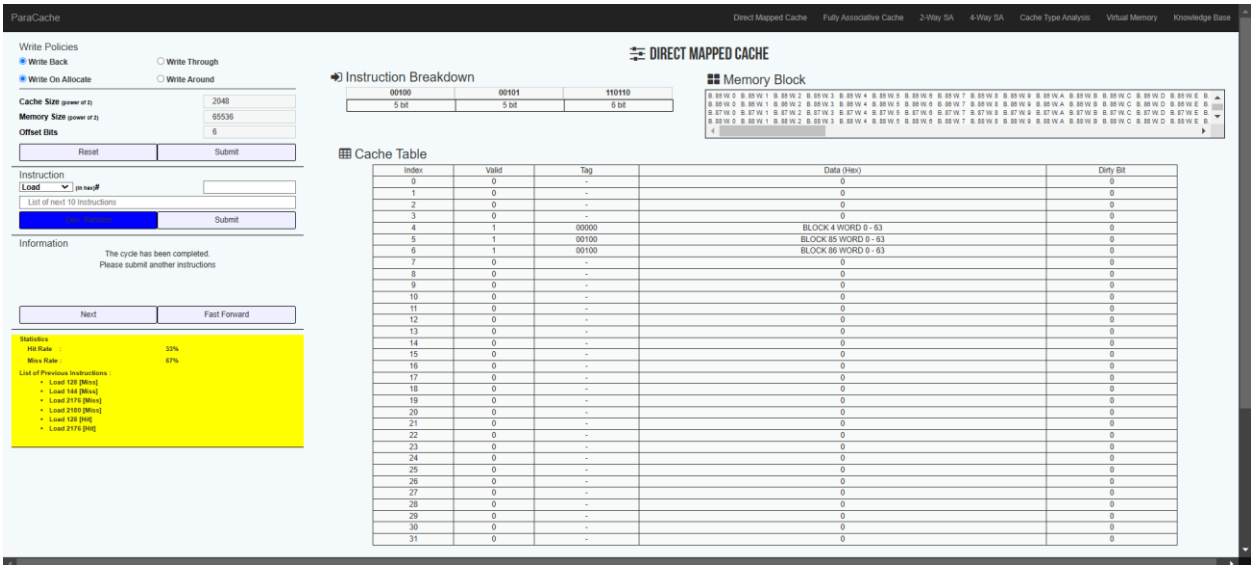
1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11.



(c)When a program is executed, the processor reads data sequentially from the following word addresses: .(One Screenshot)

128, 144, 2176, 2180, 128, 2176

All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.



Week#____8_____ Exercise: ____4_

4.Use PARACACHE SIMULATOR for the exercise below given the following configuration .

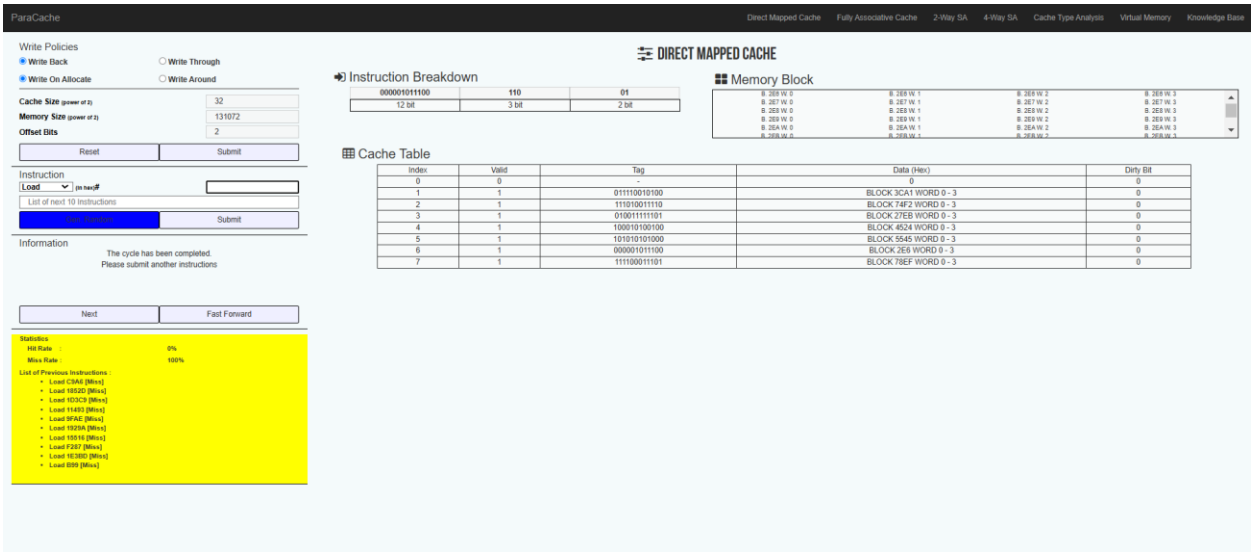
a. Direct Mapped Cache Size: 32 words
b. Memory Size: 131072 words[main memory].
c. Block Size: 4 words.
   Use Write back policy
   Also, repeat the exercise for Write through policy.

Include One Screenshot(for Write Back Cache) with
i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor
ii) Screenshot showing the Cache Table
iii) Screenshot showing hit and miss rates

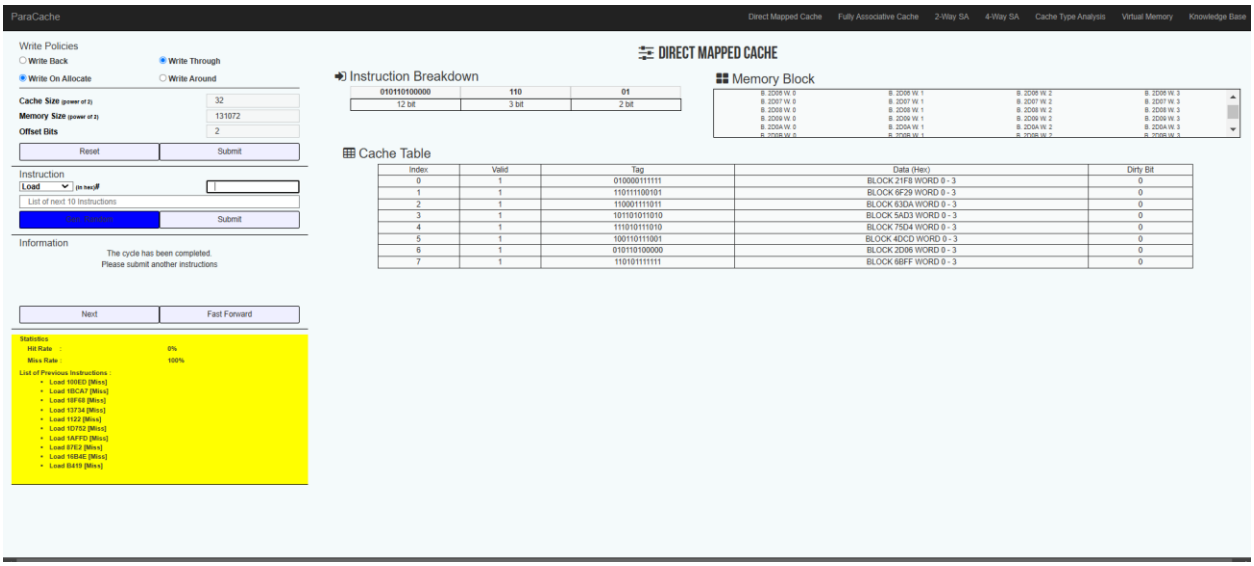
Include One Screenshot(for Write Through Cache) with
i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

ii) Screenshot showing the Cache Table
iii) Screenshot showing hit and miss rates

a.Write back cache



b.Write through cache



Week#____8_____ Exercise: ____5__

5.Try using PARACACHE SIMULATOR for the exercise for the following configuration .

Cache Size(Direct Mapped): 32 words

Memory Size: 16-bit memory address

Block Size: 16 words.

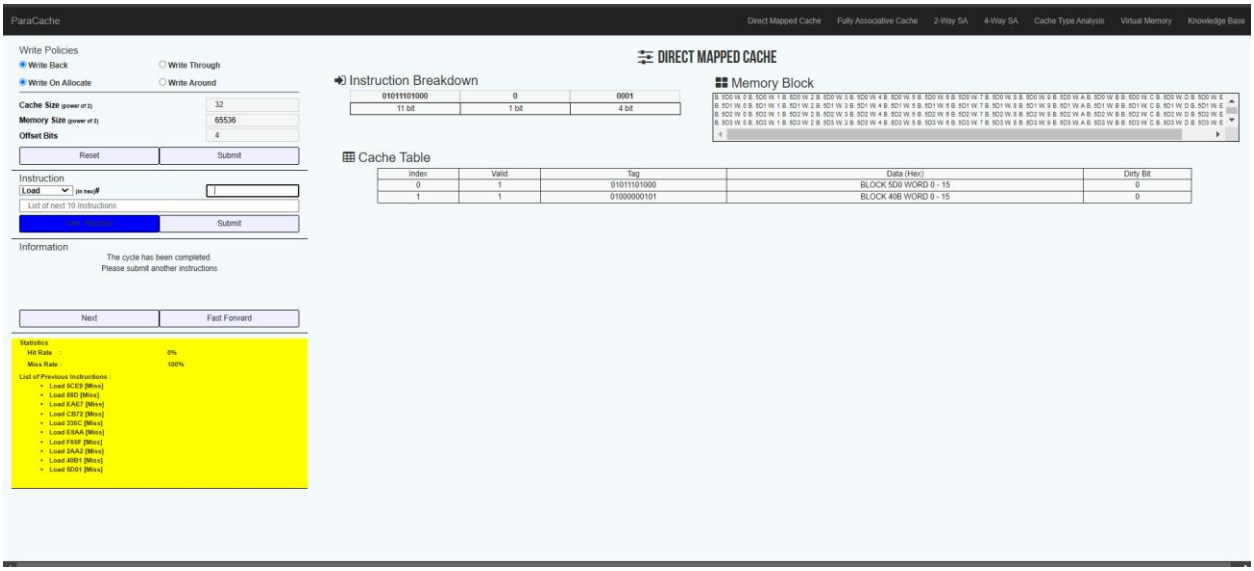
Use Write back policy

Also, repeat the exercise for Write through policy.

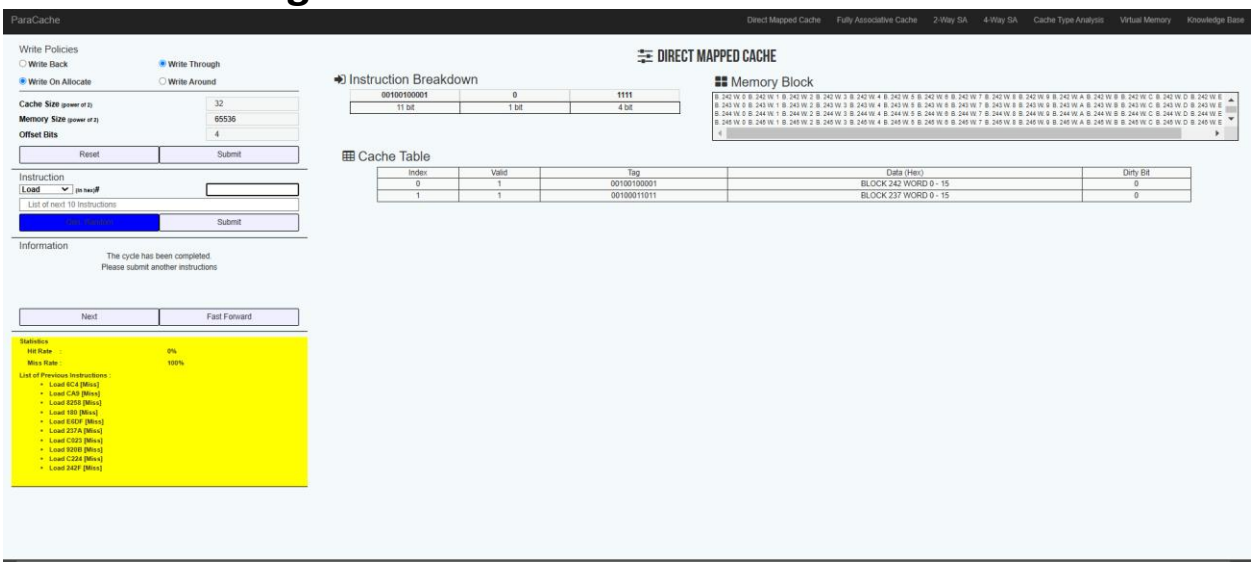
Include One Screenshot for each case with

i) Cache Address Table showing the splitup of the address fields for the requests generated by the processor
ii) Screenshot showing the Cache Table
iii) Screenshot showing hit and miss rates

a.Write Back cache



b. write Through cache



Week#____8_____ Exercise: ____6__

6. Try using PARACACHE SIMULATOR for the exercise for the following configuration .

Consider a fully associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find number of tag bits.

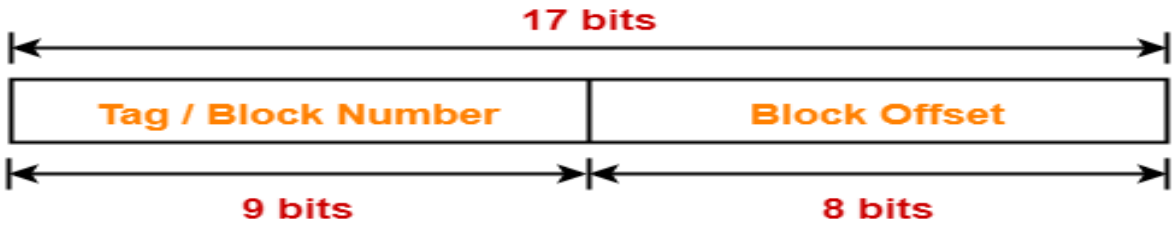
a)Use LRU replacement policy calculate the hit ratio and miss ratio for the following sequence:

0,1,2,3,4,5,6,7,0,1,2,8,10,15,15,12

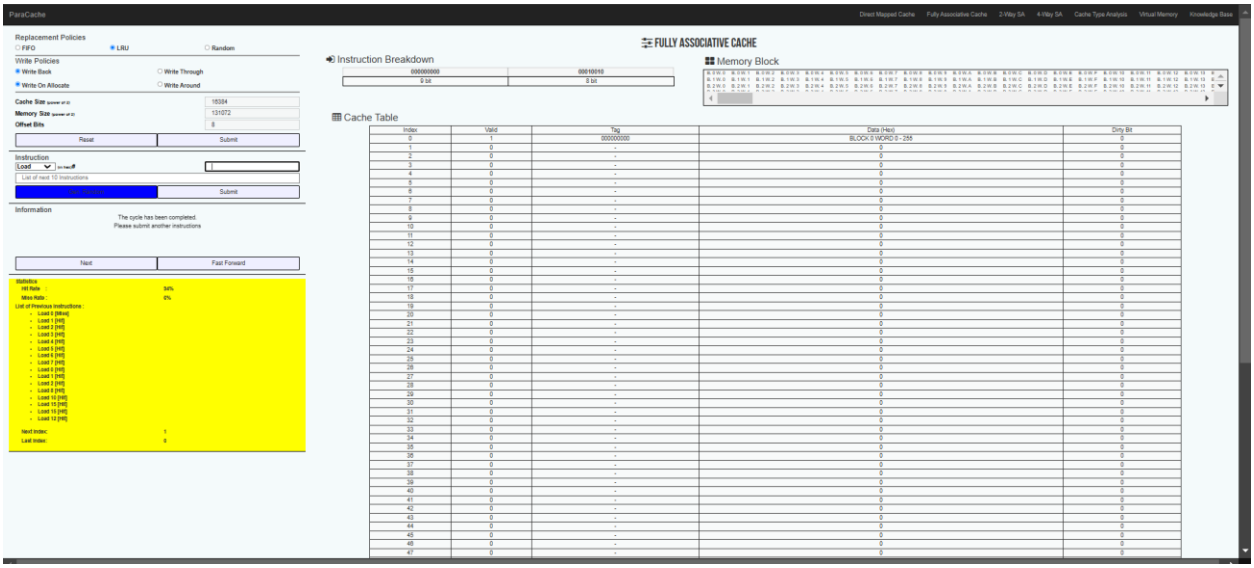
b)Use FIFO replacement policy calculate the hit ratio and miss ratio for the following sequence:

0,1,2,3,4,5,6,7,0,1,2,8,10,15,15,12

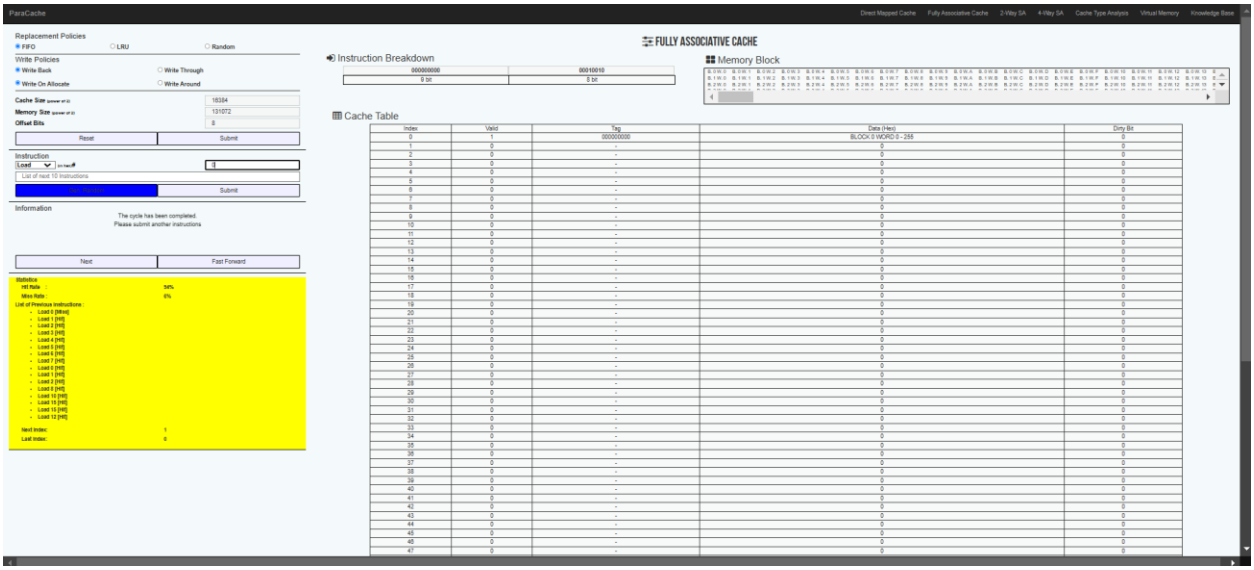
Solution



a.LRU Replacement Policy:



b.FIFO Replacement Policy:



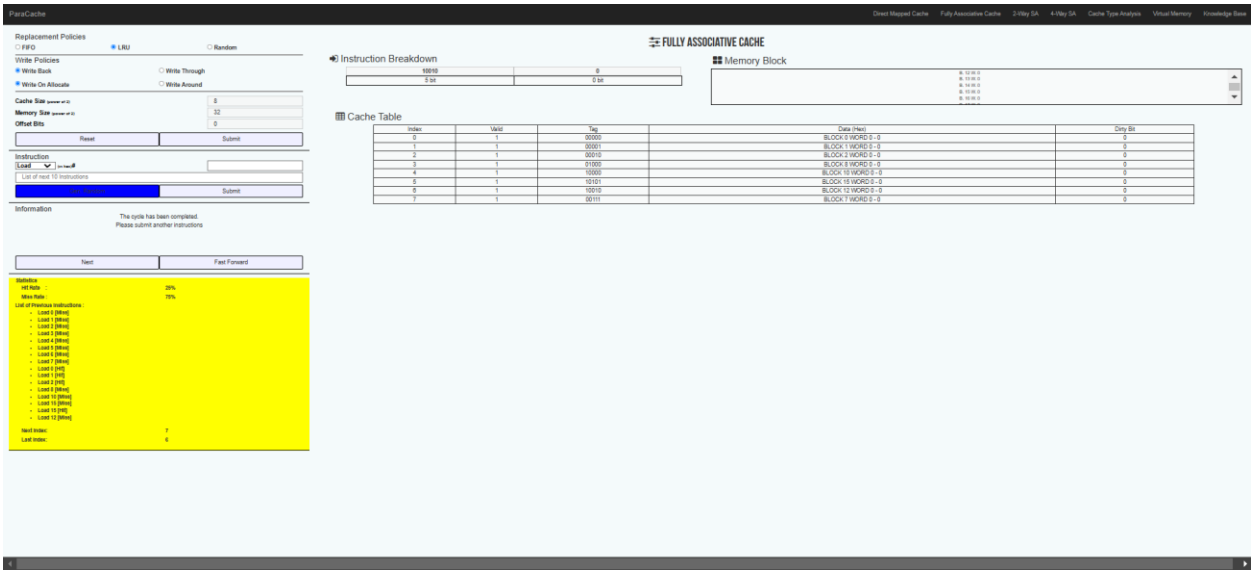
Week#____8_____ Exercise: ____7__

7. Try using PARACACHE SIMULATOR for the exercise for the following configuration .

Consider the following cache design: main memory having 32 bytes, cache memory of 8 bytes, block size is 1 byte. Use LRU replacement policy

Using fully associative cache calculate the hit ratio and miss ratio for the following sequence:

0,1,2,3,4,5,6,7,0,1,2,8,10,15,15,12



Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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