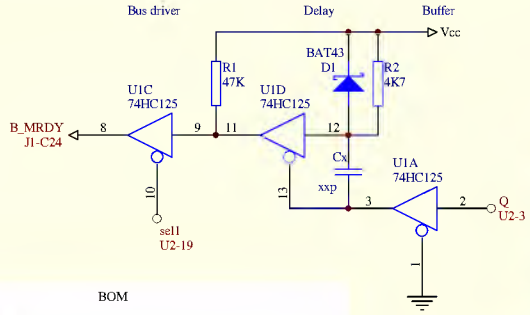
Timing:

5MHz bus FDC(2.5MHz) E=300nsec /E=100nsec

4MHz bus FDC(2MHz) E=375nsec /E=125nsec

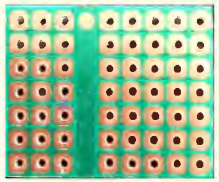


BOM

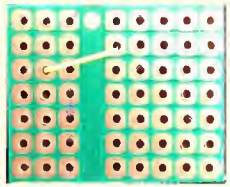
#	Device	Value	Package type	Refdes	
	RES 250W	47K 10%	RES12	R1	
	RES 125W	4K7 5%	RES12	R2	
	CER CAP	39p 5%	1206 SMD	Cx	5MHz bus
	CER CAP	56p 5%	1206 SMD	Cx	4MHz bus
	DIODE.SCHOTT	BAT43	DIO_DO35	D1	
	74HC125	74HC125	DIP14	U1	

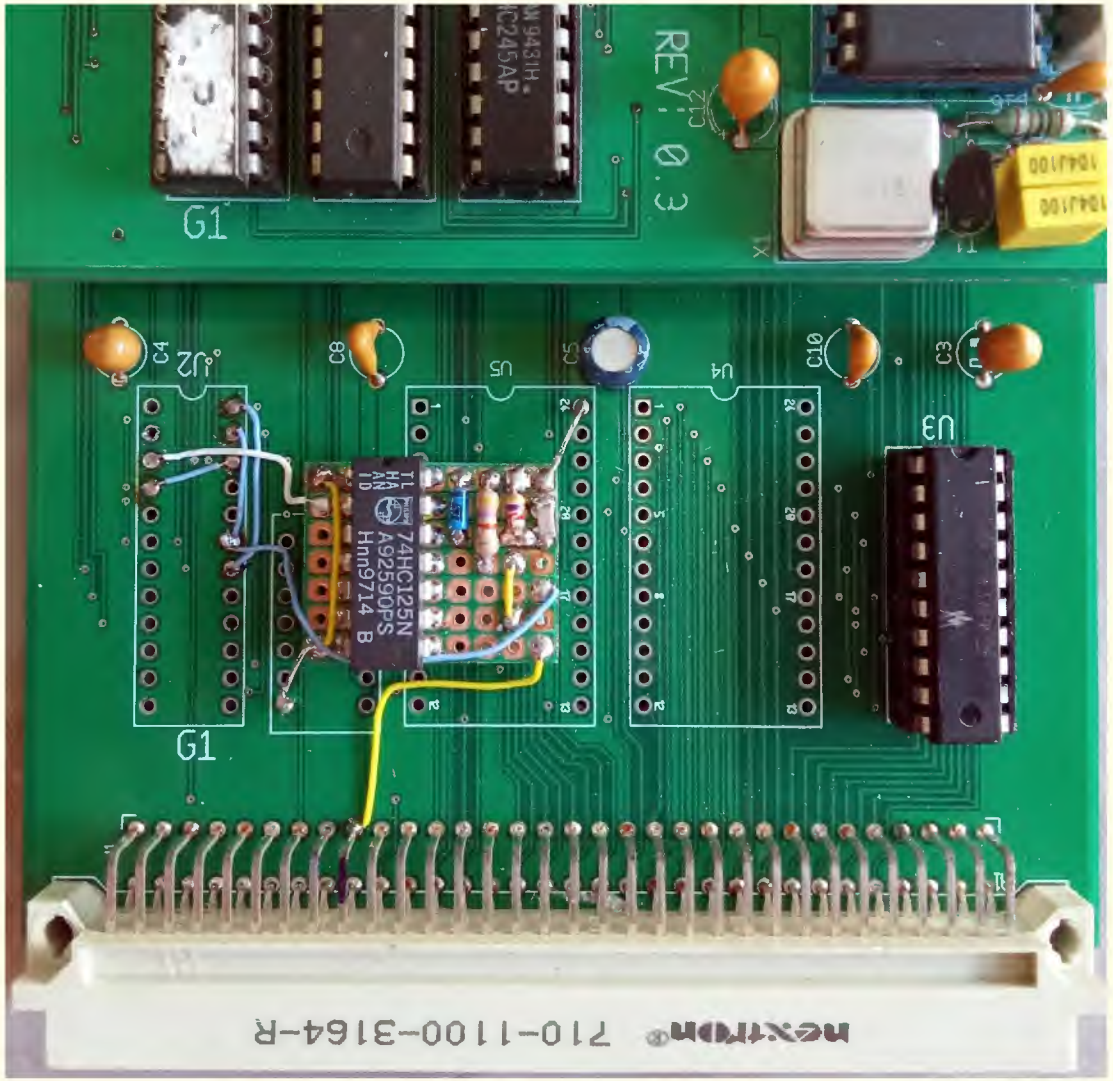
Solder all parts like SMD.

Print



Jumper





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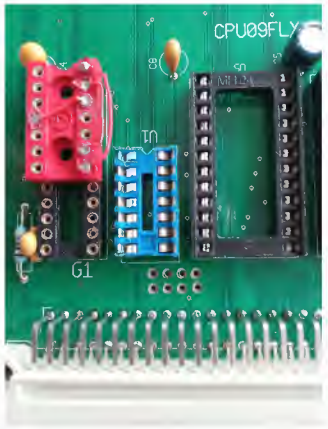
Date: 15-Dec-2025		Sheet of
File: C:\ISO\FLP_MRDY\FLP_MRDY.ddb		Drawn By:

Above show MRDY for 09FLP.
It will stretch E with 1 cycle.

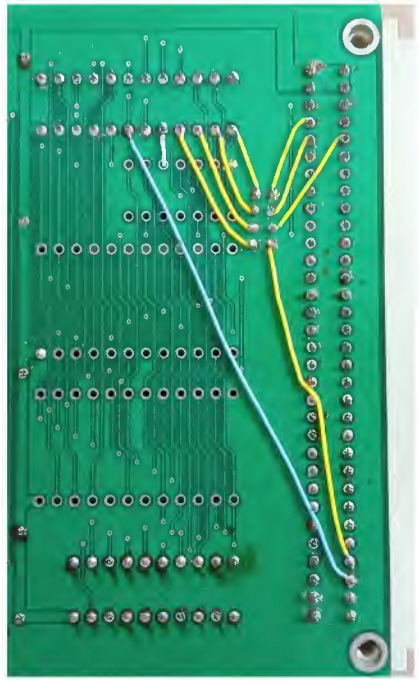
Below show MRDY option for all IO except CPU09RAM and CPU09ID6,
these two work fine on a 5MHz bus.
Also the option to use MRDY for the ACIA on the CPU09CMI, see "RUN CPU09CMI at 20Mhz.".
It will stretch E with ½ or 1 cycle depending on Cx.

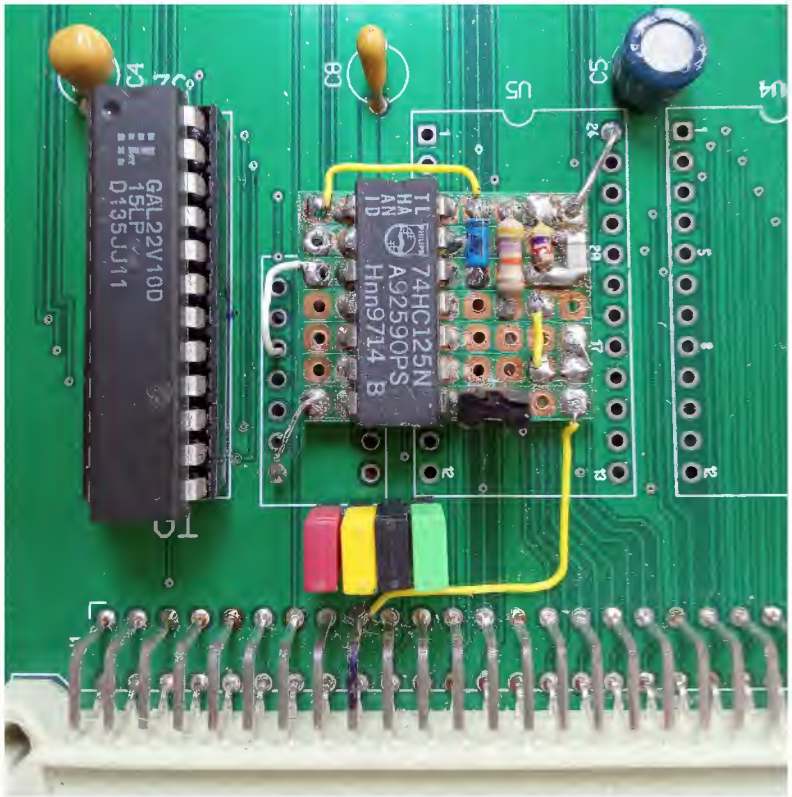
The ACIA, DIV3, DIV4, DIV7 are jumper selectable.



Drill 8 holes for the jumper block, remove ground >

and wire the FLXMIN_M >



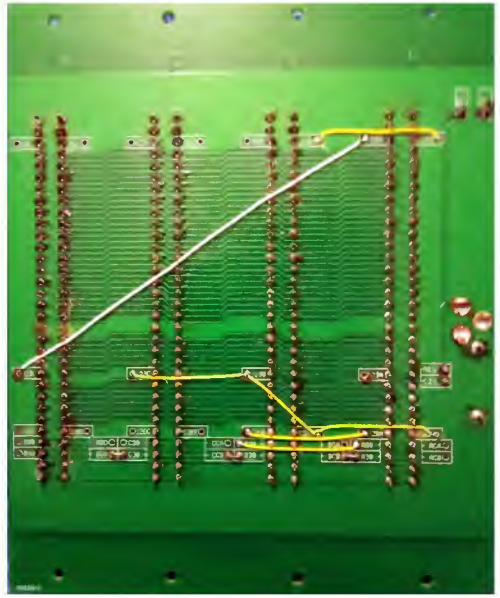


Use the print from before, but the wiring is different.

Select Cx for ½ or 1 cycle: 5MHz 27pF ½ cycle is fine
4MHz 47PF ½ cycle.
Use a GAL with internal pull-ups,
parts U1, U4, U5 may not be placed !

MDRY = On jumper

Backplane wiring >



Select for MRDY:
Red = M_ACIA with wire on CPU09CMI.
Yellow = DIV7
Black = DIV3
Green = DIV4 with DIV4 jumper on CPU09CMI.

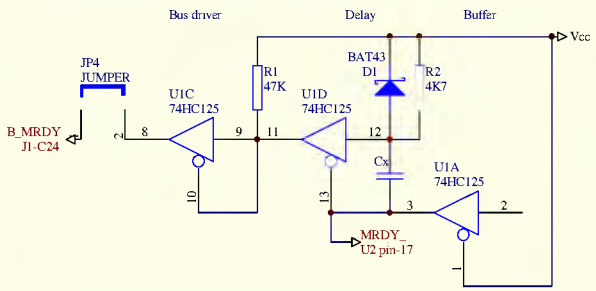
CdeJ

MRDY for MINFLX and ACIA on CPU09CMI
need G1 - FLX_2

Timing:

5MHz CPU bus Cx 27pF E=200nsec /E=100nsec FDC 3.3MHz

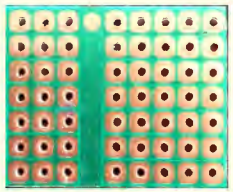
5MHz CPU bus Cx 47pF E=300nsec /E=100nsec FDC 2.5MHz)



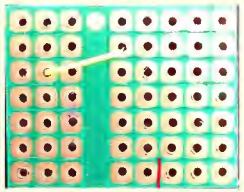
BOM

#	Device	Value	Package type	Refdes	
	RES 250W	47K 10%	RES12	R1	
	RES 125W	4K7 5%	RES12	R2	
	CER CAP	27p 5%	1206 SMD	Cx	bus 300nsec
	CER CAP	47p 5%	1206 SMD	Cx	bus 400nsec
	DIODE.SCHOTT	BAT43	DIO_DO35	D1	
	74HC125	74HC125	DIP14	U1	
	HDR1x2	HDR1x2	HDR1x2	J4	
	Solder all above parts like SMD.				
	GAL22V10	GAL22V10D	SDIP24	U2	
	HDR2x4	HDR2x4	HDR2x4	J3	

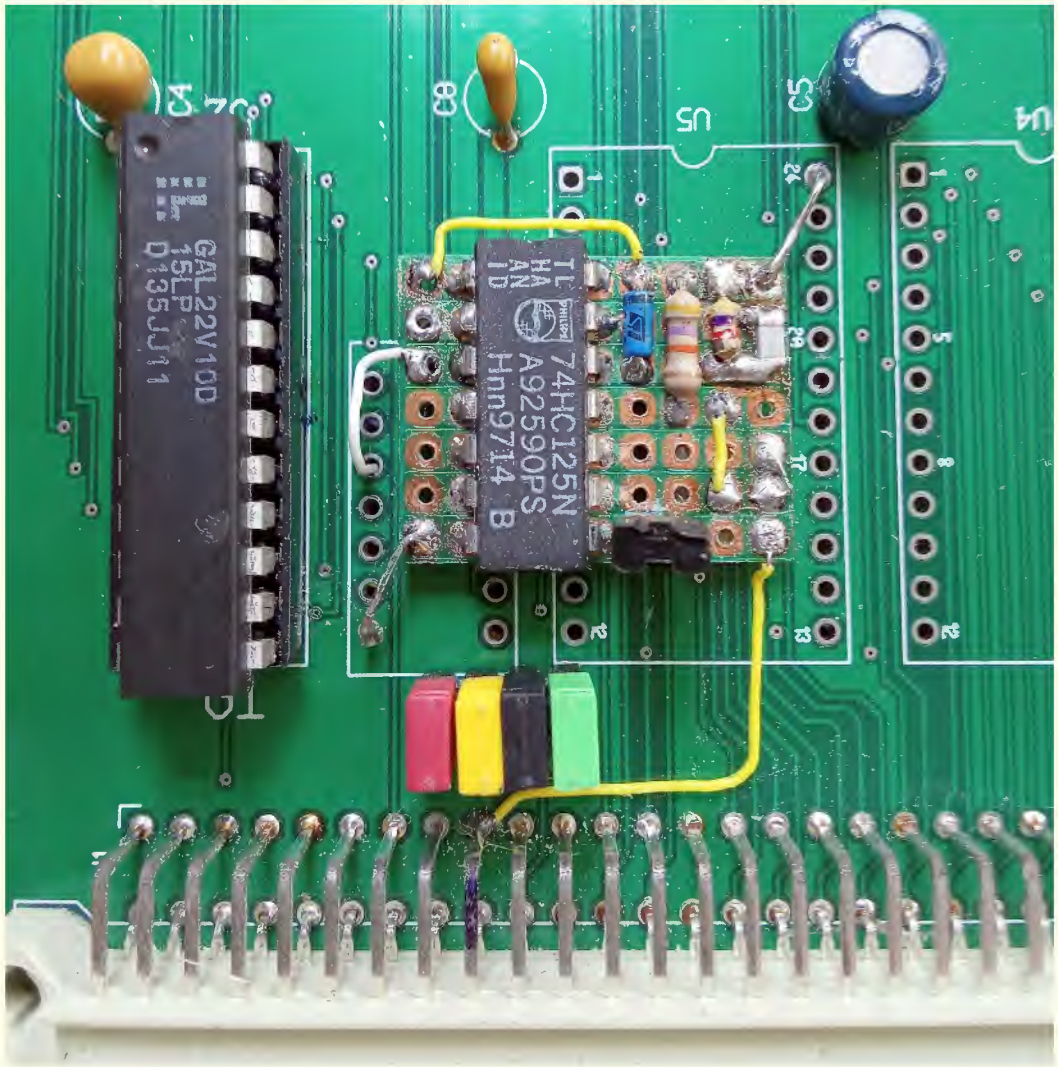
Print



Jumper



Cut



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