Chip stress test in the CPU09CMI

chip	Bus 2 MHz		Bus 3 MHz		Bus 4 MHz	
HD6350	20	0	20	0	20	0
HD63B50	40	0	40	0	40	0
MC6850	15	0	15	0	15	0
MC68B50	13	0	13	0	13	0
HD6809	6	X	6	X	6	X
HD68B09	1	X	1	X	1	X
MC6809	2	X	2	X	2	X
MC68B09	3	X	3	X	3	X
HD63C09	40	0	40	0	40	0
S6802	20	X	--	--	--	--
MC68B02	na	X	na	X	--	--
	Pcs	Fail	Pcs	Fail	Pcs	Fail

The ‘X’ means can not test them on this board because the different C1 and C2 values.
The ‘na’ means not in stock.
For all bus frequencies the PAL CMI-4_1 is used, which is using the Q clock.
All CPU’s are tested by running FLEX.

Remarkable even all the 1 MHz ACIA’s are working on the 16MHz CMI board.

CdeJ