Overview

The "Sump" Logic Analyzer supports 32 channels with 6K sample memory or 8 channels with 24K and runs up to 200MHz. The included Java client application allows waveform exploration as well as SPI and I2C protocol analysis. This project is synthesized for the Papilio One and shares the same code base as the Openbench Logic Sniffer project.

Features

- 6K sample memory at 32 channels, 24K sample memory at 8 channels
- 32 channels sampling at 100MHz
- 16 channels sampling at 200MHz
- Four stage serial and parallel triggering
- External clock input
- Noise filter
- RLE built into the hardware to make the most of available memory.
- SPI protocol analysis (SPI debugger)
- I2C protocol analysis (I2C debugger)
- UART protocol analysis (UART debugger)
- State Analysis

Limitations

- The FPGA can only sample 1.2V, 2.5V, and 3.3V. Any higher voltages can damage the input pins of the FPGA. Given time a plugin board will be developed to address this issue.

> NOTE: The current 2.12 release is based on the Openbench Logic Sniffer 2.12 source code. There are issues with RLE, test mode, and there are some failing timing constraints in the project. This release has not been well tested, it is being released while the new Verilog branch of the project is completed. The Verilog branch should fix all of the above issues and will be available soon.

Quick Start

Requirements

This project works with both the Papilio One 250K board and the Papilio One 500K board. The input channels are connected to Wing Slot A and Wing Slot C.

1.2V, 2.5V, and 3.3V signals can be sampled directly on Wing Slot A and C. Using a Input Buffer Wing allows 5V signals (up to 7V) to be sampled on either Wing

Optional Wings	Wing Slot
Input Buffer Wing	A
Input Buffer Wing	B

Downloads

Description	Link
Ready to run bitstream for the Papilio One 500K board. Version 2.12, use Papilio Loader to load the bitstream.	Sump_Logic_Analyzer_P1_500K.bit
Ready to run bitstream for the Papilio One 500K board. Version 2.12, use Papilio Loader to load the bitstream.	Sump_Logic_Analyzer_P1_250K.bit
Source code version 2.12. Use Xilinx ISE Webpack to open project.	Papilio_One_Sump_LA_VHDL_source_2.12.zip
Java Client - Download the latest client from Jawi's Alternate Client Homepage.	Jawi Client 0.9.2
Quick Start package, download this to get started without any fuss. A loader script and Jawi's client make this ready to go.	Papilio_One_Logic_Analyzer_QuickStart_2.12.zip

Current Status

2/4/2011 - Version 2.12 Released

Version 2.12 is based on the OpenBench Logic Sniffer branch of the "Sump" Logic Analyzer. The following new features are included:

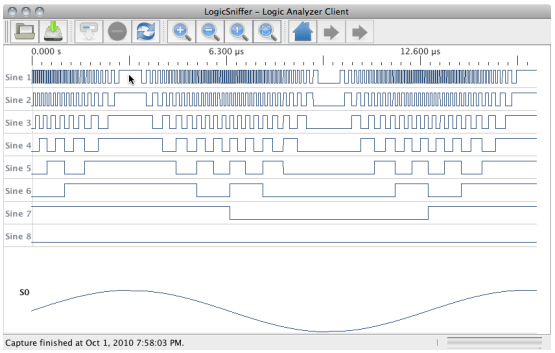
- Dynamic memory allows 24K of memory when 1 channel group is used and 6K of memory when 4 channel group is used.
- Switch row A with row C on the fly, change the "Inside" and "Outside" option in the Java client.
- Test Mode - (This feature is not working in 2.12)
- RLE - (This feature is not working in 2.12)

Sources and Attribution

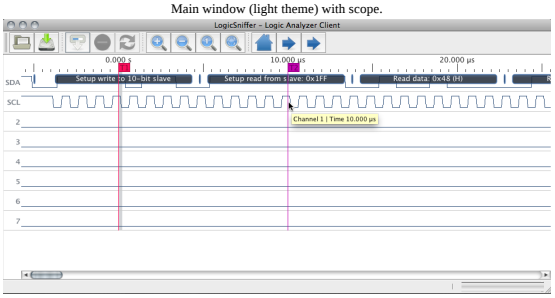
- Michael Poppitz was the original author of this great Logic Analyzer design. He wrote the original VHDL and Java client and released it GPL at http://www.sump.org/projects/analyzer/. Please visit his website for more information.

- The very latest development for the Java client is hosted on SourceForge here.
- OakMicros has created a very nice tutorial for the Java client here . They also offer a nice buffer card to allow any Voltage level to be sampled. It is not currently compatible with the Butterfly Platform but watch for an adapter in the future.

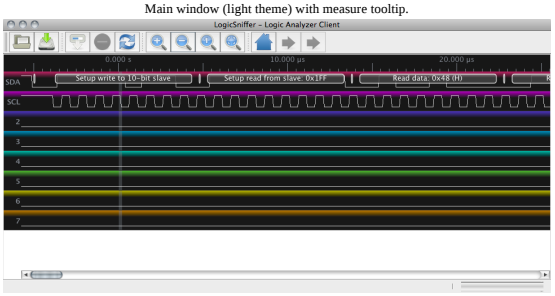
Screenshots



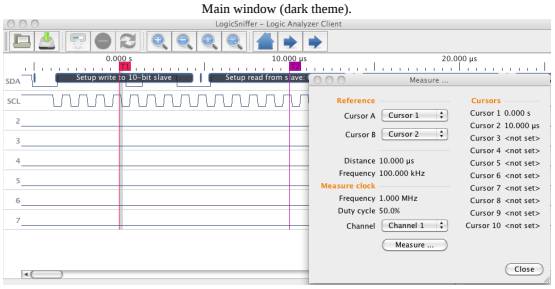
Main window (light theme) with scope.



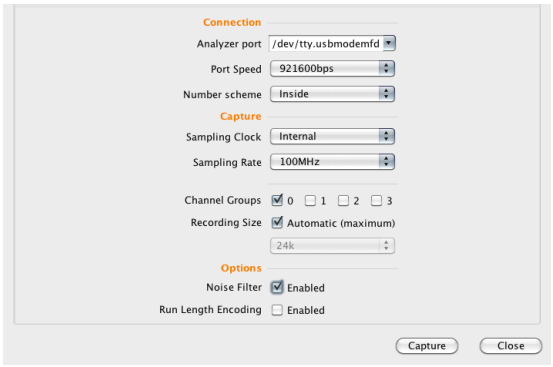
Main window (light theme) with measure tooltip.



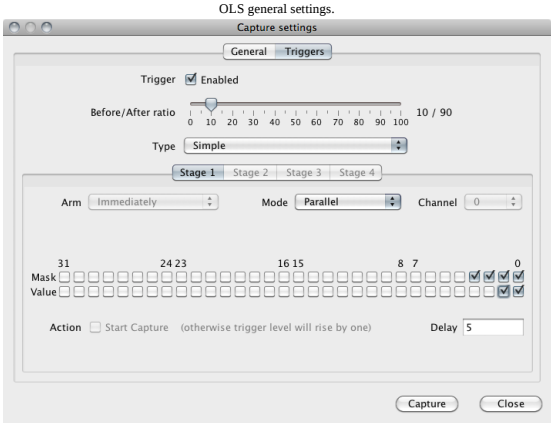
Main window (dark theme).



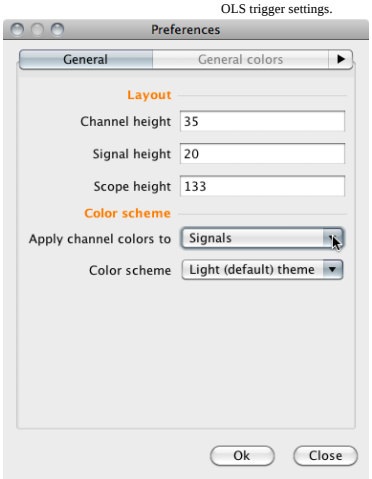
Measurement tool.



OLS general settings.



OLS trigger settings.



General preferences.