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 Nov 13, 2017
 Digital Logic Design
 Homework

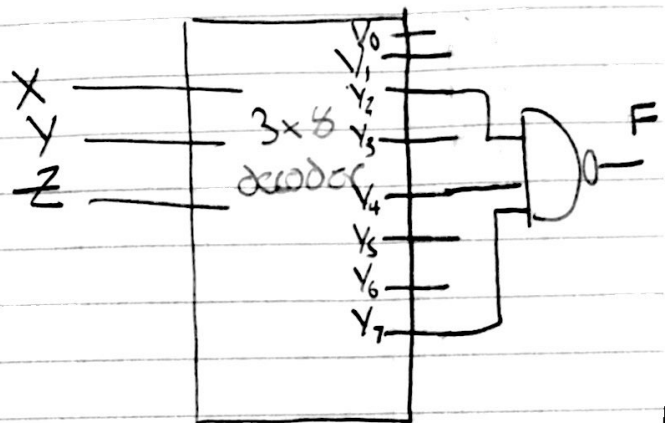
HW 7:

6.20)

a) $F = \sum XYZ(2, 4, 7)$

X \ YZ	00	01	11	10
0				1
1	1		1	

$$F = \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XYZ$$

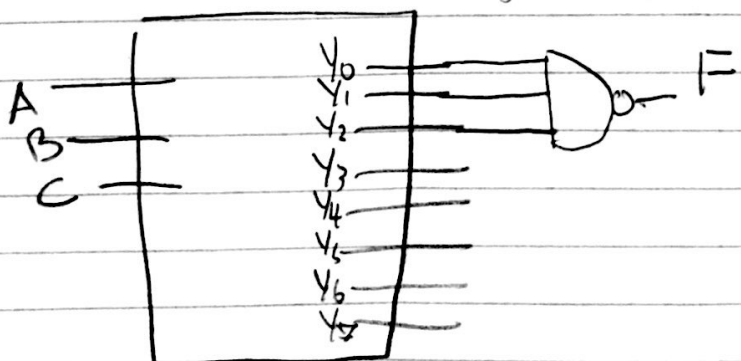


b) $F = \prod_{ABC}(3, 4, 5, 6, 7)$

$$F = \sum_{ABC}(0, 1, 2)$$

A \ BC	00	01	11	10
0	1	1		1
1				

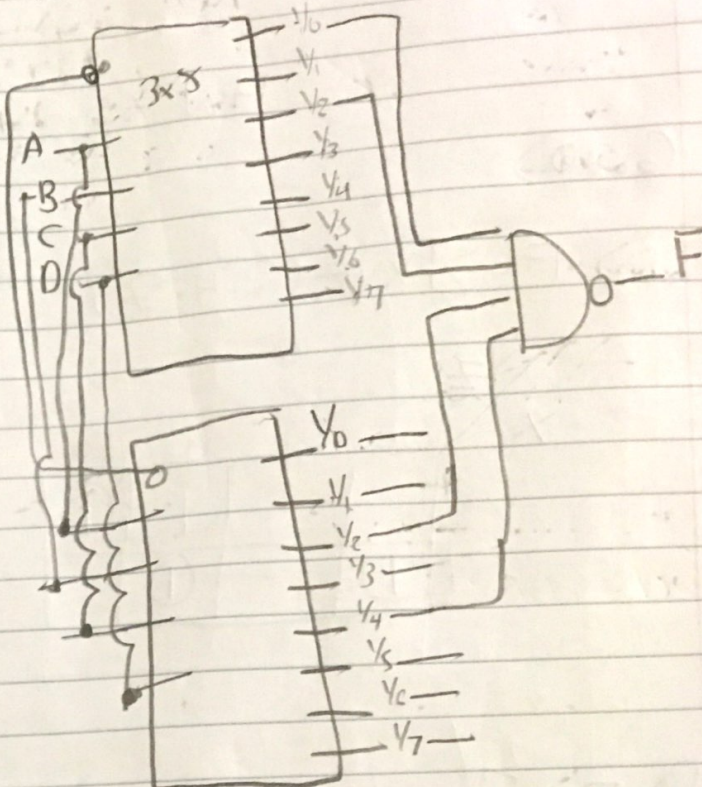
$$F = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$



c) $F = \sum_{ABCD} (0, 2, 10, 12)$

$$F = \overline{A}BCD + \overline{A}B\overline{C}\overline{D} + \overline{A}B\overline{C}D + \overline{A}B\overline{C}\overline{D}$$

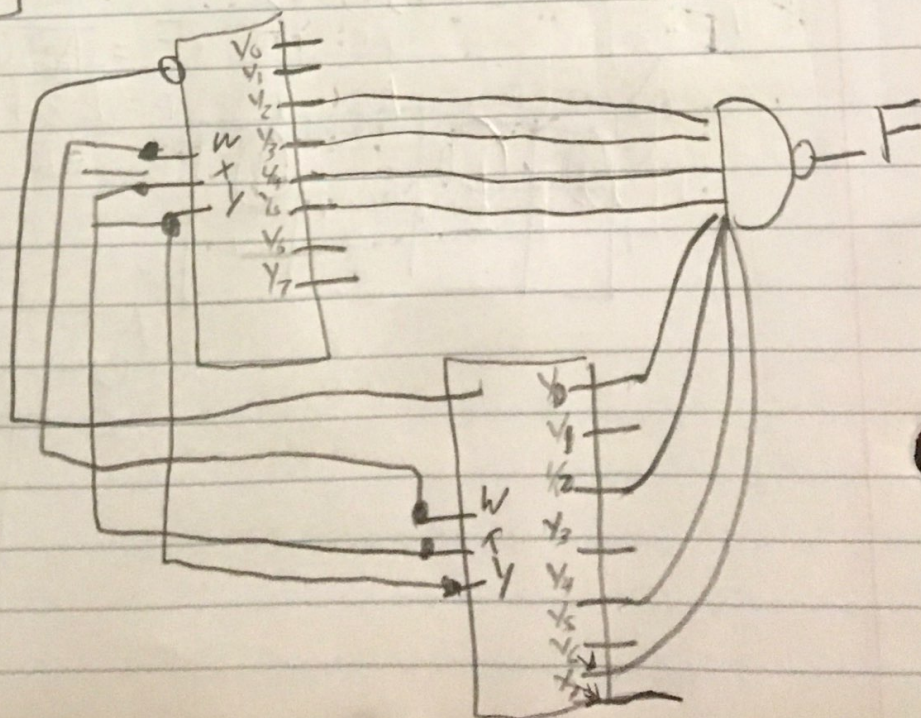
AB \ CD	00	01	11	10
00	1			1
01				
11	1			
10				1



d)

WX \ YZ	00	01	11	10
00			1	1
01	1	1		
11	1			1
10	1			1

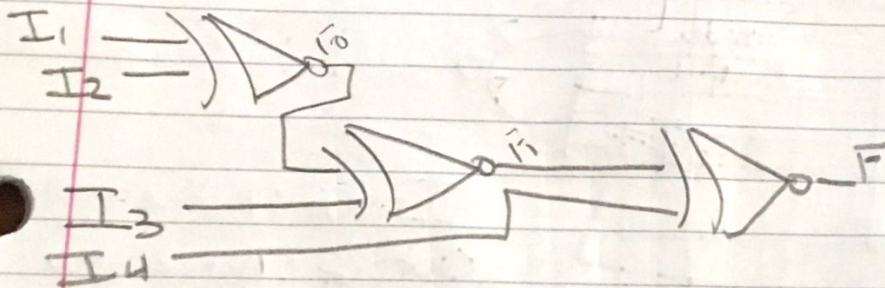
$$F = WXY + \overline{W}X\overline{Y} + W\overline{Y}\overline{Z} + WY\overline{Z}$$



6.21:

- The circuit is wrong because if you look closely you can see that both halves of the 74x139 are enabled at the same time.
- This problem can be solved by putting an inverter on the signal going 16 to 26, which ensures that only one source drives SDATA at all times!

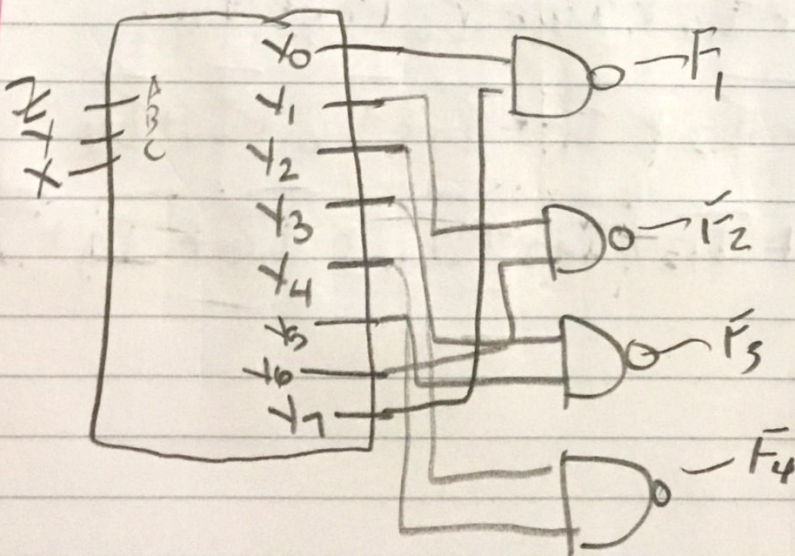
6.24:



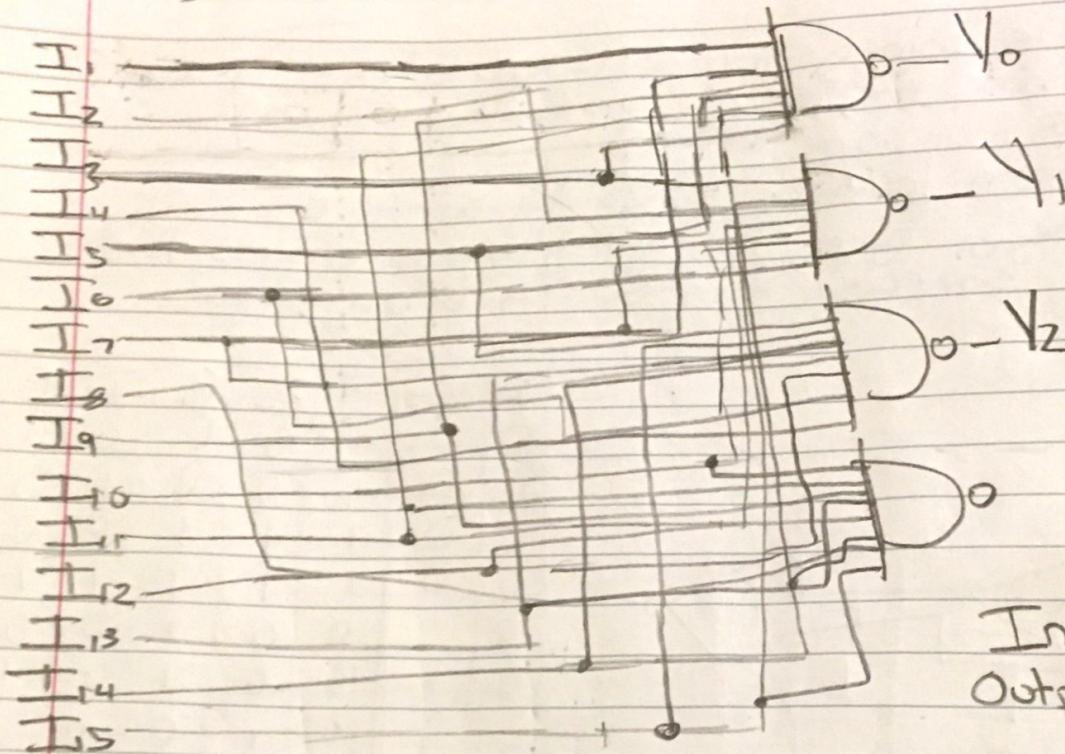
I_1	I_2	F_0	I_3	F_1	I_4	F
0	0	1	0	0	0	1
0	0	1	0	0	1	0
0	0	1	1	1	0	0
0	0	1	1	1	1	1
0	1	0	0	1	0	0
0	1	0	0	1	1	1
0	1	0	1	0	0	1
0	1	0	1	0	1	0
1	0	0	0	1	0	0
1	0	0	0	1	1	1
1	0	0	1	0	0	1
1	0	0	1	0	1	0
1	1	1	0	0	0	1
1	1	1	0	0	1	0
1	1	1	1	1	0	0
1	1	1	1	1	1	1

This is an even parity

6.43)



6:51)



Input : Active High
Output : Active Low

$$Y_0 = \overline{I_{15}} + \overline{I_{13}} + \overline{I_{11}} + \overline{I_9} + \overline{I_7} + \overline{I_5} + \overline{I_3} + \overline{I_1}$$

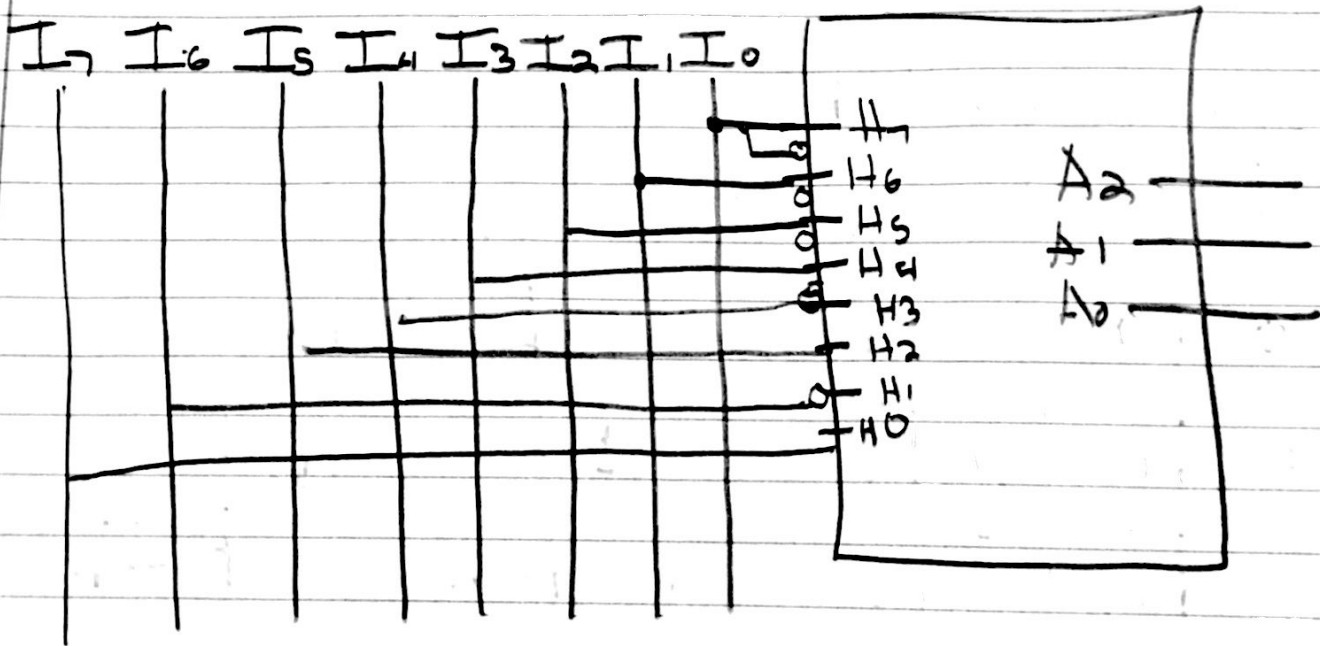
$$Y_1 = \overline{I_{15}} + \overline{I_{14}} + \overline{I_{11}} + \overline{I_{10}} + \overline{I_7} + \overline{I_6} + \overline{I_3} + \overline{I_2}$$

$$Y_2 = \overline{I_{15}} + \overline{I_{14}} + \overline{I_{13}} + \overline{I_{12}} + \overline{I_7} + \overline{I_6} + \overline{I_5} + \overline{I_4}$$

$$Y_3 = \overline{I_{15}} + \overline{I_{14}} + \overline{I_{13}} + \overline{I_{12}} + \overline{I_{11}} + \overline{I_{10}} + \overline{I_9} + \overline{I_8}$$

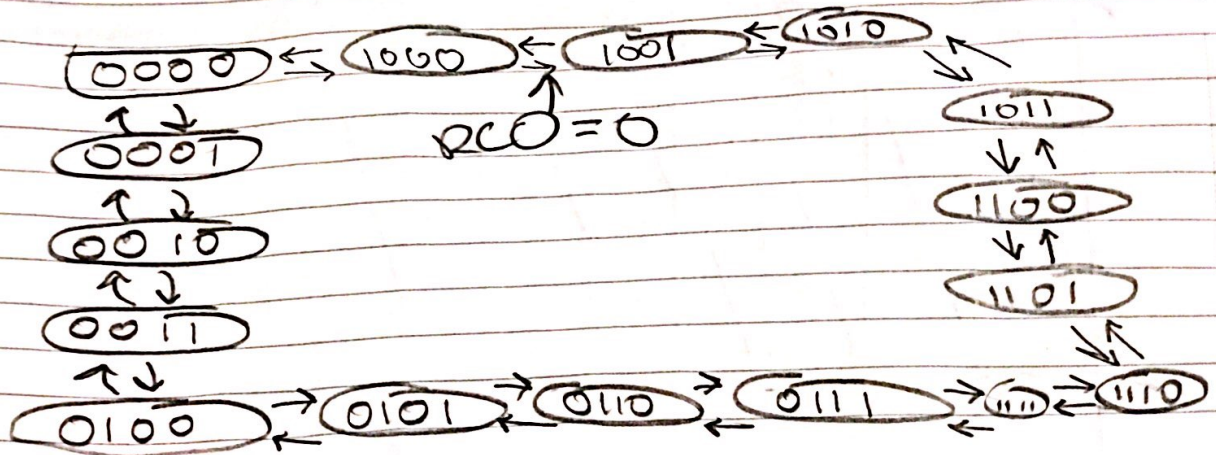
53)

								Outputs			Avalid
I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	A_2	A_1	A_0	
1	1	1	1	1	1	1	1	0	0	0	1
1	1	1	1	1	1	1	1	0	0	1	1
1	1	1	1	1	1	1	1	0	1	0	1
1	1	1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	1	1	0	0	1
1	1	1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0



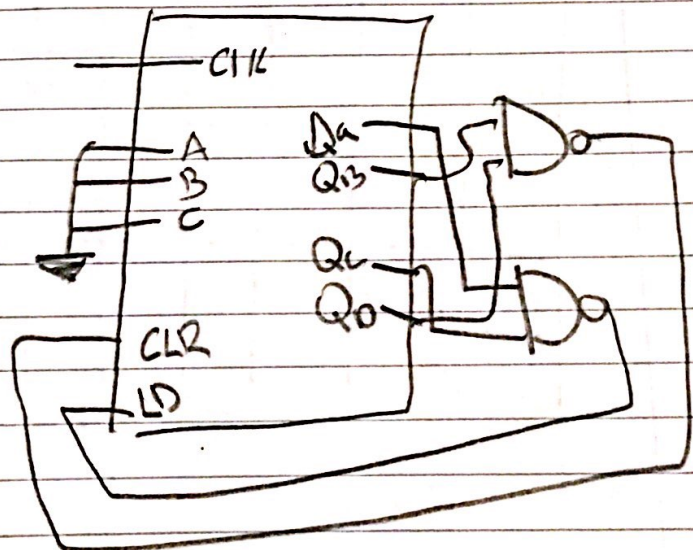
Chapter 3:

13)

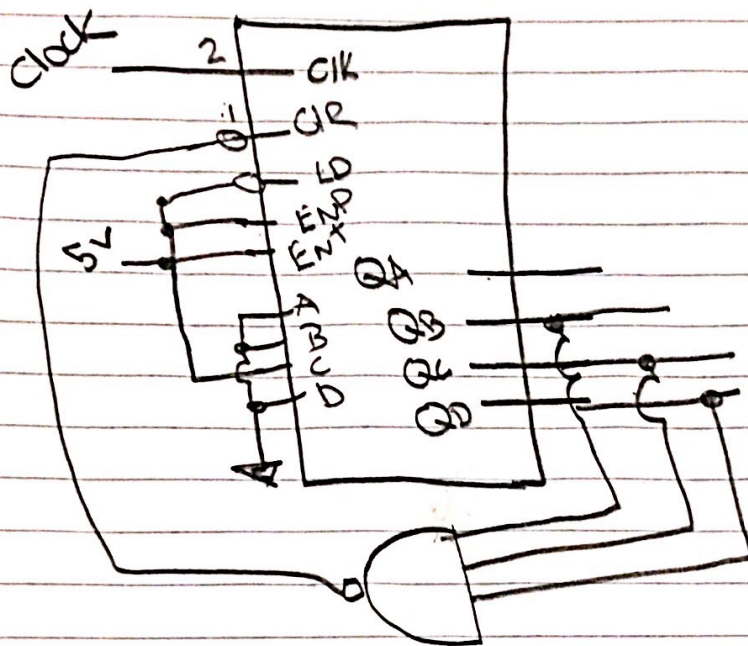


14)

QD	QC	QB	QA
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1



35)



36)

