EE P 538
Analog Circuits for Sensor Systems

Spring 2020

Instructor: Jason Silver, PhD

Announcements

- Assignment 4 due Saturday, May 2 at midnight
- Assignment 5 will be posted May 1
  - Due Saturday, May 9 at midnight

Midterm Info

- Administered as a timed quiz on Canvas
- 3 hours to complete, submitted as a PDF within time limit
- Will consist of 3 problems (1 BJT/FET problem, 2 opamp problems), covering the first 5 weeks of course material
- Practice exam will be made available this weekend

Week 5

- AoE Chapter 5 – Precision Circuits
  - 5.1 – 5.8
  - 5.13 – 5.15

Overview

- Last time…
  - Basic opamp behavior
  - Feedback
  - Frequency response
  - Non-ideal behavior
- Today…
  - Error modeling
  - Opamp errors
  - Differential signaling
  - Difference amplifiers
  - Instrumentation amplifiers

Lecture 5 – Precision Design

Precision Design Goals

- There is often a need for high precision circuits in measurement and control applications
- Circuits should be accurate, stable with time and temperature, and predictable
- Numerous sources of error make these goals challenging (noisy power supplies, thermal noise, nonlinearity, amplifier errors, to name a few)
- Precision analog design is all about using the right combination of components and circuit architectures to achieve strict performance goals in the face of device limitations and variability

Error Budget

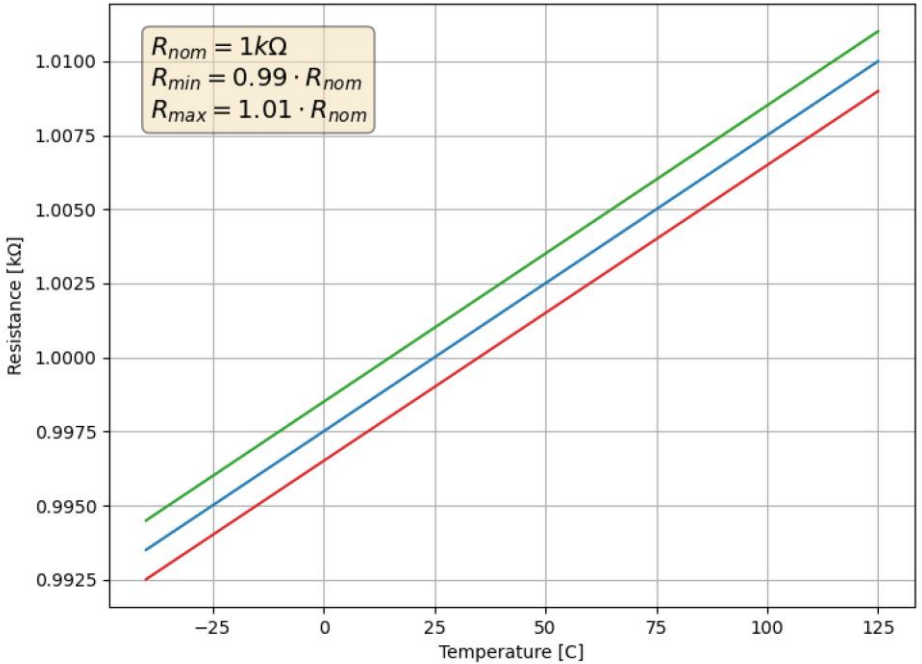
- It's important to understand how individual sources of error affect performance for a given application
- All error sources should be accounted for to understand potential problem areas and how the design might be improved
- It is good practice to *refer all errors to the input* of a system to be able to clearly quantify their net effect and make direct comparisons
- Once this "error budget" is created, rational decisions can be made regarding component selection and (inevitable) performance tradeoffs

Sources of Error

- *Initial accuracy*
  - Manufacturing tolerance – specified as a percentage (e.g. 1%, 0.1%)
- *Stability*
  - Component value drift over time – specified in ppm/(large time unit)
- *Temperature*
  - Component value drift with temperature – specified in ppm/°C
- *Nonlinearity*
  - Voltage dependence of component values (e.g. gain) – specified

Example: Resistor Accuracy

- Resistors used in opamp feedback networks may require tight tolerance for gain accuracy and noise performance
- A resistor with 0.1% tolerance may have a temperature coefficient as high as 100ppm/°C
- At the extremes of its operating range, this will result in an error as high as 1%
- If a resistor dissipates significant power, heating is inevitable



Error Modeling

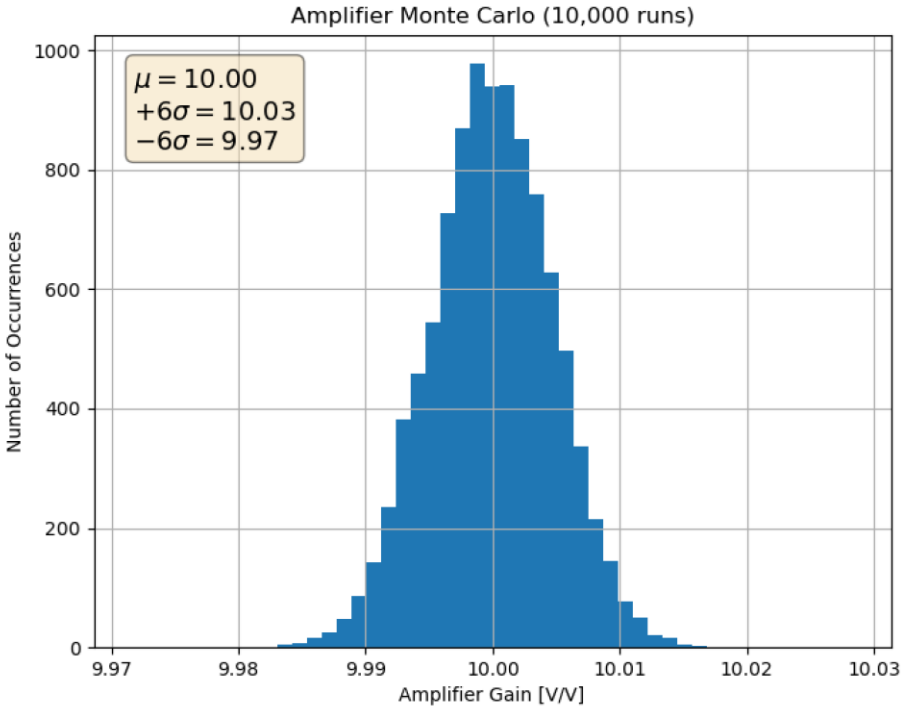
- *Initial accuracy*: Tolerance, smaller is better (e.g. 1%, 0.1%)
  - Monte Carlo (MC) or worst-case (WC) analysis (“corners”)
- *Stability*: Component value drift over time, specified in ppm/(time)
  - Modeled manually and incorporated into error budget
- *Temperature*: Parameter variation with temperature
  - Temperature sweep with appropriate temperature coefficient
- *Nonlinearity*: Voltage dependence of component values (e.g. gain)
  - Transient simulation, FFT, THD

Modeling Component Variability

- Monte Carlo simulations can be used to randomly vary component values according to a known statistical distribution (e.g. Gaussian)
  - Can predict the probability of failing spec based individual component error probabilities
  - Requires large number of samples, time-consuming for complex circuits, component statistics may be unreliable/unavailable
- Worst-case “corner” simulations can save time by only considering the extremes (e.g. min/max temperature, min/max resistance)
  - Doesn’t assume anything about statistical distributions
  - Must ensure that all relevant “corner” cases are considered
  - May be overly pessimistic in accounting for low probability events

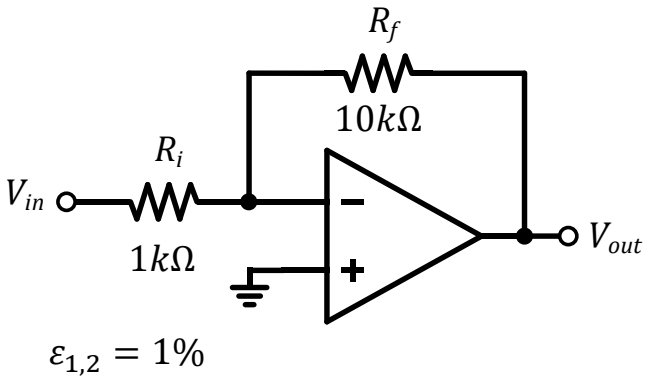
Monte Carlo Analysis

- In Monte Carlo (MC) analysis, a parameter (e.g. resistance) is cast as a random variable with a specific distribution (e.g. uniform, Gaussian)
- The performance of the circuit is then assessed relative to a specified probability of "failure" (e.g. 6σ = 3.4/million)
- *Problem*: component values may not have known or consistent distributions



Worst-Case Analysis

- As an alternative to MC analysis, a given parameter (or group of parameters) is varied between its min/max values
- For example, in an inverting amplifier, the gain of which is $-R_f/R_i$, we would examine the behavior of the circuit at all min/max combinations:



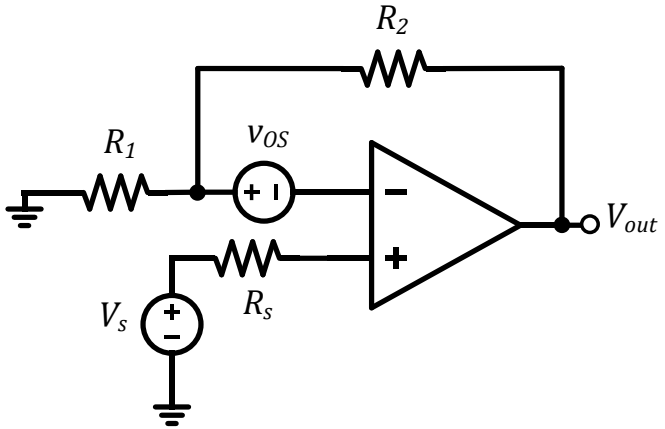
R_i	R_f	$-R_f/R_i$
0.99kΩ	9.9kΩ	–10
0.99kΩ	10.1kΩ	–10.2
1.01kΩ	9.9kΩ	–9.8
1.01kΩ	10.1kΩ	–10

Opamp Errors

- Input offset voltage and bias current
  - Input bias current errors vary with source resistance
- Finite power supply rejection (PSRR)
  - Typically fairly high, and may not be a concern with a well-designed power supply
- Finite common-mode rejection (CMRR)
  - Ability of an amplifier to suppress common-mode “noise”
- Finite gain, bandwidth, and slew rate (SR)
- Voltage and current noise
  - Johnson and flicker noise

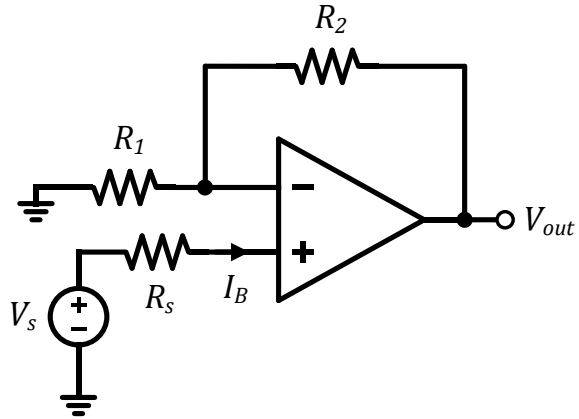
Input Offset Voltage Error

- Opamp can't distinguish between its own offset and a "real" input
- As a result, v_{os} is amplified along with the sensor voltage
- For signals at DC, special techniques (e.g. auto-zeroing) may be required to achieve the required precision
- However, there are tradeoffs, as such techniques tend to increase noise and affect amplifier input impedance



$$V_{out} = \left(1 + \frac{R_2}{R_1}\right)(V_s + v_{OS})$$

Input Bias Current Voltage Error



Example values: $I_B = 1nA$ $R_s = 1k\Omega$

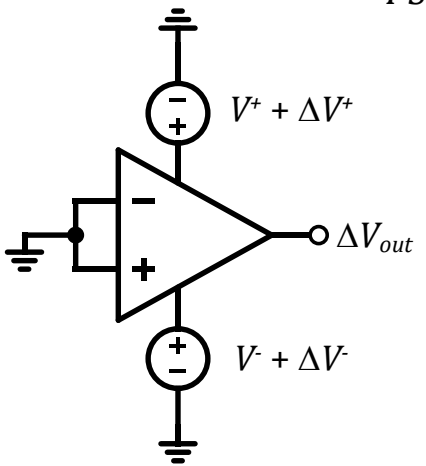
$$V_{err} = I_B R_S = 1\mu V$$

- Nanoamp currents produce voltage errors of microvolts for source impedances as small as 1kΩ
- FET op-amps can do better, but at the expense of increased voltage offset and noise
- Input current for FET's is actually gate leakage, which rises dramatically with temperature (in contrast to BJT base current)

Power Supply Rejection

- An opamp's power-supply rejection ratio (PSRR) refers to its ability to "reject" changes in power supply voltage at its output
- A higher PSRR corresponds to a lower "gain" from the power supply to the output
- PSRR typically tracks the opamp's open-loop gain, falling off at higher frequencies
- PSRR is generally not the same for the positive and negative supplies

$$PSRR_+ = \frac{\Delta V^+}{\Delta V_{out}}$$

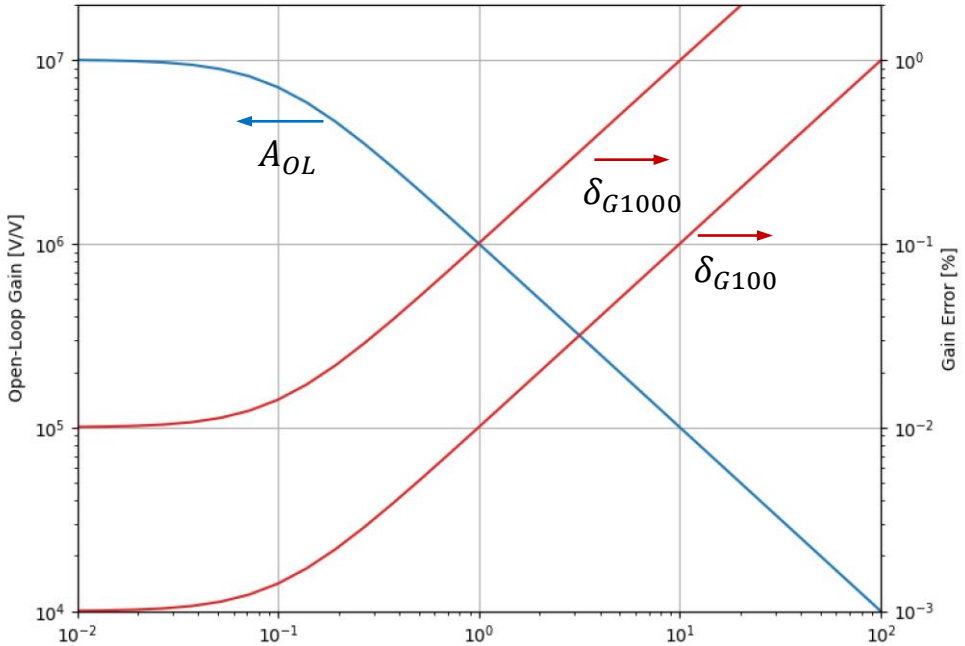


$$PSRR_- = \frac{\Delta V^-}{\Delta V_{out}}$$

Gain Error

- Gain accuracy is important not only at DC, but at all signal frequencies of interest
- As the open-loop gain decreases with frequency, so does the closed-loop precision
- The gain error for a given closed-loop gain target is given as

$$\delta_G = \frac{G_{ideal} - G_{actual}}{G_{ideal}}$$



Settling Time

- An amplifier's output cannot change instantaneously due to finite bandwidth
- For small-signal changes, the settling time can be well-approximated by a 1st-order response
- The equivalent time constant is roughly given as

$$\tau_{CL} = \frac{1}{2\pi f_{3dB,CL}} \approx \frac{1}{2\pi\beta f_T}$$

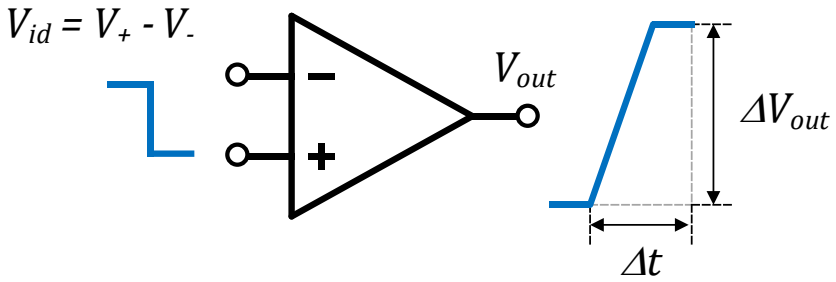
- For example, given an f_T of 10MHz and a feedback factor β = 0.1, suppose we need our design to settling to 0.1% precision
- The time constant is

$$\tau_{CL} \approx \frac{1}{2\pi\beta f_T} = 159ns$$

- For 0.1% precision, we need approximately 7τ:

$$t_{settle} \approx 7\tau_{CL} \approx 1.1\mu s$$

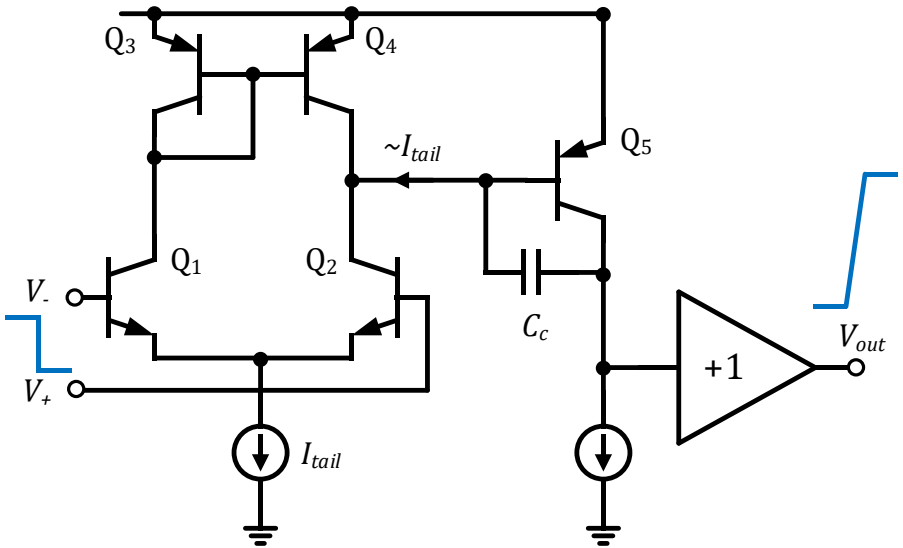
Finite Slew Rate



$$SR = \frac{\Delta V_{out}}{\Delta t} \left[\frac{V}{\mu s}\right]$$

- Both bandwidth (f_T) and settling time represent an opamp's response to small-signal perturbations
- An opamp's slew rate represents the *maximum rate of change* of the output voltage when a large differential input voltage is applied
- Slew rate (SR) is generally expressed in V/µs, with typical values from 0.1 to 10 V/µs (Ltspice AD8691)

Opamp Slew Rate



$$f_T \approx \frac{g_{m1,2}}{C_c} \qquad SR \approx 0.3 f_T$$

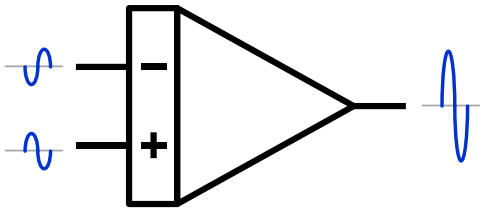
- A typical opamp consists of a differential input stage ($Q_{1,2}$), a second gain stage (Q_5), and a low-impedance output buffer
- C_C is a compensation capacitance used to set the amplifier bandwidth
- For a sufficiently large differential input (~60mV), the majority of I_{tail} is steered through Q_2 to discharge C_c
- The slew rate (SR) is determined by the values of I_{tail} and C_c

Differential Signaling

$$V_{id} = V_i^+ - V_i^-$$

$$V_i^- = V_{icm} - \frac{V_{id}}{2}$$

$$V_i^+ = V_{icm} + \frac{V_{id}}{2}$$

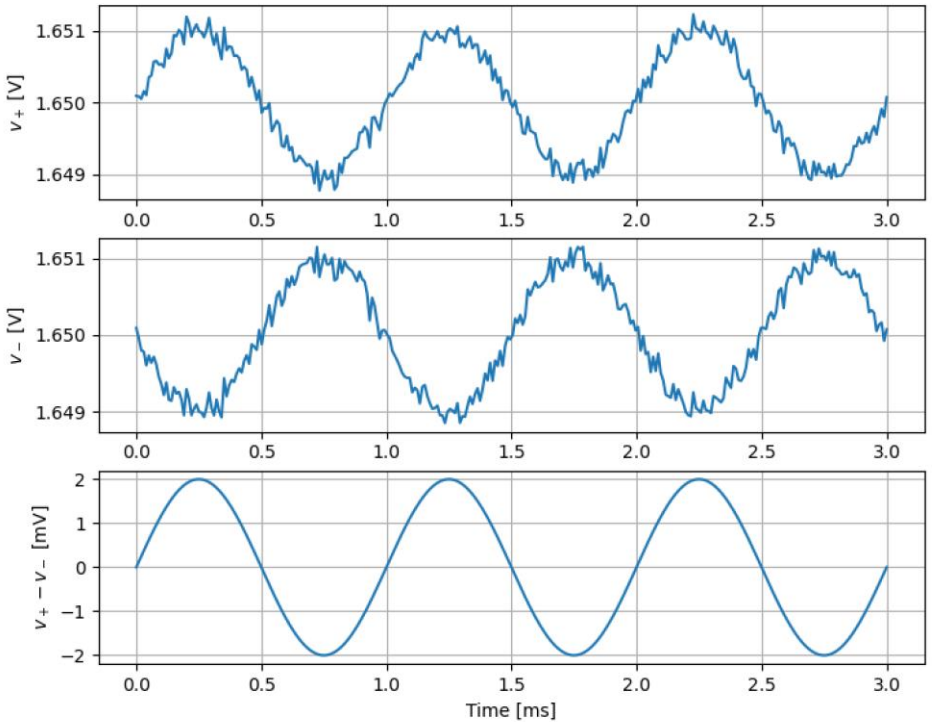


$$V_o = V_{ocm} + A_{vd}V_{id}$$

- Applications demanding high precision often employ differential signaling for robustness against certain types of noise/error
- A *differential signal* is encoded as the *difference* between two voltages (or currents)
- Differential operation can guard against errors that affect both equally, typically referred to as *common-mode* errors

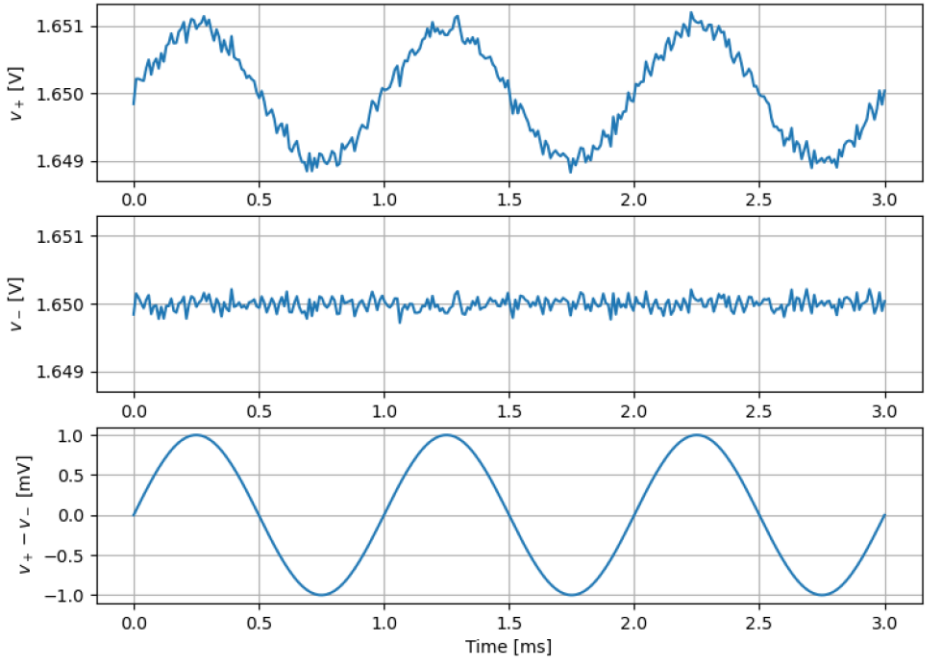
Differential Signals

- Here, we see that the *common-mode* component consists of both the DC level (1.65V) and noise (the wiggly stuff)
- Taking the difference removes both the DC component and the “noise,” leaving behind only the *differential* content
- Note that *many* sources of noise are *not* common-mode, and as a result are not eliminated by differential signaling



Asymmetric Differential Signals

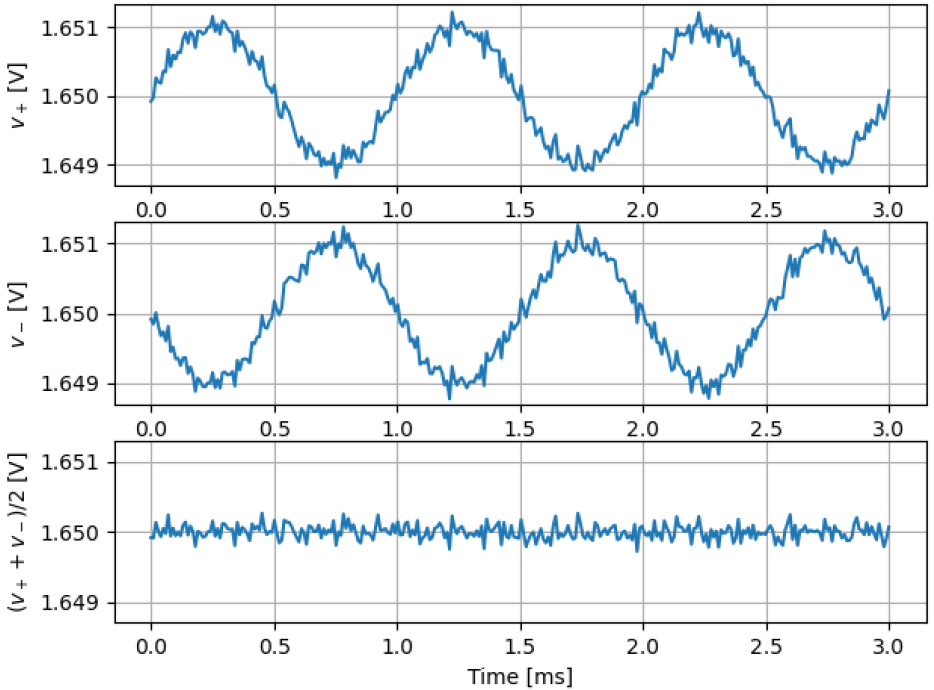
- Differential signals need not be symmetric to retain the benefits of differential signaling (such as *common-mode rejection*)
- It is common to drive one input of a differential amplifier with a single-ended signal and connect the other to a DC voltage
- Note that again, all common-mode components are removed when taking the difference



Common-Mode "Stuff"

- The common-mode component of a pair of differential voltages is the average of the two
- The common-mode is either incidental or undesirable (or both), and not part of the signal
- While the differential component is the difference, the common-mode component is the sum (divided by 2)

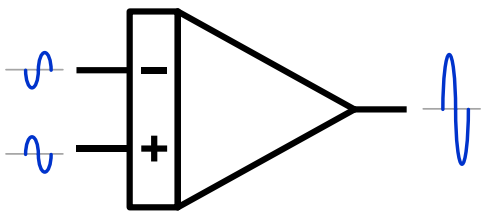
$$V_{cm} = \frac{V_+ + V_-}{2}$$



Common-Mode Rejection

$$V_{icm} = \frac{V_{ip} + V_{id}}{2}$$

$$V_{id} = V_{ip} + V_{id}$$

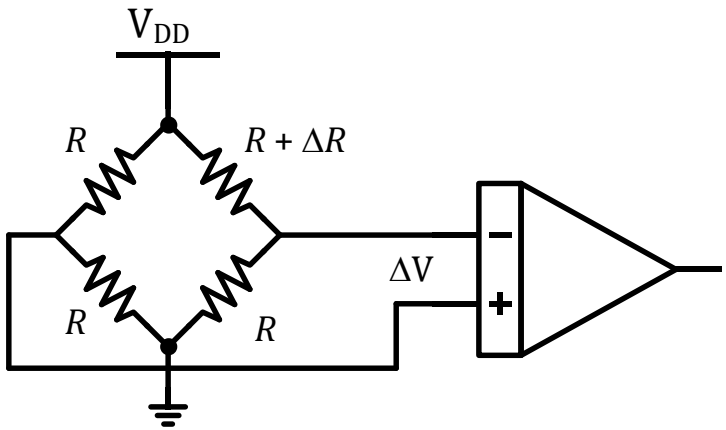


$$A_{vd} = \frac{V_o}{V_{id}} \qquad A_{vcm} = \frac{V_o}{V_{icm}}$$

$$CMRR = \frac{A_{vd}}{|A_{vcm}|}$$

- An ideal difference amplifier amplifies differential signals and completely rejects common-mode noise
- However, without proper matching of critical components, the ratio of differential signal to common-mode noise may not be adequate
- The common-mode rejection ratio (CMRR) of an amplifier quantifies how well it suppresses common-mode signals

Application: Strain Gages

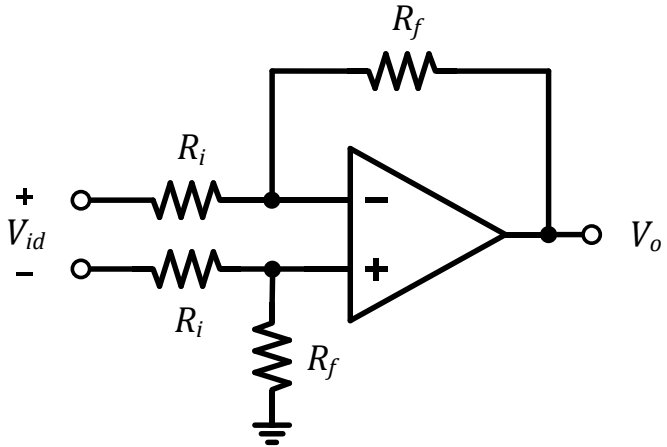


$$V_{icm} = \frac{V_{DD}}{2} \qquad sens \approx \pm 2mV/V$$

- A strain gage converts material strain into a change in resistance
- Without strain, resistors are all nominally equal, so $\Delta V = 0$
- When the resistances are subjected to differing strains, the output voltage changes based on the strain gage sensitivity
- An amplifier with differential inputs amplifies the sensor voltage for further processing

Difference Amplifier

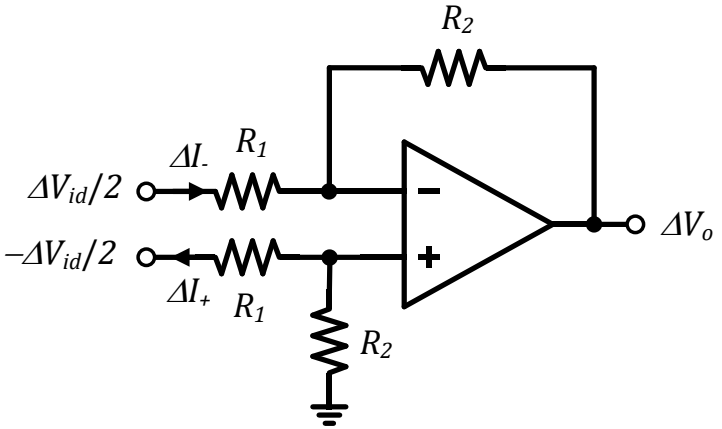
- Difference amplifiers are convenient for interfacing with sensors with differential outputs (e.g. strain gages)
- The single-ended output is readily used with other circuit blocks (e.g. filters or ADC's)
- However, the input resistance of a difference amplifier is low, making it challenging to interface with high-resistance sensors



$$V_o = -\frac{R_f}{R_i} V_{id}$$

Differential Input Impedance

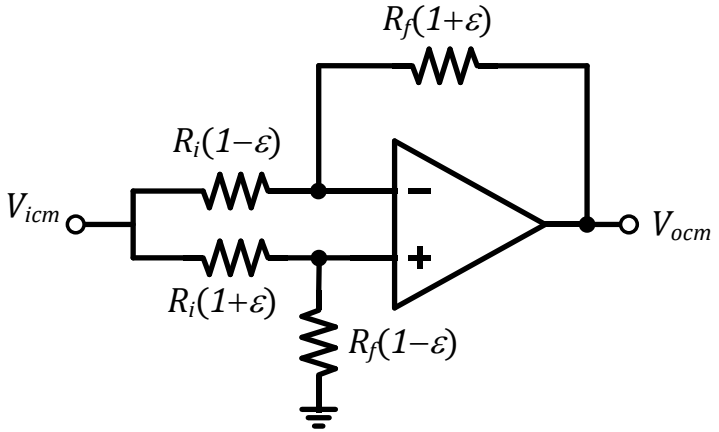
- The differential input impedance is the impedance seen a circuit driving the amplifier differentially
- This is in contrast with the common-mode impedance, where the inputs are driven with the same voltage
- In order to provide gain, R_1 must be small (to limit its noise), which decreases the input impedance of the amplifier (undesirable)



$$Z_{in} = \frac{\Delta V_{id}}{\Delta(I_- - I_+)} = R_1\left(1 + \frac{R_1}{R_2}\right)$$

Common-Mode Rejection

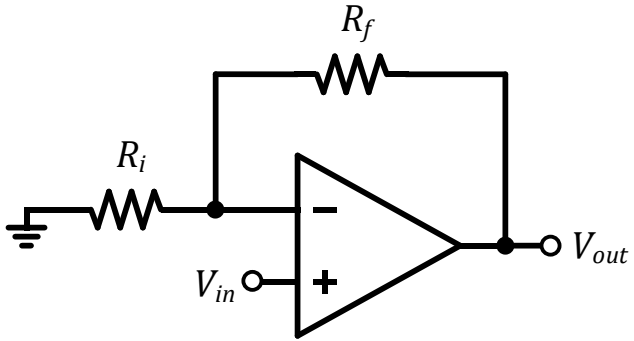
- Even with a perfect opamp, component errors in the feedback network degrade precision
- For differential applications, this affects both gain *and* common-mode rejection
- For A_{vd} = 100 and ε = 1%, we get a CMRR of ~74dB
- For higher CMRR, use resistors with tight tolerances (e.g. ε = 0.1%), or use an integrated difference amplifier



$$CMRR = \frac{A_{vd}}{|A_{vcm}|} \approx \frac{A_{vd}+1}{4\times\varepsilon}$$

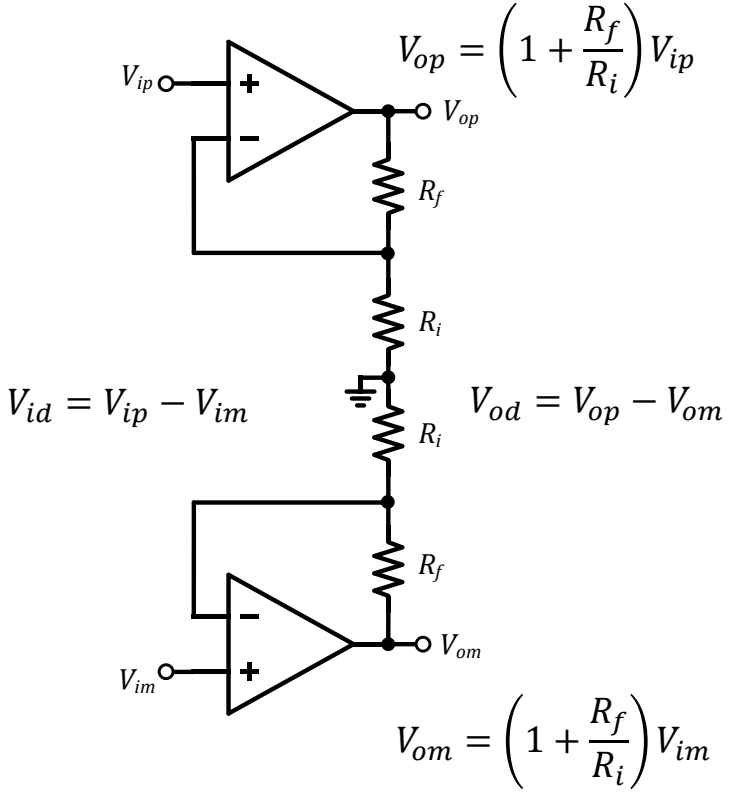
Non-inverting Amplifier

- The high input impedance (up to 100's of GΩ's) of the non-inverting amplifier makes it ideal for interfacing with many sensors
- However, the single-ended structure means it has a CMRR of 0dB, which won't work for a small signal voltage riding on a much larger common-mode
- We need a structure with both *differential inputs* and *high input impedance*



$$Z_{in} = R_{in,opamp}$$

Pseudo-differential Amplifier

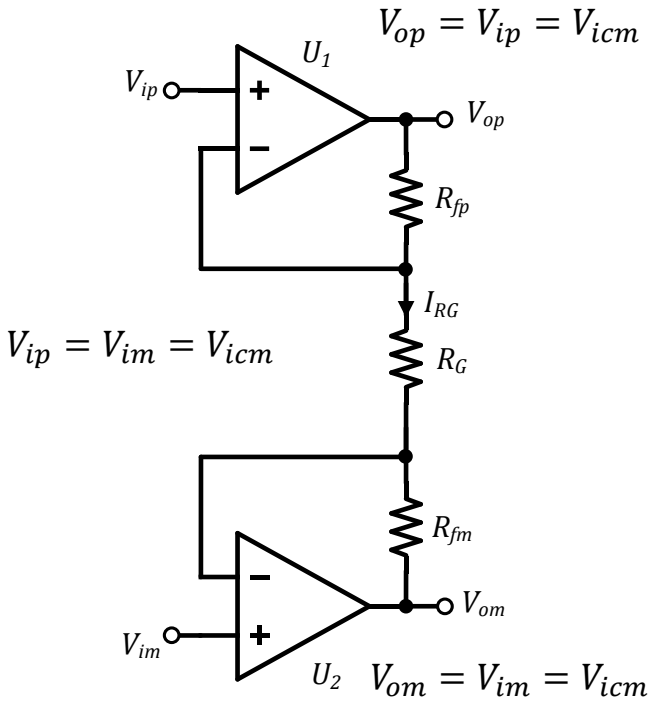


- Two non-inverting stages connected in parallel can process a differential signal
- Now we have a "differential" structure with high-impedance inputs, the gain of which is defined as

$$\frac{V_{op} - V_{om}}{V_{ip} - V_{im}} = 1 + \frac{R_f}{R_i}$$

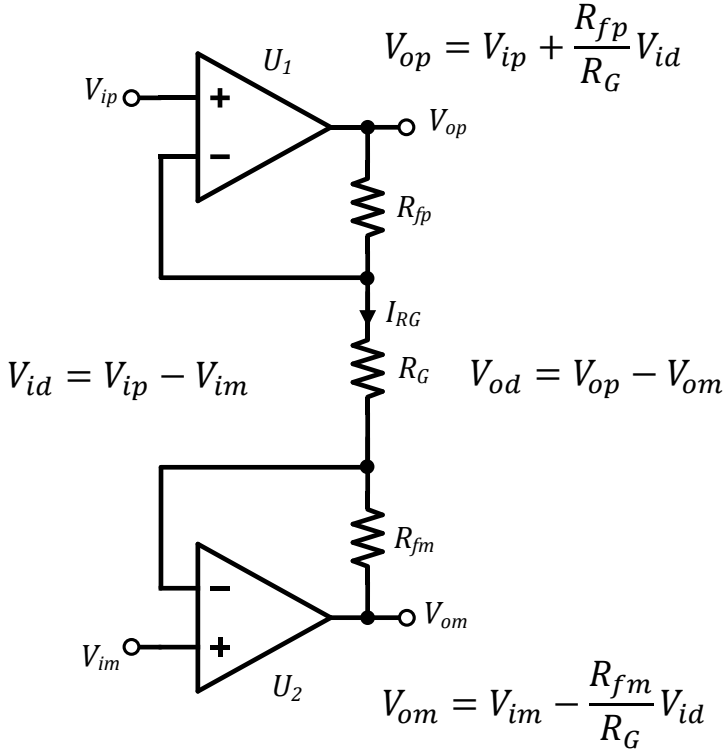
- However, the common-mode gain is equal to the differential gain (CMRR = 1!)

Instrumentation Amplifier Input Stage



- With the ground connection removed, we effectively establish a “floating” reference for the first stage ($U_{1,2}$)
- The common-mode gain is 1, regardless of matching between R_{fp} and R_{fm}
- To understand why, imagine connecting the same voltage to both inputs (V_{ip} = V_{im})
- No current flows through the resistors, so both outputs (V_{op} and V_{om}) are equal to V_{icm}

Differential Gain



- For a differential input signal V_{id}, the voltage across R_G becomes $V_{ip} - V_{im} = V_{id}$
- The current through the three resistors is thus

$$I_{RG} = \frac{V_{id}}{R_G}$$

- The output voltage is then simply

$$V_{od} = V_{id} + \left(\frac{R_{fp} + R_{fm}}{R_G} \right) V_{id}$$

1st Stage CMRR

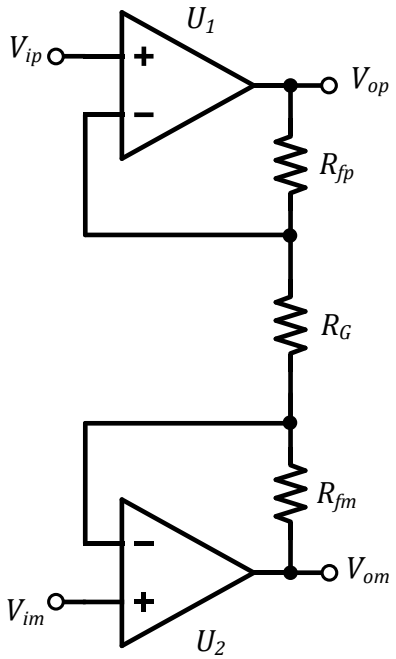
$$A_{vd1} = \frac{V_{od}}{V_{id}} = 1 + \left(\frac{R_{fp} + R_{fm}}{R_G}\right)$$

$$A_{vcm1} = \frac{V_o}{V_{icm}} = 1$$

$$CMRR = \frac{A_{vd1}}{A_{vcm1}} = 1 + \left(\frac{R_f}{R_G}\right)$$

- R_{fp} and R_{fm} are nominally the same resistance, R_f
- The common-mode sees a gain of 1, while the differential-mode sees the gain of a non-inverting opamp stage
- We get high differential gain with no degradation in the common mode (AoE: common-mode “blessings”)

Effect of Resistor Mismatch

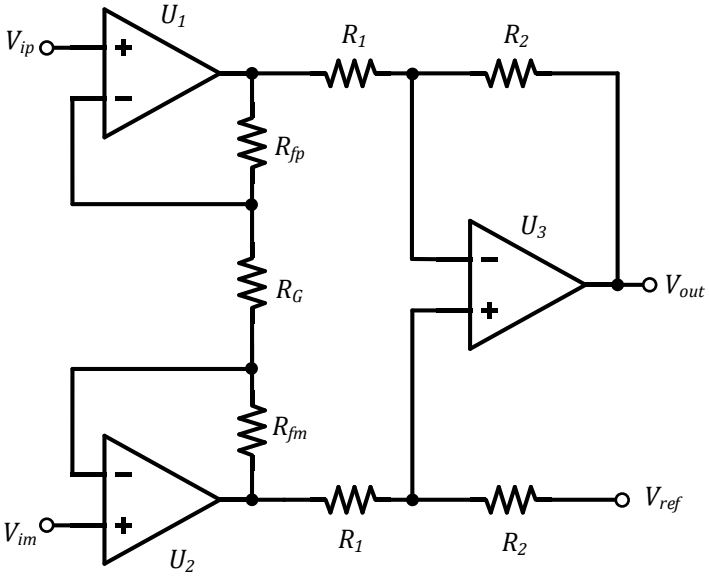


- Even if R_{fp} and R_{fm} are poorly matched, the circuit performs well
- The differential gain is just

$$A_{vd1} = \frac{V_{od}}{V_{id}} = 1 + \left(\frac{R_{fp} + R_{fm}}{R_G} \right)$$

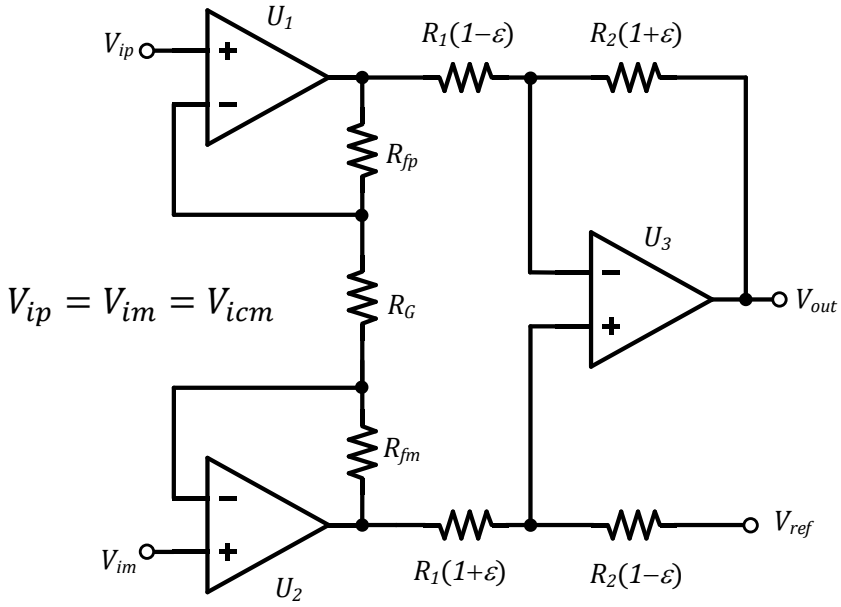
  where $R_{fp} \neq R_{fm}$
- The common-mode gain is still just 1, since U_1 and U_2 ensure that no current flows through R_G regardless of the values of R_{fp} and R_{fm}

Diff Amp Output Stage



- A difference amplifier is cascaded with the first stage to convert its output to a single-ended voltage
- The second stage can increase the gain, or its gain can be set to 1 ($R_1 = R_2$)
- The low input impedance of difference amplifier is easily driven by the two non-inverting stages
- The CMRR is A_{vd1} times higher than that of the difference amplifier alone

Instrumentation Amp CMRR



$$CMRR_1 = 1 + \left(\frac{R_{fp} + R_{fm}}{R_G}\right)$$

$$CMRR_2 \approx \frac{A_{vd2} + 1}{4 \times \varepsilon}$$

$$\frac{R_{fp} + R_{fm}}{R_G} = 99 \qquad R_1 = 10R_1$$

$$20 \log CMRR \approx 109dB$$