EE P 328 Spring 2020
Analog Circuits for Sensor Systems
University of Washington Electrical & Computer Engineering

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Design Project: Strain-Gage Low-Noise Signal Conditioning

The final project for this course involves the design of the signal conditioning electronics for a strain gage sensor. You will design amplification and filtering for a strain gage signal with minimum amplitude in the μV range. The goals of this project are:

- To understand how to translate application specifications (e.g. dynamic range of a sensor output) into circuit specifications
- To understand the impact of different noise sources in a circuit and how they affect the achievement of performance targets (e.g. SNR), both individually and collectively
- To understand how to choose devices and apply gain and filtering to optimize for SNR, power dissipation, size, and cost
- To understanding the impact of manufacturing variations on performance goals, and how to select components that achieve the optimal balance between performance, component availability, and cost

The project will comprise two phases, each phase lasting 2-3 weeks. At the end of Phase 1 you are asked to submit 5-10 slides providing the details of your design choices and the results of any relevant analyses (e.g. circuit analysis or simulation results). Your Phase 2 submission will be a design report summarizing your approach and presenting your simulation results.

Please note that you will not be graded on meeting specifications until the final report submission. The primary purpose of the slide submission is to receive feedback and ensure that you are on track for meeting the final submission deadline. *Full credit will be given for the Phase 1 submission if all required deliverables are included (details to come).*

Table 1. Submission deadlines

Item	Due date	Proportion of project grade
Phase 1 slides	May 30	30%
Phase 2 report	June 12	70%

System Architecture

Many sensor systems employ analog multiplexing, a technique in which more than one sensor output is processed by a single ADC. Multiplexing reduces the overall component count and cost by sharing components between multiple sensor "channels". Because the ADC samples multiple inputs, the sampling frequency needs to be higher than the case where the ADC only converts a single channel. To first order, the sampling frequency of the ADC should be at least N times higher than the Nyquist frequency, where N is the number of sensor channels.

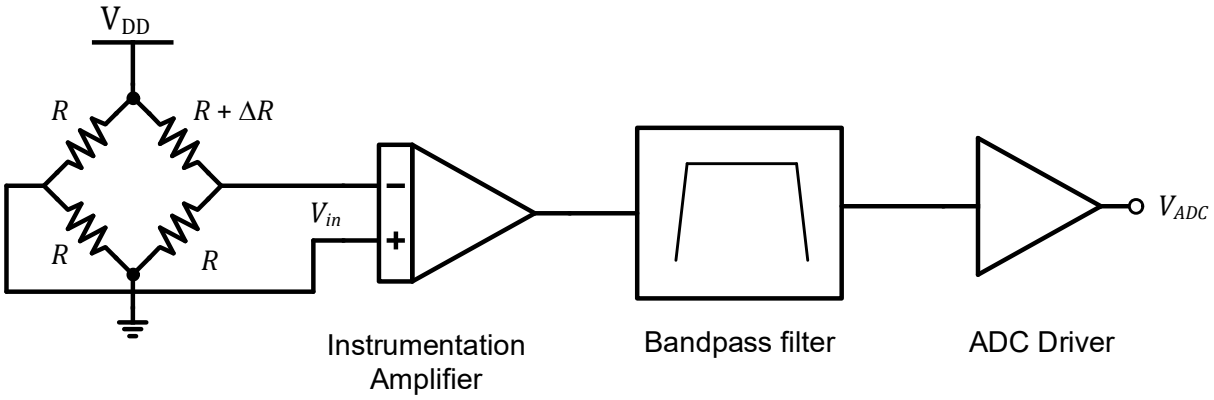

Figure 1. Strain gage signal conditioning architecture.

Fig 1. show the sensor signal conditioning "front-end" architecture for a single channel. The differential output voltage of the strain gage is amplified by the instrumentation amplifier and converted to a single-ended voltage. The output of the amplifier is fed to a bandpass filter which sets the noise bandwidth of the front-end circuitry and removes DC offset. The ADC driver is needed to settle the output voltage within the short sampling period of the multiplexed ADC.

The strain gage produces a differential output in response to an applied strain. This occurs as the result of the lengthening or shortening of a conductive element, which in turn changes its resistance. These changes in resistance are typically quite small, as the change in length (ΔL) relative to the nominal length (L) is small, on the order of 0.1% (for example).

Strain gage configurations are typically based on the Wheatstone bridge, a network of four resistances with an "excitation voltage" applied across the bridge (V_{DD} in Fig. 1). The number of bridge resistances subjected to strain determines the strain gage sensitivity (expressed in mV/V).

Phase 1

For the first phase you are to design a low-noise instrumentation amplifier to amplify the strain gage signal while adding minimal noise.

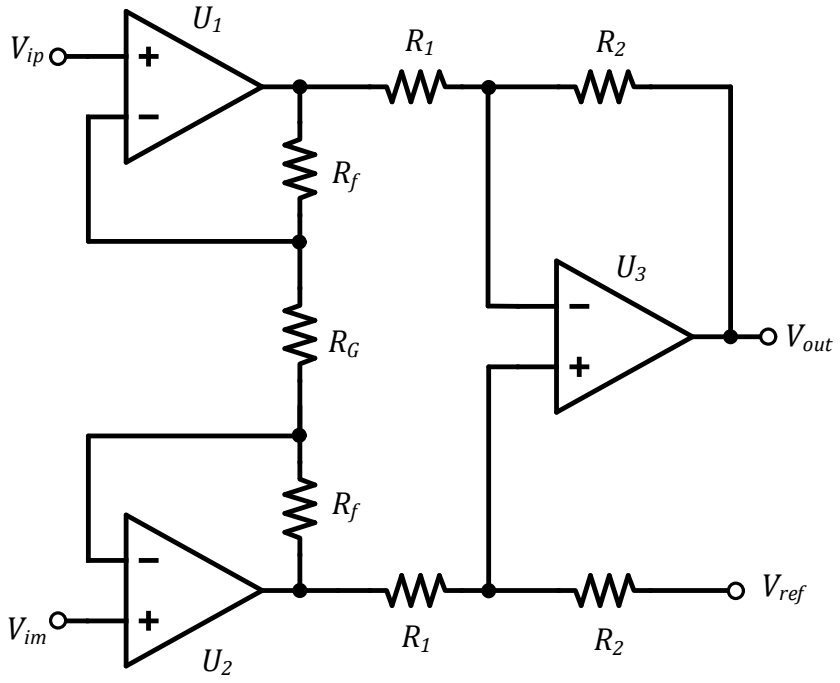

Table 2. Phase 1 specifications

Parameter	Specification	Unit
Supply voltage (V_{DD})	5	V
Peak-to-peak input signal amplitude (max)	20	mV
Nominal strain gage resistance (R)	1	kΩ
Peak-to-peak output amplitude (max)	2	V
Signal-to-noise ratio ($V_{id,rms}$ = 10mV/√2)	≥ 77	dB
Signal bandwidth	1 – 5k	Hz
CMRR	90	dB
Power dissipation ($I_{DD} \times V_{DD}$)	Optimize	mW
Cost	Optimize	$

Recommended design approach

- Determine the input-referred *voltage noise density* required to meet the specifications.
- Perform noise analysis of the instrumentation amplifier and determine the relative impact of all noise sources on the input-referred noise.
- Be sure to include the noise from the strain gage resistance. You should model the strain gage as a Thevenin equivalent circuit.
- Use the first stage to realize the required gain. This will minimize the impact of U_3's noise, as well as that of R_1 and R_2.
- Select component values that allow you to achieve the noise target, with resistor tolerances that make it possible to meet the CMRR specification.
- Use Digikey's or Analog Devices' component selection tables to select opamps that meet the requirements. Note that one limitation here is that the opamps you use have available SPICE models that include noise. Many of Analog Devices' models are already available in Ltspice. For any that aren't, you just need to import the SPICE netlist and create a new component (Ltspice will autogenerate the symbol for you, but you can also create a custom symbol).
- Take a systematic approach, rather than trying to simulate the amplifier straight away and "guess" at the component values.

Note on supply voltage and input range: *You need to ensure that both the single-ended supply voltage of 5V and the nominal sensor output voltage (5V/2 = 2.5V) are compatible with your opamp selection. The small sensor output swing of ±5mV won't be an issue for any opamp worth using.*

Flicker (*1/f*) noise: Some CMOS opamps exhibit particularly high *1/f* corner frequencies (f_c), which can significantly degrade your SNR. This can often be seen by the $e_{np\text{-}p}$ parameter provided in many datasheets (or the '*0.1 to 10Hz VNoise*' parameter in Analog Devices' opamp selection table). If your noise simulation result seems higher than expected, make sure your noise isn't being dominated by flicker noise.

Phase 1 deliverables

5-10 slides detailing the following:

1. Input-referred noise target based on the specifications
2. Expression showing the relative contribution of each noise source on the input-referred noise. Justify any assumptions.
3. Complete schematic showing the strain gage model, supply voltages, opamp models, resistor values, and DC operating point voltages at all nodes
4. AC simulation results showing the frequency response of the amplifier
5. Input-referred noise plot showing the noise density at 1kHz, along with the integrated noise from 1Hz to 5kHz.