

**EE 538 Spring 2020**  
**Analog Circuits for Sensor Systems**  
**University of Washington Electrical & Computer Engineering**

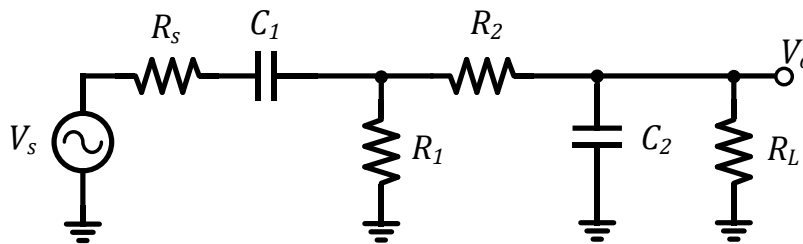
**Instructor: Jason Silver**

**Homework #1 (40 points)**

**Due Wednesday, April 8, Submit on Canvas**

*Please show your work.*

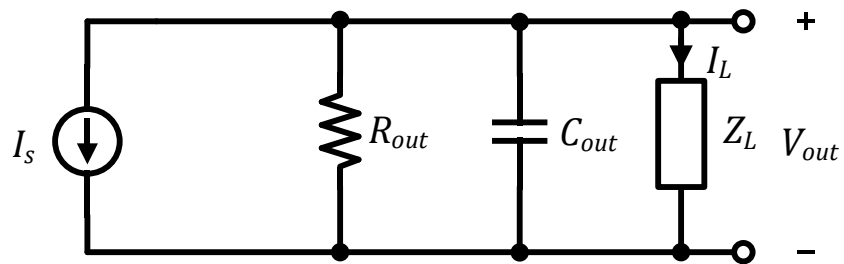
**Problem 1: Circuit loading, filtering**



Design the bandpass RC filter to achieve >20dB attenuation at 1MHz and less than 0.1dB attenuation from 1 Hz to 10 kHz.

- First, ignoring loading effects, determine 3dB frequencies ( $f_{3dB,HP}$  and  $f_{3dB,LP}$ ) that meet the specifications.
- With  $R_s = 100\Omega$  and  $R_L = 10M\Omega$ , choose  $R_1$ ,  $R_2$ ,  $C_1$ , and  $C_2$  to minimize loading effects.
- Simulate the frequency response ( $V_o/V_s$ ) in Ltspice and plot it together with the ideal response in MATLAB/Python.

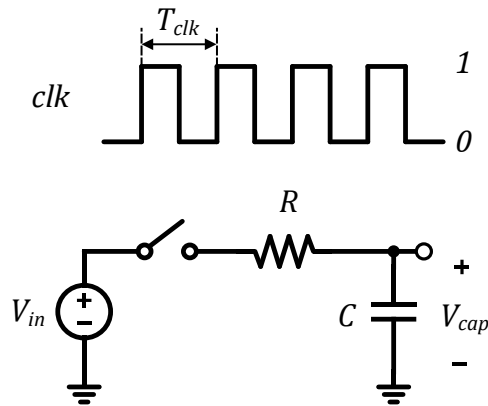
**Problem 2: Current sources, frequency response, loading**



Use the circuit and variables (no values) for the following.

- Sketch the frequency response (magnitude and phase)  $V_{out}/I_s$  for  $Z_L \rightarrow \infty$ .
- Sketch the frequency response (magnitude and phase)  $V_{out}/I_s$  together with the unloaded response (part a) for the two conditions
  - $Z_L = C_L$
  - $Z_L = R_L$
- Sketch the transient response of  $V_{out}$  for  $I_s$  as a current step from 0 to  $I_{max}$  ( $Z_L \rightarrow \infty$ ).

### Problem 3: Sampling, settling, power dissipation



The clock waveform shown above is used to drive the switch open and closed ( $clk = 1 \rightarrow$  switch closed,  $clk = 0 \rightarrow$  switch open).  $T_{clk}$  is the clock period (50% duty cycle), where  $T_{clk} = 1/f_{clk}$ .  $V_{in} = 1V$ ,  $R = 100\ \Omega$ , and  $C = 10\text{ pF}$

- What is the maximum clock frequency,  $f_{clk}$ , that allows 0.1% settling precision of  $V_{cap}$  each period?
- Given this clock frequency, what is the average current delivered to the capacitor?
- Verify your answers to a) and b) using Ltspice. To do this using a DC source for  $V_{in}$ , you need to use an initial condition (0V) on  $V_{cap}$ . Include any relevant plots in your submission.
- Perform an AC simulation on the circuit in Ltspice (switch closed). Relate the frequency response to the settling time and include any relevant plots.