EE P 538
Analog Circuits for Sensor Systems

Spring 2020

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Announcements

- Assignment 2 due Saturday, April 18 at midnight
- Assignment 3 will be posted April 17
  - Due Saturday, April 25 at midnight

Week 3

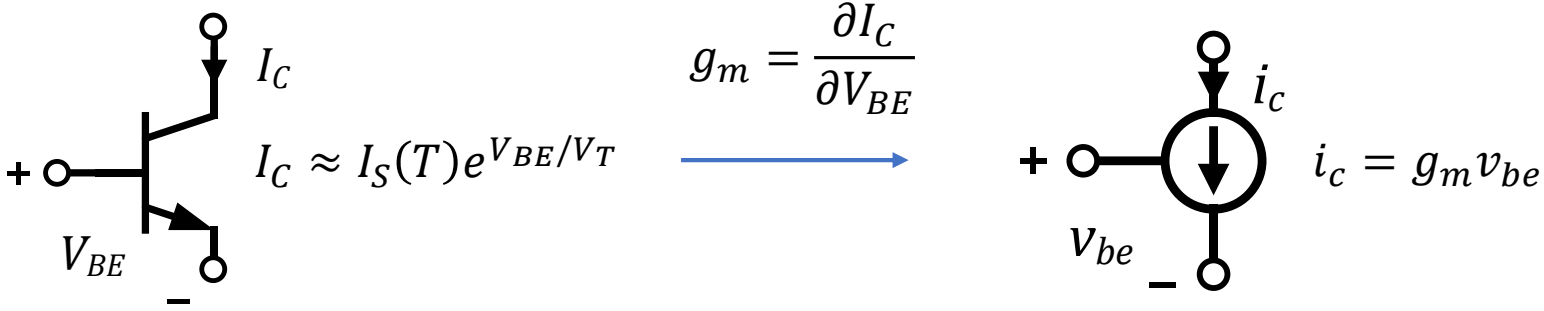
- AoE Chapter 2 – Bipolar Transistors
  - 2.3, 2.4.2, 2.4.4
- AoE Chapter 3 – Field Effect Transistors
  - 3.1 – 3.4

Overview

- Last time…
  - Constant V_{BE} BJT model
  - Ebers–Moll BJT model
  - Emitter follower and common emitter amplifiers
  - Small-signal model of a BJT
- Today…
  - Small-signal BJT model
  - Current sources
  - Differential amplifiers
  - Field effect transistors
  - Small-signal model of a MOSFET

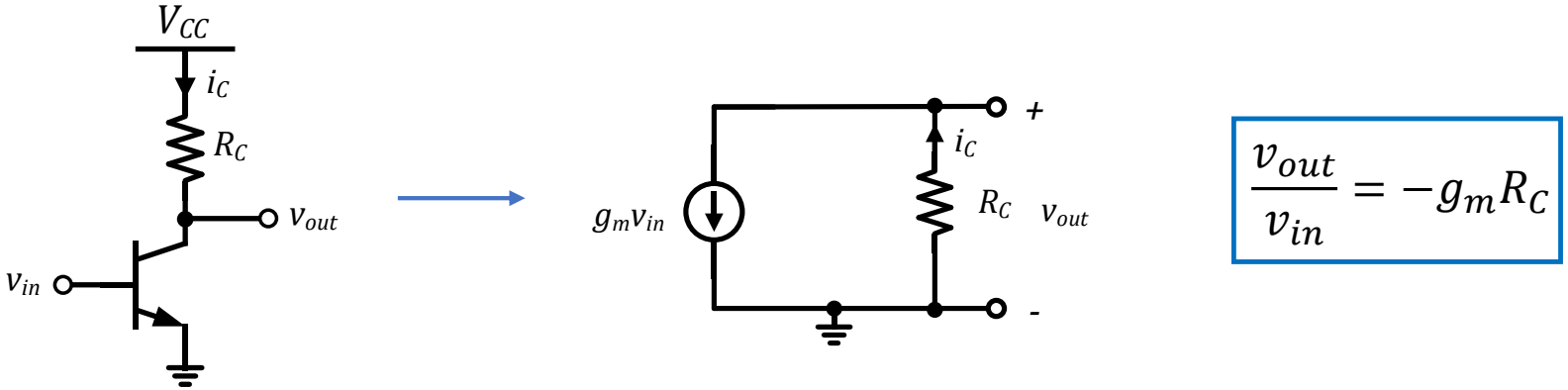
Lecture 3 – Transistors 2

Small-Signal Transconductance



- The Ebers–Moll model describes the behavior of collector current with respect to base-emitter voltage (large signal)
- g_m (the m stands from mutual) describes how the collector current responds to *small changes* in base-emitter voltage (small signal)
- Linear circuit design is based on this *small-signal approximation*

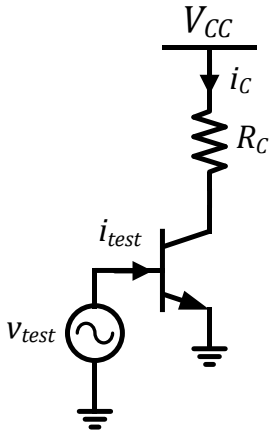
Realizing Voltage Gain



$$\frac{v_{out}}{v_{in}} = -g_m R_C$$

- The common-emitter amplifier exemplifies how we achieve voltage gain in circuits:
  1. Input voltage is use to generate a current via transconductance
  2. Output voltage is the product of current and resistance
- This is the method by which gain is realized in circuits based on BJT's, FET's, and even vacuum tubes

CE Input Impedance



$$i_c = g_m v_{test}$$

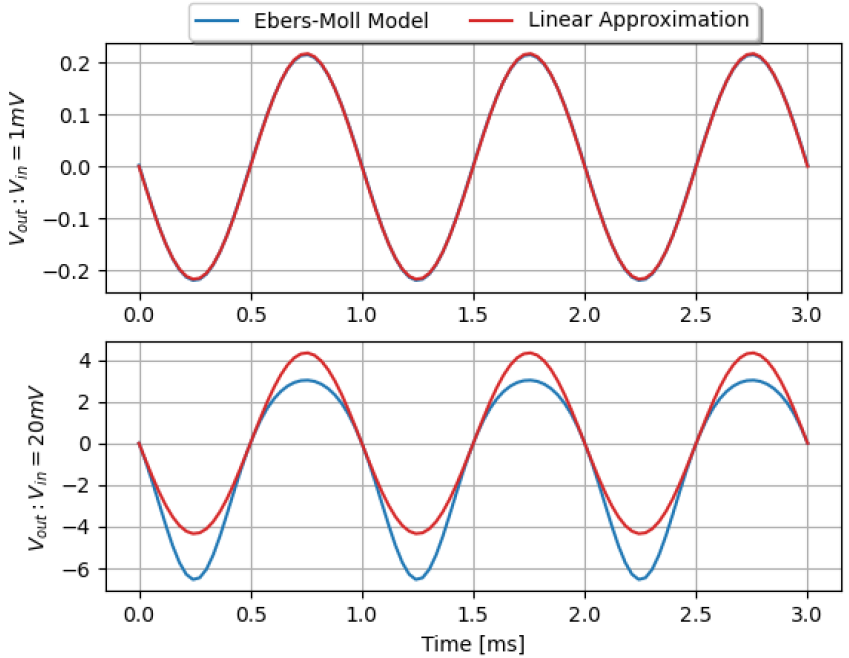
$$i_b = i_{test} = \frac{i_c}{\beta} = \frac{g_m v_{test}}{\beta}$$

$$r_{in} = \frac{v_{test}}{i_{test}} = \boxed{\frac{\beta}{g_m}}$$

- The impedance “looking into” the base is β times higher that that looking into the emitter
- This may be unacceptably low for applications requiring high input impedance (e.g. sensor with high equivalent impedance)
- Field-effect transistors exhibit much higher input impedance (up to tera-ohms and more), and thus may be preferred for such applications

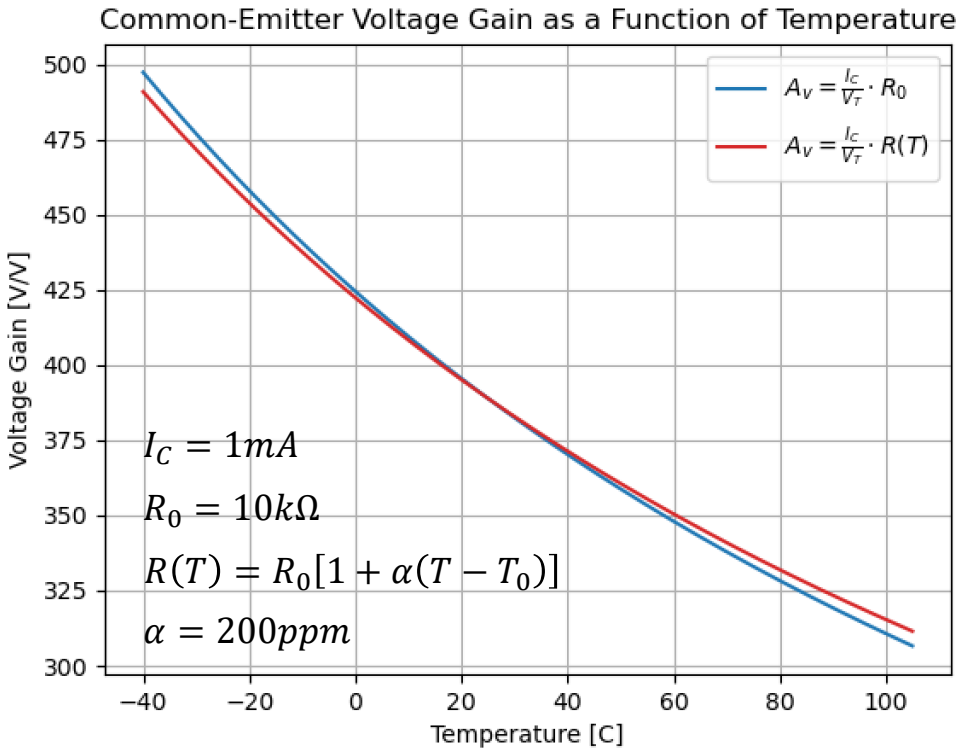
CE Nonlinearity

- Larger signal amplitudes cause nonlinear “distortion” in the output, due to the exponential relationship between V_{BE} and I_C
- As seen here, this is apparent for even moderate signal amplitudes
- The amount of distortion can be better quantified in the frequency domain using a Fourier transform
- CE distortion (Ltspice)

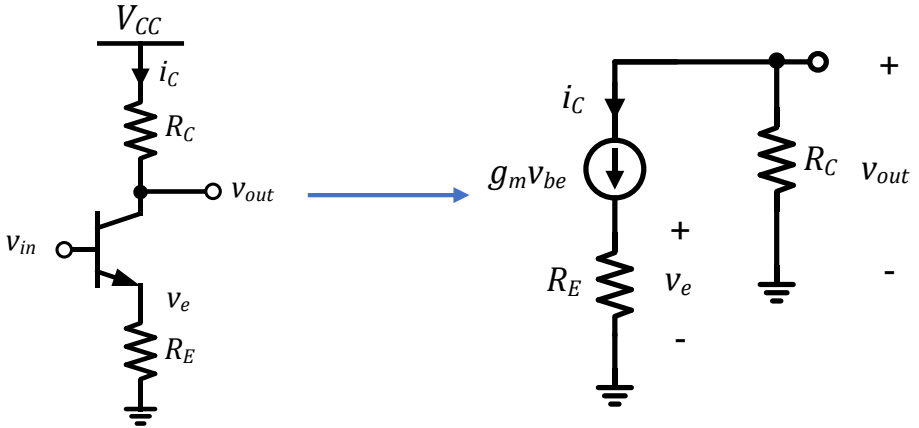


CE Gain Temperature Dependence

- Both g_m and resistance vary with temperature
- Over typical specified temperature ranges (e.g. industrial or military spec), the common-emitter gain varies substantially ($\pm$ 25%)
- Is it possible to ensure consistent gain over a wide temperature range?



Emitter Degeneration



$$v_{in} \uparrow \Rightarrow v_e \uparrow \Rightarrow i_c \downarrow$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_m}{1 + g_m R_E} R_C \approx \boxed{-\frac{R_C}{R_E}}$$

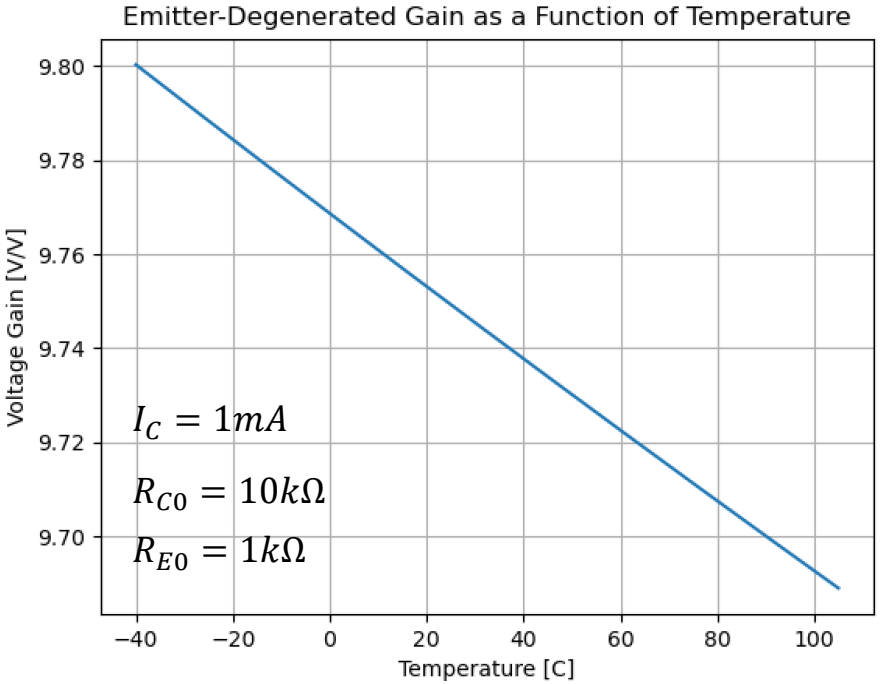
- The "degenerated" common emitter amplifier employs feedback:

1. As the input voltage increases, so does the current (i_c)
2. The increase in produces an increase in the emitter voltage (v_e) proportional to R_E
3. This decreases i_c, leading to a dependence of gain on R_E

Temperature Performance

- Through the use a feedback, we are able to reduce the gain variability from ± 25% to ± 0.6%
- This comes at a cost, as the gain has been reduced from 400 V/V to 10 V/V
- This is central to the use of feedback in engineered systems:

We employ high open-loop gain and feedback to achieve precise closed-loop control



Early Effect

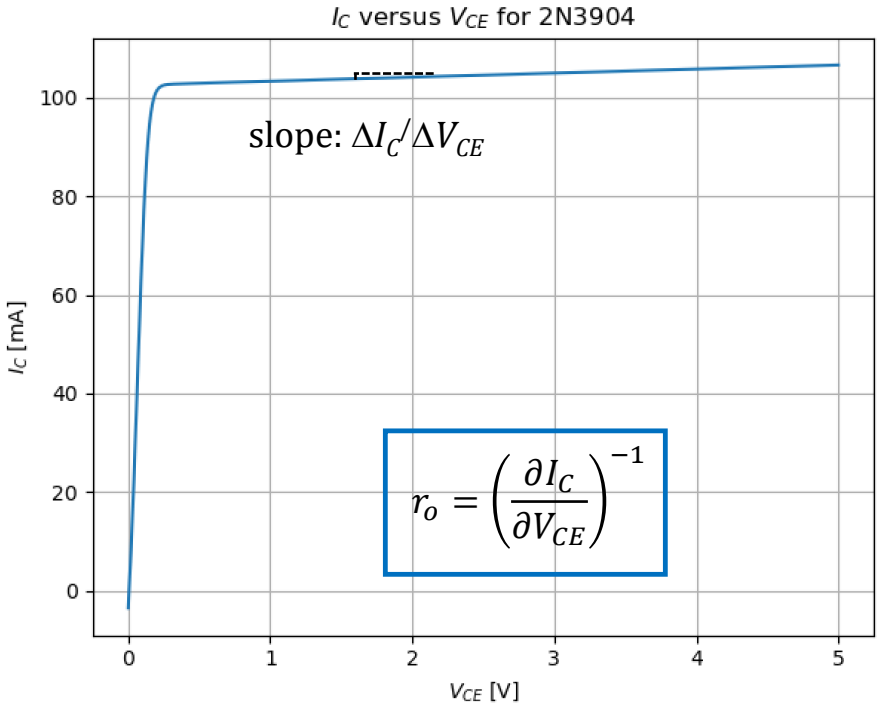
- According to the model we've employed so far, I_C depends only on V_{BE} and is independent of V_{CE}
- In reality, the collector current has a slight dependence on V_{CE}
- This dependence is due to the variation of base width as V_{CE} changes
- The variation of I_C with V_{CE} is captured by the Early voltage (V_A)
- The collector current is thus expressed as

$$I_C = I_{C0}\left(1 + \frac{V_{CE}}{V_A}\right),$$

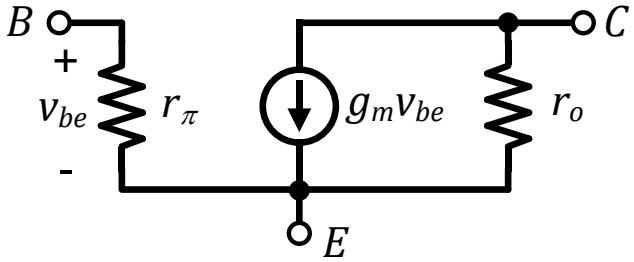
where $\quad I_{C0} = I_S\left(e^{V_{BE}/V_T} - 1\right)$

Output Resistance

- For values of V_{CE} above a few 10's of mV, the collector current varies approximately linearly
- We capture this dependence with the *small-signal resistance* r_o, called the *output resistance*
- r_o depends on the DC collector current, so a given value of r_o is only valid only a narrow signal range (small-signal assumption)
- 2N3904 DC sweep (Ltspice)



Hybrid-pi BJT Model

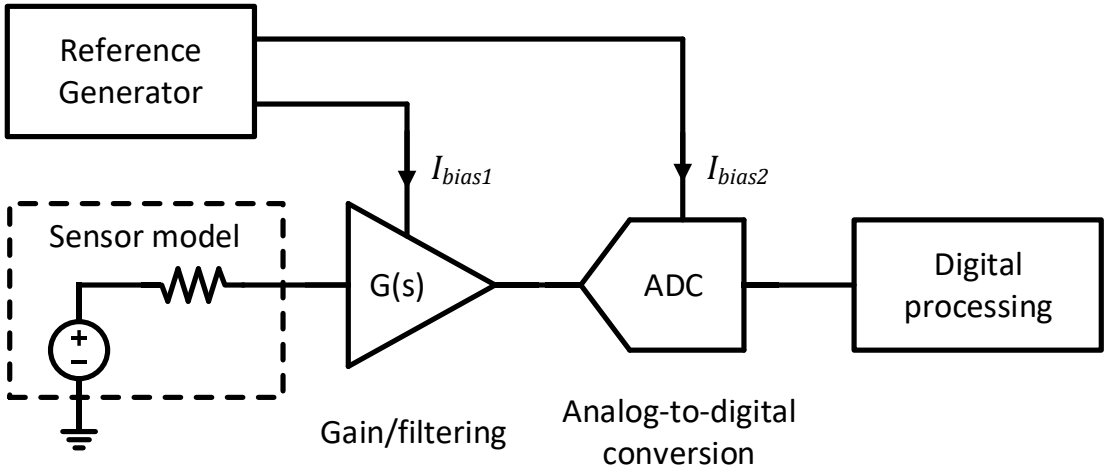


$$g_m = \frac{I_{C0}}{V_T} \qquad r_o = \frac{V_A}{I_{C0}}$$

$$r_\pi = \frac{\beta}{g_m}$$

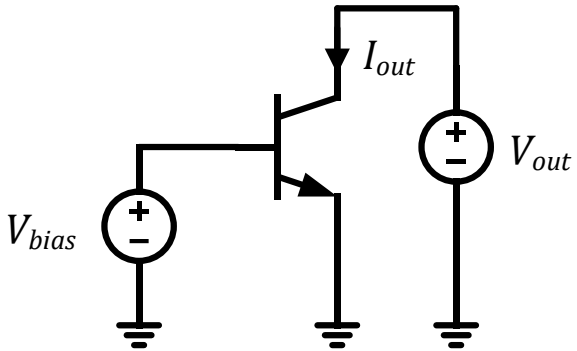
- The improved small-signal model includes the linear transconductance (g_m), base resistance (r_π), and the output resistance (r_o)
- This model is adequate for “hand” analysis for a wide range of applications of linear analog circuits
- Note that the product $g_m r_o$ is the “intrinsic gain” of the transistor, and represents the transistor gain with no external load

Analog Circuit Biasing



- Nearly all analog circuits utilize some form of current bias
- This is largely due to the dependence of critical circuit parameters (e.g. g_m) on current
- For this reason, the availability of good current sources is essential to analog design

BJT Current Source

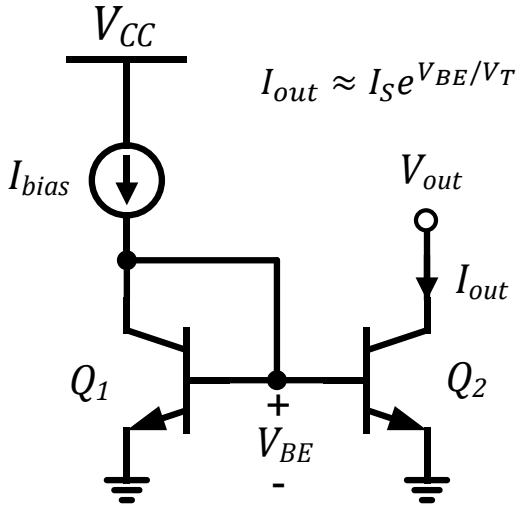


$$R_{out} = r_o \approx \frac{V_A}{I_{out}}$$

$$\frac{\Delta I_{out}}{I_{out}} = \frac{\Delta V_{out}}{I_{out} r_{out}} = \frac{\Delta V_{out}}{V_A}$$

- A higher value of V_A corresponds to a higher output resistance
- Consequently, the *precision* of the output current also depends on Early voltage, which is a device parameter
- Typical values of V_A are from ~50V to several hundred
- How do we generate the bias voltage V_{bias}?

Current Mirror

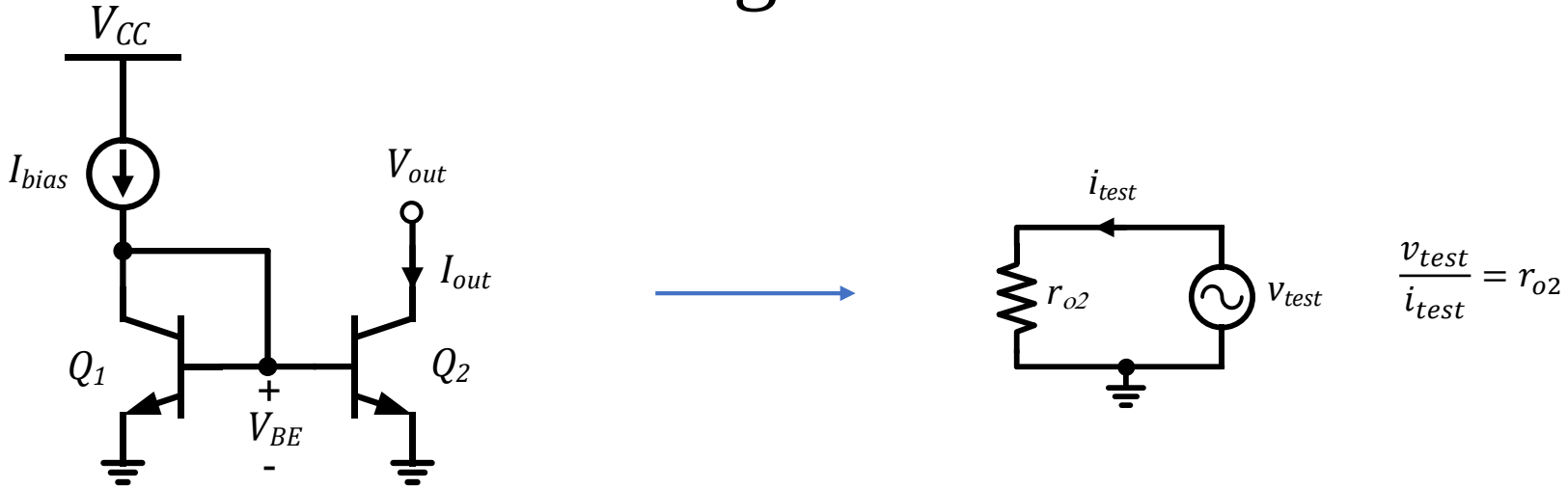


$$I_{out} \approx I_S e^{V_{BE}/V_T} \approx I_{bias}$$

$$V_{BE} \approx V_T \ln \frac{I_{bias}}{I_S}$$

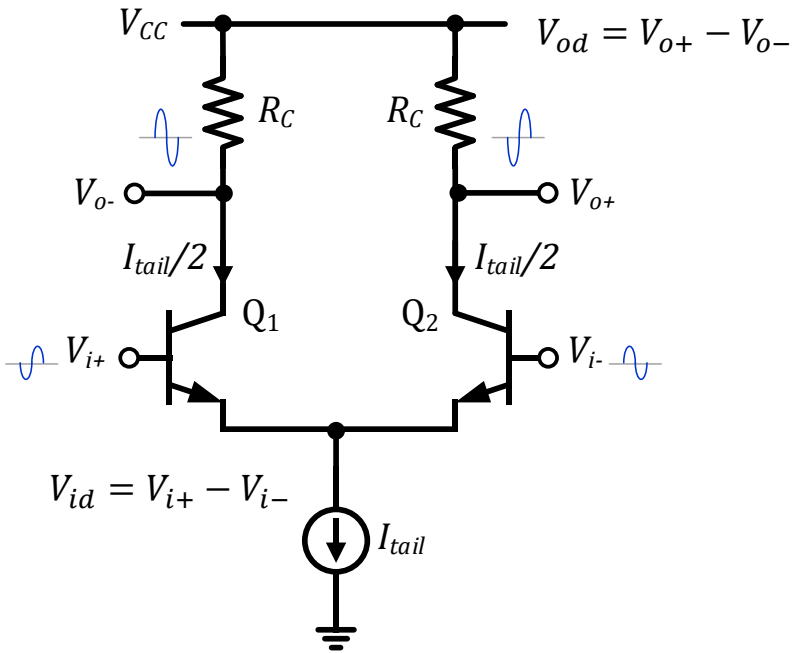
- Q_1 "compresses" Ibias into V_{BE} via a logarithmic relationship
- Q_2 "expands" V_{BE} into Iout via an exponential one
- A current mirror is an example of a *translinear circuit*, as the linear relationship between input and output is accomplished via nonlinear device operation
- Current Mirror (Ltspice)
- How do we generate I_{bias}?

Small-Signal Model



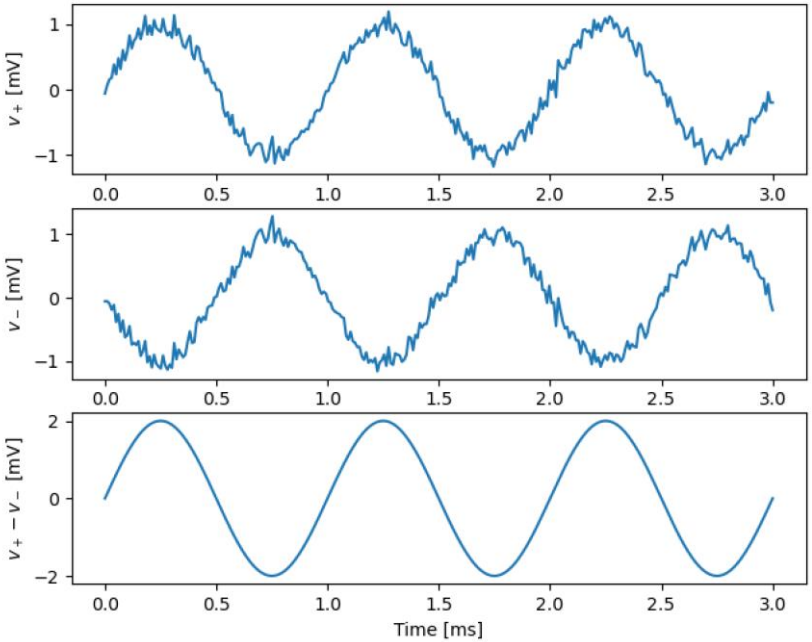
- As always, DC voltages and currents become zero
- Because the small-signal base voltage of Q_2 is zero, no current flows through its transconductance
- The equivalent circuit at the output is just Q_2's output resistance

Differential Amplifiers



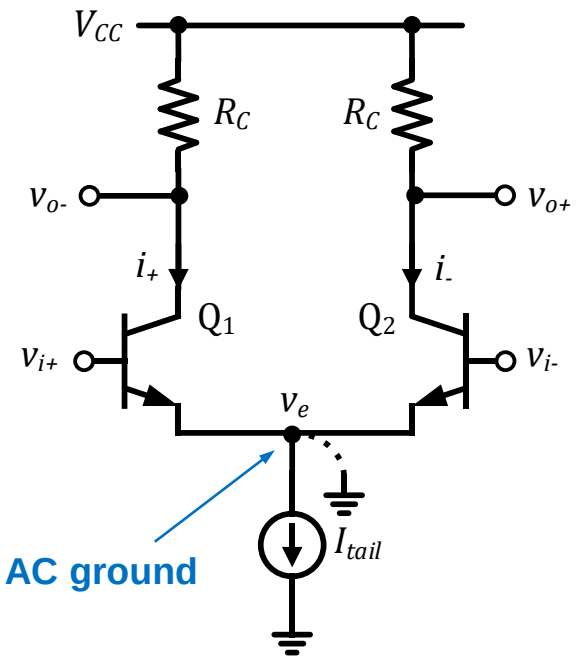
- Differential amplifiers process *differential signals*, or signals encoded as the difference between two voltages (or currents)
- An advantage of differential amplifiers is their rejection of *common-mode signals*
- The differential gain is defined as the ratio of differential output voltage to differential input voltage

Differential Signaling



- Differential signaling provides an inherent immunity to “noise” that affects both signals equally
- The signal is always encoded as the difference between two voltages or currents with opposite phases
- When their difference is taken, the *signal* adds constructively and the *common-mode noise* is removed

Half-Circuit Analysis



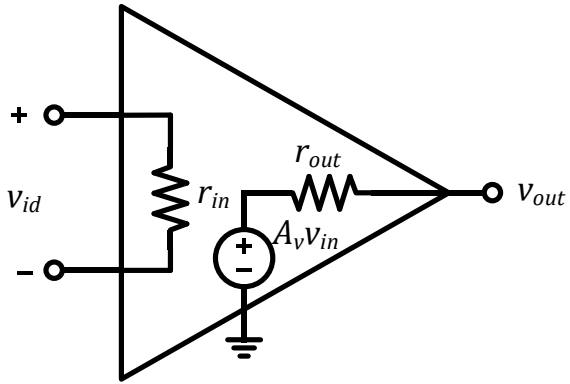
$$i_+ = -i_- = g_m v_{i+} = g_m \frac{v_{id}}{2}$$

$$g_m = \frac{I_{tail}}{2V_T} \qquad v_e = 0$$

$$v_{o-} = -g_m \frac{v_{id}}{2} R_C \qquad v_{o+} = g_m \frac{v_{id}}{2} R_C$$

$$\boxed{v_{od} = v_{o+} - v_{o-} = -g_m v_{id} R_C}$$

Ideal Opamp



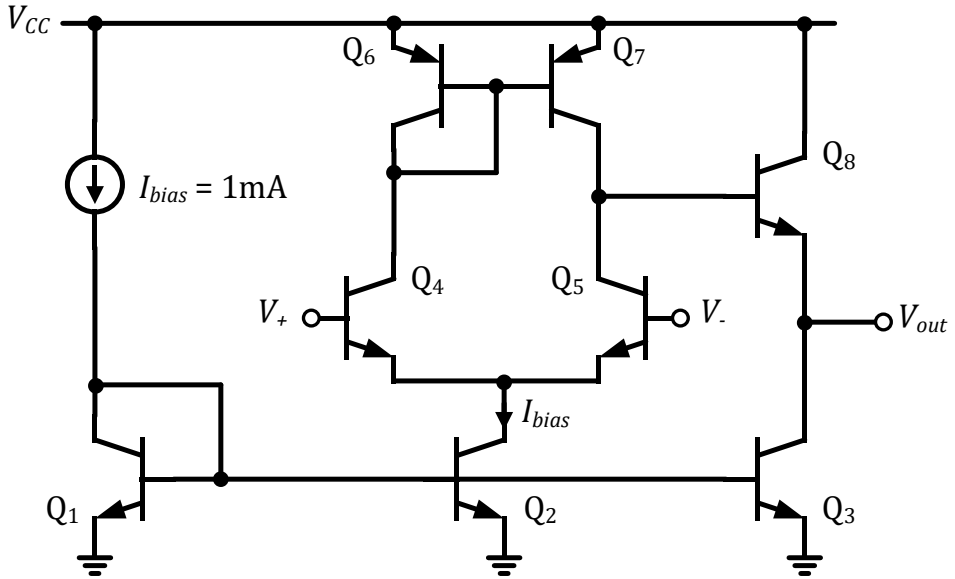
$$A_v \to \infty$$

$$r_{out} \to 0$$

$$r_{in} \to \infty$$

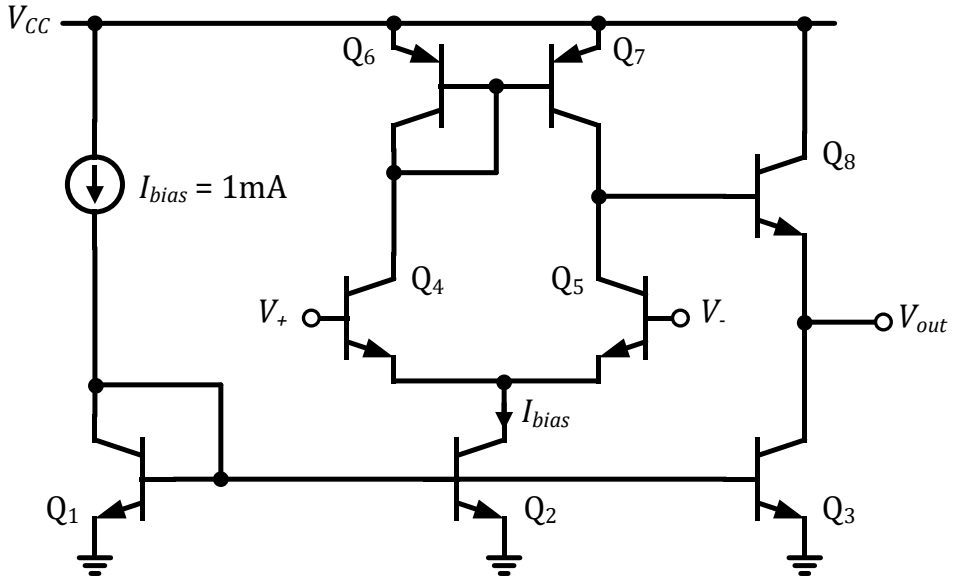
- Opamps (typically) have differential inputs and single-ended outputs
- The desirable characteristics of an opamp are:
  a) High open-loop gain
  b) Low output impedance
  c) High input-impedance

Simple Opamp



- Q_1 – Q_3 form *current mirrors,* biasing the amplifier
- Q_4 and Q_5 are *transconductors*, which realize gain
- Q_6 and Q_7 form an *active load*, converting the differential input signal to a single-ended voltage
- What about Q_8?

How does it stack up?

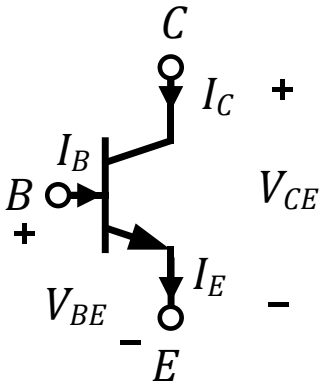


$$A_v \approx \frac{g_m r_o}{2} = \frac{I_{bias}}{2V_T}\frac{V_A}{I_{bias}} = \frac{V_A}{2V_T} \approx 1000\frac{V}{V}$$

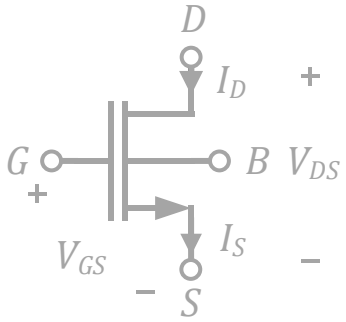
$$r_{out} \approx \frac{1}{g_{m8}} = \frac{V_T}{I_{bias}} \approx 25\Omega$$

$$r_{in} = r_{\pi 4,5} = \frac{\beta}{g_{m4,5}} = \frac{2\beta V_T}{I_{bias}} \approx 5k\Omega$$

BJT Operation



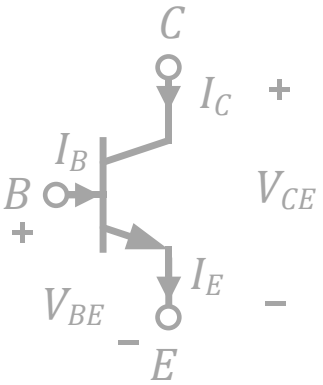
$$I_C = f(V_{BE}, V_{CE})$$



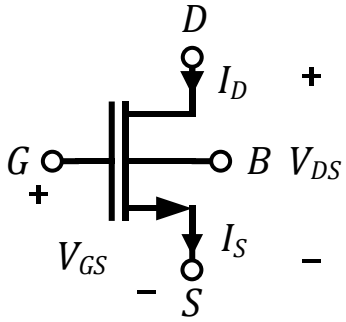
$$I_D = f(V_{GS}, V_{DS})$$

- For current to flow in a BJT, we need to overcome the “potential barrier” formed by the base-emitter junction diode
- Beyond this threshold (~0.6V), charge carriers are injected into base region as a exponential function of V_{BE}
- The base current is “amplified” in the collector by a roughly constant factor β

FET Operation



$I_C = f(V_{BE}, V_{CE})$

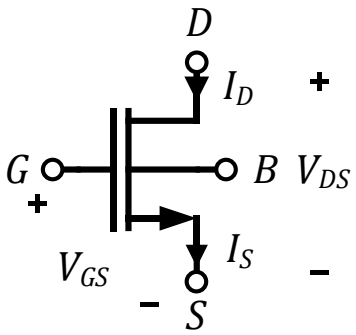


$I_D = f(V_{GS}, V_{DS})$

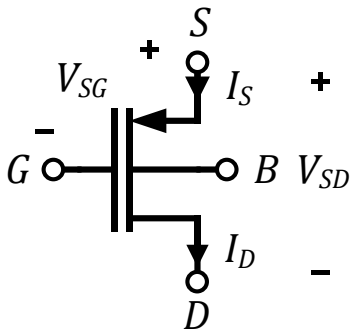
- Conduction in a FET (**F**ield-**E**ffect **T**ransistor) occurs in a conducting channel formed by an electric field
- The absence of a forward biased junction (V_{BE} in the BJT) means that the *gate draws no current*
- The high input impedance (up to tera-ohms and above) is the FET's *most essential characteristic*, important for many applications

FET Flavors

N-channel

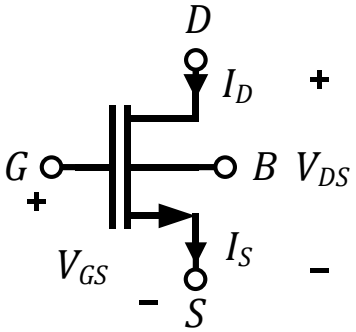


P-channel



- In an n-channel FET, conduction occurs as the movement of electrons
  - In normal operation, drain is at a higher potential than the source
- In a p-channel FET, “holes” are the charge carriers
  - Source has a higher potential than the drain in normal operation
- As with BJT’s, p-type FET’s typically perform worse than n-type

Enhancement-mode MOSFET

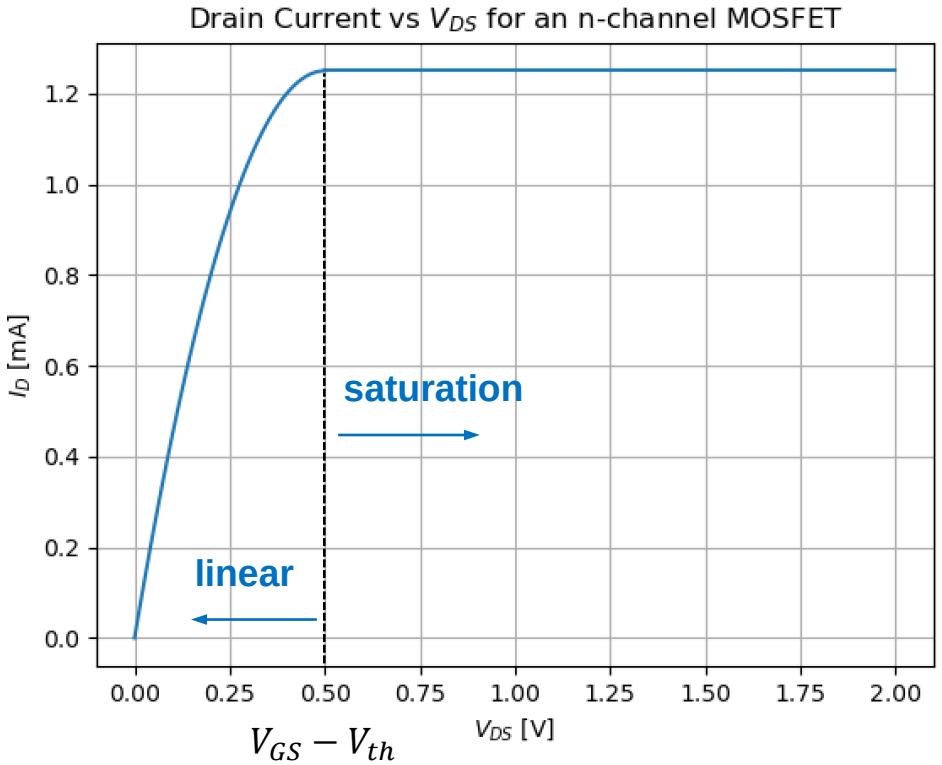


for $V_{DS} < V_{GS} - V_{th}$, $I_D = 2\kappa\left[(V_{GS} - V_{th})V_{DS} - \frac{{V_{DS}}^2}{2}\right]$ (linear region)

for $V_{DS} > V_{GS} - V_{th}$, $I_D = \kappa(V_{GS} - V_{th})^2$ (saturation region)

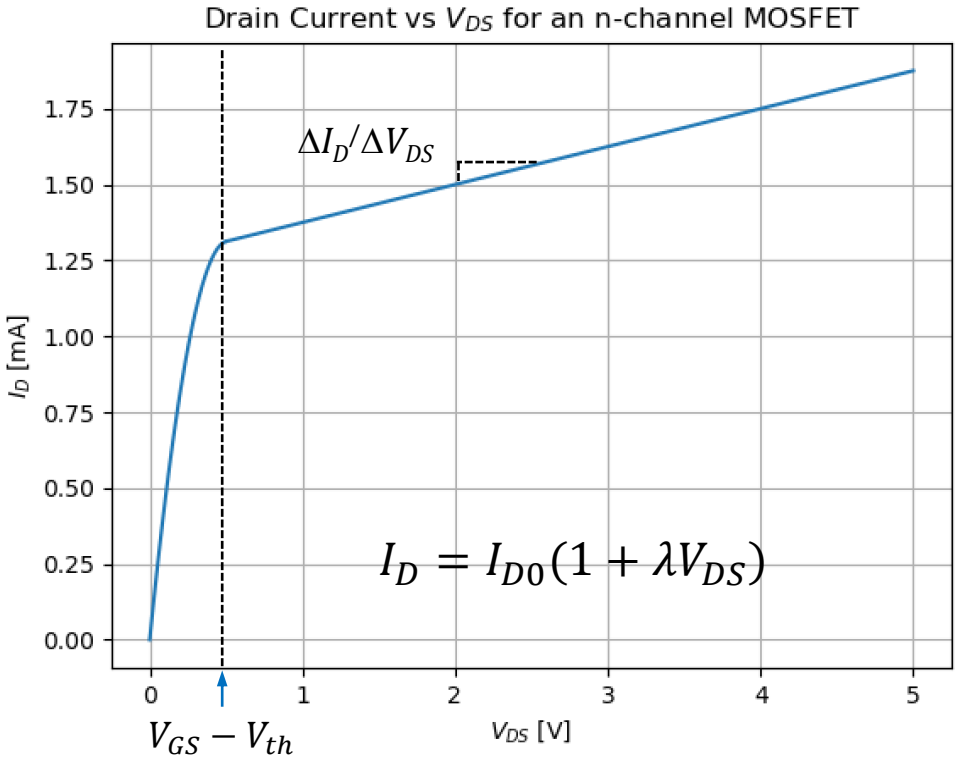
- "Enhancement-mode" just means that the bulk semiconductor is doped to limit conduction to gate-source voltages above V_{th}
- The two regions of operation are used for different applications:
  - *Linear region*: Switches, logic gates, and (sometimes) resistors
  - *Saturation region*: Amplifiers, current sources

Regions of Operation



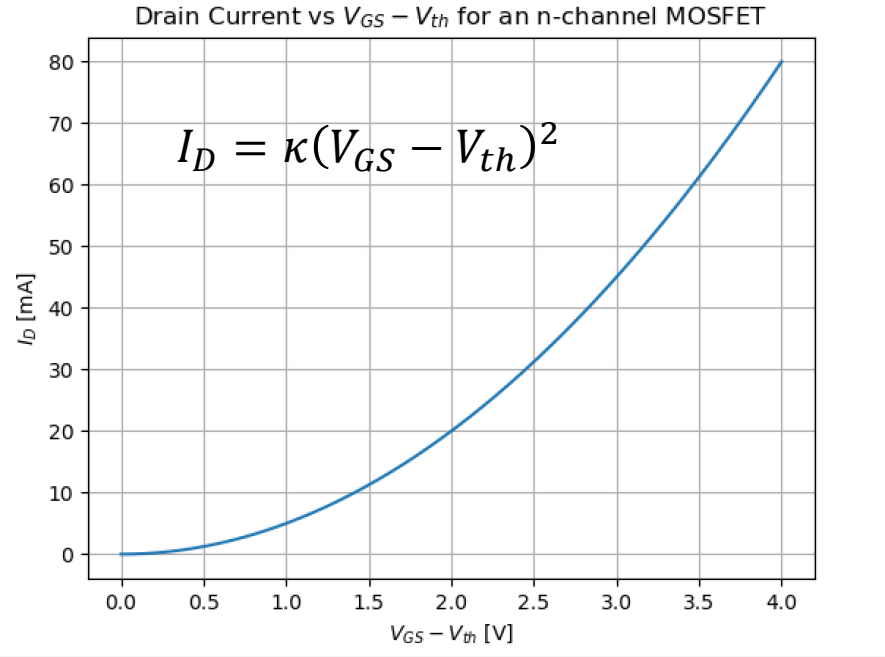
- At low values of V_{DS}, I_D is approximately linear with V_{DS}
- Above the critical value $V_{GS} - V_{th}$, the conducting channel becomes "pinched off" and I_D is (approximately) constant with V_{DS}
- For linear circuits, we typically operate FETs in the saturation region, due to the high output resistance there ("good" transconductor)

Dependence on V_{DS}

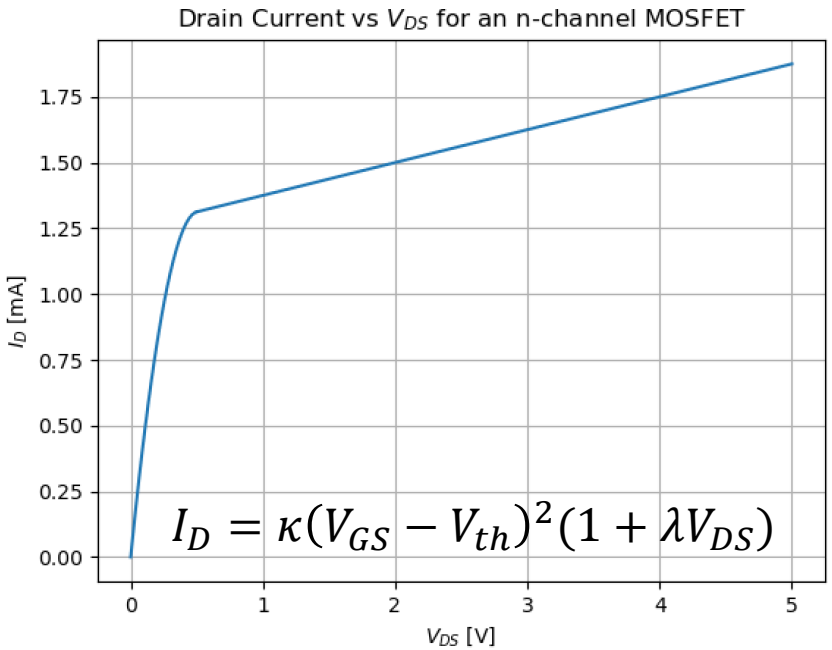


- Due to a number of contributing effects, drain current varies slightly with V_{DS} (similar to BJT's)
- The combination of effects is often referred to as "channel-length modulation," due to the variation of the conducting channel length with V_{DS}
- Thus, similar to BJT's, FET's exhibit *finite output resistance*, which sets limits on their performance as current sources

MOSFET I-V Characteristics



V_{GS} dependence



V_{DS} dependence

Small-Signal Transconductance

- As with the BJT (or any transconductance device), g_m is defined as the derivative of drain current with respect to gate-source voltage:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}} \kappa (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) = 2\kappa (V_{GS} - V_{th})$$

- g_m can be expressed in terms of drain current:

$$g_m = 2\kappa (V_{GS} - V_{th}) = \frac{2I_{D0}}{(V_{GS} - V_{th})}$$

- Again, we have a linear dependence of g_m on current

Output Resistance in Saturation

- As with the BJT, the dependence of FET drain current on VDS is captured by a scalar λ
- The drain current can be defined as

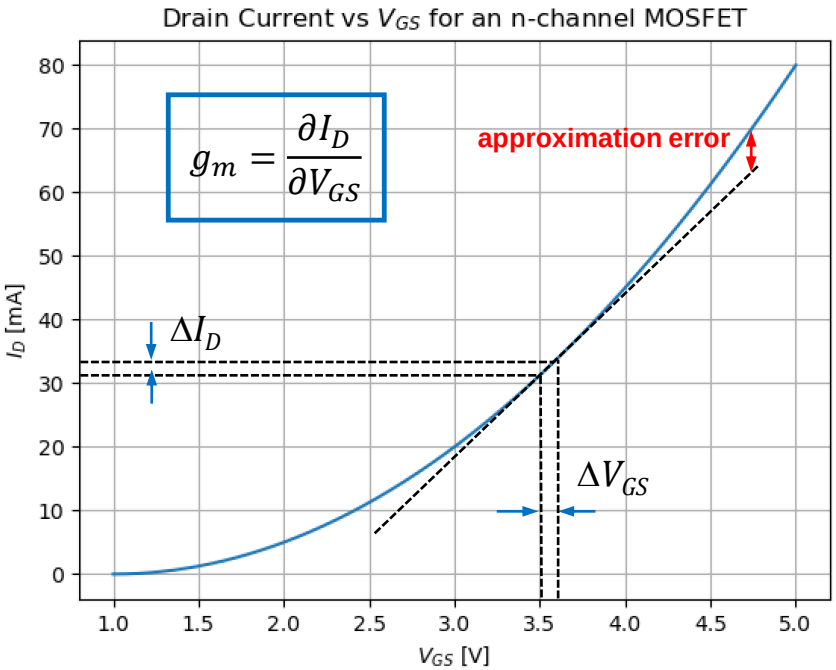
$$I_D = I_{D0}(1 + \lambda V_{DS}), \quad \text{where} \quad I_{D0} = \kappa(V_{GS} - V_{th})^2$$

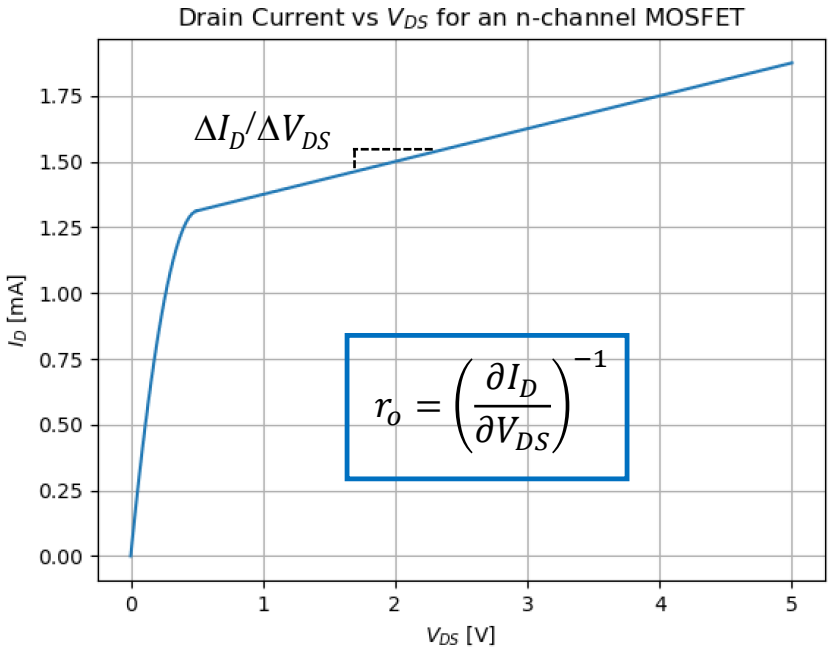
- The output resistance is thus

$$r_o = \frac{\partial I_D}{\partial V_{DS}} = \frac{1}{\lambda I_{D0}}$$

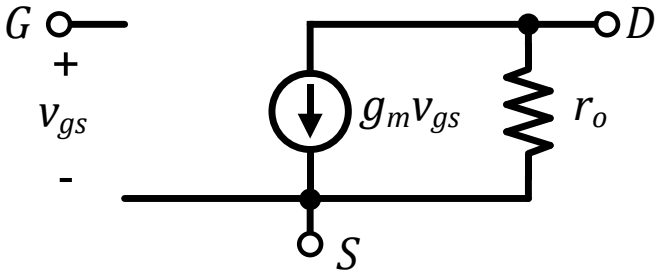
- A typical value of λ for an integrated MOSFET is around $0.1V^{-1}$, though this can vary considerably

Small-Signal Model





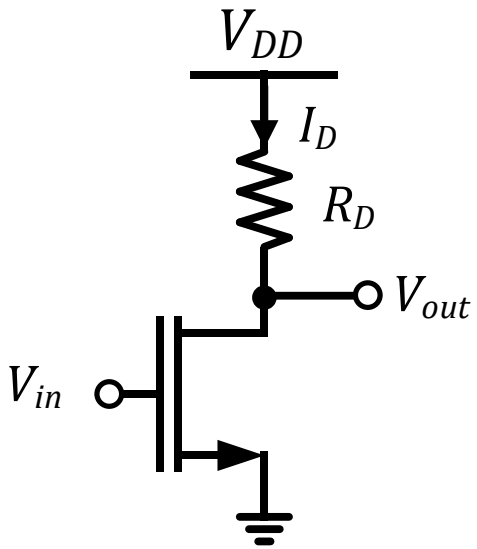
Hybrid-pi FET Model



$$g_m = \frac{2I_{D0}}{V_{GS} - V_{th}} \qquad r_o = \frac{1}{\lambda I_{D0}}$$

- The DC small-signal model of the FET is similar to the BJT, but lacks the r_π parameter (high input impedance)
- Again, this model is sufficiently accurate for many applications
- The product $g_m r_o$ is the “intrinsic gain” of the transistor, and represents the transistor gain with no external load

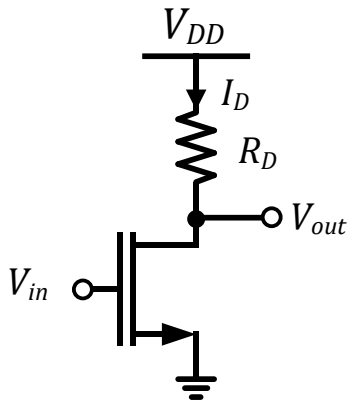
Common-Source Amplifier



- High-gain structure, essentially identical to the common-emitter amplifier
- High gate impedance of FET devices makes it ideal for interfacing with sensors with high source resistance
- For higher gain, R_D can be replaced by an “active load,” which is p-channel FET in saturation

Small-Signal Approach

DC operating point



$$I_D = I_{D0}(1 + \lambda V_{DS})$$

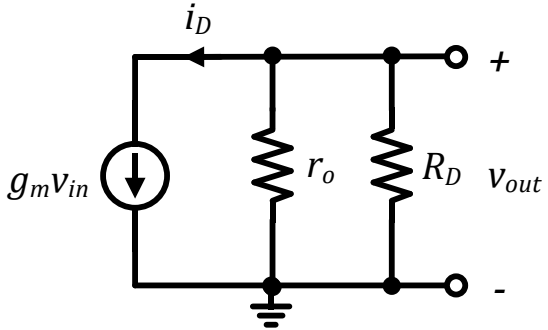
$$V_{OUT} = V_{CC} - I_D R_D$$

Small-signal model

$$g_m = \frac{2I_{D0}}{V_{GS} - V_{th}}$$

$$r_o = \frac{1}{\lambda I_{D0}}$$

Small-signal analysis



$$i_D = g_m v_{in} \qquad v_{out} = -i_D(r_o || R_D)$$

$$\frac{v_{out}}{v_{in}} = -g_m(r_o || R_D) \approx -g_m R_D$$