EE 538 Spring 2020
Analog Circuits for Sensor Systems
University of Washington Electrical & Computer Engineering

Instructor: Jason Silver
Homework #5 (40 points)
Due Saturday, May 9, Submit on Canvas

Please show your work.

Problem 1: Difference amplifier analysis

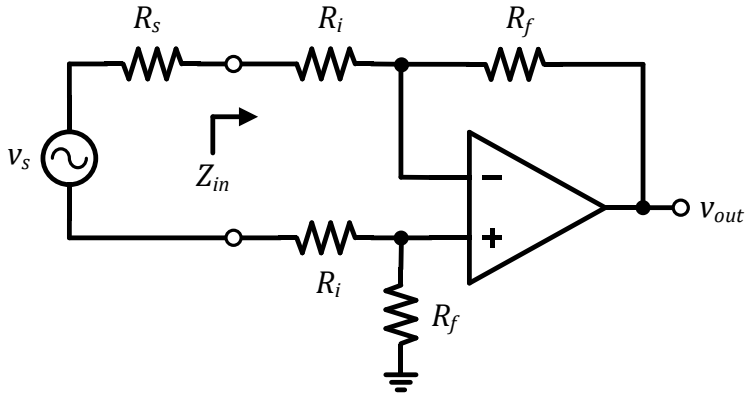

Figure 1. Difference amplifier

A difference amplifier is driven by a sensor with source impedance R_s. Let R_f = 10kΩ and R_i = 100Ω. Assume ideal opamp behavior.

a) (5 points) Derive an expression and determine a value for the DC differential input impedance Z_{in} of the amplifier. Determine the source impedance R_s that results in a maximum of 0.1% attenuation of the input voltage.
b) (5 points) Simulate the amplifier in Ltspice using the UniversalOpamp2 component (default parameters). Plot Z_{in} up to 10MHz using AC analysis to show how it varies as a function of opamp gain.

Problem 2: Instrumentation amplifier analysis

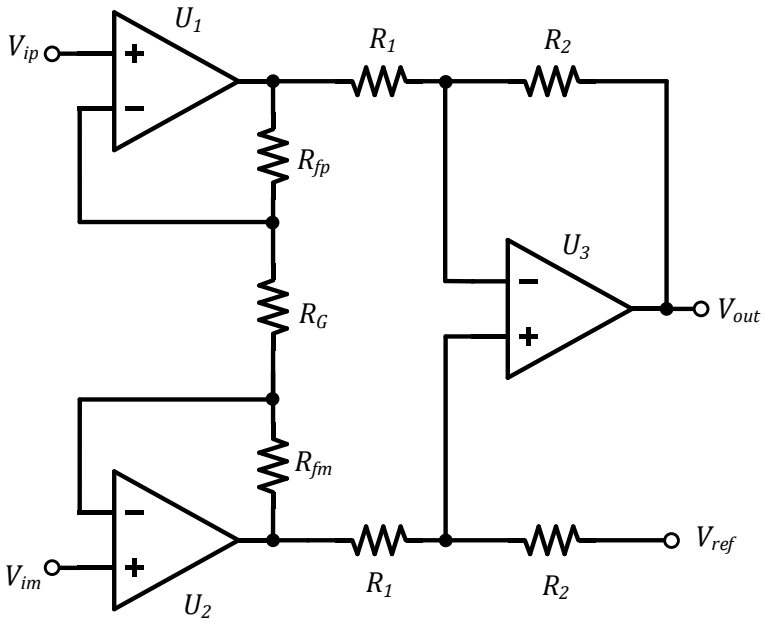

Figure 2. Instrumentation amplifier

Assume the above opamps have a DC gain of 120dB and an f_T of 1MHz. Nominal resistance values are R_{fp} = R_{fm} = 4.95kΩ, R_G = 100Ω, and R_1 = R_2 = 10kΩ, all with 0.1% tolerance.

a) (5 points) Determine the differential DC gain of the amplifier and the closed-loop bandwidth. *Ignore resistor mismatch.*

b) (5 points) Based on the value of f_T, what is the closed-loop gain error at 100Hz? *Ignore mismatch.*

c) (5 points) Including the effect of resistor mismatch, what are the CMRR and the worst-case DC gain error? *Assume infinite opamp open-loop gain.*

d) (5 points) Assume U_1 and U_2 have min/max input offset voltages of ±100μV but are otherwise identical. What is the maximum allowable offset of U_3 to achieve a *worst-case input-referred offset* (the offset at V_{out} divided by the differential gain) of 250μV? *Ignore resistor mismatch.*

e) (10 points) Simulate the instrumentation amplifier in Ltspice using the UniversalOpamp2 component with appropriate Avol, GBW, and Vos values. Provide the following in your submission:

1. Image of your schematic showing the DC operating point (DC voltages at all nodes). Use the worst-case mismatch condition for the resistors. How much is the offset affected by resistor mismatch?
2. Plot showing the closed loop gain error at 100Hz using WC analysis. You can do this by selecting 'list' for the sweep type under AC analysis. Note that you need to run 128 iterations (2^7, where 7 is the number of resistors) to cover all mismatch combinations. Compare the contributions to gain error from finite opamp gain and resistor mismatch (i.e. which effect is more significant?).
3. Bode plots demonstrating closed-loop differential gain/phase and closed-loop common-mode gain/phase. For common-mode gain you should use the worst-case mismatch condition for the resistors.