EE P 538
Analog Circuits for Sensor Systems

Spring 2020

Instructor: Jason Silver, PhD

Announcements

- Solutions for Assignment 2 are posted on Canvas
- Office hours moved to Friday at 7pm
- Assignment 3 due Saturday, April 25 at midnight
- Assignment 4 will be posted April 24
  - Due Saturday, May 2 at midnight

Week 4

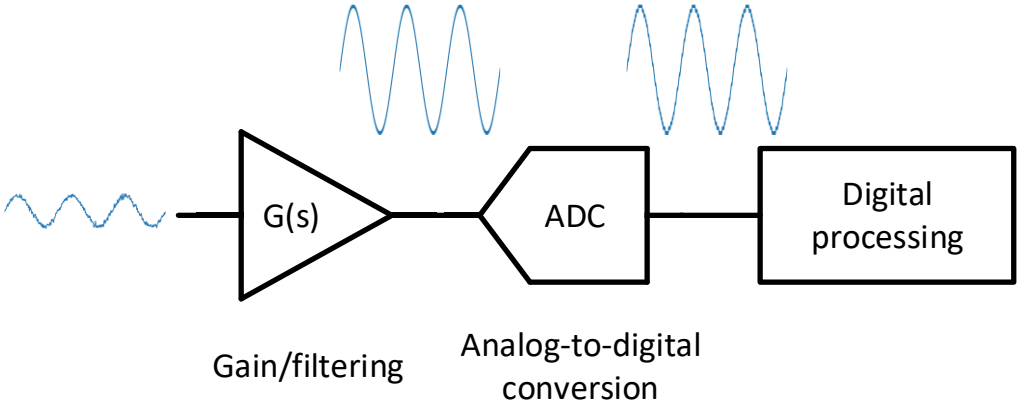
- AoE Section 2.5 – Negative Feedback
- AoE Chapter 4 – Operational Amplifiers

Overview

- Last time…
  - Small-signal BJT model
  - Current sources
  - Differential amplifiers
  - Field effect transistors
  - Small-signal model of a MOSFET
- Today…
  - Basic opamp behavior
  - Feedback
  - Frequency response
  - Non-ideal behavior

Lecture 4 – Opamps

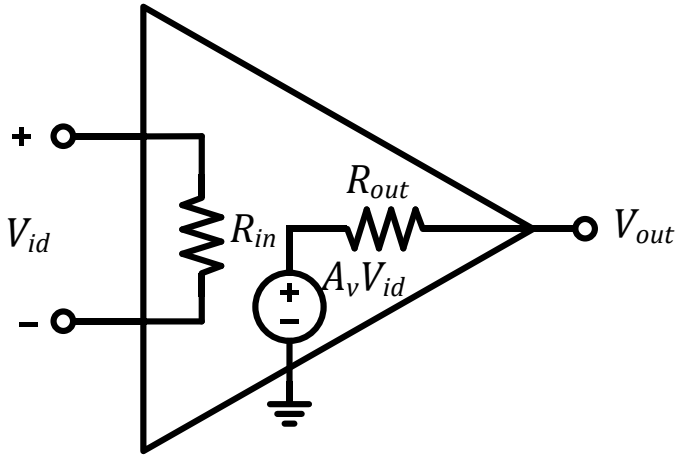
Analog Signal Conditioning



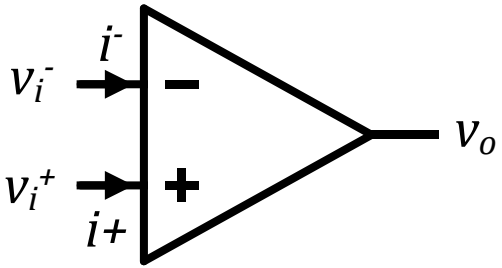
- The goal of signal conditioning is to prepare analog signals for analog-to-digital conversion while adding minimal noise
- Gain is used ensure that signals are optimized for ADC resolution and range, while filtering is required to ensure an acceptable signal-to-noise ratio (SNR)
- All components should be designed to minimize loading between stages

Ideal Opamp Characteristics

- Input impedance = ∞
- Output impedance = 0
- Voltage gain = ∞
- Common-mode rejection = ∞
- Offset voltage = 0
- No added noise
- Output can change instantaneously



Opamp “Golden Rules”



$$v_o = A_v\left(v_i^+ - v_i^-\right)$$

$$i_+ = i_- = 0$$

1. The output tries to do whatever it takes to make the voltage difference between the inputs zero
2. The inputs draw no current

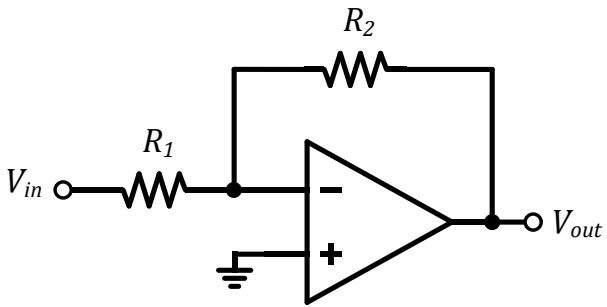
Opamp Design Caveats

1. Inputs and outputs should be within their prescribed ranges
   - Voltages outside these ranges can damage the opamp
2. Feedback should *always*[1] be negative and shouldn't introduce excessive phase shift
   - Phase lag in the feedback path can lead to oscillation!
3. Feedback is required at DC to set the operating point
   - This ties into 1, as the input voltage is otherwise ill-defined
4. Supply voltages should be bypassed with capacitors to avoid instabilities due to supply rail wiring inductance
   - Most important for opamps with wide bandwidths

[1]Electronic oscillators use positive feedback to compensate for energy losses in resonant structures, but this is outside the realm of linear circuit design.

Inverting/Non-inverting Amps

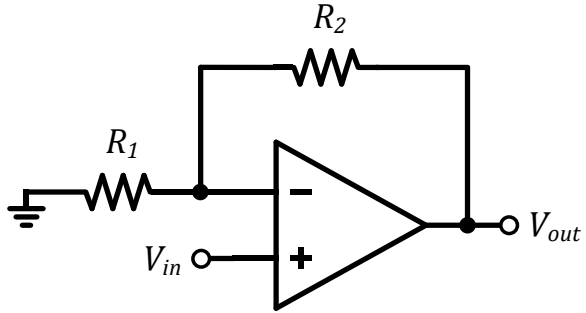
Inverting Amplifier



$$\frac{V_{in}}{R_1} = -\frac{V_{out}}{R_2}$$

$$\boxed{\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}}$$

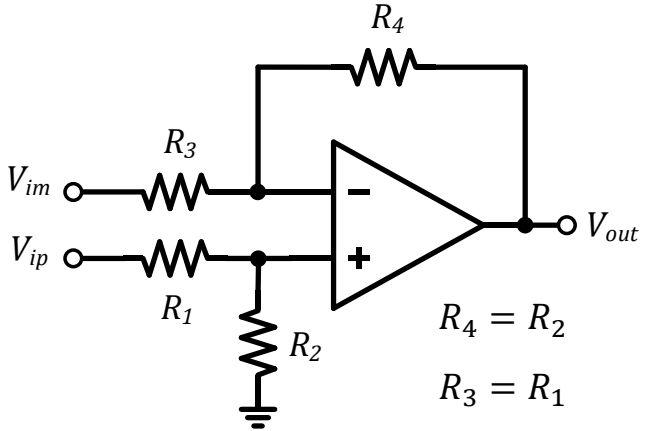
Non-inverting Amplifier



$$\frac{V_{in}}{R_1} = \frac{V_{out} - V_{in}}{R_2}$$

$$\boxed{\frac{V_{out}}{V_{in}} = \left(1 + \frac{R_2}{R_1}\right)}$$

Difference Amplifier

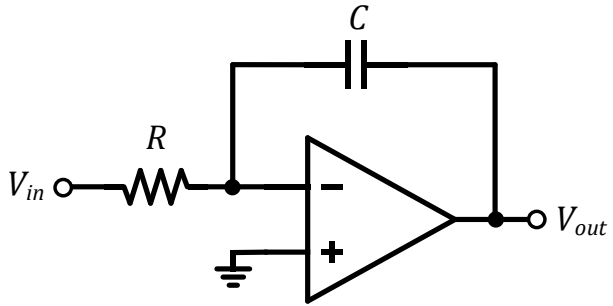


$$V_{out} = -\frac{R_2}{R_1}V_{im} + \frac{R_2}{R_1}V_{ip}$$

$$= \frac{R_2}{R_1}(V_{ip} - V_{im})$$

- R_1 and R_2 form a divider which sets the non-inverting terminal voltage
- V_{ip} sees an inverting gain, while V_{im} sees a non-inverting gain
- Output voltage can be determined by superposition
- Can be used to achieve gain or perform differential to single-ended conversion (or both)

Opamp Integrator

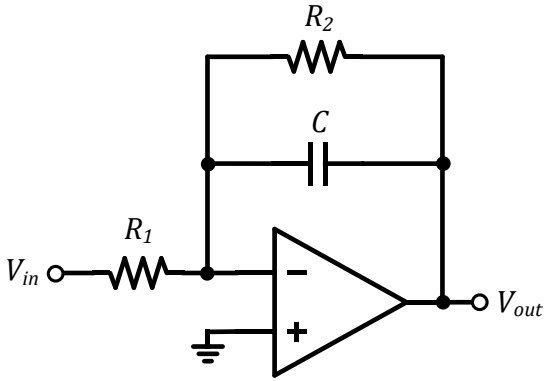


$$V_{out} = -\frac{Z_C}{R} V_{in} = -\frac{V_{in}}{sRC}$$

$$\Delta V_{out} = -\frac{V_{in}}{RC} \Delta t$$

- Opamps allow the design of *nearly* perfect integrators
- V_{in}/R is a constant current that is integrated onto C
- Avoids the restriction of V_{out} << V_{in} for RC “integrators”
- Requires feedback at DC to have stable operating point!

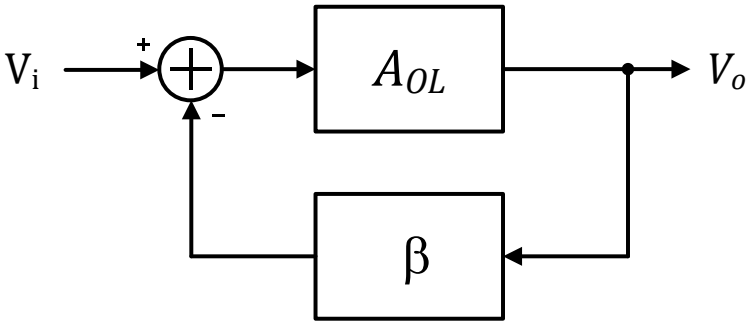
“Leaky” Integrator



$$\frac{V_{out}}{V_{in}} = -\frac{R_2 || \frac{1}{sC}}{R_1} = \frac{-R_2/R_1}{sCR_2 + 1}$$

- R_2 (or a reset switch, closed periodically) required to provide DC feedback
- At DC, the capacitor looks like an open circuit, so we just have an inverting amplifier
- At high frequency, the capacitor impedance dominates R_2, so the structure behaves like an integrator (with some leakage current through R_2)

Feedback

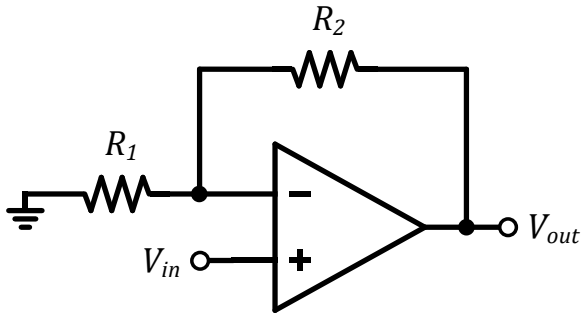


$$A_{CL} = \frac{V_o}{V_i} = \frac{A_{OL}}{1 + \beta A_{OL}}$$

$$as\ A_{OL} \to \infty, \quad A_{CL} \to \frac{1}{\beta}$$

- We use *negative* feedback to process the error $V_i - \beta V_o$, and A_{OL} should be "large" to minimize this error
- The combination of negative feedback and open-loop gain that is *high enough* desensitizes the transfer function to variations in open-loop gain
- The *feedback factor* β is the fraction of the output signal that is fed back to the input

Non-inverting Amplifier



$$v_i^- = \frac{R_1}{R_1 + R_2} V_{out} \longrightarrow \beta = \frac{R_1}{R_1 + R_2}$$

$$A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}} \approx \frac{1}{\beta} = 1 + \frac{R_2}{R_1}$$

- The output voltage, scaled by β, is fed back to the inverting terminal of the opamp
- The opamp *only processes the error voltage*, $v_i^+ - v_i^-$
  - This gives credence to our small-signal assumption when analyzing BJT/MOS circuits

Open-loop Frequency Response

- For internally-compensated opamps, the frequency response is approximately first-order (one pole) within the opamp's bandwidth
- The opamp bandwidth is its unity-gain, or transit, frequency ω_T
- The open-loop (DC) gain and bandwidth are related by the open-loop pole frequency:

$$\omega_T \approx A_0 \cdot \omega_{3dB}$$

Transfer function:

$$A_{OL}(j\omega) = \frac{A_0}{1 + j\omega\tau}$$

Magnitude:

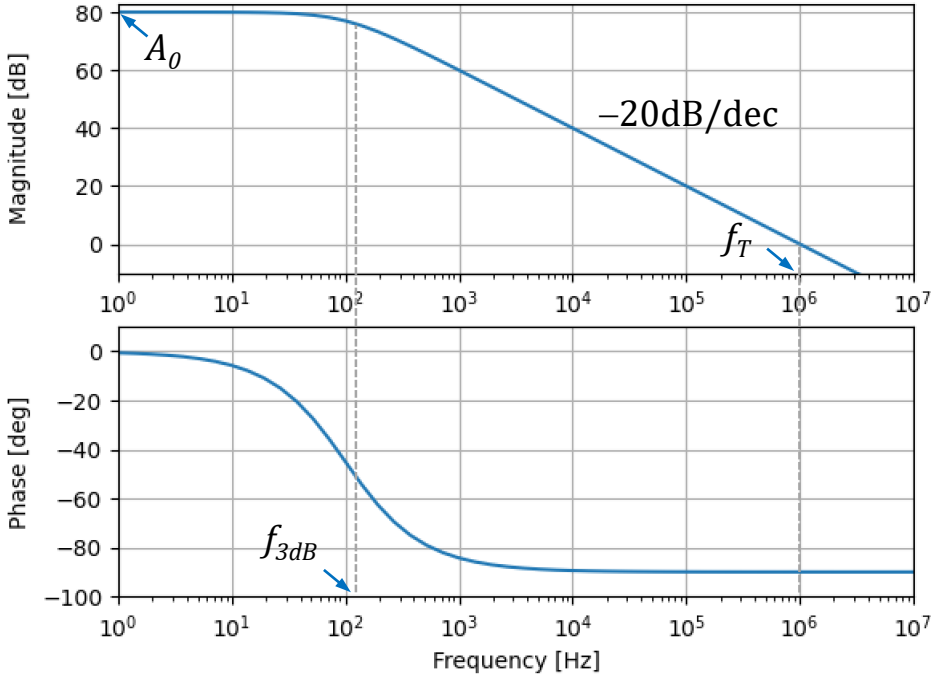
$$|A_{OL}(j\omega)| = \frac{A_0}{\sqrt{1 + \omega^2/\omega_{3dB}^2}}$$

Phase:

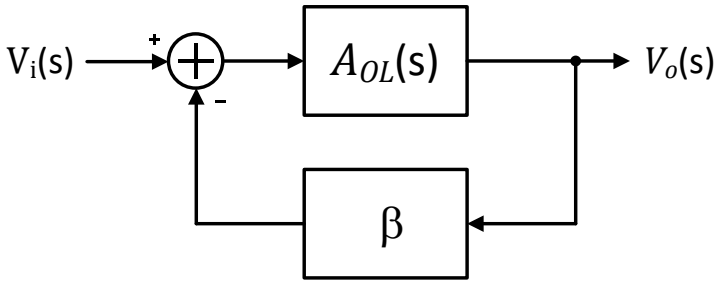
$$\angle A_{OL}(j\omega) = -\tan^{-1}\omega\tau$$

Open-loop Frequency Response

- As with any first-order system, the magnitude rolls off at 20dB per decade
- The single in-band pole results in 45° of phase lag at the pole frequency, f_{3dB}
- Beyond the unity-gain frequency (f_T), “non-dominant” poles create additional phase lag and steeper roll-off (not shown)



Closed-loop Frequency Response

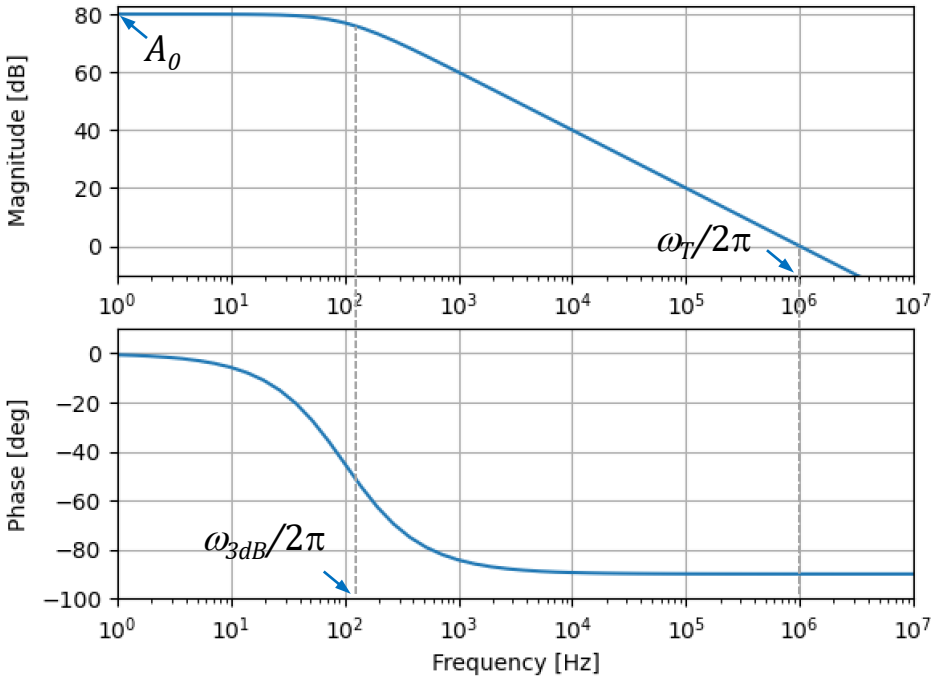


$$A_{OL}(s) = \frac{A_0}{1 + s\tau} \qquad f_{3dB,OL} = \frac{f_T}{A_0}$$

$$A_{CL}(s) = \frac{A_0}{1 + s\tau + \beta A_0} \qquad f_{3dB,CL} = \frac{1 + \beta A_0}{\tau}$$

- Opamps exhibit a constant *gain-bandwidth product,* approximately equal to f_T
- As the loop βA_0 increases, the 3dB bandwidth increases proportionally

Gain-Bandwidth Product



$$|A_{OL}(j\omega)| = \frac{A_0}{\sqrt{1 + \omega_T^2/\omega_{3dB}^2}} = 1 \qquad (1)$$

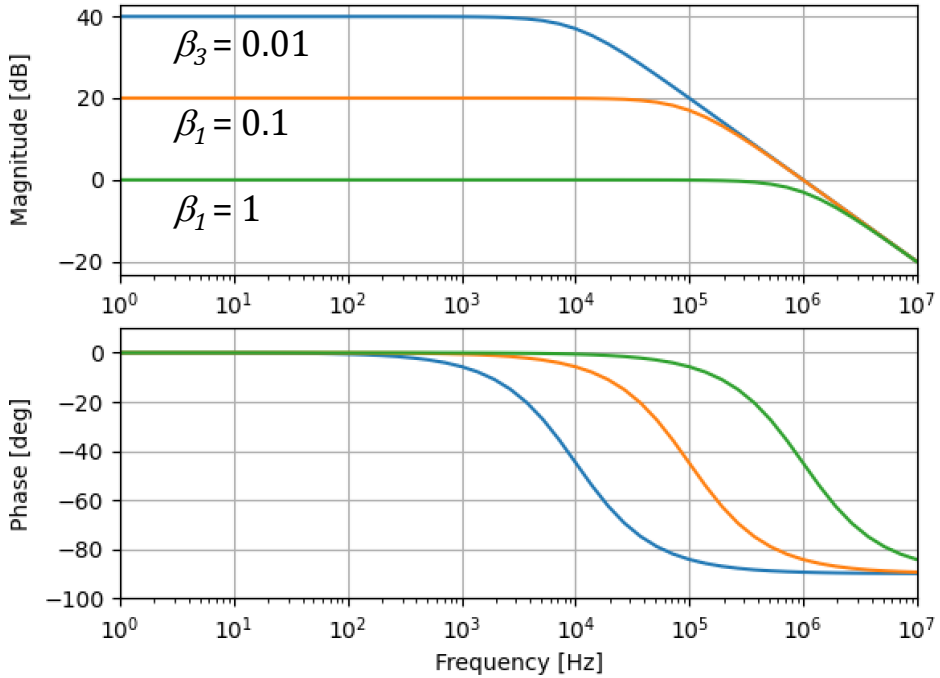
$$A_0^2 = 1 + \omega_T^2/\omega_{3dB}^2 \qquad (2)$$

$$\omega_{3dB}^2 A_0^2 = \omega_{3dB}^2 + \omega_T^2 \qquad (3)$$

$$\boxed{\omega_{3dB} A_0 \approx \omega_T} \qquad (4)$$

Closed-loop Bandwidth

- Because $\omega_{3\mathrm{dB}}$ and A_0 are constants, so is the gain-bandwidth product
- For different values of β, the magnitude response follows the same roll-off, but "breaks" at a different frequency
- An implicit assumption here is that the feedback network is frequency-independent (i.e. resistors only)



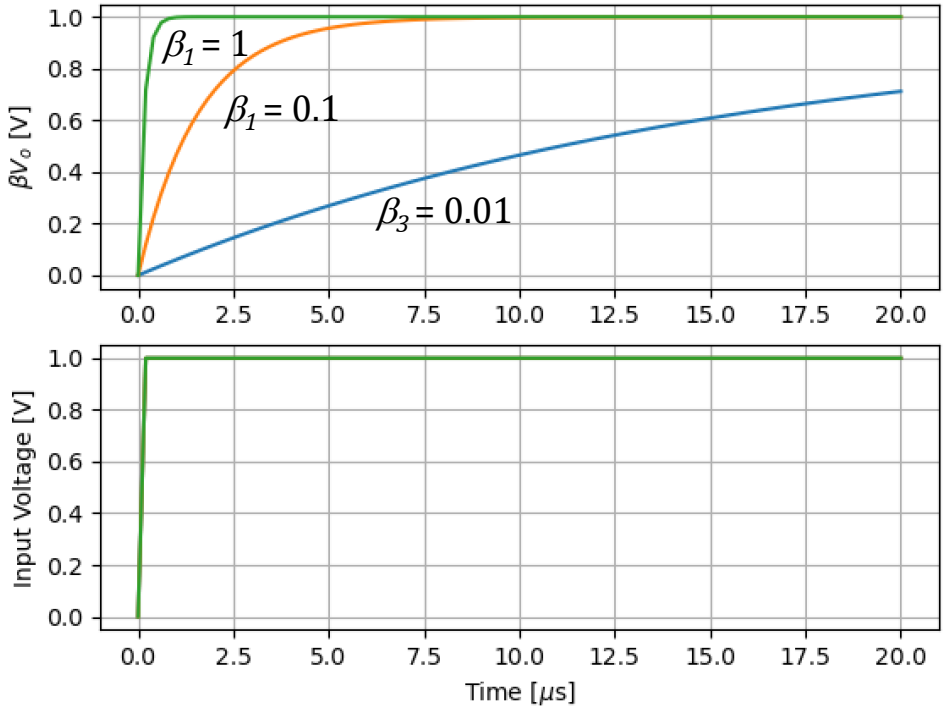
Closed-loop Settling Time

- As expected, settling time *decreases* with higher feedback factors

$$A_{CL}(s) = \frac{A_0}{1 + s\tau + \beta A_0}$$

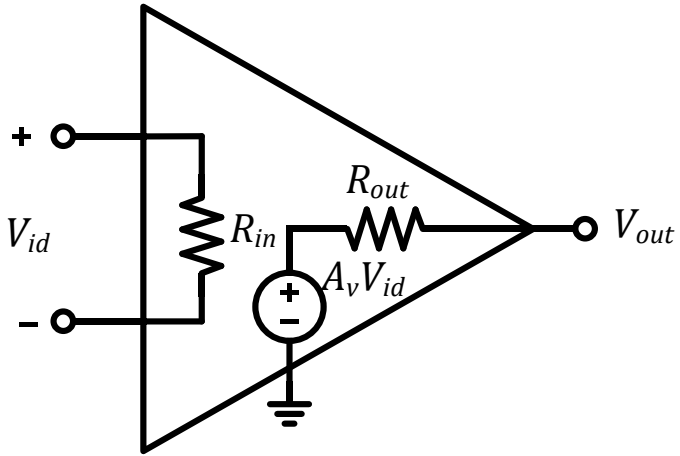
$$\tau_{CL} = \frac{\tau}{\beta A_0}$$

$$V_o(t) = u(t)(1 - e^{\frac{-t}{\tau_{CL}}})$$

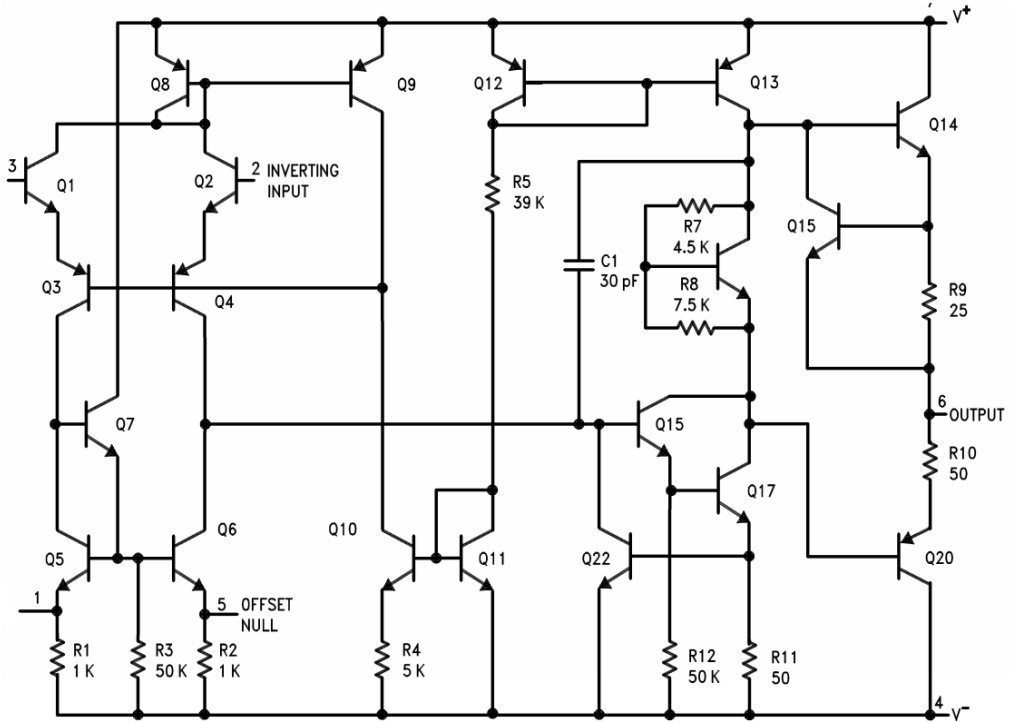


Real Opamp Characteristics

- Input impedance 1MΩ – 1TΩ
- Output impedance: 1Ω – 1kΩ
- Voltage gain < 150dB
- Common-mode rejection < 120dB
- Offset voltage: 1μV – 1mV
- Nonzero input-referred noise
- Finite slew rate

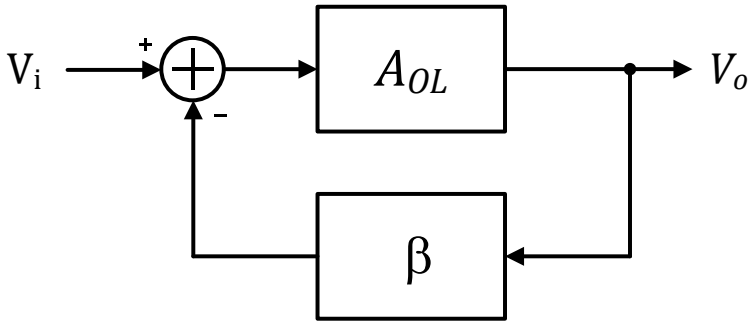


LM741 Architecture



- LM741 general-purpose opamp from Texas Instruments
- $Q_{1,2}$ form a common-emitter input pair
- C_1 is an internal compensation capacitance which sets the bandwidth
- $Q_{14,20}$ form a push-pull output stage

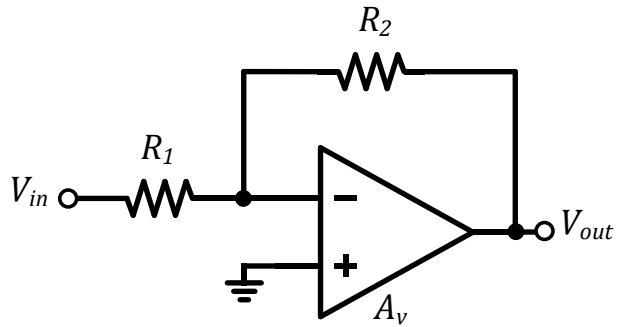
Finite Gain



A_{OL}	$\beta = 1$	$\beta = 0.1$
40 dB	1%	9%
60 dB	0.1%	1%
80 dB	0.01%	0.1%
100 dB	0.001%	0.01%

- Real opamps exhibit gain based on *finite physical parameters* (such as transconductance and output resistance)
- Finite open-loop gain results in an error in the output voltage

Finite Gain

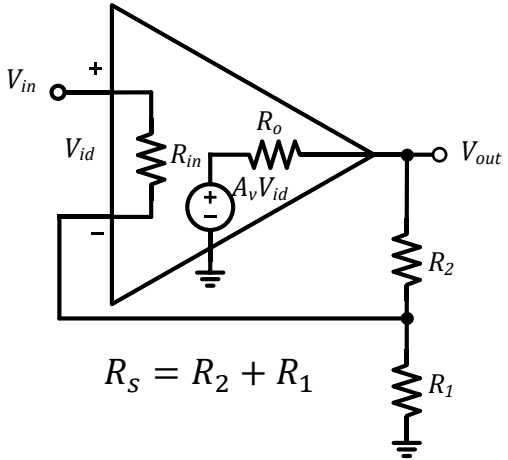


$$V_{out} = A_v(v^+ - v^-)$$

$$\frac{V_{out}}{V_{in}} = -\frac{\frac{R_2}{R_1}}{\frac{1}{A_v}\left(1 + \frac{R_2}{R_1}\right) + 1}$$

- Opamp inputs are only *exactly equal* if the open loop gain is *infinite*
- Finite *open-loop* gain of the opamp affects the precision of the *closed-loop* gain
- Even if R_1 and R_2 are *exactly* their expected values, there will be an error in the output voltage

Loading with Feedback



Without loading:

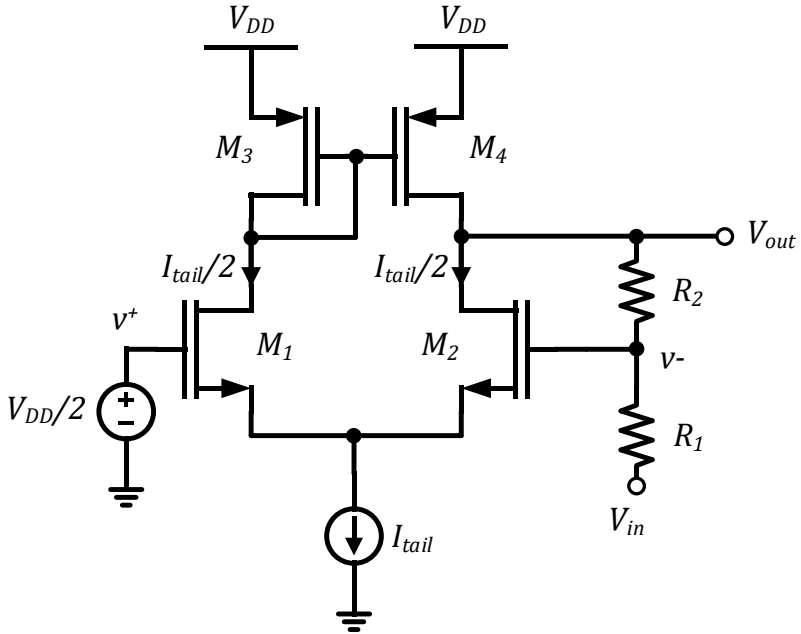
$$V_{out} = \frac{A_v}{1 + \beta A_v} V_{in}$$

With loading:

$$V_{out} = \frac{A_v}{\frac{R_o}{R_1 + R_2} + 1 + \beta A_v} V_{in}$$

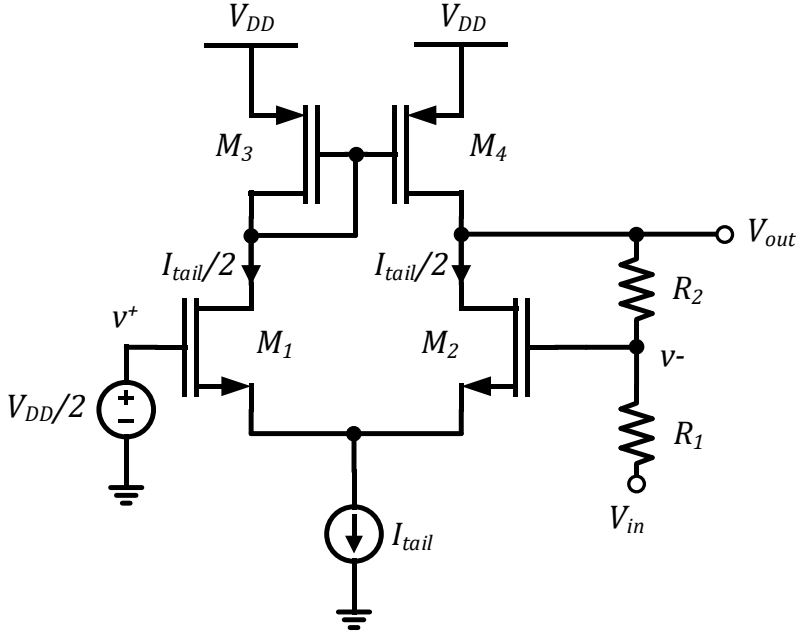
- The feedback network comprising R_2 and R_1 loads the opamp's output
- The effect of the loading depends on the magnitude of the opamp's output resistance relative to the feedback network resistance
- Loading due to the feedback network affects precision, but the effect is substantially alleviated by high open-loop gain

Input Mismatch



- Amplifier does “whatever it takes” to ensure $I_{D1} = I_{D2} = I_{bias}/2$
- Manufacturing variations result in a mismatch in the threshold voltages of M_1/M_2
- Because the source node is common to both transistors, their gate (or base, for BJT’s) voltages must differ
- Mismatch of other device parameters plays a role, but threshold mismatch dominates

Input Mismatch



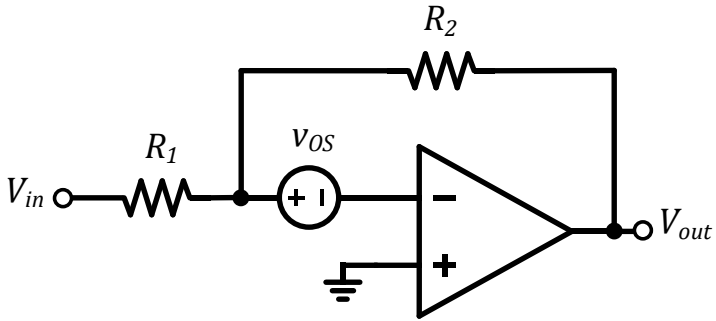
$$I_D = \kappa(V_{GS} - V_{th})^2$$

$$V_{GS1} = \sqrt{\frac{I_{tail}}{2\kappa}} + V_{th1} \qquad V_{GS2} = \sqrt{\frac{I_{tail}}{2\kappa}} + V_{th2}$$

$$\Delta V_{th} = V_{th1} - V_{th2} = v_{os}$$

$$v^- = v^+ + v_{os}$$

Input Offset Voltage

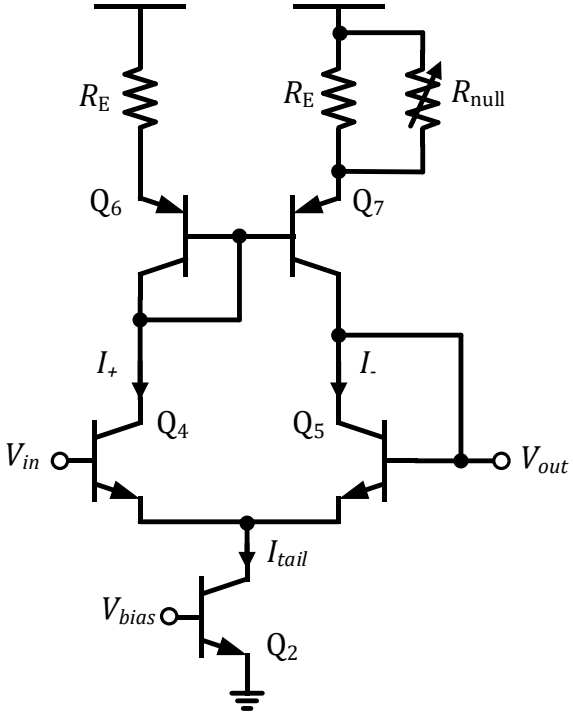


$$\frac{V_{in} - v_{os}}{R_1} = \frac{v_{os} - V_{out}}{R_2}$$

$$V_{out} = -\frac{R_2}{R_1}V_{in} + v_{os}\left(1 + \frac{R_2}{R_1}\right)$$

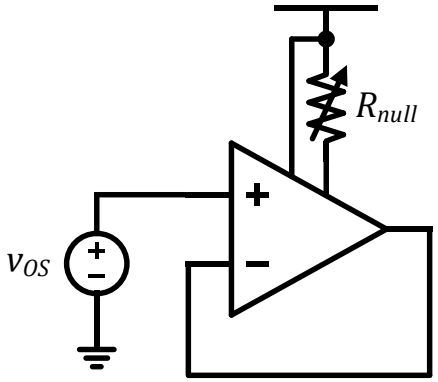
- Use superposition to include the effect of amplifier offset on the output voltage
- Input offset "sees" the gain of a non-inverting amplifier, while V_{in} is amplified as expected
- In general, offset voltage is much worse for FET-based opamps, primarily due to threshold voltage mismatch (Ltspice: BJT OTA offset)

Offset Nulling



- I_+ and I_- nominally equal, and $V_{\text{out}} = V_{\text{in}} - v_{\text{OS}}$
- R_{null} increases the effective "size" of Q_7 in the current mirror, making I_- greater than I_+ ($I_+ + I_- = I_{\text{tail}}$)
- Since more current flows through Q_5, its V_{BE} increases as R_{null} decreases
- R_{null} is adjusted until $V_{\text{out}} = V_{\text{in}}$
- Offset nulling (LTspice)

Offset Voltage Drift

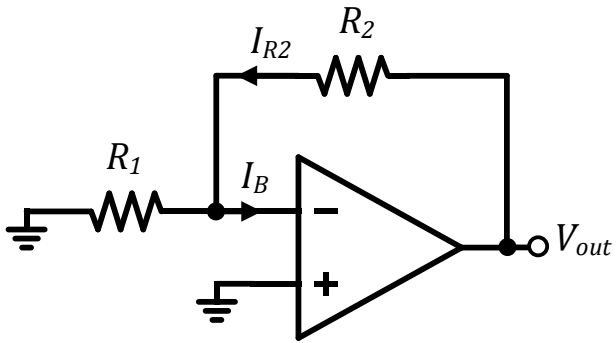


Before offset nulling: $V_{out} = v_{OS}(T)$

After offset nulling: $V_{out} = v_{OS}(T) - v_{OS}(T_0)$

- Dependence of offset voltage on temperature confounds simply "trimming" the offset at a given temperature as a blanket solution
- Nulling is performed at a single temperature (say, T_0 = 25°C)
- However, an offset voltage drift of $10\mu V/°C$ can cause output errors of a mV or more over typical operating ranges (e.g. –40 to 125°C)

Input Bias Current



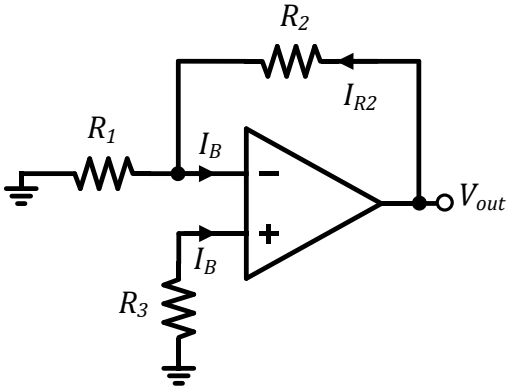
$$v_i^- = 0$$

$$I_{R2} = I_B$$

$$V_{out} = I_B R_2$$

- Opamp input currents cause an offset error in the output voltage proportional to the resistance of the feedback network
- Input currents can be as low as single-digit picoamperes (FET inputs), into the microamperes (BJT inputs)
- To avoid large voltage errors, use smaller resistances (but not so small as to load the opamp)

Bias Current Compensation

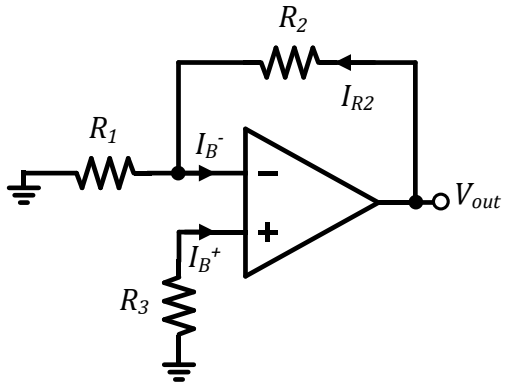


$$v_i^+ = -I_B R_3 = v_i^-$$

$$V_{out} = I_B R_2 - \left(1 + \frac{R_2}{R_1}\right) I_B R_3 = 0$$

- *Solution*: Add a resistor to the non-inverting terminal to equalize the voltage drops due to input bias current
- If the value of R_3 is equal to the *parallel combination of* R_1 *and* R_2, the offset is cancelled
- It is good practice to keep R_1 and R_2 small, to minimize mismatch errors

Input Offset Current



$$I_{OS} = I_B^- - I_B^+$$

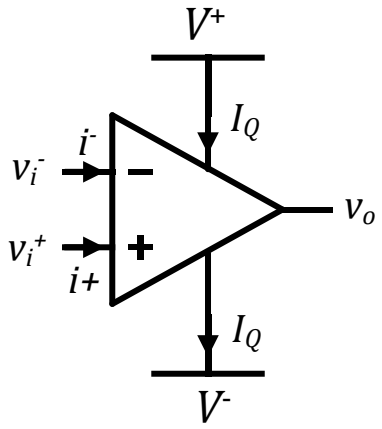
$$V_{out} = -\left(1 + \frac{R_2}{R_1}\right) I_B^+ R_3 + I_B^- R_2$$

$$V_{out} = R_2(I_B^- - I_B^+) = R_2 I_{OS}$$

- Input bias current is less problematic for balanced circuits
- However, a mismatch between I_B^+ and I_B^- (I_{OS}) will cause an error
- The only recourse is to use small resistance values in the feedback network (ensuring minimal loading of the opamp output)
- Input offset current is typically around 10 – 25% of input bias current

Opamp Supply Voltage

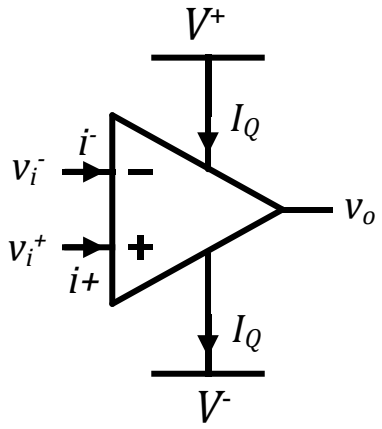
- Both bipolar and unipolar (ground-referenced) options abound
- Bipolar amplifiers can avoid AC-coupling for ground-referenced sensors
- Opamp power supply should be compatible with that of the ADC
- Most digital systems are unipolar, level conversion may be needed



$$V^- \leq v_i^+, v_i^-, v_o \leq V^+$$

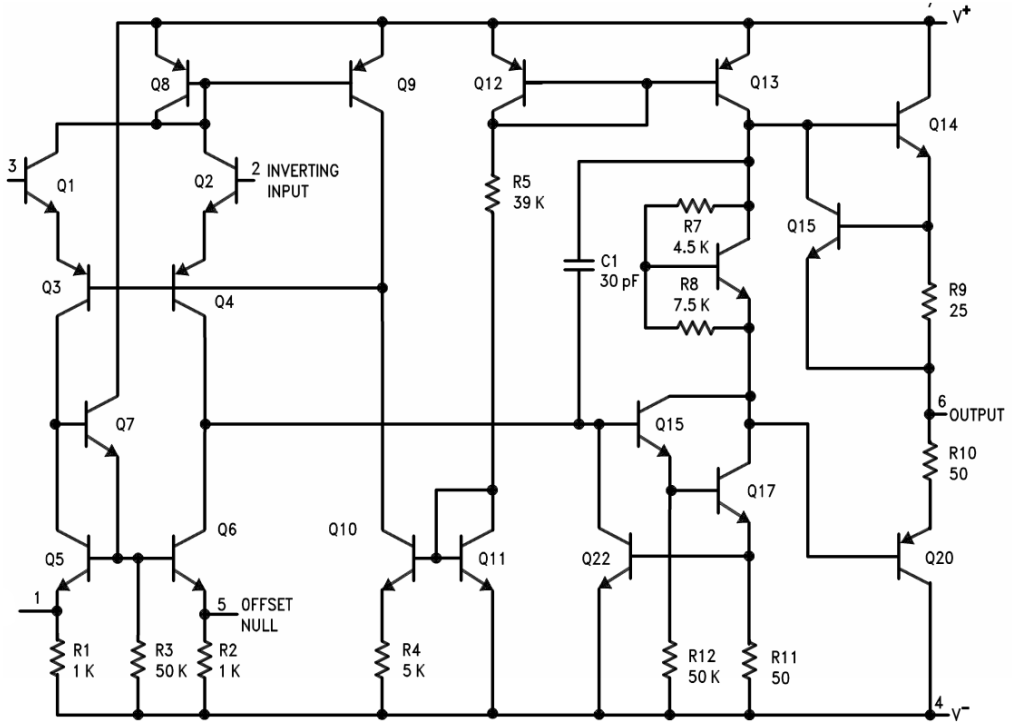
Opamp Quiescent Current

- Supply current opamps varies widely, dependent on application
- Both bandwidth and noise scale favorably with increasing supply current
- However, higher current means more heat generation
- For power-sensitive applications (e.g. energy harvesting or battery-powered), power efficiency is critical



$$f_T \propto I_Q \qquad e_n \propto \frac{1}{\sqrt{I_Q}}$$

LM741 Specifications



Parameter	Typical
Open-loop gain	106 dB
Bandwidth	1.5 MHz
Input resistance	2 MΩ
Input offset voltage	1 mV
Offset voltage drift	15 μV/°C
Input bias current	80 nA
Input offset current	20 nA
Supply current	1.7 mA