EE P 538
Analog Circuits for Sensor Systems

Spring 2020

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Announcements

- Design Project Phase 2 due Friday, June 12 at midnight

Week 10

- AoE Chapter 13 – Analog Meets Digital
- Analog Devices: Mixed Signal Electronic Systems
  - MT-010: Data Converter Static Specifications
  - MT-020: Flash ADCs
  - MT-021: SAR ADCs
  - MT-022: Sigma-Delta ADC Basics

Overview

- Last time…
  - Representation of signals (Fourier Series/Transform)
  - Sampling/aliasing
  - Quantization
- Today…
  - ADC performance
  - SAR ADC
  - Delta-Sigma ADC

Lecture 10 – Analog-to-Digital Converters

ADC Performance Limitations

- Both noise and distortion in real ADCs limit their maximum attainable resolution
- For example, a 16-bit ADC doesn’t necessarily (and almost certainly does not) exhibit 16-bit performance
- The effects of all ADC non-idealities are captured by the signal-to-noise-and-distortion ratio (SINAD)
- From this ratio, we can determine the “effective number of bits” (ENOB), which gives a sense of the actual performance of the ADC

Effective Number of Bits (ENOB)

- For a full-scale input, the SQNR of an ideal ADC is given by

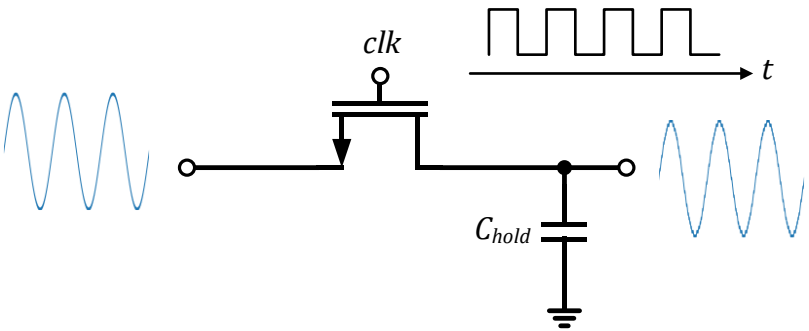
$$SQNR = 20\log_{10}\frac{(V_{FS}/2)/\sqrt{2}}{V_{LSB}/\sqrt{12}} = 20\log_{10}\left(2^N \cdot \sqrt{1.5}\right) \approx 6.02N + 1.76\text{dB}$$

- From this expression we define the effective number of bits as

$$ENOB = \frac{SINAD - 1.76\text{dB}}{6.02}$$

- The notion of ENOB allows us to compare the performance of different ADCs with the same number of output bits

Sampling Noise



$$e_{n,sw}^2 = 4kTR_{sw}$$

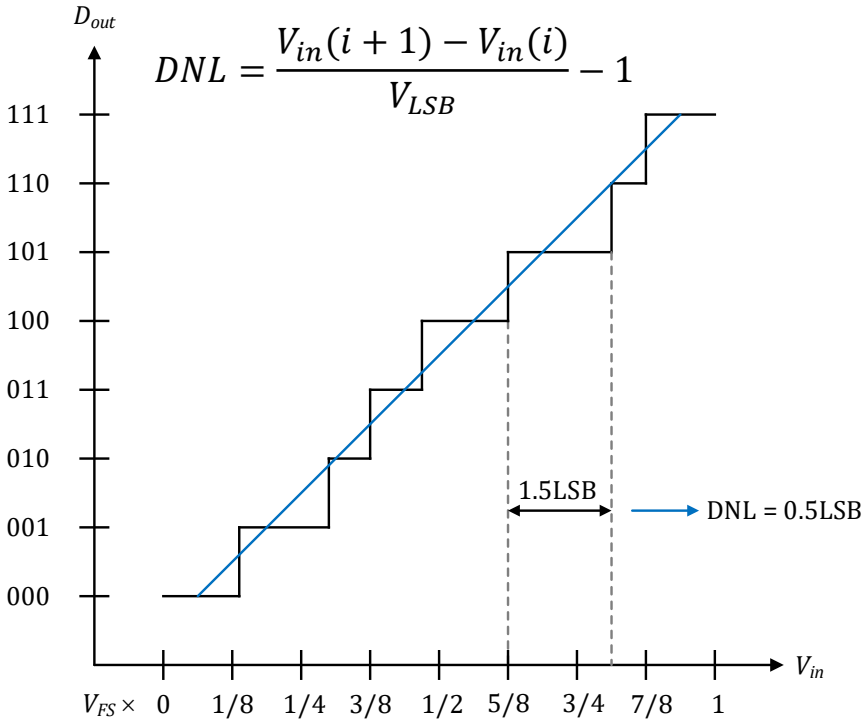
$$f_{ENB} = 1/4R_{sw}C_{hold}$$

$$v_{n,sw(rms)} = \sqrt{kT/C_{hold}}$$

- All real sampling switches (which are constructed using transistors) exhibit resistance and thermal noise
- The total integrated noise (from the switch only) depends on the value of the hold capacitor C_{hold}
- Higher sampling rates require smaller capacitors, increasing the thermal noise

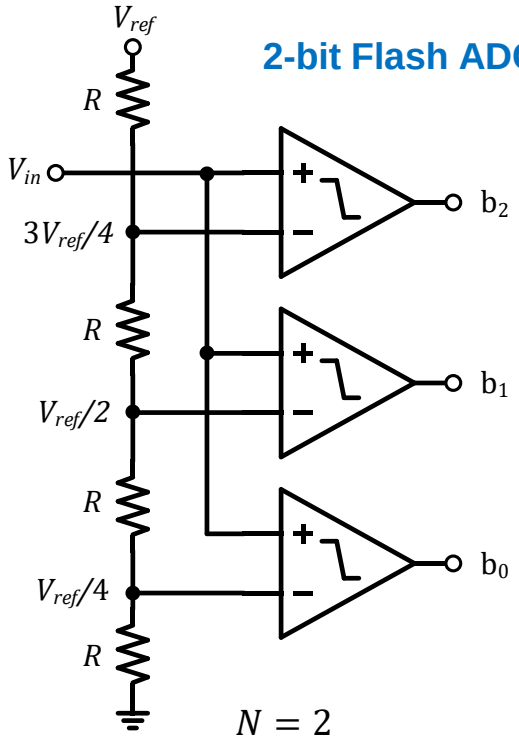
Differential Nonlinearity (DNL)

- Distortion in ADCs arises due to quantizer nonlinearity
- DNL arises when a change of 1 LSB (in voltage) of the input voltage produces more or less than 1 LSB change in the output code
- DNL in excess of 1 LSB can result in *missing codes* and *non-monotonicity*
- Typically, the DNL of an ADC signifies the worst-case deviation from the ideal 1-LSB step



Flash ADC

- Flash ADCs are fast; the conversion time is limited only by comparator delay, which can be as low as few hundred picoseconds for modern CMOS processes
- Sampling rates in Gsps are common for Flash converters
- Linearity of Flash ADCs is limited by comparator offset, setting the maximum resolution to approximately 8-10 bits



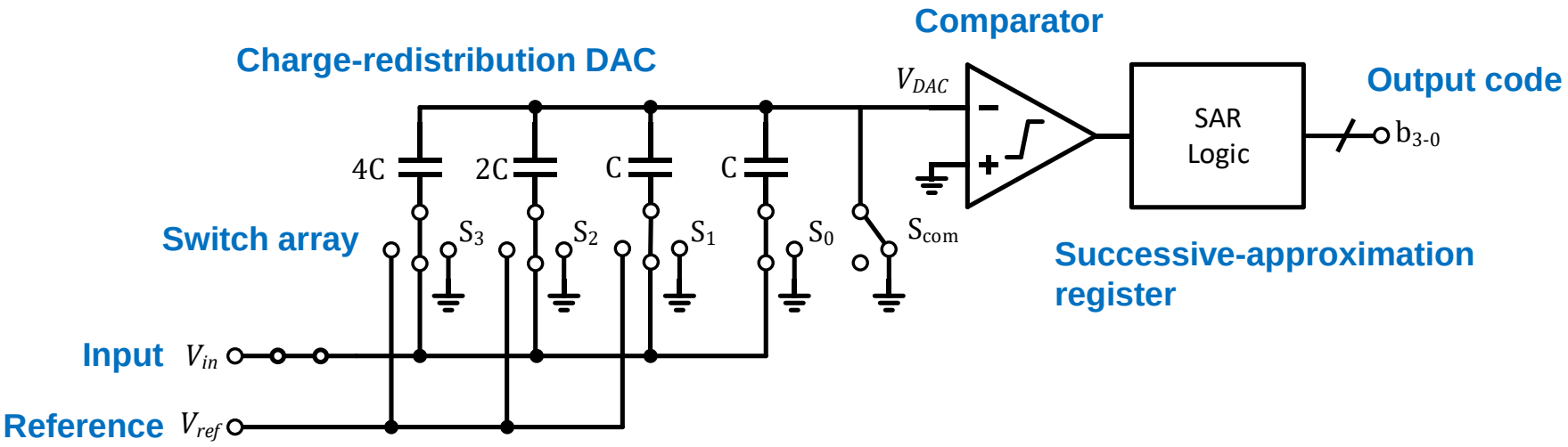
Analog	Therm.	Binary
$3V_{FS}/4$	111	11
$V_{FS}/2$	011	10
$V_{FS}/4$	001	01
0	000	00

$$V_{LSB} = \frac{V_{ref}}{2^N} = \frac{V_{ref}}{4}$$

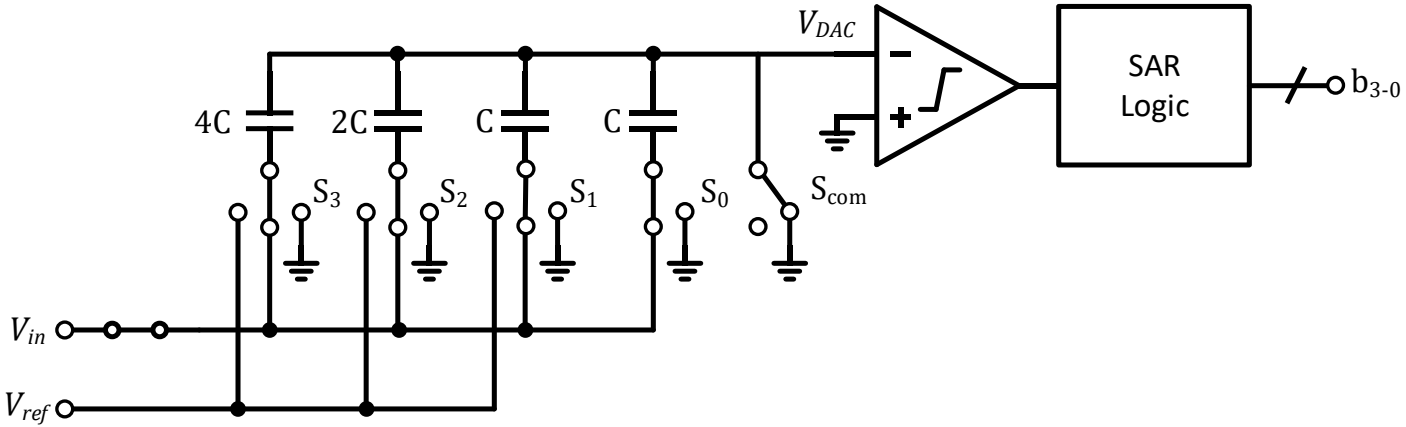
Successive Approximation (SAR) ADC

- Whereas a Flash ADC determines the value of each bit in *parallel*, a Successive Approximation (SAR) ADC does this in sequence
- SAR ADCs use a binary search algorithm to determine the value of each output bit in succession, successively approximating the input
- Due the serial operation, SAR ADCs require a minimum of N clock cycles for an N-bit converter, making them substantially slower than Flash converters
- However, improvements in digital processing technology and transistor sizes have enabled the design of high-resolution (> 16 bits) SAR ADCs with clock rates as high as 100 Msps
- Linearity in SAR ADCs is limited by capacitor mismatch

SAR ADC Architecture

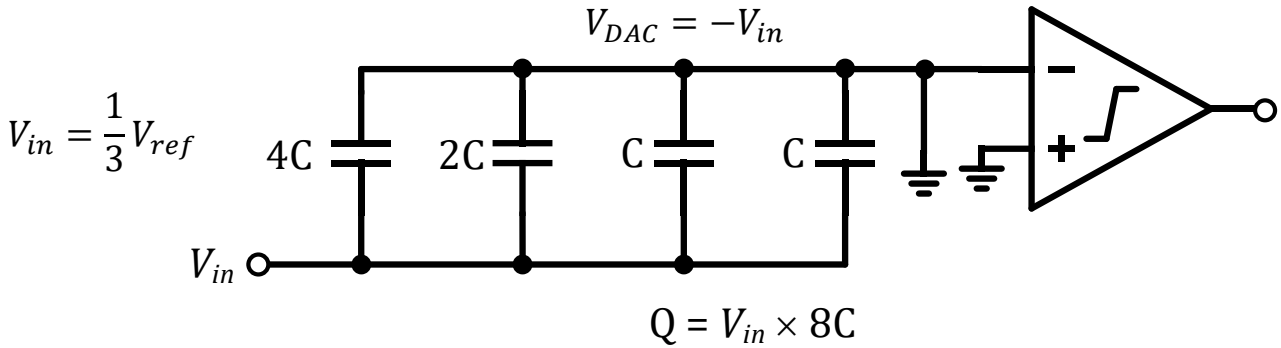


3-bit SAR ADC



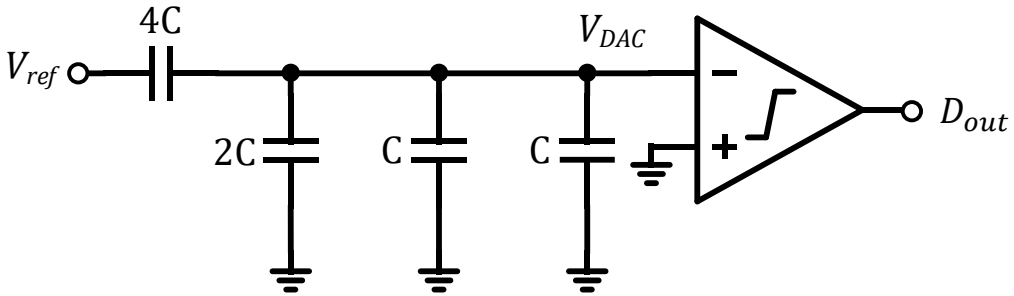
- Input voltage V_{in} is sampled onto a binary-weighted capacitor array
- Charge is redistributed based on each successive comparator decision
- The capacitor/switch array forms a digital-to-analog converter referred to as a “charge-redistribution DAC” (CDAC)

Sampling Phase



- During the sampling phase, the input voltage is sampled onto the full capacitor array, such that $Q = V_{in} \cdot 8C$
- Comparisons are performed for each bit of the output
- During the conversion process, the charge on the array is added to or subtracted from based on the decision for each bit

Redistribution Phase



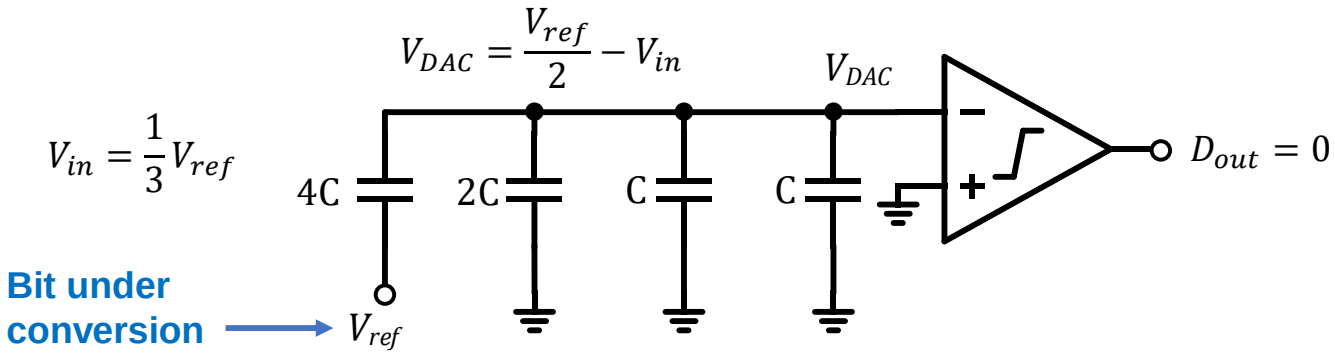
$$V_{DAC,init} = -V_{in}$$

$$V_{DAC,MSB} = V_{ref}\frac{4C}{C_{tot}} - V_{in}$$

$$= \frac{V_{ref}}{2} - V_{in}$$

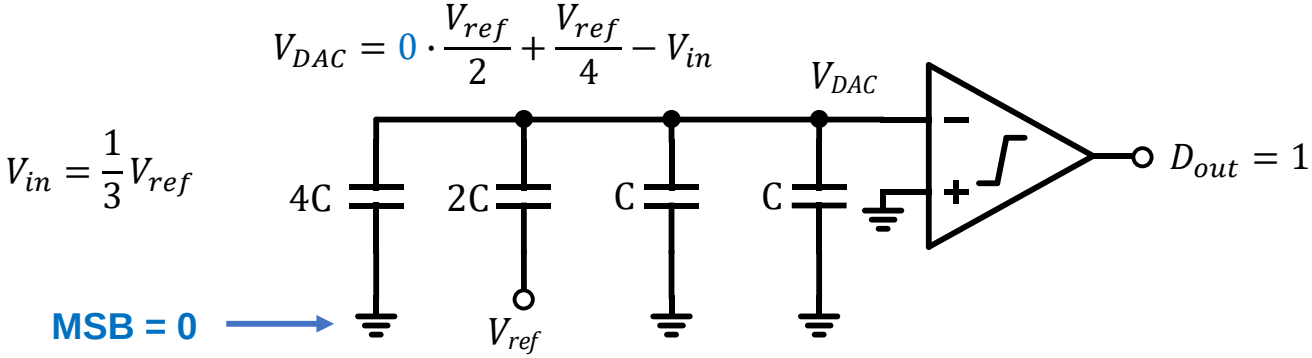
- As the bottom plate of each capacitor in the array is connected to V_{ref}, V_{DAC} is set by the ratio of that capacitor to the total array capacitance
- V_{DAC} is either greater or less than zero, depending on the value of V_{in}
- The comparator output D_{out} sets the switch state for the current bit, and the conversion proceeds to the next bit

MSB Decision



- The bottom plate of MSB capacitor is connected to V_{ref}, which sets the DAC voltage V_{DAC} to $V_{ref}/2 - V_{in}$
- If $V_{in} > V_{ref}/2$, V_{com} is negative and the output of the comparator is 1
- If $V_{in} < V_{ref}/2$, V_{com} is positive and the output of the comparator is 0
- The comparator output sets the MSB switch position for subsequent decisions

Bit N–2 Decision

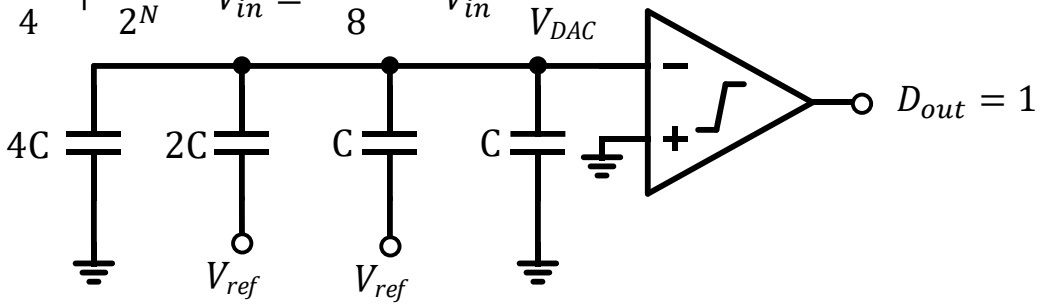


- Next, the bottom plate of the $(N-2)_{th}$ capacitor is connected to V_{ref}, which drives the DAC voltage V_{DAC} to $V_{ref}/4 - V_{in}$
- If $V_{in} > V_{ref}/4$, V_{com} is negative and the output of the comparator is 1
- If $V_{in} < V_{ref}/4$, V_{com} is positive and the output of the comparator is 0
- Again, the comparator output sets the switch position for the bottom plate of the $(N-1)_{th}$ capacitor

Bit 0 Decision (LSB)

$$V_{DAC} = 0 \cdot \frac{V_{ref}}{2} + 1 \cdot \frac{V_{ref}}{4} + \frac{V_{ref}}{2^N} - V_{in} = \frac{3V_{ref}}{8} - V_{in}$$

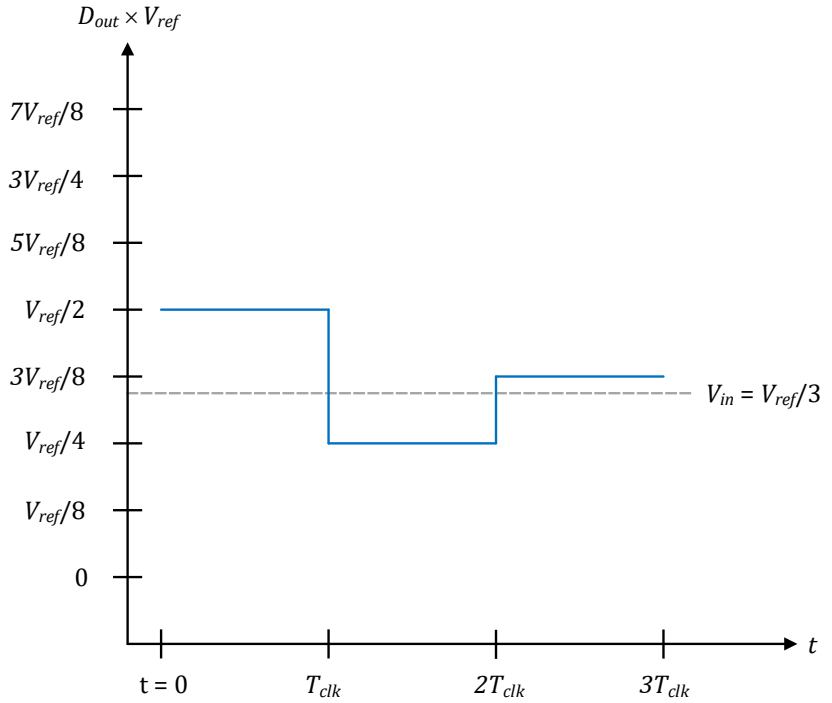
$$V_{in} = \frac{1}{3} V_{ref}$$



- The comparator decision for the $(N-2)^{th}$ bit is retained in the form of charge on the CDAC
- The final comparison determines the LSB of the output code and completes the conversion process

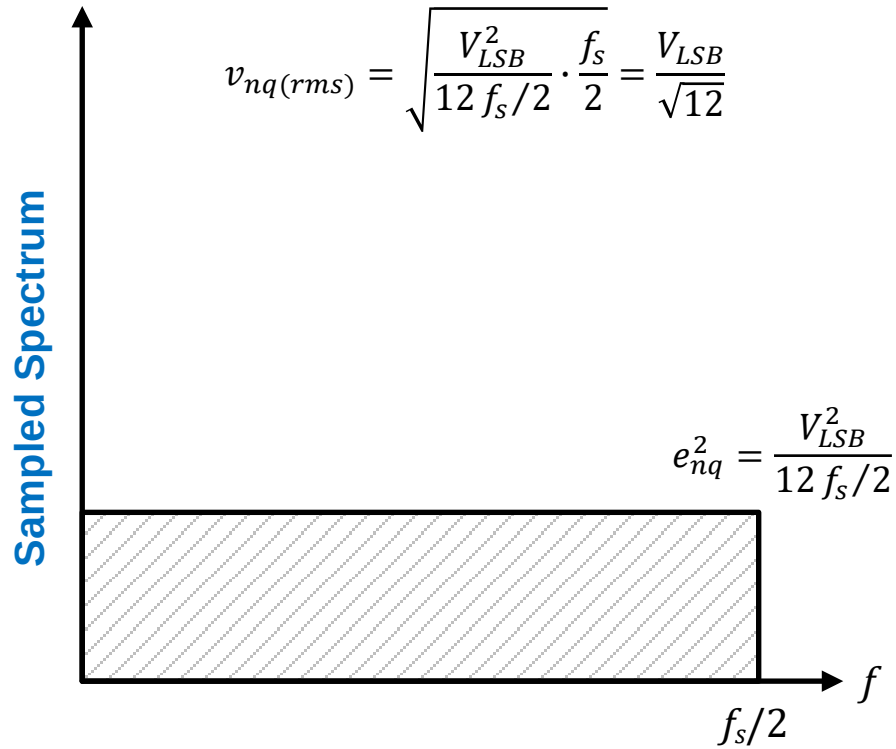
Conversion Example

- The output code *successively approximates* the input voltage by comparing the input against reference levels in a step-wise fashion
- Each conversion step requires a single clock cycle, such that the overall sampling frequency is limited by the number of output bits
- Due to the large amount of charge transferred, the MSB step determines the minimum clock period T_{clk}



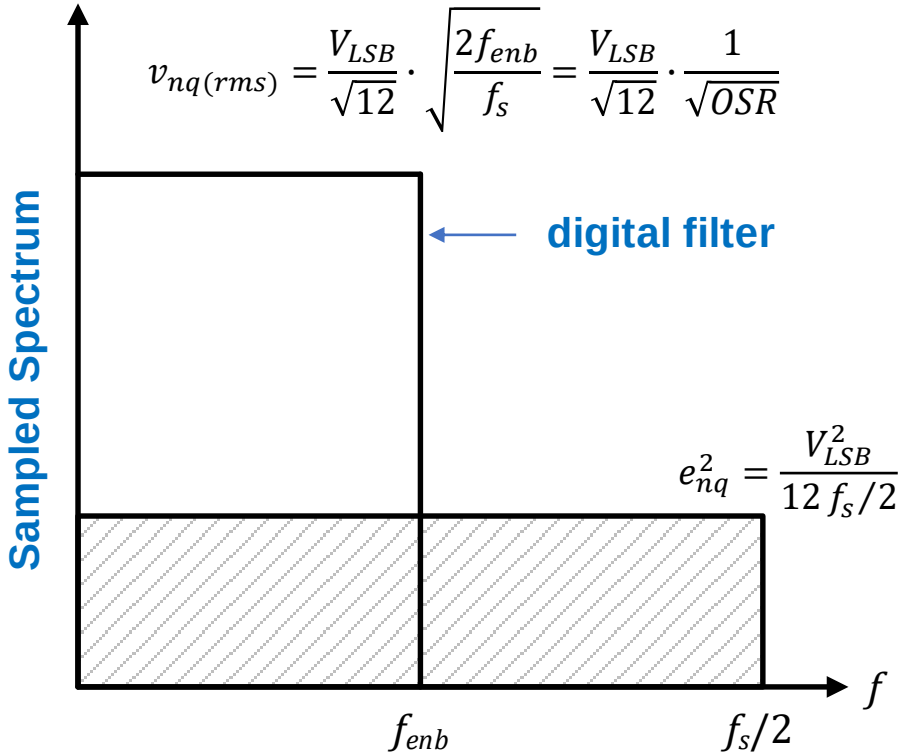
Nyquist-Rate Sampling

- When sampling at the Nyquist rate (relative to the input signal) there is no need to filter in the digital domain
- In this case, the quantization noise is fixed and the effective resolution is set by the raw quantization error
- This places the burden of filtering in the analog domain, which may be costly in terms of power, size, and price



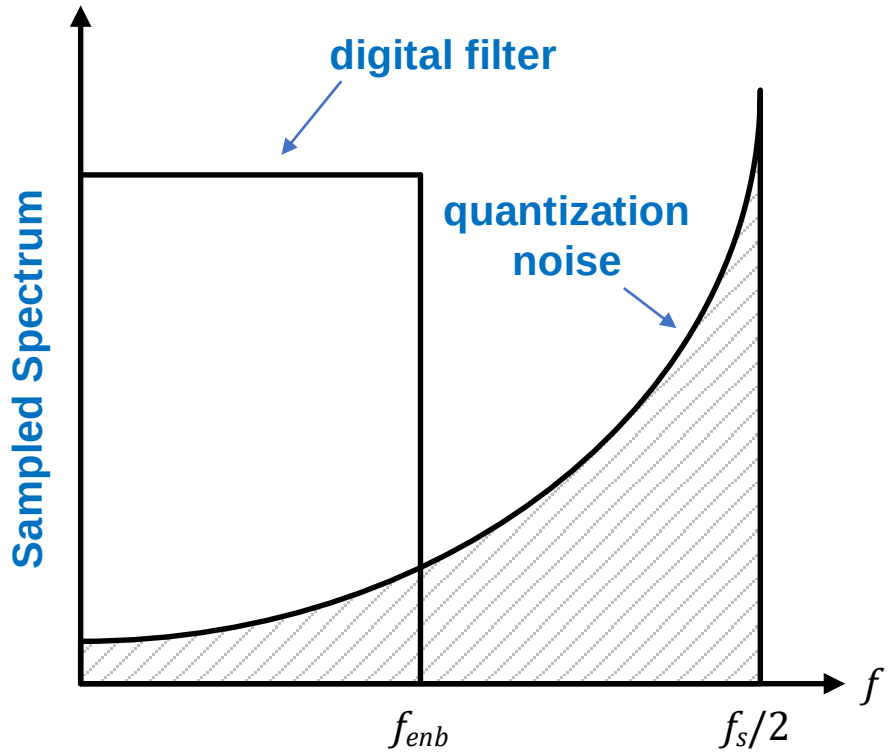
Oversampling

- As we have seen, sampling a signal at frequencies higher than the Nyquist rate (i.e. oversampling) provides an advantage with respect to quantization noise
- After sampling, digital filtering can be applied to limit the noise bandwidth and improve *effective* resolution
- Shifting the burden of filtering to the digital domain can be beneficial in terms of cost and precision

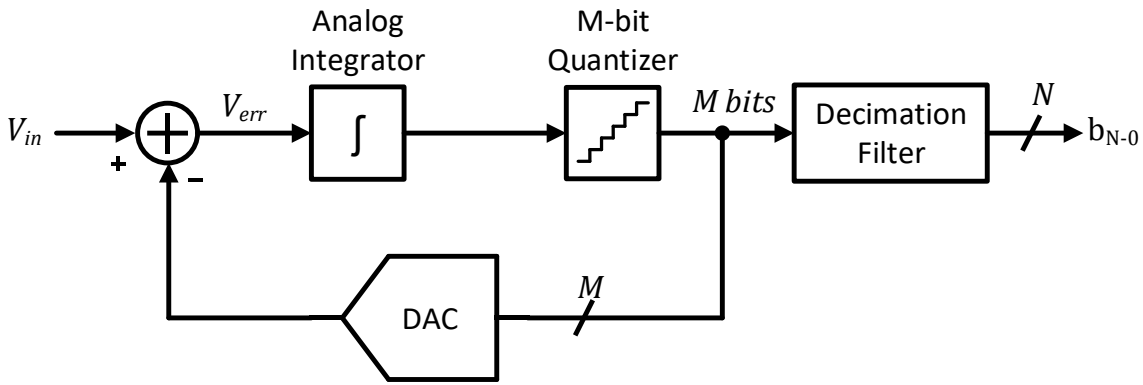


Noise Shaping

- Oversampling has limited benefits, since the effective *voltage* noise density only scales as $1/\sqrt{OSR}$
- If, in addition to oversampling, we can shape the quantization noise so that filtering is more effective in removing it, we can achieve even higher resolution
- This is accomplished by a process called “noise shaping,” and is the fundamental principle of Delta-Sigma converter operation

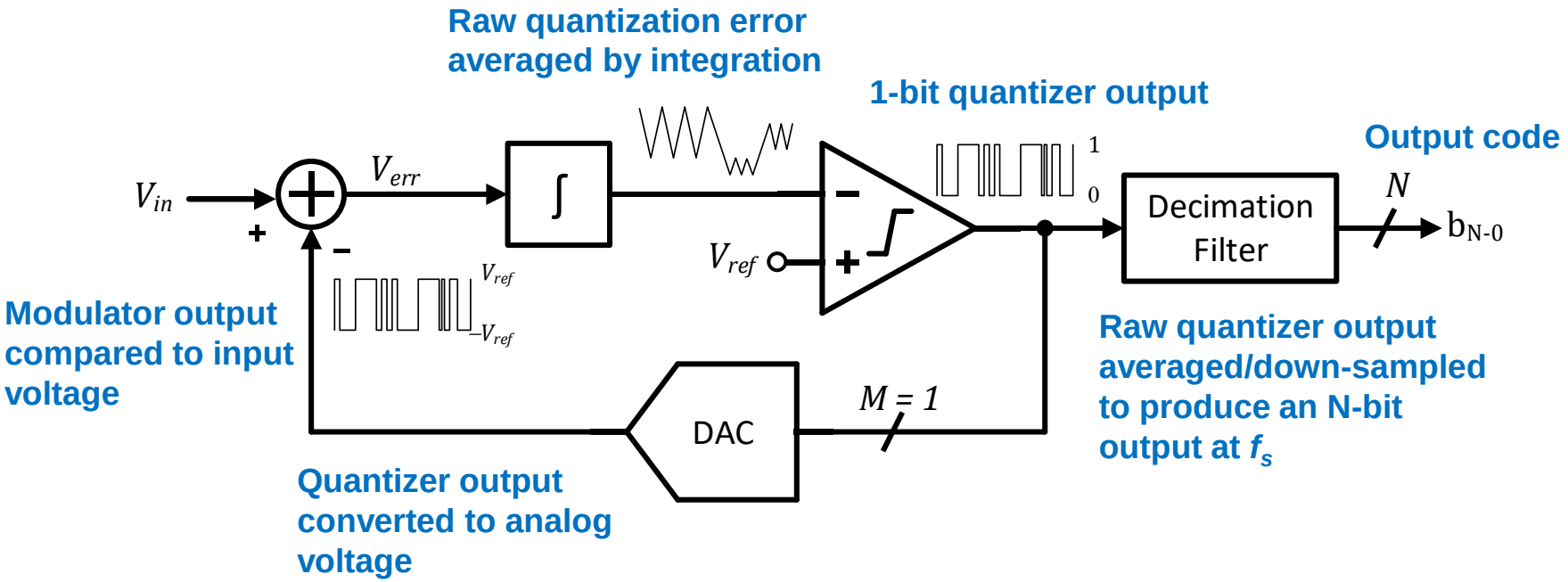


Delta-Sigma Modulation

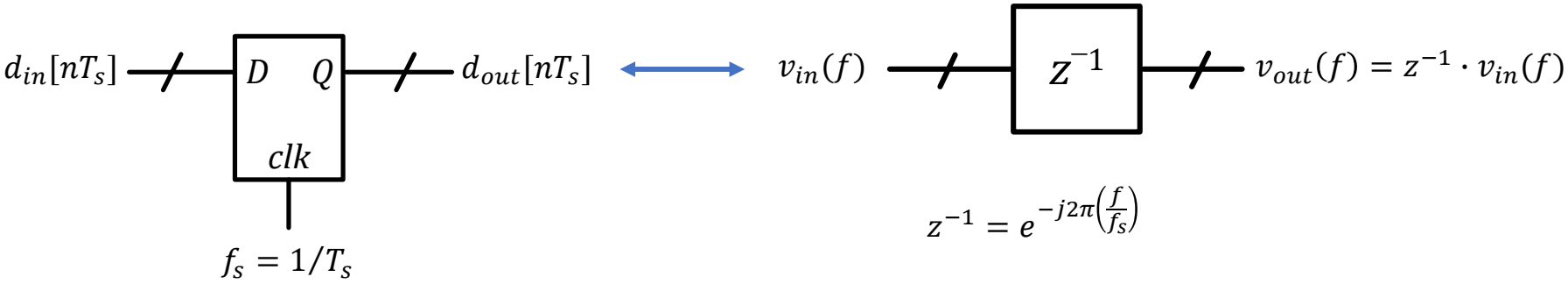


- A low-resolution quantizer (e.g. 1-bit) is combined with *oversampling* and *negative feedback* to realize an *average* quantization error much lower than that of the raw quantization
- The Delta-Sigma modulator (DSM) output is applied to a digital filter for averaging and down-sampling
- The Delta-Sigma converter architecture trades *speed* for *precision*

1-bit Delta-Sigma ADC

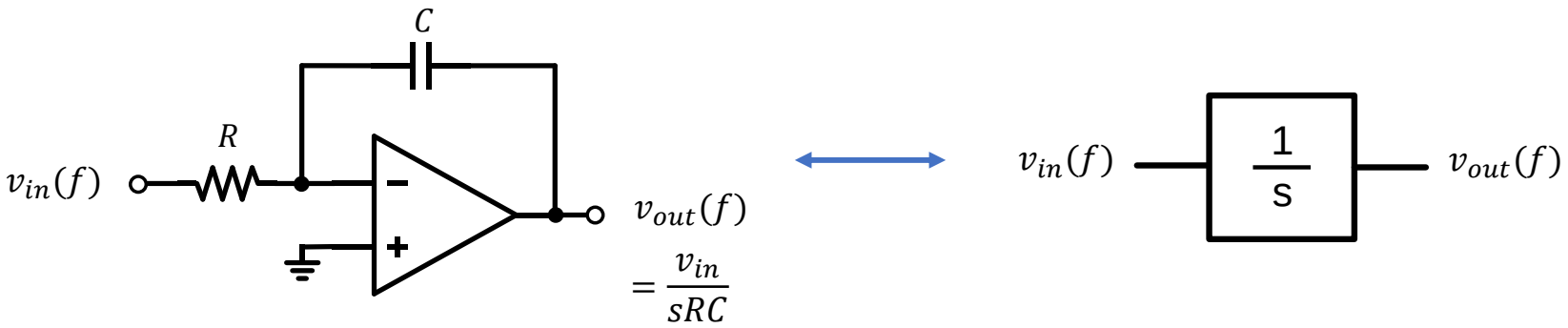


Z-domain Representation



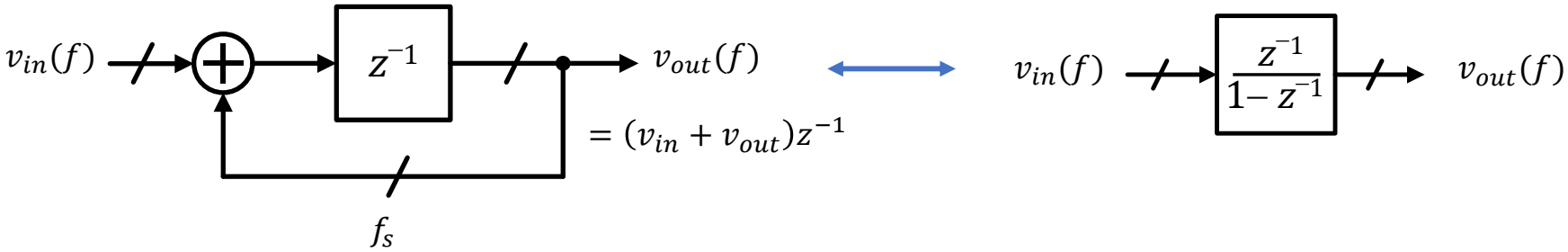
- A phase delay is represented in the frequency domain as a complex exponential, of which the magnitude is 1
- Because delays are so common in digital systems, we instead use the term z^{-1} (which signifies the complex z-plane) to simplify the expressions

Continuous–Time Integrator



- Integration in the analog (i.e. continuous-time) domain involves integration of charge onto a capacitance
- This integration has an intrinsic phase delay, due to the 90° phase relationship between capacitor current and voltage
- The capacitor “remembers” all previous values of the input and continually “adds” the current value to the integrated value

Discrete–Time Integrator



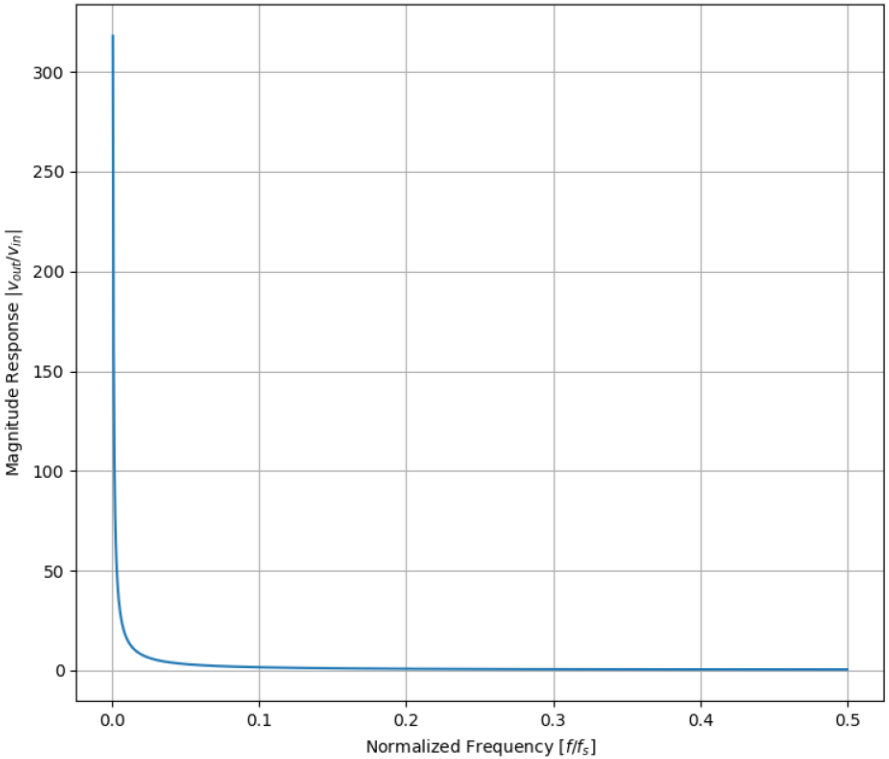
- Integration in the digital domain (often referred to as accumulation) is as simple as continually adding (at the rising edge of each clock period) the current input value to the accumulated sum of all previous inputs
- The integrator can be thought of as a summing, or *averaging*, element, as it “remembers” the input value over a long period of time
- Hence, the integrator emphasizes-low frequency information

Magnitude Response

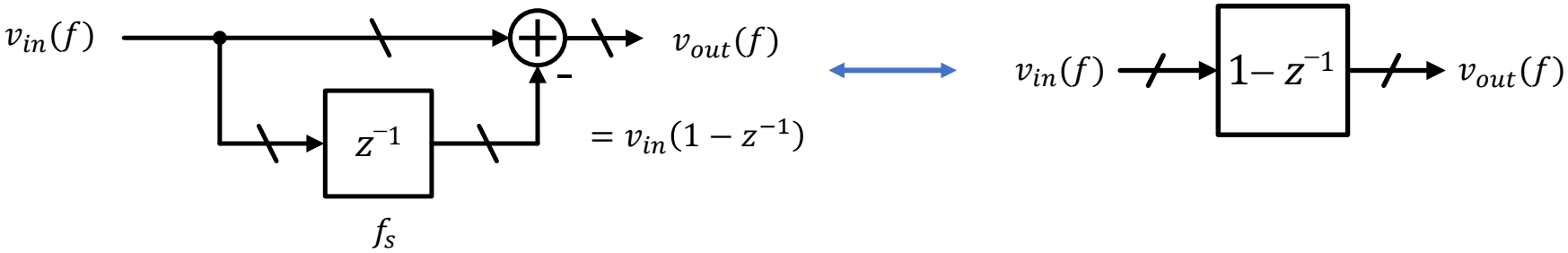
- The magnitude response of the discrete-time integrator is given by

$$|H(f)| = \left|\frac{v_{out}(f)}{v_{in}(f)}\right| = \frac{1}{2\left|\sin \pi \frac{f}{f_s}\right|}$$

- As expected, the integrator has high gain at low frequencies and very little at high frequencies
- This is in line with the idea that the integrator “remembers” long-term information but suppresses short-term content



Discrete–Time Differentiator



- The differentiator processes the *difference* between input values occurring in sequence
- The differentiator can be thought of as processing the *change* in the input (differentiation is the process of taking the derivative)
- As a result, the differentiator emphasizes high-frequency information

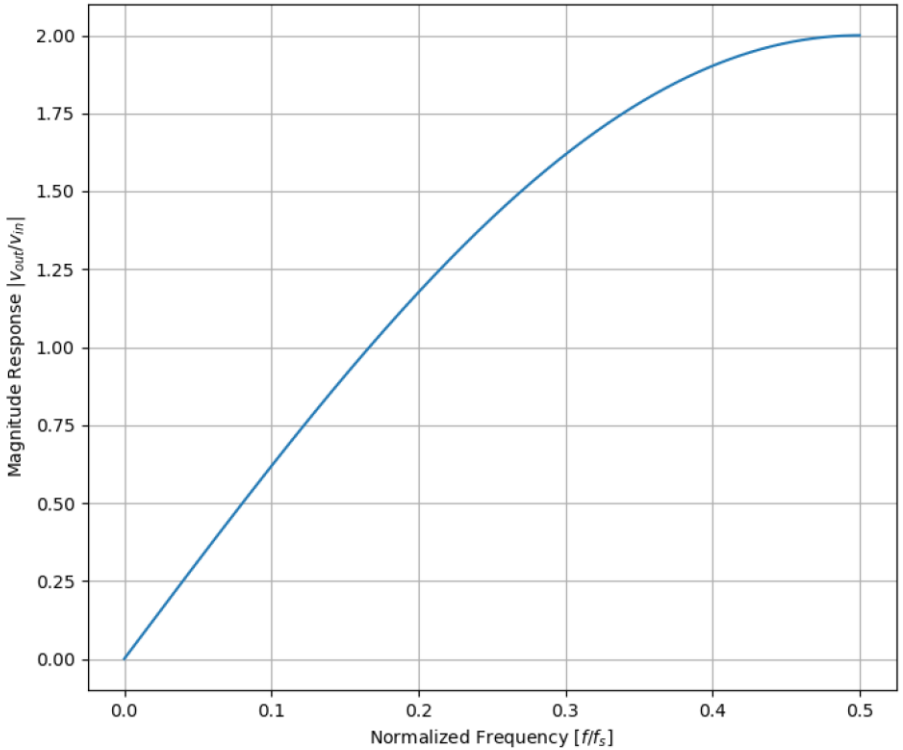
Magnitude Response

- The magnitude response of the discrete-time differentiator is given by

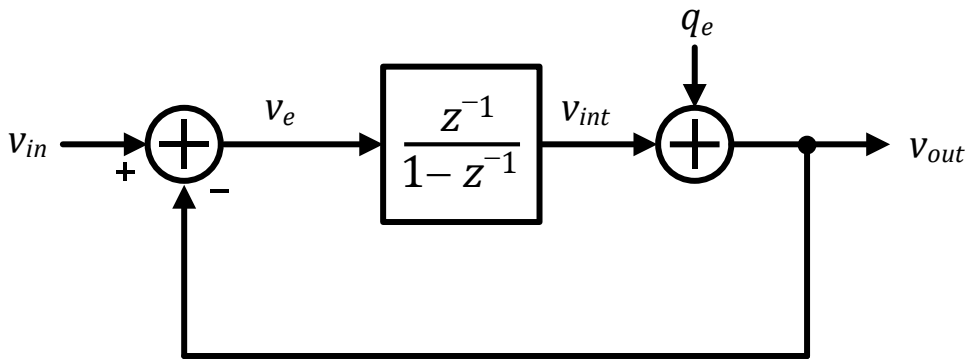
$$|H(f)| = \left|\frac{v_{out}(f)}{v_{in}(f)}\right| = 2\left|\sin \pi \frac{f}{f_s}\right|$$

  which (possibly as expected) is the inverse of the integrator magnitude response

- In contrast to the integrator, the differentiator passes high-frequency content and suppresses that at low frequencies

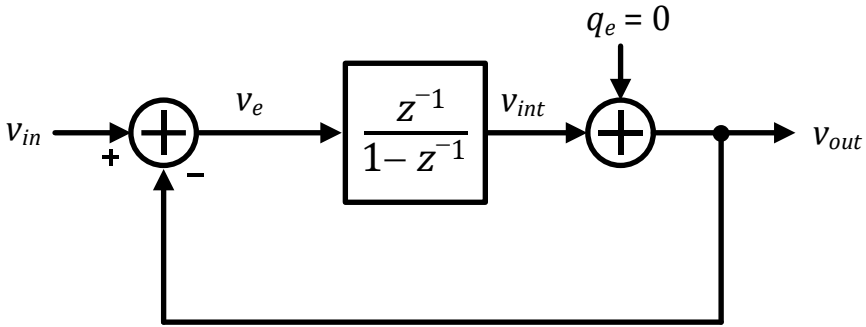


DSM Linear Model



- The DSM can be modeled as a linear feedback look with quantization error added to the output
- Using superposition, we can analyze the loop processing of the input and quantization noise separately
- The integrator element provides high low-frequency *open-loop* gain, similar to that of an opamp

Signal Transfer Function



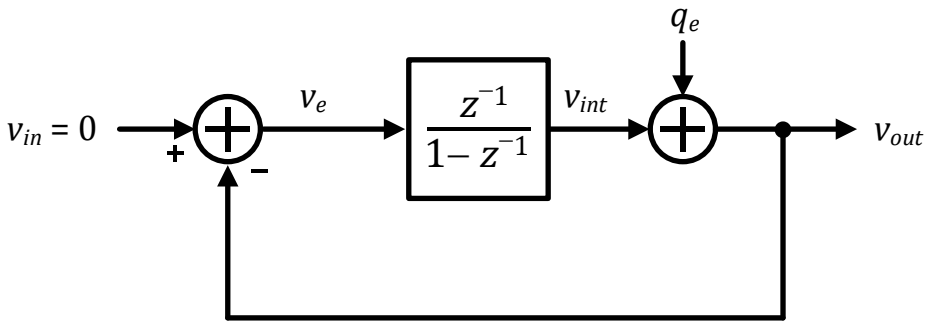
$$v_e = v_{in} - v_{out} \qquad v_{out} = \frac{(v_{in} - v_{out})z^{-1}}{1 - z^{-1}}$$

$$\frac{v_{out}}{v_{in}} = \frac{z^{-1}}{1 - z^{-1} + z^{-1}} = z^{-1}$$

$$STF = z^{-1}$$

- The signal merely passes through the modulator with a delay
- We call the relationship between the input signal and output signal the "signal transfer function," designated by STF
- The situation is analogous to an opamp in unity-gain feedback, which has a gain of 1 and a phase delay determined by the opamp bandwidth

Noise Transfer Function



$$v_e = -v_{out} \qquad v_{out} = v_{int} + q_e$$

$$v_{out} = (1 - z^{-1}) \cdot q_e$$

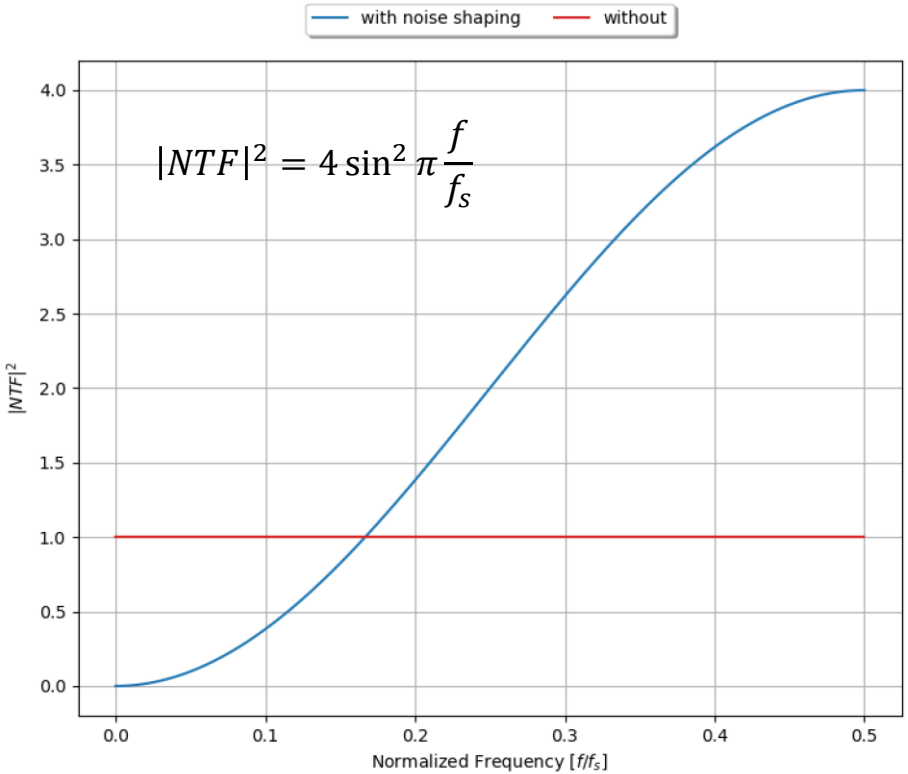
$$NTF = 1 - z^{-1} = 1 - e^{-j2\pi\frac{f}{f_s}}$$

- Because it is added to the output after the integrator, the quantization error is differentiated instead of integrated
- The transfer function with respect to the quantization noise has a high-pass characteristic, suppressing it at low frequencies
- This characteristic of the Delta-Sigma Modulator is referred to as “noise-shaping,” and it is the fundamental advantage of the architecture

Noise Transfer Function

- At frequencies well below $f_s/2$, the NTF magnitude is substantially lower than 1
- This means that if we apply a filter with bandwidth much lower than $f_s/2$, we can substantially reduce the effective quantization error
- We can quantify the improvement in performance with respect to the oversampling rate (OSR):

$$OSR = \frac{f_s}{2f_B}$$



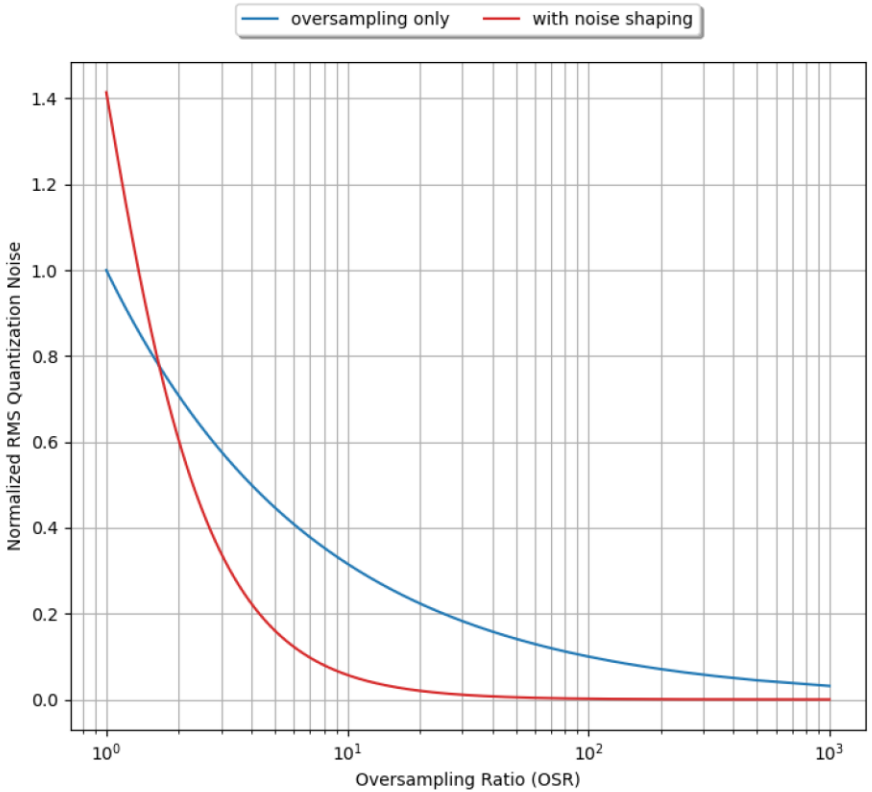
RMS Quantization Noise

- With oversampling alone, the in-band rms quantization noise is given by

$$v_{nq,os(rms)} = \frac{V_{LSB}}{\sqrt{12}} \cdot \frac{1}{\sqrt{OSR}}$$

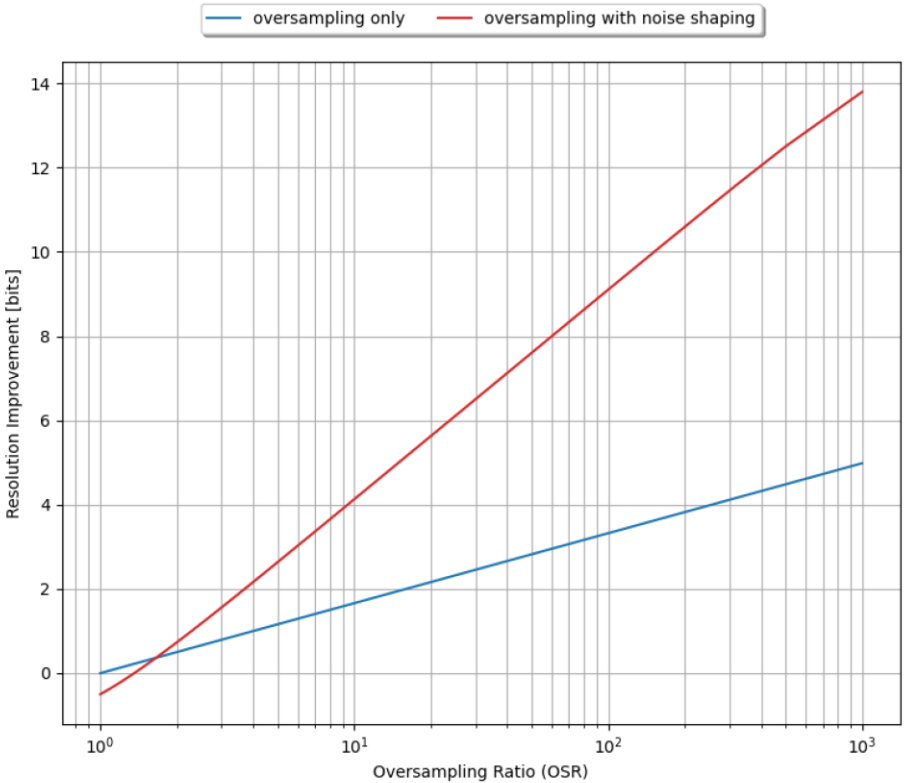
- With 1st–order noise shaping, the benefit is much more pronounced

$$v_{nq,ns(rms)} = \frac{V_{LSB}}{\sqrt{12}} \cdot \frac{\pi}{\sqrt{3}} \cdot \frac{1}{OSR^{3/2}}$$



Effective Resolution

- The effect of oversampling/noise-shaping on ADC performance can be quantified as an improvement in the effective resolution, in terms of bits added
- For oversampling alone, every doubling of the oversampling rate adds only 0.5 bits of resolution
- With 1st–order noise shaping, doubling the OSR adds 1.5 bits of resolution
- Higher order DSMs can improve this even further!



Higher-Order Modulators

- The “order” of a Delta-Sigma modulator is increased by adding integrator stages
- The noise transfer function for higher-order modulators can be expressed as

$$|NTF|^M = |NTF_1|^M = \left(4\sin^2\pi\frac{f}{f_s}\right)^M$$

- The quantization noise of an M^{th} order modulator is given by

$$v_{nq,M(rms)} = \frac{V_{LSB}}{\sqrt{12}} \cdot \frac{\pi^M}{\sqrt{2M+1}} \cdot \frac{1}{OSR^{M+1/2}}$$