Transient on TL 11/1/04

Important Subjects in Time-Domain Responses

(1) Unit step function responses (covered in EE361)
(2) Delta-I noise
(3) Finite rise-time pulse and Laplace transform technique
(4) Pulse on lossy transmission lines and dispersion
(5) Forward and backward coupled noise (To be covered in the coupled line)
(6) Time-domain measurement techniques

Ref: HP application note 1304-2 (Web page)

1. Unit Step Function Response from a Resistive Load

A digital signal on PCB (microstrip or stripline TL) is not a continuous wave. Rather it is a square (or pseudo square) pulse train which contains many frequency components. In this section, we will study the responses of matched and unmatched TL in time-domain. This is called "Transient Response".

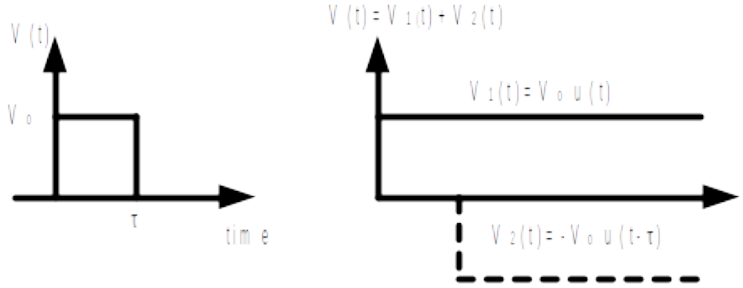
Applications:

-TDR is an instrument which combines a high speed step function generator and fast oscilloscope scope. The reflection from an unmatched impedance can be detected. Example: Computer network.

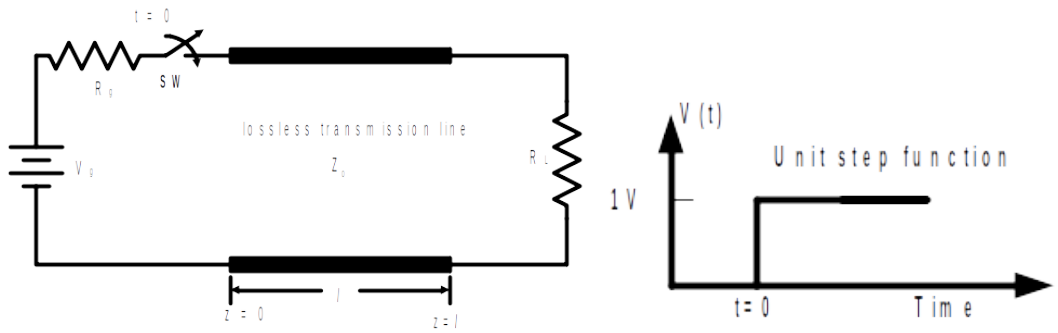
-Optical TDR is similar to TDR but it uses a short pulse to find a faulty optical fiber cable.

Rectangular Pulse:

Assume the input signal is a pulse of duration τ which can be expressed as a sum of two unit step functions as shown below. Therefore, once we find the circuit response to a unit step function, we can obtain the circuit response to a rectangular pulse.



The unit step function can be created by closing and opening a switch at the source side as shown below.

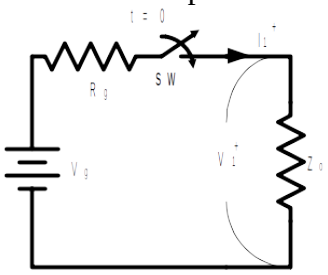


Rg: source impedance
SW is closed at t=0

TL Response to a Unit Step Function

Initial Condition

Let us assume the SW is closed at t=0. First, we need to find a initial voltage and current which propagate into the TL from the source. When the rise-time (voltage step) arrives at a TL, it does not see the load (R_L). Instead, it sees the TL which has a characteristic impedance of Z_o. Therefore, the voltage going into the TL is given by a voltage divider between the source impedance and Z_o.

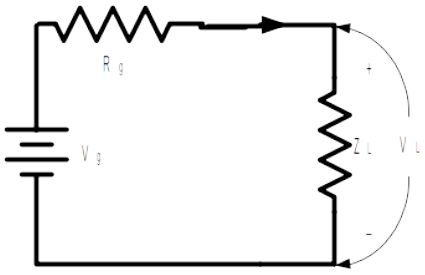


$R_g=4\ Z_o$
$Z_L=2\ Z_o$
$V_g=1V$

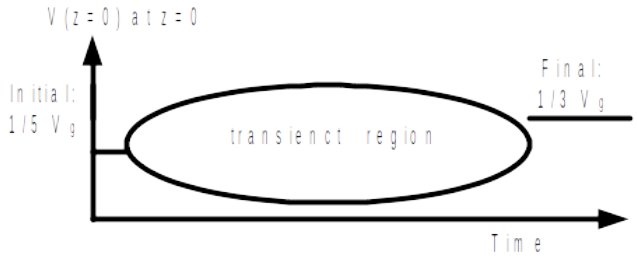
$$V_1^+ = I_1^+ Z_o \quad , \qquad I_1^+ = \frac{V_g}{R_g + Z_0} \quad , \qquad V_1^+ = \frac{V_g Z_0}{R_g + Z_0} = \frac{1}{5} V_g = 0.2V$$

Final Condition

We also need to take a look at a final condition. If the SW is ON for a long time, this corresponds to the DC voltage. The TL has no effect. The voltage on the load is given by



$$V_\infty = \left(\frac{Z_L}{R_g + Z_L} \right) Vg = 0.33V$$



The transient response is, therefore, a time response from the initial condition to the final condition.

Between Initial and Final Conditions (Transient)

The incident voltage reaches the load Z_L at t=T=l/U_p where U_p is the phase velocity on a TL. If the load impedance is not matched to the TL characteristic impedance, part of the incident voltage will be reflected. The polarity (positive or negative) of the reflected voltage depends on the load Z_L. It is positive for $Z_L>Z_o$ and negative for $Z_L<Z_o$. Although we calculate the reflected voltage using the reflection coefficient, what we can observe is the total voltage. The total voltage on a TL is the sum of all incident and reflected voltages which occur up to the observation time.

Load side $$\Gamma_L=\frac{2Z_0-Z_0}{2Z_0+Z_0}=\frac{1}{3}$$

Source side $$\Gamma_g=\frac{4Z_0-Z_0}{4Z_0+Z_0}=\frac{3}{5}$$

The first reflected voltage from the load

$$V_1^-=\Gamma_L V_1^+=\left(\frac{1}{3}\right)\left(\frac{1}{5}\right)V_g=\left(\frac{1}{15}\right)V_g$$

Total voltage is

$$V=V_1^++V_1^-=\left(\frac{1}{5}+\frac{1}{15}\right)V_g=\frac{4}{15}V_g\ \ (=0.267\,V)$$

If the source impedance R_g is matched to a TL ($R_g=Z_o$), the reflected voltage will be absorbed by the source impedance and no signal will be reflected back to the TL when the reflected voltage arrives to the source. However, the reflected voltage which arrives to the source may also see an unmatched impedance ($R_g<>Z_o$). This will create a secondary reflection from the source side which becomes a new incident voltage.

Reflected voltage from the source

$$V_2^+=\Gamma_g V_1^-=\Gamma_g\Gamma_L V_1^+=\left(\frac{3}{5}\right)\left(\frac{1}{3}\right)V_1^+=\left(\frac{3}{15}\right)\left(\frac{1}{5}V_g\right)$$

Total voltage

$$V = V_1^+ + V_1^- + V_2^+ = \left(1 + \Gamma_L + \Gamma_L \Gamma_g\right) V_1^+$$

$$= \left(1 + \frac{1}{3} + \frac{3}{15}\right)\left(\frac{1}{5} V_g\right)$$

$$= \left(\frac{23}{15}\right)\left(\frac{1}{5} V_g\right)$$

$$= \frac{23}{75} V_g \qquad (0.306\text{V})$$

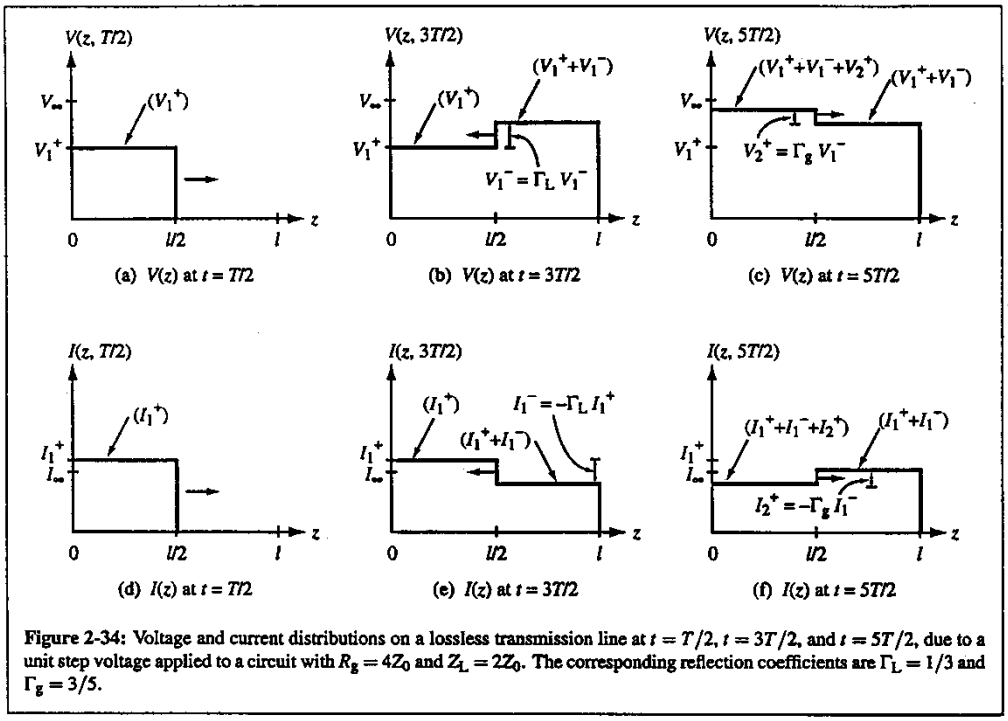


Figure 2-34: Voltage and current distributions on a lossless transmission line at $t = T/2$, $t = 3T/2$, and $t = 5T/2$, due to a unit step voltage applied to a circuit with $R_g = 4Z_0$ and $Z_L = 2Z_0$. The corresponding reflection coefficients are $\Gamma_L = 1/3$ and $\Gamma_g = 3/5$.

This multiple reflection can be shown using the bounce diagrams.

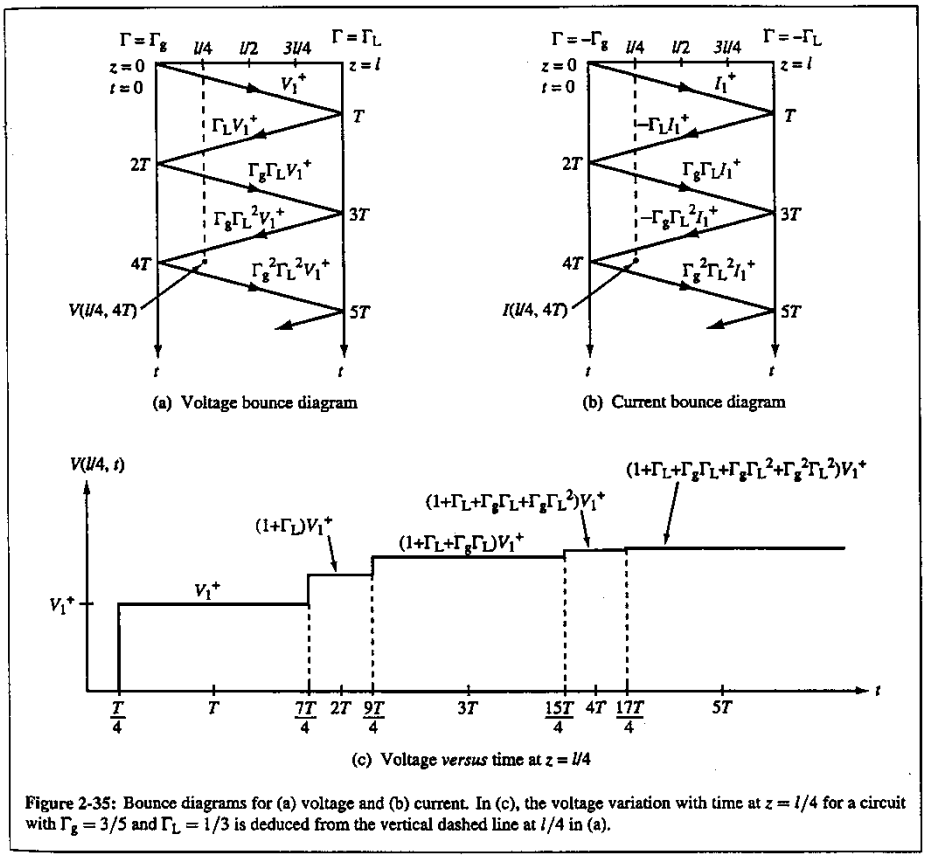


Figure 2-35: Bounce diagrams for (a) voltage and (b) current. In (c), the voltage variation with time at $z = l/4$ for a circuit with $\Gamma_g = 3/5$ and $\Gamma_L = 1/3$ is deduced from the vertical dashed line at $l/4$ in (a).

Useful formula for a infinite series

$$1+x+x^2+x^3\ldots.=\frac{1}{1-x} \qquad |x|<1$$

$$1+\Gamma_L+\Gamma_g\Gamma_L+\Gamma_g\Gamma_{L^2}+\left(\Gamma_g\Gamma_L\right)^2+\ldots=\left[1+\Gamma_g\Gamma_L+\left(\Gamma_g\Gamma_L\right)^2+..\right]+\left[\Gamma_L+\Gamma_g\Gamma_{L^2}+\ldots\right]$$

$$=\left[1+\Gamma_L\right]\left[1+\Gamma_g\Gamma_L+\left(\Gamma_g\Gamma_L\right)^2\ldots\right]$$

Using this we can get

$$V_\infty=V_1^+ +V_1^- +V_2^+ +V_2^- +V_3^+ +V_3^- \ldots$$

$$= V_1^+\left[\left(1+\Gamma_L\right)\left(1+\Gamma_L\Gamma_g+\Gamma_L^2\Gamma_g^2+\ldots.\right)\right]$$

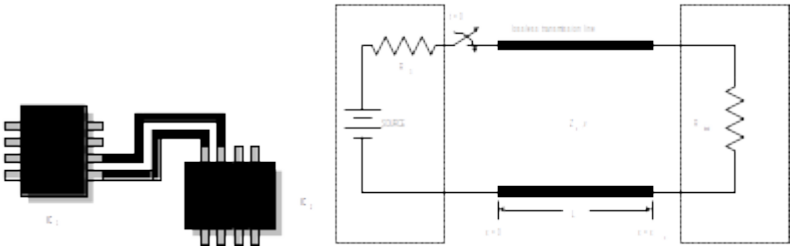
$$=V_1^+\left(1+\Gamma_L\right)\left(1+x+x^2+\ldots\right), \qquad x=\Gamma_L\Gamma_g$$

$$V_\infty=V_1^+\left(\frac{1+\Gamma_L}{1-\Gamma_L\Gamma_g}\right)=\frac{V_gZ_L}{R_g+Z_L}, \qquad 1+x+x^2+\ldots.=\frac{1}{1-x}$$

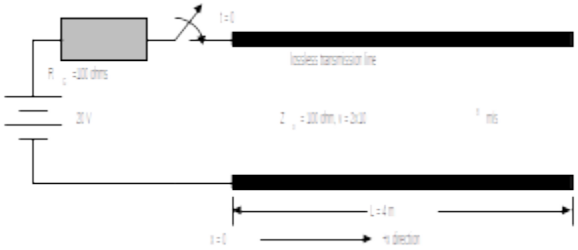
Another Reference Material

Modeling signal propagation between ICs using transmission line

Modern ICs are usually mounted on PCB and interconnected by conducting line of very high conductivity (loss characteristics can be therefore neglected). We start our study with the following example: two ICs are connected in series, with one being master (the *driving* IC - IC_1) and the other slave (the driven IC - IC_2).
This typical configuration can be modeled using this transmission line model:



Example 1: An open–circuited transmission line ($Z_{load} \rightarrow \infty$)



Describe in words and space-diagrams what happens as signal propagates from voltage source to the far-end of the transmission line.

Solution:

Consider the case of a 20 V battery with R_G = 100 ohms connected to an open–circuited, lossless transmission line. This situation, with specific values of L, *v* and Z_o, is shown in the figure above. With the initially open switch closed at t = 0, the voltage at the input to the line immediately becomes 10 V. This occurs because at the first instant, the dc source has no indication that the line is not infinite in length and hence “sees” an input impedance Z_o = 100 ohms. Thus at t = 0^+ (that is, immediately after closing the switch), the current and voltage at the input to the line are $20/(R_G + Z_o)$ = 0.10 A and 10 V, respectively. These values remain constant until the battery has some indication (via a reflected wave) that the line is not infinite in length. With the velocity given as 2 x 10^8 m/s, it takes 10 ns for **V** and **I** to travel halfway down the 4 m line. This situation is

shown in part (a) of Fig. 1. Part (b) shows the waves at t = 20^- ns (that is, slightly less than 20 ns). When the waves arrive at the open circuit, something must happen since two contradictory impedance requirements exist. First, the **V/I** ratio for the traveling wave must be Z_o = 100 ohms. On the other hand, Ohm's law at the open–circuited end of the line requires an infinite impedance since current must be zero. The creation of reflected waves ($\mathbf{V_-}$, $\mathbf{I_-}$) allows both of these requirements to be satisfied. Thus at the load end (x = 4 m, corresponding t = 20 ns),

$$\mathbf{V_{load}} = \mathbf{V_+} + \mathbf{V_-}$$

$$\mathbf{I_{load}} = \mathbf{I_+} - \mathbf{I_-}$$

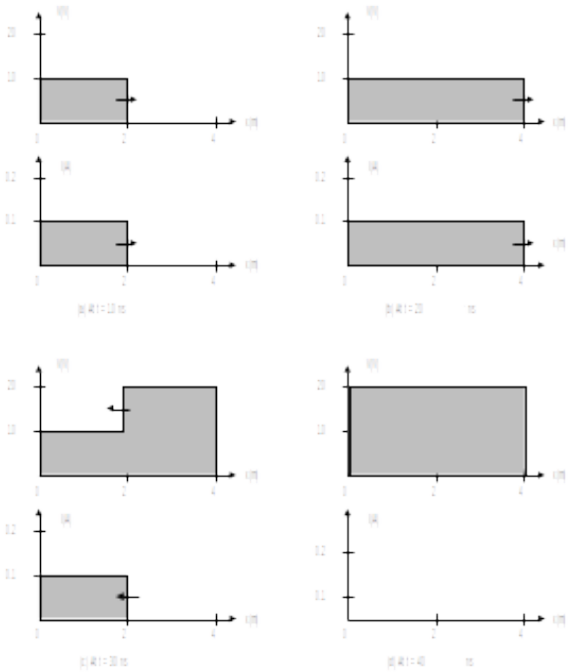


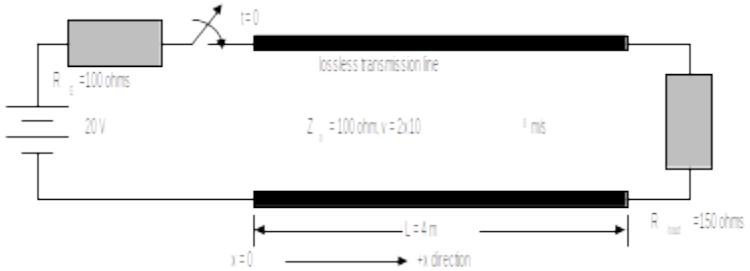
Fig. 1

The condition $\mathbf{I_{load}}$ = 0 requires $\mathbf{I_-}$ and $\mathbf{I_+}$ = 0.10 A. Also, with $\mathbf{V_+} = \mathbf{I_+Z_o}$ and $\mathbf{V_-} = \mathbf{I_-Z_o}$, $\mathbf{V_-} = \mathbf{V_+}$ = 10 V. Therefore, $\mathbf{I_{load}}$ = 0 A and $\mathbf{V_{load}}$ = 20 V at the load end.

The open-circuit condition at the load end creates reflected voltage and current waes of 10 V and 0.10 A, respectively. These waves travel in the negative x direction with the same velocity as the incident (transmitted) waves. Part (c) and (d) of Fig. 1 show the resultant voltage and current (due to the sum of + and

- waves) at t = 30 ns and 40 ns. As the wavefront of the 10 V, 0.10 A reflected waves moves to the left, it leaves behind a net voltage of 20 V and a net current of zero. Since R_G = 100 ohms, both Ohm's law and the condition that $\mathbf{V}_-/\mathbf{I}_-$ = 100 ohms are satisfied at t = 40 ns, and hence no reflections are required at the generator end. The process thus ends and a steady state is achieved with **V** = 20 V and **I** = 0 A everywhere on the transmission line. The time-flow plots of these incident and reflected signals as a function of distance and time are shown on the next page.

Example 2: A resistively terminated transmission line (Z_{load} : real number)



Describe in words and space-diagrams what happens as signal propagates from voltage source to the far-end of the transmission line.

Solution:

Consider now the case of a finite length transmission line terminated with a pure resistance. This situation is shown above, where R_{load} (= 150 ohms) is the terminating or load resistance. As before, closing the switch initiates a 10 V, 0,10 A forward traveling wave. At t = 20 ns, the wave arrives at the load end. Since $R_{load} \neq Z_o$, Ohm's law can only be satisfied by assuming reflected waves. Thus at z = 4 m, $\mathbf{V}_{load} = \mathbf{V}_+ + \mathbf{V}_-$ and $\mathbf{I}_{load} = \mathbf{I}_+ - \mathbf{I}_- = (\mathbf{V}_+ - \mathbf{V}_-)/Zo$. Ohm's law requires $\mathbf{V}_{load}/\mathbf{I}_{load} = R_{load}$ and hence

$$R_{load} = Z_o(\mathbf{V}_+ + \mathbf{V}_-) / (\mathbf{V}_+ - \mathbf{V}_-) = Z_o[\ 1 + (\mathbf{V}_-/\mathbf{V}_+)\ ] / [\ 1 - (\mathbf{V}_-/\mathbf{V}_+)\ ]$$

$$= Z_o(1 + \Gamma_{load}) / (1 - \Gamma_{load})$$

Solving for the load reflection coefficient yields

$$\Gamma_{load} = (R_{load} - Z_o) / (R_{load} + Z_o)$$

(compare this with $\boldsymbol{\Gamma_{load}} = (\mathbf{Z_{load}} - Z_o) / (\mathbf{Z_{load}} + Z_o) = \mathbf{V}_-(x=0) / \mathbf{V}_+(x=0)$
on page 3 of this handout).

For resistively terminations, $\boldsymbol{\Gamma_{load}}$ is real and can take on any value between –1 and +1. If $R_{load} = 0$ (short circuit), $\boldsymbol{\Gamma_{load}} = -1$, while if $R_{load} = \infty$ (open circuit, the previous case), $\boldsymbol{\Gamma_{load}} = +1$.

In the present case for $R_{load} = 150$ ohms, $\boldsymbol{\Gamma_{load}} = 0.2$. With the forward wave equal to 10 V and 0.10 A, the reflected voltage and current are 10 V $\times$ 0.2 = 2 V and 0.10 A $\times$ 0.2 = 0.02 A, respectively. Parts (a) and (b) of Fig. 2 shows the voltage and current along the line at t = 10 ns and 30 ns. At t = 10 ns, only the forward traveling waves exist, having arrived only at the halfway point of the 4 m line. At t = 30 ns, the reflected waves have been generated and have traveled halfway back toward the generator end of the line. At t = 40 ns (not shown), the reflected waves arrive at the input and the resultant voltage and current everywhere along the line become 12 V and 0.08 A. Since $R_G = Z_o$, no reflection is required at the generator end and the steady state is achieved after 40 ns. Note that the final values (12 V and 0.08 A) are those expected from a dc analysis of the circuit.

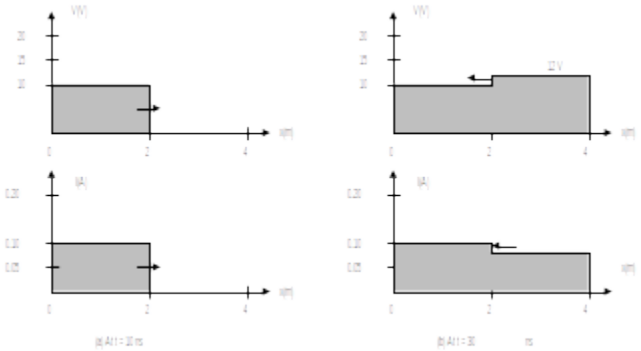


Fig. 2

<u>Example 3</u>: Multiple reflections on a transmission line

From the above cases, it is clear that when $R_G = Z_o$, the steady state is achieved after one round trip (40 ns, in our example). On the other hand, if $R_{load} = Z_o$, the steady state occurs after an *one-way* trip (20 ns, in our example). Let us now explore the situation when neither R_G nor R_{load} is equal to the characteristic impedance Z_o. The analysis will show that reflections occur at both ends of the line and the steady start values are approached only as t becomes *infinite*!

Describe in words and space-diagrams what happens as signal propagates from voltage source to the far-end of the transmission line.

Solution:

As a specific example, consider the circuit above, where R_G = 200 ohms, R_{load} = 25 ohms, and Z_o = 100 ohms. When the switch is closed at t = 0, the 90 V source sees 200 ohms in series with the characteristic impedance of the line. Therefore, the current and voltage at the input end of the line (x = 0) are initially $\mathbf{I}_+$ = 90/300 = 0.3 A and $\mathbf{V}_+ = \mathbf{I}_+ Z_o$ = 30 V. After 20 ns, the $\mathbf{V}_+$ and $\mathbf{I}_+$ waves arrive at the load end where the reflection coefficient $\boldsymbol{\Gamma}_{\mathbf{load}}$ = (25 - 100)/(25 + 100) = -75/125 = -0.6 and hence $\mathbf{V}_- = \boldsymbol{\Gamma}_{\mathbf{load}} \times \mathbf{V}_+$ = -18 V and $\mathbf{I}_- = \boldsymbol{\Gamma}_{\mathbf{load}} \times \mathbf{I}_+$ = -0.18 A. At the end of 3o ns, the voltage between x = 2 m and x = 4 m is reduced to 30 - 18 = 12 V, while the current has increased to 0.3 + 0.18 = 0.48 A. The progress of the voltage wave along the line is shown in Fig. 3 for t = 30, 50, 70, and 90 ns.

Let us observe the voltage wave as time marches on. At the end of 40 ns, the -18 V wave arrives at the input where it sees an impedance R_G = 200 ohms. Since $R_G \neq Z_o$, a reflection occurs at the generator end. By analogy with $\boldsymbol{\Gamma}_{\mathbf{load}}$, the generator reflection coefficient $\boldsymbol{\Gamma}_{\mathbf{G}}$ is given by

$$\boldsymbol{\Gamma}_{\mathbf{G}} = (R_G - Z_o) / (R_G + Z_o)$$

For R_G = 200 ohms, $\boldsymbol{\Gamma}_{\mathbf{G}}$ = 1/3 and hence a –6 V wave is reflected towards the load end. At t = 50 ns, it has progressed halfway down the line, leaving behind it a voltage of (30 – 18 – 6) = 6 V. This is shown in part (b) of the figure. At t = 60 ns, the –6V wave arrives at the load which generates a reflected wave of value (–6) $\times$ $\boldsymbol{\Gamma}_{\mathbf{load}}$ = +3.6 V. The situations at 70 and 90 ns are also shown in the figure. Note that at t = 90 ns, another forward traveling wave exists having a value (+3.6) $\times$ $\boldsymbol{\Gamma}_{\mathbf{G}}$ = +1.2V. This process continues indefinitely with the amplitude of the re-reflected waves getting smaller and smaller (due to energy dissipation of the resistors). A plot of voltage versus time at any fixed point on the line would show that, in the limit, the voltage becomes the expected dc value (namely, $90R_{load}/(R_G + R_{load})$ = 10 V). Such a plot at x = 0, the input, is shown in Fig. 4. Every step in voltage represents the arrival and generation of the reflected waves at the input. After five round-trip (200 ns), the voltage is within 0.10 percent of the steady-state value.

It is interesting to note that the voltage shown in Fig. 4 is oscillatory as it approaches its final value. The period of this ringing effect is 80 ns (twice the round-trip time) and hence its reciprocal is the natural resonant frequency of the circuit, namely, 12.5 MHz. Since $v = 2 \times 10^8$ m/s, this means that the line is $\lambda/4$ long at the resonant frequency. Thus we see that by connecting a dc source to a transmission line, high frequency oscillations are possible. In a PCB system, the emitted power from these high-frequency oscillations, if left unchecked, will result in interference to other devices, impairing the performance of the overall system.

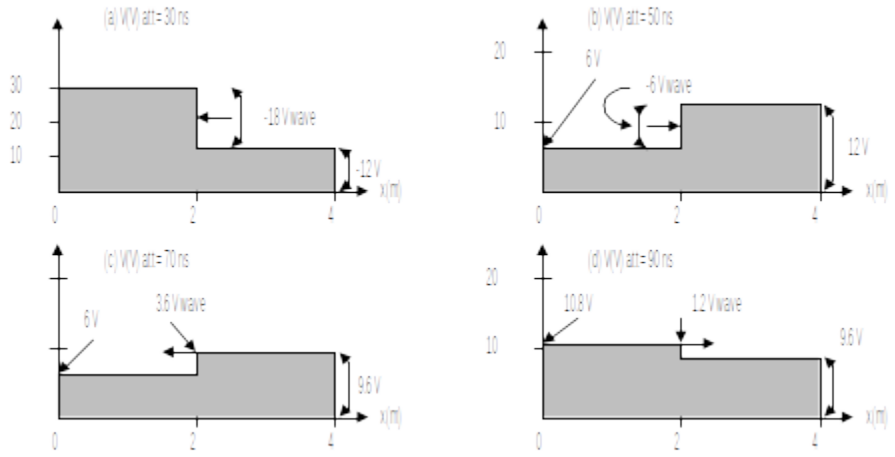


Fig. 3

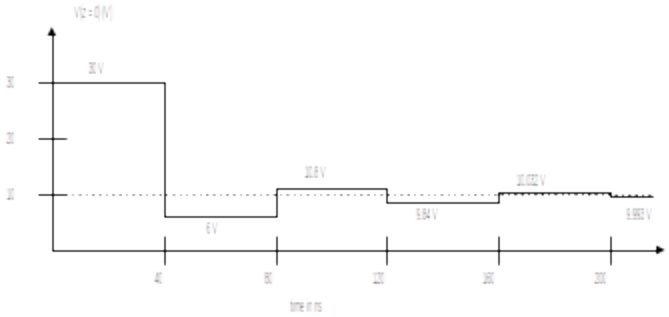


Fig. 4

2. Space-Time Representation of Signals

The space-time diagram is a graphical aid in determining the voltage and current as a function of either time or position along the line. Fig. 5 shows the diagram for the circuit in Example 3. The abscissa indicates position along the line and the ordinate represents the time scale, t = 0 being the moment that the switch is closed. For reference, the values of Γ_G and Γ_{load} are given at the top of the diagram. The lines sloping downward and to the right represent forward traveling waves, while those sloping down and to the left represent reverse waves. The voltage and current values for the particular wave are shown above and below the sloping line. As explained, the load end creates reflections equal to Γload of the arriving wave. Generator reflections are equal to Γ_G times the value of the wave arriving at the generator end.

To illustrate, Fig. 5 will be used to determine the voltage and current at x = 2 m. Each intersection of a sloping line with the interval x = 2 m line represents the arrival of a wavefront. For t < 10 ns, no intersection exists and hence both **V** and **I** are zero. For 10 < t < 30 ns, there is one intersection which means **V** = 30 V and I = 0.30 A. For t > 30 ns, the voltage is the sum of all the forward and reverse waves that have passed the x = 2 m location. For example, at t = 80 ns, **V** = 30 - 18 - 6 + 3.6 = 9.6 V. The current may be determined in a similar manner except that current values associated with reverse waves must be subtracted from those associated with the forward waves. For example, at t = 80 ns, **I** = 0.30 - (-0.18) + (-0.06) + (-0.06) - (+0.036) = 0.384 A. The diagram may also be used to determined voltage and current versus x for a fixed time by drawing a horizontal line corresponding to the particular value of time. The sum of voltages above the line corresponds to the voltage at that point on the line. The same applies to the current except that, as before, reverse-traveling current waves must be subtracted from forward-traveling current waves.

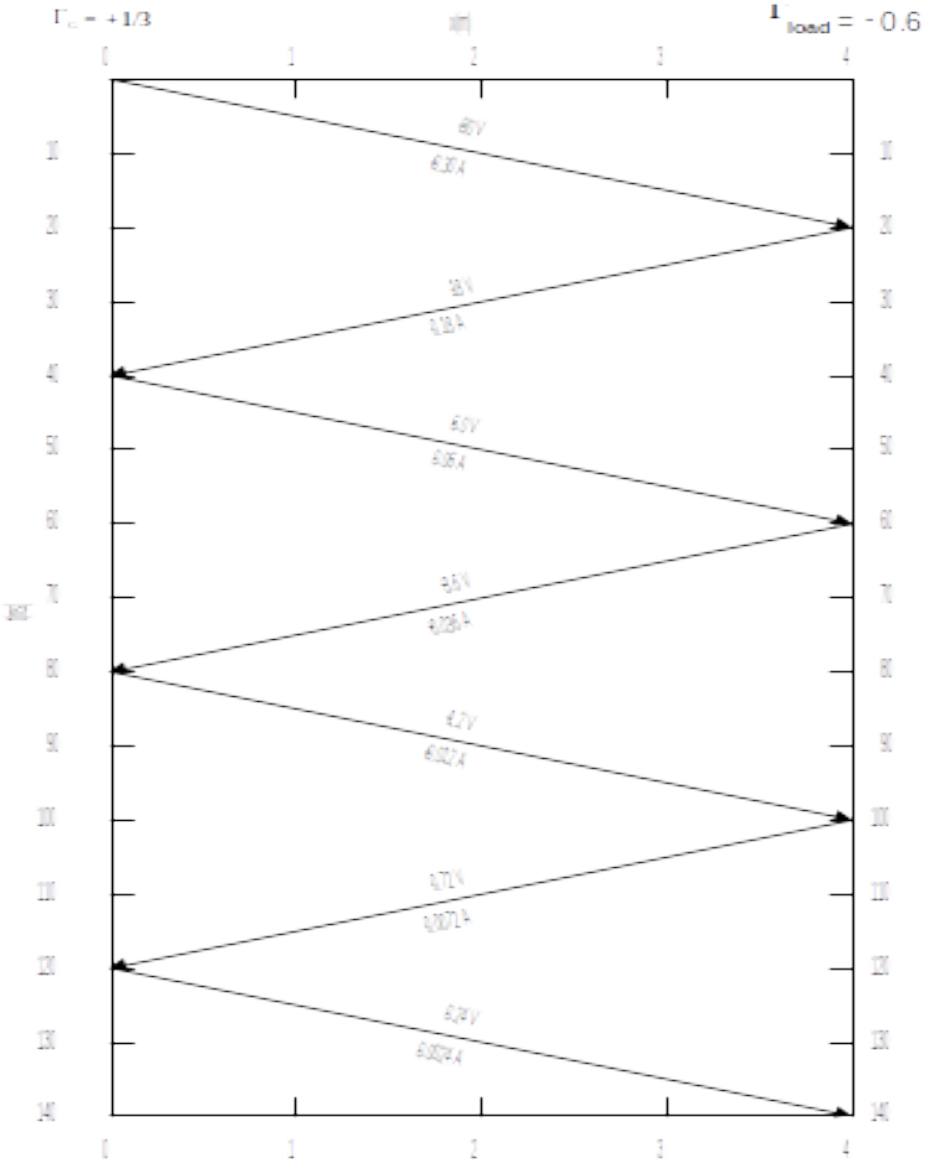


Fig. 5

3. Some examples of transient responses

Incident and Reflected short pulses from a TL with SHORT

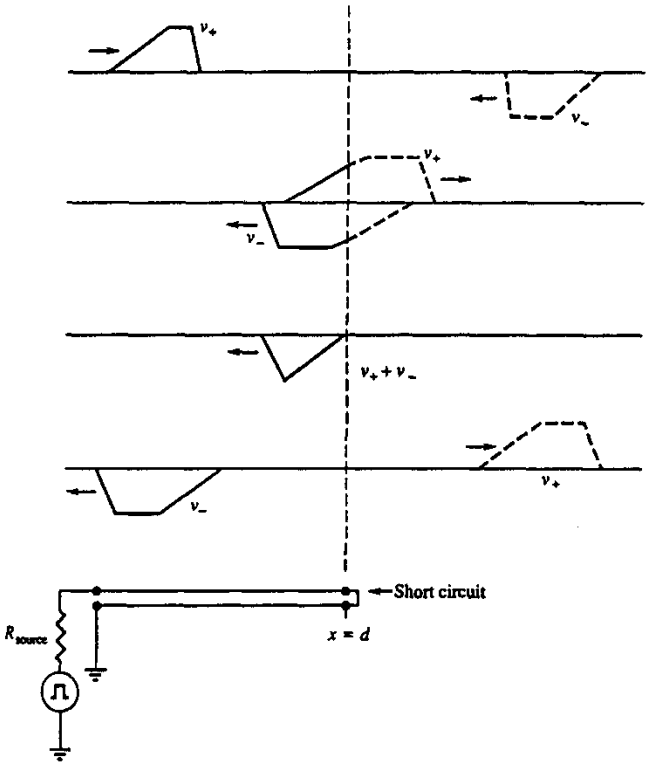


FIGURE 3-8
Snapshot of incident and reflected waves as a function of position on a transmission line terminated with a short circuit. Reflected wave is mirror image of incident wave, and is inverted in sign. Reflection coefficient is $r = -1$.

Transient in cascaded logic circuits

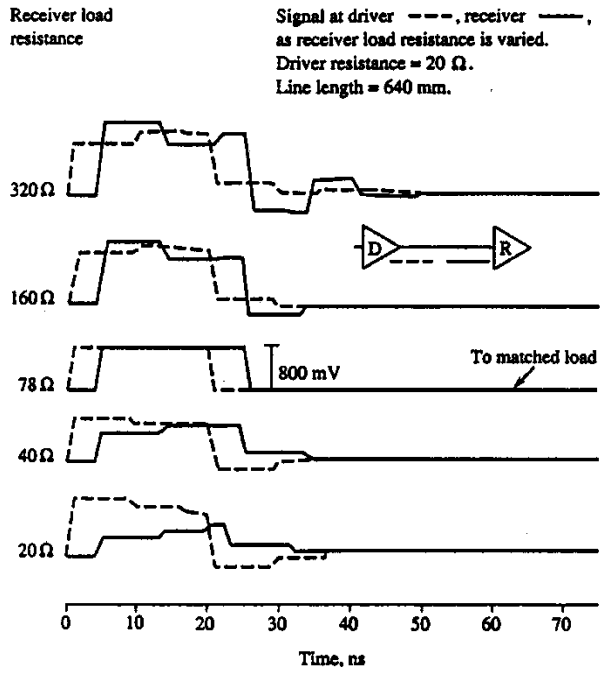


FIGURE 3-9
Multiple reflections on a transmission line. Signal at driver and receiver, driver resistance fixed at 20 Ω. R_T is varied from low to high values. Characteristic impedance Z_0 of line is 78 Ω. Driving waveform is a 20-ns wide trapezoidal pulse with 1 ns rise and fall times and 1 V peak amplitude into an open circuit.

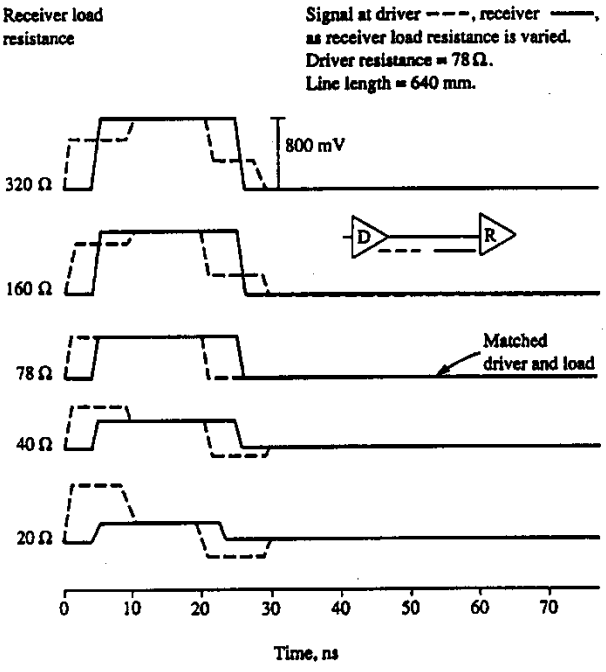


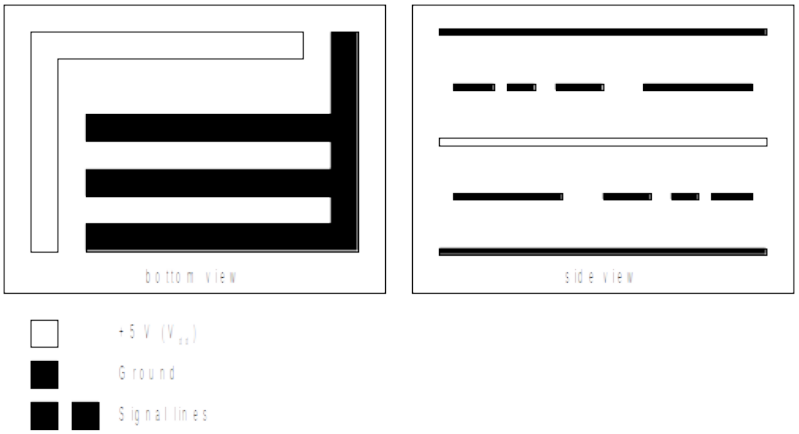
FIGURE 3-10
Same as Figure 3-9, but driver resistance is 78 Ω.

4. Power Requirements for High-Performance PCB and Delta-I Noise

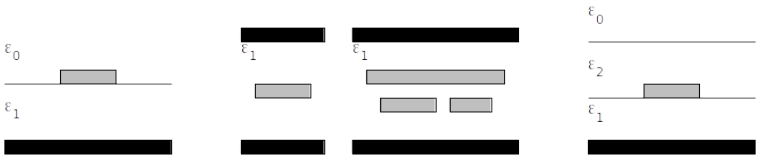
- Stable voltage level at all IC modules
- Uniformity of voltage levels to all parts
- Adequate amount of current under varying conditions

DC Power Distribution on a PCB

A typical multi-layer PCB looks like



Besides multi-layer PCB geometry, other common PCB structures are as follows:

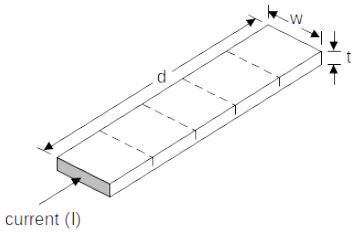


In a computer system, DC power is supplied to the electronic circuit chips at a specific set of voltages. In large computer systems, the current required may exceed 500 A, at a voltage of 1.5-3.0 V. In these systems, DC power may be distributed with large rectangular copper bus bars instead of wires.

The delivery of DC power is best controlled by designing the path from the power supply to the circuits to have as little ohmic resistance as possible. A procedure for calculating the resistance of rectangular bus bars and printed circuit traces is developed here.

Electrical Resistance

Many electrical conductors used in electronic packaging are formed from rectangular-shaped sections. A useful concept for calculating the DC resistance of these conductors is the *sheet resistance*. Consider the following rectangular resistor section:
The resistance of this resistor is given by $R = \rho d / A$, where A is the cross-section area (in cm^2) of the resistor and ρ the resistivity (in Ω-cm) of the material that makes up the resistor. Given a thickness of t and width of w, one has the following expression



$$R = \rho d / (wt) = (\rho / t) * (d / w) = R_{\bullet} * N_{\bullet}$$

where $R_{\bullet}$ = sheet resistance (in Ω / •) and $N_{\bullet}$ = number of squares (•) of length w along the resistor length d.

Example: Resistance Calculation

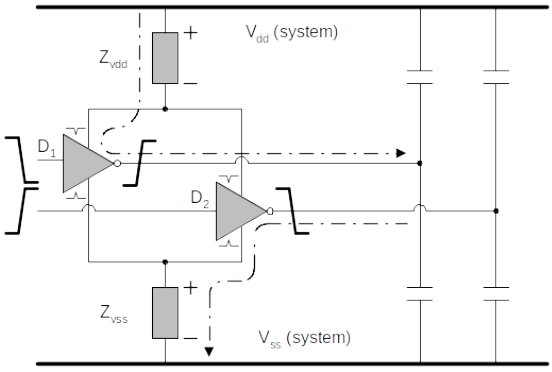
> Given a 200-mm-long printed circuit line of width 0.1 mm (made of 1-oz copper, whose resistivity is 1.8 μΩ-cm), compute its DC resistance. (Note: Copper sheet thickness is usually specified in terms of weight per area. 1-oz copper denotes a sheet that weighs 1 oz / ft^2 with a thickness of 35.6 μm.)

Solution:

> $N_{\bullet} = d / w = 200 / 0.1 = 2000$ •
>
> $R_{\bullet} = \rho / t = 1.8 \times 10^{-6} \times 10^{-2} / (35.6 \times 10^{-6}) = 5.06 \times 10^{-4}$ Ω/•
>
> ⇒ DC resistance = $R_{\bullet} \times N_{\bullet} = 5.06 \times 10^{-4} \times 2000 =$ **1.01 Ω**
>
> If the current is 200 mA, the voltage drop due to this copper line is about 200 mV.
>
> Q: What if one uses a wider line, say d = 200 mm and w = 2.5 mm?

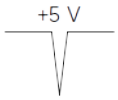
Dynamic Power Distribution on a PCB

Voltage stability is an especially important requirement for suppressing Simultaneously Switching Output (SSO) noise. SSO noise is caused by gate switching (change of current). Therefore, SSO noise is also commonly known as Δ-I noise. The following circuit illustrates this phenomenon.



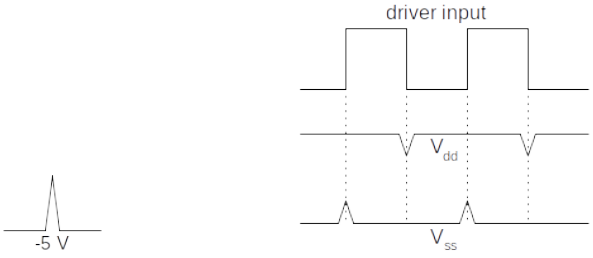
Case I.

1. HIGH-TO-LOW (hi→lo) transition at D_1 inverter input
2. LOW-TO-HIGH (lo→hi) transition at D_1 inverter output
3. D_1 inverter output *sources* large current from V_{dd} through impedance Z_{vdd}
4. Voltage drop across the *inductive* Z_{vdd} decreases the positive bias of D_1 (and D_2 too)
5. Negative voltage spike along the positive V_{dd} power line



Case II.

1. LOW-TO-HIGH (lo→hi) transition at D_2 inverter input
2. HIGH-TO-LOW (hi→lo) transition at D_2 inverter output
3. D_2 inverter output *sinks* large current to V_{ss} through impedance Z_{vss}
4. Voltage drop across *inductive* Z_{vss} increases the negative bias of D_2 (and D_1 too)
5. Positive voltage spike along the negative V_{ss} power line



In other words, current change induces Δ-I noise. The occurrence of voltage spikes owing to Δ-I noise is synchronous with the logic transitions of the input driving signal.

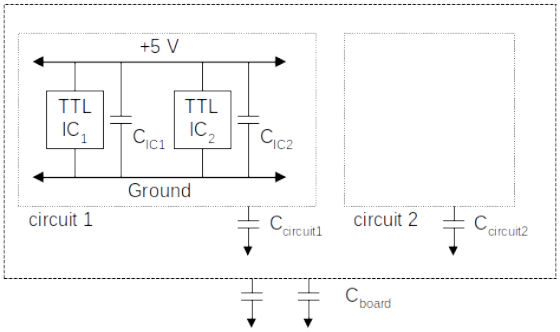
In addition, in the case when the circuit has many IC's, Δ-I noise becomes accumulative. Assume that, for instance, each IC draws 100 mA. Then, the total current for 100 IC's will be 100 × 100 mA = 10 A. Therefore, both the power and ground lines must be stable enough to handle this current load in order to minimize the Δ-I noise.

Obviously, the amount of Δ-I noise is proportional to the number of IC's that are simultaneously switching. Given a PCB system, the Power Distribution Noise (PDN) determines the number of IC's that are simultaneously switching.

Some ways to reduce PDN:

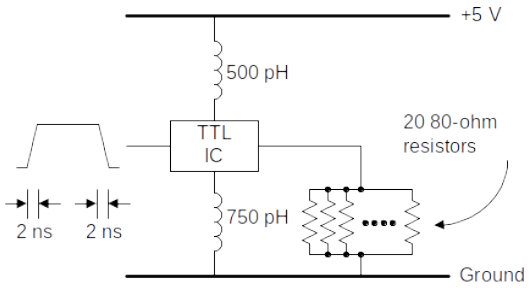
- Apply power and ground lines directly over as many signal lines as possible
- Place signal lines as close to the power and ground lines as possible
- Use by-pass (de-coupling) capacitors along the power and ground lines

The use of by-pass capacitors (with large capacitance) can be implemented at (1) IC level, (2) circuit level, and (3) board level:



Example: Power Consumption Calculation

Given a TTL IC system that consists of 20 internal amplifier sub-systems. Each of these amplifier sub-systems drives a resistive load of 80Ω. Estimate the worst-case reduction in signal swing of the IC system due to Δ-I noise.



Solution:

Since each amplifier sub-system output is attached to a 80Ω load, the corresponding source current (I_{source}) at HIGH state = 5/80 = 62.5 mA. During a 2-

ns period of rise time and fall time, the time-change (di/dt) of I_{source} = 62.5/2 = 31.3 mA/ns

The voltage drop across the 500 pH inductor due to 20 amplifier sub-systems = N * L * di/dt = $20 * 500 * 10^{-12} * 31.3 * 10^{-3} / 10^{-9}$ = 0.31 V

Likewise, the voltage drop across the 750 pH inductor due to 20 amplifier sub-systems = N * L * di/dt = $20 * 750 * 10^{-12} * 31.3 * 10^{-3} / 10^{-9}$ = 0.47 V

Thus, the worst-case signal swing of the whole IC system is 5 - 0.31 - 0.47 = **4.22 V**

Note: Typical digital signal exhibits rise time on the order of ns:

IC Fabrication Technology	**rise time**
ECL (emitter-coupled logic)	1 ns
TTL (transistor-transistor logic)	4 ns
High-speed CMOS (complimentary metal oxide semiconductor)	10 ns
CMOS	50 ns

Potential Problems:

- Latch circuit may change state due to the voltage drop, causing logic error or even triggering undesirable operations.
- Quiet lines are particularly prone to the effect of Δ-I noise, resulting in logic errors and/or timing errors.
- The transient voltage spikes produced by one circuit can propagate through the power/ground lines to other circuits, potentially resulting in the failure of the entire PCB system.