Final Project: 2.4 GHz Balanced Amplifier Design 2020

Project Report Due: 4:00 p.m. on March 18(Wed), 2020

Important layout information:

The min gap width is 0.5mm.

The min TL width is 0.4mm

Your final layout should be clean and pleasant to look at.

I. Objectives:

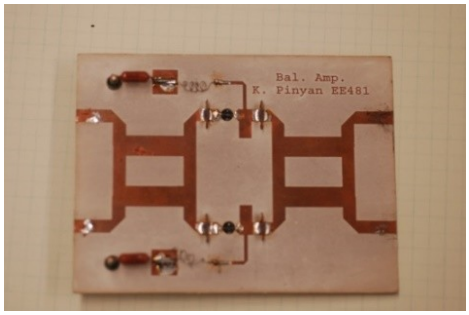
To design a balanced amplifier at 2.4 GHz. The circuit must include DC bias sections and decoupling capacitors.

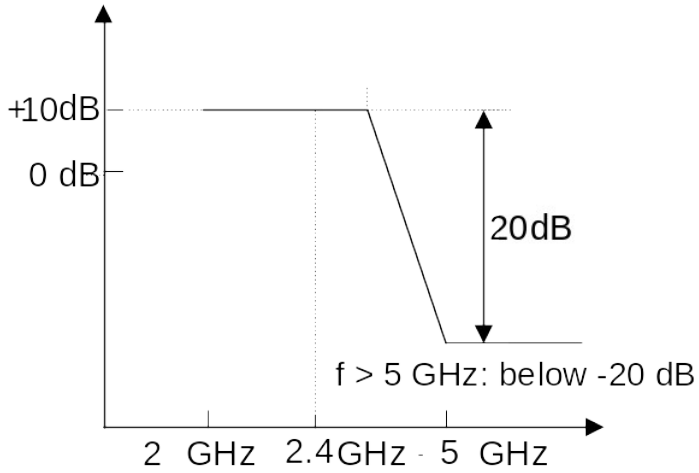
Requirements

+10 dB gain at 2.4 GHz

At least -20 dB attenuation at 5 GHz *wrt* 2.4 GHz.

No gain requirement below 2.4 GHz.





II. Supplies:

PC board

Roger Duroid 5870, 0.5 oz copper

Duroid 5870, ε_r=2.33 - *j*0.0028, d=1.57mm (62 mil)

Two SMA connectors

Capacitors: Custom-made for less than 10 pF

Chip capacitor for 10 pF, 47 pF, and 100pF

Feedthru cap 1000pF

Chip capacitor spects are available at the EE572 class site.

Two ERA-2SM+ : Use specification of Id=48mA at 25C degree

ERA_2SM_48mA_Plus25.S2P

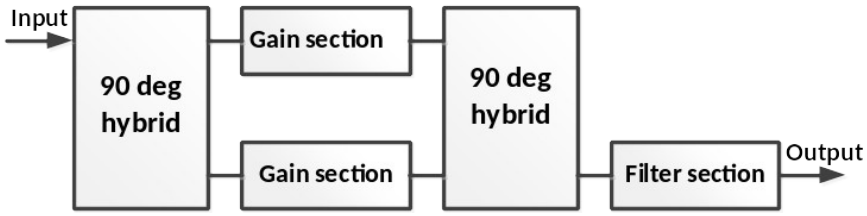
Specification: www.minicircuits.com

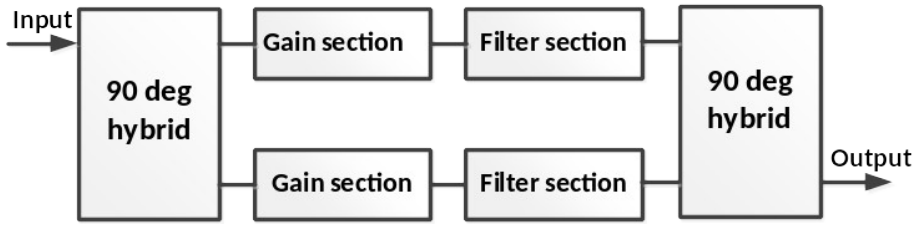
ERA-2SM+ data file is available at the EE572 class site.

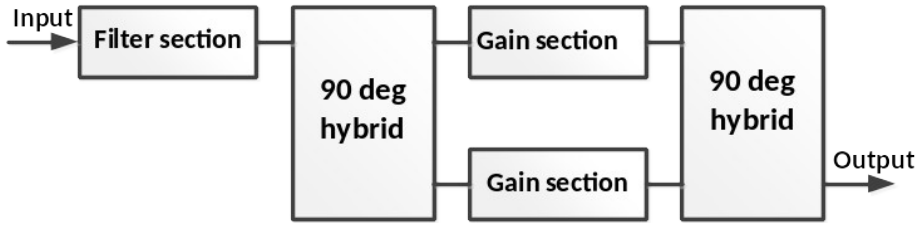
Also at http://www.minicircuits.com/sparameters.html

III. Design Process

To satisfy the design requirements, you need to come up with a block diagram and the function/parameter of each block. In this project you must use a balanced amplifier shown in Appendix II. Some examples are shown here.







1. Stability Testing of ERA-2SM+
Check the stability of an amplifier (ERA-2SM+) at all frequencies. If it is conditionally stable (or untable), design input/output matching circuits.

2. Circuit Simulations Using ED
Using the ERA-2SM+ specification data, simulate the amplifier. The amplifier must have the following characteristics

Gain of at least +10 dB at 2.4 GHz

Optimize the gain at 2.4 GHz. Design matching circuits and filter to obtain a desired frequency response. As you know by now all microwave filters show unwanted passbands at high frequency and you may not be able to satisfy one of the requirements of -20 dB attenuation beyond 5 GHz.. A simple band-reject filter constructed by an open-stub/s may be useful for reducing them.

If you are using a λ/4 high-Z TL for a DC bias, add all items relevant to the microwave performance. This includes a capacitor at the end of a λ/4 TL.
Make sure to add the physical dimension of ERA-2SM+ and capacitors into the layout. (See Appendix I)

Important: All devices (amplifiers, capacitors, TLs) must be included in the ED simulations. You don't need to include a small inductor attached to the DC bias circuit.

3. EM Simulations Using ED
To reduce the simulation time, conduct the EM simulation of each block (hybrid,filters, gain media..) before conducting the simulation of the whole amplifier.

ERA-2SM+ can be included as a two-port device in the EM simulations.

IV. PCB Layout
The locations of all components including, connectors, capacitors, resister, and inductors. The ERA-2SM+ spec is given at I_d=48mA. Assume a DC sourse has 5V output. Make sure to design a DC circuit to provide this current.

Make sure to include the copper layout of all items including DC supply. Two ground pins of ERA-2SM+ should be connected to the ground thru VIA.

V. PCB fabrication (not done in 2020)

VI. Assembly of an amplifier and testing (not done in 2020)
Drill holes for a feedthru capacitor and ERA-2SM+ ground pins (VIA). Insert a feedthru cap for the power supply +5V (Do not exceed 4.1 V at the amp. 4.1 V is absolute max).

First, you need to check if an amplifer is oscillating using spectrum analyzer (SA). Terminate the input with the matched impedance (50 ohm) and connect the output to SA. If you see, any large signal (more than -10 dBm) beyond 1 GHz, the amp may be oscillating. You need to fix it. You may see small signals from wireless devices/systems but igore them.

(a) S-parameter measurement (see Measurement section)
This must be done in the amplifier linear region. The default NWA output power is close to 0 dBm and it is too high. Set the Attenuator to 20 dB so that Port 1 power level becomes about –20 dBm. If the input power level is too high, you may be measuring the gain in nonlinear region. Obtain S11, S21, S12, S22 of this amplifier.

(b) Dynamic range

(c) Third-order intermodulation

(d) Noise figure measurement

7. Format of the Final Report

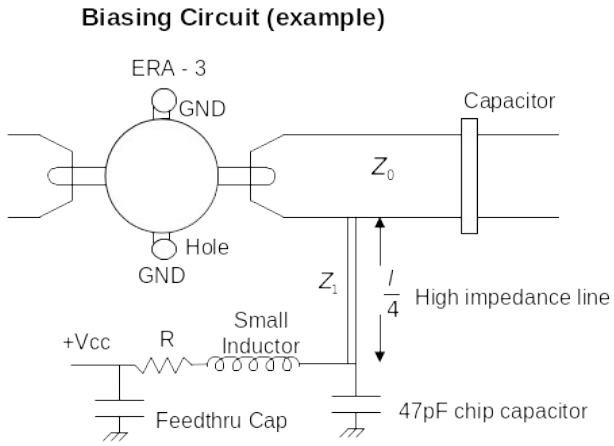
A formal report is required for the final project. The report must be written clearly and typed. All figures and results must be clearly labeled and figure captions should be attached.

The following items must be included in the final report.

1. Title page: title, name, date,.....
2. Objectives
3. Description of the project (or introduction)
4. Simulations
5. Circuit layout
6. Results
7. Discussion
8. References

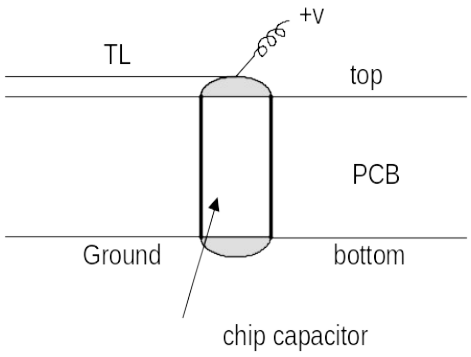
Appendix I. DC bias circuit

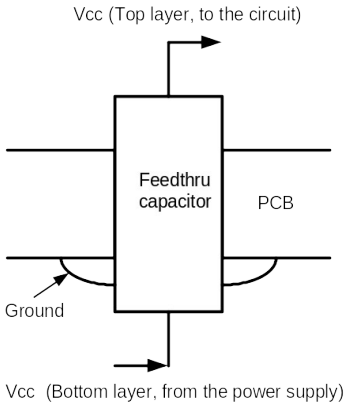
R is used for limiting current into ERA-2SM+. A small inductance is used to create an effective OPEN circuit. Assume Vcc=+5V and find R to get Id=48mA.



The end of the high-Z λ/4 line must be AC grounded by a small capacitor as shown below (left). In this example, a chip capacitor is embedded within a PCB. The chip capacitor can also be located on the PCB but one side must be grounded using a VIA. The RF block coil should not have many turns (**2-3 turns are sufficient**).

The feedthru cap (right) is for attaching the DC wires on the bottom side of PCB. The clean top PCB surface will reduce a potential problem.





Examples

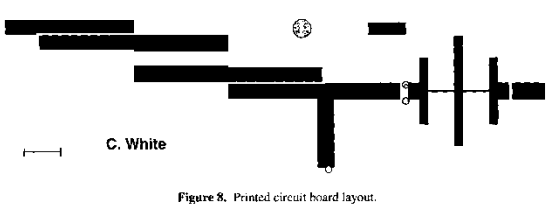
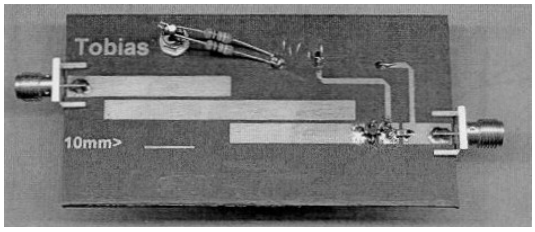
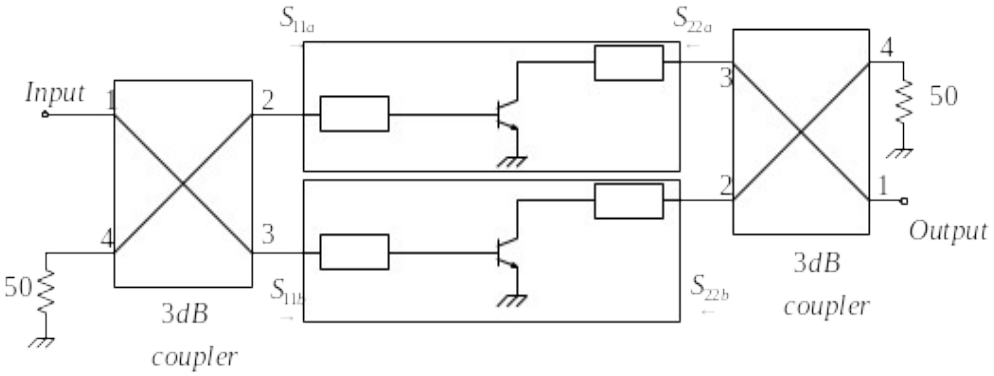


Figure 8. Printed circuit board layout.



Appendix II. Balanced Amplifier



Note: Numbering of 1st and 2nd hybrid is not the same. Output is at port 1.

90 deg hybrid and Input signal

$$[S] = -\frac{1}{\sqrt{2}}\begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix}, \quad \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix}_{1st} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

After the first 90 deg hybrid

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix}_{1st} = -\frac{1}{\sqrt{2}}\begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix}\begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 \\ \frac{-j}{\sqrt{2}} \\ \frac{-1}{\sqrt{2}} \\ 0 \end{bmatrix}$$

After the second 90 deg hybrid

Note b2 of 1st becomes a3 of 2nd . Similarly b3 of 1st becomes a2 of 2nd.

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix}_{2nd} = (G_{amplifier}) * (-\frac{1}{\sqrt{2}})\begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix}\begin{bmatrix} 0 \\ \frac{-1}{\sqrt{2}} \\ \frac{-j}{\sqrt{2}} \\ 0 \end{bmatrix} = (G_{amplifier}) * \begin{bmatrix} j \\ 0 \\ 0 \\ 0 \end{bmatrix}$$