EE 332 **Circuits and Devices II** **Autumn 2022**

Homework 3 **Due: Oct. 28th (11:59 PM)**

1. ***Razavi 3.10 (Only part a)***

VDD=3V. Assume threshold voltages from table 2.1 (uploaded to Canvas).

Consider the circuit of Fig. 3.13 with $(W/L)_1 = 50/0.5$ and $(W/L)_2 = 10/0.5$. Assume that $\lambda = \gamma = 0$.

(a) At what input voltage is M_1 at the edge of the triode region? What is the small-signal gain under this condition?

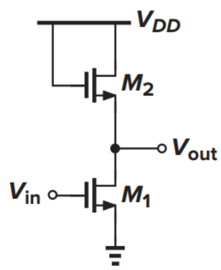
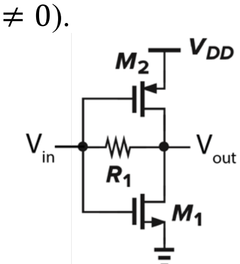


Figure 3.13 CS stage with diode-connected load.

2. Remember the amplifier with both NMOS and PMOS drivers we analyzed in the lecture. Here we add a resistor (R_1) in between input and output. Consider the output resistance of M1 and M2 in this problem (i.e. $\lambda \neq 0$).



a) A major disadvantage with the original circuit (before adding R_1) was that output bias was hard to determine and very sensitive to PVT variations. Explain how adding R_1 helps with this. What's the equation to determine the bias voltage for V_{OUT} as a function of V_{IN}? (Here assume $\lambda = 0$, just write down the equation)

b) Draw the small-signal model and calculate the gain (A_v) as a function of small-signal parameters (g_m, r_o) and R_1.

c) Calculate input and output impedance of the amplifier.

d) Recalculate gain using the lemma ($A_v = -G_m R_{out}$) and show it is the same as part b.

e) Another important aspect of amplifiers is how sensitive is the output to supply fluctuations/noise (on VDD). Since we can model these fluctuations with small-signal analysis, treating the VDD node as the input, derive the gain from VDD node to the output and compare that with the A_v. (*Hint:* Same small-signal model as part b, but this time V_{in} node should be AC-grounded and place a small-signal (AC) voltage source to model supply noises at the VDD node)

3. *Razavi 3.2*

For the following problem, if not specified, use the following parameters: (parameters are defined for a nominal gate length (L) of 0.5um)

$$\mu_n = 350\ cm^2/V/s$$
$$\mu_p = 100\ cm^2/V/s$$
$$C_{ox} = 77.6\ fF/\mu m^2$$
$$V_{THN} = 0.7\ V$$
$$V_{THP} = -0.8\ V$$
$$\lambda_{nmos} = 0.1\ V^{-1}$$
$$\lambda_{pmos} = 0.2\ V^{-1}$$

In the circuit of Fig. 3.18, assume that $(W/L)_1 = 50/0.5$, $(W/L)_2 = 50/2$, and $I_{D1} = I_{D2} = 0.5$ mA when both devices are in saturation. Recall that $\lambda \propto 1/L$.

(a) Calculate the small-signal voltage gain.

(b) Calculate the maximum output voltage swing while both devices are saturated.

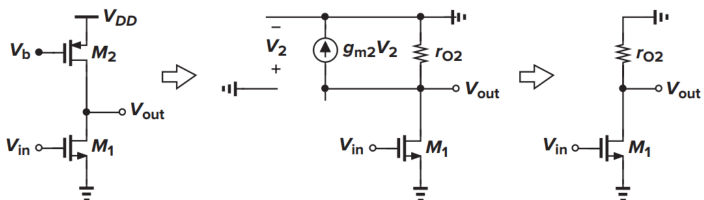


Figure 3.18 CS stage with current-source load.