EE 332 CAD Lab 2 Autumn 2022

Inverter Layout and Extraction Tutorial

Introduction

Transistor technology has come a long way since the work of *Bardeen*, *Brattain*, and *Shockley* in 1947. Integrated circuit technology packs so many devices in such a small scale that a single MOSFET device is smaller than a virus! For this reason, the physical design of integrated circuits must be performed through computing tools and mechanized interfaces.

The final stage of any chip design is called "**layout**," when designers organize the physical structure of the silicon, doping, metal, and insulators that make up an integrated circuit. This step is crucial, as the placement and connection of devices has dramatic impact on performance. The wires and devices on a chip form an array of physical capacitors, resistors, and inductors, which are not captured by schematic-level simulation. Automated analysis of a layout allows for estimation of these "**parasitic**" elements and their impact on circuit functionality, a process called "**extraction**".

This tutorial walks through the layout, extraction of a CMOS inverter.

Setting up the Free45PDK

Step 1: add the following line in your .cshrc file:

```
setenv PDK_DIR /homes/lab.apps/vlsiapps/kits/FreePDK45
```

Step 2: add following 3 line into your cds.lib in EE332/cadence:

```
DEFINE gpdk045 /home/lab.apps/vlsiapps/kits/GPDK045/gpdk045_v_6_0/gpdk045
DEFINE NCSU_Devices_FreePDK45 /home/lab.apps/vlsiapps/kits/FreePDK45/ncsu_basekit/lib/NCSU_Devices_FreePDK45
DEFINE NCSU_TechLib_FreePDK45 /home/lab.apps/vlsiapps/kits/FreePDK45/ncsu_basekit/lib/NCSU_TechLib_FreePDK45
```

Step 3: updated your display.drf file for this new PDK in EE332/cadence:

```
cp /home/lab.apps/vlsiapps/kits/FreePDK45/ncsu_basekit/cdssetup/display.drf ~/EE332/cadence
```

Now follow the lab instructions from:

https://www.brown.edu/Departments/Engineering/Courses/engn1600/Assignments/Cadence_Tutorial_EN1600.pdf

You should go through all the lab steps including building a schematic, running dc/tran simulations, making a layout cell, and run DRC & LVS (except pages 15-17).

For ADE simulation, load the HSPICE model file from:

```
/home/lab.apps/vlsiapps/kits/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include
```

For DRC and LVS check setup (page 25 and page 27):

1. If you have already created runset, load the runset file (skip to step 8) and run drc/lvs(step 6). Otherwise, close the "**Load Runset File**" form.
2. In the interactive window, select the "**Rules**" tab and use the rules from:

   DRC: /home/lab.apps/vlsiapps/kits/FreePDK45/ncsu_basekit/techfile/calibre/calibreDRC.rul

   LVS: /home/lab.apps/vlsiapps/kits/FreePDK45/ncsu_basekit/techfile/calibre/calibreLVS.rul

3. In your **terminal**, we will make a directory under ~/EE332/cadence for the drc/lvs information to be stored.

   mkdir drc

   mkdir lvs

4. Change your "**DRC Run Directory**" and "**LVS Run Directory**" to these locations so you don't flood your project space with drc and lvs files

   The DRC and LVS check setting should be similar as below:

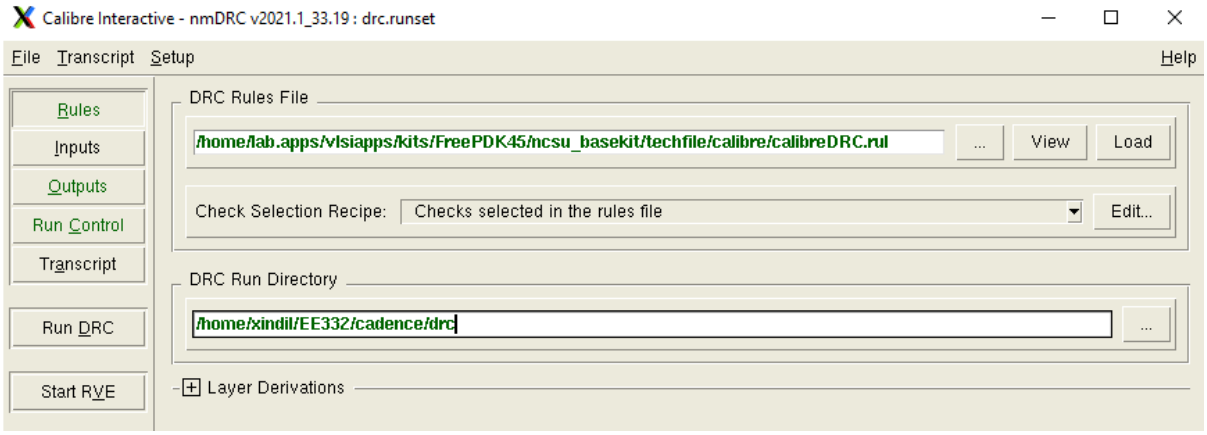

Figure 1. DRC Rules Setup

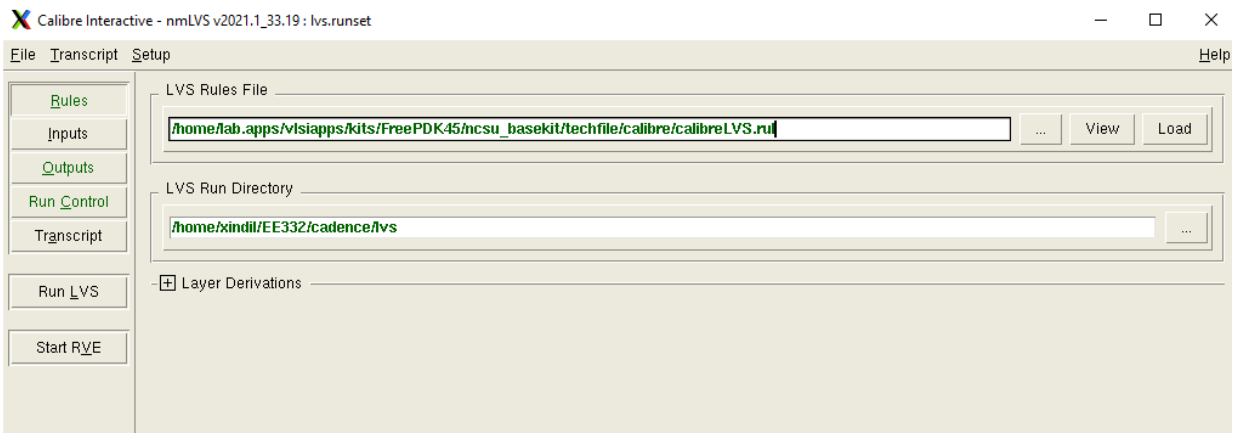

Figure 2. LVS Rules Setup

5. If you are running LVS, go to **Input** and check **Export from schematic viewer** (Page 28, Figure 44)
6. Now, select "**Run DRC**" or "**Run LVS**"
7. To save this runset, go to File-> Save Runset,

Figure 3. Save DRC Runset

8. Next time when you run DRC or LVS, you can load the runset you just created from this window

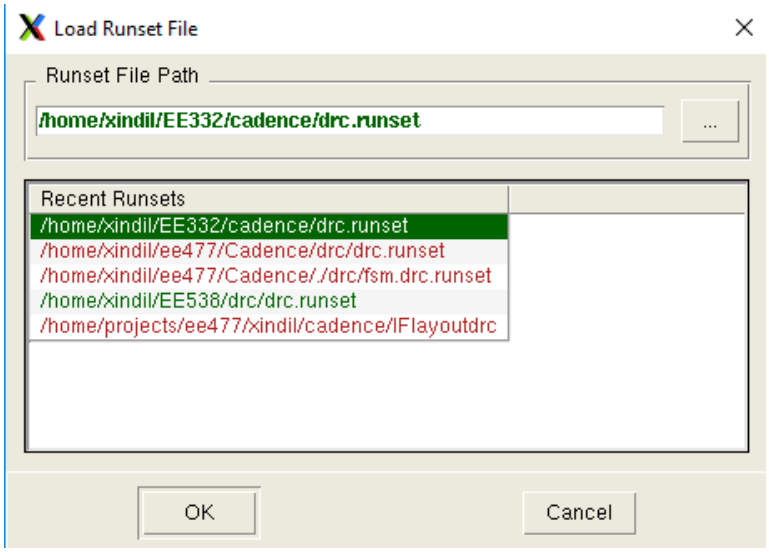

Figure 4. Load Runset File

Deliverables:

Screenshots of simulation results (dc & transient), final schematic, final layout, and clean DRC & LVS windows.