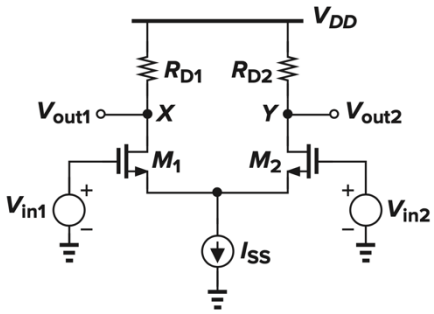
Lab 4 Differential amplifier design and simulation

Introduction

We will use **Cadence** to design and verify a basic **differential amplifier** in this lab. By the end of this lab you will learn what type of simulation setup and analysis (DC, AC, Tran.) is required measuring each metric of the circuit. Also, you will learn how to simulate differential mode (DM) and common-mode (CM) and measure them at the output.

Note – in this lab, Vdd will always be 1.0V (even if diagrams suggest otherwise).

A differential pair consists of two matched, source-coupled transistors as shown below. The difference between V_{in1} and V_{in2} is amplified as $V_{od} = V_{out1} - V_{out2}$.



Differential amplifier design

Parameter design and simulations

Design the amplifier shown above such that

$I_{ss} = 100\mu A$, Differential peak-to-peak output swing = $0.5V$, $A_d > 10dB$, Vdd = 1

Find R_D, W/L and Vin bias which will be part of CM. (this should be make the Vout the middle point of the upper and lower bound of Vin, there could have multiple designs)

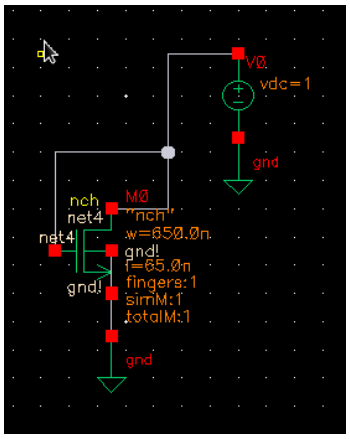
You are all experts in doing this kind of design now, normally we will directly provide parameters of transistors, e.g., $\mu_n C_{ox}$, λ_n. In this lab, you will need to extract these parameters by yourself from cadence.

Note: each technology has its own largest tolerant voltage, the largest voltage for gpdk045 is around 1.0V.

NMOS parameter extraction

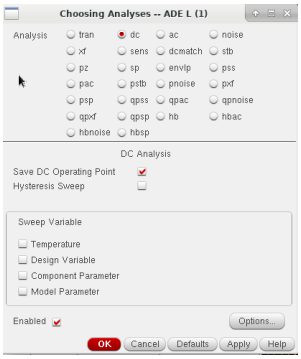
Change directory to cadence directory (people need to do **cd…** first, do not forget this!) and open cadence from the terminal. Go to **Tools->Library Manager** and create a new library **LAB4** for this lab, attach to **gpdk045** library.

Create a new schematic cellview in **LAB4** with name **EX_PA_tb**, _tb means this is a testbench cellview. It is generally a good habit to make it clear when the schematic is a testbench. In this schematic, you need to extract the transistor parameters of NMOS (you can use the same method to extract parameters for PMOS) by the following circuit.

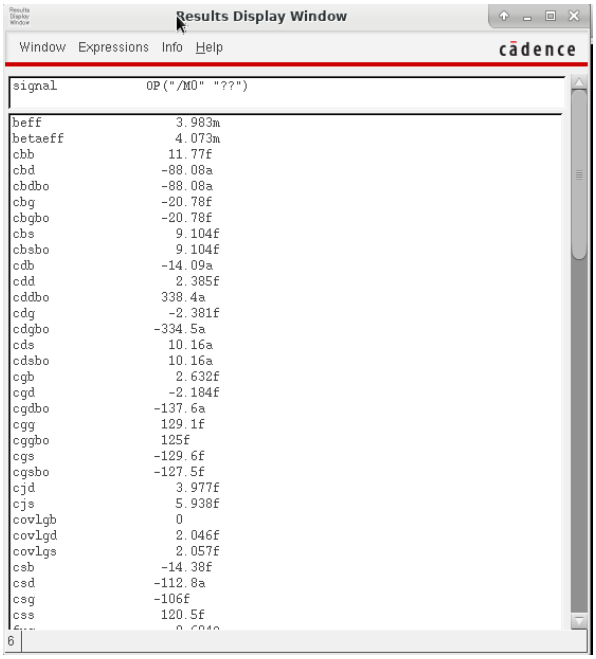


Notice the device we use is **gpdk045->nmos_1v**, all other components are from AnalogLib. For the NMOS, L=45nm and $W = 450nm$. We note the smaller the length the better the performance and 45nm is the smallest length you can get in this technology, but for smaller device the model we learnt is not accurate. This circuit assures the NMOS in saturation region, so that we can obtain the correct parameters.

After finishing building the schematic, go to **Launch->ADE L**. In the Analyses section, add a new dc simulation by right click on the blank->**edit->dc**. Make sure you check the box after Save DC Operating Point, as below, then click OK.



Go back to the ADE L and click the green run button  . After the simulation finishes (usually takes 1 sec), go to **Results->Print->DC operating Points**, then the schematic should pop up. Select the NMOS, and you will see the following report (but with different values):



These are the DC operating points of NMOS, you can check the result for example there are vgs, vth, id and so forth. One important parameter is **region,** this tells the working region of the NMOS. When region=1, it is in the triode region; when region=2, in saturation region; when region=0, the transistor is off.

To extract $\mu_n C_{ox}$, you will need to use betaeff, the second parameter in the report. The definition of this parameter is

$$\beta_{eff} = \mu_n C_{ox}(\frac{W}{L})$$

You will also need to extract V_{th}, λ_n (hint, there is a parameter r_{out} in the dc operating point report).

You will need to extract λ_n as an exercise and part of your report, also do the same exercise on PMOS. We will start our design with the necessary parameters at hand.

First-principle design

This is a simple calculation without considering the channel length modulation ($\lambda = 0$), but it is enough for first-principle design. We have

$$I_{ss} = 100\mu A$$

The differential peak-to-peak swing is given by $2R_D I_{ss}$, so

$$R_D = \frac{0.5}{2I_{ss}} = 2.5k\Omega$$

Then the gain is given by (convert from db to normal)

$$A_d = -g_{m1}R_D = -10^{\frac{10}{20}} = -3.2$$

It yields that $g_{m1} = \frac{3.2}{R_D} = 1.28 \times 10^{-3}\Omega^{-1}$

And $g_{m1} = \sqrt{\frac{2\mu_n C_{ox}(\frac{W}{L})I_{ss}}{2}} = \mu_n C_{ox}(\frac{W}{L})(V_{GS} - V_{th})$, it yields $\left(\frac{W}{L}\right)$ and $V_{GS1} - V_{th}$.

Why do we use $\frac{I_{ss}}{2}$ as I_D here? Recall the gain is maximized when current on the two arms is the same.

The next question is what common mode DC input to set? Need to determine the input swing. You will need to do the calculation by yourself. In fact, you can try different voltages in cadence and see whether the transistor is in saturation by checking the **region** in the DC operating report.

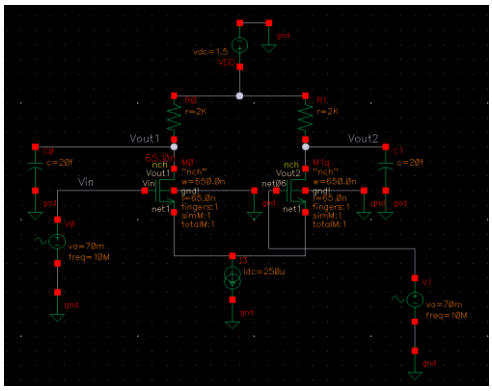
Congrats! You have finished design your first differential amplifier in gpdk045 technology! Let us run the simulation and see the performance of it. Note in the calculation, we ignored the resistance of the current source as well as the channel-length modulation. We would expect some minor discrepancies between the calculation and the simulation result.

Use the parameter provided above to verify the followings:

- DC sim to find operating points: I_d, V_{od}.
- AC sim to find: Differential gain A_d, Common-mode gain A_c.

Cadence simulation of your design!

Create a new schematic view in your LAB4 library with name DIFF_AMP1_tb. Build the following circuit:



Except for the NMOS, all the other components are from AnalogLib, they are "idc","vsin","cap","gnd","res". In NMOS, set $L = 45nm$, $W = 450nm$ as we designed. Set the resistance of "res" as $2.5k\Omega$. Note that since we use long channel model for the transistors, also we ignore the channel length modulation and body effect, our calculation is not so accurate. Thus the simulated performance would be much worse than we expect. You will need tune the parameters R and W/L so that the performance can be improved to meet the design requirement.

The parameters in vsin are worth mentioning. DC voltage is clear, for dc simulation. AC magnitude and AC phase are for ac simulation. Amplitude and initial phase for Sinusoid are for trans simulation. You should set the parameters for dc and ac simulation as follows: (why the Amplitude is 80mV? Due to output swing and gain requirement).

A note about AC simulation – Cadence does AC simulations with a small signal model. It looks at the DC biasing and then decides how the circuit will behave in a linear manner if a very small input is applied. However, it will apply this linear model no matter how large your "AC magnitude" is. The circuits we are designing are clearly non-linear (hence the multiple operating regions of the transistor), so this can be confusing. For example, if your circuit here has a gain of 10 and then AC magnitude of your input voltage source is 1V, then the output will show a swing of 10V. We know that this cannot happen in real life (the supply voltage is 1V), so this just gives us a sense of the magnitude of amplification, not of actual values that can take place.

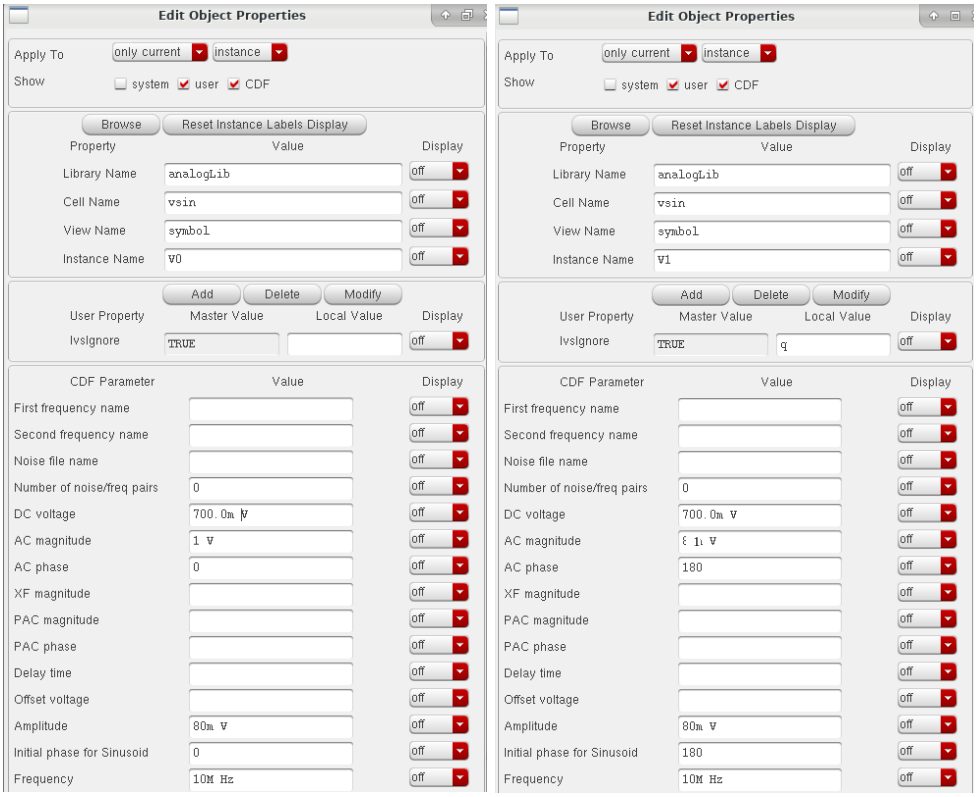
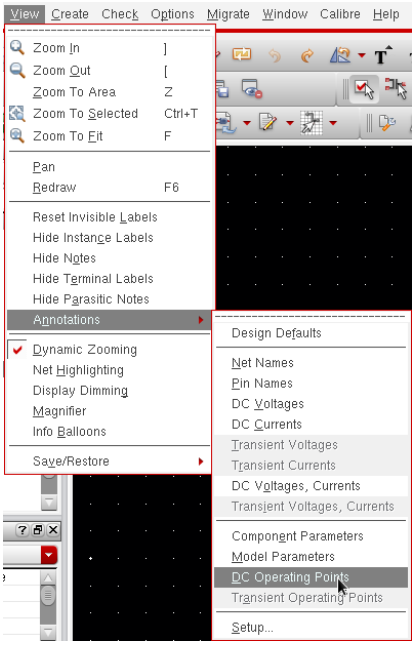


Fig. Voltage source configuration for diff mode input. For common mode input, make the phases of two sources the same. Note: AC magnitude and AC phase are for ac sim only; Amplitude, Initial phase for sinusoid and frequency are for trans sim only.

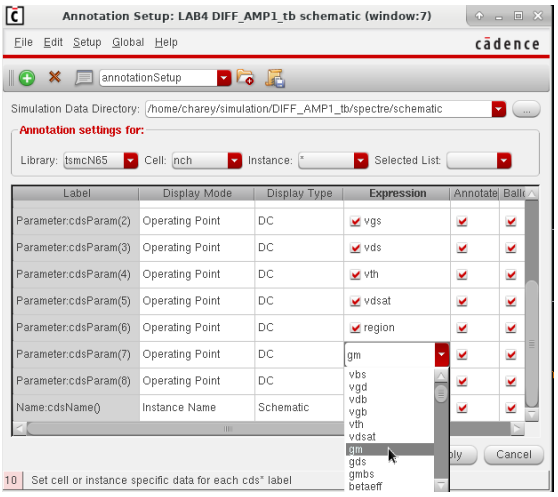
You can modify the phase to simulate differential mode or common mode. If V_1 and V_2 have the same phase, for example, both are 0, then you are simulating common mode. If one of them is 0 and the other is 180, then you are simulating the differential mode.

First, let us do the DC simulation. Go to **launch->ADE L->create a dc analyses.** Remember to check the box after save DC operating point, then click OK and run simulation.

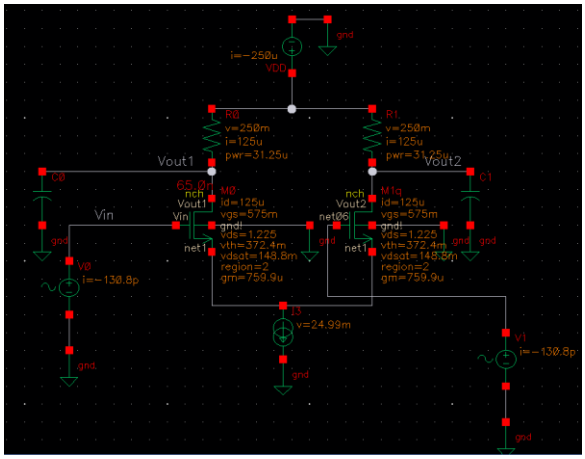
It's annoying that we need to go to the dc operating point report for the result, there is a very useful tool, you can show the DC operating points on the schematic rather than go to the report and find them over and over again. To do that, go to **Schematic->View->Annotations->DC Operating Points**, as below.



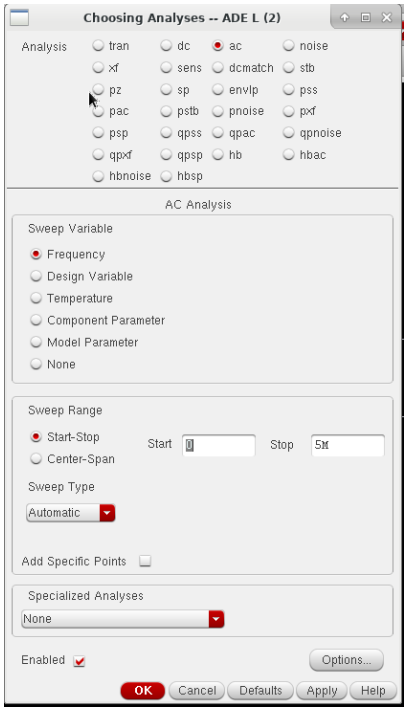
After turning that on, you will be able to see some dc operating points for example id, vgs and vth. However, we need two other dc points: gm and region. Gm is important to check the performance of transistor, if it's much smaller than we expected, then we need to go back and do the design again. Region is import to check all the transistors are in saturation region, remember that is region is equal to 2. To add those two, go to **View->Annotations->Setup**, you see the following window



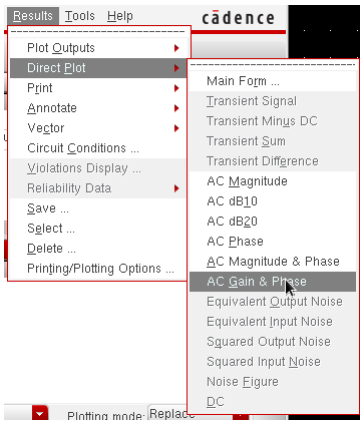
Note you need to choose gpdk045 and nmos1v as library and cell. Then you see a few DC operating points, you can edit them by double click in the expression. Double click on the blank ones and select region and gm, click OK. You can see these points in the schematic now!



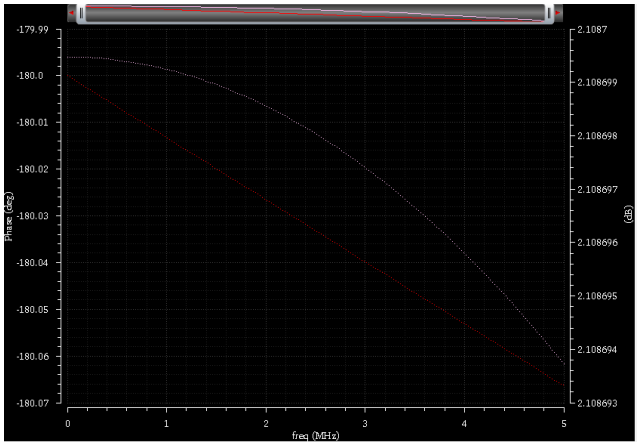
At the first glance, we notice the *gm* is much smaller than we designed. Facing this problem, it is better to do the ac simulation to check the differential gain. Set the ac phase of V0 as 0 and that of V1 as 180 so that we can simulate the differential mode. Then go back to ADE L window and add an ac simulation. Here we simulate the ac response between 0 and 5MHz. Click Ok and run the simulation.



After the simulation finishes, go to **Results->Direct Plot-> AC Gain & Phase in ADE L**



And the schematic view will pop up, you will need to choose two wires, the first wire corresponds to the output, and the second is the input, you can choose one side of the circuit because single-end gain is the same as differential gain. In our case, you can also just use dB20 since we have set the single ended input voltage to 1V in the voltage sources. After you click the two wires, press escape and then you will see this plot:



The pink curve is the gain, we note that in cadence, the gain is calculated using:

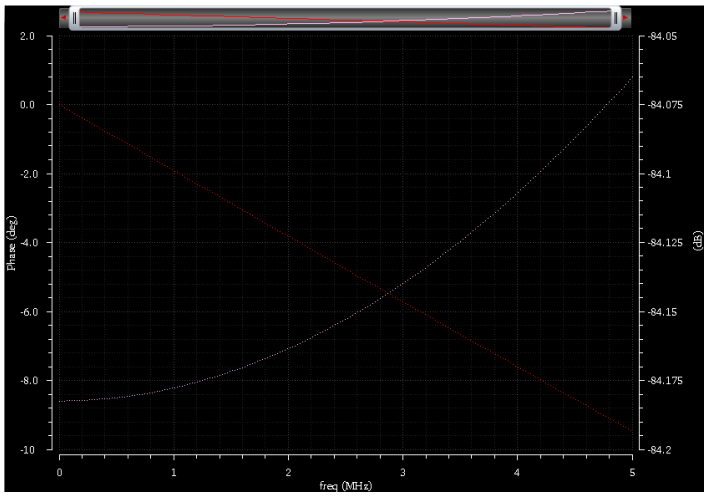
$$gain(dB) = 20\log(\frac{V_{out}}{V_{in}})$$

But we expected the gain to be 10dB, which is around 3.2, so the gain you are seeing is probably than what we want. How to fix it?

Analog circuits are complicated, there are many parameters that affect the performance. Experiment with changing the parameters of your circuit to achieve a higher gain of 10dB. This could be the transistor width, the value of Rd, Iss or anything else. I recommend thinking about how changing a single parameter will affect the gain – for example, increasing Rd should increase the gain, right? This is true, but if Rd is too high, the transistors will no longer be in saturation, so gain will decrease.

Now, we also want to check the common mode gain. To do this, you need to put both voltage sources in phase, in other words, the AC phase of both vsin's needs to be the same, e.g., 0. Then the common mode gain A_c can be obtained similarly as before. You can choose one side

of the circuit because the single ended common mode gain is the same as common mode gain. You will see this plot.



The gain of -85dB (yours may be different) means the common mode gain is very small, which is what we want.

This design is done, next we will change the ideal current source into a NMOS which is a more practical design.

Use NMOS as the current tail

Design the NMOS current source

At the saturation region, an NMOS can be considered as a current source. In this section, we replace the tail current source I_{ss} with a single NMOS with $V_b = 0.7V$.

This time, you will need to do some calculation. Please find W/L of the newly added NMOS so that the current is 100 uA. Hint: $I_d = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2$

In the cadence, use L=100nm and find the correct W. Note since this is a short channel device, your calculation might not be accurate. Tune the W so that the current is 100uA.

Making the Actual Circuit

Go to library manager and create a new schematic cellview in LAB4 with name "**DIFF_AMP2_tb**" as below. You can copy the previous schematic view, which will be faster, but make sure to make the appropriate modifications (swap the current source out for the NMOS you designed).

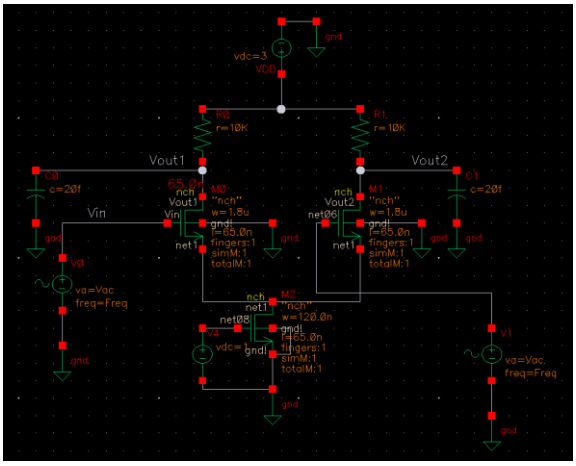


Fig schematic with a transistor as the current source. Note the parameters in the plot are not correct, don't directly use them.

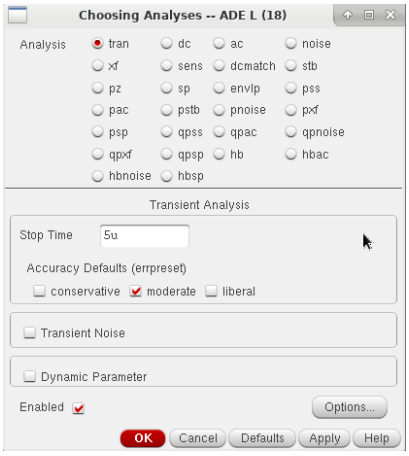
Trans and DC simulation

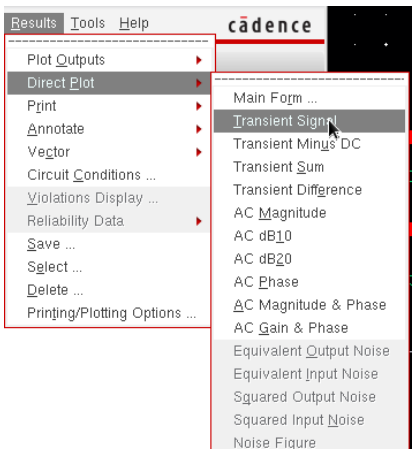
The first thing we need to do is a DC simulation so we can determine how the circuit is biased. Run a DC simulation (if you want, you can load the same ADE state from your previous circuit, just change the cell to match the name of the first differential amplifier circuit you made). Follow the same steps from part 1 to make the schematic window display DC operating points – transistor gm, region, etc. You may notice that your transistors are no longer biased properly or in the right operating region – if this is the case, do the following steps to understand what affect this has on circuit performance. Afterwards, we will modify the parameters to achieve better operation.

We can see the signal more clearly in trans simulation. To do that, you need to type in Amplitude, Initial Phase for Sinusoid and frequency in vsin, as shown in the previous picture of the voltage sources. Remember we want to simulate the differential mode, so the phase for the other vsin needs to be 180. Make sure you do this, otherwise you will not see any gain in signal.

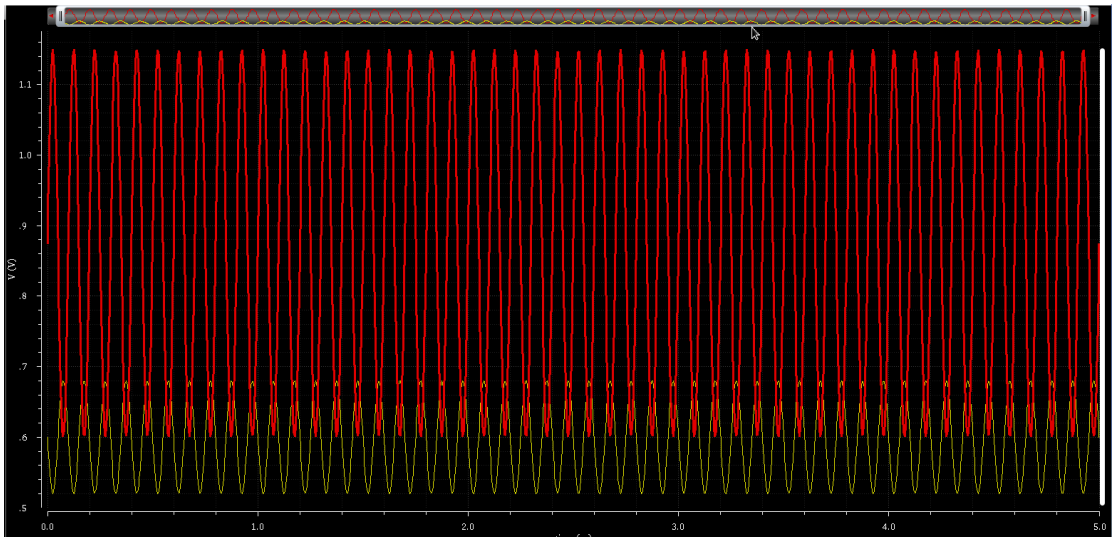
After you finish the schematic and set the vsin's correctly, go back to your ADE L and add a trans simulation as below.

Then run the simulation, after the simulation, go **to Results->Direct Plot-> Transient signal**, then the schematic will pop up. You will need to choose the voltage you want to plot, here we choose the inputs and outputs as below:





Then press esc, you will be able to see the following plot. Yours will have different values, but should look similar in that it will have one signal will a small oscillation (input) and one with a large oscillation (output).



By reading the plot, what is the differential gain of the device? Hint: you should care about the oscillating signal (ac).

Use the same method in previous section, do ac simulation and obtain the gain. Compare it with the trans simulation result. What is the influence of using an NMOS as current source rather than an ideal current source? If the gain is less than 10dB, try to adjust the design to obtain a 10dB gain. You may notice some difficulties you didn't have before (again, what is the influence of the NMOS current source?). You can try adjusting the bias voltage of the signal inputs if that helps. In real life, adjusting parameters will often involve tradeoffs. For now, we just want you to get a sense of how the circuit performance is highly dependent on how it is tuned.

What if the output voltage is beyond the output voltage swing? Set the amplitude as 200 mV and compare the output voltage transient signal with that when amplitude is 80mV. You can see the distortion of the output signal.

Design exploration: drain resistance mismatch

Add a mismatch of 5% over RDs in your final design in the previous section, find differential gain A_v and common mode gain $A_{v,cm}$ now.

How about CMRR? (Hint: use the trans simulation to see that differential gain of common mode input).

Deliverables

Diff amp with Ideal current source

- Extract λ_n and V_{th} of nmos1v in gpdk045, show your process and result in report.
- Determine the input swing by making sure the NMOS is saturated verify your conclusions by checking the region of NMOS under different input bias. Compare it with your calculation and explain.
- Adjust your design a bit and show a plot of gain larger than 10dB.
- Show the plot of common mode gain, convert the dB into percentage (or the ratio between output and input voltage)

Using NMOS as the current source

- Do the calculations to find W/L for the NMOS current source.
- Find $V_{in,cm}$ range and use DC simulation to verify it. You can show boundary situation where M2 is in triode region or M1/M0 is in triode region. Note region=1 if it is in triode region.
- Obtain the transient plot and analyze it, what is the differential gain after using NMOS as current source? Then adjust your design to maintain a gain of 10dB, show the transient plot and ac gain plot.
- Show the distorted output voltage signal in trans simulation.

Resistance mismatch

- Show your schematic, show the ac simulation result plot for A_d and A_c, analyze the result by comparing the two.
- Show the trans simulation plot and analyze, what is the value of CMRR in this case?