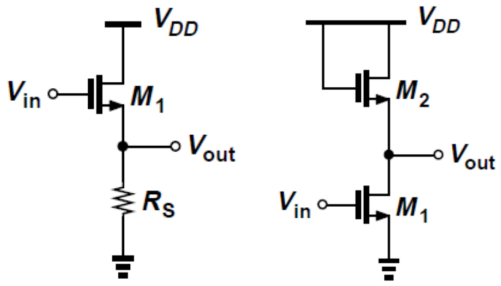
EE 332 Circuits and Devices II Autumn 2022

Homework 4 Due: Nov. 4th (11:59pm)

1. For the amplifier circuits below, fine gain, input impedance, output impedance, and the voltage swing (peak-to-peak). Assume that all transistors are biased such that: $VDD = 3V, V_{th} = 0.5V, V_{OD} = 0.2V, \gamma = 0,\ \lambda = 0.1V^{-1},\ I_D = 1mA,\ R_S = 1k\Omega$.



2. Consider a common-source amplifier with R_s=100Ω source degeneration (like Fig 3.23a from the book) and R_D=10kΩ. For NMOS, assume: VDD=1V, V_{Th}=0.3V, $\mu_n C_{ox} = 100uA/V^2, \lambda = \gamma = 0$.

a) Find W/L and V_{in} bias point to achieve Gain>10 and V_{out} DC bias of VDD/2.
b) How would the gain change if $\lambda = 0.1V^{-1}$?
c) How much is the output voltage swing?
d) If we are informed that gate-oxide thickness (t_{ox}) ended up 10% thicker than nominal target value after fabrication, how much this impacts the gain? (*Hint:* what aspect of NMOS device will be influenced by t_{ox}?*)*
e) Compare your result from part (d) with a simple common-source topology case (w/o source degeneration). Which topology is more robust to process variations?

3. In this problem, we are interested to build an audio amplifier with a gain of 10. Assume the "speaker" that we will drive with our amplifier can be modeled as a load resistor (R_L) of 100Ω. For MOSFETs: VDD=1V, $V_{th} = 0.3V, \lambda = 0, \mu_n C_{ox} = \frac{100\mu A}{V^2}$

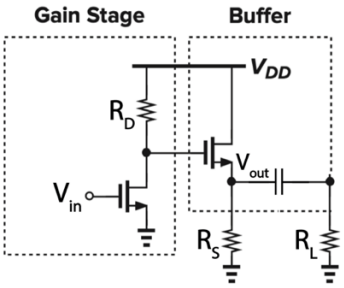
a) First, let's design a common-source amplifier with $R_D = 1k\Omega$ and a gain of 10 such that output bias will be at VDD/2. Find W/L and V_{GS} bias point.
b) Now, include the loading impact of R_L. How much is the gain once you connect the output node to R_L?
c) If you have to adjust your design to achieve the target gain, how do you redesign your amplifier? (Assume the bias point will not be affected by R_L since it can be AC-coupled)
d) What's the static power consumption from the supply in this amplifier? (*Hint:* Supply Power = V_{DD} * I_D)

Now, instead of fully redesigning your common-source amplifier from part (a), let's add a source-follower buffer with a gain of 0.5 to drive the load. Assume $R_S = 1k\Omega$, and R_L is AC-coupled.

e) First, find the W/L and bias point of the source-follower NMOS (M2) such that V_{out} of that stage will be at VDD/2 bias.

f) Now modify your CS amplifier such that overall gain will be still 10 and V_{out} is now biased at VDD/2+V_{GS2} Find new W/L and V_{GS} bias point.

g) What's the static power consumption from the supply by both of these stages? Compare the results with part (d).



4. *Common-Gate Amp.* Assume VDD=1V, $V_{th} = 0.3V, \lambda_n = 0.1V^{-1}, \gamma = 0, \mu_n C_{ox} = \frac{100\mu A}{V^2}, I_1 = 0.2mA$, and C_1 will be shorted in small-signal models and open for DC/bias analysis)

a) Find R_D, and V_{GS}-V_{th} and W/L of the M1 to achieve a gain of 50 and input impedance of 50Ω (you can assume $\lambda = 0$ for this part).
b) If we realize I_1 current-source with a single NMOS device at a fixed gate bias of 0.5V, draw the new circuit and find W/L of the new NMOS.
c) What's the output swing for part (b)?
d) How much adding this new NMOS changes the gain?
e) ***Bonus:*** if this amplifier is designed for recording neural activities at 300Hz-20kHz frequencies, what should be acceptable C_1 values as a AC-decoupling cap?