Lab 5 5 – Transistor OTA Design in Cadence

1 Introduction

Current mirrors based on the MOSFETs are useful to process signals. One of the important examples is the current mirror topology combined with differential pairs. In the class, we learnt about five-transistor "operational transconductance amplifier" (5-OTA), which finds application in many analog and digital circuits. In order to further study the performance of such topology, as well as to strengthen the skill of using Cadence to optimize electrical circuit, we will design a high performance 5-OTA circuit using ADE XL in Cadence Virtuoso in this Lab 5.

A 5-OTA, as suggested by its name, consists of five transistors, as shown in Fig.1. The current mirror here forces the current flowing through M1 to Such topology takes differential inputs and has a single output. We will also explore the frequency response of 5-OTA.

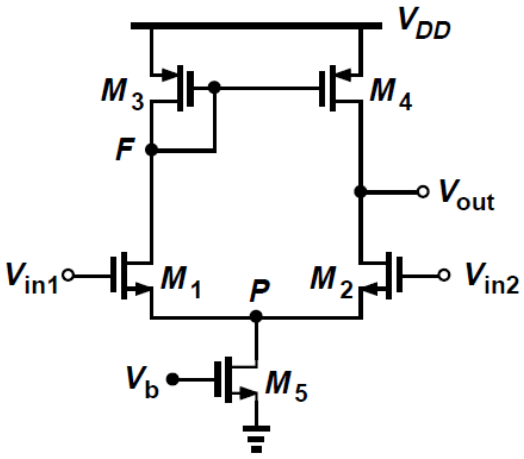


Fig. 1. Topology 5 - OTA

In previous labs we introduced ADE XL. In this lab, we will further take advantage of ADE XL and its powerful optimization engine to help us design a high performance circuit.

This lab is going to be different from previous ones in that you will not be provided with detailed instructions, since you already have a lot of experience using Cadence. Only the design requirements, a reference schematic, and an example of using ADE XL for optimization will be given.

2 Objective

1. Understand the working principles of 5-OTA and know how to design it, e.g., how to determine **DC Output Voltage**, how to select **Common-mode input voltage**, what is the **output swing**, what is the **gain**, what is the **CMRR** and so forth. Design a high performance 5-OTA based on 45 nm technology with Vdd = 1.2.

2. Learn the skill of using ADE XL to optimize the circuit. At least, you need some back of the envelope calculation to have a design to optimize. Software optimization could make things easier only when you have full control over it.
3. Use ADE XL to simulate and analyze the ac response (in other words, frequency response) of differential and common mode operation. Simulate and analyze the trans response, learn about the output swing and output DC bias.

3 Design requirements

We will use a current mirror to set the current in M5. Use gpdk045 for all nmos and pmos devices.

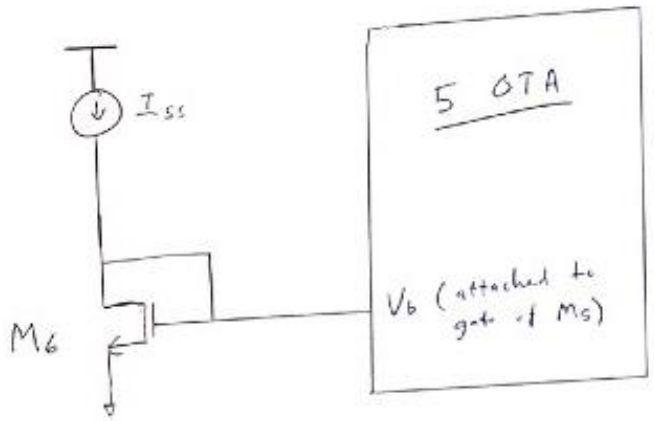


Table 1 VDD and length of the transistors

Parameter	Value
VDD	1.2 V
Iss	10 μA
$L_{1\text{-}4}$	45 nm
$L_{5,6}$	90 nm

Table 2 Design requirements

Performance	Requirement
Diff gain, Av	15 dB
Peal to peak output swing	1 V
3-dB gain bandwidth	500 MHz
Gain-bandwidth product	2.5 GHz

Note: remember M1,2 are identical, M3,4 are identical and M5,6 have identical length. Small discrepancy with respect to the requirements is allowed.

Hint: the output swing is limited by $|V_{GS4}|$, thus you need to choose the input common mode voltage judiciously to get a large output swing (very important!).

Similarly, to get a large gain, you need to consider $g_{m1,2}$ and $r_{o2,4}$. It's hard to take the frequency response into account when do the first principle calculation, you can rely on the optimization for this one!

Start this lab by doing some hand calculations to find the W/L of each transistor, as well as bias voltages for the inputs. For the hand calculations, try to achieve these relaxed requirements – we will rely on the optimizer to achieve the final design requirements listed above.

- The peak to peak output swing > 0.6V
- Find the common mode input voltage so that all the transistors are in saturation (you can verify this using dc simulation)
- The DC gain (without taking into account the frequency response) is larger than 12dB

During the calculation, feel free to use the technique we used in the previous lab – extracting the parameters through a DC simulation. Also, since we are dealing with short channel transistors here, your calculation is likely not to be the same as your later simulation. But that's fine, the purpose of this is just trying to make sure you have some intuition about the circuit.

4 Schematic of the 5-OTA

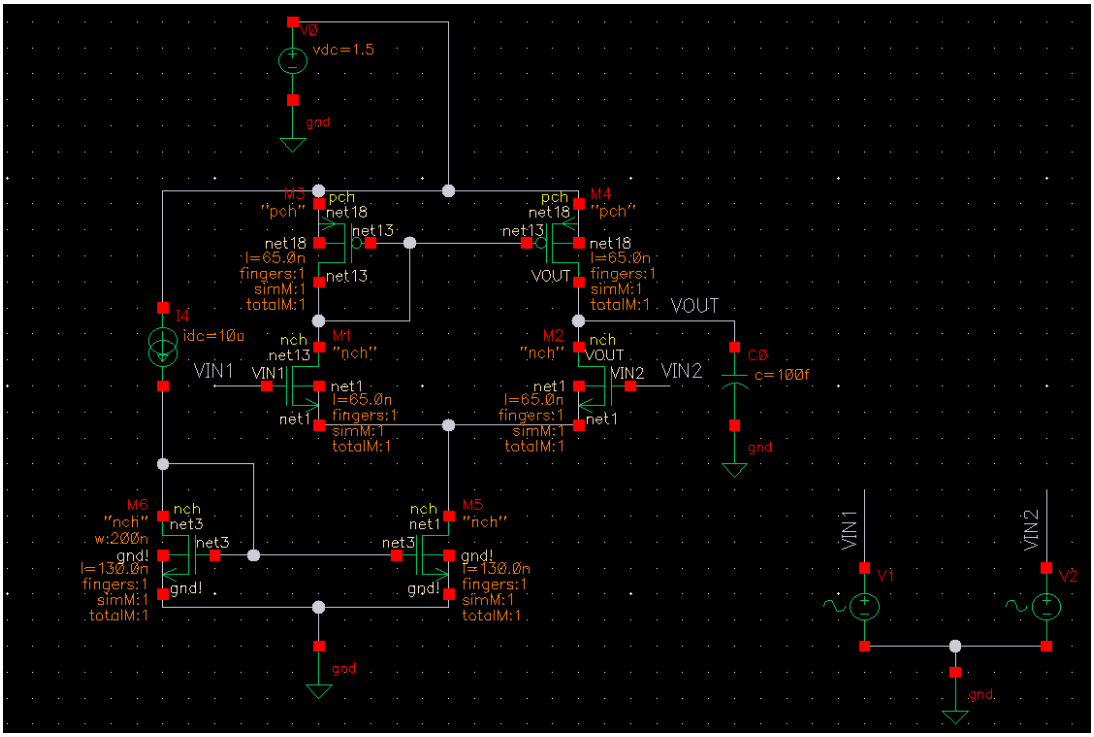


Fig. 2. Schematic of 5-OTA

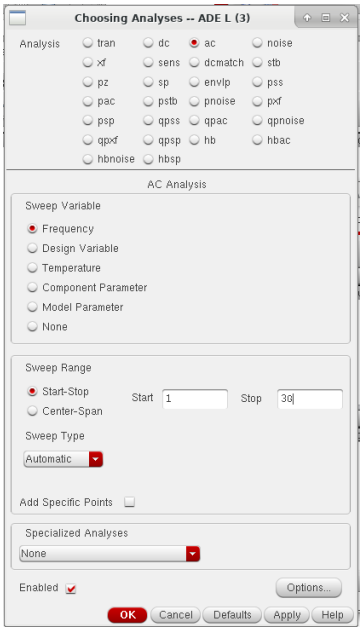
Note the length of M5 and M6 is 90 nm, all the other transistors are using the minimum length. When you set up the schematic, make the ac amplitude of each voltage source 0.5V, so that you have 1V differential input, later you can directly view ac magnitude of Vout as the gain (gain=Vout/Vin, now Vin=1, so Vout = gain). Use a 100fF capacitor at the output.

Note: set the width of M6 to be 120nm, which is the default value, and only tune the width of M5.

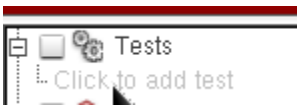
5 Optimization using ADE XL

You can also check the reference video for this part link at bottom of lab).

5.1 Open ADE XL and configure simulation

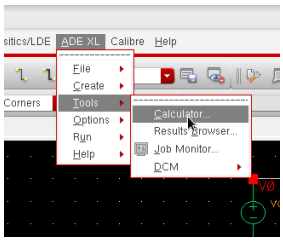


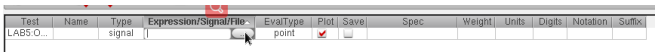
After finishing the schematic, go to Launch -> ADE XL -> Create New View, select lab 5 cell, click OK. Expand Tests -> Click to add test -> select lab 5 cell and enter the ADE XL test editor. Add “dc” and “ac” simulation for optimization purposes. In dc simulation, tick Save DC Operating point. In ac simulation, set the frequency from 1 to 5G. After finishing this, go back to ADE XL Editing window run the simulation.



5.2 Add outputs

We recommend watching the video at the bottom of this lab for visual assistance with this section (but please read this section first). Note though that we will be optimizing for a limited set out outputs (see below). Go to Outputs Setup tab, double click under Expression/Signal/File, and click on the …, this should bring you to the calculator. If it brings you to the schematic, click ADE XL -> Tools -> Calculator to enter calculator.





In this optimization, you will need to set constrains on the following parameters:

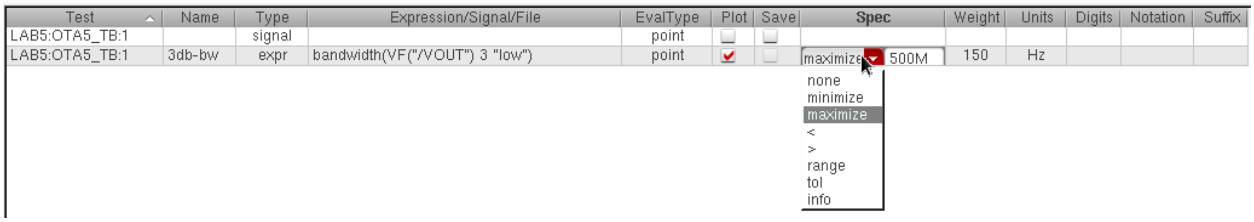
- Region: make sure all the transistors are in saturation
- Gain: make sure the gain is larger than 15 dB
- Gain bandwidth product: larger than 2.5 GHz
- 3-dB bandwidth: larger than 500MHz

In the calculator, the following functions are useful:

- dB20 (change the value into dB)

- value (if the result is more than one number, get the single number you want)
- gainBWProd
- 3dB-bandwidth (use bandwidth function for this part, set the bandwidth as 3)

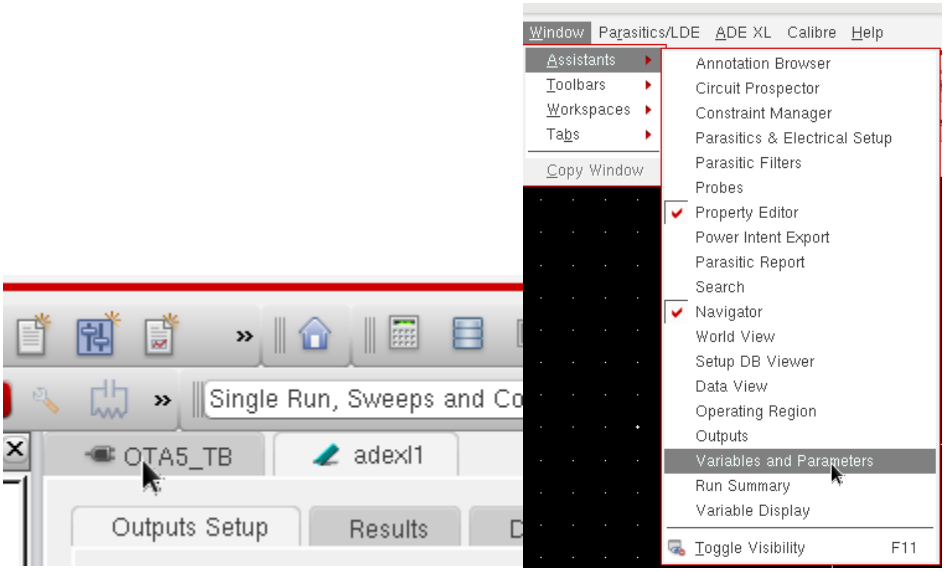
After adding all the parameters, you need to go back to ADE XL editing window to set the Spec. For regions, you need to use tol, which means in the tolerance. Set it as 2 and in the range 1%. For other parameters, you need to use maximize, and set the value according to the requirements in Section 3.



You also need to set the weights, you can manually tune the weight.

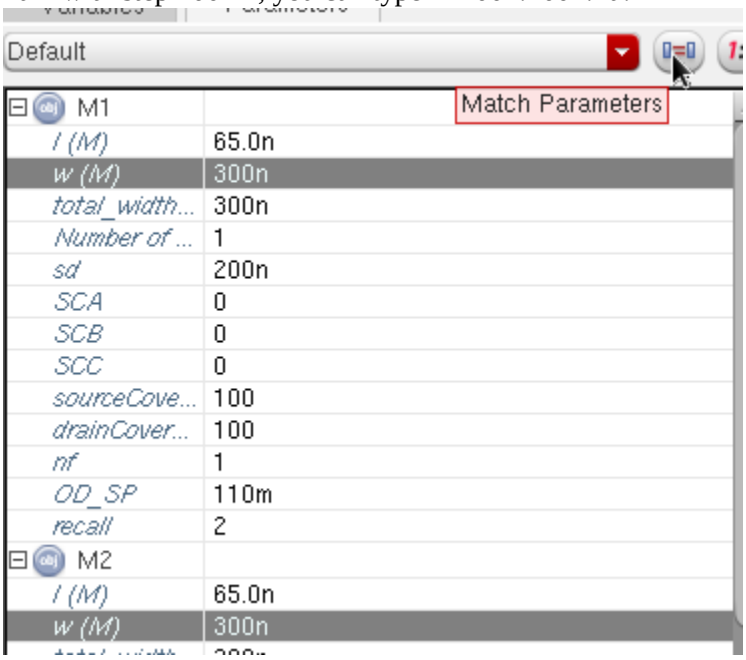
Note: this is not the full list of constraints, you need to finish others.

5.3 Add parameters

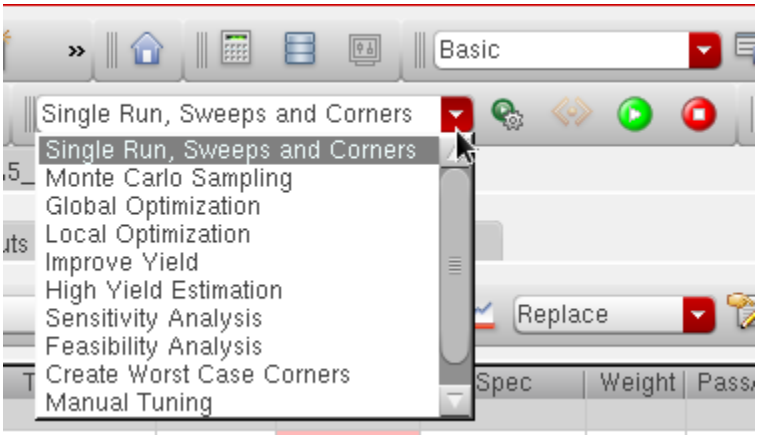


Before this, run the simulation again and check your initial design performance. If it needs further optimization, which usually is the case, go back to the schematic by click on the tab in the ADE XL Editing window. Go to **Window -> Assistants -> Variables and Parameters,** go to the Parameters tab. In this design, we have 3 parameters to optimize, i.e., $W_{1,2}$, $W_{3,4}$,W_5. As an example, we select both M1 and M2 by press shift and click on M1,2. You should see M1 and M2 being added to the Variable and Parameters window. Expand them and choose the width of both device, and press match parameters, since we want them to be the same. Then M1 w is added to the window below, you can set the value, which is the value, which is the range you want to optimize. For example, you want to optimize from 200nm to

1um with step 100nm, you can type in 200n:100n:1u.

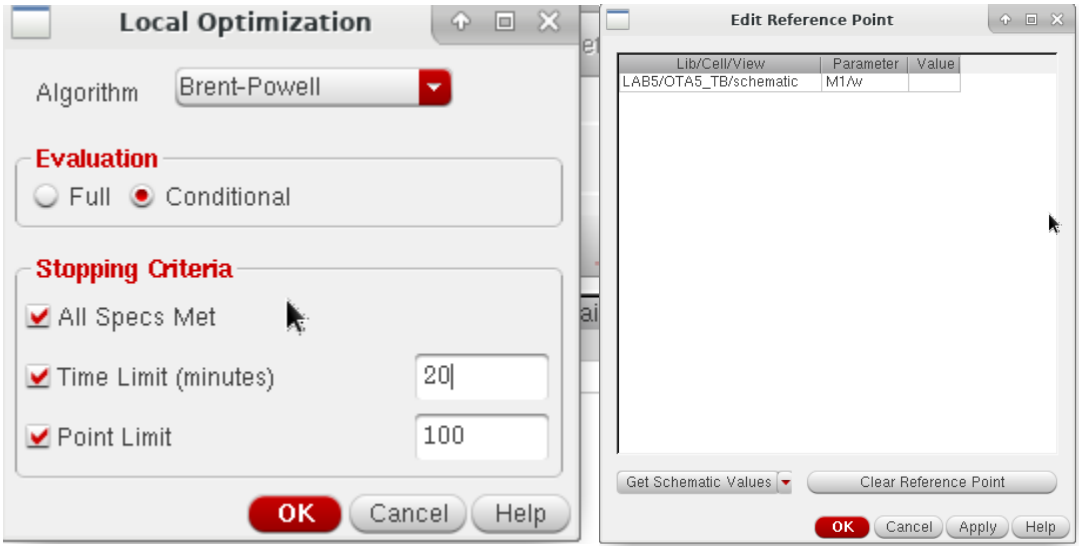


5.4 Setup the optimizer



After you finish setting up the parameters, you can go back to ADE XL Editing window. Choose Local Optimization. You can set up the optimizer by click on these two buttons 

to the right. You can set the algorithm, simulation time limit and # of design point limit clicking on the first button (not necessarily the same as below). You can edit the parameters you want to optimize by clicking on the second button. Click on get Schmetaic values->All parameters and Ok.



Question: is it possible to optimize the differential output swing? What are the constraints for that?

After this, you just need to click on the run button and maybe have a cup of coffee!

6 Deliverable

1. Your calculations of (W/L)'s and V_{od}'s to fulfill DC performances, i.e., $V_{in,cm}$, Vout swing, DC gain.
2. Your final, optimized schematic view with device parameters on it, i.e., W and L of the transistors.
3. Common mode (CM) and differential mode (DM) gain vs. frequency from 1Hz to 4GHz using ac simulation. Estimate zeros and poles based on DM gain plot.
4. Check the output swing (using a transient sim) and DC level using trans simulation. Show the figure of trans simulation and analyze it in the report.

Reference

https://www.youtube.com/watch?v=2kAUN_xBGuc