EE 332: Devices and Circuits II

Lecture 3: Single-stage Amplifiers (Part 1)

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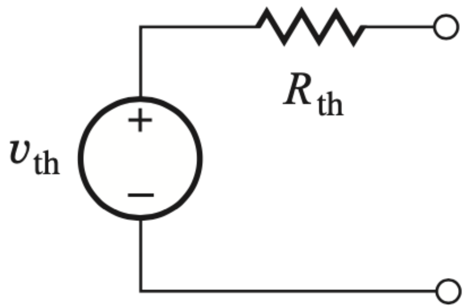
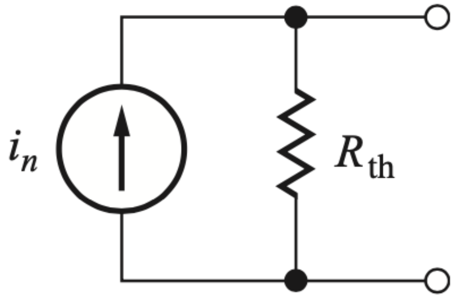
ELECTRICAL & COMPUTER ENGINEERING

Thevenin/Norton Models

- ***Thevenin*** equivalent theorem: any one-port linear network can be reduced to a single voltage source in series with a resistance (can have a complex impedance).
- ***Norton*** equivalent: similar to Thevenin theorem, but this time a current source in parallel to a single resistance.
- Notice:
  - V_{th} is the open-circuit voltage of the port
  - I_n is the short-circuit current of the port
  - R_{th} is the impedance "seen" through the port by nulling the independent sources
  - $V_{th} = I_n \times R_{th}$



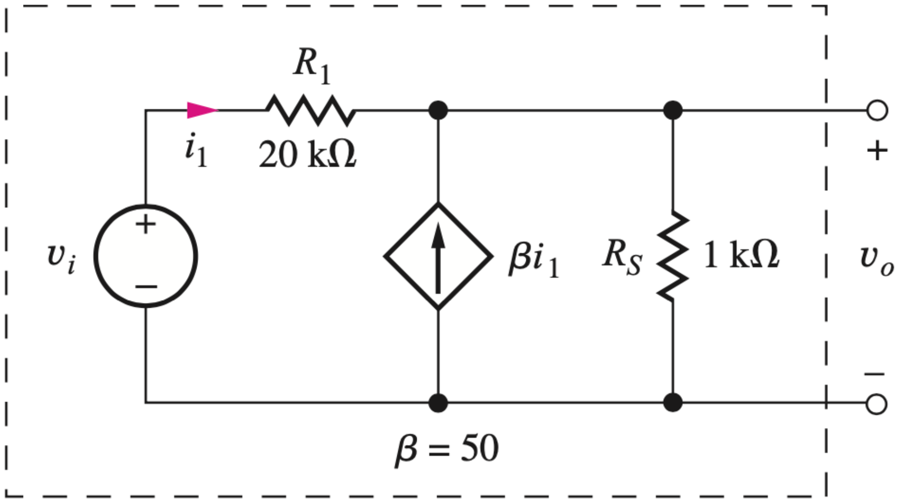
Thevenin



Norton

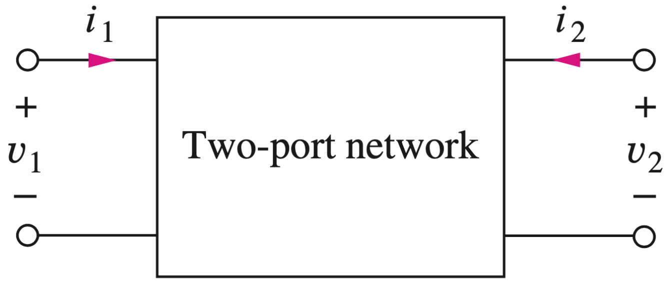
An example …

- Derive the Thevenin & Norton models (*Method: Calculate open-circuit Vo and Measure output impedance by nulling independent sources*)



Input/Output Impedance

- Two-port model from circuit theory



$$\mathbf{v_1} = z_{11}\mathbf{i_1} + z_{12}\mathbf{i_2}$$

$$\mathbf{v_2} = z_{21}\mathbf{i_1} + z_{22}\mathbf{i_2}$$

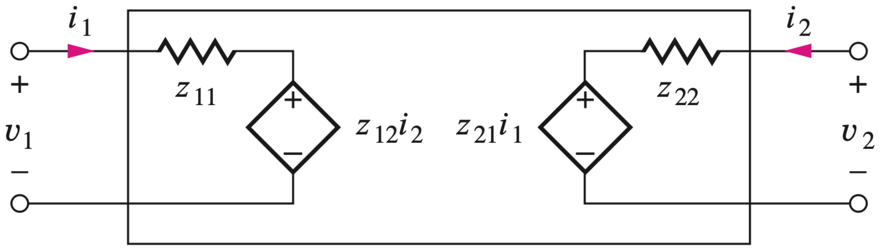


Figure C.4 Two-port z-parameter representation.

Ideal vs Non-ideal Amplifier

- Ideal amplifier (Fig. a)

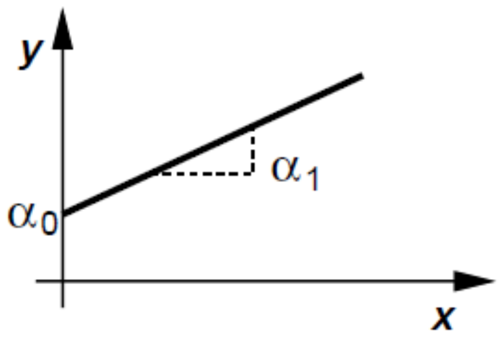
$$y(t) = \alpha_0 + \alpha_1 x(t)$$

  - Large-signal characteristic is a straight line
  - α_1 is the "gain", α_0 is the "dc bias"

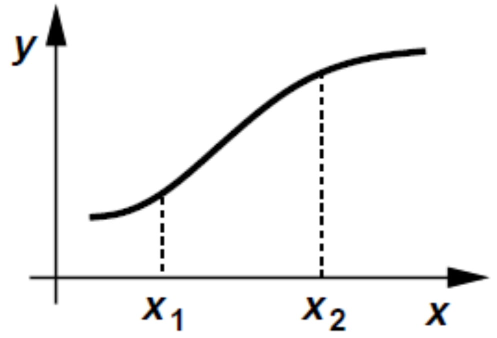
- Nonlinear amplifier (Fig. b)

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \cdots + \alpha_n x^n(t)$$

  - Large signal excursions around bias point
  - Varying "gain", approximated by polynomial
  - Causes distortion of signal of interest



(a)

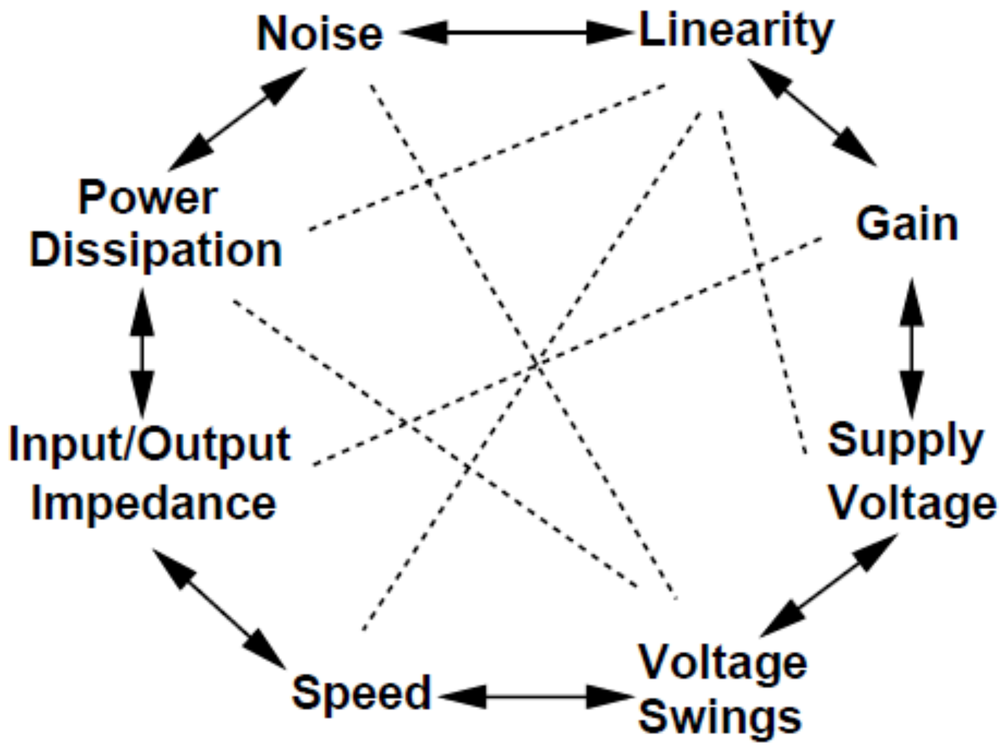


(b)

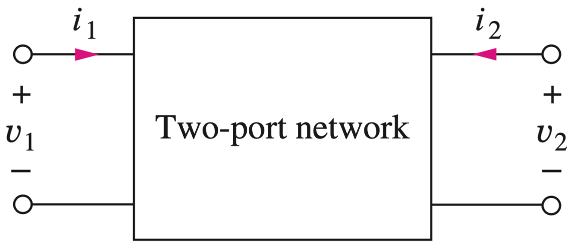
Analog Design Tradeoff

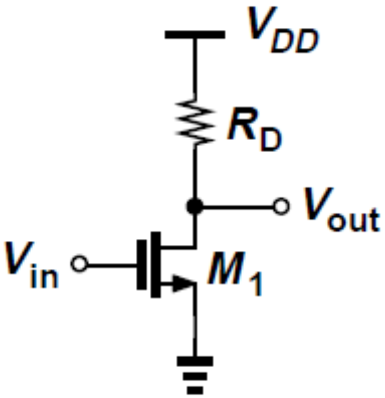
- Along with gain and speed, other parameters also important for amplifiers
- Input and output impedances decide interaction with preceding and subsequent stages
- Note that linearity will be analyzed using the large-signal models (not the small-signal!)

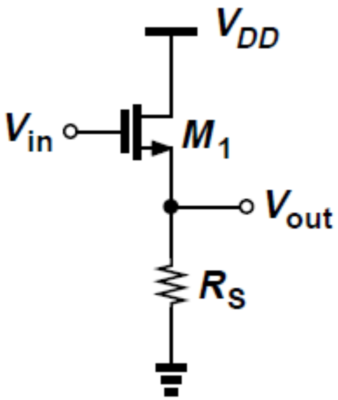
- Performance parameters trade with each other
  - Multi-dimensional optimization problem

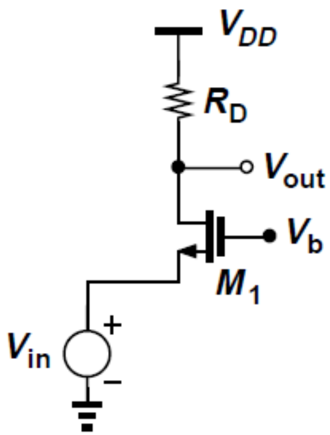


Common-"X" Single-stage Amps.

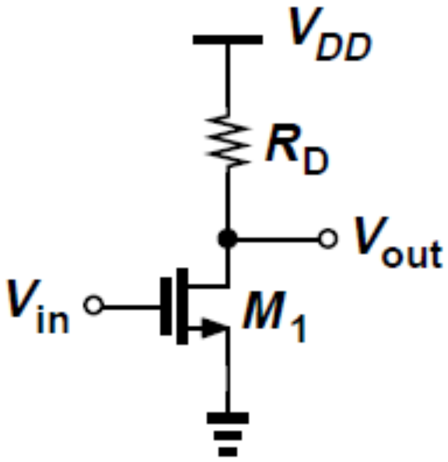






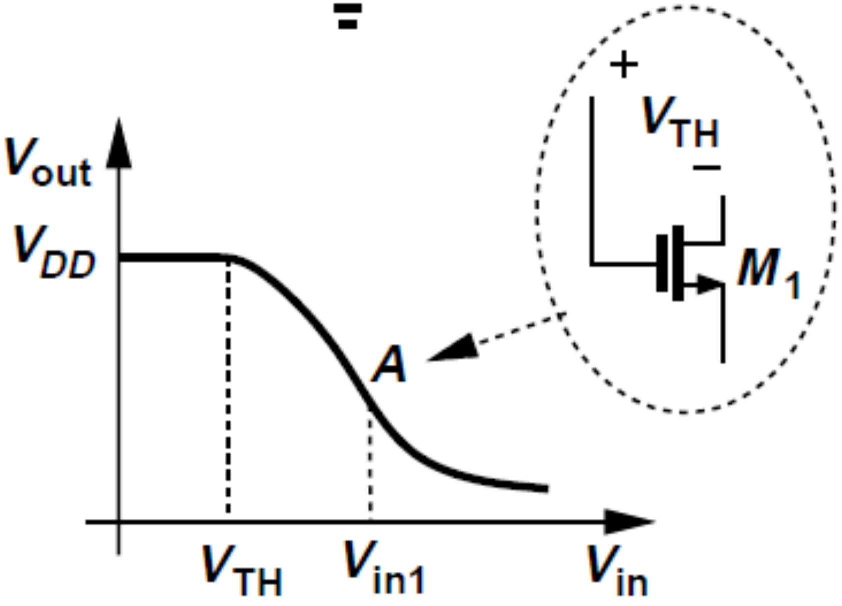


Common-Source stage with Resistive load



- For $V_{in} < V_{TH}$, M_1 is off and $V_{out} = V_{DD}$
- When $V_{in} > V_{TH}$, M_1 turns on in saturation region, V_{out} falls

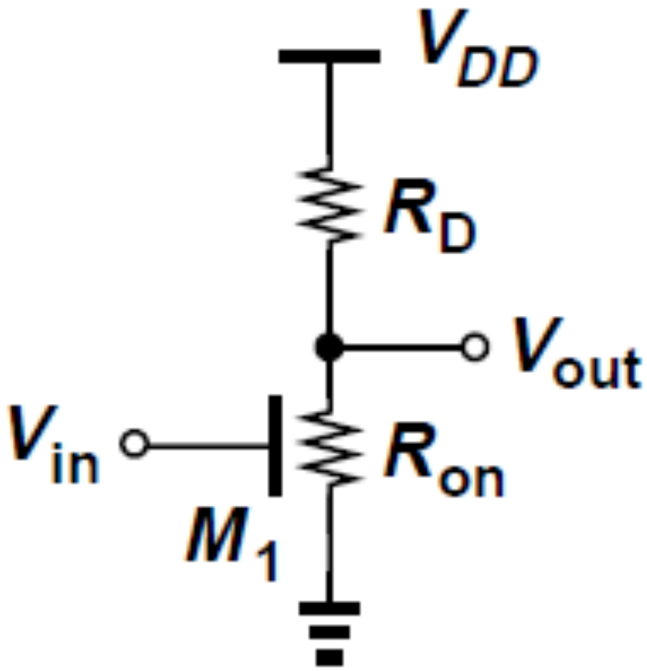
$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2$$



- When $V_{in} > V_{in1}$, M_1 enters triode region
- At point A, $V_{out} = V_{in1} - V_{TH}$

$$V_{in1} - V_{TH} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{TH})^2$$

Common-Source stage with Resistive load



- For $V_{in} > V_{in1},$

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left[2(V_{in} - V_{TH})V_{out} - V_{out}^2 \right]$$

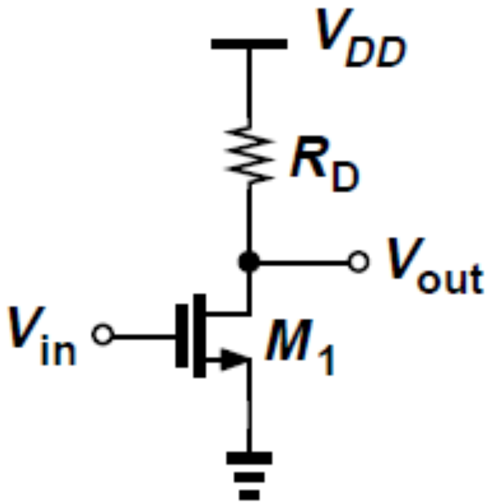
- If V_{in} is high enough to drive M_1 into deep triode region so that $V_{out} << 2(V_{in} - V_{TH}),$

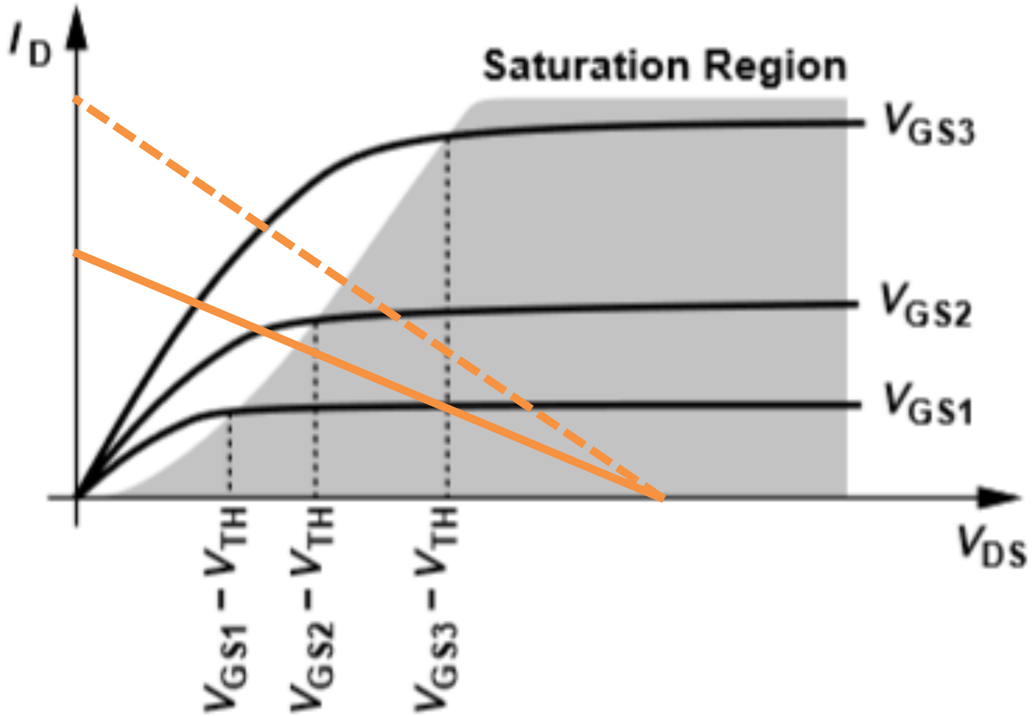
$$V_{out} = V_{DD} \frac{R_{on}}{R_{on} + R_D}$$

$$= \frac{V_{DD}}{1 + \mu_n C_{ox} \frac{W}{L} R_D (V_{in} - V_{TH})}$$

Load-line & Bias point

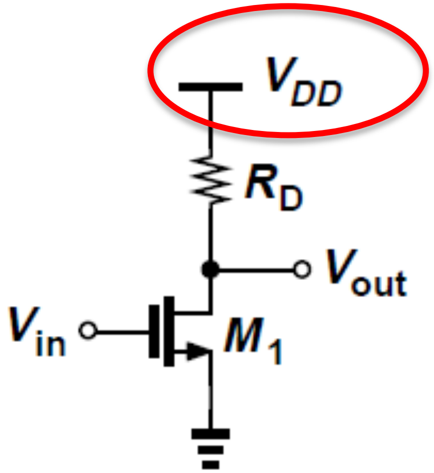
- Visualizing the "equations" by load-lines to find the operating (bias) point





Small-signal models for CS Stage

Notice the notations for small-signal in this book! (***V_{in}*** = small-signal source)



DC Supplies will be nulled for SS-models!

For NMOS

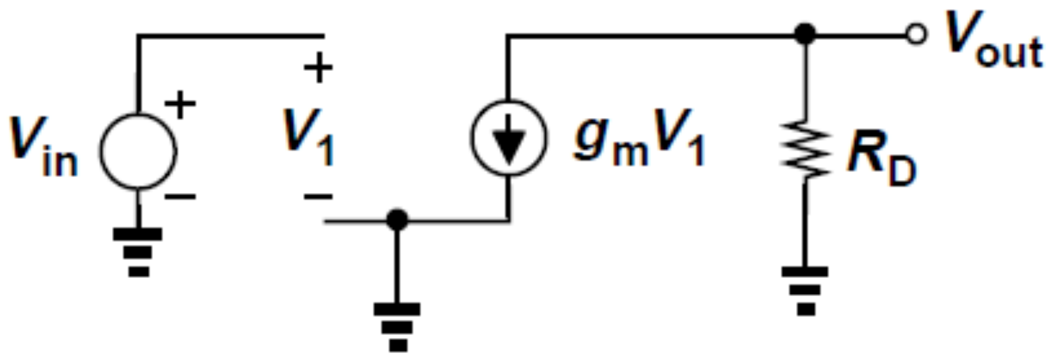
For PMOS

Common-Source stage with Resistive load

- Taking derivative of I_D equation in saturation region, small-signal gain is obtained

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2$$

$$\begin{aligned} A_v &= \frac{\partial V_{out}}{\partial V_{in}} \\ &= -R_D \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH}) \\ &= -g_m R_D \end{aligned}$$



- Same result is obtained from small-signal equivalent circuit

$$V_{out} = -g_m V_1 R_D = -g_m V_{in} R_D$$

- g_m *and* A_v vary for large input signal swings according to

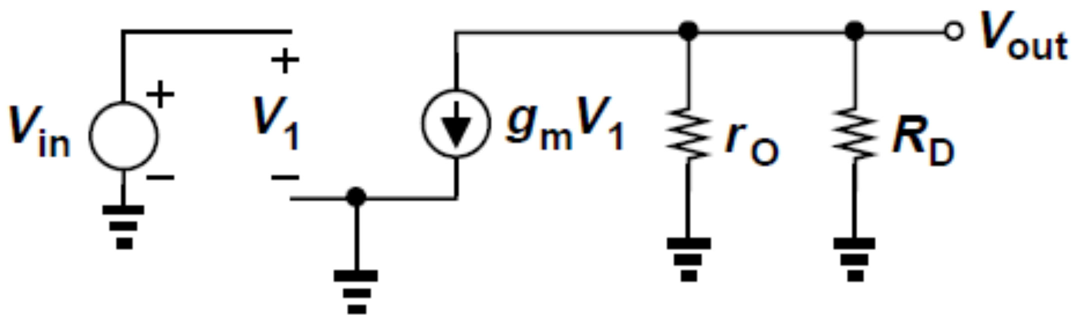
$$g_m = \mu_n C_{ox} (W/L)(V_{GS} - V_{TH})$$

- This causes non-linearity!!!

Examples 3.1 & 3.2 from Razavi

Common-Source stage with Resistive load

- Above result is also obtained from small-signal equivalent circuit



$$V_1 = V_{in}$$

$$g_m V_1 (r_O \| R_D) = -V_{out}$$

$$V_{out}/V_{in} = -g_m (r_O \| R_D)$$

- For large values of R_D, channel-length modulation of M_1 becomes significant, V_{out} equation becomes

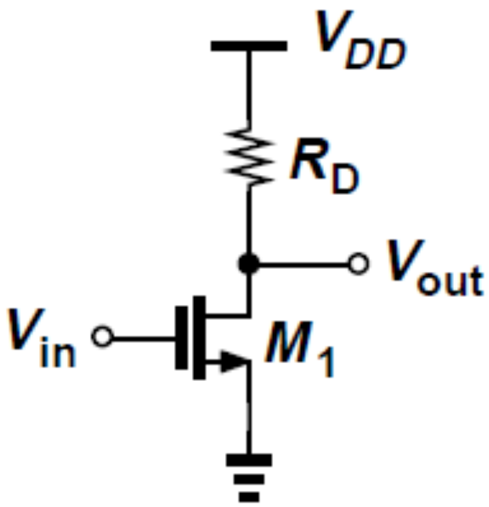
$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2 (1 + \lambda V_{out})$$

- Voltage gain is

$$A_v = -g_m \frac{r_O R_D}{r_O + R_D}$$

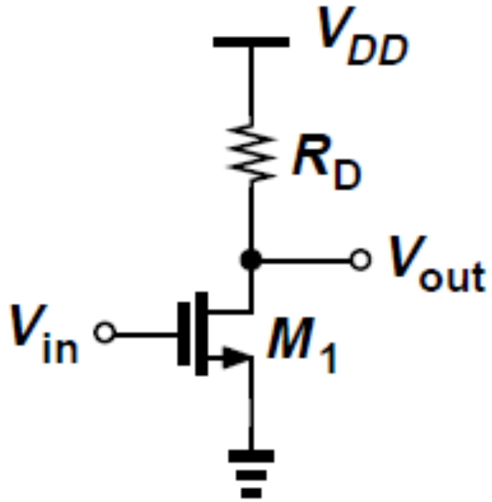
CS Stage Example

- What's the **voltage swing** of V_{out}? What's the optimal bias point for V_{out} to achieve max swing?



CS Stage Example

- Find V_{in} & R_D value such that: V_{out} = VDD/2 & Gain > 10



$$\mu_n C_{ox} = 50\ \mu\text{A/V}^2$$

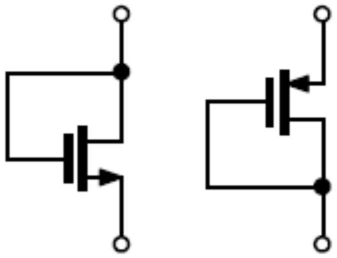
$$W/L = 10$$

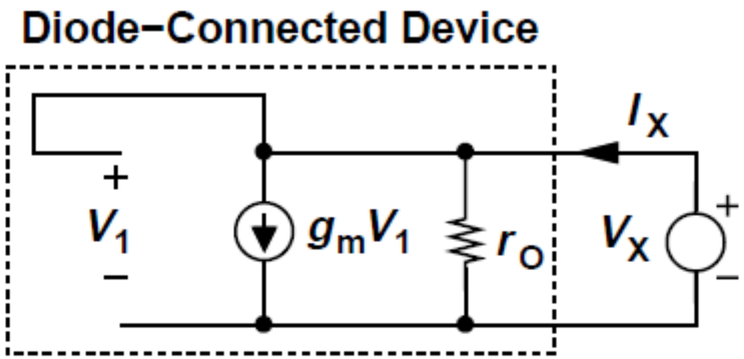
$$V_{TH} = 0.3\text{ V}$$

$$\lambda = 0.1V^{-1}$$

Diode-Connected MOSFET

- A MOSFET can operate as a small-signal resistor if its gate and drain are shorted, called a "<u>diode-connected</u>" device
- Transistor always operates in **<u>saturation</u>** (why?)



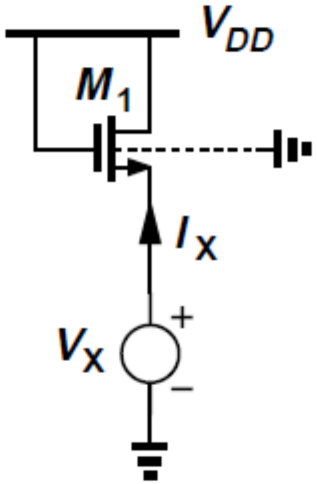


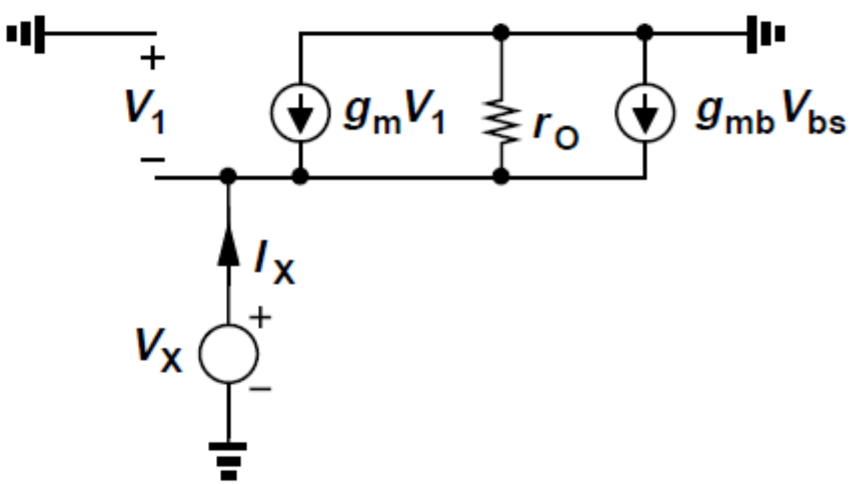
- Impedance of the device can be found from small-signal equivalent model

$$V_1 = V_X \qquad I_X = V_X/r_O + g_m V_X$$

$$V_X/I_X = (1/g_m)\|r_O \approx 1/g_m$$

Diode-Connected MOSFET





- Including body-effect, impedance "looking into" the source terminal of diode-connected device is found as

$$V_1 = -V_X \qquad V_{bs} = -V_X$$

$$(g_m + g_{mb})V_X + \frac{V_X}{r_O} = I_X$$

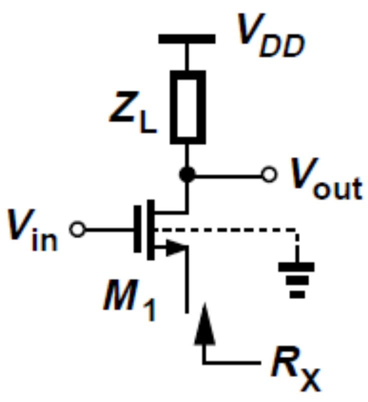
$$\frac{V_X}{I_X} = \frac{1}{g_m + g_{mb} + r_O^{-1}}$$

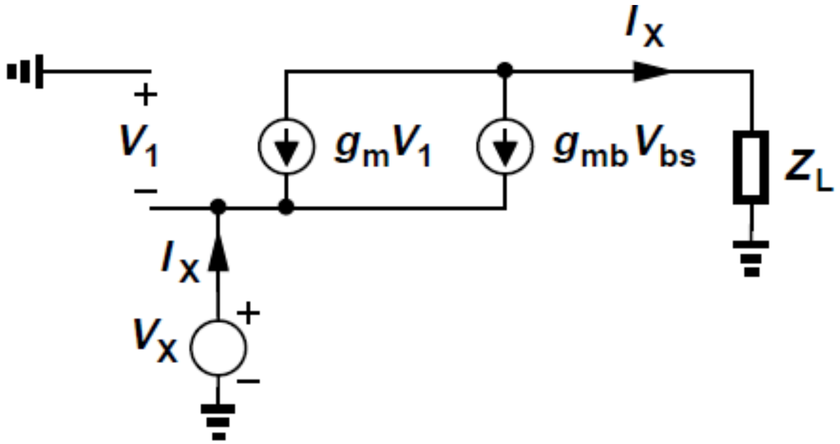
$$= \frac{1}{g_m + g_{mb}} \| r_O$$

$$\approx \frac{1}{g_m + g_{mb}}$$

Diode-Connected MOSFET: Example

- Find R_X if $\lambda = 0$





- Set independent sources to zero, apply V_X and find resulting I_X

$$V_1 = -V_X$$

$$V_{bs} = -V_X$$

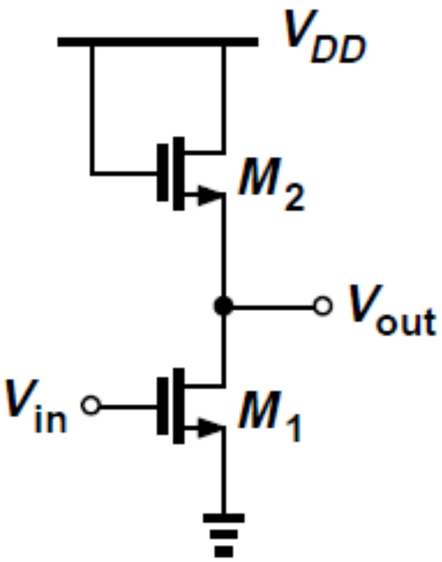
$$(g_m + g_{mb})V_X = I_X$$

$$\frac{V_X}{I_X} = \frac{1}{g_m + g_{mb}}$$

- Result is same compared to when drain of M_1 is at ac ground, but only when $\lambda = 0$

- Loosely said that looking into source of MOSFET, we see $1/g_m$ when $\lambda = \gamma = 0$

CS Stage with Diode-Connected Load



- Neglecting channel-length modulation, using impedance result for diode-connected device,

$$A_v = -g_{m1}\frac{1}{g_{m2}+g_{mb2}}$$

$$= -\frac{g_{m1}}{g_{m2}}\frac{1}{1+\eta}$$

where,

$$\eta = g_{mb2}/g_{m2}$$

- Expressing g_{m1} and g_{m2} in terms of device dimensions,

$$A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}\frac{1}{1+\eta}$$

- This shows that gain is a weak function of bias currents and voltages, i.e., relatively linear input-output characteristic

Process Variations in CMOS

- Real-world is non-deterministic …
- Additionally many parameters such as mobility (μ) is temperature sensitive
- We use term "**PVT**" dependent: Process-Voltage-Temperature sensitive
- There are all sort of process variations: wafer-to-wafer, chip-to-chip, etc.
- We normally model the variations using Gaussian models and simulate circuit performance using
  - Process corners such as: typical-typical, fast-fast, etc.
  - Monte-Carlo Simulations

"Golden" design rules to minimize the impacts of PVT variations:

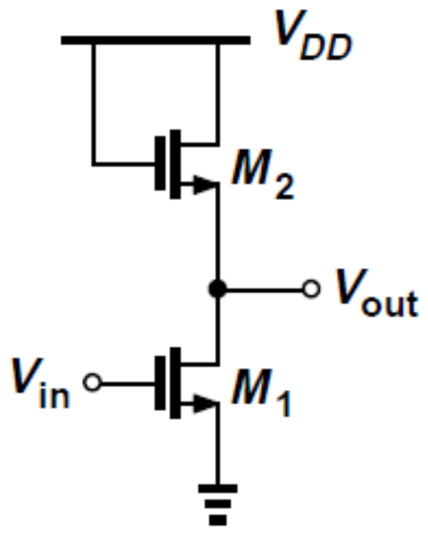
- *Rely on ratios as opposed to absolute values*
- *Make circuits symmetric*

CS Stage with Diode-Connected Load

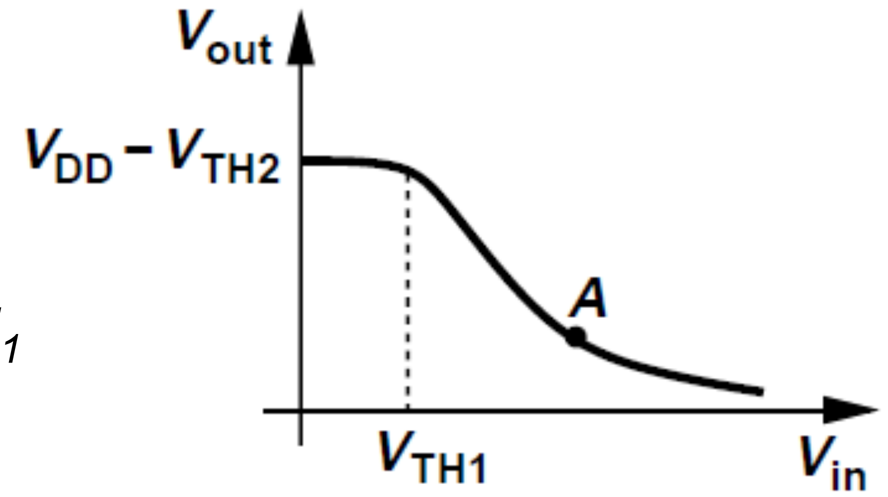
- From large-signal analysis,

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{in} - V_{TH1})^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{DD} - V_{out} - V_{TH2})^2$$

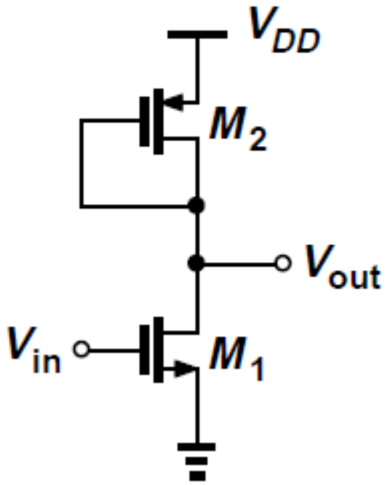
$$\sqrt{\left(\frac{W}{L}\right)_1}(V_{in} - V_{TH1}) = \sqrt{\left(\frac{W}{L}\right)_2}(V_{DD} - V_{out} - V_{TH2})$$



- For $V_{in} < V_{TH1}$, $V_{out} = V_{DD} - V_{TH2}$
- When $V_{in} > V_{TH1}$, previous large-signal analysis predicts that V_{out} approximately follows a single line
- As V_{in} exceeds $V_{out} + V_{TH1}$ (to the right of point A), M_1 enters the triode region and the characteristic becomes nonlinear.



CS Stage with Diode-Connected PMOS device



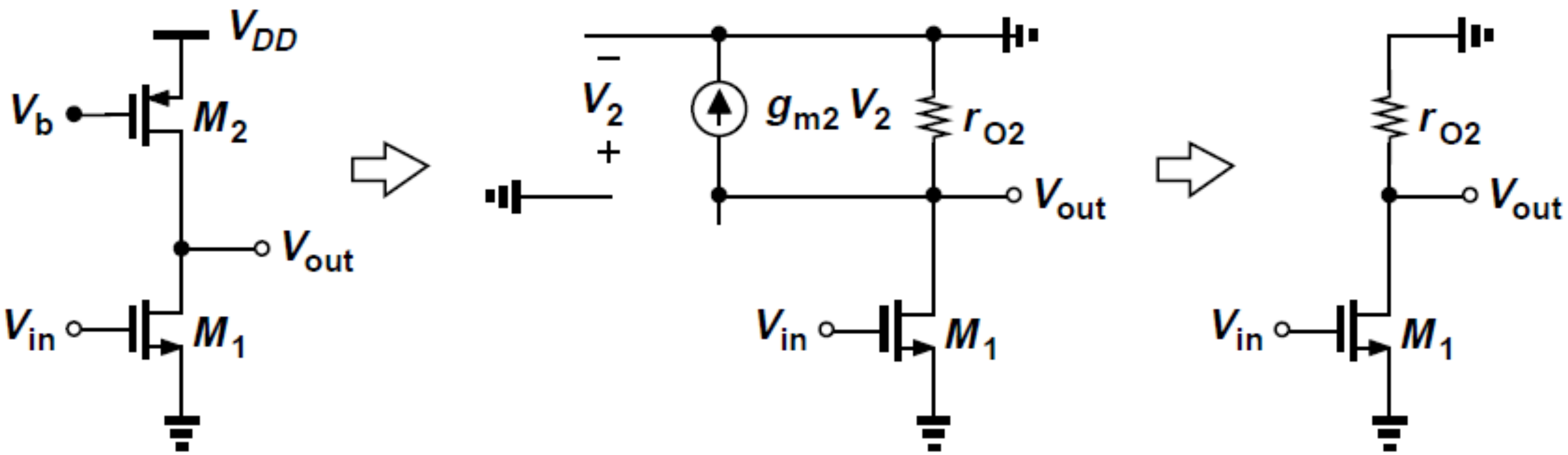
- Diode-connected load can be implemented as a PMOS device, free of body-effect
- Small-signal voltage gain neglecting channel-length modulation

$$A_v = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}}$$

- Gain is a relatively weak function of device dimensions
- Since $\mu_n \approx 2\mu_p$, high gain requires “strong” input device (large W/L_1) and “weak” load device (small large W/L_2)

- Voltage-swing?

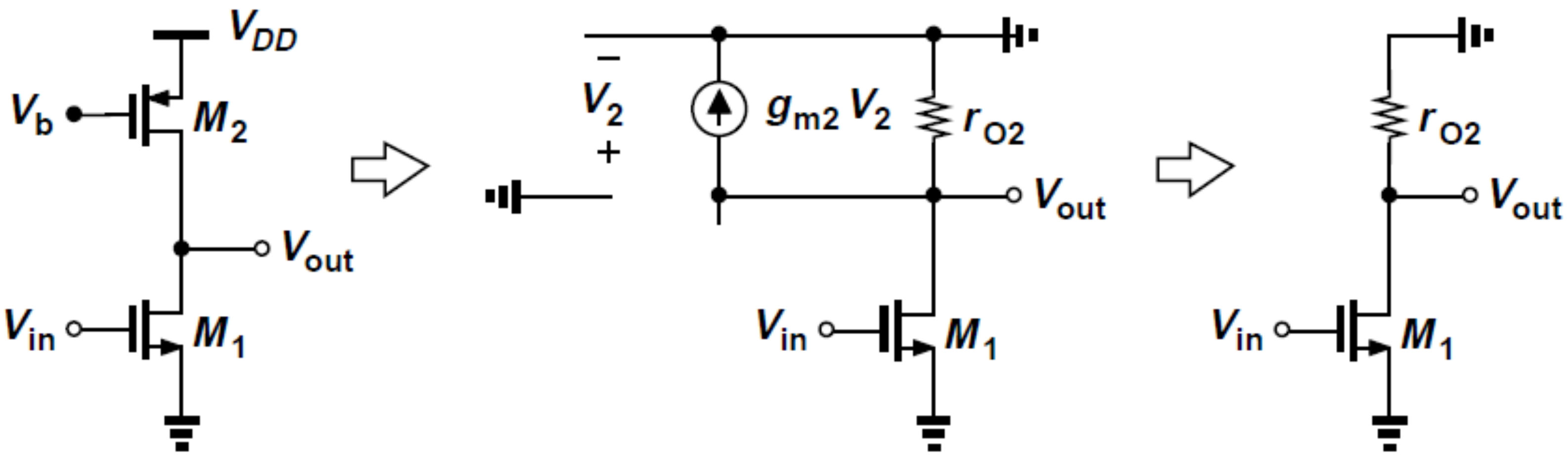
CS Stage with Current-Source Load



- Current-source load allows a high load resistance without limiting output swing
- Voltage gain ?

- Overdrive of M_2 can be reduced by increasing its width, r_{o2} can be increased by increasing its length

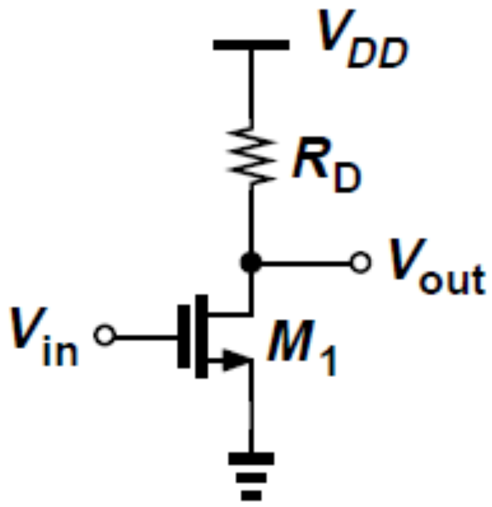
CS Stage with Current-Source Load

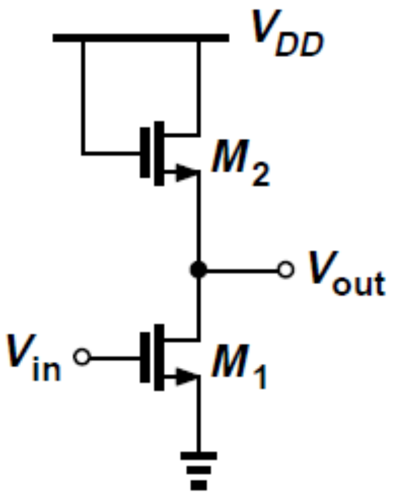


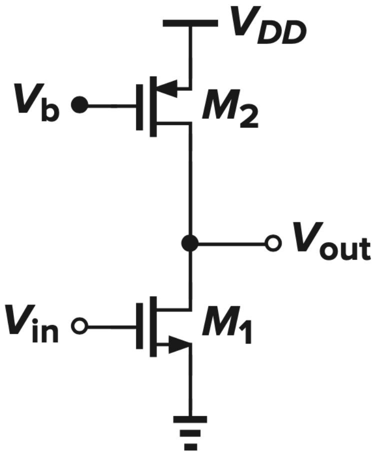
- Output bias voltage is not well-defined (why?)

- Intrinsic gain of M_1 decreases with I_D (Why?)

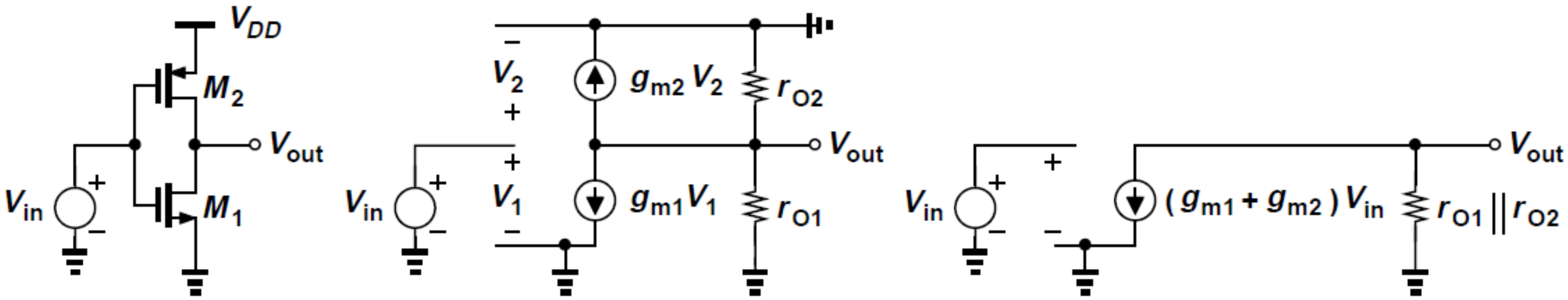
Summary of CS Amps.







CS Stage with Active Load



- Input signal is also applied to gate of load device, making it an “active” load
- M_1 and M_2 operate in parallel and enhance the voltage gain
- From small-signal equivalent circuit,

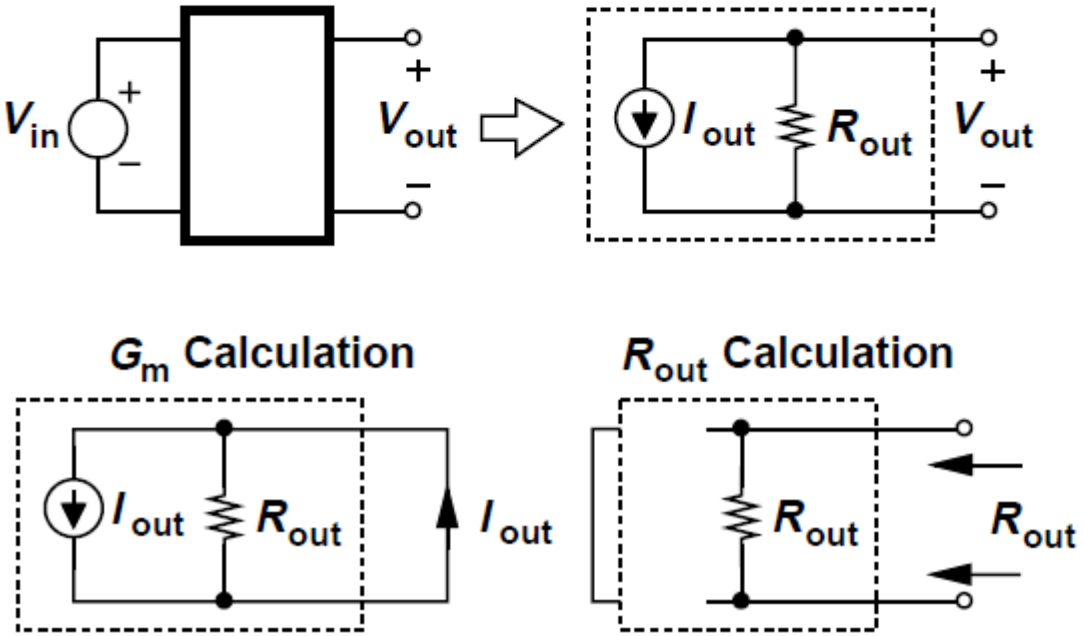
$$-(g_{m1}+g_{m2})V_{in}(r_{O1}||r_{O2}) = V_{out}$$

$$A_v = -(g_{m1}+g_{m2})(r_{O1}||r_{O2})$$

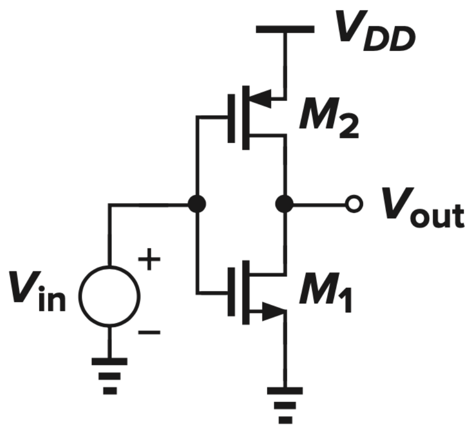
- Same output resistance as CS stage with current-source load, but higher transconductance
- Bias current of M_1 and M_2 is a strong function of PVT (why?)

Lemma

- In a linear circuit, the voltage gain is equal to $-G_m R_{out}$
  - G_m denotes the transconductance of the circuit when output is shorted to ground
  - R_{out} represents the output resistance of the circuit when the input voltage is set to zero
- Norton equivalent of a linear circuit



Using the Lemma …

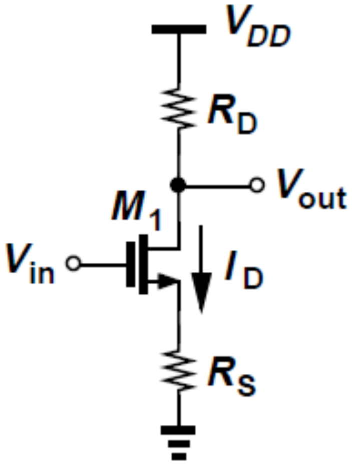


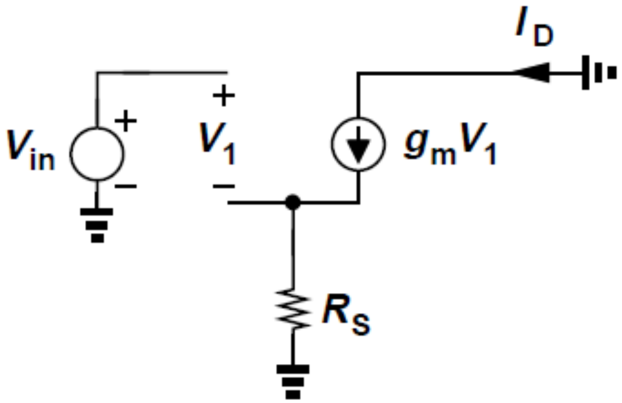
1. Find G_m

2. Find R_{out}

3. Gain=$-G_mR_{out}$

CS Stage with Source Degeneration





- Degeneration resistor R_S in series with source terminal makes input device more linear
  - As V_{in} increases, so do I_D and the voltage drop across R_S
  - Part of the change in V_{in} appears across R_S rather than gate-source overdrive, making variation in I_D smoother
- Gain is now a weaker function of g_m

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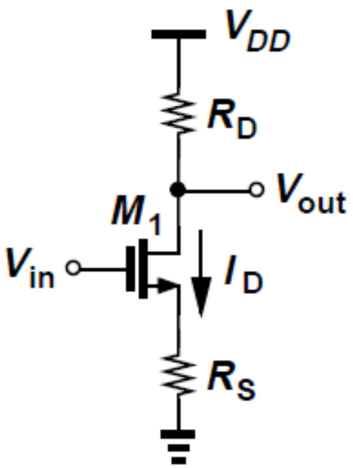
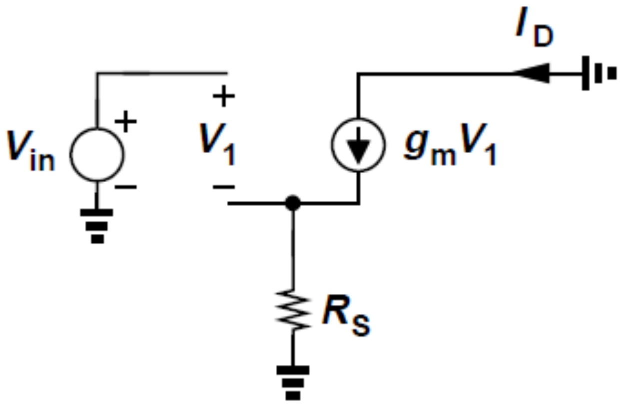
CS Stage with Source Degeneration





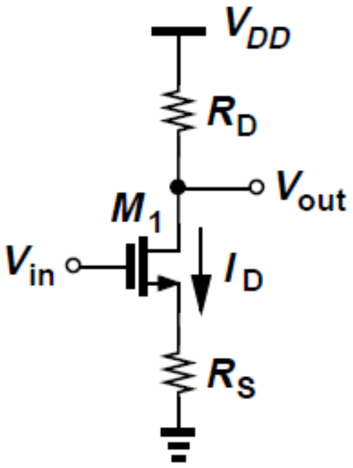
- Nonlinearity of circuit is due to nonlinear dependence of I_D (and consequently g_m) upon V_{in}
- Equivalent transconductance G_m of the circuit can be defied as

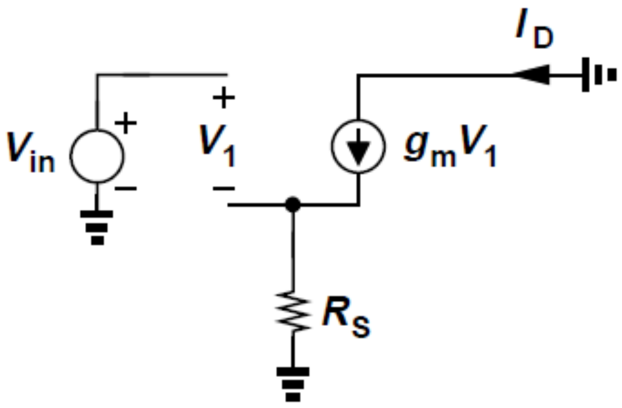
$$V_{in} = V_1 + I_{out} R_S$$
$$I_D = g_m V_1$$

$$G_m = \frac{g_m}{1 + g_m R_S}$$

$$A_v = -G_m R_D = \frac{-g_m R_D}{1 + g_m R_S}$$

CS Stage with Source Degeneration

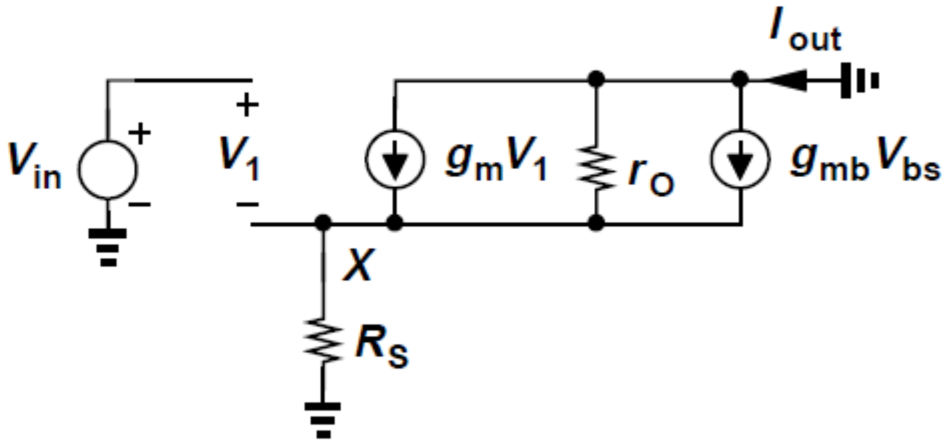




$$A_v = -G_m R_D$$
$$= \frac{-g_m R_D}{1 + g_m R_S}$$

- As R_S increases, G_m becomes a weaker function of g_m and hence I_D
- For $R_S \gg 1/g_m$, $G_m \approx 1/R_S$, i.e., $\Delta I_D \approx \Delta V_{in}/R_S$.
- Most of the change in V_{in} across R_S and drain current becomes a "linearized" function of input voltage

CS Stage with Source Degeneration



- Including body-effect and channel-length modulation, G_m is found from modified small-signal equivalent circuit

$$V_{in} = V_1 + I_{out} R_S$$

$$I_{out} = g_m V_1 - g_{mb} V_X - \frac{I_{out} R_S}{r_O}$$

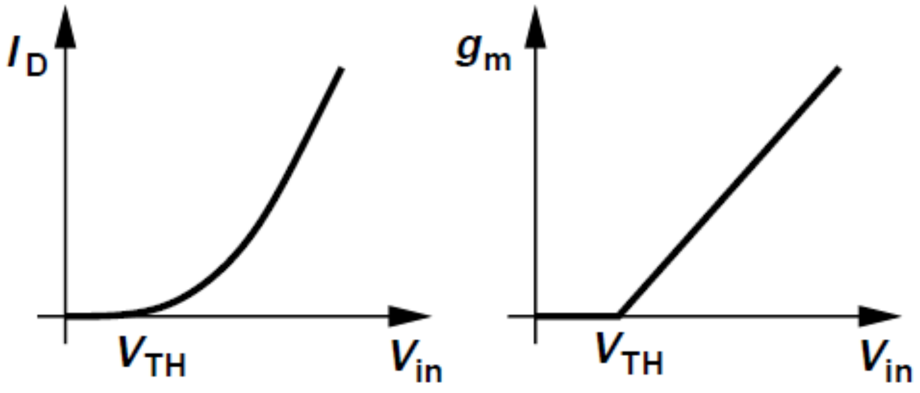
$$= g_m (V_{in} - I_{out} R_S) + g_{mb}(-I_{out} R_S) - \frac{I_{out} R_S}{r_O}$$

$$G_m = \frac{I_{out}}{V_{in}}$$

$$= \frac{g_m r_O}{R_S + [1 + (g_m + g_{mb}) R_S] r_O}$$

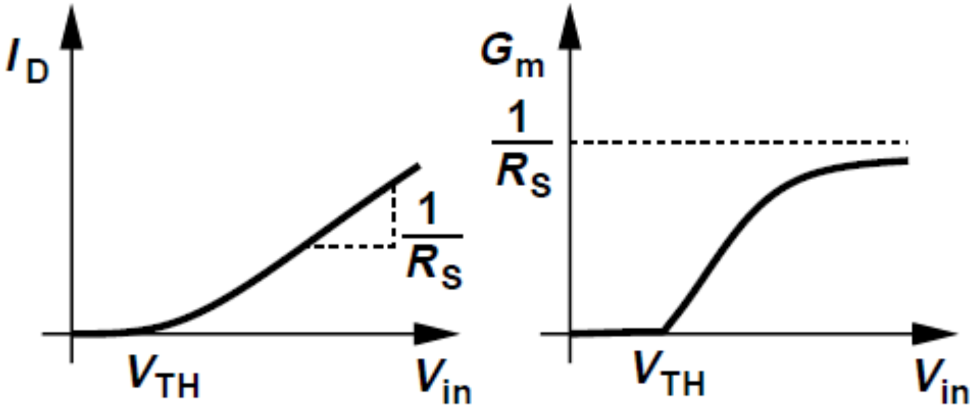
CS Stage with Source Degeneration: Large-signal Behavior

R_S=0



- I_D and g_m vary with V_{in} as derived in calculations in Chapter 2

R_S≠0



- At low current levels, turn-on behavior is similar to when R_S=0 since $1/g_m \gg R_S$ and hence $G_m \approx g_m$
- As overdrive and g_m increase, effect of R_S becomes more significant

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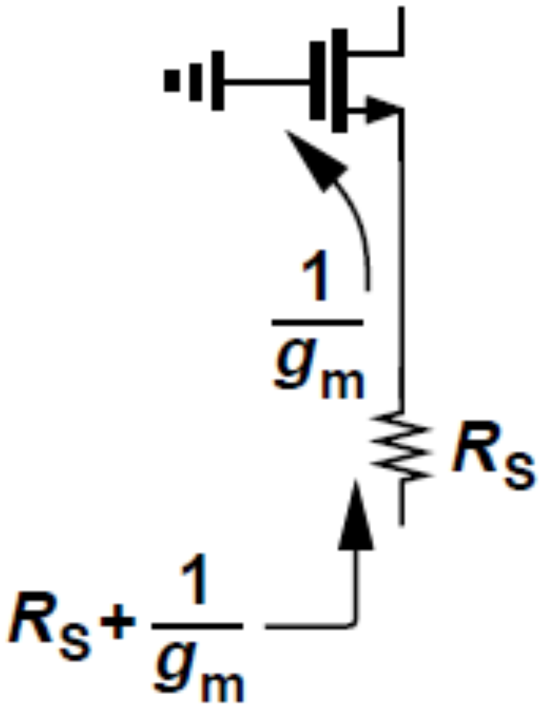
CS Stage with Source Degeneration

- Small-signal derived previously can be written as

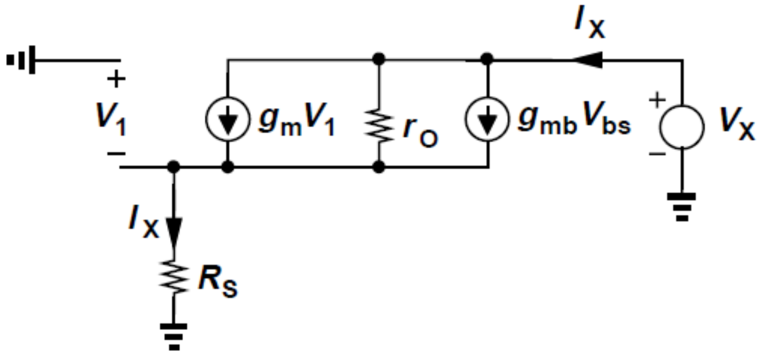
$$A_v = -\frac{R_D}{\frac{1}{g_m} + R_S}$$

- Denominator = Series combination of inverse transconductance + explicit resistance seen from source to ground
- Called "resistance seen in the source path"
- Magnitude of gain = Resistance seen at the drain/ Total resistance seen in the source path



CS Stage with Source Degeneration

- Degeneration causes increase in output resistance



- Ignoring R_D and including body effect in small-signal equivalent model,

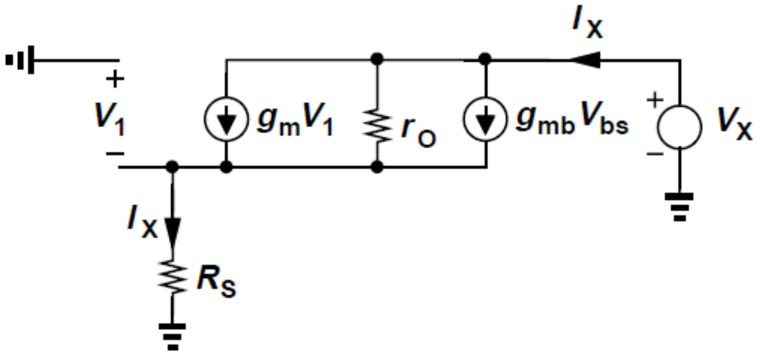
$$V_1 = -I_X R_S,$$
$$I_X - (g_m + g_{mb})V_1 = I_X + (g_m + g_{mb})R_S I_X$$
$$r_O[I_X + (g_m + g_{mb})R_S I_X] + I_X R_S = V_X$$

$$R_{out} = [1 + (g_m + g_{mb})R_S]r_O + R_S$$
$$= [1 + (g_m + g_{mb})r_O]R_S + r_O$$

- r_o is boosted by a factor of $\{1 + (g_m+g_{mb})R_S\}$ and then added to R_S
- Alternatively, R_S is boosted by a factor of $\{1 + (g_m+g_{mb})r_o\}$ and then added to r_o

CS Stage with Source Degeneration

- Compare $R_S = 0$ with $R_S > 0$



- If $R_S = 0$, $g_m V_1 = g_{mb} V_{bs} = 0$ and $I_X = V_X / r_O$

- If $R_S > 0$, $I_X R_S > 0$ and $V_1 < 0$, obtaining negative $g_m V_1$ and $g_{mb} V_{bs}$
- Thus, current supplied by V_X is less than V_X/r_o and hence output impedance is greater than r_o

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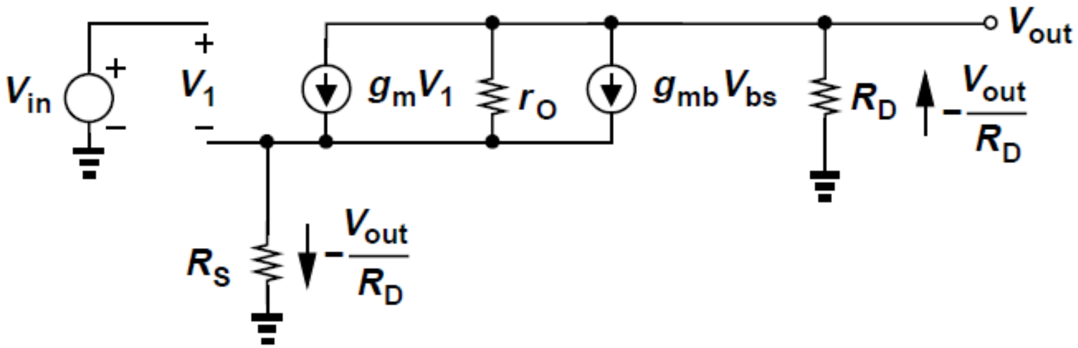
CS Stage with Source Degeneration



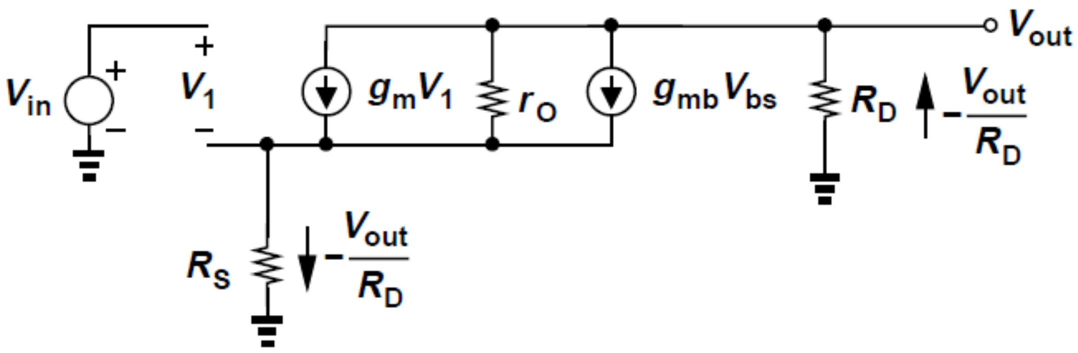
- To compute gain in the general case including body effect and channel-length modulation, consider above small-signal model
- From KVL at input,

$$V_1 = V_{in} + V_{out} R_S / R_D$$

- KCL at output gives

$$\begin{aligned} I_{ro} &= -\frac{V_{out}}{R_D} - (g_m V_1 + g_{mb} V_{bs}) \\ &= -\frac{V_{out}}{R_D} - \left[g_m \left(V_{in} + V_{out} \frac{R_S}{R_D} \right) + g_{mb} V_{out} \frac{R_S}{R_D} \right] \end{aligned}$$

CS Stage with Source Degeneration



- Since voltage drops across r_O and R_S must add up to V_{out},

$$
\begin{aligned}
V_{out} &= I_{ro} r_O - \frac{V_{out}}{R_D} R_S \\
&= -\frac{V_{out}}{R_D} r_O - \left[g_m \left(V_{in} + V_{out} \frac{R_S}{R_D} \right) + g_{mb} V_{out} \frac{R_S}{R_D} \right] r_O - V_{out} \frac{R_S}{R_D}
\end{aligned}
$$

- Voltage gain is therefore

$$\frac{V_{out}}{V_{in}} = \frac{-g_m r_O R_D}{R_D + R_S + r_O + (g_m + g_{mb}) R_S r_O}$$

CS Stage with Source Degeneration

- Calculate the gain using the lemma (A_v=-$G_m R_{out}$):