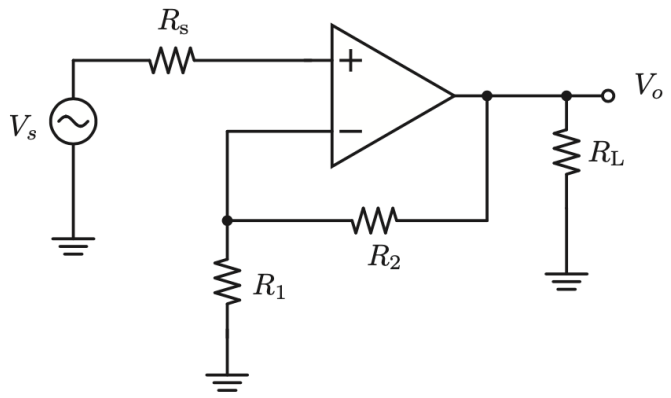
EE 332 Circuits and Devices II Autumn 2020
Final Exam Date: Dec. 15 (8:30-10:30am)

1. (30 pts) An op-amp is configured to provide gain (V_O/V_S) of 10V/V to a $R_L = 1k\Omega$ load. Model the op-amp with the following parameters:

- $R_{in} = \infty$ (ideal)
- $R_{out} = 0$ (ideal)
- $A_0 = 100$ (not infinite)
- $f_0 = 100MHz$ (not ideal: finite bandwidth frequency)
- DC offset voltage of V_{OS} (not ideal)



a) What should be the ratio of R_2/R_1 to achieve the target close-loop gain assuming amplifier has an infinite gain.

b) How does the closed-loop gain change if R_s or R_L changes?

c) What's the gain error due to the non-infinite gain of amplifier?

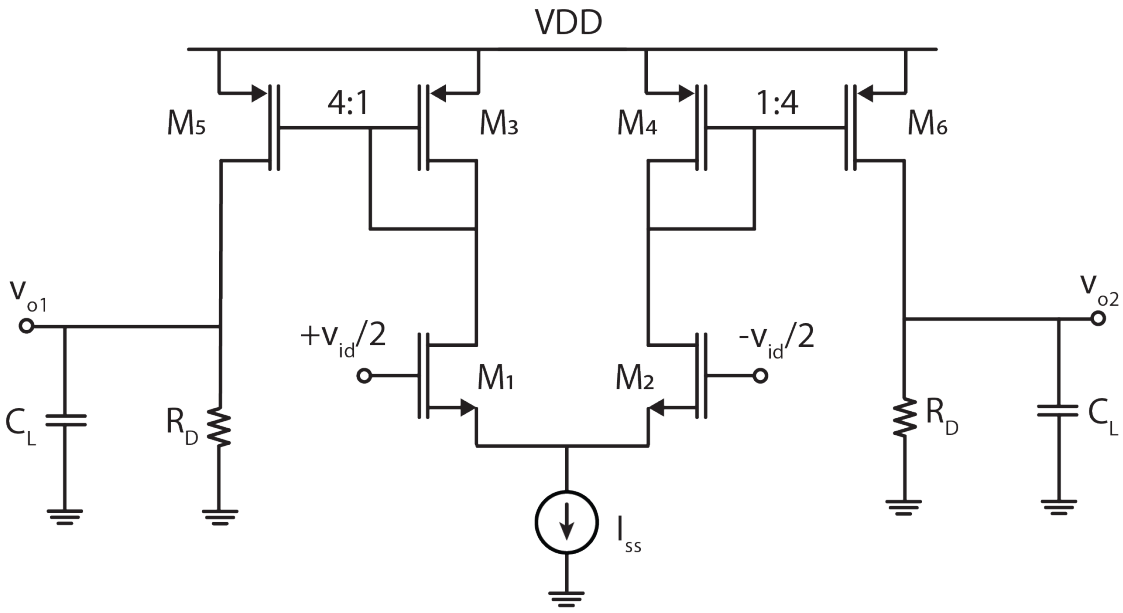
d) When the input voltage is set to zero, we observe an output voltage of +50mV. What is the offset voltage? Specify the magnitude and draw an equivalent offset voltage in front of an ideal op-amp to model this effect.

e) What's the approximate bandwidth for small signals? (-3dB bandwidth) *Hint*: You do not need to derive this result but simply state it from what you know about feedback amplifiers.

f) Assuming that amplifier has an input-referred voltage noise of $\overline{V_{n,in}^2}$, calculate the noise PSD at the output node due to the amplifier, R_1, R_2, and R_S noise sources. (Write down your answer in parameters only)

2. (40 pts) For the fully differential amplifier shown below:

Assume: VDD=1.5V, $|Vth_{n,p}|$=0.3V, $\mu_n C_{ox} = \frac{400\mu A}{V^2}, \mu_n = 2\mu_p, \lambda_p = 0.2V^{-1}, \lambda_n = 0.1V^{-1}, \gamma = 0$ *for both NMOS and PMOS devices.*



$$R_D = 1.5k\Omega, I_{SS} = 2mA$$

$$\left(\frac{W}{L}\right)_{3,4} = 2\left(\frac{W}{L}\right)_{1,2} = 250, \left(\frac{W}{L}\right)_{5,6} = 4\left(\frac{W}{L}\right)_{3,4}, L = 65nm$$

a) Draw the half-circuit model for differential mode.

b) Find the small-signal differential gain (V_{out}/V_{id}), where $V_{out}=V_{o1}-V_{o2}$.

c) What's the output single-ended and differential peak-to-peak output swing?

d) Find the output pole (ω_{out}) assuming $C_L = 1pF$.

e) Assuming amplifier has only a single pole from part (d), what is the unity-gain bandwidth (ω_u)?

f) Assuming $C_{GS} = 1fF$ for $W = 1um$ (and it linearly scales with W for larger transistors), find the second pole location (ignore all other parasitic capacitances).

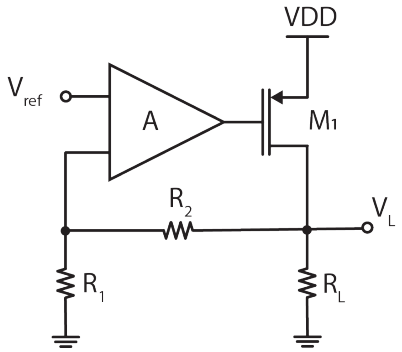
g) Draw the Bode plot (magnitude only, label the slopes and poles).

3. (30 pts) In this problem we are interested to build a circuit that can generate a lower supply voltage (V_L) from a VDD supply (V_L < VDD) to support a circuit-block with a total load of R_L.

a) Suggest a very simple circuit to generate V_L from VDD?

b) In your proposed circuit, how would the output voltage (V_L) change if R_L varies?

A student taking EE332 suggested the circuit below using a feedback to generate V_L:



c) What would be the polarity of amplifier inputs to make sure it forms a negative feedback? (either redraw the circuit or annotate the figure and explain your answer here)

d) Ideally, what is the value of V_L as a function of V_{ref}, and resistor values.

e) Calculate the loop-gain in this circuit in terms of circuit parameters and g_m of M_1. Ignore r_o of M_1 and assume there is no loading effect from the feedback network (i.e., $R_{1,2} >> R_L$).

f) How does the output voltage (V_L) change if R_L varies in this circuit supposing amplifier's gain (A) is large enough?