EE 332 Circuits and Devices II Autumn 2020

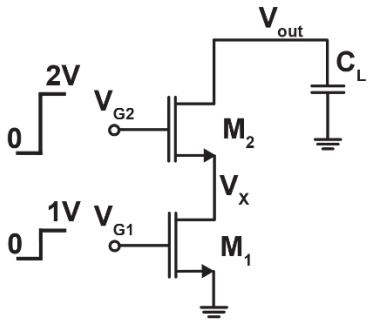
Midterm Exam Exam Date: Nov. 16 (5-7pm)

Assume: VDD=1.5V, $|Vth_{n,p}|$=0.3V, $\mu_n C_{ox} = \frac{400\mu A}{V^2}$, $\mu_n = 2\mu_p$, $\lambda_p = 0.2V^{-1}$, $\lambda_n = 0.1V^{-1}$, $\gamma = 0$ for both NMOS and PMOS devices.

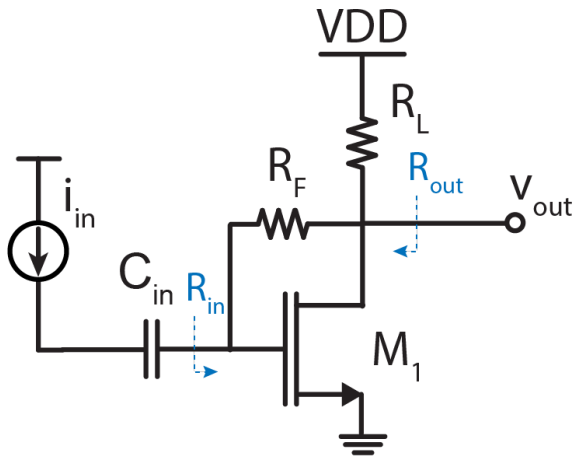
1. (15 pts) Suppose that while V_{out} at the beginning is at 5V, V_{G1} and V_{G2} will rise to 1V and 2V respectively and the capacitance starts discharging through $M_{1,2}$. Answer the following questions:

a) Find the regions of operation for M1 and M2 as C_L discharges.

b) Plot V_x,V_{out}, and the current through C_L over time, mark the voltage levels and voltages where M1 or M2 transit into another operation region (a qualitative plot is enough, no need to solve any equation!). Describe shortly how the circuit behaves and ends up discharging the cap.



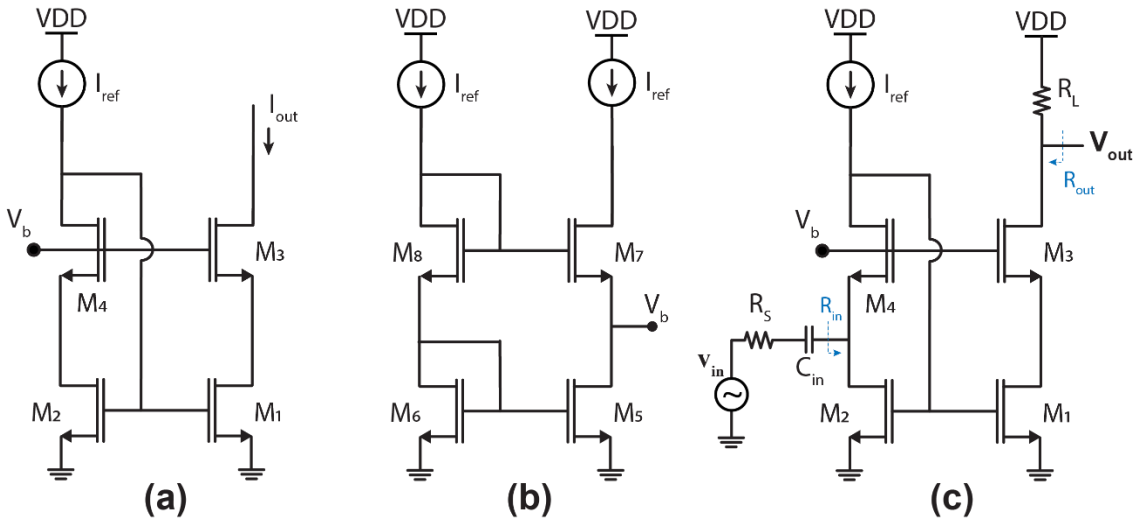
2. (25 pts) For the single-stage amplifier given below, answer to the following questions. Assume C_{in} is very large and will be short in small-signal models and i_{in} is an AC current source at the input. Your solution should only depend on gm, r_o, R_F, and R_L.



a) Draw the small-signal model.
b) Find the small-signal gain (V_{out}/i_{in})
c) Find R_{out} and R_{in}.

3. (30 pts) For the current-mirror circuit shown in Figure a,

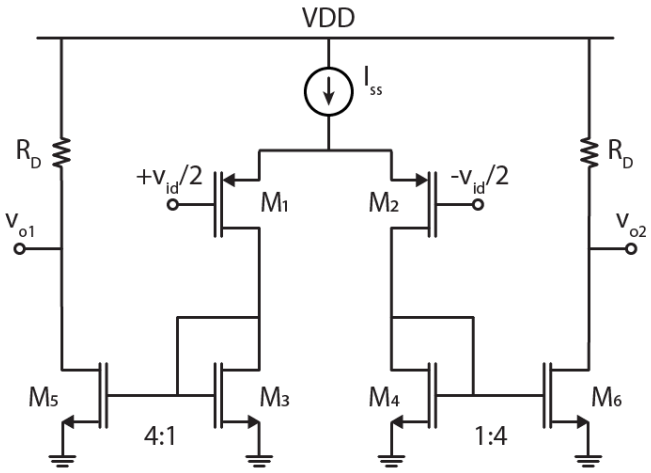
a) If $(W/L)_1=(W/L)_3=k(W/L)_2= k(W/L)_4$, what is the ratio of I_{out}/I_{ref}?
b) What is the minimum working voltage at the output as a function of V_{od} and V_b? What should be V_b value to minimize this voltage limit?
c) Suppose we want to use the circuit shown in Figure b to generate this V_b. Assuming W/L of M_{5-7} is the same as W/L of M_2, what should be the ratio of $(W/L)_8/(W/L)_1$?



Now we decided to turn this current mirror into an amplifier shown in Figure c. Assume that C_{in} is a very large decoupling cap (short in small-signal) and the input voltage source has a series resistance of Rs. Also, assume $\boldsymbol{\lambda = 0}$ and the I_{ref} current source has an output impedance of R_{ref}. For parts d-e, write down your answers in terms of g_m of M_{1-4}, Rs, R_L, and R_{ref}.

d) Calculate the input and output impedances.
e) Find the gain (Vout/Vin).

4. (30 pts) For the differential amplifier shown below:



$$VDD = 1.2V, R_D = 1.5k\Omega, R_{SS} = 10k\Omega$$

$$\left(\frac{W}{L}\right)_{3,4} = 2\left(\frac{W}{L}\right)_{1,2} = 200, \left(\frac{W}{L}\right)_5 = 4\left(\frac{W}{L}\right)_3, \left(\frac{W}{L}\right)_6 = 4\left(\frac{W}{L}\right)_4$$

a) What should be the I_{SS} value in order to bias output nodes ($V_{o1/2}$) at VDD/2=0.6V?
b) Based on I_{SS} value from part a, what is the g_m and V_{od} of $M_{1,2}$?
c) Draw the differential-mode half circuit and calculate the differential gain ($\frac{v_{o2}-v_{o1}}{v_{id}}$)?
d) Draw the common-mode half circuit and calculate single ended common-mode gain ($\frac{v_{o1/2}}{v_{cm}}$)?
e) Find differential and single-ended peak-to-peak output swing.
f) If we implement the tail current with a PMOS with W/L=200, what would be the input common-mode range?