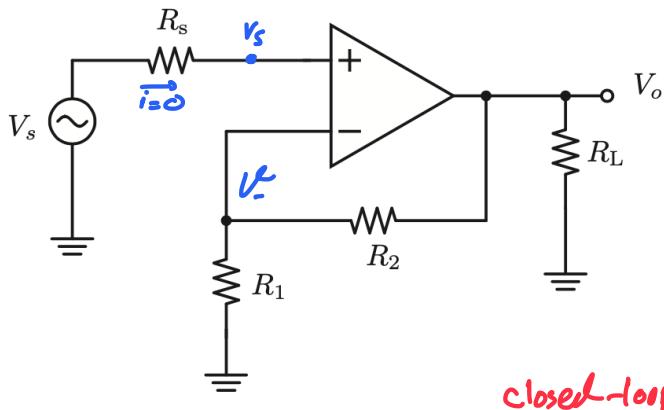


1. (30 pts) An op-amp is configured to provide gain (V_o/V_s) of 10V/V to a $R_L = 1k\Omega$ load. Model the op-amp with the following parameters:

- $R_{in} = \infty$ (ideal)
- $R_{out} = 0$ (ideal)
- $A_0 = 100$ (not infinite)
- ~~$\omega_0 = 100MHz$~~ (not ideal: finite bandwidth frequency)
- DC offset voltage of V_{os} (not ideal)



- a) What should be the ratio of R_2/R_1 to achieve the target gain assuming amplifier has an infinite gain.

By "feedback law", $V_- = V_S$, thus:

$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_s \implies \text{for } 1 + \frac{R_2}{R_1} = 10 \implies \boxed{\frac{R_2}{R_1} = 9}$$

- b) How does the closed-loop gain change if R_s or R_L changes?

closed-loop gain is $1 + \frac{R_2}{R_1}$, which doesn't depend on $R_s/R_L \Rightarrow$ No change

- c) What's the gain error due to the non-infinite gain of amplifier?

$$\beta A = \text{loop-gain} = \frac{R_1}{R_1+R_2} A$$

$$\text{closed-loop gain} = \frac{A}{1+\beta A} = \frac{A}{1 + \frac{R_1}{R_1+R_2} A} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + \frac{(1+R_2/R_1)}{A}}$$

$$\approx \left(1 + \frac{R_2}{R_1}\right) \left(1 - \underbrace{\left(1 + \frac{R_2}{R_1}\right) \frac{1}{A}}_{\text{gain error}}\right) \quad \text{error} = 1.0 \times \frac{1}{100} = 0.1 \quad \boxed{1\%}$$

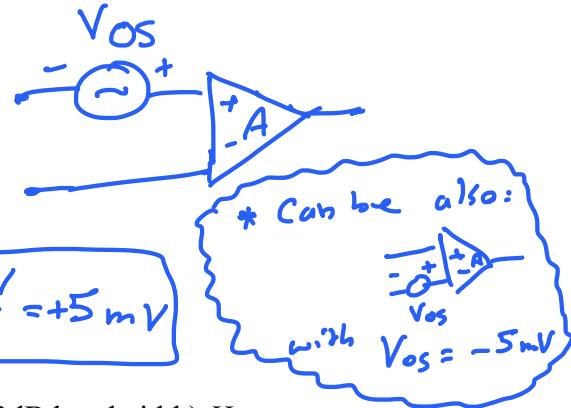
- d) When the input voltage is set to zero, we observe an output voltage of +50mV. What is the offset voltage? Specify the magnitude and draw an equivalent offset voltage in front of an ideal op-amp to model this effect.

$V_{os} \rightarrow V_o$ is similar to $V_s \rightarrow V_o$

thus :

$$V_o = \underbrace{(1 + R_2/R_1)}_{50\text{mV}} \underbrace{(A_s + V_{os})}_{10}$$

$$\Rightarrow V_{os} = \frac{50\text{mV}}{10} = +5\text{mV}$$



- e) What's the approximate bandwidth for small signals? (-3dB bandwidth) Hint: You do not need to derive this result but simply state it from what you know about feedback amplifiers.

$$\omega_{cl} = (1 + \beta A) \omega_o = (1 + \frac{R_1}{R_1 + R_2} A) \omega_o$$

$$\Rightarrow f_{cl} = (1 + \frac{100}{9}) \times 100 \text{ MHz}$$

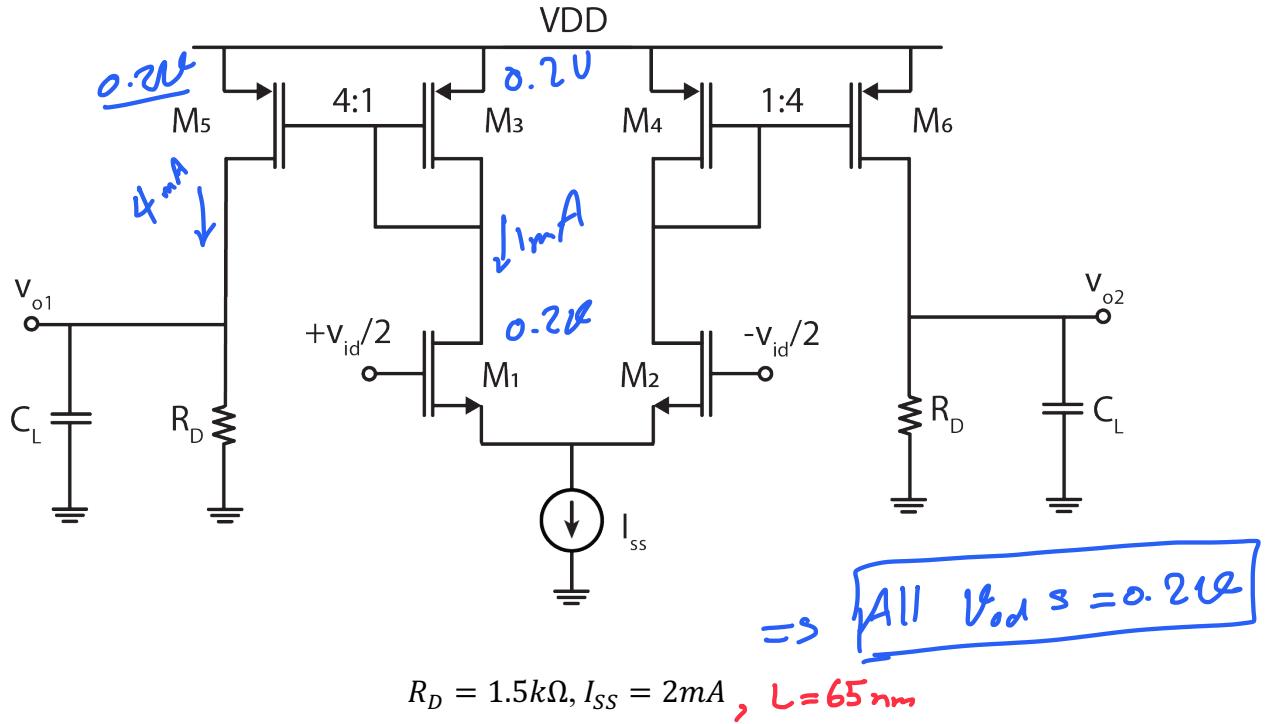
$$\approx 1.21 \text{ GHz}$$

- f) Assuming that amplifier has an input-referred voltage noise of $\overline{V_{n,in}^2}$, calculate the noise PSD at the output node due to the amplifier, R_1 , R_2 , and R_s noise sources. (Write down your answer in parameters only)

Noise Source	$\overline{V_{n,in}^2}$	H	$\overline{V_n^2} \times H ^2 @ \text{output}$
Amp.	$\overline{V_{n,in}^2}$	$1 + R_2/R_1$	$\overline{V_{n,in}^2} (1 + R_2/R_1)^2$
R_s	$4kT R_s$	$1 + R_2/R_1$	$4kT R_s (1 + R_2/R_1)^2$
R_1	$4kT / R_1$	R_2	$4kT R_1 (R_2/R_1)^2$
R_2	$4kT R_2$	1	$4kT R_2 \times 1$
			$\sum \rightarrow \overline{V_{n,out}^2}$

2. (40 pts) For the fully differential amplifier shown below:

Assume: $VDD = 1.5V$, $|V_{th,n,p}| = 0.3V$, $\mu_n C_{ox} = \frac{400\mu A}{V^2}$, $\mu_n = 2\mu_p$, $\lambda_p = 0.2V^{-1}$, $\lambda_n = 0.1V^{-1}$, $\gamma = 0$ for both NMOS and PMOS devices.

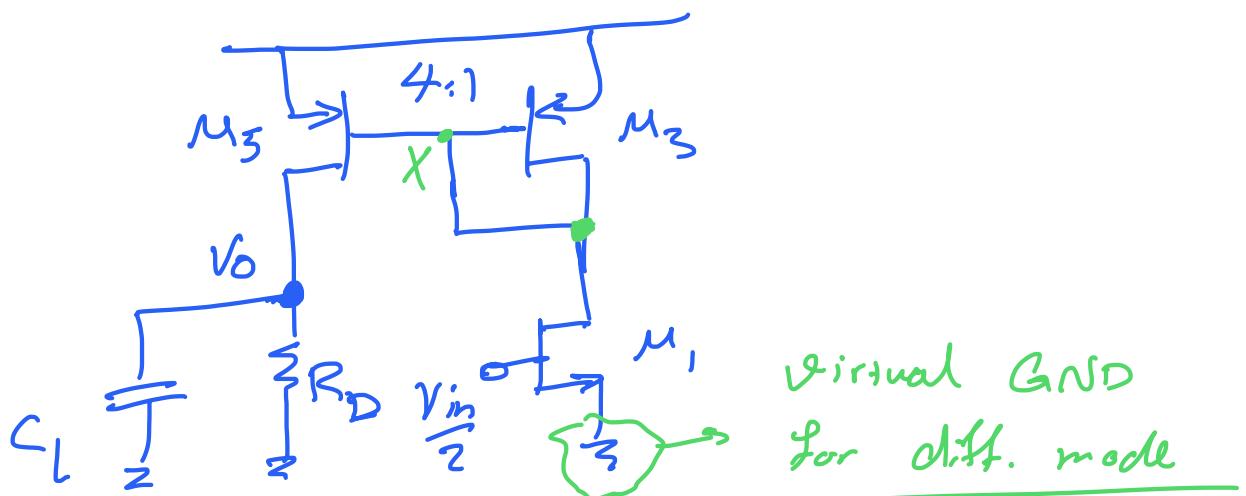


$$\left(\frac{W}{L}\right)_{3,4} = 2 \left(\frac{W}{L}\right)_{1,2} = \cancel{250}, \left(\frac{W}{L}\right)_5 = 4 \left(\frac{W}{L}\right)_3, \left(\frac{W}{L}\right)_6 = 4 \left(\frac{W}{L}\right)_4$$

$\cancel{250}$

$\frac{5}{125}$

- a) Draw the half-circuit model for differential mode.



b) Find the small-signal differential gain (V_{out}/V_{id}).

$$\frac{V_o}{\left(\frac{V_{in}}{2}\right)} = \frac{V_x}{\left(\frac{V_{in}}{2}\right)} \times \frac{V_o}{V_x} = -g_{m_1} \underbrace{\left(R_o \parallel R_{o3} \parallel \frac{1}{g_{m_3}}\right)}_{1.0mS} \times -g_{m_5} \underbrace{\left(R_o \parallel R_D\right)}_{1.25k\Omega} \\ = g_{m_1} \times \frac{g_{m_5}}{g_{m_3}} \times \left(R_o \parallel R_L\right) = 4 \times \frac{1.0mS}{2 \times 1mA} \times \left(\frac{1}{0.2 \times 1mA} \parallel 1.5k\Omega\right) \\ = 40 \times \frac{1.5 \times 1.25}{1.5 + 1.25} \approx \boxed{28}$$

c) What's the output single-ended and differential peak-to-peak output swing?

$$S.E_{pp} \text{ Swing} = V_{DD} - V_{oD5} = 1.5 - 0.2V = \boxed{1.3V}$$

$$D.M_{pp} \text{ Swing} = 2 \times S.E_{pp} = \boxed{2.6V}$$

d) Find the output pole (ω_{out}) assuming $C_L = 1pF$.

$$\omega_{out} = \frac{1}{R_{out} + C_L} = \frac{1}{(R_o \parallel R_D) C_L} = \frac{1}{0.7k\Omega \times 1pF} \\ \approx \frac{1 \text{ Grad/s}}{0.7} \approx \boxed{1.4 \text{ Grad/s}} \quad \left(f_{out} = \frac{\omega_{out}}{2\pi} = 223 \text{ MHz} \right)$$

e) Assuming $C_{GS} = 1fF/um$, find the second pole location (ignore all other parasitic capacitances).

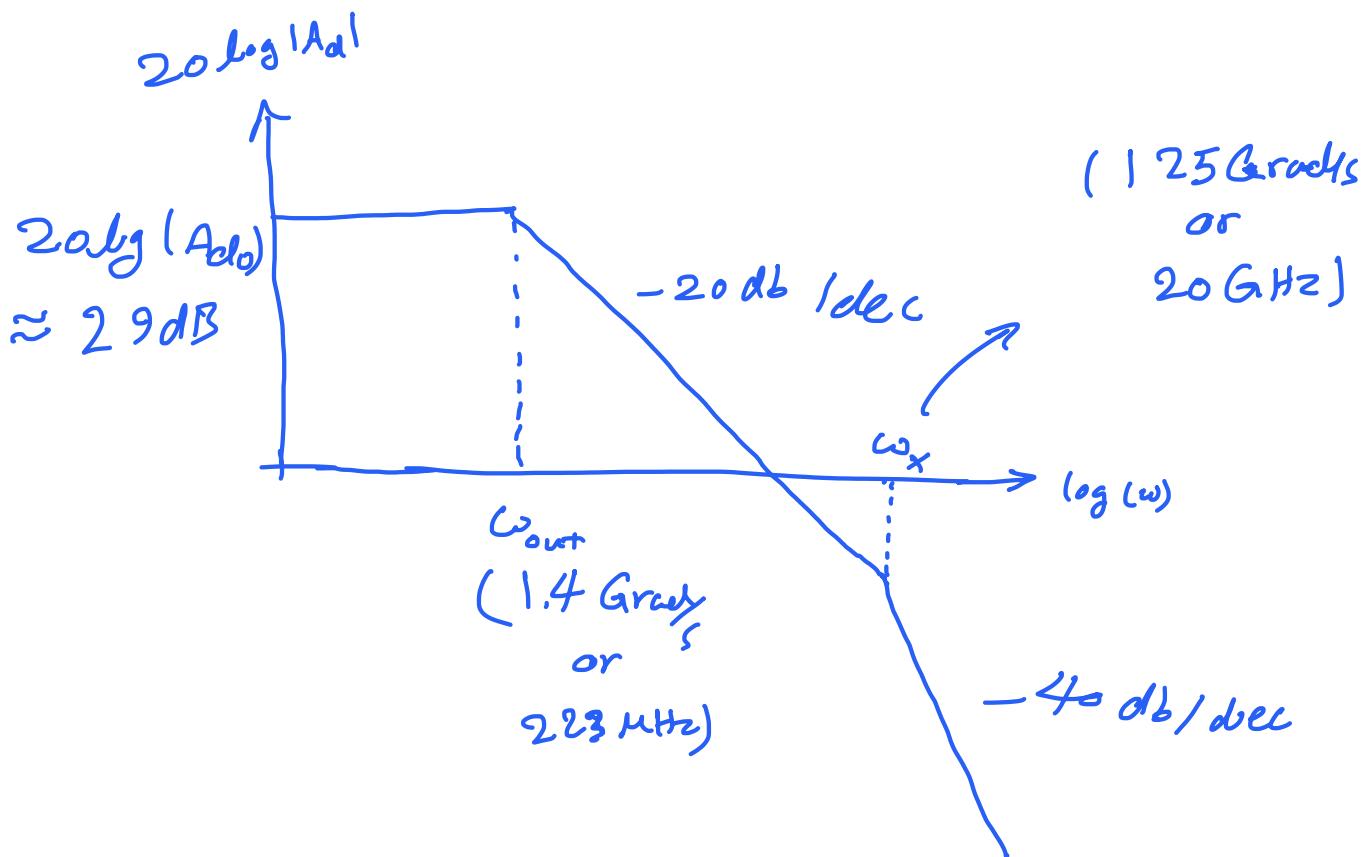
$$C_X = C_{GS3} + C_{GS5} = \frac{(250 + 1000) \times 65nm}{1.3k\Omega} \times 1fF/\mu m \approx \boxed{80fF}$$

$$R_X = R_{o3} \parallel \frac{1}{g_{m3}} = \frac{1.3k\Omega}{0.2 \times 1mA} \parallel \frac{1000}{2 \times 1mA} \approx \boxed{0.1k\Omega}$$

$$\Rightarrow \omega_X = \frac{1}{R_X C_X} = \frac{1}{0.1k\Omega \times 80fF} = \frac{1000 \text{ Grad/s}}{8} \approx \boxed{125 \text{ Grad/s}}$$

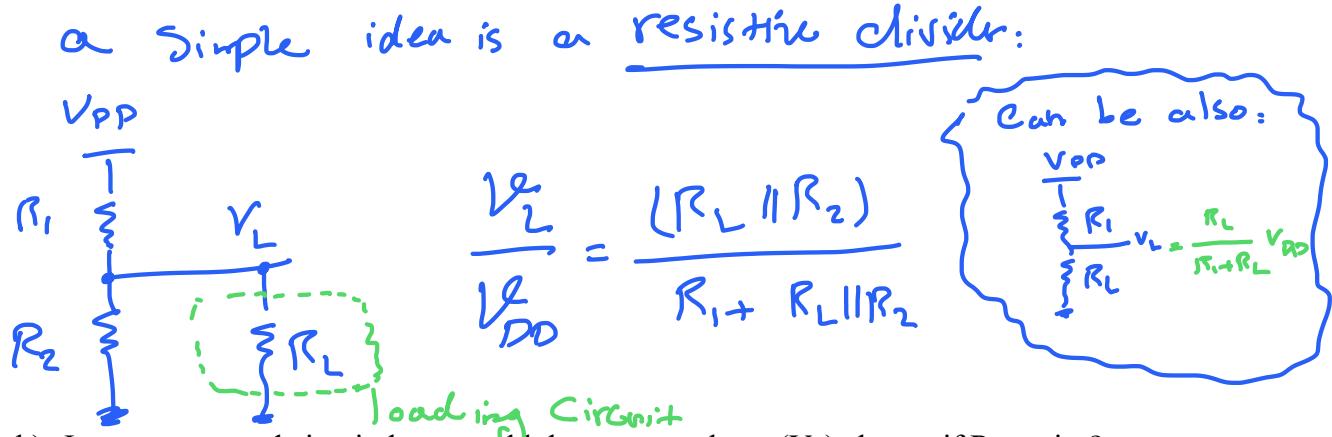
$$(f_X = \frac{\omega_X}{2\pi} \approx 20 \text{ GHz})$$

f) Plot the bode plot (magnitude only, label the slopes and poles).



3. (30 pts) In this problem we are interested to build a circuit that can generate a lower supply voltage (V_L) from a VDD supply to support a circuit-block with a total load of R_L .

- a) Suggest a very simple circuit to generate V_L from VDD?



- b) In your proposed circuit, how would the output voltage (V_L) change if R_L varies?

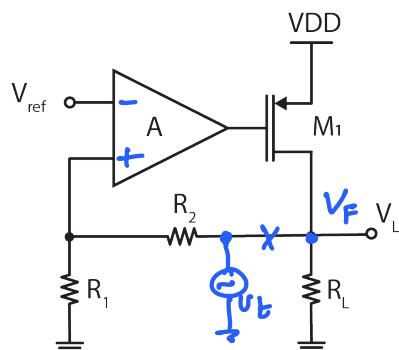
if R_L changes, $\frac{V_L}{V_{DD}}$ changes

Since $R_L \parallel R_2$ will also change!

and this is not good :(

* in practice current drawn by any circuit fluctuates depending on the operation mode, etc., thus R_L will vary over time.

One EE332 student suggested the circuit below which uses feedback to set the V_L value.



- c) What would be the polarity of amplifier inputs to make sure it forms a negative feedback? *Shown on the circuit* ←

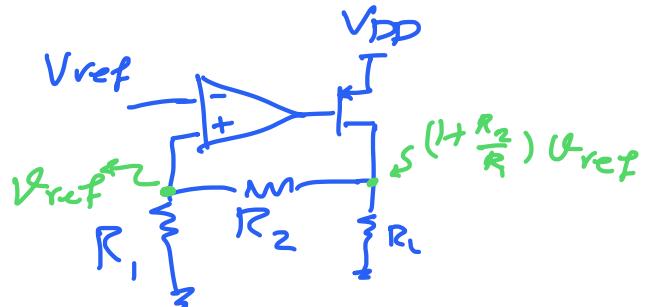
use loop-gain method & see how to make

$$\text{loop-gain negative} \Rightarrow \text{loop gain} = \frac{R_1}{R_1 + R_2} \times A \times -g_m R_L$$

if you choose wrong polarity, it will be positive!

- d) Ideally, what would be the value of V_L (as a function of V_{ref} , and resistor values)

$$V_L = V_{ref} \times \left(1 + \frac{R_2}{R_1}\right)$$



- e) Calculate the loop-gain in this circuit in terms of circuit parameters and g_m of M_1 . (ignore r_o of M_1) *ignore load*.

$$\text{Loop-gain} = -\frac{R_1}{R_1 + R_2} A (g_m, R_L)$$

** ignoring the loading impact of feedback network.*

- f) How does the output voltage (V_L) change if R_L varies in this circuit? *If A is large!*

Doesn't change as long as loop-gain is large enough.