EE 332 Circuits and Devices II Autumn 2022

Homework 8 Due: Dec. 4 (11:59pm)

1. *Razavi Problem 6.7:* Estimate the poles of each circuit in Fig. 6.59. *(Hint:* First add/draw the parasitic capacitances of transistors, next try to lump them together and reduce the circuit, then use Miller approximation, and finally associate each node to a pole and file the pole from 1/RC*)*

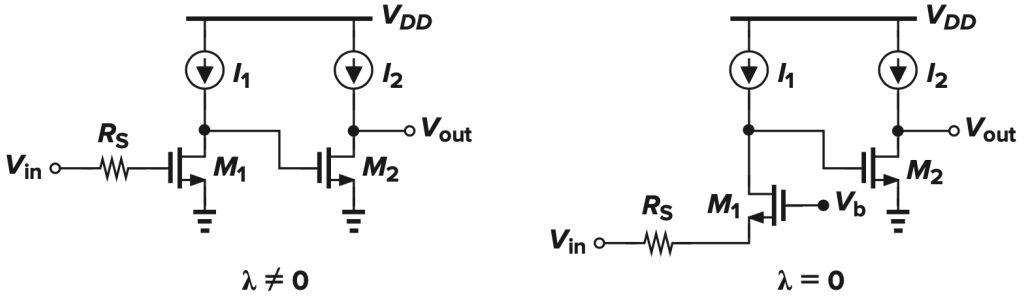
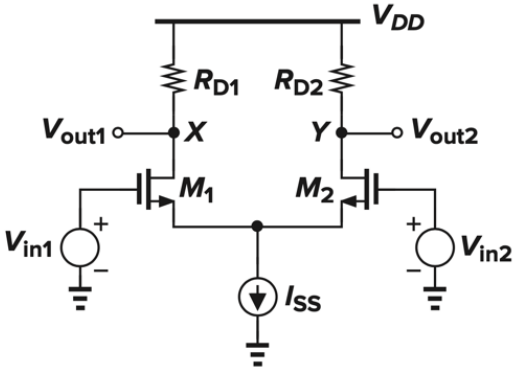


Figure 6.59

2. For the symmetric differential amplifier shown below, assume a capacitor of size 0.5pF is connected between output nodes (V_{out1} and V_{out2}), ignore all parasitic capacitances, $\lambda = \gamma = 0$, and $R_{D1}=R_{D2}=R_D$:



a) What should be R_D for the amplifier to have a 3db-bandwidth of 100MHz?
b) For a differential gain of 20, what should be g_m of input devices?
c) What would be the I_{ss} and W for $M_{1,2}$ if L=65nm, V_{od}=0.2V and $\mu_n C_{ox} = \frac{200\mu A}{V^2}$?
d) If C_{GS} and C_{DB} of $M_{1,2}$ will be ~1fF/μm and ~0.2fF/μm (fF per μm-width), respectively, estimate an additional pole at the input created by $Cgs_{1,2}$ and assuming a source resistance (R_s) of 100Ω. (Use Miller approximation)
e) Draw the amplitude and phase Bode plots using these two poles.