EE 332: Devices and Circuits II

Lecture 5: Current Mirrors

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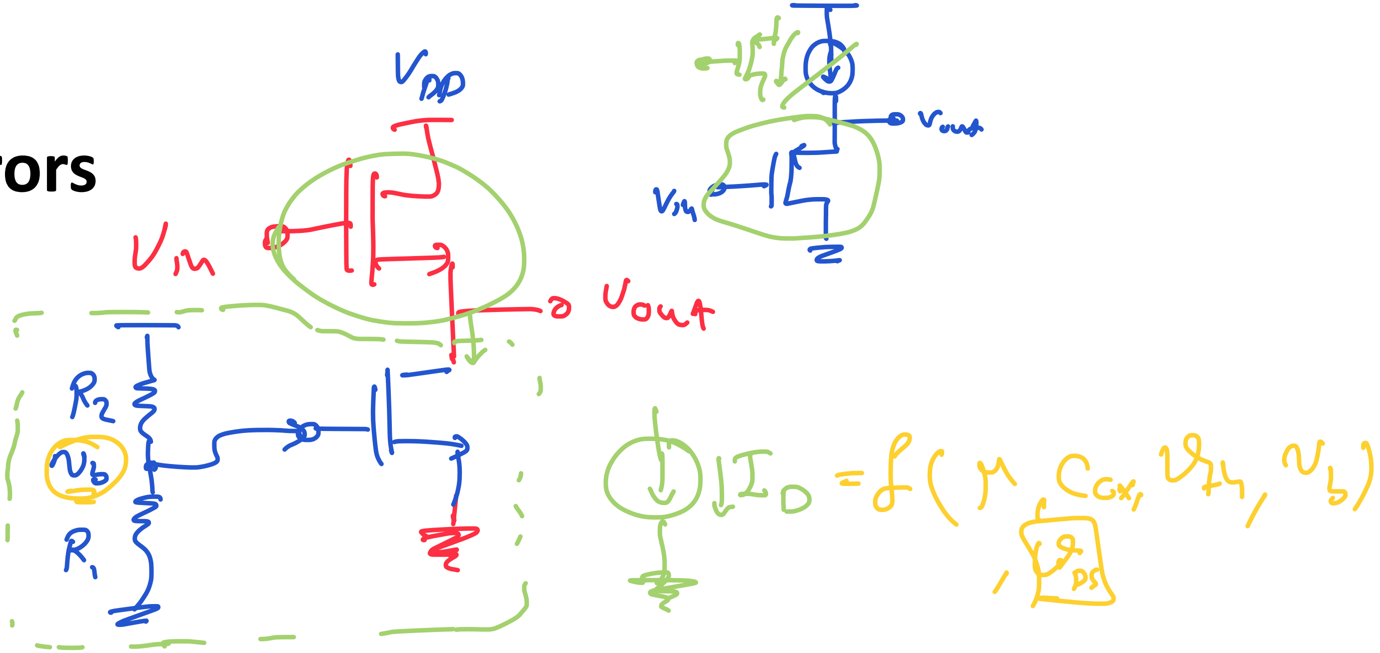
$V_{DD} \times \frac{R_1}{R_1+R_2}$



ELECTRICAL & COMPUTER ENGINEERING

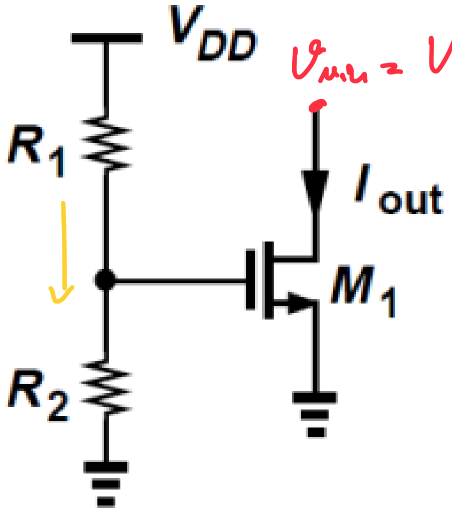
Basic Current Source

Ideal Current Source: ?

large R_s => big area X

X thermal Noise

$\frac{V_{DD}}{R_1+R_2}$



$V_{min} = V_{OD}$

- Assuming M1 is in saturation, we can write

$$I_{out} \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1+R_2}V_{DD} - V_{TH}\right)^2$$

X PVT Sensitive

- The threshold voltage may vary by 50 to 100 mV from wafer to wafer
- Both μn and VTH exhibit temperature dependence
- We must seek other methods of biasing MOS current sources.

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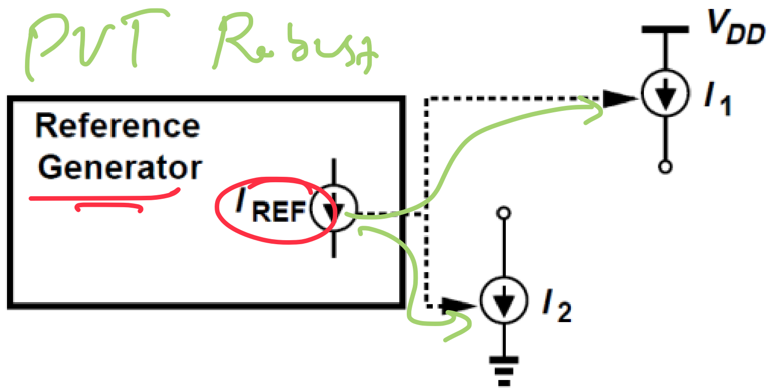
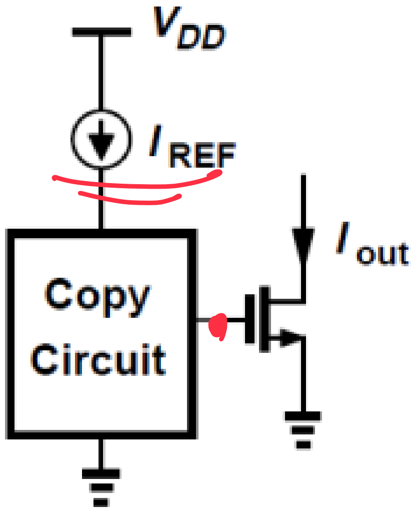
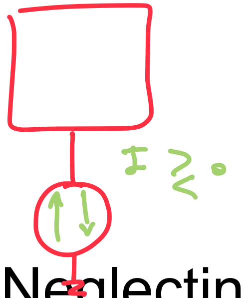
Copying currents (Current Mirroring)

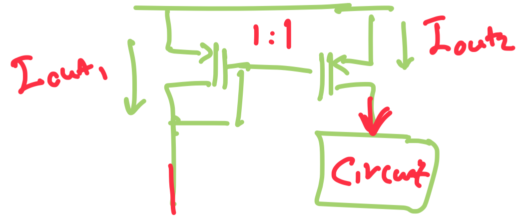




- Use of a reference to generate various currents.
- Two identical MOS devices that have equal V_{GS} and operate in saturation carry equal currents
  - Can change the ratio with W/L
- Distributed "Ref" can be eventually in either Voltage or Current domain.
  - What are the Pros/Cons of each?

Basic Current Mirror





$V_{x} = V_{DD_1}$

- Neglecting channel-length modulation (CLM), we can write

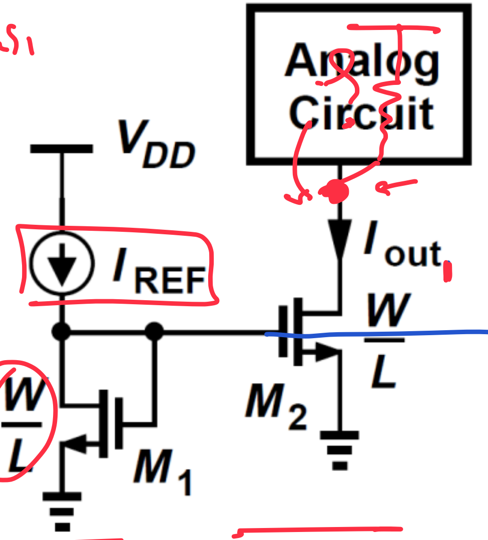
V_{GS_1}

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2 \quad (1+\lambda \cancel{V_{DS}})$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2 \quad (1+\lambda V_{DS})$$

$$\boxed{I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}}$$

diode connected device



$V_{GS_1} = V_{GS_2}$

- Allows precise copying of the current with no dependence on process and temperature
- How would Channel-Length Modulation will impact this result?

ELECTRICAL & COMPUTER ENGINEERING

$g_m = \frac{\partial I}{\partial V_{gs}}$ $\quad \frac{1}{r_o} = g_{ds} = \frac{\partial I}{\partial V_{DS}}$

Example

$g_m = \mu C_{ox} \frac{W}{L}(V_{gs} - V_{th})$

$\frac{(W/L)_3}{(W/L)_2} = k \Longrightarrow \frac{g_{m3}}{g_{m2}} = \cancel{?}\ k$

- Calculate the small-signal voltage gain of the circuit shown in Figure.

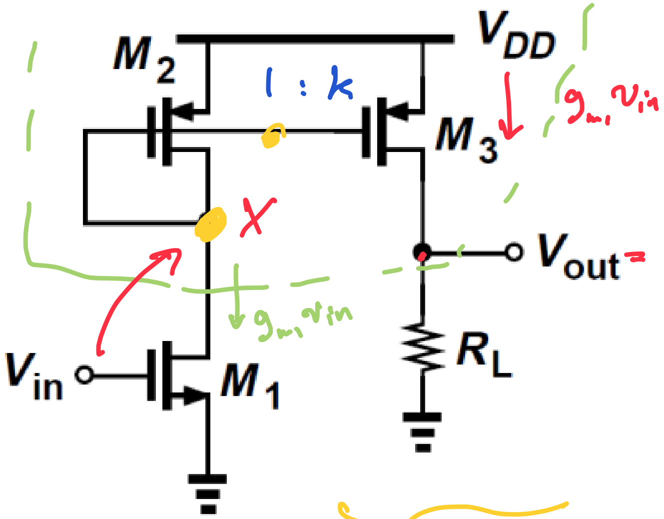
$$I_{D2} = I_{D1}$$

$$I_{D3} = I_{D2}(W/L)_3/(W/L)_2$$

- $A_v = ?$ $\quad \frac{V_{out}}{V_{in}} = \frac{V_X}{V_{in}} \times \frac{V_{out}}{V_X}$

$$= \left(-g_{m1} \times \frac{1}{g_{m2}}\right) \times \left(-g_{m3} \times R_L\right)$$

$$= g_{m1} R_L \times \left(\cancel{\frac{g_{m3}}{g_{m2}}}\right) k$$

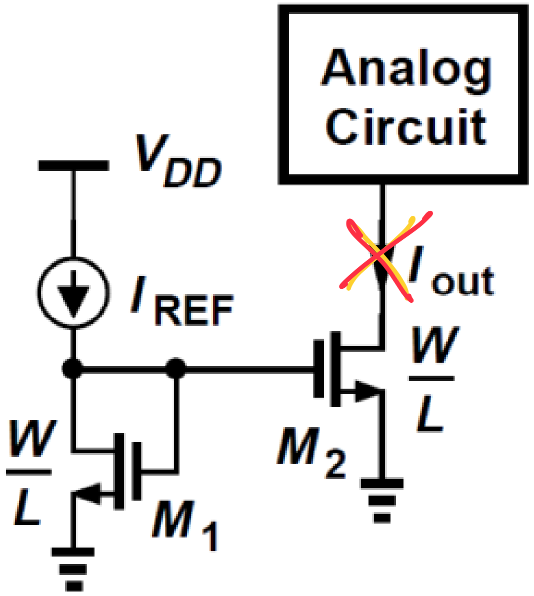


C.S

diode connected load

C.S in PMOS

Cascode Current Mirrors



$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS1})$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS2})$$

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \cdot \underbrace{\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}}$$

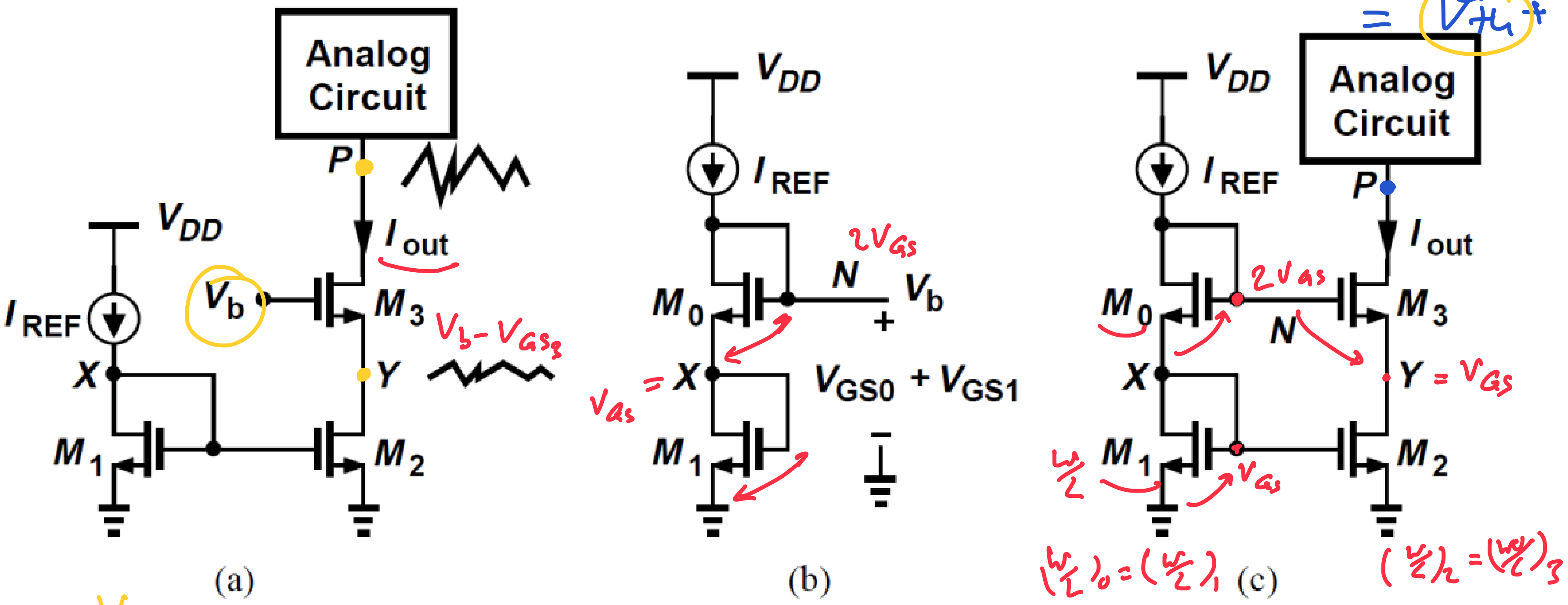
depends on "Box" circuit.

$V_{DS_2} = V_{GS_1} = V_{DS_1}$

- While $V_{DS1} = V_{GS1} = V_{GS2}$, V_{DS2} may not equal V_{GS2}
- We can (a) force V_{DS2} to be equal to V_{DS1}, or (b) force V_{DS1} to be equal to V_{DS2}.

First Approach

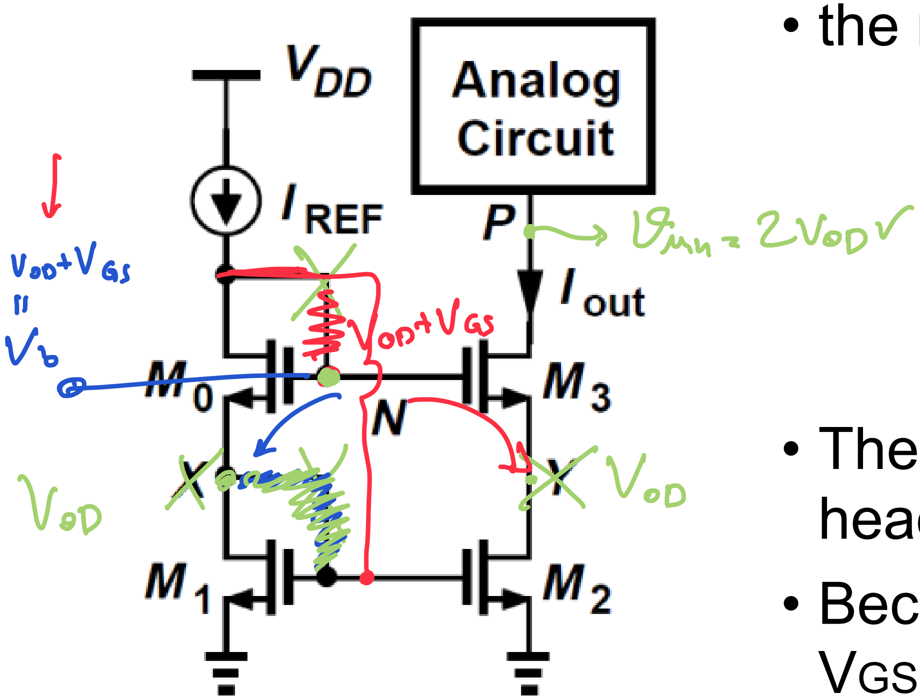
$\times\ V_{min}\ @\ P = V_{GS} + V_{OD}$
$= V_{th} + 2V_{OD}$



$V_b = 2V_{GS} \Rightarrow V_Y = V_X = V_{GS}$

- A cascode device can shield a current source, thereby reducing the voltage variations across it.
- But, how do we ensure that $V_{DS2} = V_{DS1}$?
- We must generate V_b such that $V_b - V_{GS3} = V_{DS1} (= V_{GS1})$

Example

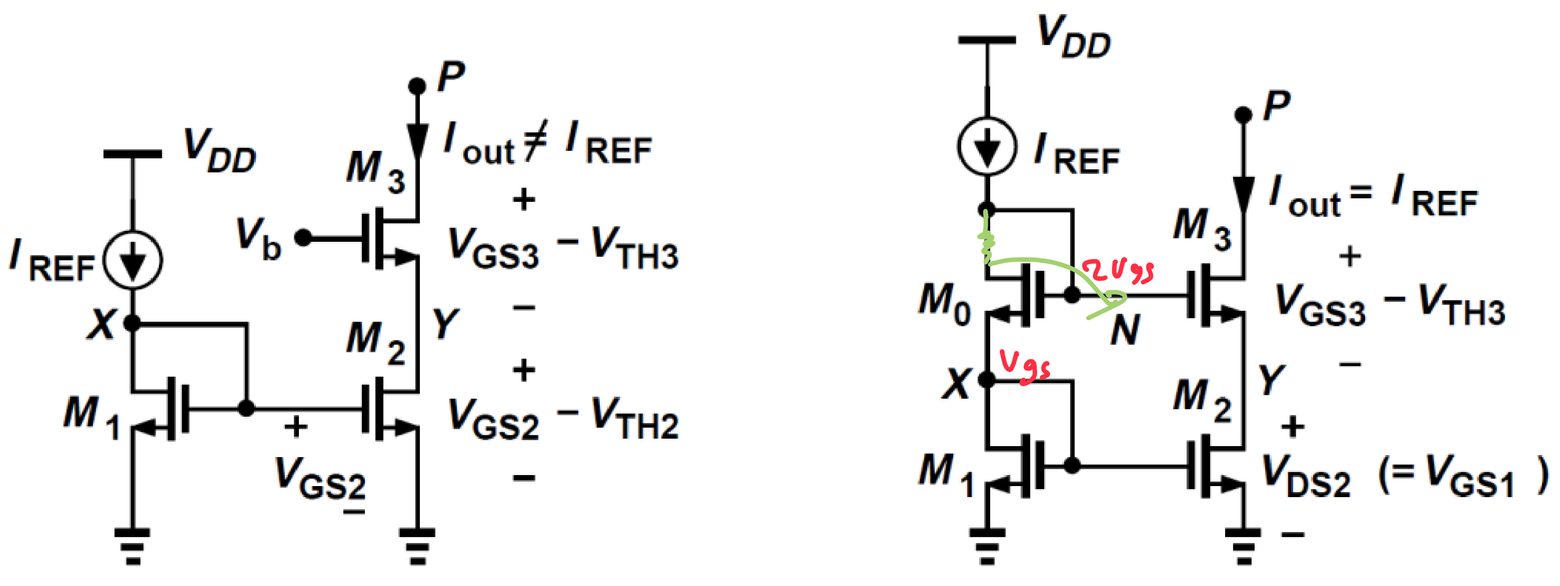


- the minimum allowable voltage at node P is equal to

$$V_N - V_{TH} = V_{GS0} + V_{GS1} - V_{TH}$$
$$= (V_{GS0} - V_{TH}) + (V_{GS1} - V_{TH}) + V_{TH}$$

- The cascode mirror "wastes" one threshold voltage in the headroom.
- Because $V_{DS2} = V_{GS2}$, whereas V_{DS2} could be as low as $V_{GS2}-V_{TH}$ while maintaining M2 in saturation.

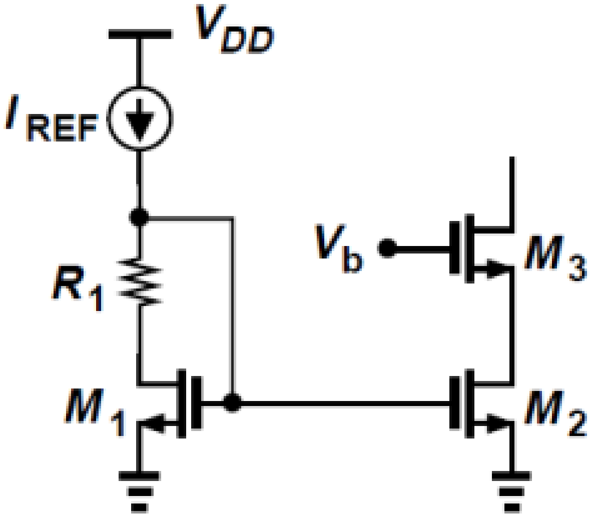
Approach summary



(a) (b)

- In Fig(a), V_b is chosen to allow the lowest possible value of V_P but the output current does not accurately track I_{REF}.
- In Fig(b), a higher accuracy is achieved, but the minimum level at P is higher by one threshold voltage.

Second Approach



- Consider the branch shown in Fig. 5.16(b)
- As a candidate and write $V_b = V_{GS5} + R_6 I_6$.

$$R_1 I_{REF} \approx V_{TH1}$$

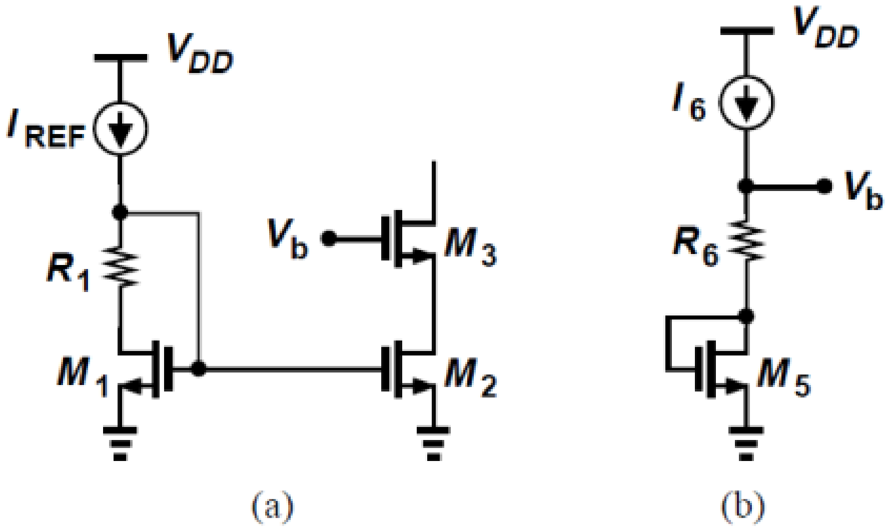
$$V_b = V_{GS3} + (V_{GS1} - V_{TH1})$$

- Thus, from a small-signal point of view, the combination is close to a diode-connected device.
- But …

(1) It may be difficult to guarantee that $R_1 I_{REF} \approx V_{TH1}$

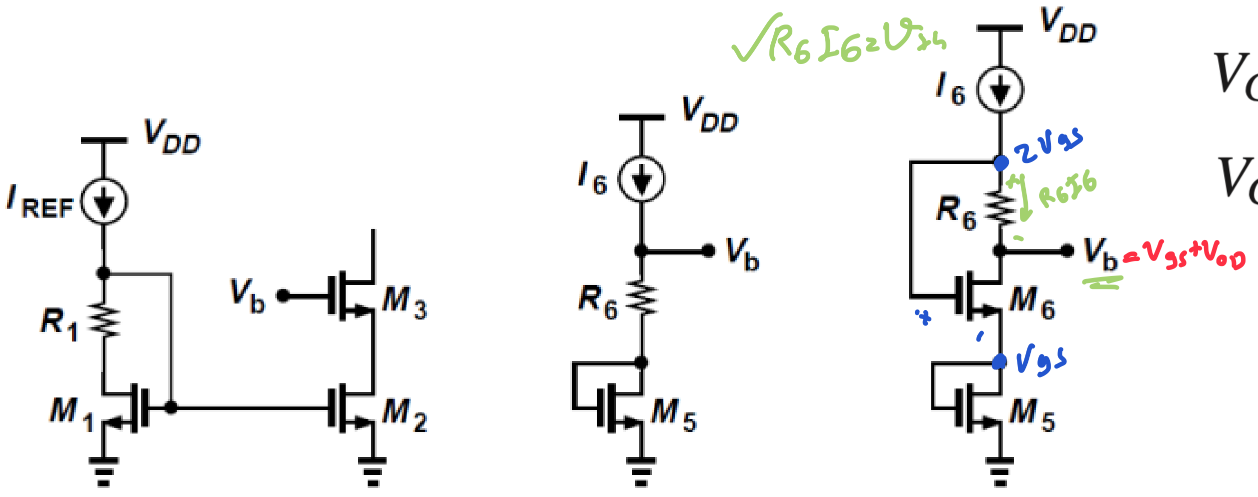
(2) The generation of V_b is not straightforward.

Generate Vb



- Consider the branch shown in Fig(b) as a candidate and write $V_b = V_{GS5} + R_6 I_6$.
- Choose I_6 and $(W/L)_5$ such that: $V_{GS5} = V_{GS3}$
- However, the condition $R_6 I_6 = V_{GS1} - V_{TH1} = V_{GS1} - R_1 I_{REF}$ is hard to meet.
  - This condition translates to: $R_6 I_6 + R_1 I_{REF} = V_{GS1}$

Generate Vb



(a) (b) (c)

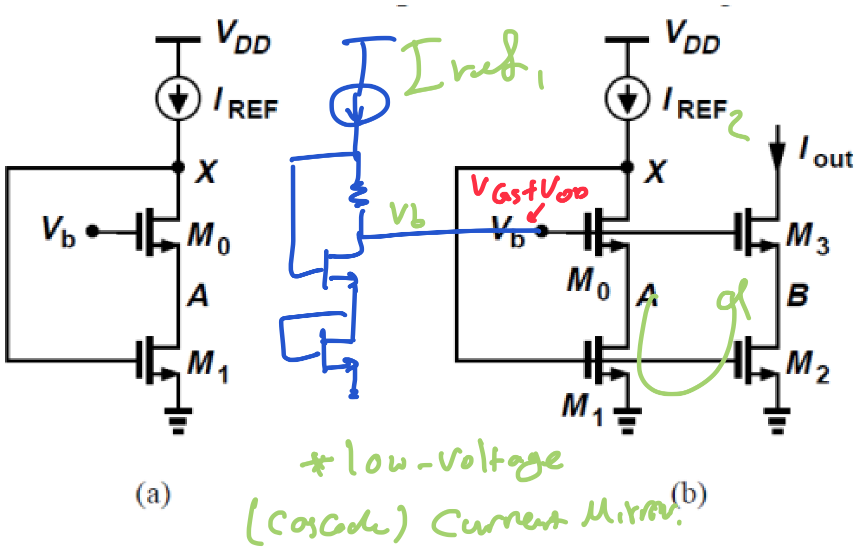
$$V_{GS5} = V_{GS3}$$

$$V_{GS6} - R_6 I_6 = V_{GS1} - V_{TH1}$$

$$= V_{GS1} - R_1 I_{REF}$$

- It is now possible to ensure that V_{GS6} and V_{GS1} track each other.
- For example, we may simply choose $I_6 = I_{REF}$, $R_6 = R_1$, and $(W/L)_6 = (W/L)_1$

Another circuit topology



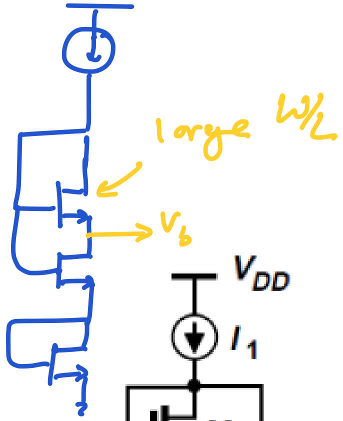
- In this case

$$V_{DS1} = V_b - V_{GS0}$$

- Must have $V_b - V_{TH0} \le V_X\ (= V_{GS1})$ for M0 to be saturated and $V_{GS1} - V_{TH1} \le V_A\ (= V_b - V_{GS0})$ for M1 to be saturated.
- A solution exists if $V_{GS0} + (V_{GS1} - V_{TH1}) \le V_b \le V_{GS1} + V_{TH0}$
- We must therefore size M_0 to ensure its overdrive is well below V_{TH1}.

W/L large $\Longrightarrow V_{gs} \approx V_{th}$

How to generate V_b



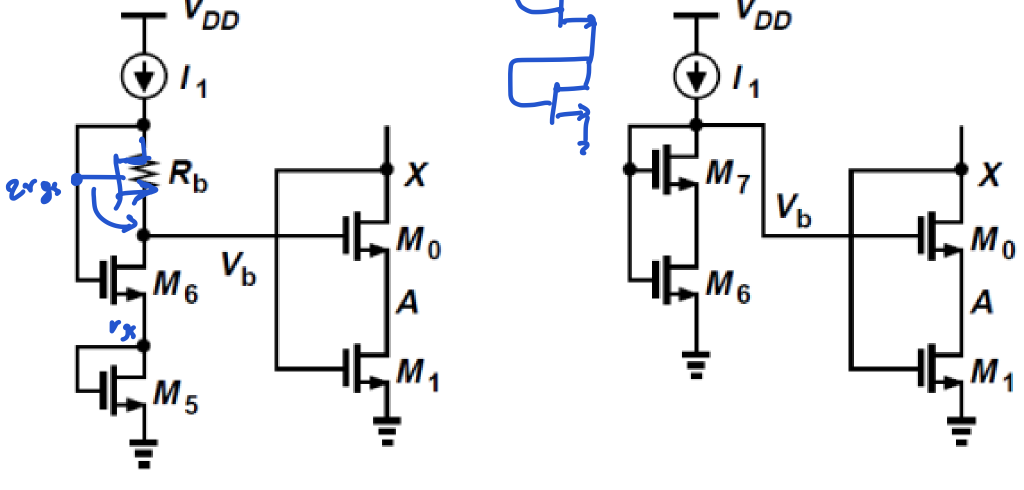
- In figure (a):
  - Need $V_b = V_{GS0} + (V_{GS1} - V_{TH1})$

- So we need to …

V_{th}

$$V_{GS5} \approx V_{GS0}$$

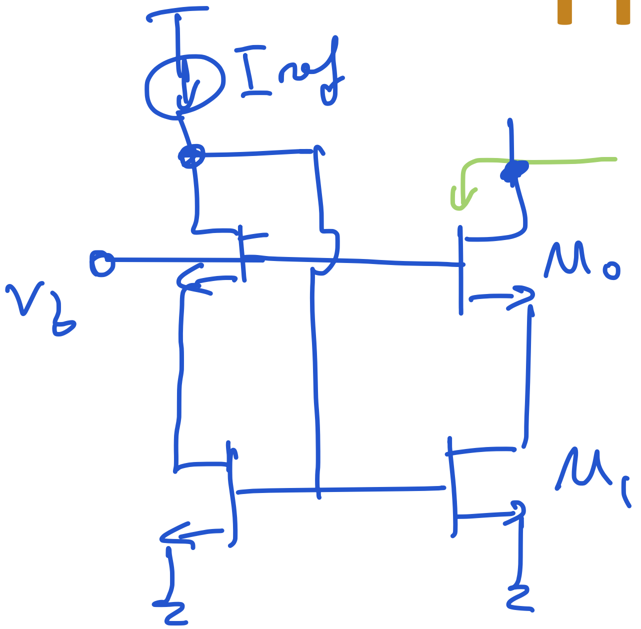
$$\underbrace{V_{DS6} = V_{GS6} - R_b I_1} \approx V_{GS1} - V_{TH1}$$



(a) (b)

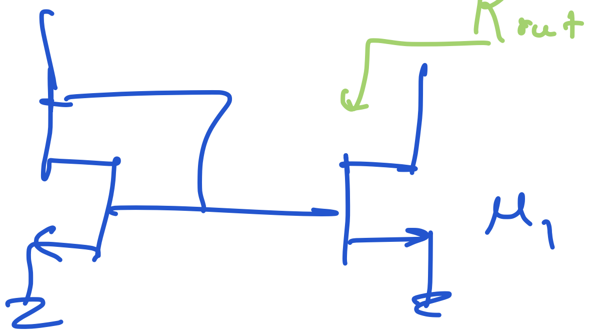
- Some inaccuracy nevertheless arises because M_5 does not suffer from body effect whereas M_0 does.
- Also, the magnitude of $R_6 x I_1$ is not well-controlled.
- A simpler alternative is shown in Fig (b)

Practical Current Distribution



$$R_{out} \approx \overbrace{r_{o_0}}^{\frac{1}{\lambda I_D}} + r_{o_0} r_{o_1} g_{m_0} + r_{o_1} \approx r_{o_1}\left(g_{m_0} r_{o_1}\right)$$

10-100



$$R_{out} \approx r_{o_1} = \frac{1}{\lambda I_D}$$

$$\lambda \propto \frac{1}{L}$$

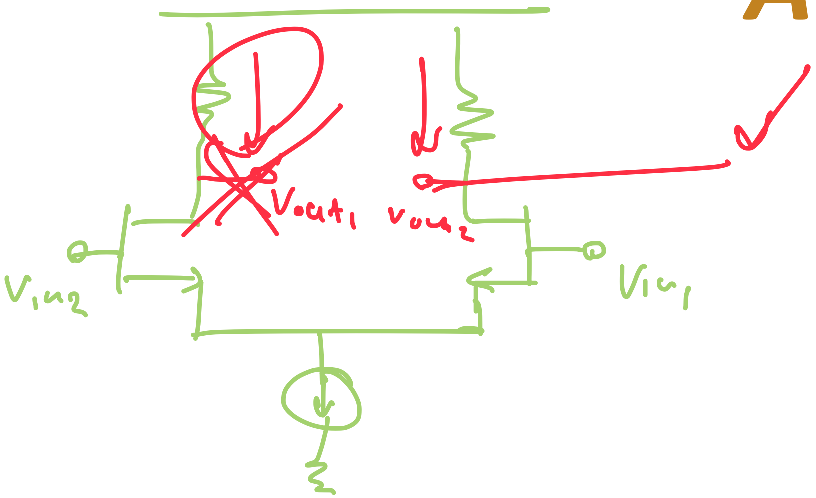
large L

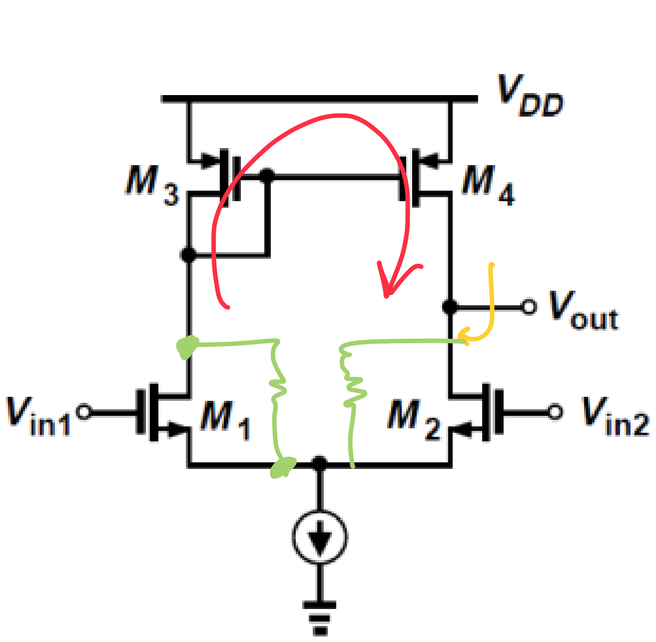
$\Downarrow$

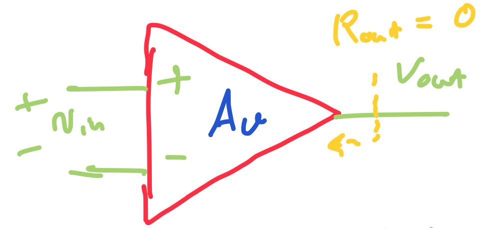
✓ increase the r_o

Active Current Mirrors

Op Amp





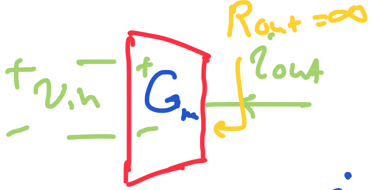


① diff input

② $A = \frac{V_{out}}{v_{in}}$ voltage gain

③ $A \gg 1$

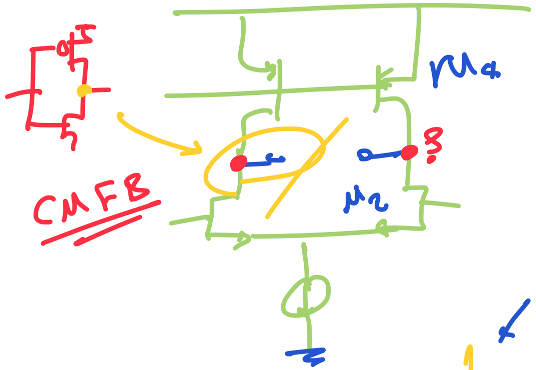
OTA



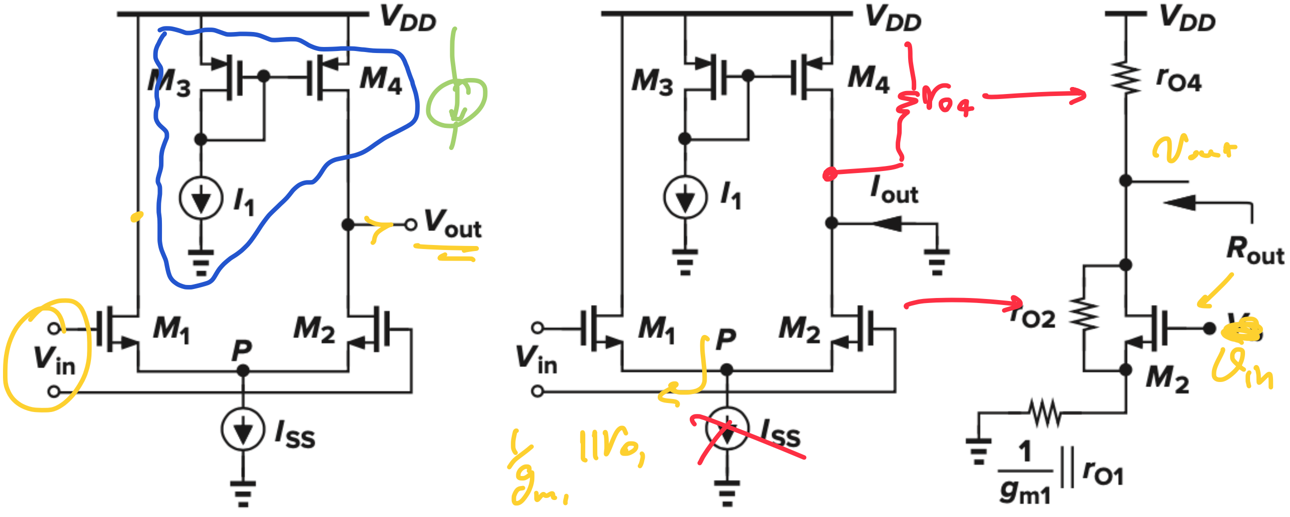
$G_m = \frac{i_{out}}{v_{in}}$

- A five-transistor "operational transconductance amplifier" (OTA).
- Note that the output is single-ended, hence the circuit is sometimes used to convert differential signals to a single-ended output.

Diff Pair + Active Mirror Load



$g_m (r_{o2} \| r_{o4}) \times \frac{1}{2}$

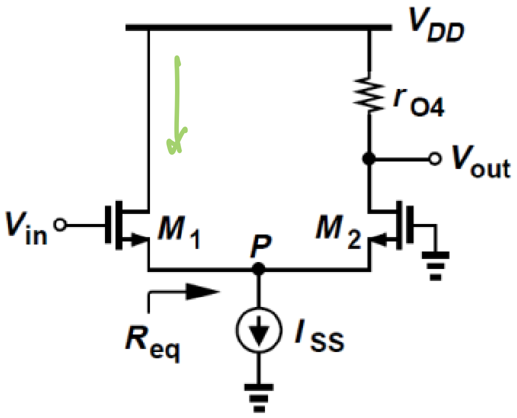


(a) (b) (c)

- We may simply discard one output of a differential pair as shown above
- What is the small-signal gain?

$A_v = \frac{V_{out}}{V_{in}}$ no symmetry $\longrightarrow$ $|A_v| = \frac{g_{m1}}{2}[(2r_{O2}) \| r_{O4}]$

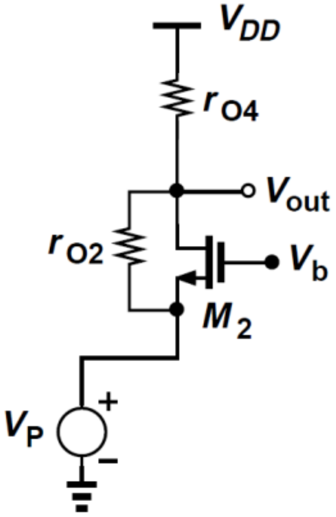
Second Approach



- We calculate Vp /Vin and Vout/Vp

$$\frac{V_P}{V_{in}} = \frac{R_{eq}||r_{O1}}{R_{eq}||r_{O1} + \frac{1}{g_{m1}}} \qquad R_{eq} = \frac{r_{O2} + r_{O4}}{1 + g_{m2}r_{O2}}$$

$$\frac{V_P}{V_{in}} = \frac{g_{m1}r_{O1}(r_{O2} + r_{O4})}{(1 + g_{m1}r_{O1})(r_{O2} + r_{O4}) + (1 + g_{m2}r_{O2})r_{O1}}$$



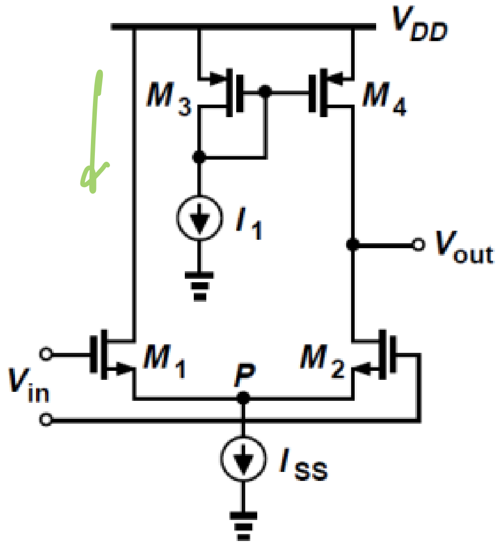
- Calculate Vout/Vp

$$\frac{V_{out}}{V_P} = \frac{(1 + g_{m2}r_{O2})r_{O4}}{r_{O2} + r_{O4}}$$

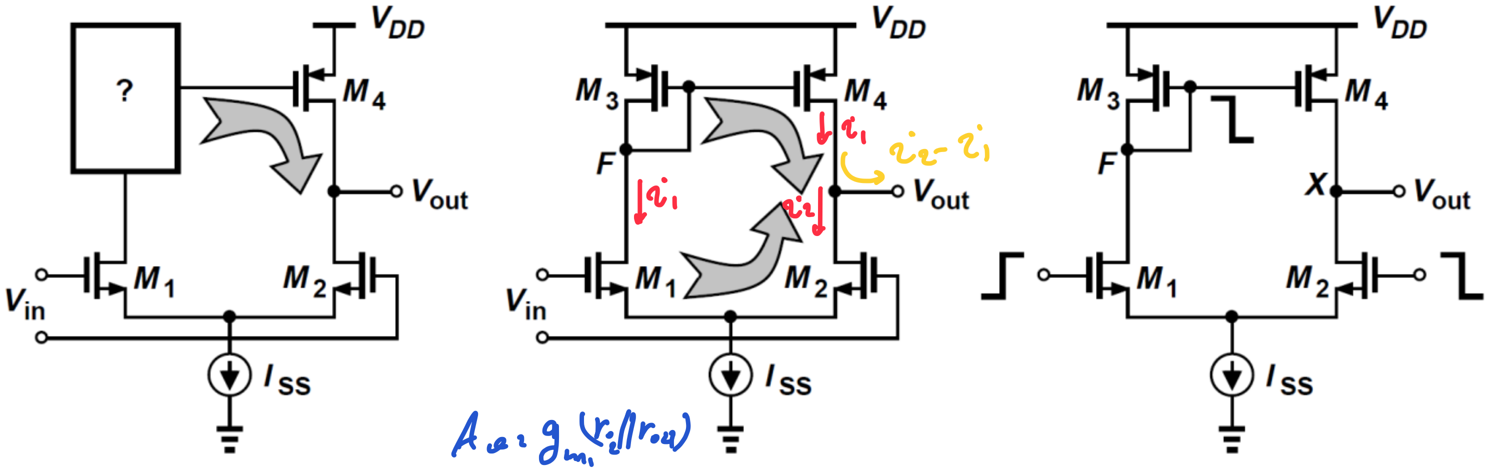
$$\frac{V_{out}}{V_{in}} = \frac{g_{m2}r_{O2}r_{O4}}{2r_{O2} + r_{O4}}$$

$$= \frac{g_{m2}}{2}[\underbrace{(2r_{O2})||r_{O4}}_{R_{out}}]$$

Differential Pair with Active Load

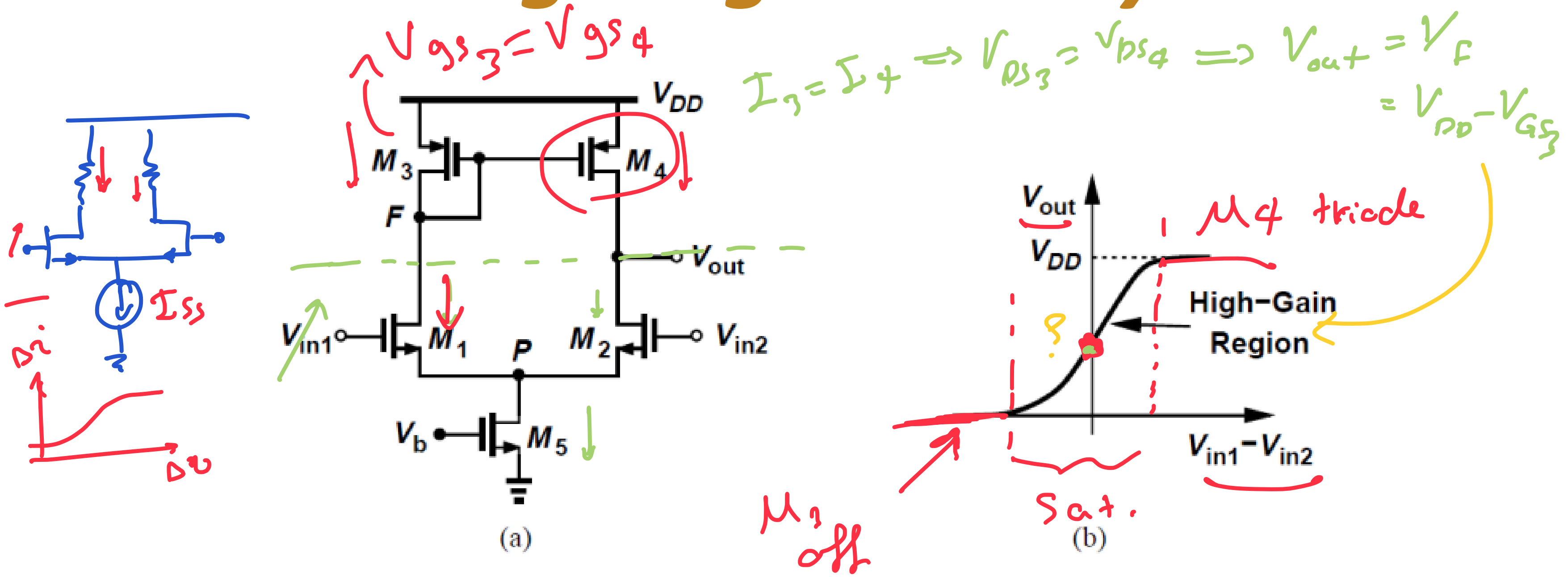


- The small-signal drain current of M1 is "wasted."
- It is desirable to utilize this current with proper polarity at the output.
- This can be accomplished by the five-transistor OTA, M3 enhances the gain.
- The five-transistor OTA is also called a differential pair with active load.



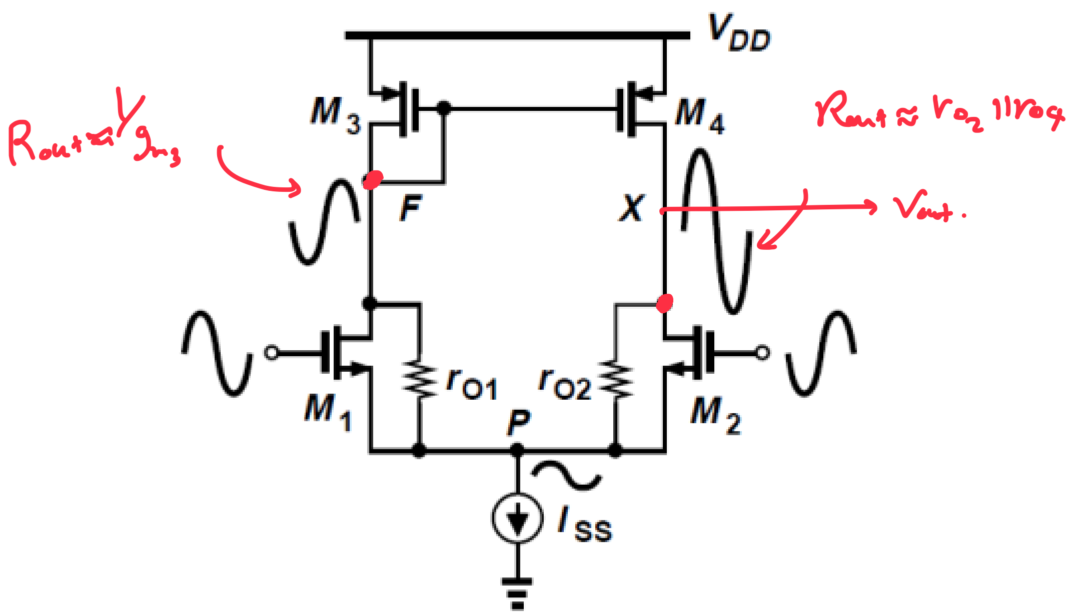
(a) (b) (c)

Large-Signal Analysis



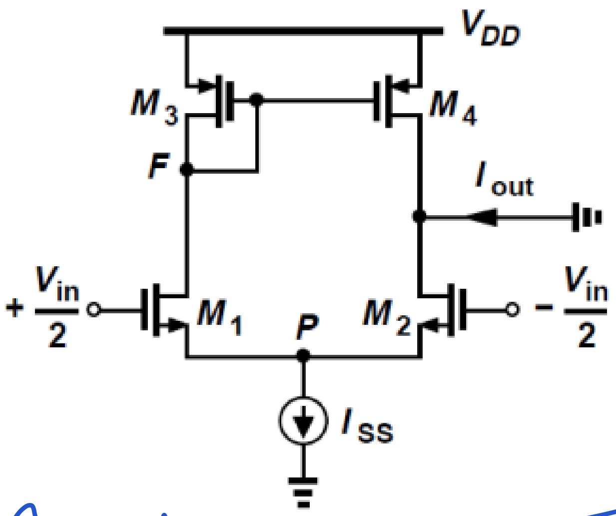
- If V_{in1} is much more negative than V_{in2}, $V_{out} = 0$.
- As V_{in1} approaches V_{in2}, the output voltage then depends on the difference between I_{D4} and I_{D2}. For a small difference between V_{in1} and V_{in2}, both M2 and M4 are saturated, providing a high gain.
- As V_{in1} becomes more positive than V_{in2}, allowing V_{out} to rise and eventually driving M4 into the triode region .

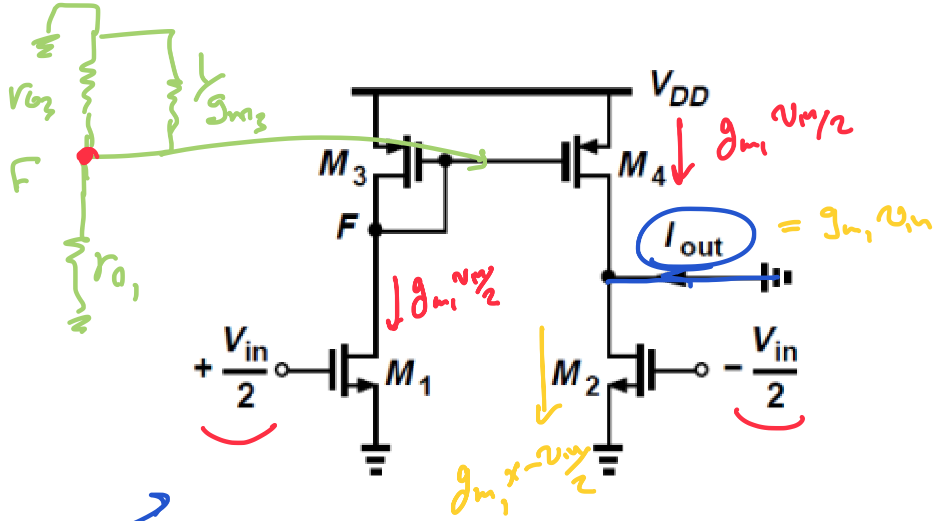
Small-Signal Analysis



- With small differential inputs, the voltage swings at nodes F and X are vastly different.
- The effects of V_F and V_X at node P (through r_{O1} and r_{O2}, respectively) do not cancel each other and this node cannot be considered a virtual ground.

Approximate Analysis





r_{o1} & r_{o2} large

half-circuit

- Node P can be approximated by a virtual ground.

$$I_{D1} = |I_{D3}| = |I_{D4}| = g_{m1,2} V_{in}/2$$

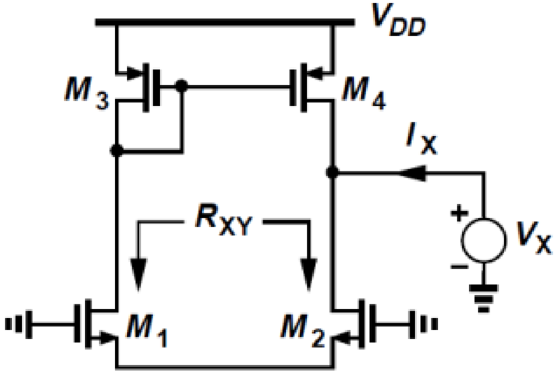
$$I_{D2} = -g_{m1,2} V_{in}/2$$

$$I_{out} = -g_{m1,2} V_{in}$$

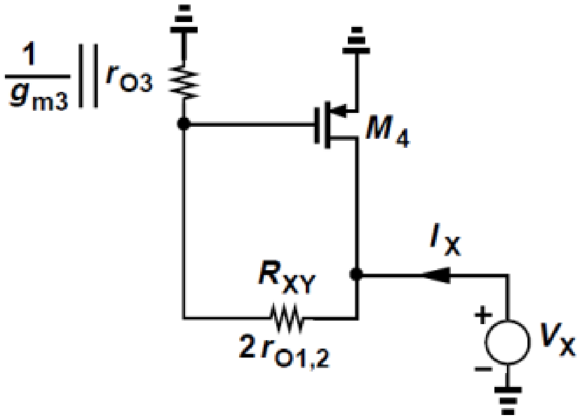
$$|G_m| = g_{m1,2}$$

$A_v \approx g_{m1,2} \times (r_{o2} \| r_{o4})$

Calculation of R_{out}



(a)



(b)

- Any current flowing intoM1 must flow out of M2, and the role of the two transistors can be represented by a resistor $R_{XY} = 2r_{O1,2}$
- The current drawn from V_X by R_{XY} is mirrored byM3 ontoM4 with unity gain.

$$I_X = \frac{V_X}{2r_{O1,2} + \frac{1}{g_{m3}}||r_{O3}}\left[1 + \left(\frac{1}{g_{m3}}||r_{O3}\right)g_{m4}\right] + \frac{V_X}{r_{O4}}$$

- For $2r_{O1,2} \gg (1/g_{m3})\|r_{O3}$

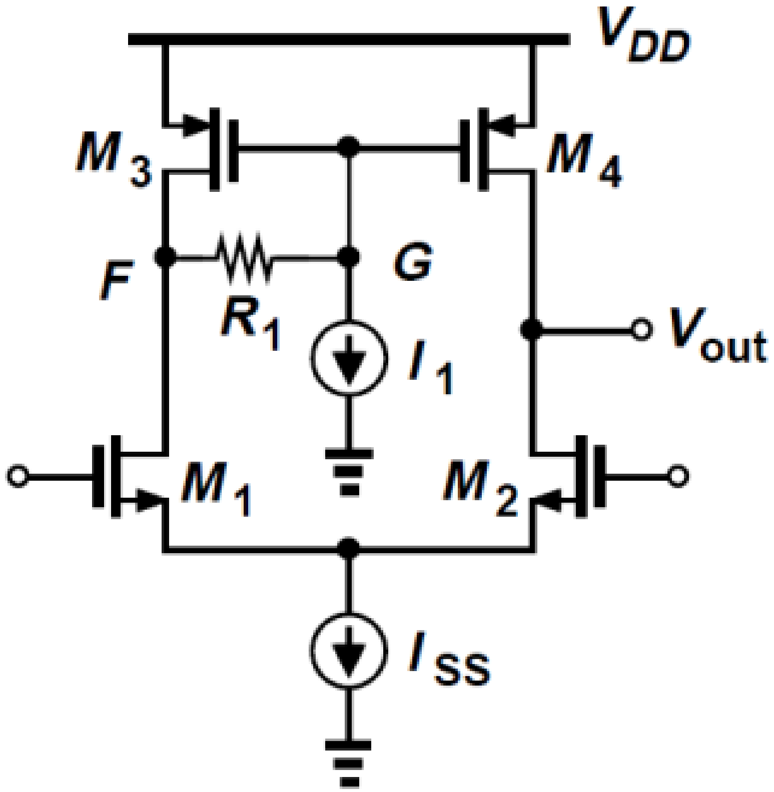
$$R_{out} \approx r_{O2}\|r_{O4}$$

Headroom Issues

- The five-transistor OTA does not easily lend itself to low-voltage operation.
- The value of I_1 must be much less than Iss/2 and
- Insert a resistor in series with the gate and draw a constant current from it.

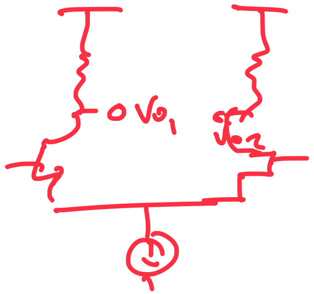
$$R_1 I_1 \leq V_{TH3}$$

- Now V_F can be larger than V_G



$V_{out} = V_{DD} - V_{GS_{3,4}}$

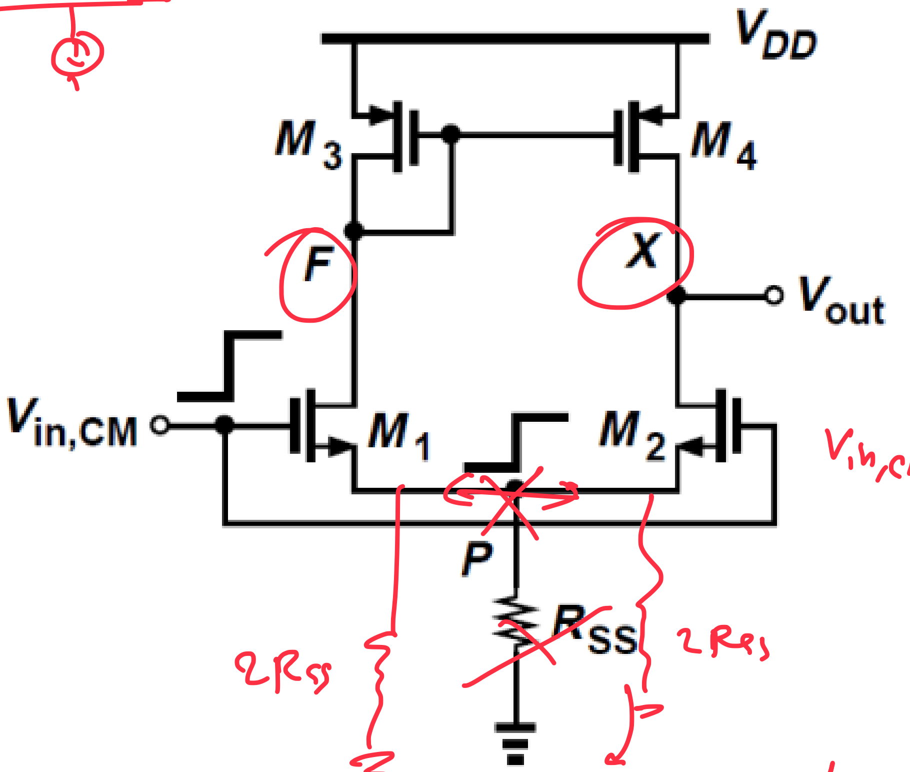
Common-Mode Properties



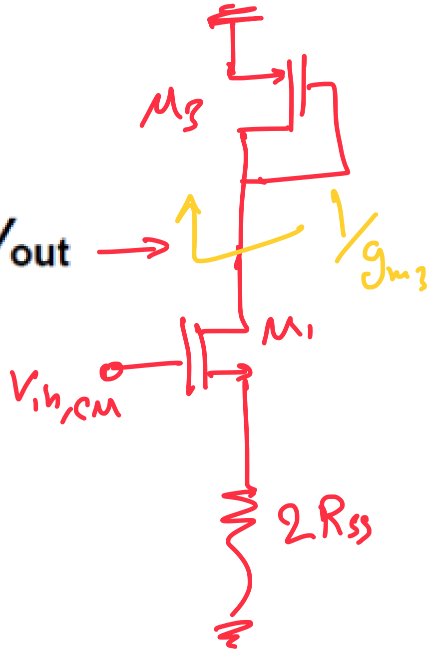
$v_{o1} - v_{o2} = v_{d,out}$

$\frac{v_{d,out}}{v_{in,CM}} = 0$

$\frac{v_{o1}}{v_{in,CM}} = \frac{-g_m R_D}{1 + g_m \times 2R_{SS}}$



output impedance of M5



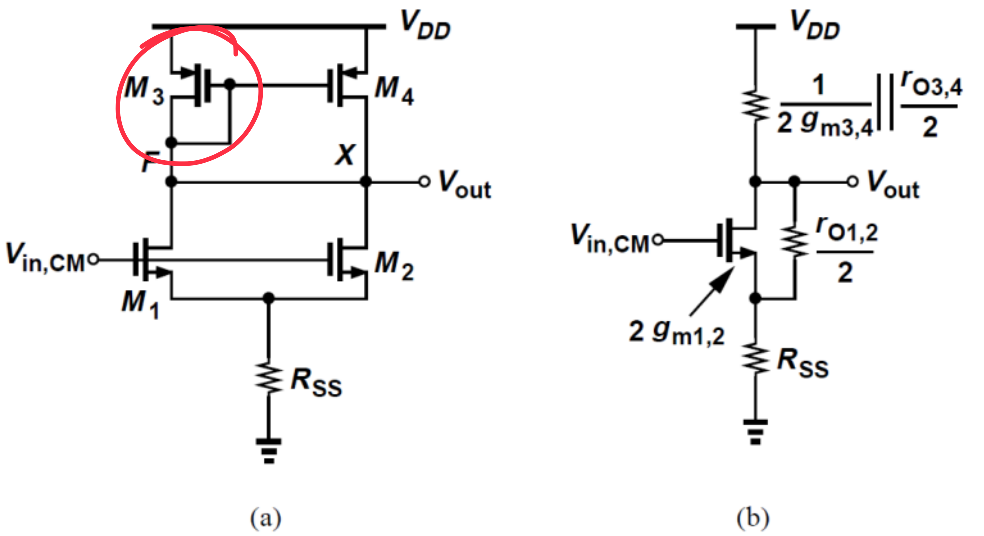
$$A_{CM} = \frac{\Delta V_{out}}{\Delta V_{in,CM}}$$

$$A_{CM} \approx \frac{-\frac{1}{2g_{m3,4}} \Big\| \frac{r_{O3,4}}{2}}{\frac{1}{2g_{m1,2}} + R_{SS}}$$

$$= \frac{-1}{1 + 2g_{m1,2}R_{SS}} \frac{g_{m1,2}}{g_{m3,4}}$$

$$A_{CM} = \frac{-g_{m1} \times \frac{1}{g_{m3}}}{1 + g_{m1} \times 2R_{SS}}$$

CMRR

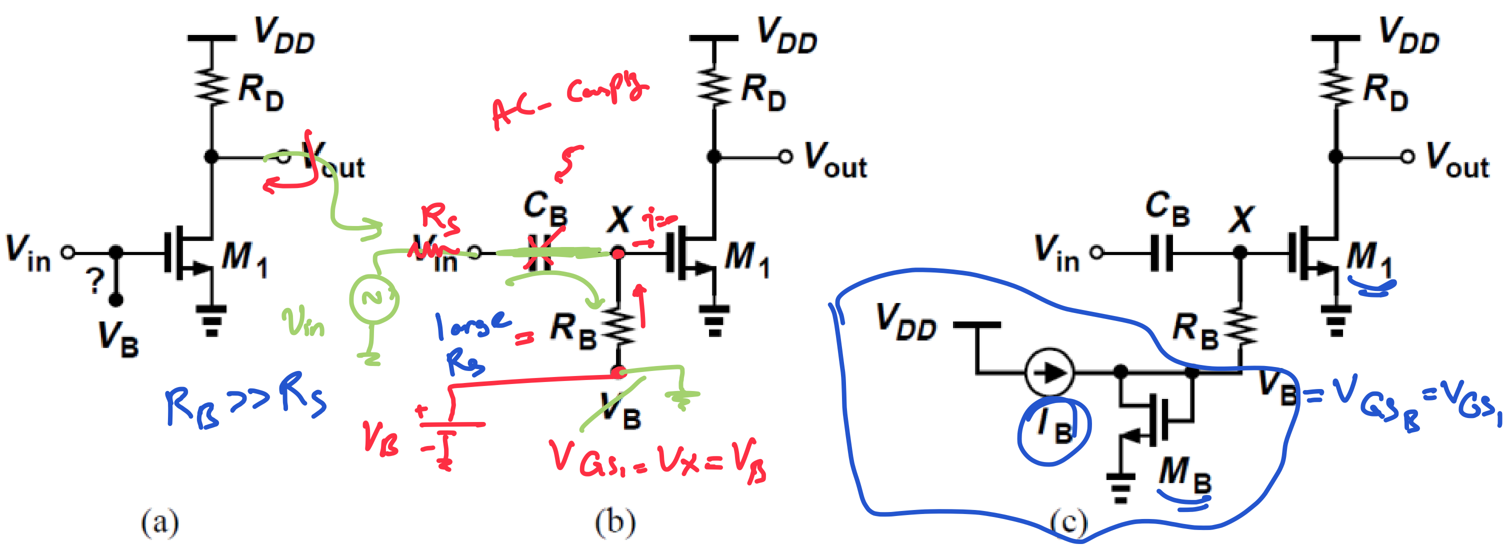


(a) Simplified circuit of Fig. 5.37, (b) equivalent circuit of (a).

$$\text{CMRR} = \left|\frac{A_{DM}}{A_{CM}}\right|$$
$$= g_{m1,2}(r_{O1,2}\|r_{O3,4})\frac{g_{m3,4}(1+2g_{m1,2}R_{SS})}{g_{m1,2}}$$
$$= (1+2g_{m1,2}R_{SS})g_{m3,4}(r_{O1,2}\|r_{O3,4})$$

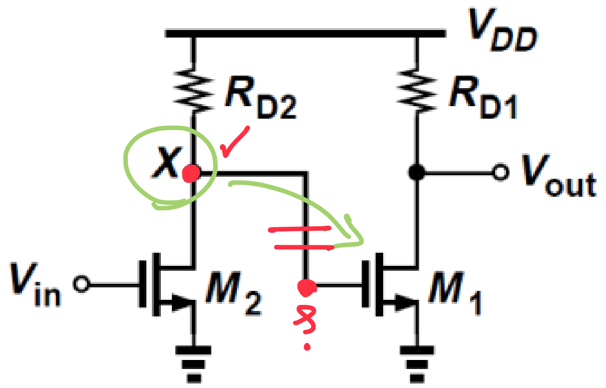
- Even with perfect symmetry, the output signal is corrupted by input CM variations.

Biasing Techniques



- Simple CS Stage
  - How do we ensure that V_B does not "fight" Vin?
- Couple V_{in} capacitively and establish a high impedance for V_B.
- Node X in Fig (b) must have a dc path to a voltage.
- The bias voltage must be generated by a diode-connected device
- Typically select I_B about one-tenth to one-fifth of I_{D1} so as to minimize the power.

Direct Coupling



Direct coupling between two stages.

- Possible to remove the input coupling capacitor and provide the bias voltage from the preceding stage?
- The bias conditions of M1 are influenced by those of M2.
- The PVT variations are amplified.
- One can employ direct coupling between two stages if each has a low gain.