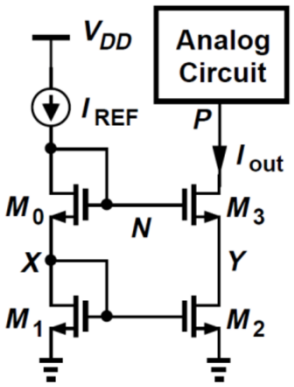
EE 332 Circuits and Devices II Autumn 2022

Homework6 Due: Nov. 18 (11:59pm)

In this HW assume: VDD=1.5V, $Vth_{n,p}$=0.3V, $\mu_n C_{ox} = \frac{500\mu A}{V^2}$, $\mu_n = 2\mu_p$, $\lambda_p = 0.2V^{-1}$, $\lambda_n = 0.1V^{-1}$, and $\gamma = 0$ for both NMOS and PMOS devices.

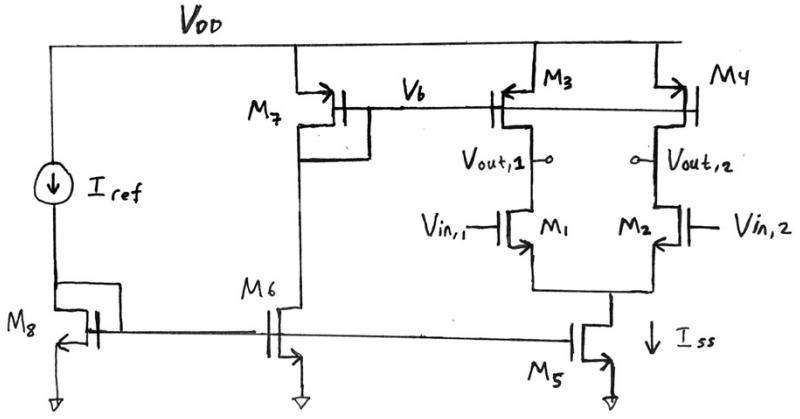
1. For the cascode current-mirror shown below:



a) Find minimum output voltage (Vp) for the current mirror to work.
b) Find output resistance of this current mirror (the resistance looking in from point P).
c) If we need to generate a 1mA output current from a 0.1mA reference current, what should be the W/L ratios for $M_{1,2}$ and $M_{0,3}$? (As in, find $\frac{(W/L)_2}{(W/L)_1}$ and $\frac{(W/L)_3}{(W/L)_0}$)
d) To have a minimum working output voltage of 0.5V, what should be the W/L values? Assume V_{od} is the same for $M_{0\text{-}3}$.
e) To implement I_{ref} in an easy way we will replace the I_{ref} ideal current source with a resistor. What should be the value of the resistor to provide 0.1mA reference current?

2. For the differential amplifier shown below:

a) Explain the role of $M_{3,4}$ and M_7.
b) If $I_{ref}/I_{ss} = 0.2$, $(W/L)_{7,8} = 50$, choose W/L of $M_{3\text{-}7}$ to bias the circuit. (You can pick the current flowing through $M_{6,7}$ as you want). The different W/L ratios do not have to be the same for the different transistors.
c) For I_{ref} = 125uA and $W/L_{1,2} = 125$, find the peak-to-peak single-ended output swing.
d) Find the input CM range (the range of the input voltage DC bias).
e) Determine the output nodes' common-mode voltage.



3. Consider the 5-Transistor OTA shown here and assume the current in the M_5 current tail will be 1mA.

a) Find W/L of $M_{1,2}$ to have a differential gain of 20.
b) Assuming $V_{od3,4}$=0.2V, find W/L of $M_{3,4}$.
c) Find minimum and maximum output swing levels.
d) Find the output DC bias and the maximum output swing.
e) Find M_5's output resistance and the OTA's CMRR.