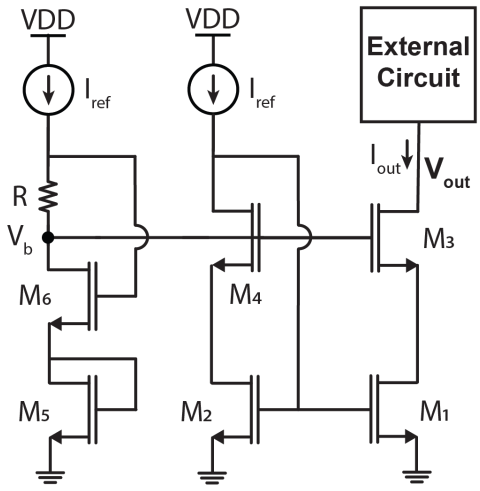
EE 332 Circuits and Devices II Autumn 2021
Final Exam Date: Dec. 14 (8:30-10:20am)

Full Name: ……. **Grade:** …… /100
SID : …….

Assume for all the problems: L=65nm, VDD=1.2V, $|Vth_{n,p}|$=0.3V, $\mu_n C_{ox} = \frac{0.5mA}{V^2}$, $\mu_n = 2\mu_p$, $\lambda_p = \lambda_n = 0.1V^{-1}$, $\gamma = 0$ for both NMOS and PMOS devices, and $V_{od}=V_{GS}-V_{th}$.

1. (25 pts) For the current mirror shown below assume: $I_{Ref} = 100\mu A$ and ***all transistors have the V_{od} of 0.2V***.



a) What should be the ratio of $(W/L)_1/(W/L)_2$ to provide an I_{out} of 1mA?

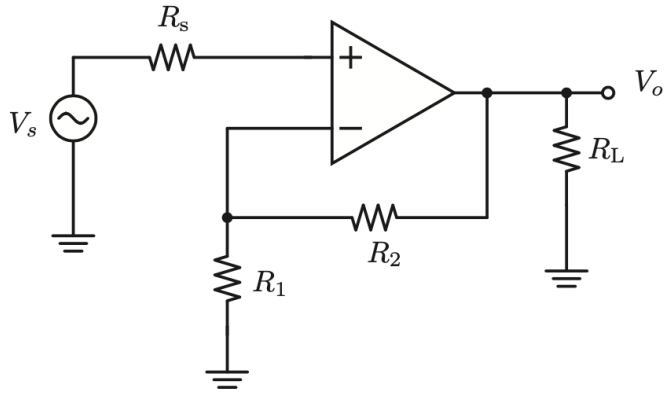
b) What is the minimum V_{out} (as a function of V_b) ? What can be the minimum V_b value to make sure all devices remain in saturation? Given this V_b value, what would be the minimum acceptable V_{out}?

c) What should be the value of R to ensure V_b will be at the optimal value from part b?

d) If there will be a fabrication error of 20% increase in the value of the resistor R, will the current mirror be still functional? Why?

2. (35 pts) An op-amp is configured to provide gain (V_O/V_S) of 5V/V to a $R_L = 1k\Omega$ load. Model the op-amp with the following parameters:

- $R_{in} = \infty$ (ideal)
- $R_{out} = 0$ (ideal)
- $A_0 = 100$ (not infinite)
- $f_0 = 10MHz$ (not ideal: finite 3dB-bandwidth frequency)



a) What should be the ratio of R_2/R_1 to achieve the target close-loop gain assuming amplifier has an infinite gain.

b) How does the closed-loop gain change if R_s or R_L changes?

c) What's the gain error due to the non-infinite gain of amplifier?

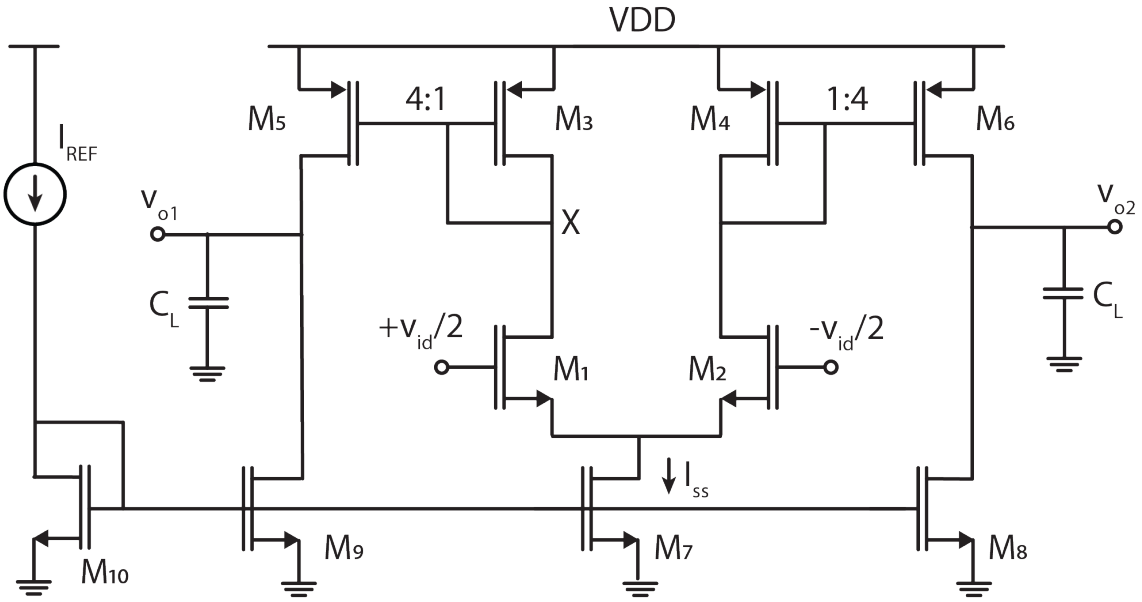
d) What's the approximate 3dB bandwidth? *Hint*: You do not need to derive this result but simply state it from what you know about feedback amplifiers.

e) What's the unity-gain bandwidth for the closed-loop amplifier?

f) Plot the magnitude Bode plot for closed-loop gain.

g) if R_{out} of OpAmp is non-zero with a value of 100Ω, calculate the output impedance assuming no loading effect R_1 & R_2.

3. (40 pts) For the fully differential amplifier shown below **<u>all transistors</u>** have the nominal channel length of **65nm** and should be biased such that $\mathbf{V_{od}}$ **= 0.2V**:



$$C_L = 1pF, I_{Ref} = 100\mu A$$

a) For I_{ss} to be 2mA, Find W for $M_{7\text{-}10}$ transistors.

b) Find W for $M_{3\text{-}6}$ transistors.

c) Draw the half-circuit model for differential mode.

d) Find the small-signal differential gain (V_{out}/V_{id}), where $V_{out}=V_{o1}-V_{o2}$.

e) What's the output differential peak-to-peak output swing?

f) Estimate output node pole (ω_{out}) location (ignore all other parasitics)

g) If $M_{3\text{-}6}$ have $C_{GS} = C_{GD} = 1fF/\mu m$ (per μm unit width), estimate the mirror pole location at node X (ω_X) using the Miller approximation and node-pole associations method. (ignore all other parasitic capacitances)

h) Assuming that first pole is dominant in this amplifier, what is the unity-gain bandwidth (ω_u)?