EE 332: Devices and Circuits II

Lecture 2: MOS Devices (Part 2)

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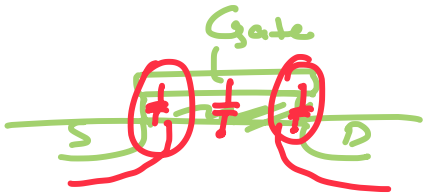
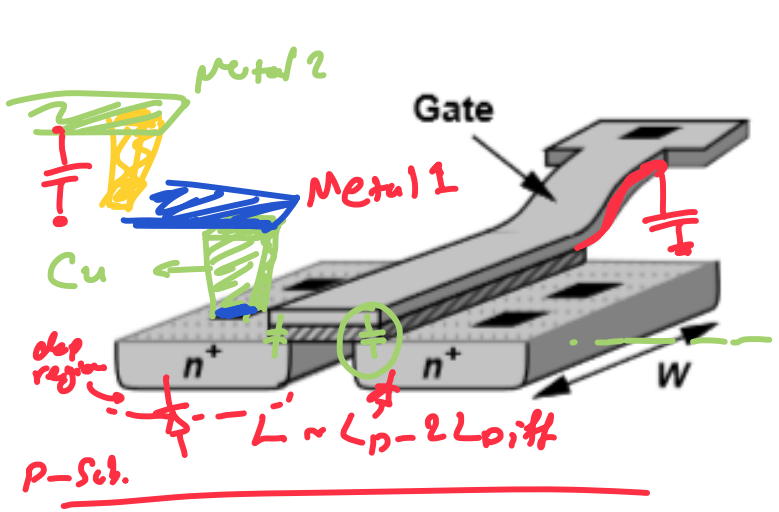
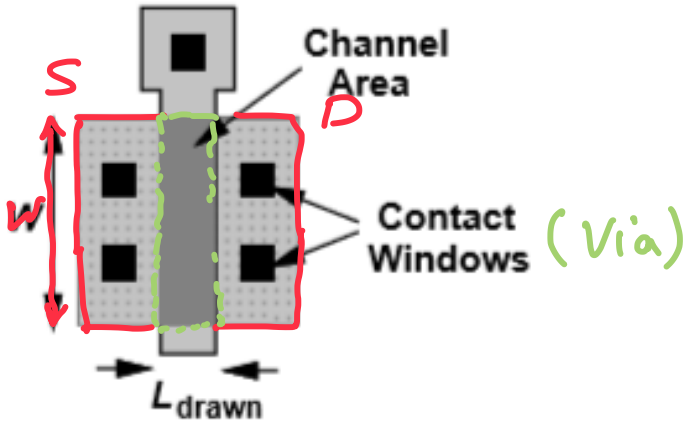
MOS Device Layout

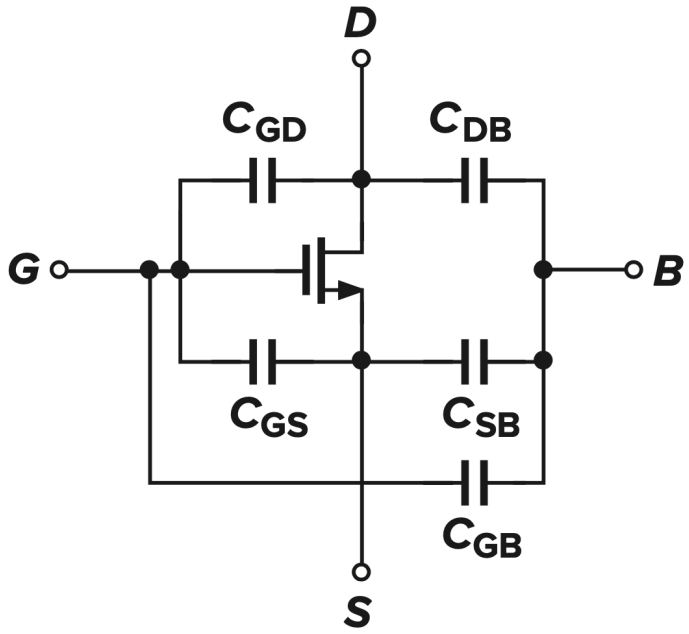






- The gate polysilicon and the source and drain terminals must be tied to metal (aluminum) wires that serve as interconnects with low resistance and capacitance.
- This is accomplished with “contact windows” which are filled with metal and connected to the upper metal wires.
- To minimize the capacitance of the source and drain, the total area of each junction must be minimized.

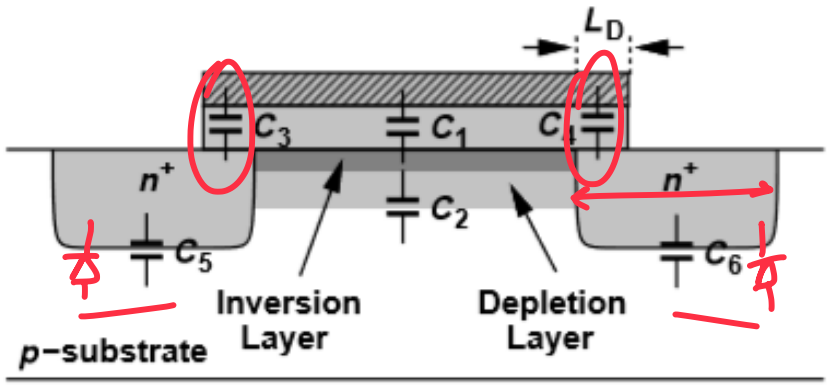
MOS Device Capacitances

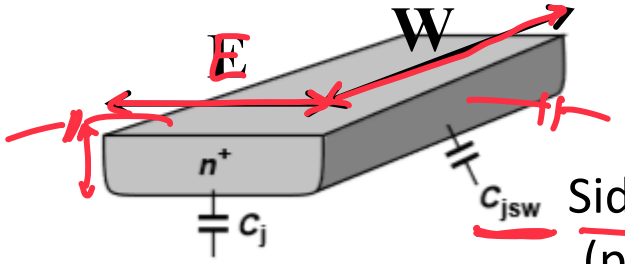


- To better predict high-frequency behavior, it is necessary to consider device capacitances.
- Capacitance exists between every two of the four terminals, and their values depend on the bias conditions of the transistor.

MOS Device Capacitances

2E+2W





Sidewall Cap (per length)

Bottom-plate Cap (per area)

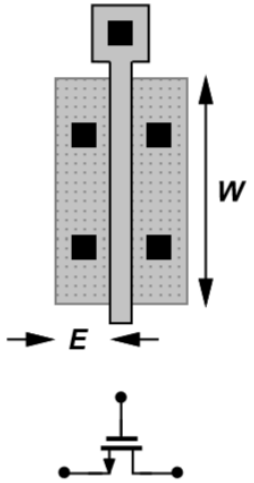
$$C_j = C_{j0}/[1+V_R/(\Phi_B)]^m,$$

$$C_1 = WLC_{ox} \qquad C_2 = WL\sqrt{q\epsilon_{si}N_{sub}/(4\Phi_F)}$$

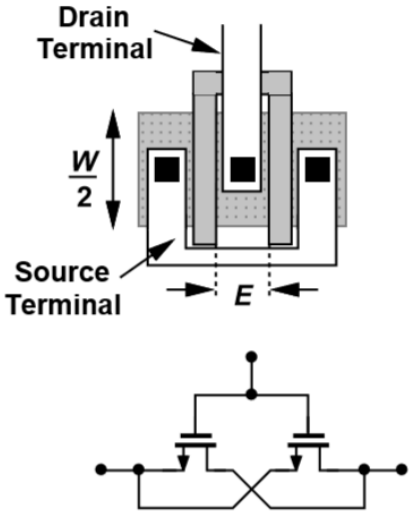
- Capacitances include
  - Oxide capacitance between the gate and the channel C_1.
  - Depletion capacitance between the channel and the substrate C_2.
  - Overlap capacitance between the gate & source/drain (C_3 and C_4).
  - Junction capacitance between the source/drain areas and the substrate C_5 and C_6.

MOS Device Capacitances (C_{DB}, C_{SB})

One "Finger"



Two "Fingers"



- For example calculating the source and drain junction capacitance of the topology on the left,

$$C_{DB} = C_{SB} = WEC_j + 2(W+E)C_{jsw}.$$

- We assumed the total source/drain perimeter 2(W+E) is multiplied by C_{jsw}.

- Calculating the source and drain junction capacitance of the second topology on the left,

$$C_{DB} = \frac{W}{2}EC_j + 2\left(\frac{W}{2}+E\right)C_{jsw} \quad < C_{DB}\ \text{one finger}$$

$$C_{SB} = 2\left[\frac{W}{2}EC_j + 2\left(\frac{W}{2}+E\right)C_{jsw}\right]$$

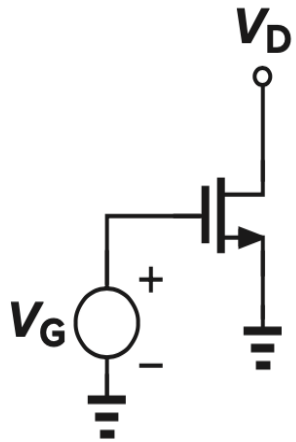
$$= WEC_j + 2(W+2E)C_{jsw}. \quad > C_{SB}\ \text{one-finger}$$

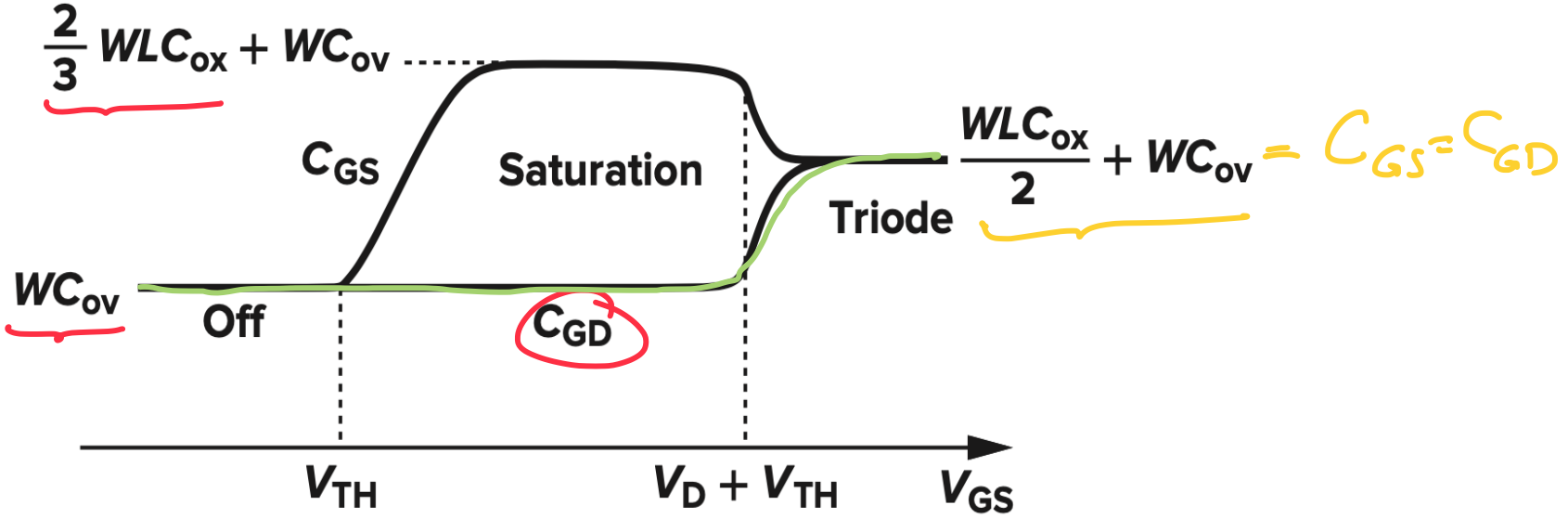
MOS Device Capacitances (C_{GS}, C_{GD})

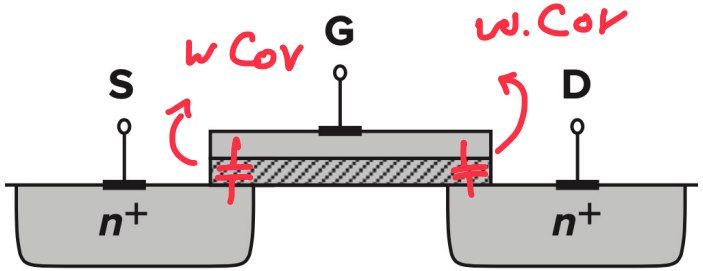
Example

$C_{GS} = 0.1\,fF/\mu m$

W



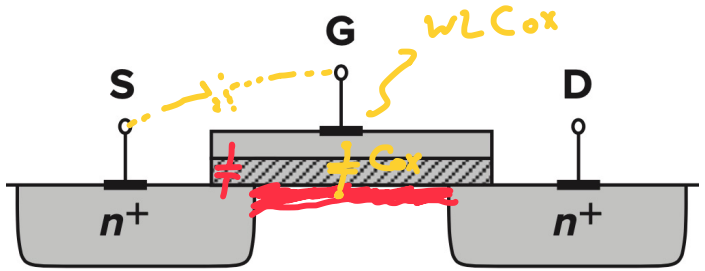




W Cov

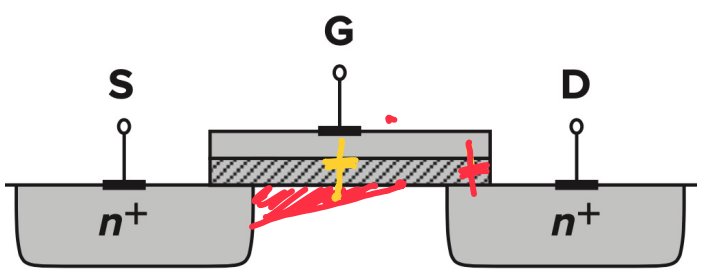
W.Cov

off



WLCox

Triode

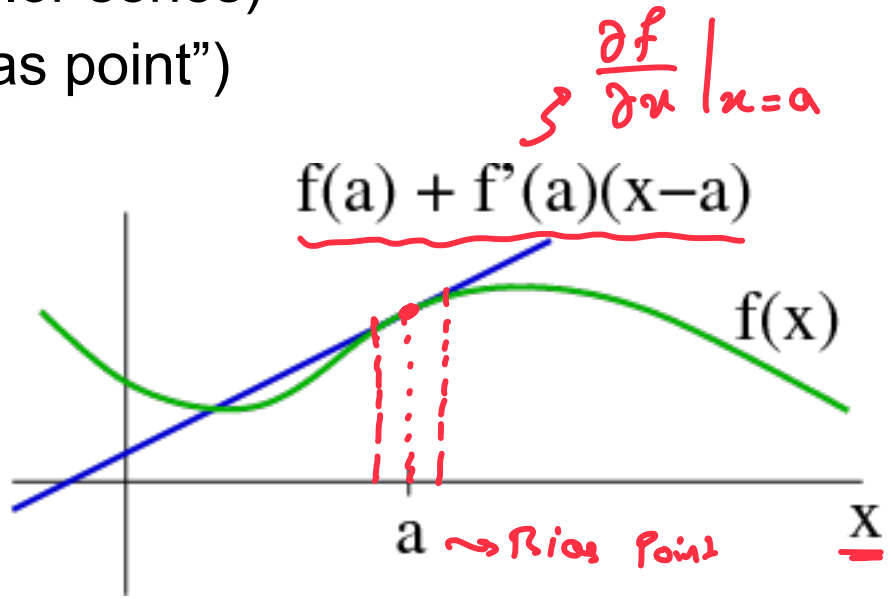


Sat.

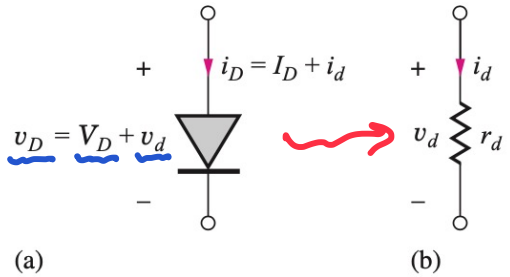
Small-signal (SS) Modeling

- Linear modeling (for AC analysis, etc.)
  - Easier to analyze circuit behavior
  - Using RLC, and voltage & current sources mapping, we can model/solve any circuit

- Linearizing a non-linear function (e.g., 1st-order Taylor series)
  - SS model depends on the operating point ("Bias point")



SS Modeling Example: Diode



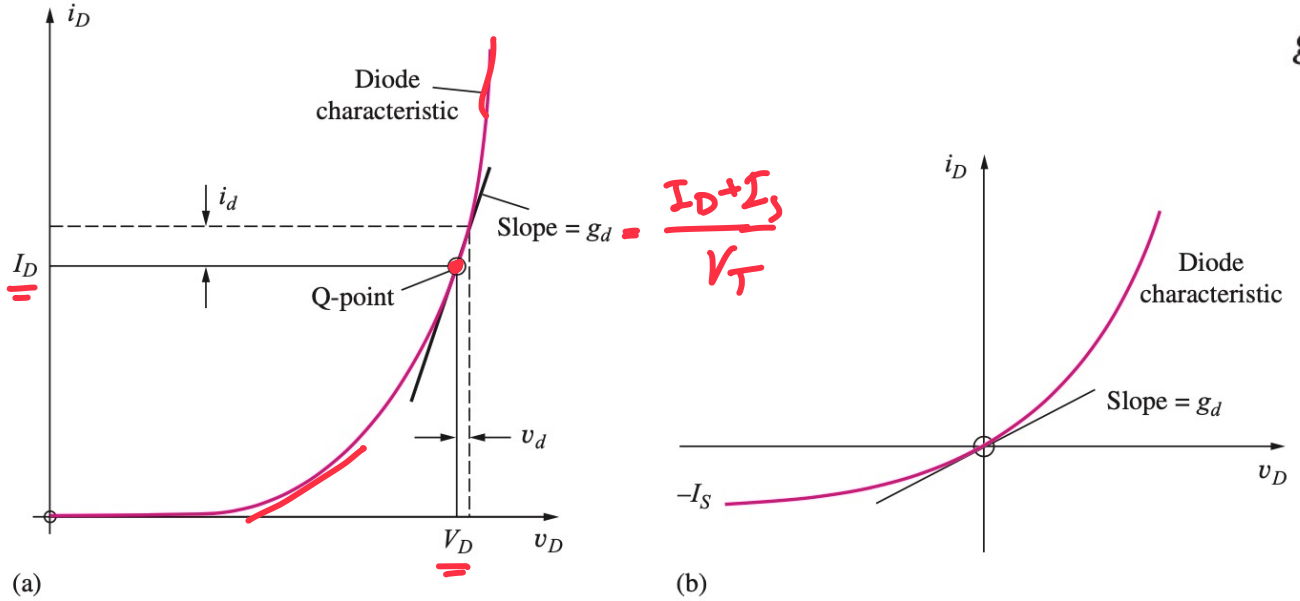
$$r_d = \frac{1}{g_d} = \frac{V_T}{I_D + I_S}$$

$$I_D = I_S\left(e^{V_D/V_T} - 1\right)$$

$$i_c = I_s\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right]$$

$$i_c = g_m v_{be}$$

Figure 13.8 (a) Total diode terminal voltage and current. (b) Small signal model for the divide.



$$g_d = \left.\frac{\partial i_D}{\partial v_D}\right|_{\text{Q-point}} = \left.\frac{\partial}{\partial v_D}\left\{I_S\left[\exp\left(\frac{v_D}{V_T}\right) - 1\right]\right\}\right|_{\text{Q-point}}$$

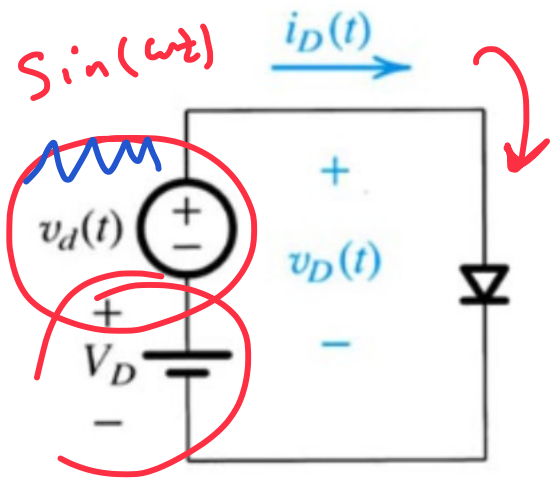
$$= \frac{I_S}{V_T}\exp\left(\frac{V_D}{V_T}\right) = \frac{I_D + I_S}{V_T}$$

$I_D + I_S$ / V_T

* V_T = Constant ($\frac{kT}{q}$)

Figure 13.9 (a) The relationship between small increases in voltage and current above the diode operating point (I_D, V_D). For small changes $i_d = g_d v_d$. (b) The diode conductance is not zero for $I_D = 0$.

Bias Point



$i_D(t) = ?$

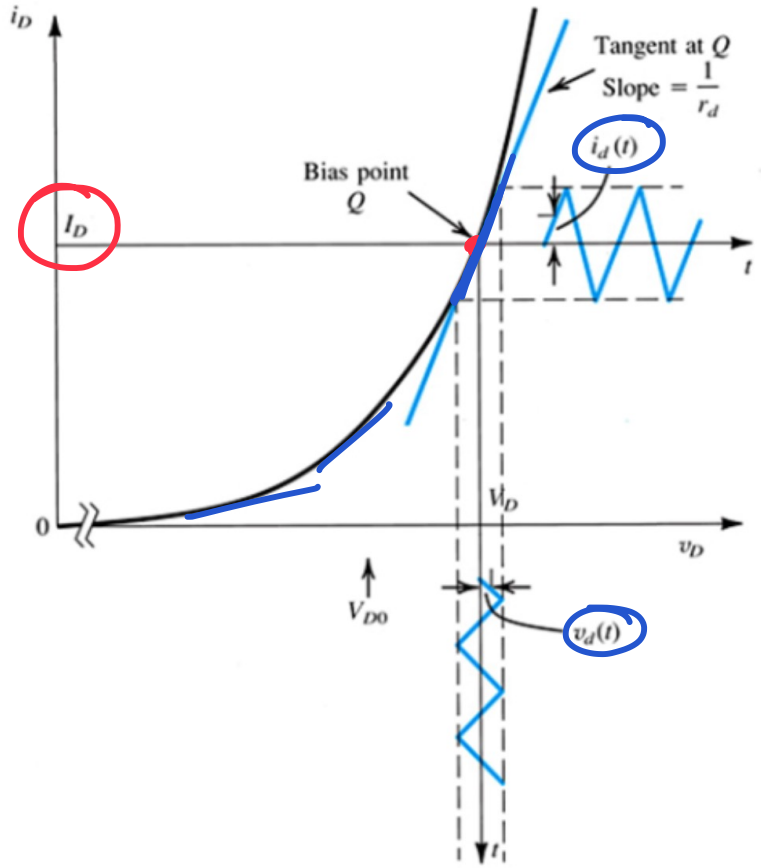
$= I_D + i_d(t)$

Bias Current

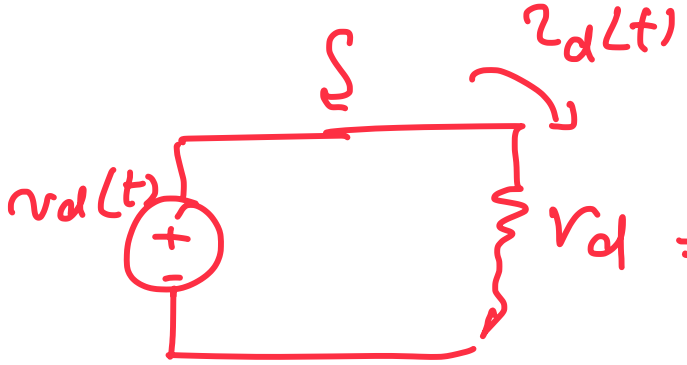
S.S Current.

Solve the exp Equ.

$= I_D + \frac{v_d(t)}{r_d}$



$|v_d(t)| \ll V_D$

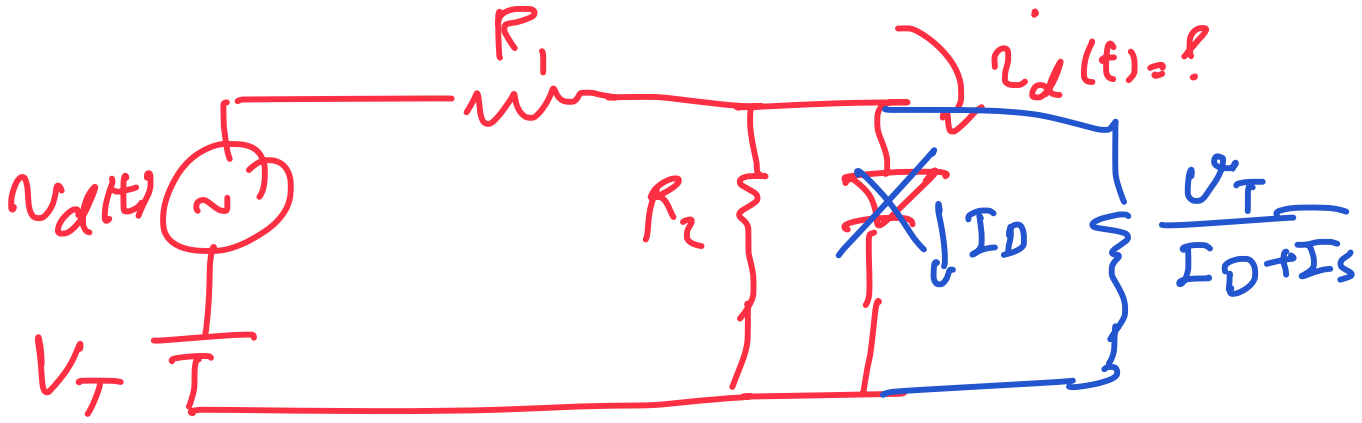


$r_d = \frac{V_T}{I_D + I_S}$

Small-signal Modeling

- For more complicated circuits (e.g., multiple devices), you can generate the SS model by either:
  1. Calculate the overall I-V -> Linearize by taking the derivative
  2. Replace each non-linear component with its SS model and then calculate the overall circuit model

Linear Model

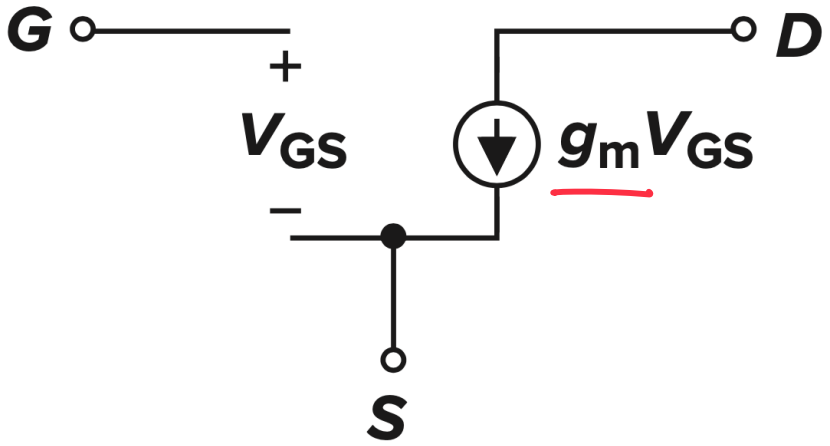


① Bias Point → I_D

② use S.S model

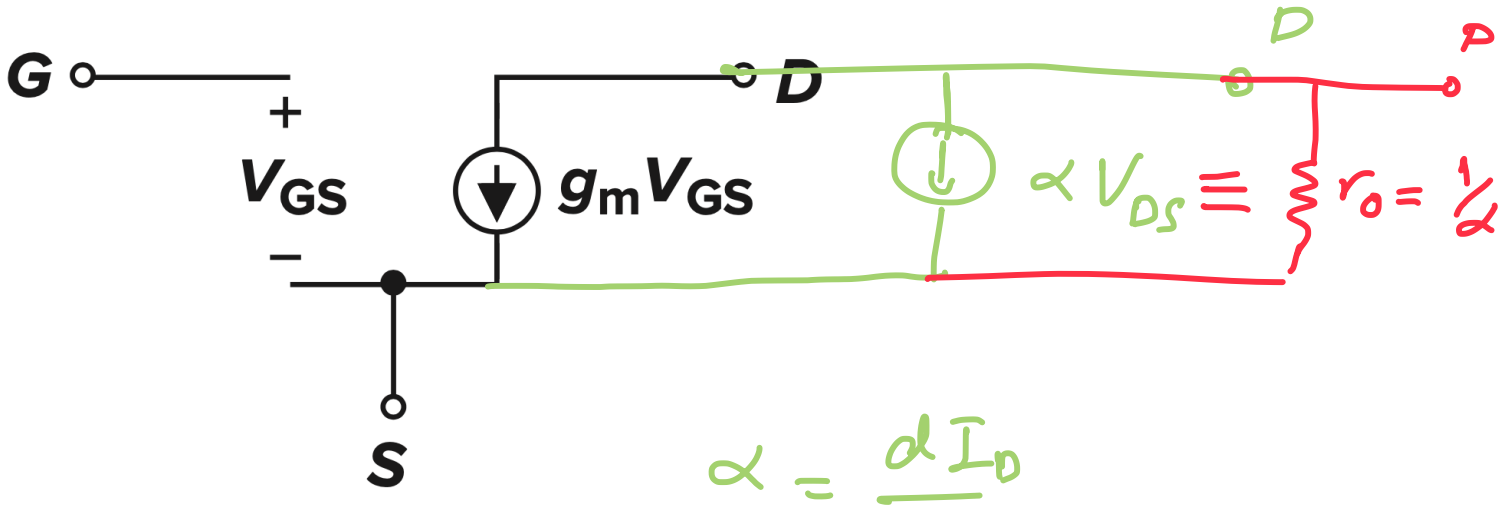
③ S.S V/I

MOS Small-Signal Model



- If perturbation in bias conditions are small, a “small-signal” model can be used to simplify calculations (derived for saturation region).
- In order to derive the small-signal model, we
  - Apply certain bias voltages to the terminals of the device.
  - Increment the potential difference between two of the terminals while the other terminal voltages remain constant.
  - Measure the resulting change in all terminal currents.

MOS Small-Signal Model



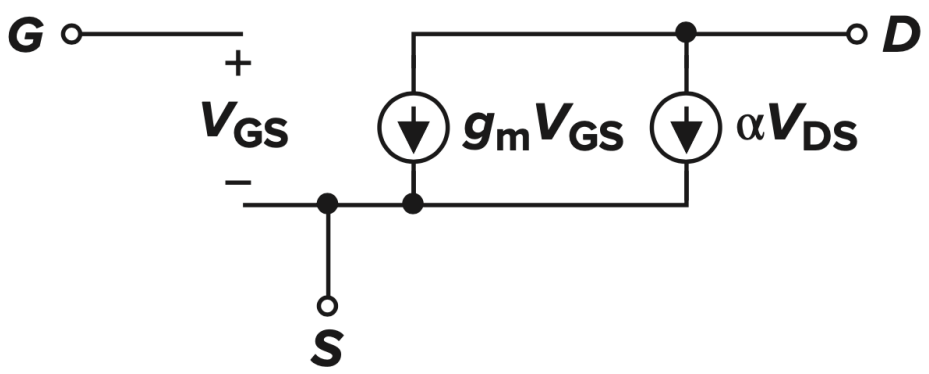
$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})$$

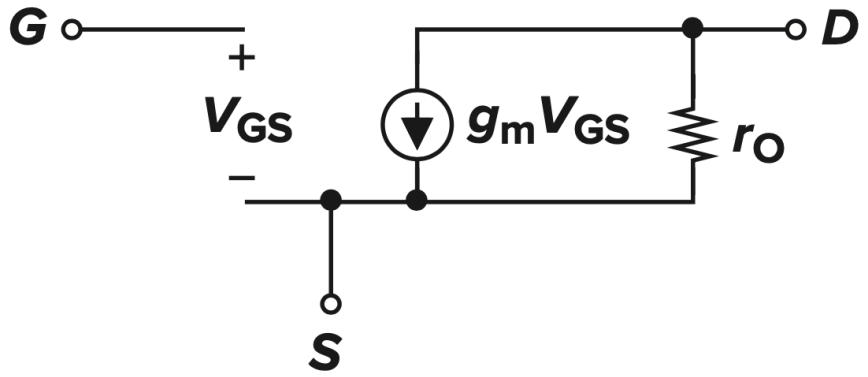
$$= \frac{2 I_D}{V_{GS} - V_{th}} = \frac{2 I_D}{V_{OD}}$$

$$\alpha = \frac{d I_D}{d V_{DS}}$$

- By changing the voltage between two terminals by $\Delta V = V_{GS}$ and then measuring a current change $\Delta I = g_m V_{GS}$, we can model the effect by a voltage-dependent current source.
- Above is the small-signal model of an ideal MOSFET.

MOS Small-Signal Model





- Due to channel-length modulation, drain current also varies with V_{DS} , but a current source whose value linearly depends on the voltage across it is equivalent to a linear resistor:

$$r_O = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\partial I_D / \partial V_{DS}} = \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2 \cdot \lambda}$$

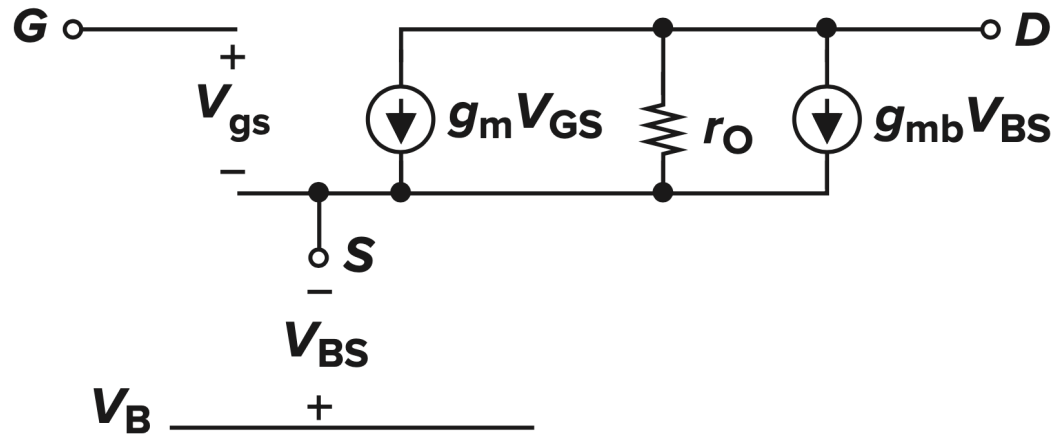
$$\approx \frac{1+\lambda V_{DS}}{\lambda I_D} \approx \frac{1}{\lambda I_D}$$

$\lambda V_{DS} \ll 1$

$\frac{I_D}{1+\lambda V_{DS}}$

- It is assumed that $\lambda V_{DS} \ll 1$.
- r_o limits the maximum voltage gain of most amplifiers.

MOS Small-Signal Model



- Due to body effect, bulk potential influences V_{TH} and hence gate-source overdrive.
- With all other terminals held at a constant voltage, the bulk behaves as a second gate since the drain current is a function of the bulk voltage given by $g_{mb}V_{BS}$, where

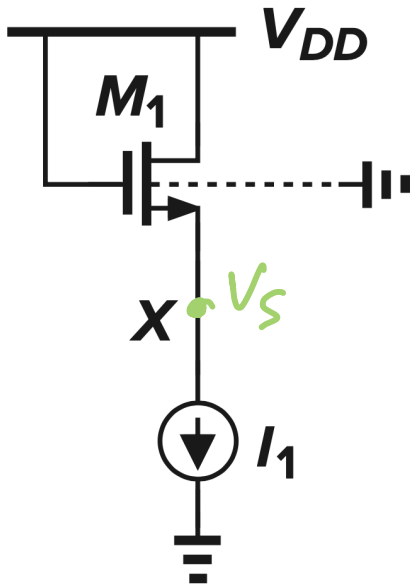
$\frac{\partial I_D}{\partial V_{TH}} \times \frac{\partial V_{TH}}{\partial V_{BS}}$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})\left(-\frac{\partial V_{TH}}{\partial V_{BS}}\right).$$

$$\frac{\partial V_{TH}}{\partial V_{BS}} = -\frac{\partial V_{TH}}{\partial V_{SB}} = -\frac{\gamma}{2}(2\Phi_F + V_{SB})^{-1/2}.$$

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} = \eta g_m, \quad \eta = g_{mb}/g_m .$$

MOS Small-Signal Model

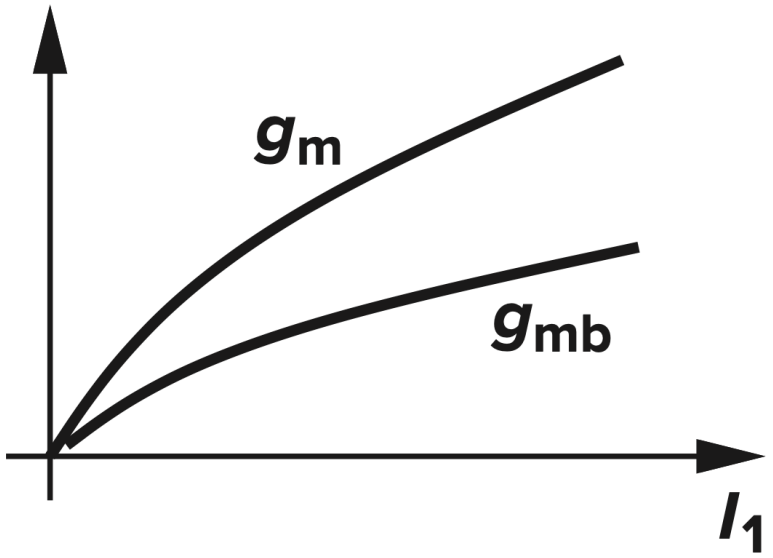


$\uparrow I_D \propto (\uparrow V_{GS} - V_{th})^2$

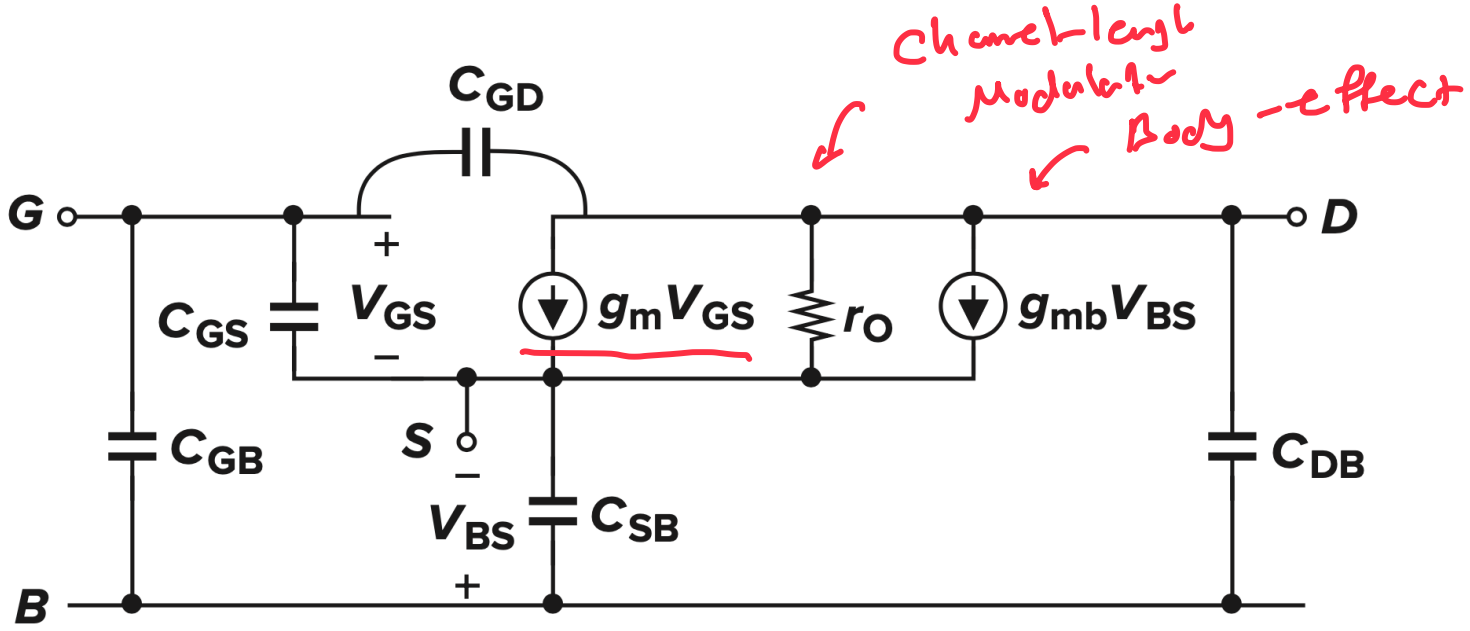
$\uparrow V_G - \downarrow V_S$

V_{DD}

- To sketch g_m and g_{mb} of M_1 on the left as a function of bias current I_1,
  - $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D} \Rightarrow g_m \propto \sqrt{I_1}$
  - g_{mb} dependence on I_1 is less straight forward, but as I_1 increases, V_X decreases and so does V_{SB}.

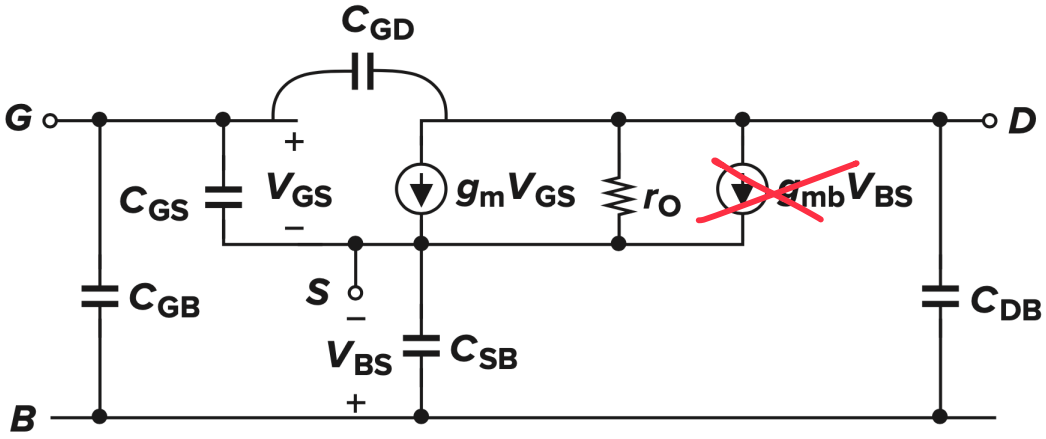


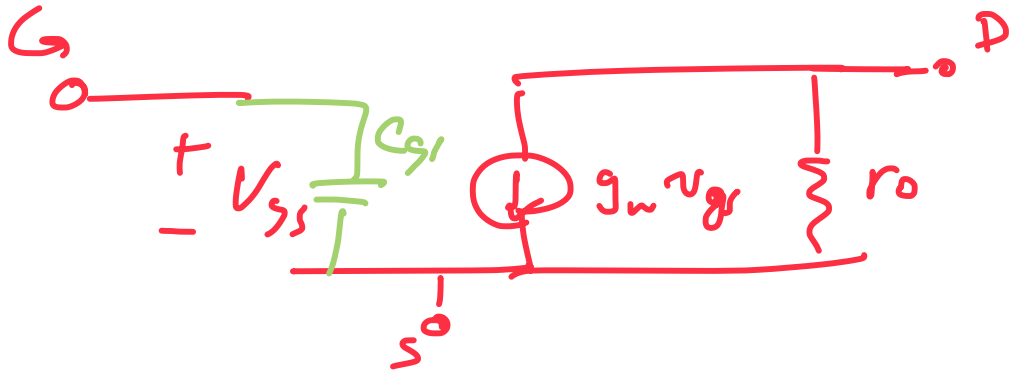
MOS Small-Signal Model

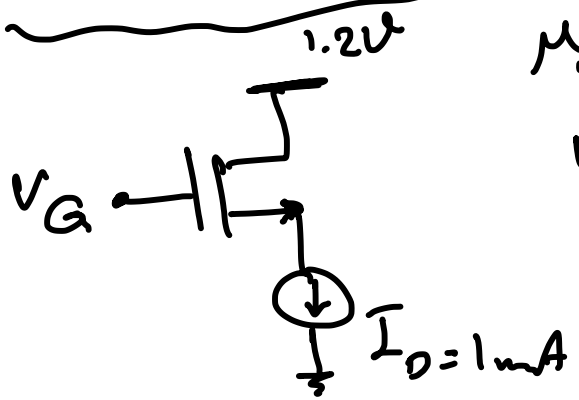


- The complete MOS small-signal model not only includes channel-length modulation and body effect, but also the capacitances between each terminal.

MOS Small-Signal Model







$\mu_n C_{ox} = 0.5 \frac{mA}{V^2}$

$W/L = 10$

$\lambda = 0.1 V^{-1}$

$L = 90nm$

$C'_{GS} = 0.2 \frac{fF}{\mu m}$

↳ if $W = 1\mu m \Rightarrow C_{GS} = 0.2fF$

$\Rightarrow$

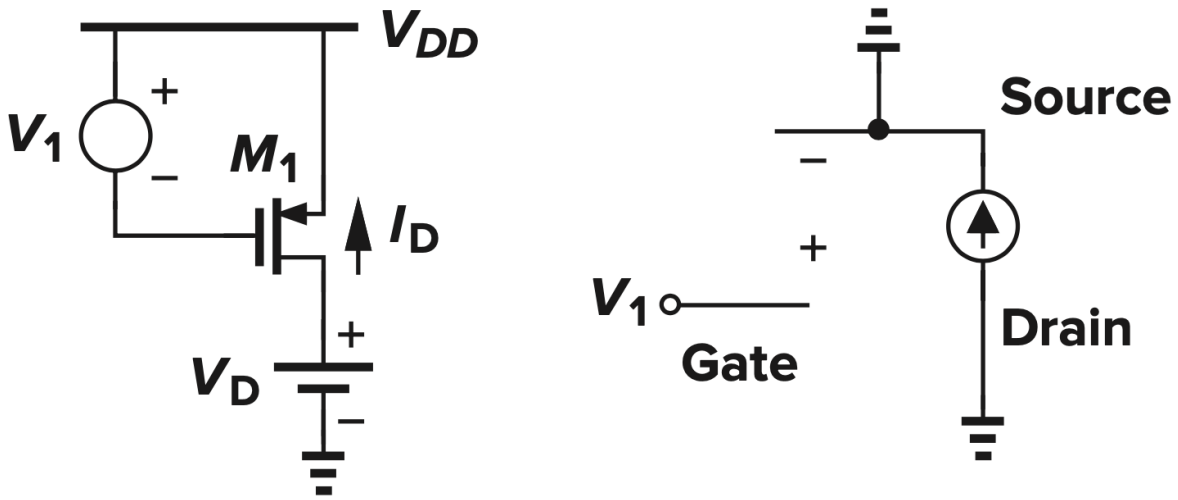
$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D} = \ldots$

$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.1 V^{-1} \cdot 1mA} = 10 k\Omega$

$C_{GS} = 0.2 \frac{fF}{\mu m} \times W \quad (W/L \times L)$

$10 \times 90nm \sim 0.18fF$

MOS Small-Signal Model



- The derivation of the small-signal model for PMOS yields the *exact* same model as for NMOS.
- The model shows the voltage-dependent current source pointing *upward*, giving the (wrong) impression that the direction of the current in the PMOS is opposite of that in NMOS.

MOS Spice Models

Table 2.1 Level 1 SPICE models for NMOS and PMOS devices.

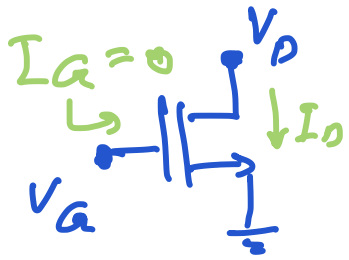
NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

- Simulators such as SPICE and Cadence need accurate models for each device.
- Above is the simplest MOS SPICE model, known as “Level 1,” and provide typical values for each parameter corresponding to 0.5-μm technology.

NMOS versus PMOS Devices

- PMOS devices are quite inferior to NMOS in most CMOS technology.
- Lower mobility of holes ($\mu_p C_{ox} \approx 0.5\mu_n C_{ox}$) yield lower current drive and conductance.
- NMOS exhibit higher output resistance, providing more ideal current sources and higher gain in amplifiers.
- As such is it preferred to incorporate NMOS rather than PMOS wherever possible.

Summary of Chapter 2 Topics

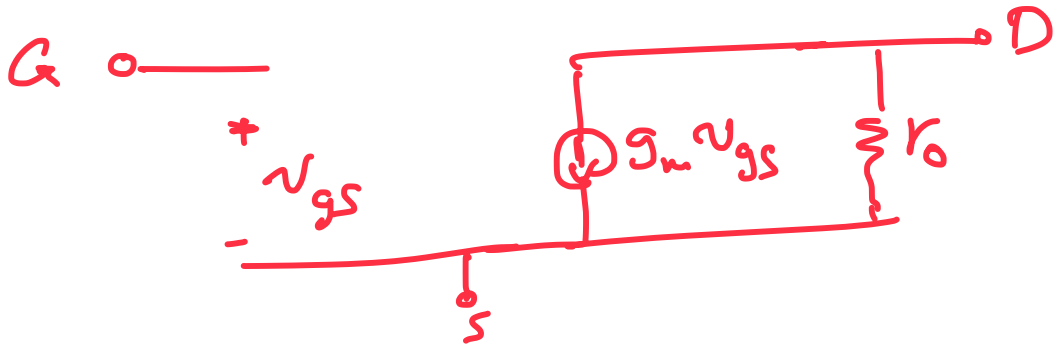


$V_{DS} > V_{GS} - V_{th} \rightarrow$ Sat. $\rightarrow$ $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th})^2(1+\lambda V_{DS})$

$V_{DS} < V_{GS} - V_{th} \rightarrow$ Triode $\rightarrow$ $I_D = \ldots$

$V_{GS} > V_{th}$

$\therefore$ ON



$V_{DD} = 1.5V$