EE 332: Devices and Circuits II

Lecture 2: MOS Devices (Part 2)

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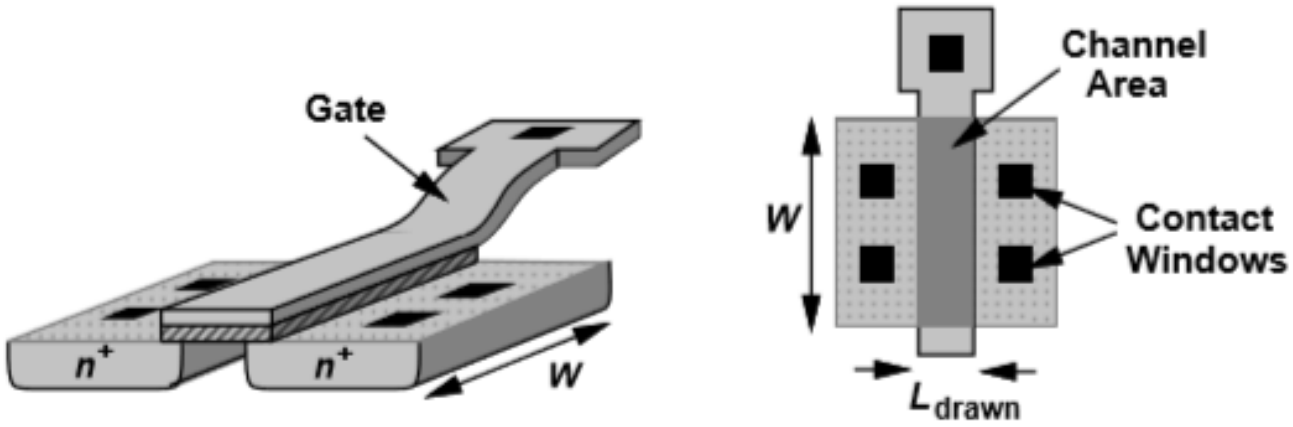
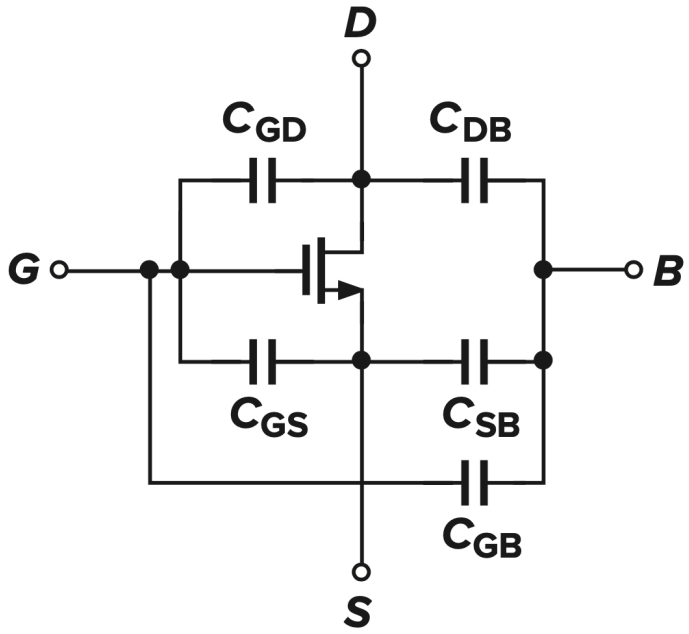
MOS Device Layout



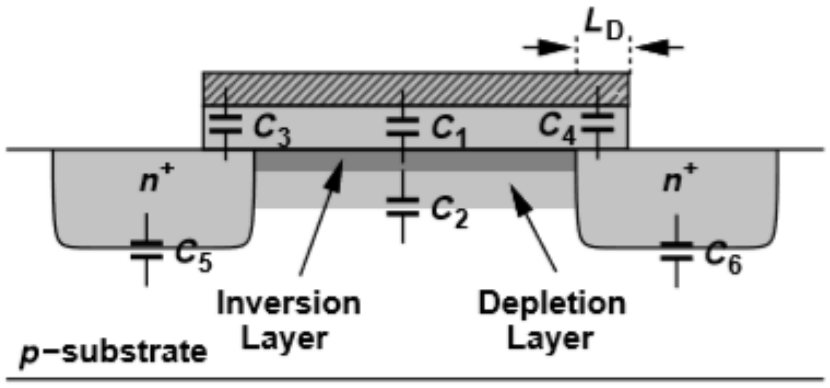
- The gate polysilicon and the source and drain terminals must be tied to metal (aluminum) wires that serve as interconnects with low resistance and capacitance.
- This is accomplished with “contact windows” which are filled with metal and connected to the upper metal wires.
- To minimize the capacitance of the source and drain, the total area of each junction must be minimized.

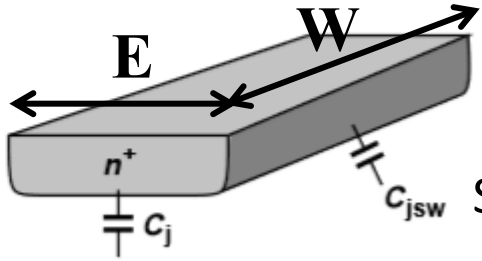
MOS Device Capacitances



- To better predict high-frequency behavior, it is necessary to consider device capacitances.
- Capacitance exists between every two of the four terminals, and their values depend on the bias conditions of the transistor.

MOS Device Capacitances





Sidewall Cap (per length)

Bottom-plate Cap (per area)

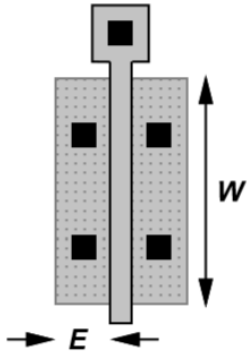
$$C_j = C_{j0}/[1+V_R/(\Phi_B)]^m,$$

$$C_1 = WLC_{ox} \qquad C_2 = WL\sqrt{q\epsilon_{si}N_{sub}/(4\Phi_F)}$$

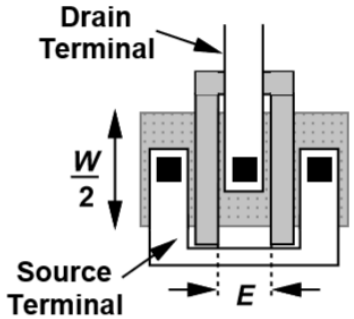
- Capacitances include
  - Oxide capacitance between the gate and the channel C_1.
  - Depletion capacitance between the channel and the substrate C_2.
  - Overlap capacitance between the gate & source/drain (C_3 and C_4).
  - Junction capacitance between the source/drain areas and the substrate C_5 and C_6.

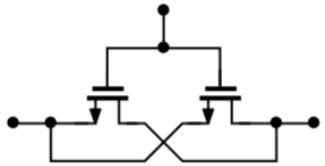
MOS Device Capacitances (C_{DB}, C_{SB})

One "Finger"



Two "Fingers"





- For example calculating the source and drain junction capacitance of the topology on the left,

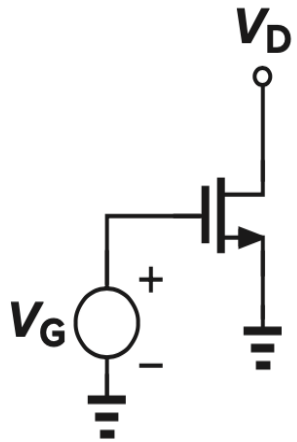
$$C_{DB} = C_{SB} = WEC_j + 2(W + E)C_{jsw}.$$

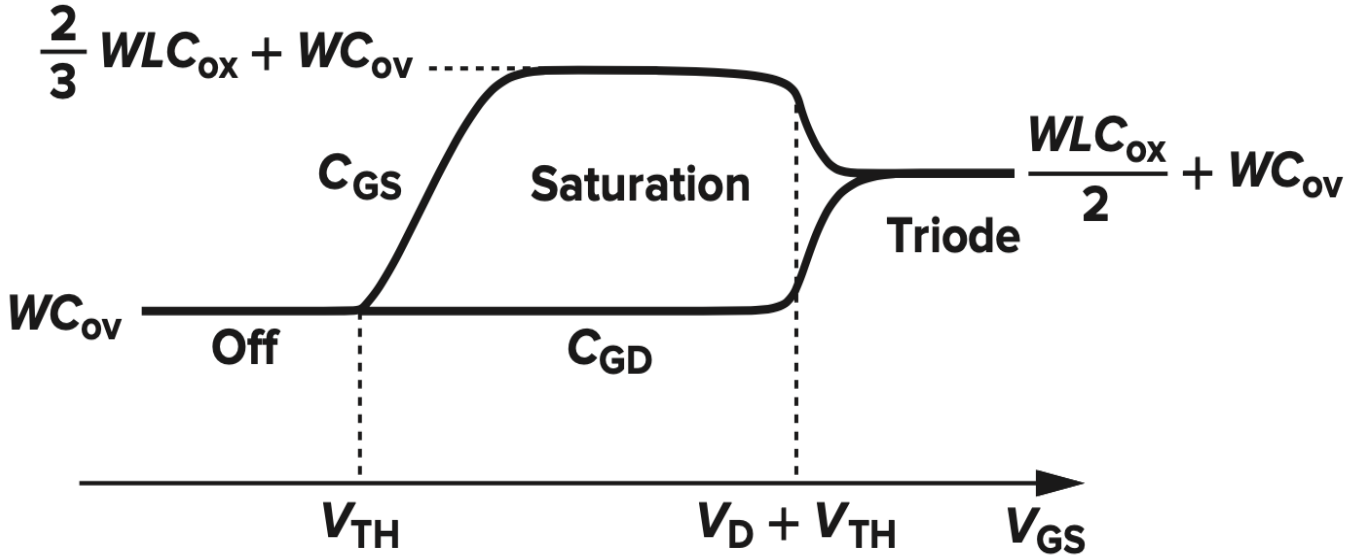
- We assumed the total source/drain perimeter 2(W+E) is multiplied by C_{jsw}.

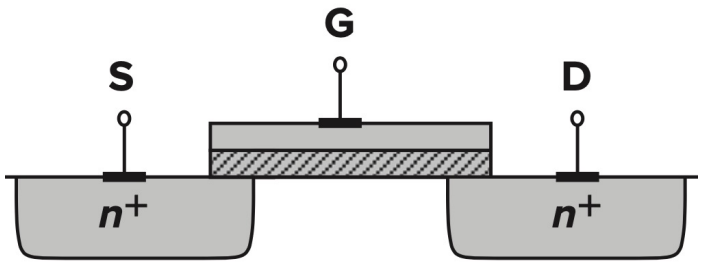
- Calculating the source and drain junction capacitance of the second topology on the left,

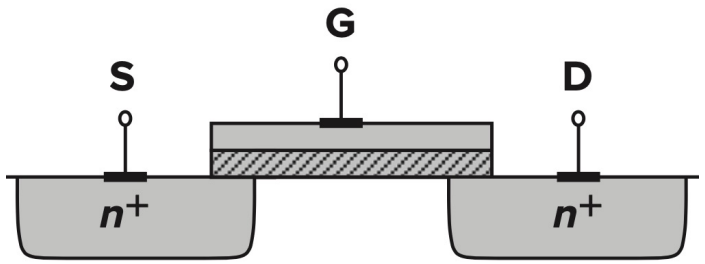
$$\begin{aligned} C_{DB} &= \frac{W}{2}EC_j + 2\left(\frac{W}{2} + E\right)C_{jsw} \\ C_{SB} &= 2\left[\frac{W}{2}EC_j + 2\left(\frac{W}{2} + E\right)C_{jsw}\right] \\ &= WEC_j + 2(W + 2E)C_{jsw}. \end{aligned}$$

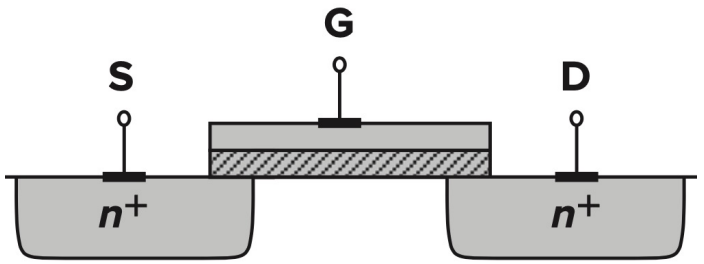
MOS Device Capacitances (C_{GS}, C_{GD})







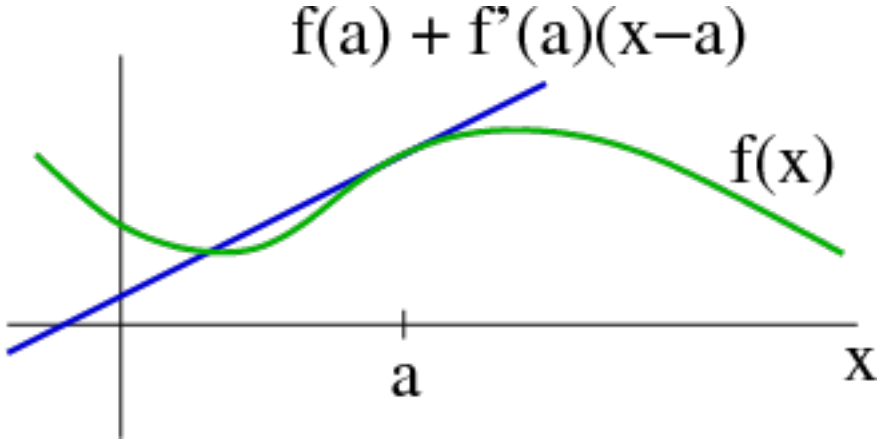




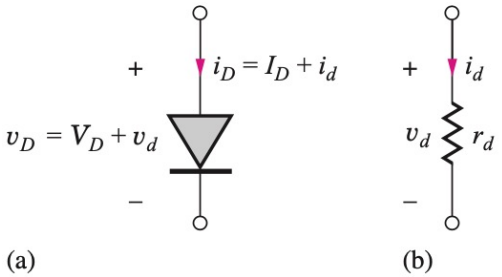
Small-signal (SS) Modeling

- Linear modeling (for AC analysis, etc.)
  - Easier to analyze circuit behavior
  - Using RLC, and voltage & current sources mapping, we can model/solve any circuit

- Linearizing a non-linear function (e.g., 1st-order Taylor series)
  - SS model depends on the operating point ("Bias point")



SS Modeling Example: Diode

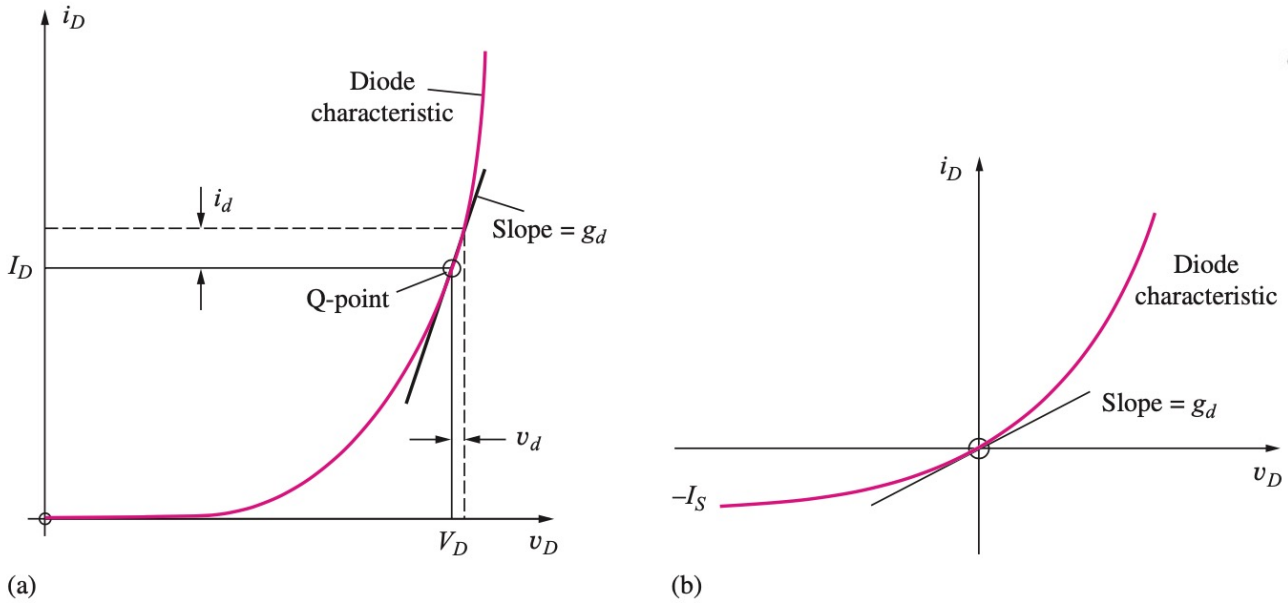


$$r_d = \frac{1}{g_d}$$

$$i_c = I_s\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right]$$

$$i_c = g_m v_{be}$$

Figure 13.8 (a) Total diode terminal voltage and current. (b) Small signal model for the divide.

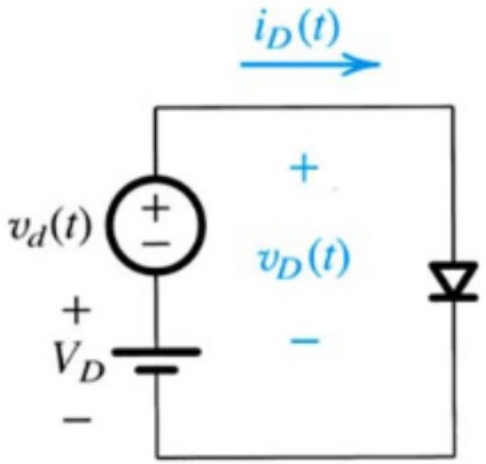


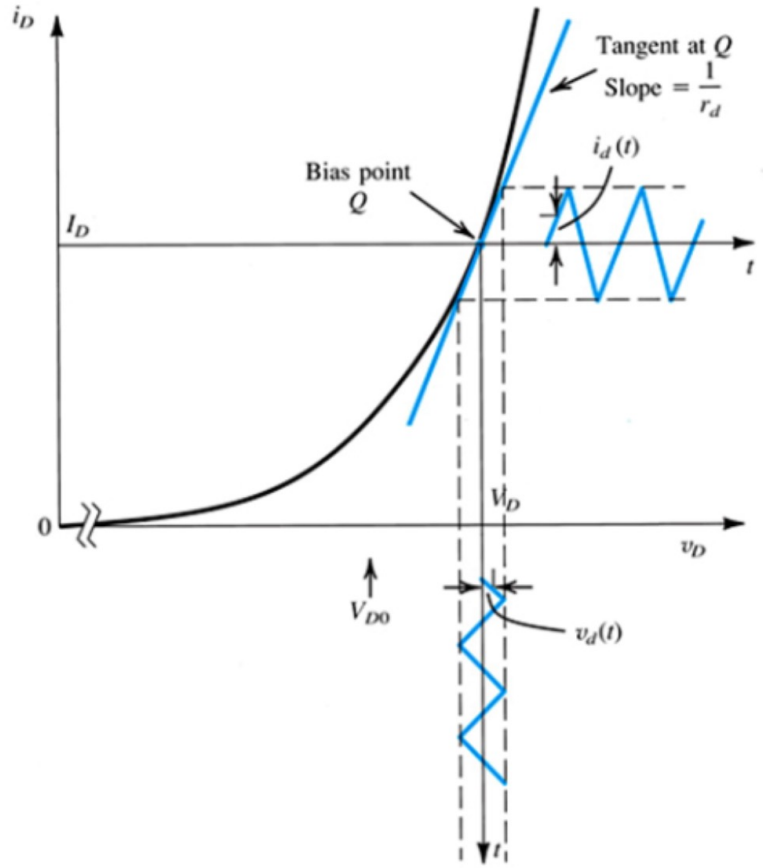
$$g_d = \left.\frac{\partial i_D}{\partial v_D}\right|_{\text{Q-point}} = \frac{\partial}{\partial v_D}\left\{I_S\left[\exp\left(\frac{v_D}{V_T}\right) - 1\right]\right\}\Bigg|_{\text{Q-point}}$$

$$= \frac{I_S}{V_T}\exp\left(\frac{V_D}{V_T}\right) = \frac{I_D + I_S}{V_T}$$

Figure 13.9 (a) The relationship between small increases in voltage and current above the diode operating point (I_D, V_D). For small changes $i_d = g_d v_d$. (b) The diode conductance is not zero for $I_D = 0$.

Bias Point

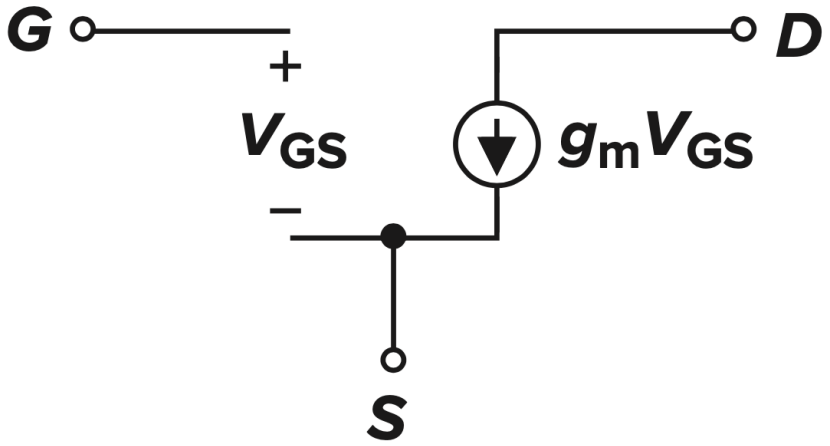

$i_D(t)$
+
$v_D(t)$
−
$v_d(t)$
+
−
+
V_D
−


i_D
Tangent at Q
Slope $= \frac{1}{r_d}$
$i_d(t)$
Bias point
Q
I_D
t
V_D
0
v_D
V_{D0}
$v_d(t)$
t

Small-signal Modeling

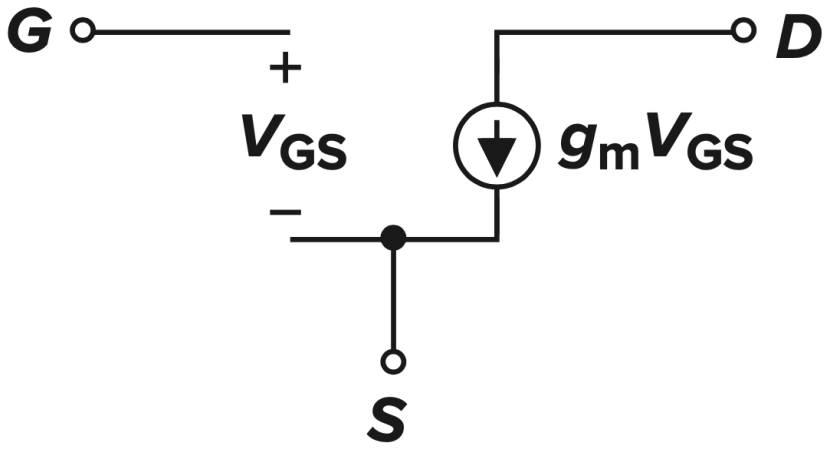
- For more complicated circuits (e.g., multiple devices), you can generate the SS model by either:
    1. Calculate the overall I-V -> Linearize by taking the derivative
    2. Replace each non-linear component with its SS model and then calculate the overall circuit model

MOS Small-Signal Model



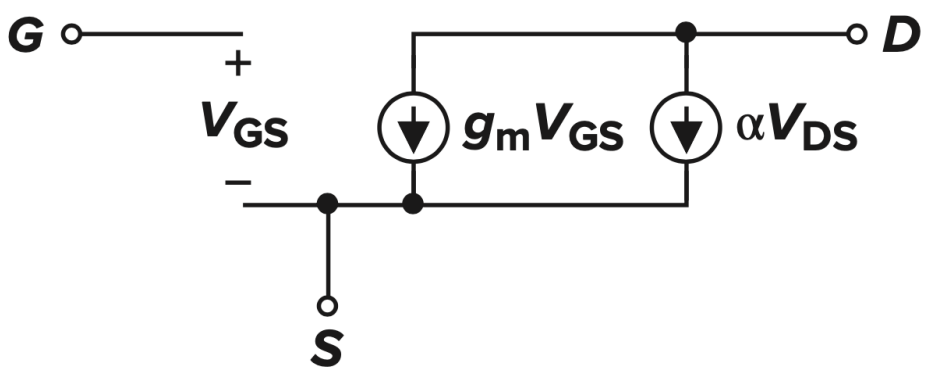
- If perturbation in bias conditions are small, a “small-signal” model can be used to simplify calculations (derived for saturation region).
- In order to derive the small-signal model, we
  - Apply certain bias voltages to the terminals of the device.
  - Increment the potential difference between two of the terminals while the other terminal voltages remain constant.
  - Measure the resulting change in all terminal currents.

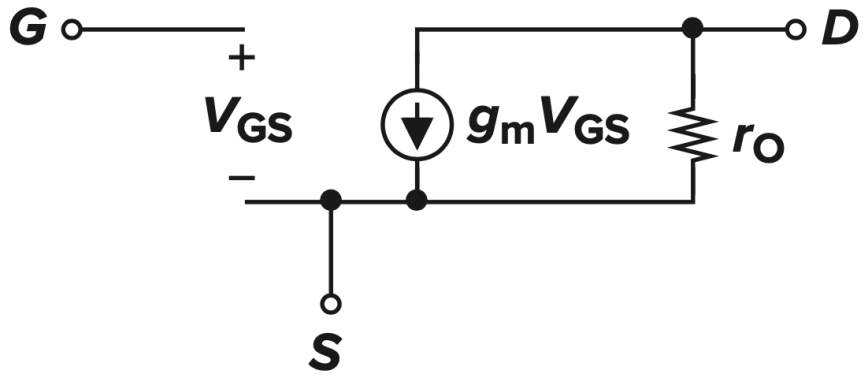
MOS Small-Signal Model



- By changing the voltage between two terminals by $\Delta V = V_{GS}$ and then measuring a current change $\Delta I = g_m V_{GS}$, we can model the effect by a voltage-dependent current source.
- Above is the small-signal model of an ideal MOSFET.

MOS Small-Signal Model





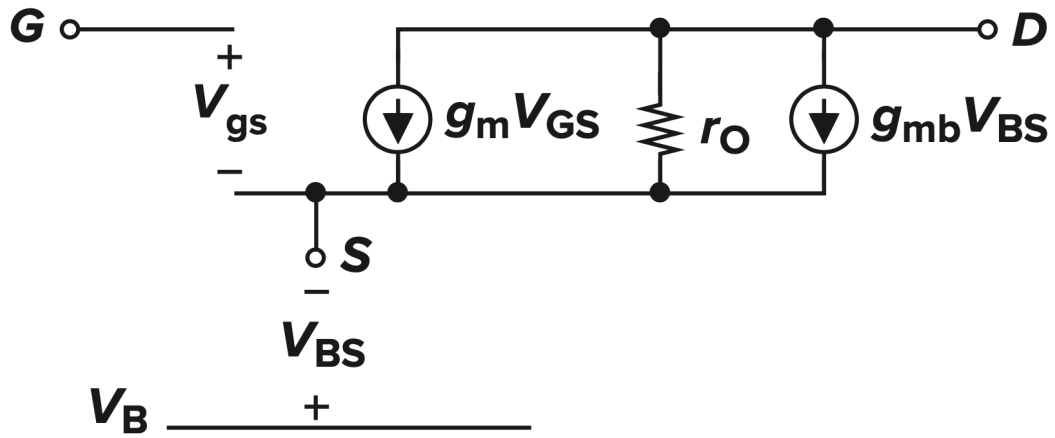
- Due to channel-length modulation, drain current also varies with V_{DS} , but a current source whose value linearly depends on the voltage across it is equivalent to a linear resistor:

$$r_O = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\partial I_D / \partial V_{DS}} = \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2 \cdot \lambda}$$

$$\approx \frac{1+\lambda V_{DS}}{\lambda I_D} \approx \frac{1}{\lambda I_D}.$$

- It is assumed that $\lambda V_{DS} << 1$.
- r_o limits the maximum voltage gain of most amplifiers.

MOS Small-Signal Model



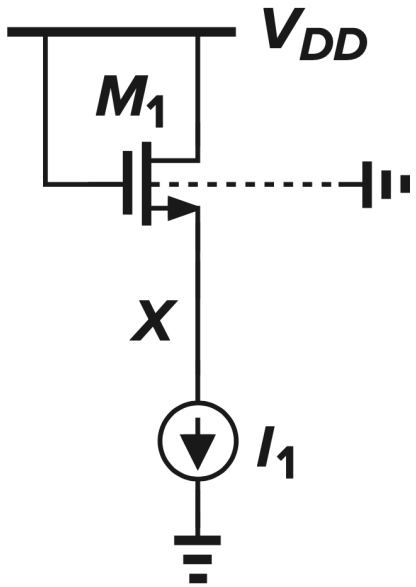
- Due to body effect, bulk potential influences V_{TH} and hence gate-source overdrive.
- With all other terminals held at a constant voltage, the bulk behaves as a second gate since the drain current is a function of the bulk voltage given by $g_{mb}V_{BS}$, where

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) \left(-\frac{\partial V_{TH}}{\partial V_{BS}}\right).$$

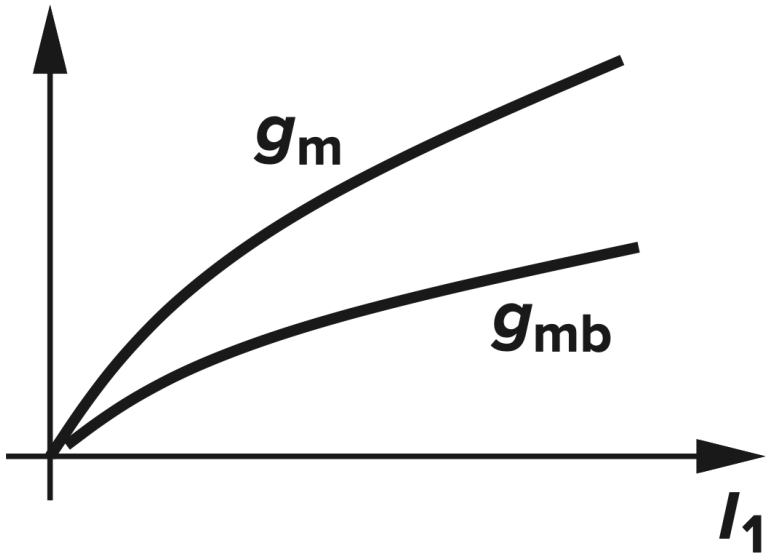
$$\frac{\partial V_{TH}}{\partial V_{BS}} = -\frac{\partial V_{TH}}{\partial V_{SB}} = -\frac{\gamma}{2}(2\Phi_F + V_{SB})^{-1/2}.$$

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} = \eta g_m, \quad \eta = g_{mb}/g_m .$$

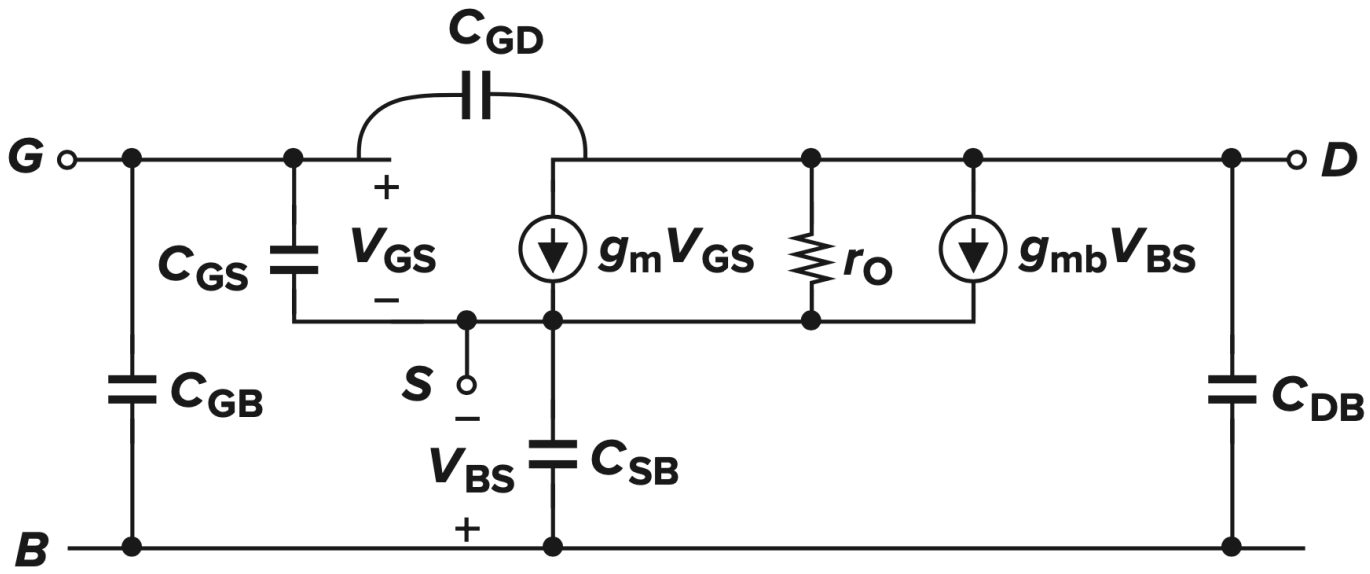
MOS Small-Signal Model



- To sketch g_m and g_{mb} of M_1 on the left as a function of bias current I_1,
  - $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D} \Rightarrow g_m \propto \sqrt{I_1}$
  - g_{mb} dependence on I_1 is less straight forward, but as I_1 increases, V_X decreases and so does V_{SB}.

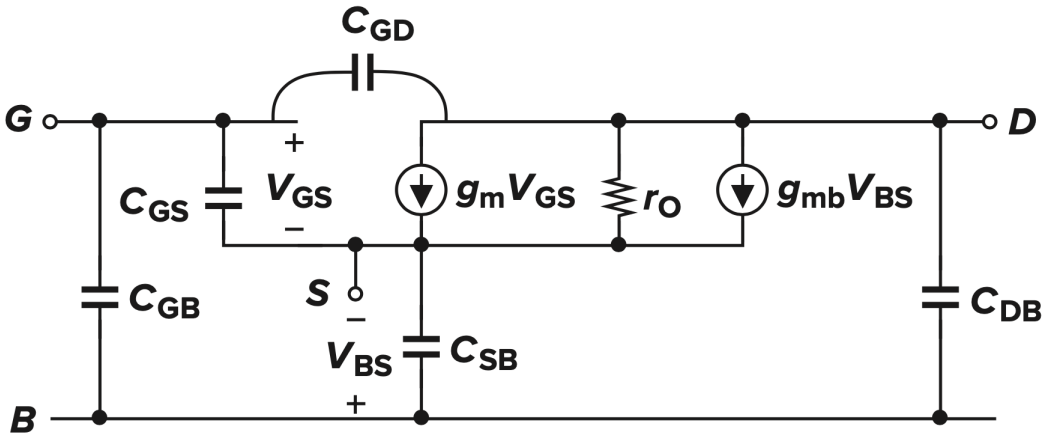


MOS Small-Signal Model

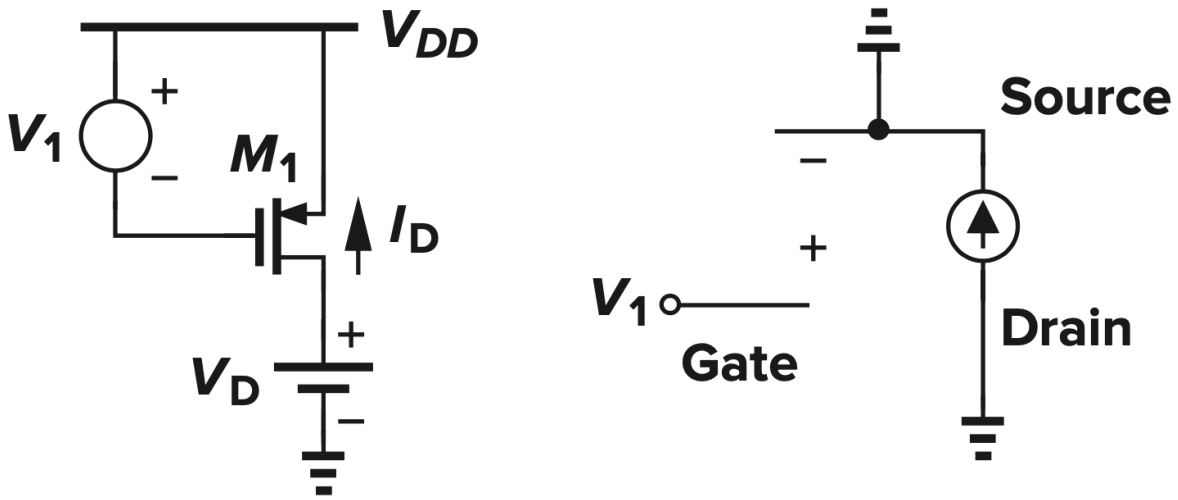


- The complete MOS small-signal model not only includes channel-length modulation and body effect, but also the capacitances between each terminal.

MOS Small-Signal Model



MOS Small-Signal Model



- The derivation of the small-signal model for PMOS yields the *exact* same model as for NMOS.
- The model shows the voltage-dependent current source pointing *upward*, giving the (wrong) impression that the direction of the current in the PMOS is opposite of that in NMOS.

MOS Spice Models

Table 2.1 Level 1 SPICE models for NMOS and PMOS devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

- Simulators such as SPICE and Cadence need accurate models for each device.
- Above is the simplest MOS SPICE model, known as “Level 1,” and provide typical values for each parameter corresponding to 0.5-μm technology.

NMOS versus PMOS Devices

- PMOS devices are quite inferior to NMOS in most CMOS technology.
- Lower mobility of holes ($\mu_p C_{ox} \approx 0.5\mu_n C_{ox}$) yield lower current drive and conductance.
- NMOS exhibit higher output resistance, providing more ideal current sources and higher gain in amplifiers.
- As such is it preferred to incorporate NMOS rather than PMOS wherever possible.

Summary of Chapter 2 Topics