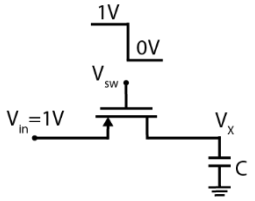
EE 332 Circuits and Devices II Autumn 2022
Homework 1 Due: Oct. 14 (11:59pm)

1. *Dennard Scaling:* Consider a basic NMOS device with quadratic I/V-relation that we studied in the first week ($I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$). Now suppose that every next generation of this CMOS technology will benefit from scaling down all the dimensions (W, L, thicknesses) by a factor of namely *s* (*s* is smaller than 1).

- **a.** What should be the nominal *s* value for Moore's law to be true (i.e. transistor density will be doubled in every new generation)?
- **b.** If we want to keep all the electrical fields constant (in particular, the field in gate oxide capacitance), how should the voltages scale? What about threshold voltage?
- **c.** Explain how the following parameters change in this type of scaling:
  Density of transistors per mm^2, drain-source current (in saturation regime), transconductance (g_m), device capacitances (C_{GS}, C_{GD}, C_{DB}), output resistance (r_o)
- **d.** If the speed of circuits can be estimated from charging/discharging time of the device capacitances, how does the speed (*f*) scale up? (*Hint:* you can estimate the time from $I = \frac{C_{GS}dV}{dt}$ and estimate *f* to be linearly proportionate to $\frac{1}{dt}$)
- **e.** If power consumption for each MOS device can be estimated from charging/discharging energy of gate capacitance (C_{GS}) as $P = C_{GS}V_{DD}^2 f$. How does a single transistor's dynamic power consumption scale? How about the total power per area?
- **f.** What are the obstacles and challenges of this scaling down trend? How far do you think we can benefit from this?

2. *Switch Cap:* We can sample an analog signal using a simple MOS switch and store the analog value on a capacitor. Circuit diagram below shows a simple "switch cap" circuit during the charging cycle:



a. If the cap is discharged initially ($V_X = 0$), describe how V_X changes after the switch turns on, and identify PMOS working regions (assume V_{TH} = -0.4V, $\mu_p C_{ox} = \frac{100\mu A}{V^2}$, W/L = 1um/65nm, C = 100fF).

b. Write down governing I/V equations for each regime and draw the plot of V_X over time. (*Hint*: MOS can be modeled as a current source in the saturation region and a resistor in the triode)

c. What will happen if the input voltage (V_{in}) is at 0.3V instead of 1V? Does the sampling circuit still work? If not, how can we solve this issue by using another circuit? (*Hint:* what if the switch was an NMOS?)

3. *Razavi 2.13 (parts a and c):* The transit frequency, f_T, of a MOSFET is defined as the frequency at which the small-signal current gain of the device drops to unity while the source and drain terminals are held at ac ground.

a. Prove that:

$$f_T = \frac{g_m}{2\pi(C_{GD} + C_{GS})}$$

Note that f_T does not include the effect of the S/D junction capacitance. *Hint:* Small-signal current gain can be derived by calculating drain current using the small-signal model when we have an ac current source at the gate.

c. For a given bias current, the minimum allowable drain-source voltage for operation in saturation can be reduced only by increasing the width and hence the capacitances of the transistor. Using square-law characteristics, prove that

$$f_T = \frac{\mu_n}{2\pi}\frac{V_{GS} - V_{TH}}{L^2}$$

This relation indicates how the speed is limited as a device is designed to operate with lower supply voltages.

4. *Razavi 2.2:* For $\frac{W}{L} = \frac{50}{0.5}$ and $|I_D| = 0.5\,mA$, calculate the transconductance and output impedance of both NMOS and PMOS devices. Also, find the "intrinsic gain", defined as $g_m r_o$. Use the device data shown in Table 2.1 from Razavi (copied below) and assume $V_{DD} = 3V$.

5. *Razavi 2.3:* Derive expressions for $g_m r_o$ in terms of I_D and W/L. Plot $g_m r_o$ as a function of I_D with L as a parameter. Note that $\lambda \propto 1/L$. Use the device data shown in Table 2.1 from Razavi (copied below) and assume $V_{DD} = 3V$.

Table 2.1 Level 1 SPICE models for NMOS and PMOS devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8