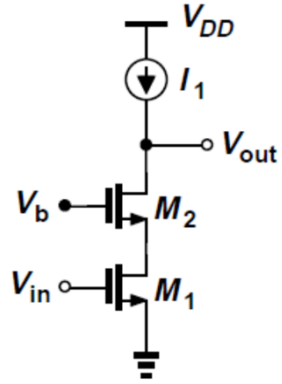
EE 332 Circuits and Devices II Autumn 2022

Homework 5 Due: Nov. 11 (11:59pm)

1. ***Cascode Stage.*** Design a Cascode amplifier shown in figure below to achieve a gain of 1600. Assume VDD=1V, $V_{th} = 0.3V, \lambda_n = 0.2V^{-1}, \gamma = 0, \mu_n C_{ox} = \frac{100\mu A}{V^2}, I_1 = 1mA, g_m r_o \gg 1$.

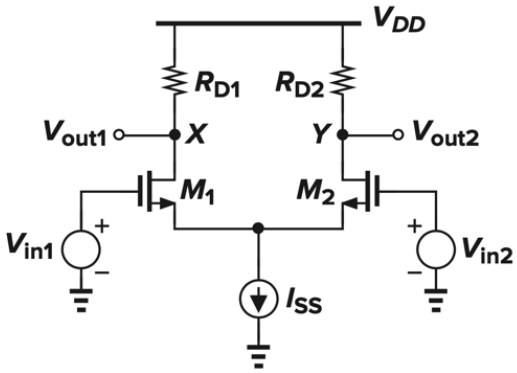


a) Find bias point (V_{GS}-V_{th} of transistors) to achieve the target gain such that we achieve maximum swing at V_{out}.
b) Find W/L for each transistor.
c) Calculate optimal V_b and V_{IN} DC bias to maximize output swing. What is this maximum/minimum voltage levels at the output? What is the maximum swing?
d) Notice you must generate a specific V_b externally to maximize the swing. If a lazy designer decides to connect V_b to VDD instead, what would be the swing in this case?
e) To realize the current source load, we will use a PMOS active load. For PMOS, use the same parameters with $\lambda_p = 0.2V^{-1}, \mu_p C_{ox} = \frac{50\mu A}{V^2}$. Assume the bias current will remain at 1mA, find the new gain value. What would be the W/L for PMOS if we want to have a V_{OD} (V_{GS}-V_{th}) of 0.1V for this device.
f) Repeat part (e) for a PMOS load with 2L gate length.
g) It seems like making the PMOS load very large (large W) is beneficial to reduce V_{OD} and consequently improving the voltage swing. What do you think is the drawback?

For this HW assume: VDD=1V, Vth=0.3V, $\mu_n C_{ox} = \frac{200\mu A}{V^2}, \lambda = 0.2V^{-1}, \gamma = 0$.

****All the differential amplifiers are symmetric unless we are interested in analyzing mismatch effects in the problem.***

2. Consider the following differential amplifier with R_{D1}=R_{D2}=R_D:

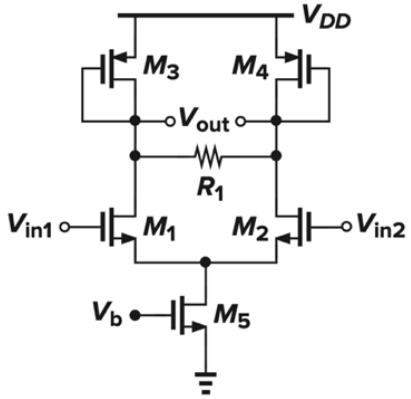


a) If the power consumption is limited to 2mW, what should be R_D to achieve a differential peak-to-peak swing of 1V?
b) Draw the small-signal half-circuits for differential-mode (DM) and common-mode (CM). Clearly determine differential and CM input sources as a result of V_{in1} and V_{in2}. (For CM, assume tail current source has an output impedance of R_{SS})
c) If we need a differential gain of 5, what should be g_m, V_{OD} ($V_{OD} = V_{GS} - V_{TH}$), and W/L for input devices ($M_{1,2}$)? Use R_D determined in part a.

d) What is the maximum tolerable differential input voltage range for the circuit to operate in the linear region? (i.e. $\Delta V_{in1} = ?$)
e) For a CM gain of 0.05, what should be the value of R_{SS}? ignore output resistance of $M_{1,2}$ in this part.
f) If we decide to realize the tail current source with an NMOS, what should be the L for that device? (Assume that $\lambda = 0.2V^{-1}$ for L= L_0=65nm)
g) What would be W for this device (tail current NMOS) in order to set its V_{OD} to 0.2V?
h) What is the acceptable input common-mode range to keep the amplifier linear after adding the tail device?

3. For the differential pair amplifier circuit shown below: (Write down final answers in terms of key circuit parameters g_m, r_o, etc.)

a) Draw the differential and common mode half-circuits. (*Hint:* how can you replace R_1 with two elements such that circuit will be still symmetric to use half-circuit techniques?)
b) Find the differential and CM small-signal gains.
c) What's the single-ended and differential output peak-to-peak swings?
d) What is the CM input range?



4. For a basic differential amplifier (shown in Problem 1), suppose that there are some fluctuations/noise sources on the supply, namely, V_{dd} that can be modeled as an AC voltage source.

a) Does this supply cause the differential output to change? How about the CM at each output?
b) Draw the half-circuit model to find the impact of such a supply noise source at the output.
c) Calculate the resultant output CM voltage due to the supply noise (in terms of circuit parameters, no need for numerical answers!)
d) If the R_Ds have ΔR_D mismatch, what would be the impact of this noise source on the differential output voltage?

5. We can make a differential pair amplifier with PMOS input devices as shown below. Suppose circuits are completely symmetric (R_Ds are equal, $M_{1,2}$ are similar, and each tail current source requires minimum of V_{od} to operate)

a) What is the single-ended and differential output swing?

b) Draw DM and CM half-circuits. (assume that the tail current source has an output impendence of R_{SS})
c) Calculate DM and CM gains.
d) What is the acceptable input CM range?
e) Compare the results from (d) with the NMOS diff pair we studied in the class.