EE 437/538B: Integrated Systems Capstone/Design of Analog Integrated Circuits and Systems

Suggested Project Ideas

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Spring 2022

Grades & Project

- ***Group Project***
  - Groups of two students
  - Will be assigned and discussed by the end of Week 2 (so that you can do proper literature review for Week 5)
  - Details of project will be finalized by Week 4
  - We will discuss progress, results, simulations every week in “Project Discussion Sessions”

Grading

- Class Participation: 20%
- Project: 60%
  - Lit. Review: 20%
  - Final presentation: 20%
  - Paper: 20%

Examples from Spring 2021

Proposed Projects (EE536)

1) Study the role/impacts of CTLE for +50GS/s Rx Analog-front end (AFE)

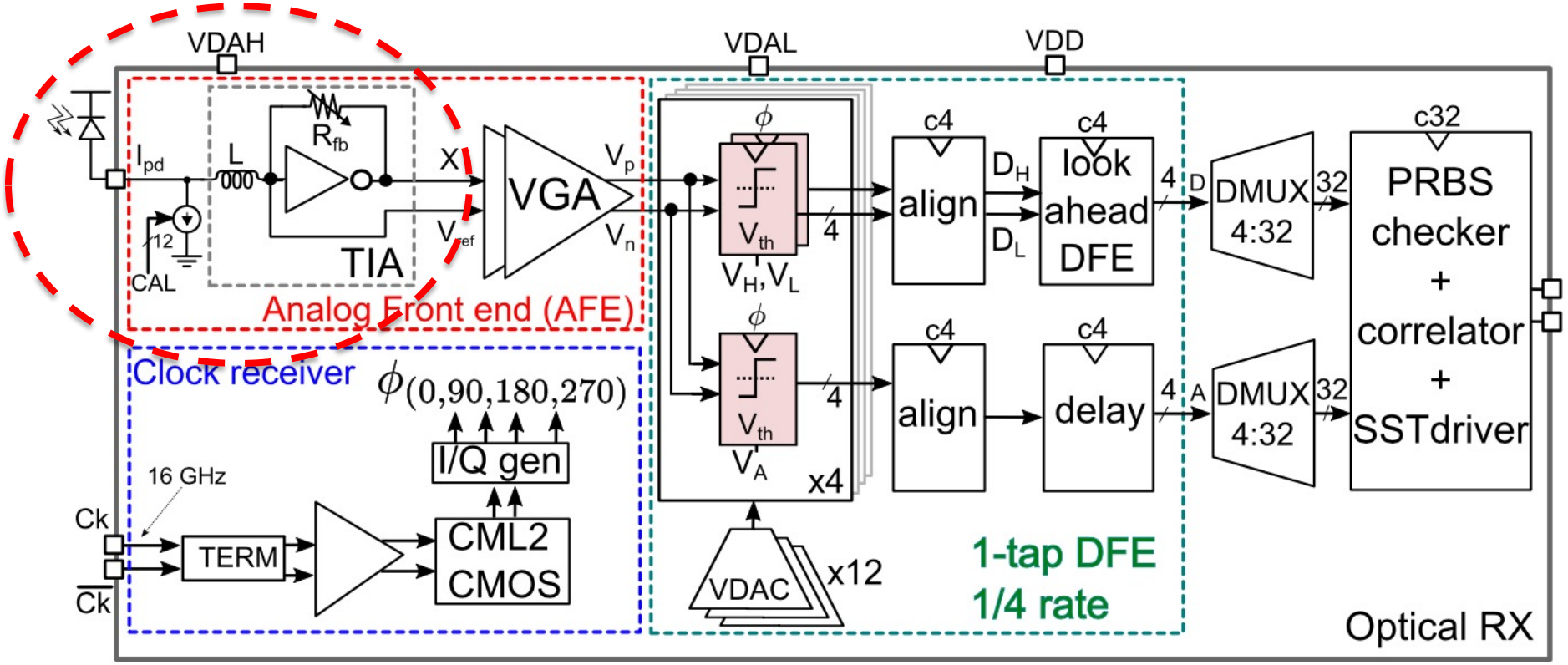
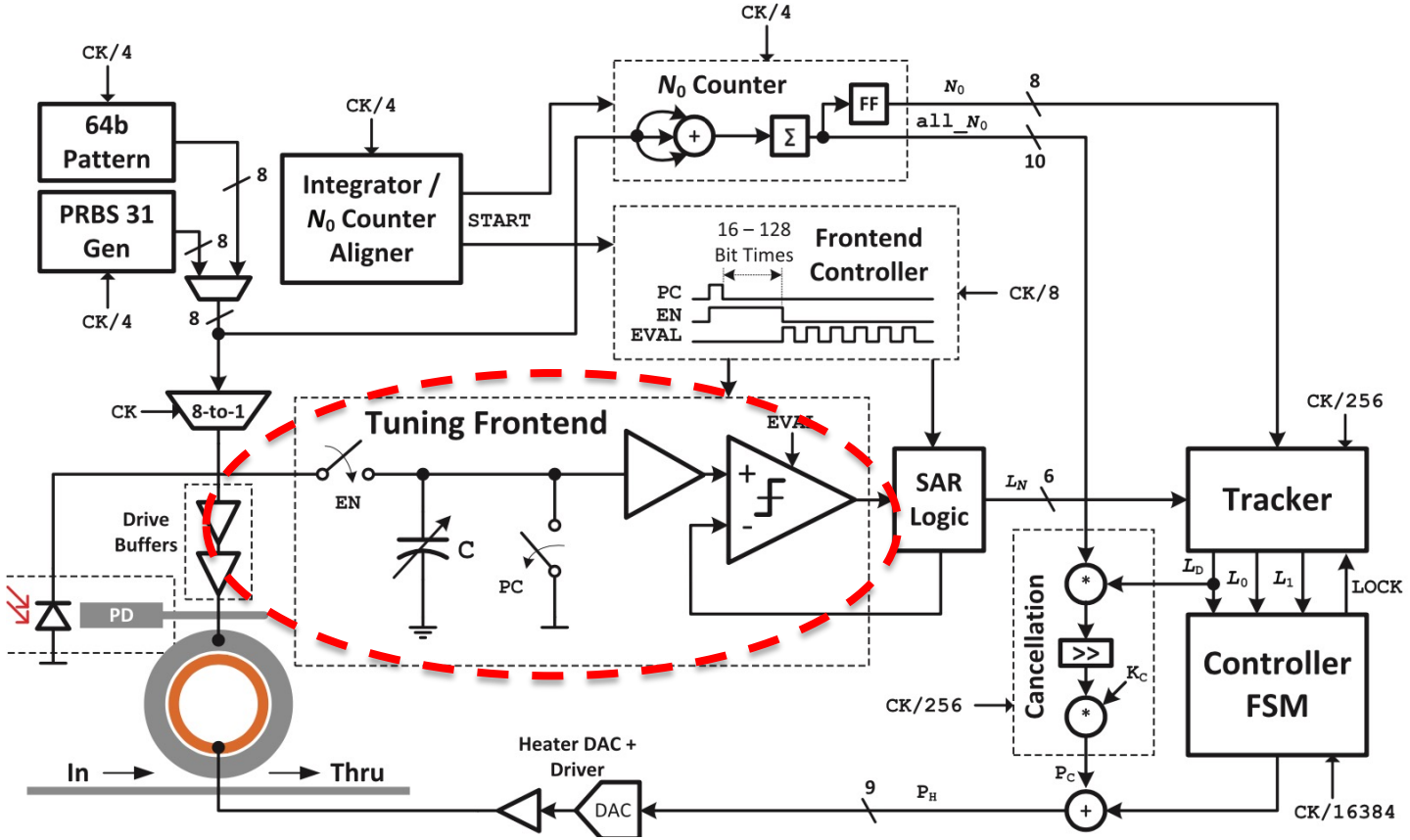


Fig. 9. Top-level schematic of the RX.

Ref 1: A 64-Gb/s 1.4-pJ/b NRZ Optical Receiver Data-Path in 14-nm CMOS FinFET (JSSC 2017)

Proposed Projects (EE437)

2) Design a high-dynamic range receiver front-end + ADC for thermal tuning at Tx



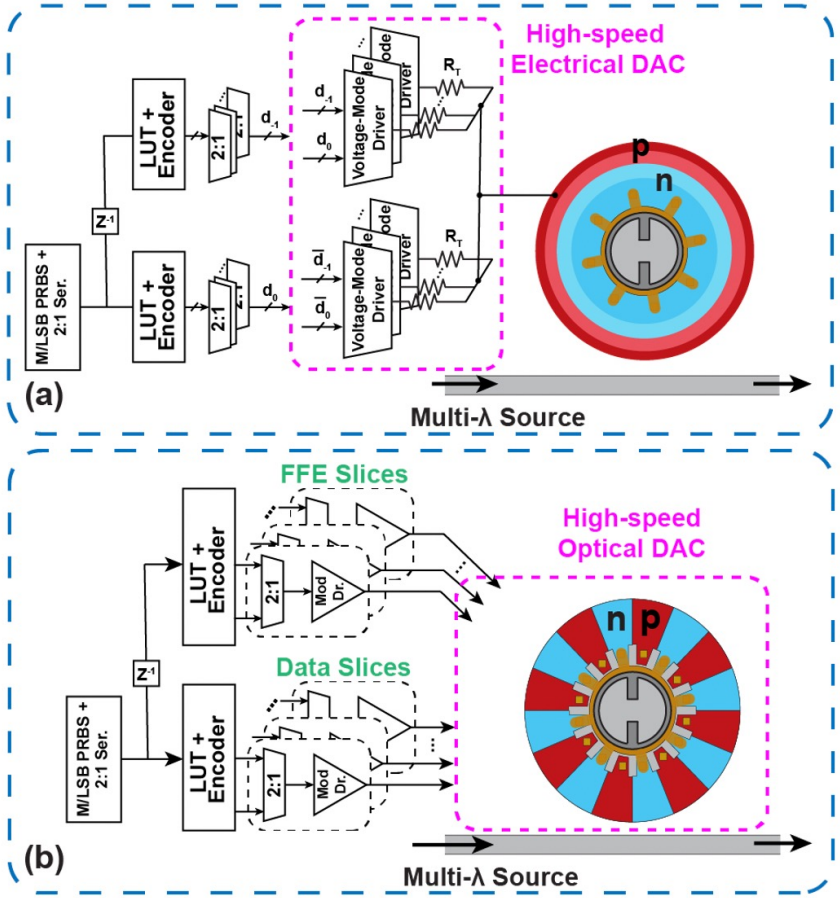
Ref 1: A 45 nm CMOS-SOI Monolithic Photonics Platform With Bit-Statistics-Based Resonant Microring Thermal Tuning (JSSC 2016)

Ideas for Spring 2022

Project 1

Embedded Equalization in a ring-modulator:

- Challenges, modulation schemes, link budget, etc.



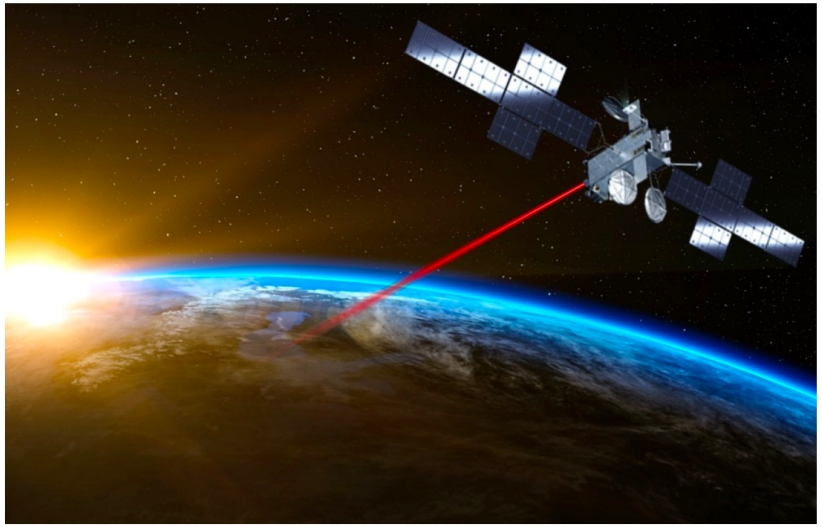
References:

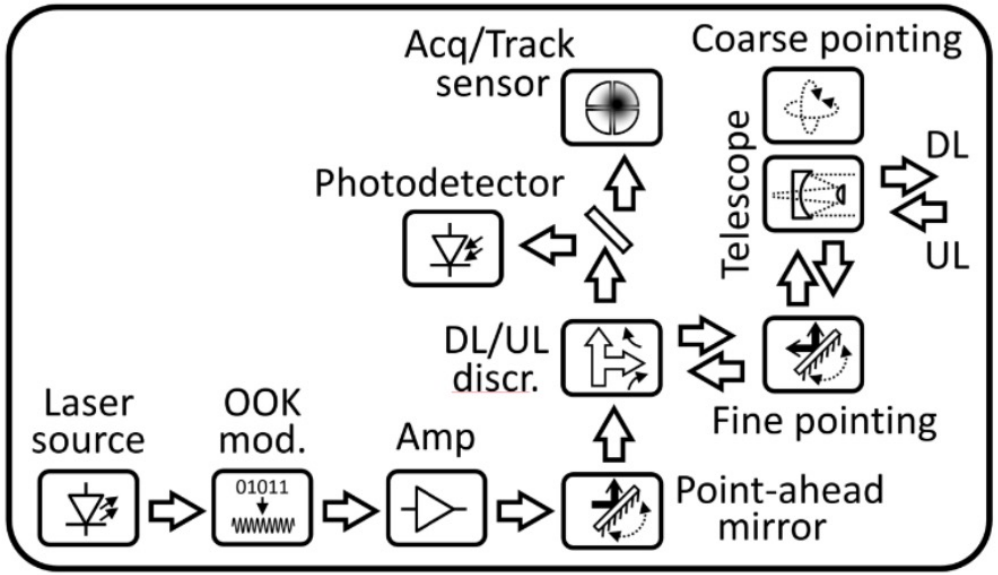
1) S. Moazeni, A 40-Gb/s PAM-4 Transmitter Based on a Ring-Resonator Optical DAC in 45-nm SOI CMOS, JSSC 2018
2) ?

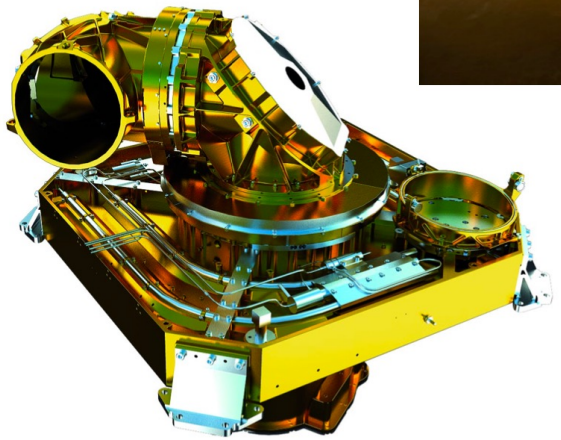
Project 2

Optical Satellite Communications:

– Challenges, modulation schemes, link budget, etc.





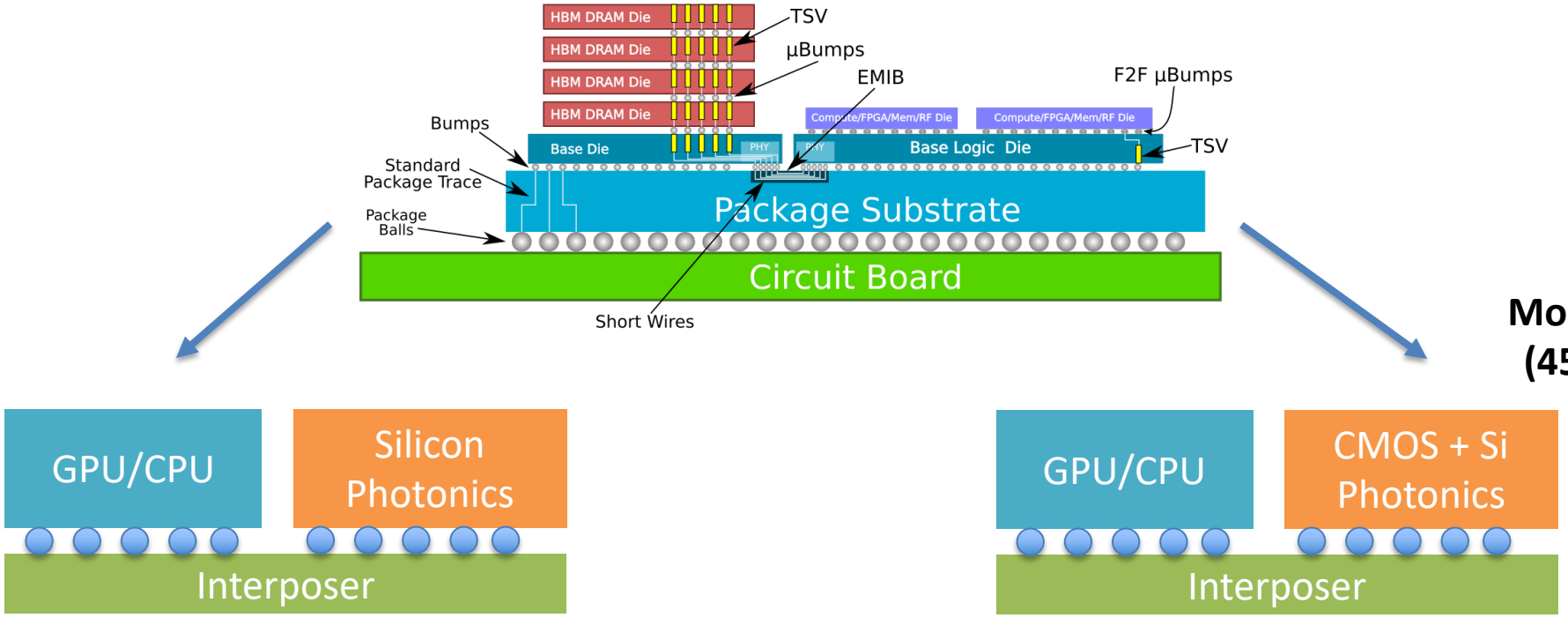


References:

1) Free-space optical links for space communication networks, https://doi.org/10.1007/978-3-030-16250-4_34
2) ?

Project 3

Analysis of a 2.5D integration vs. 3D integrated co-packaged optics:



Monolithic SiPh (45nm CMOS)

References:

1) Silicon Photonic 2.5D Multi-Chip Module Transceiver for High-Performance Data Centers (JLT 2020)
2) ?

Other ideas?

- *Only device projects are not accepted!*
- *Projects should include the circuit level details.*