EE 437/538B: Integrated Systems Capstone/Design of Analog Integrated Circuits and Systems

Lecture 1: Logistics & Intro

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Course Information

- Instructor:
  - Prof. Sajjad Moazeni
  - M422 ECE, smoazeni@uw.edu
  - Office hours by email appointment

- Website:
  - UW Canvas (https://canvas.uw.edu)
  - Lectures (annotated), discussions, Zoom meetings!!!
  - Lectures: 2:30 pm -4:30 pm on Tue/Thu

- No TA/Grader

Introduce yourself …

- Name
- Grad / Undergrad
- Major
- Which year?
- Your advisor
- Your research/background/interests
- Why interested in this course?

Topics

Course Objectives:

- Learn basic architecture of a wireline/optical transceiver (TRx)
- Learn the challenges and gain design experience of some major blocks
- Present and report your work in a professional academic format

Week	Lectures
Week 1	Lect. 1: Course Logistics & Intro (March. 29)
	Lect. 2: Channel pulse model
Week 2	Lect. 3: Overview of equalization techniques & Basic TRx blocks
	Lect. 4: Basic TRx blocks & Examples of the state-of-the-art wireline TRx
Week 3	Lect. 5: Optical Interconnects (Overview)
	Lect. 6: Optical Interconnects (Modulators & Silicon Photonics)
Week 4	**Project Assignments and Discussion**
	Lect. 7: MRM-based Optical Tx
Week 5	**Literature Review Presentations**
	Lect. 7: MRM-based Optical Tx (part 2)
Week 6	Project Discussion
	Lect. 8: Optical Rx Analog Front-end
Week 7	Project Discussion
	Lect. 9: Timing Basics (Jitter, Clock distribution, etc.)
Week 8	Project Discussion
	Lect. 10: Timing (PLL)
Week 9	Project Discussion
	Lect. 11: Timing (CDR)
Week 10	**Final Presentations**
	Final Presentations

ELECTRICAL & COMPUTER ENGINEERING

Grades & Project

- ***Group Project***
  - Groups of two students
  - Will be assigned and discussed by the end of Week 2 (so that you can do proper literature review for Week 5)
  - Details of project will be finalized by Week 4
  - We will discuss progress, results, simulations every week in "Project Discussion Sessions"

Grading

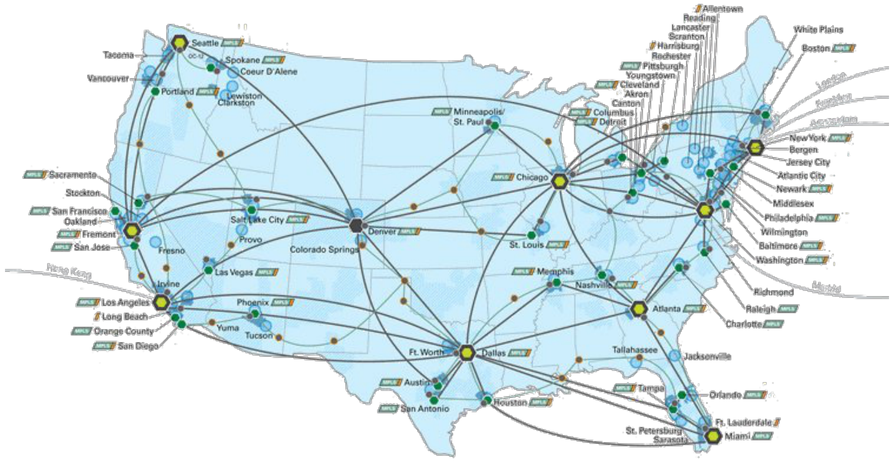
- Class Participation: 20%
- Project: 60%
  - Lit. Review: 20%
  - Final presentation: 20%
  - Paper: 20%

Resources

- EE 538B Slides/Videos
- Sam Palermo's slides from Texas A&M:
  - https://people.engr.tamu.edu/spalermo/ecen720.html
  - https://people.engr.tamu.edu/spalermo/ecen689_oi.html
- Elad Alon's lectures from UC Berkeley (Wireline TRx):
  - https://archive.org/details/ucberkeley-webcast-PL81E2F15D026EEA81
- Recent papers and lectures to be shared on Canvas

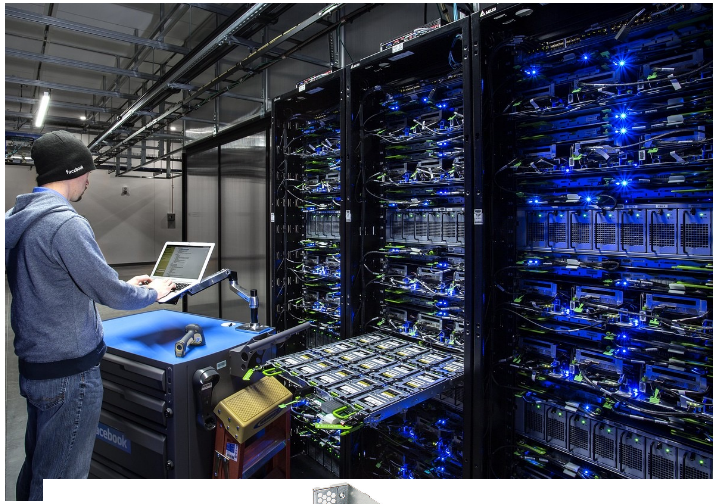
Interconnects

US IT Map



Large Data Centers

Server Racks/Blades



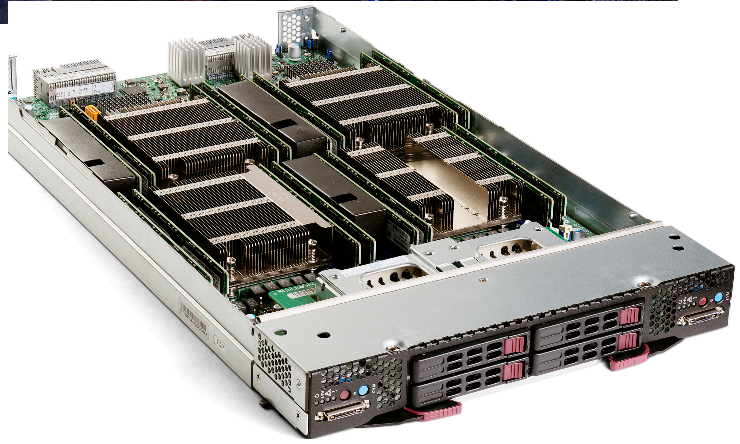
Inter-continents

inter-datacenter

intra-data center

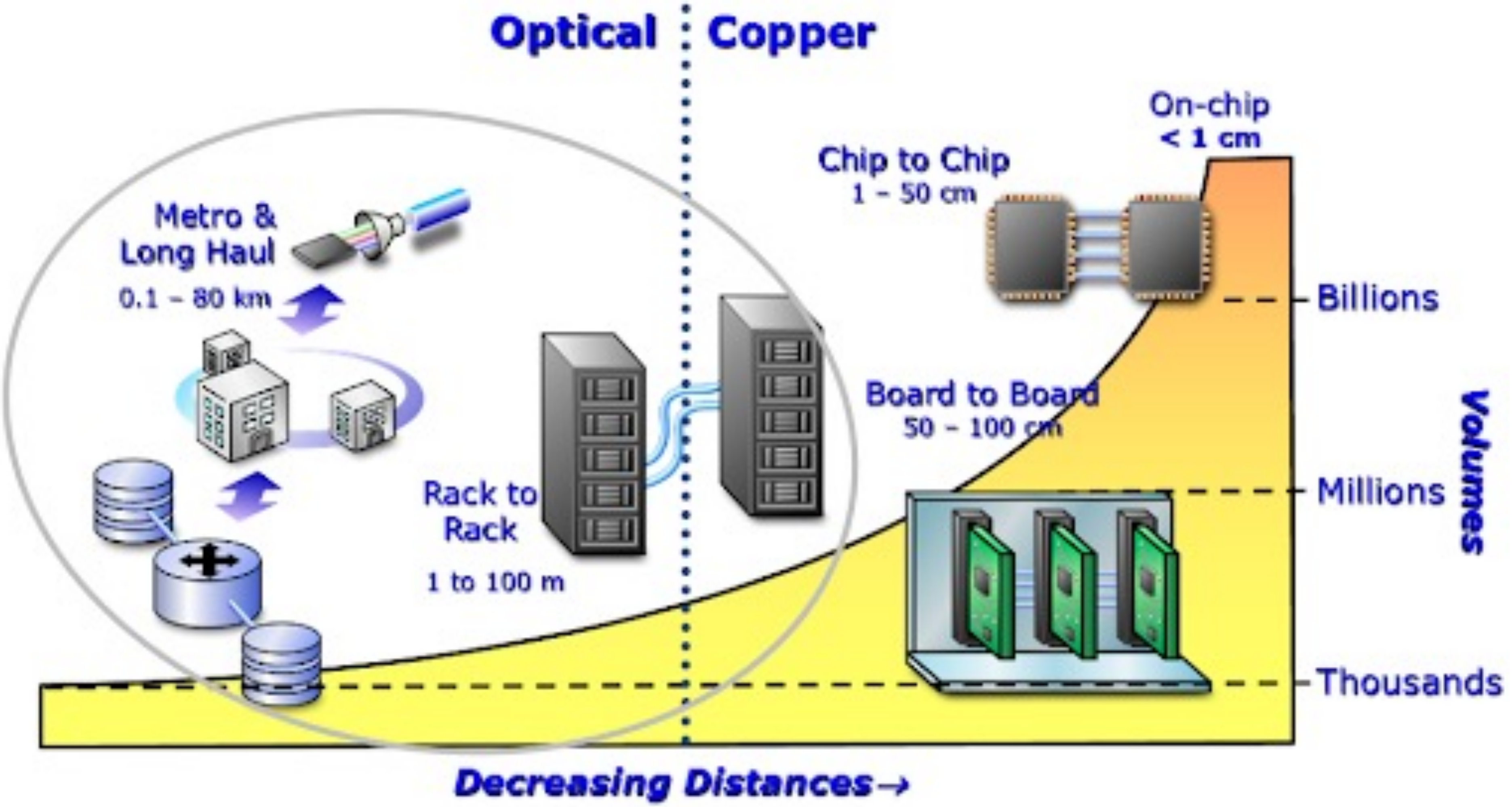
inter-rack

…



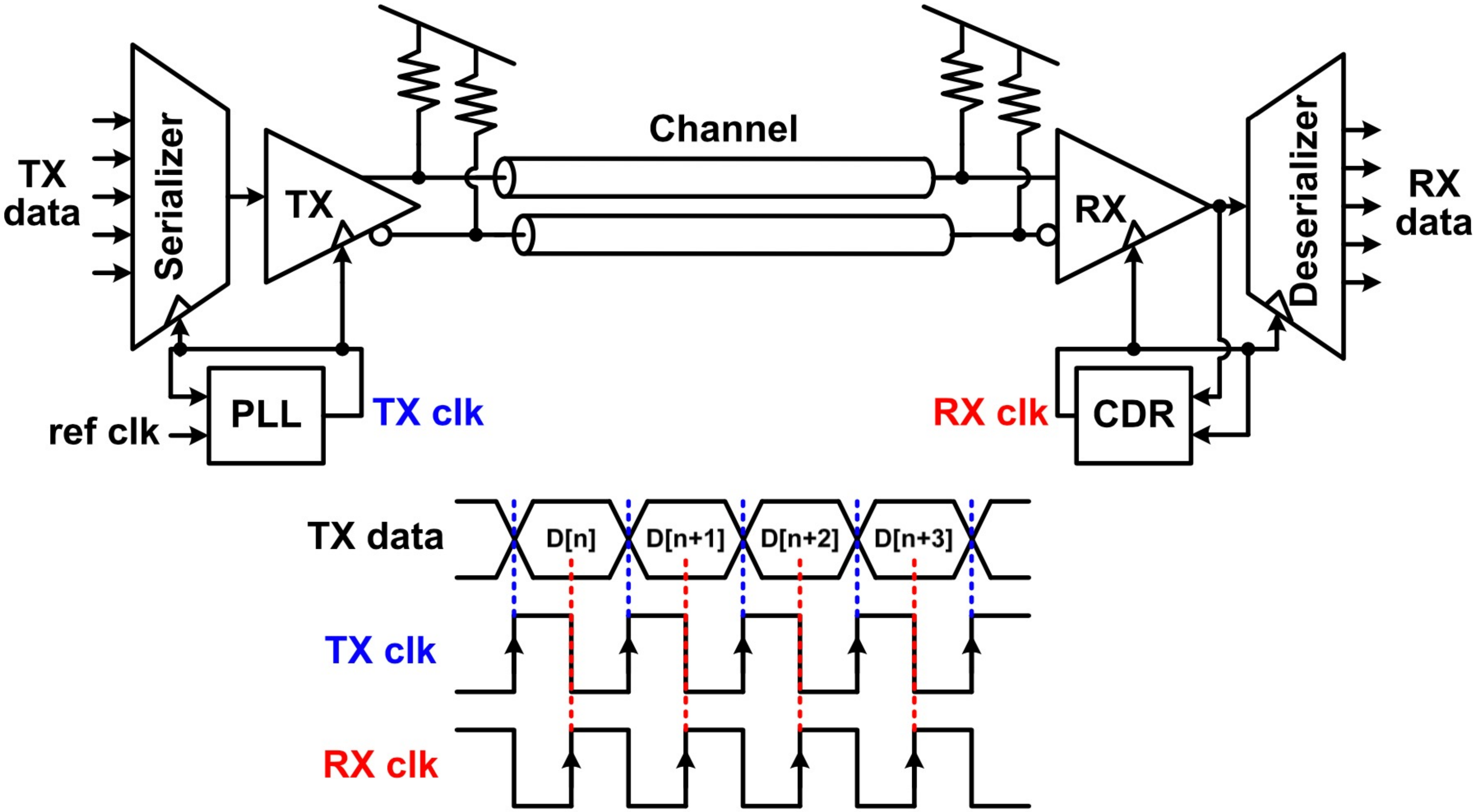
Chip-to-chip

Interconnects



Source: Prof. John Bowers

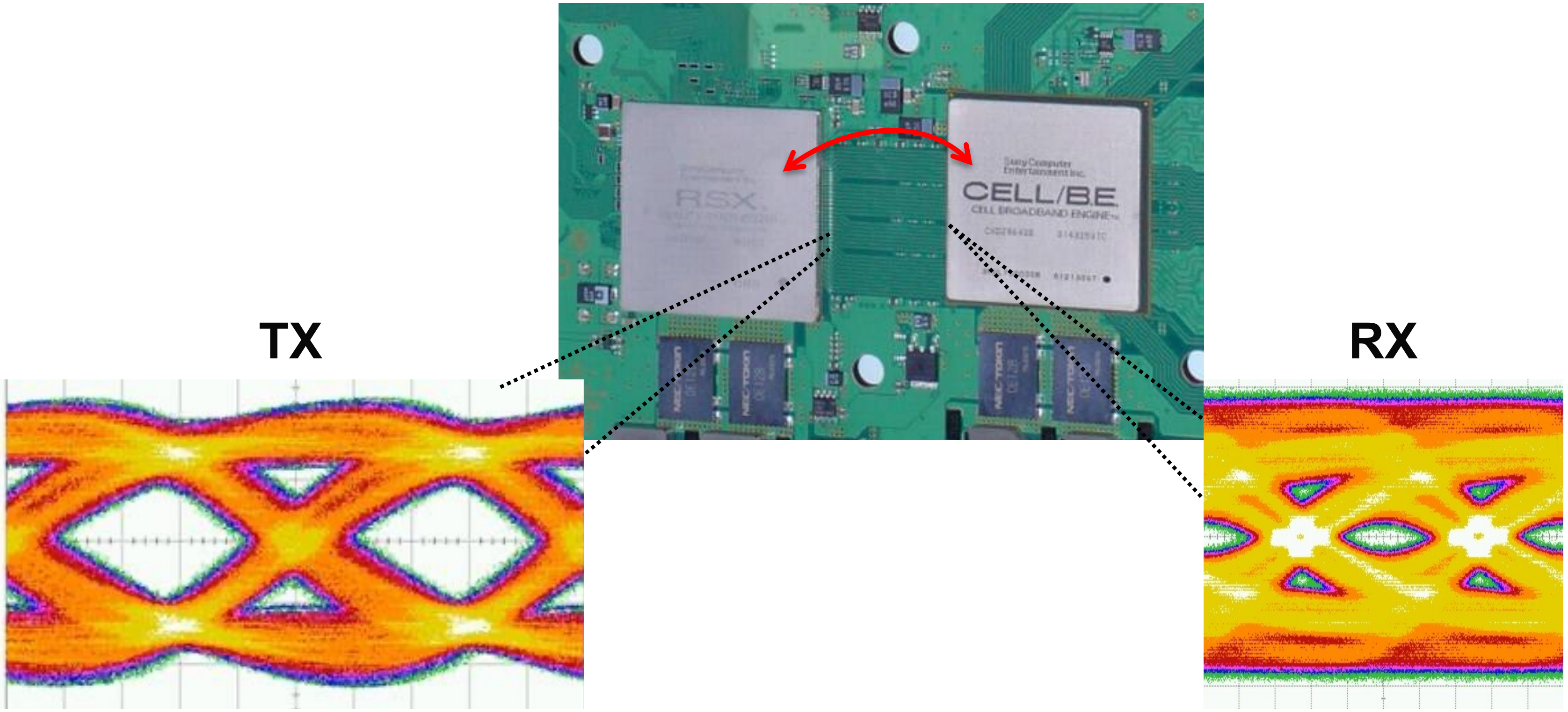
High-Speed Electrical Link System



[Palermo]

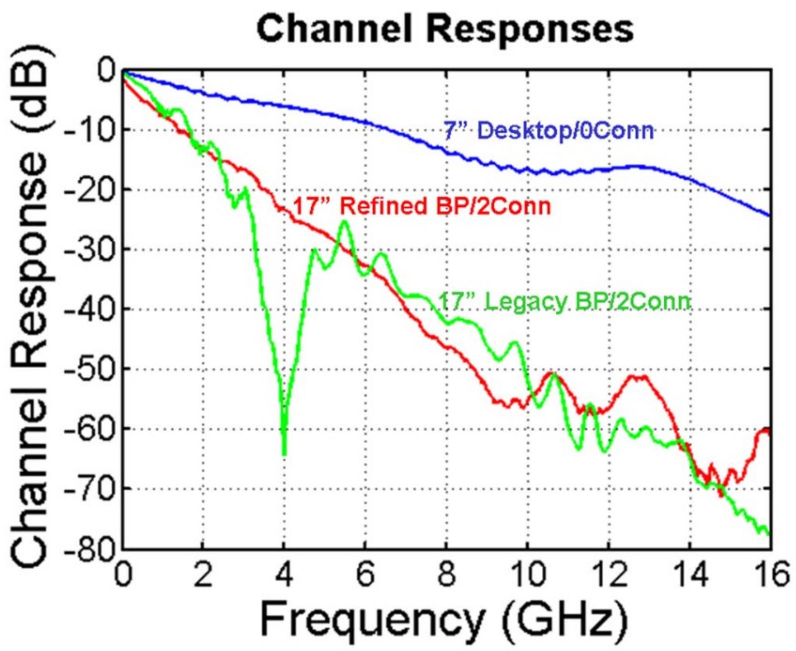
Wireline Interconnects

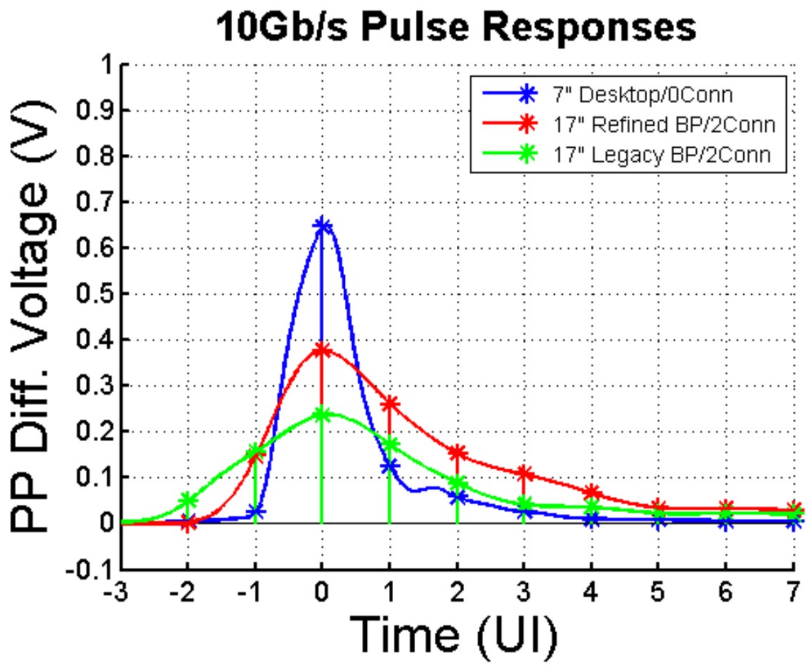
- Transmitter (Tx) + Channel + Receiver (Rx)
  - a.k.a SerDes (look at next slide)

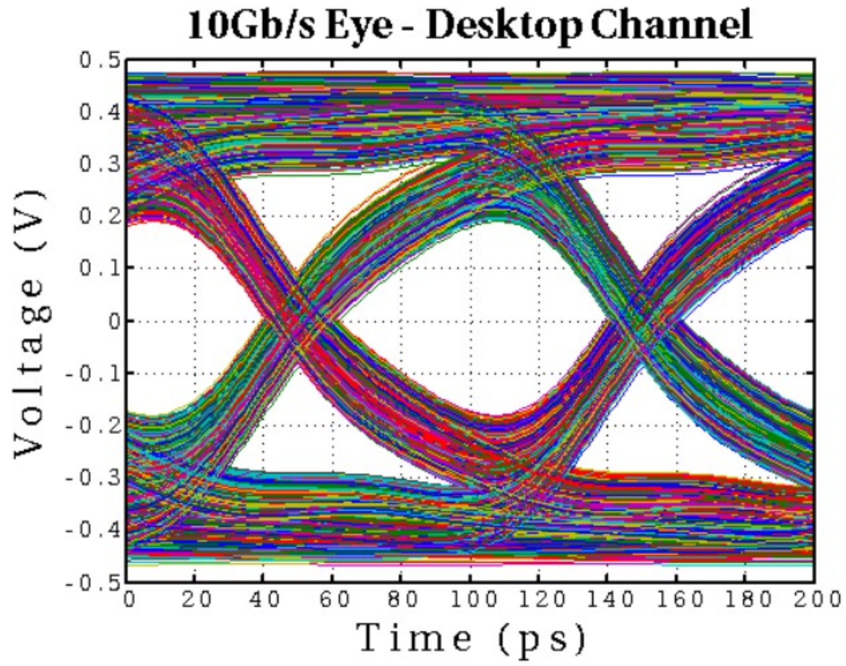


(Elad Alon)

Channel Example



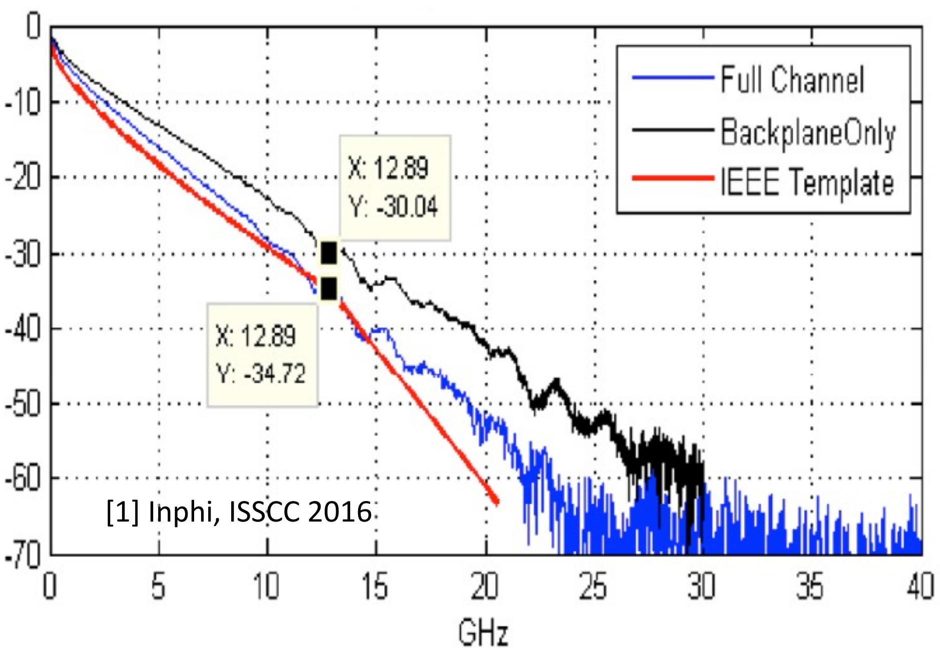




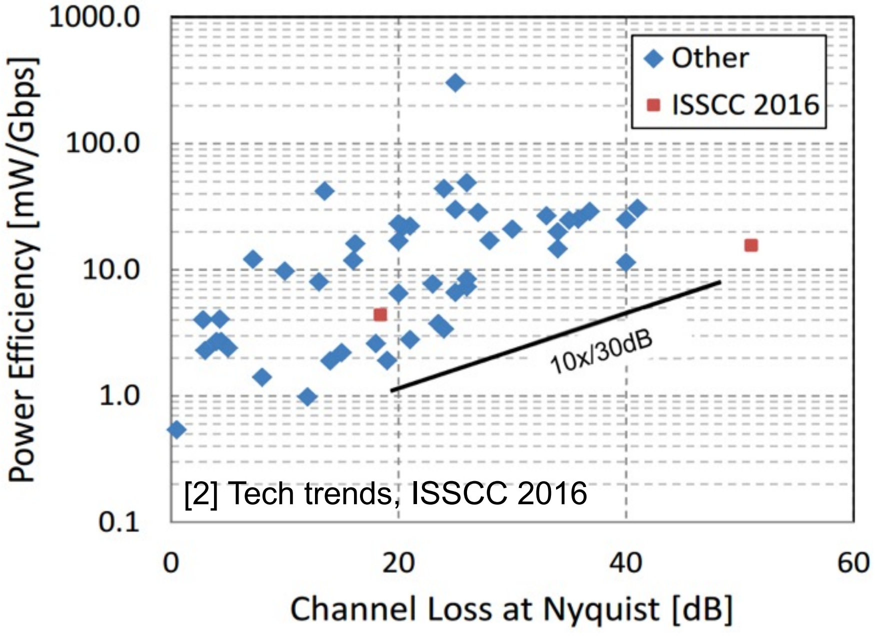
[Palermo]

Electrical Links Limitations

Electrical Backplane Channel Loss [1]

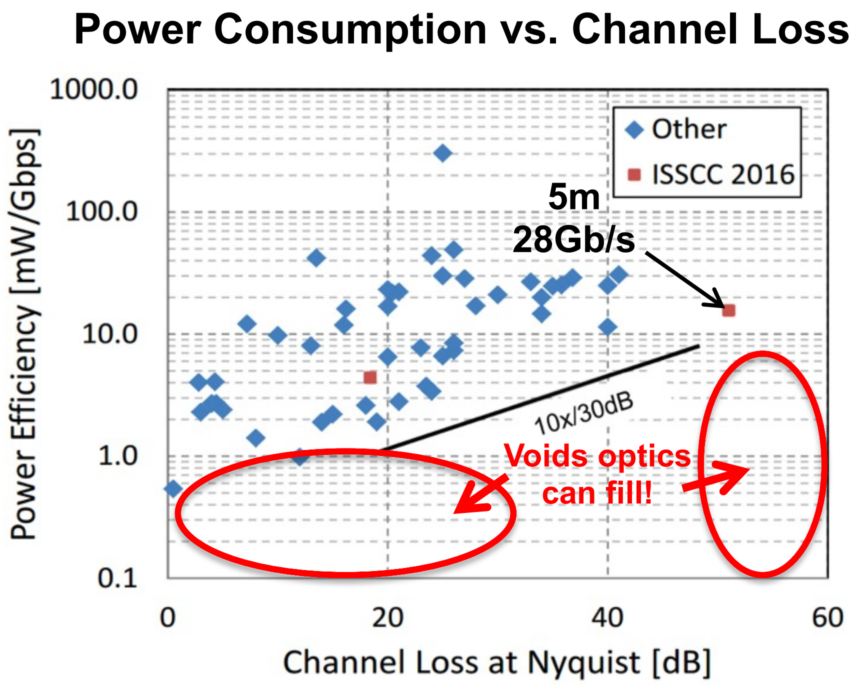


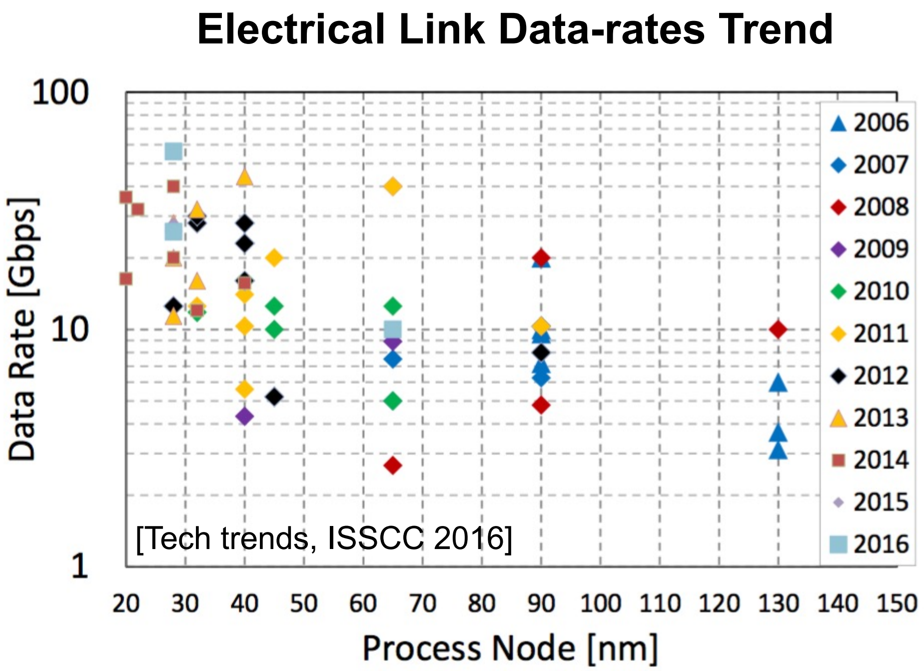
Power Consumption vs. Channel Loss [2]



- High data rate → High channel loss → High transceiver power
- **10 pJ/bit** with -40 dB channel loss at Nyquist frequency

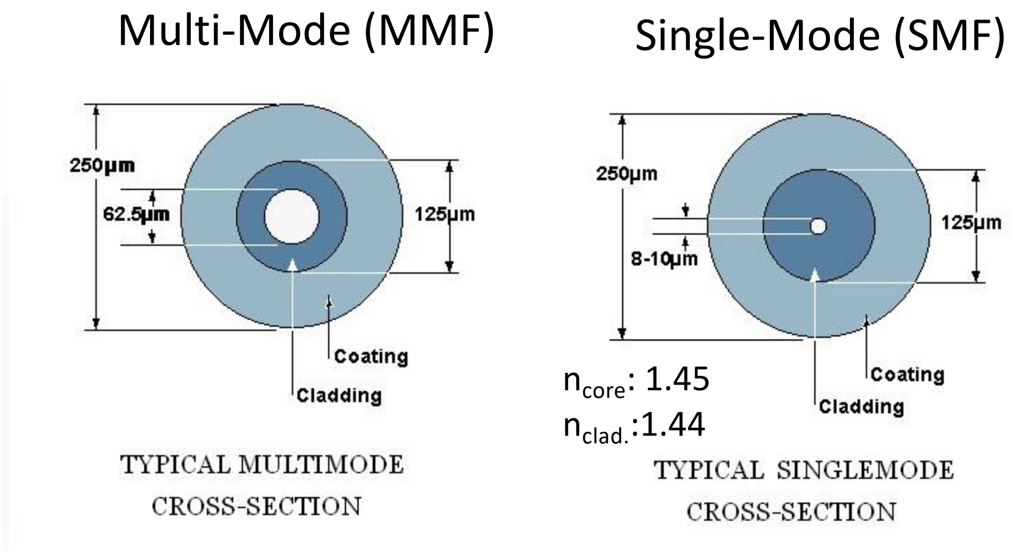
Electrical Links Limitations

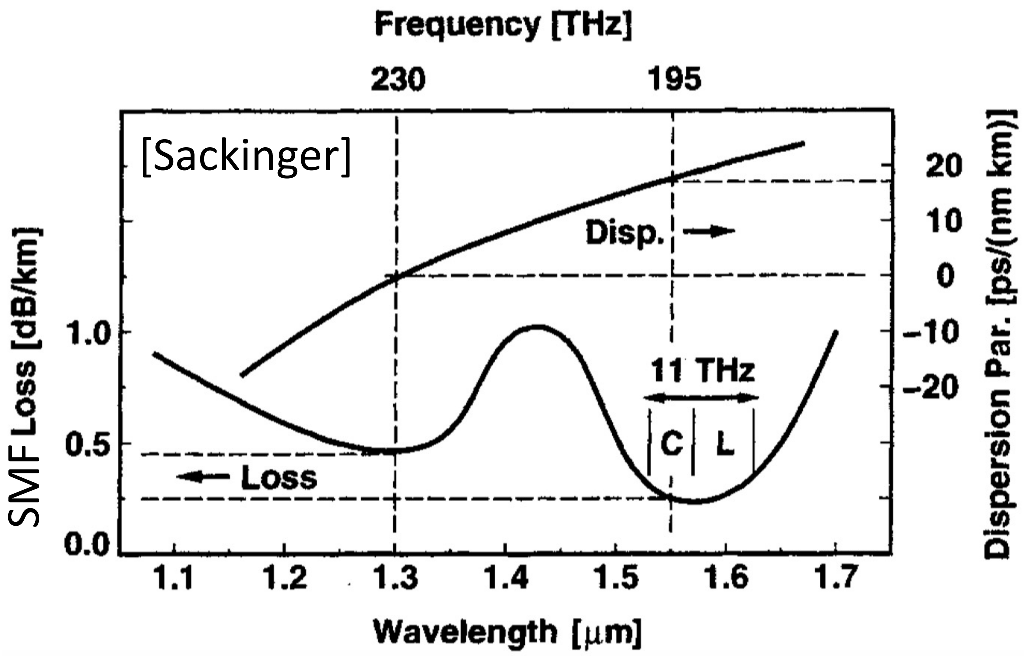




- Higher data rates & Longer channels ➔ Higher channel loss
- Moore’s law !? …
- **Optical links can break this barrier!**

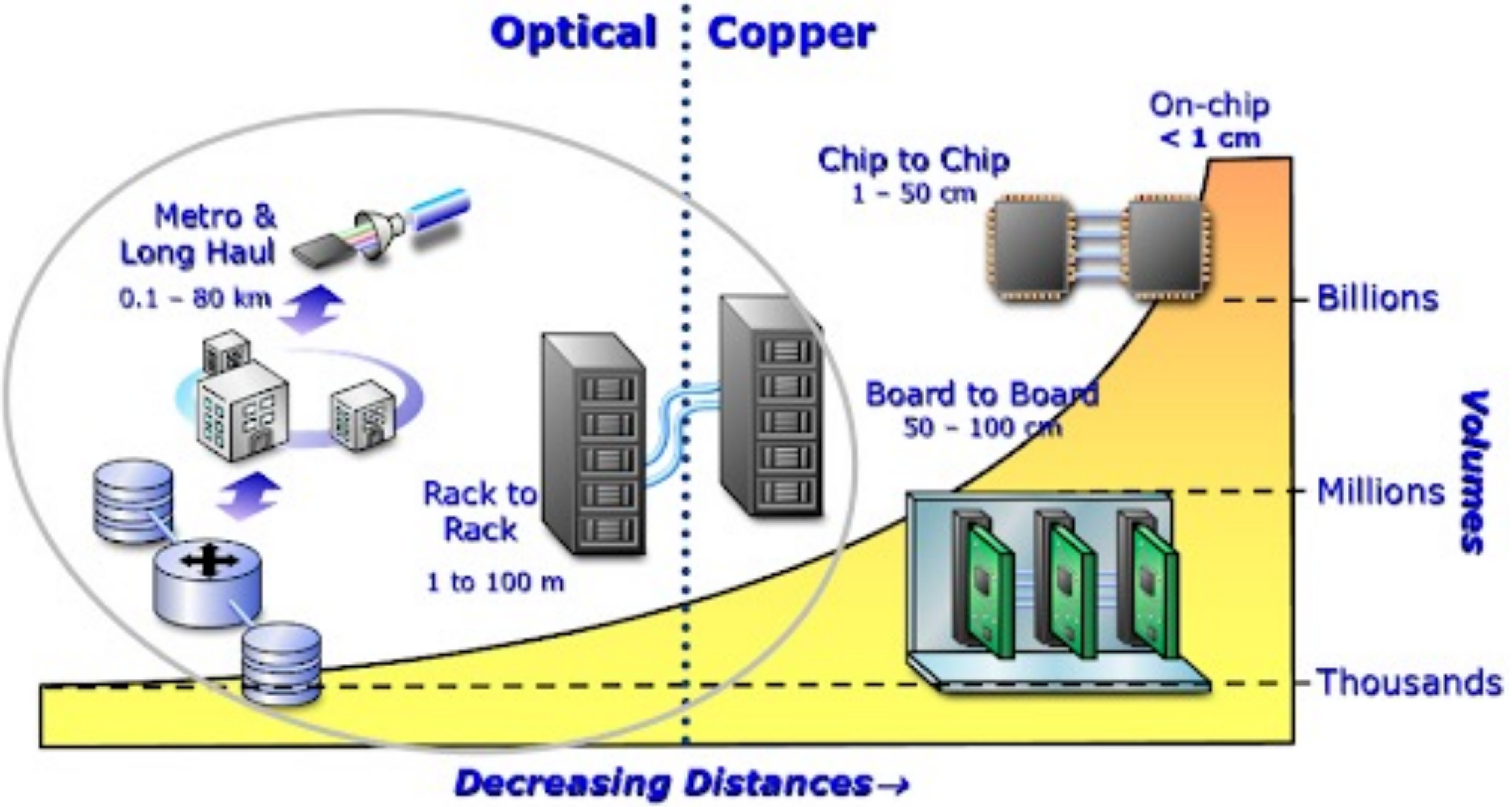
Fiber Optics





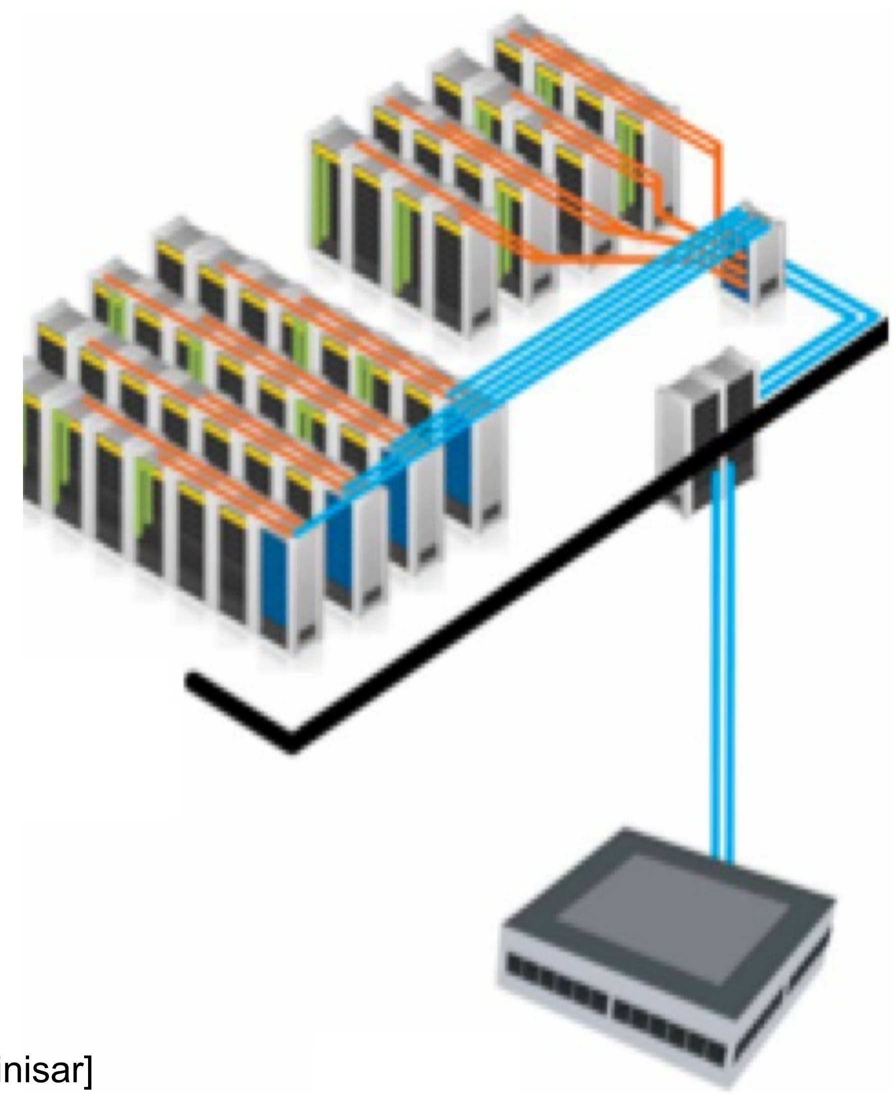
- Multi-mode vs. Single-mode fibers
  - Dispersion, Cost, …
  - MMF for short (< 300m) & SMF for longer distances
- Lowest fiber losses: *1310nm (O-band) & 1550nm (C-band)*: ~0.1db/km!
  - 1550nm for long-range communication (tele-communication)

Interconnects



Source: Prof. John Bowers

Optical Links

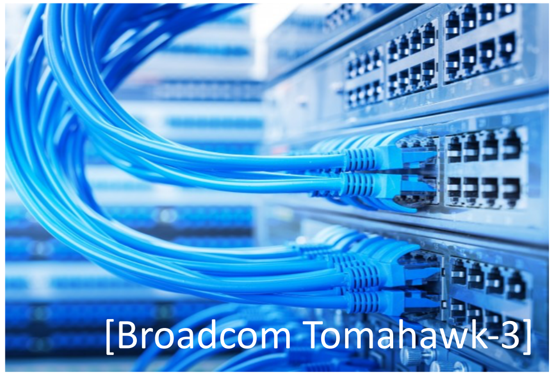


[Finisar]

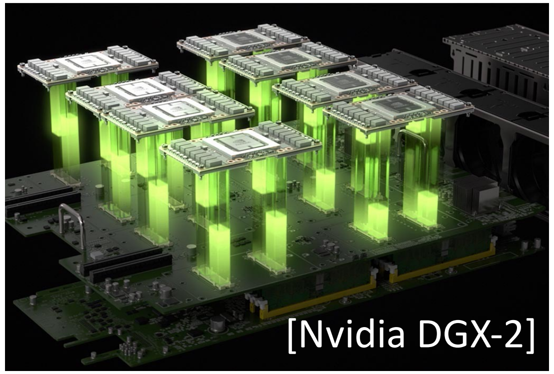
As of 2018:

Long-span Inter-building	40G → 100G → **200G/400G** → **Tb/s**	
2km/metro	Single-mode Fiber	Optical
Inter-rack	40G → 100G → **200G/400G** → **Tb/s**	
20m-2km 1-20 m	Single-mode Fiber Multi-mode Fiber	Optical
Intra-rack	10G → 25G → 56G → 100G/200G → **400G<**	
0.5-3 m	Copper Channels Multi-mode Fiber	Electrical/Optical

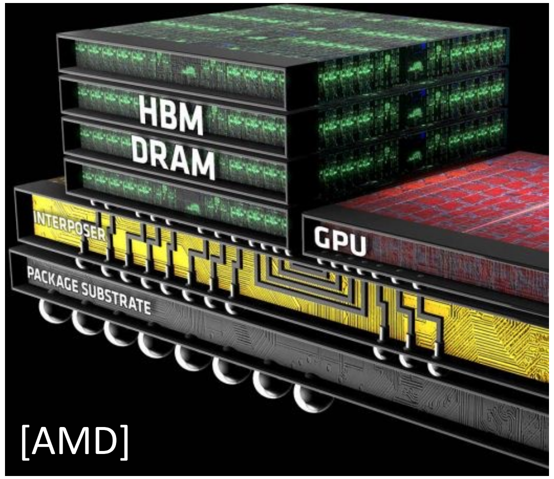
Emerging Needs for Photonics



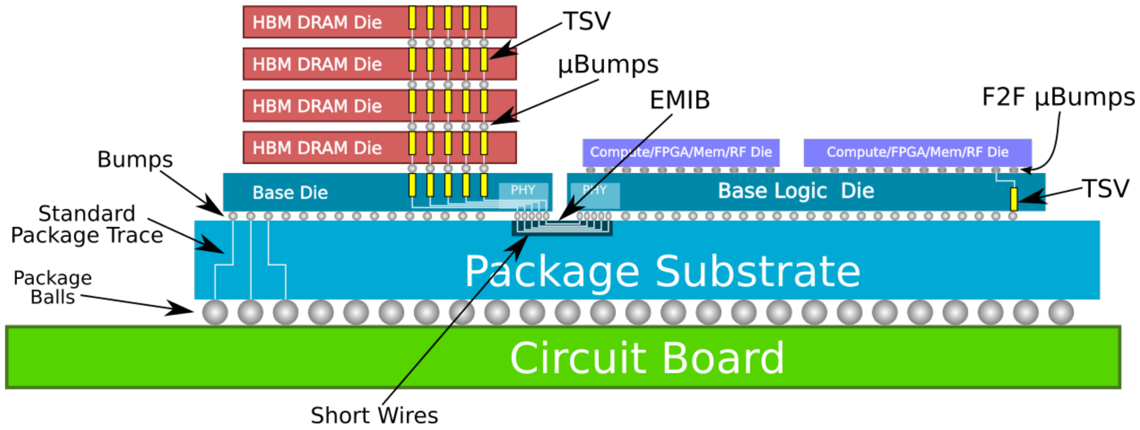
32x400 Gb/s



4.8Tb/s

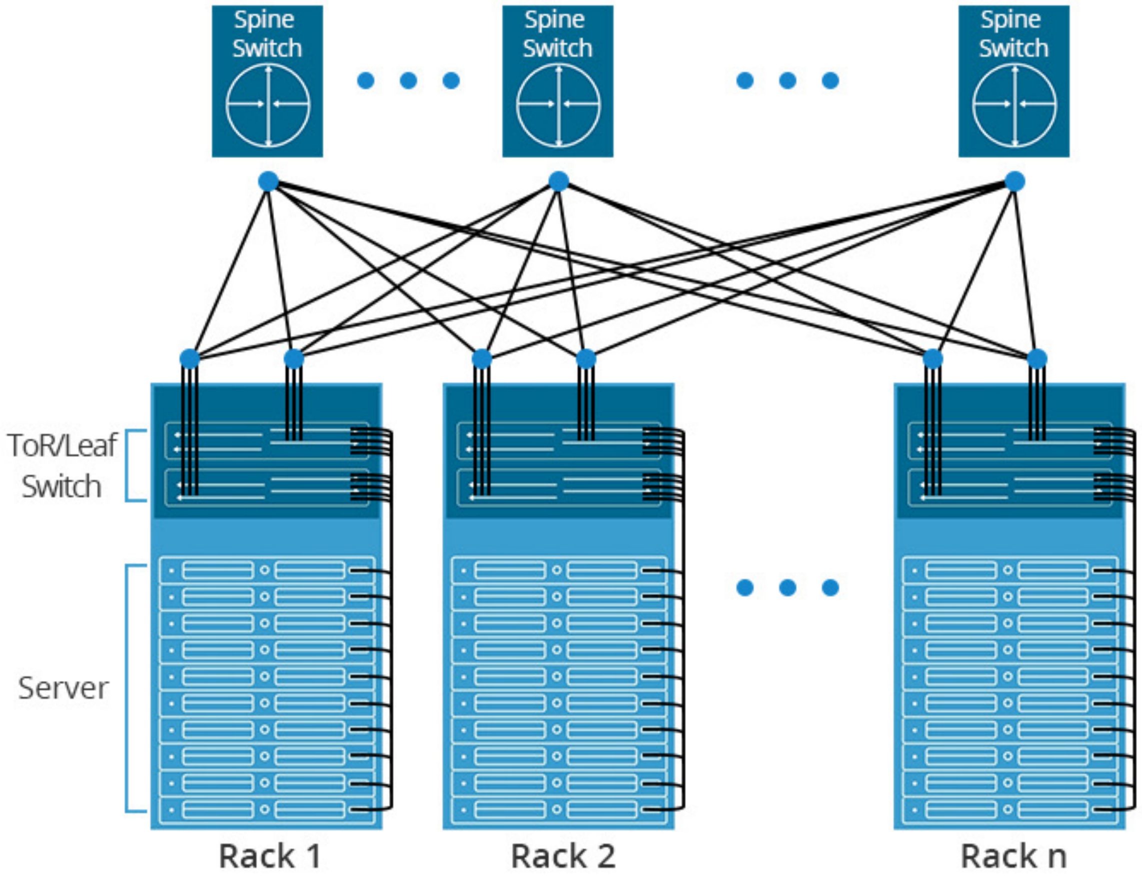


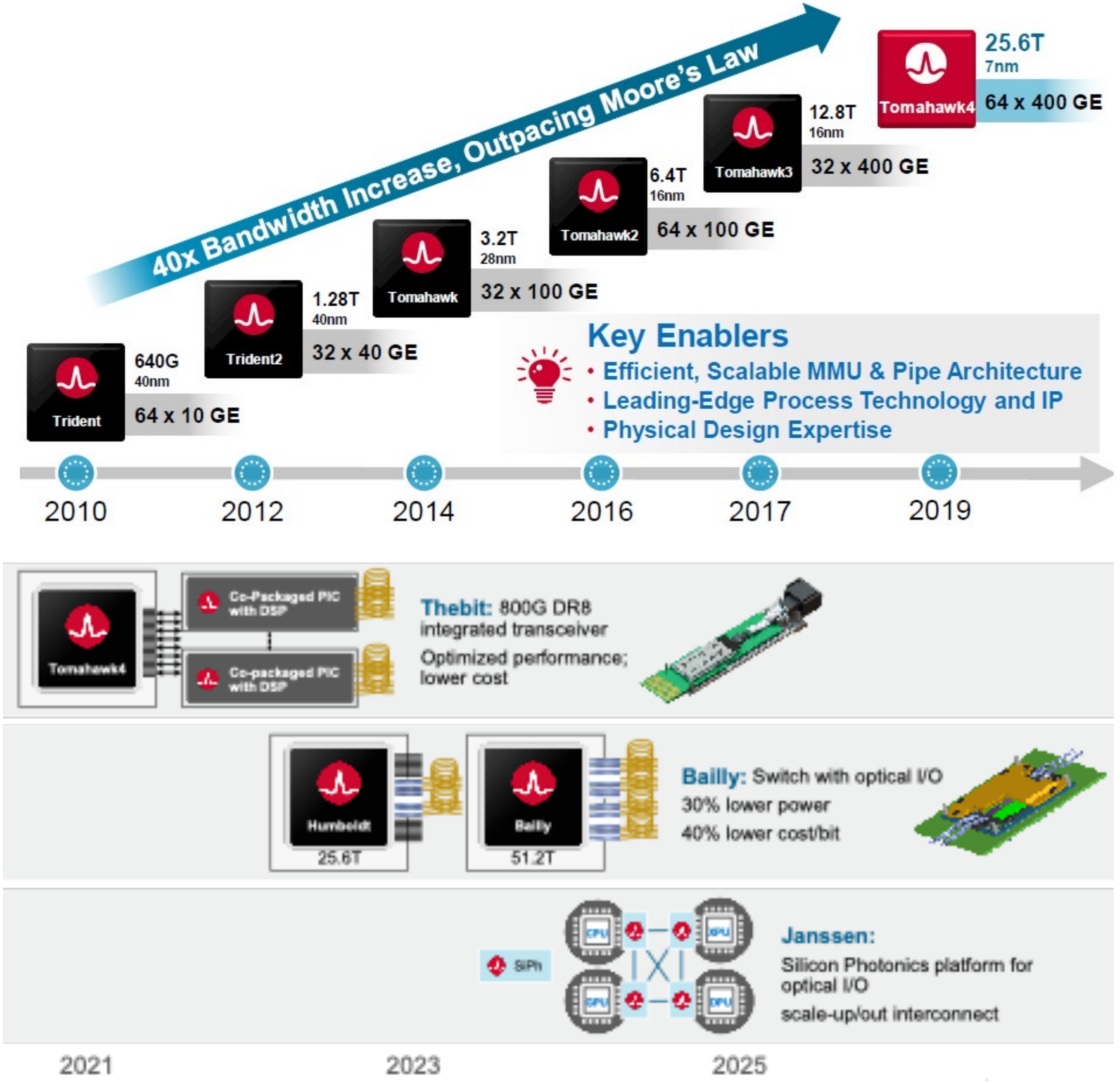
- **Demand for ultra-high data-rates!**
  - Heterogeneity: HBM, …
  - Advanced integration and packaging
- **Time for photonics to join …**
  - Energy-efficiency & High-bandwidth density



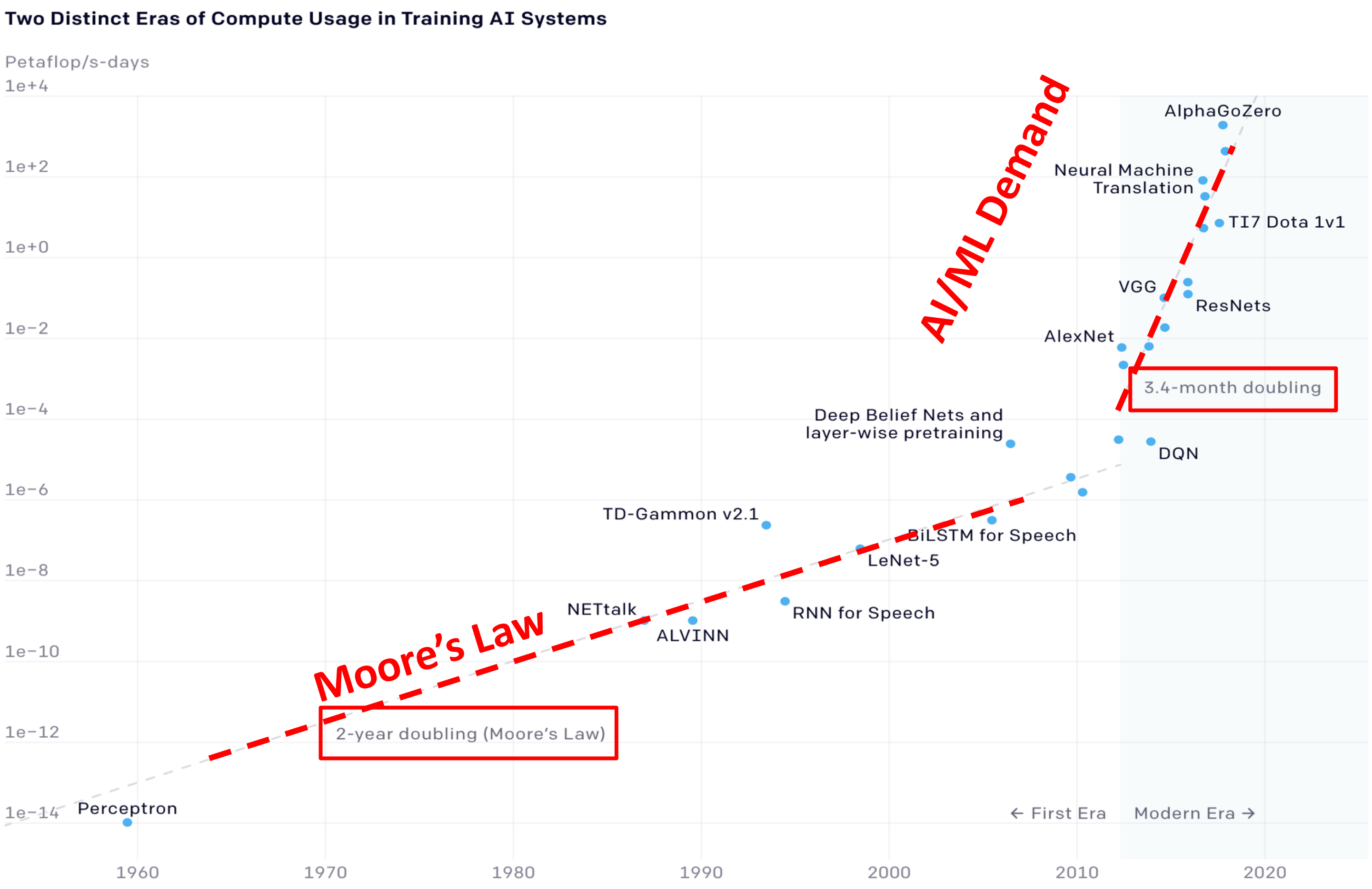
Example: Top-of-the-rack (ToR) Switch

The leaf switches are not connected to each other and spine switches only connect to the leaf switches (and an upstream core device).



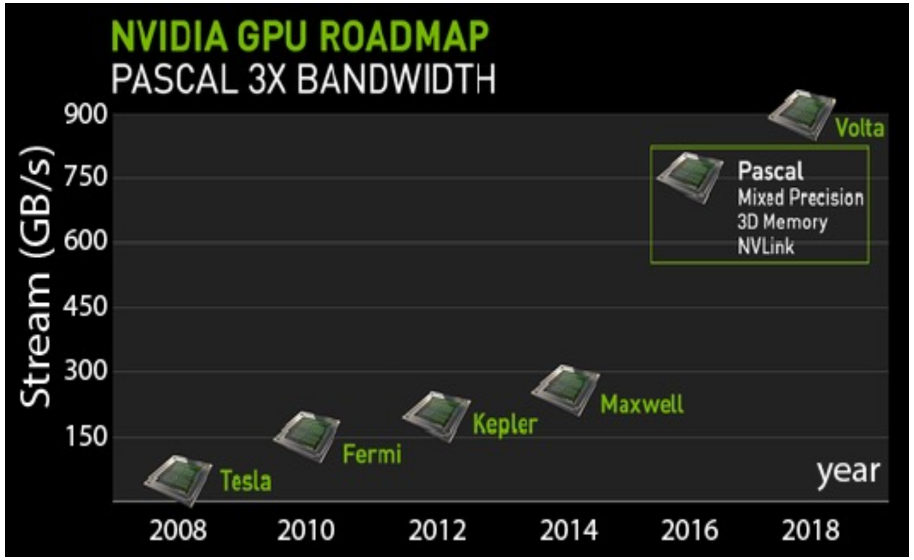


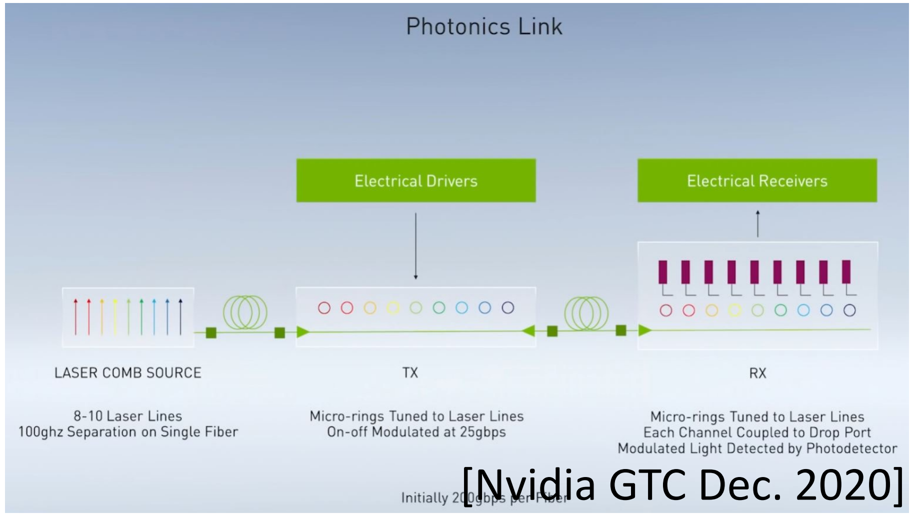
Emerging Demands by ML/AI



[Open AI]

GPU Memory BW Growth

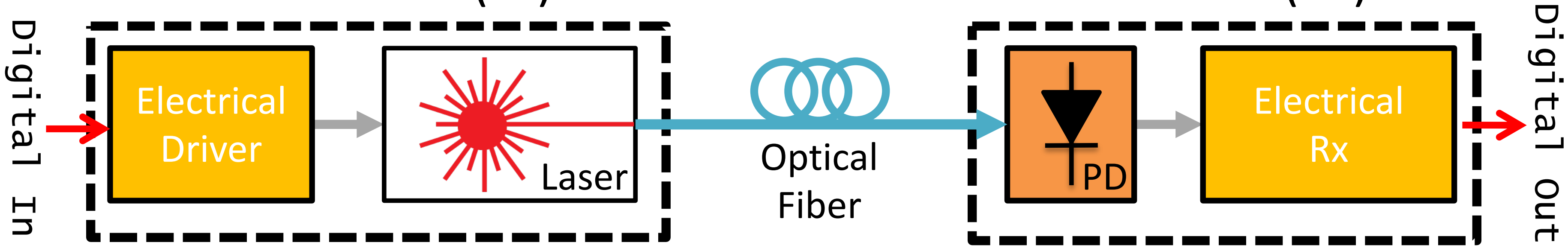




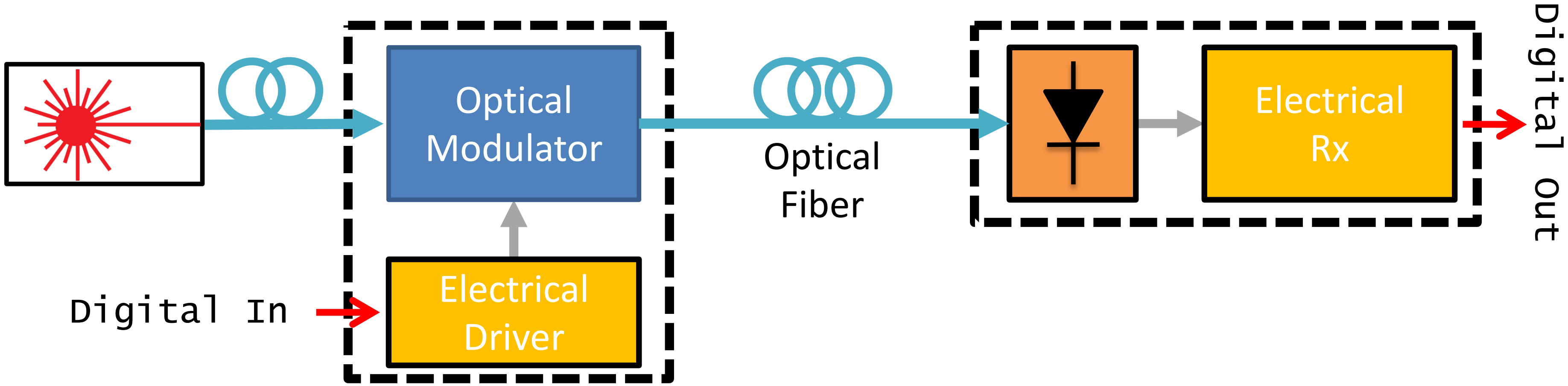
[Nvidia GTC Dec. 2020]

An Optical Link

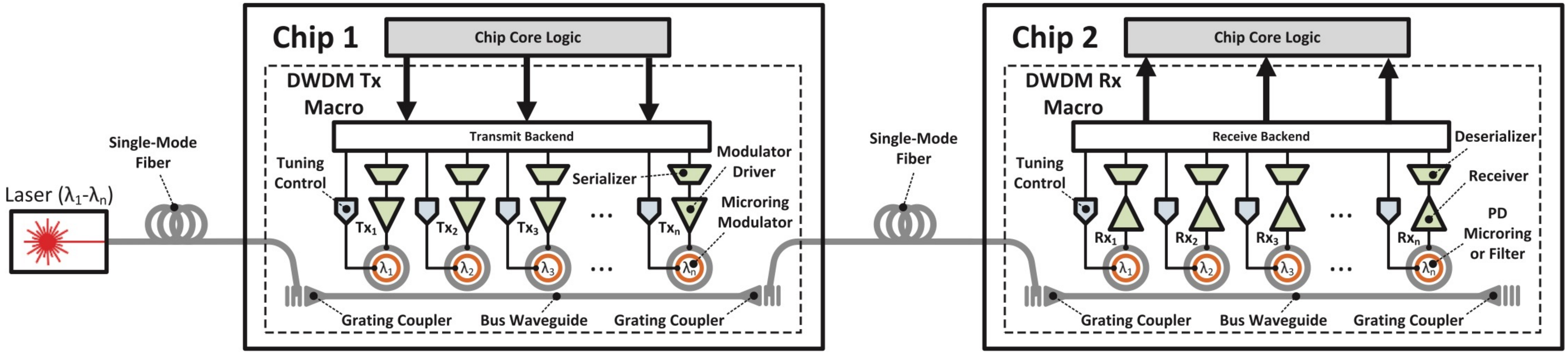
Directly Modulated Laser

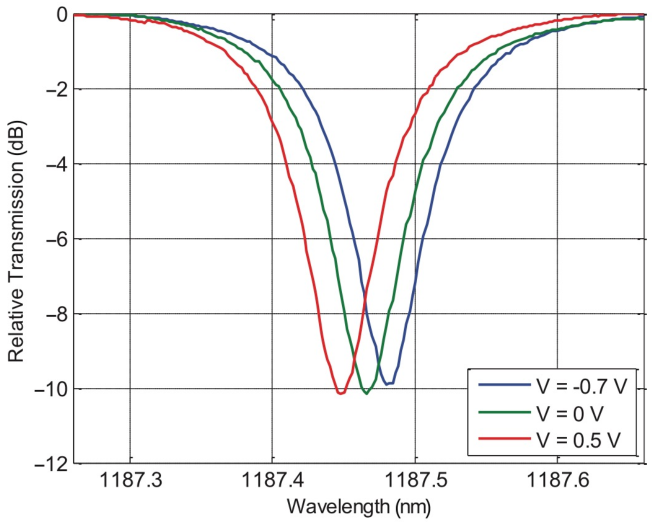


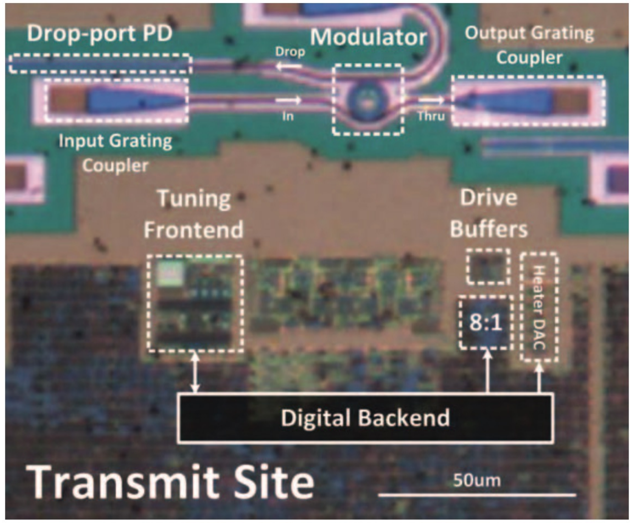
Externally Modulated Laser



MRM-based Optical I/O

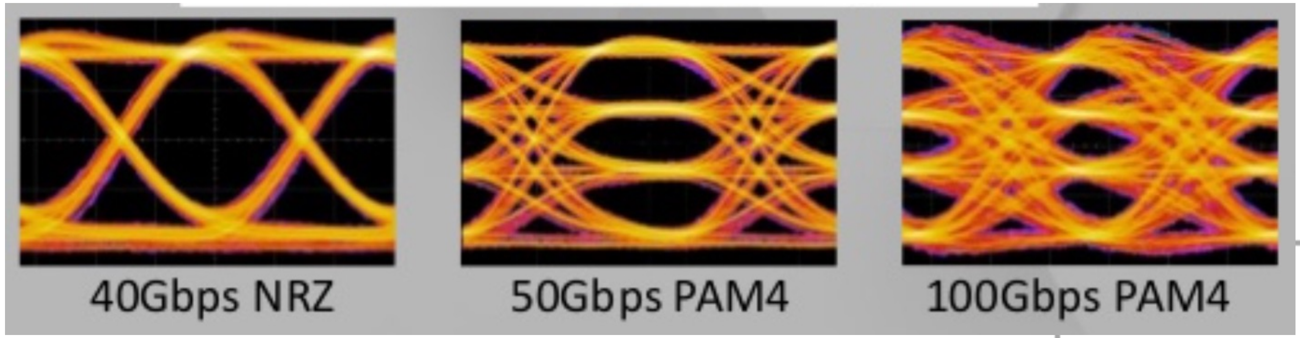




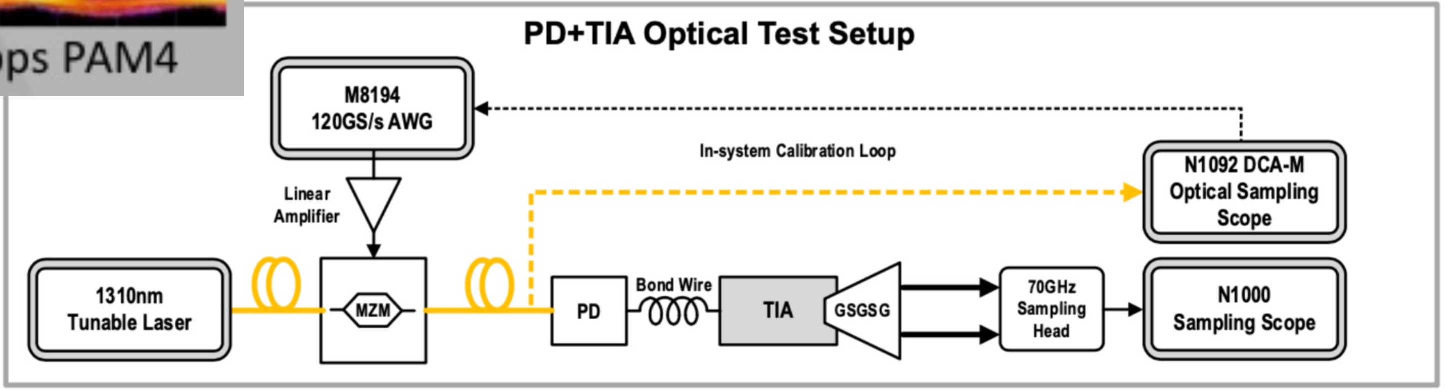


[Chen Sun, JSSC 2016]

Optical TRX Examples

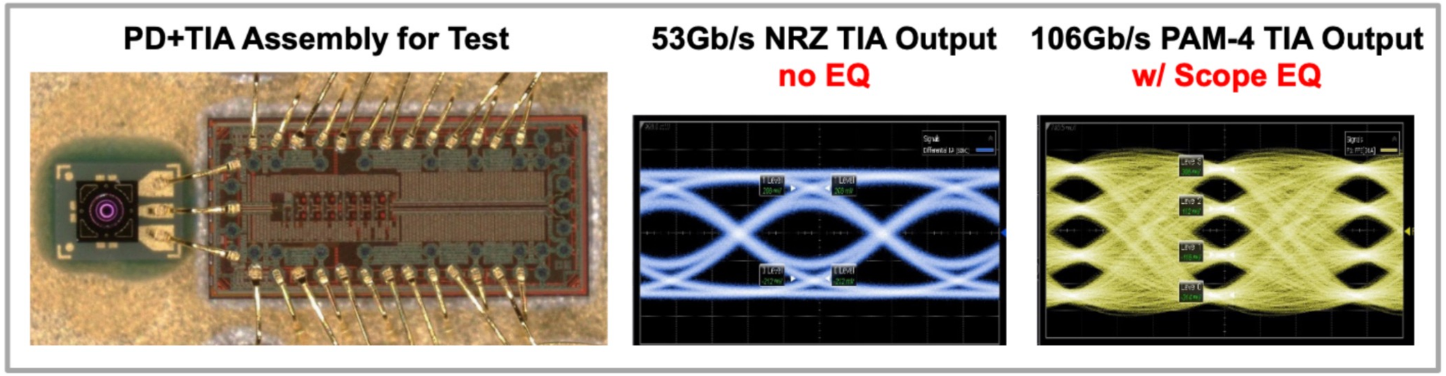


[Ayar Labs]



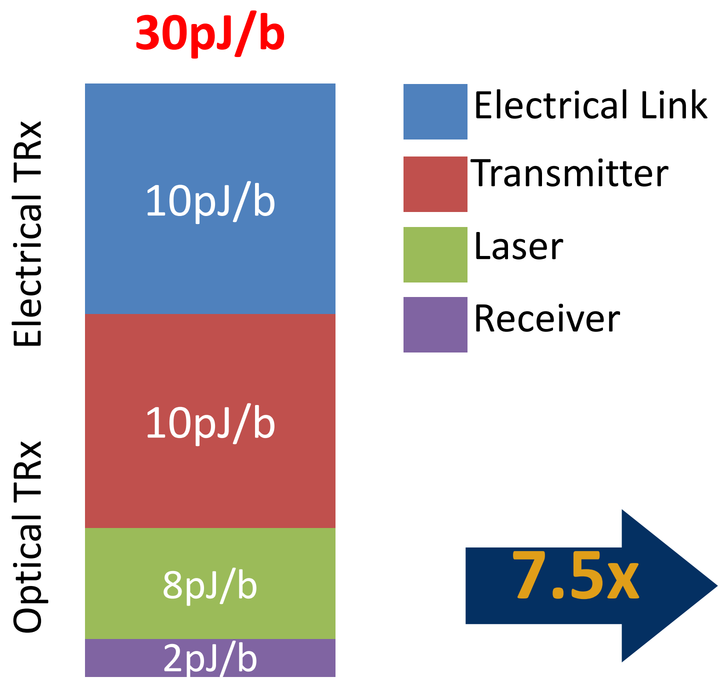
Bandwidth limitations!

Energy: 5-10pJ/b!



[intel ISSCC2021]

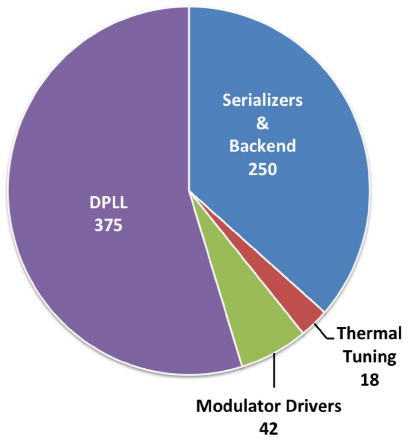
Next-generations of Optical I/O

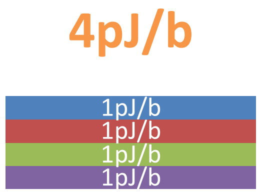


Commercial Pluggable Silicon-Photonic (SiPh)
< 100Gb/s/mm

7.5x

40Gb/s PAM-4 Tx (0.5pJ/b)
[Moazeni *et al.*, ISSCC17]

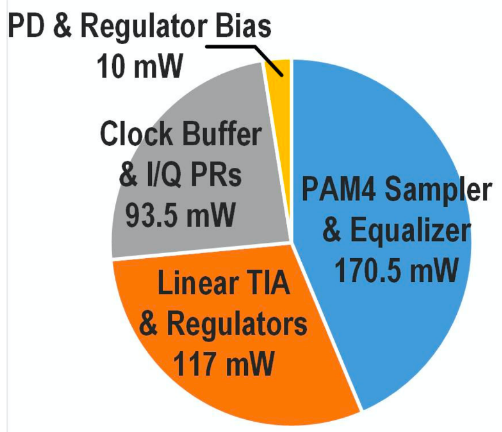




Co-packaged (45nm) Monolithic SiPh
> 0.5Tb/s/mm

>4x

100Gb/s PAM-4 Rx (3.9pJ/b)
[Li *et al.*, ISSCC21]



Monolithic Photonics in Sub-10nm (?)
Multi-Tb/s/mm