

EE 437/538B: Integrated Systems

Capstone/Design of Analog Integrated Circuits and Systems

Lecture 9: CDR & PLL

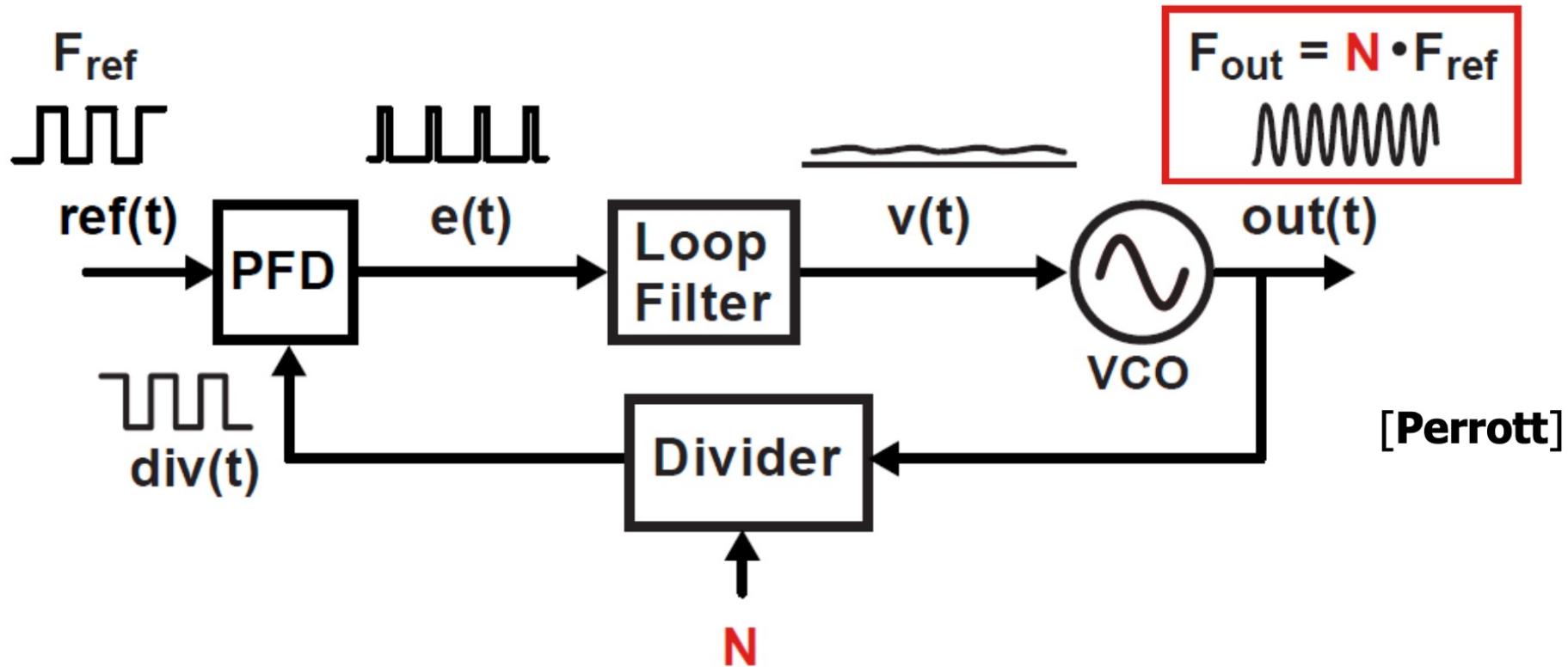
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Spring 2022

PLL, DLL, CDR

PLL Block Diagram



- A phase-locked loop (PLL) is a negative feedback system where an oscillator-generated signal is phase AND frequency locked to a reference signal

[Sam Palermo]

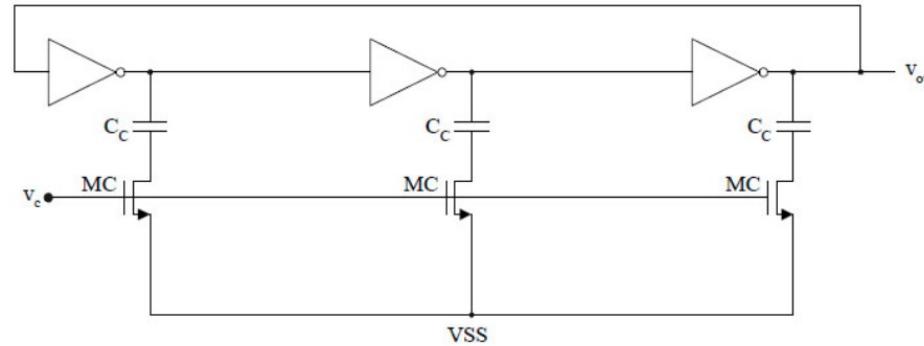
PLL Applications

- PLLs applications
 - Frequency synthesis
 - Multiplying a 100MHz reference clock to 10GHz
 - Skew cancellation
 - Phase aligning an internal clock to an I/O clock
 - Clock recovery
 - Extract from incoming data stream the clock frequency and optimum phase of high-speed sampling clocks
 - Modulation/De-modulation
 - Wireless systems
 - Spread-spectrum clocking

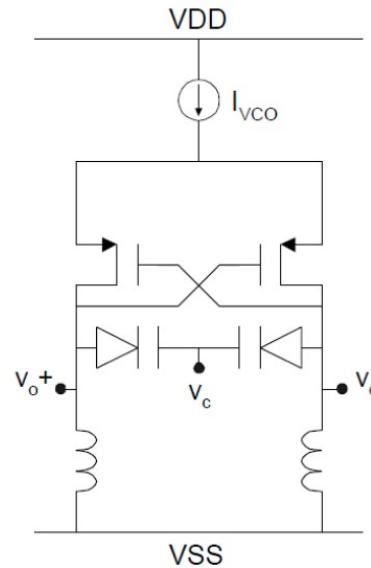
[Sam Palermo]

Voltage-Controlled Oscillators (VCO)

- Ring Oscillator
 - Easy to integrate
 - Wide tuning range (5x)
 - Higher phase noise

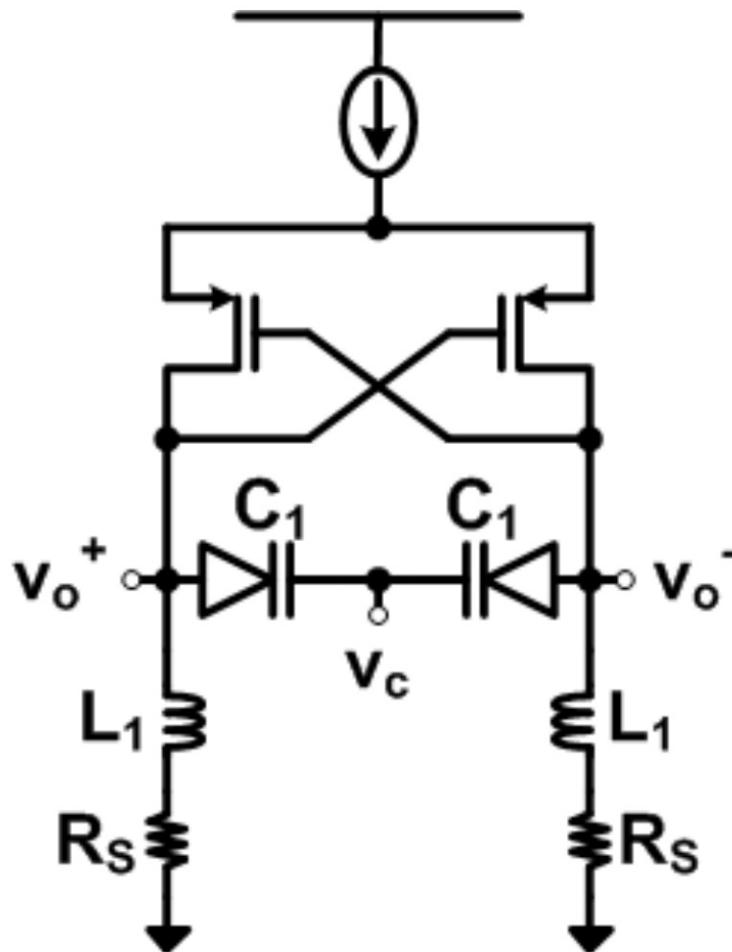


- LC Oscillator
 - Large area
 - Narrow tuning range (20-30%)
 - Lower phase noise

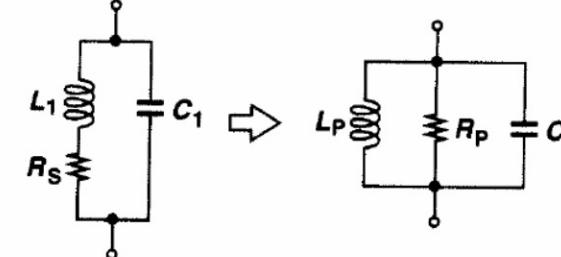


[Sam Palermo]

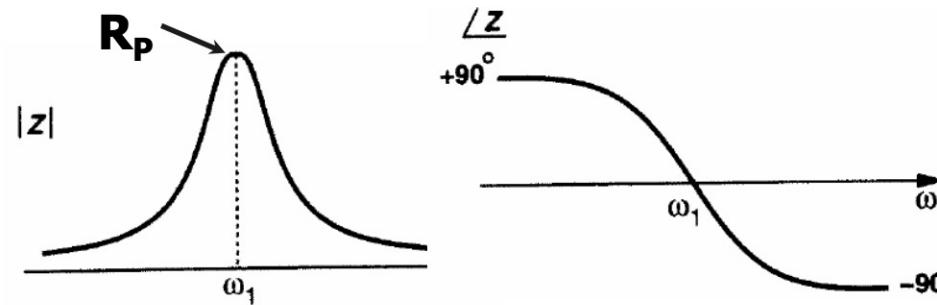
LC Oscillator Example



- Transforming the series loss resistor of the inductor to an equivalent parallel resistance



$$L_P = L_1 \left(1 + \frac{R_s^2}{L_1^2 \omega^2} \right), \quad C_P = C_1, \quad R_P \approx \frac{L_1^2 \omega^2}{R_s}$$

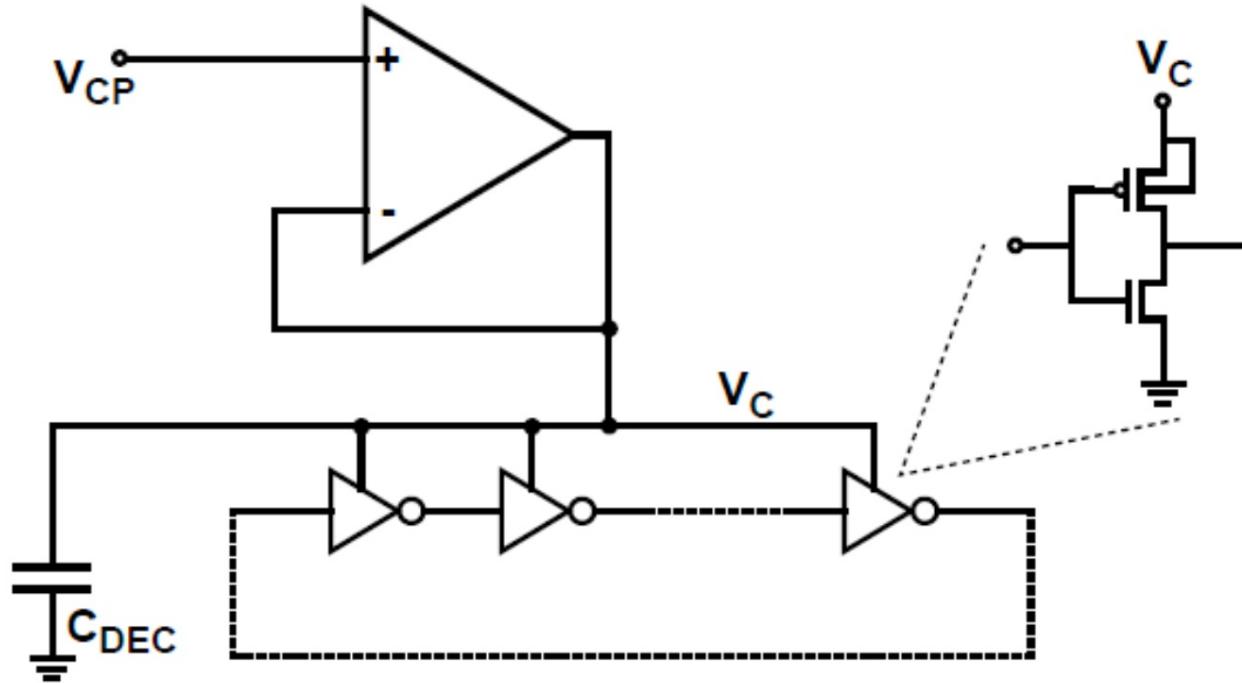


$$\omega_1 = \frac{1}{\sqrt{L_P C_P}}$$

[Razavi]

[Sam Palermo]

Supply-Tuned Ring Oscillator



[Sidiropoulos VLSI 2000]

$$T_{VCO} = 2nT_D \approx \frac{2nC_{stage}}{\beta(V_c - V_{th})}$$

$$K_{VCO} = \frac{\partial f_{VCO}}{\partial V_c} = \frac{\beta}{2nC_{stage}}$$

[Sam Palermo]

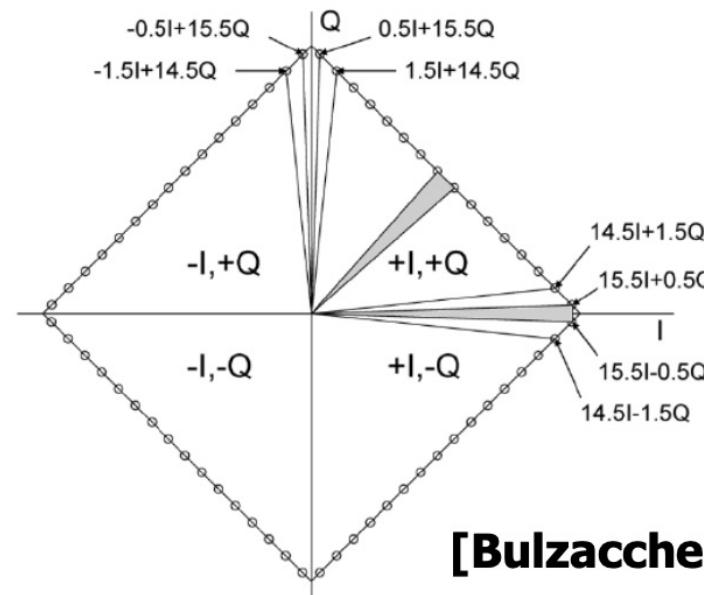
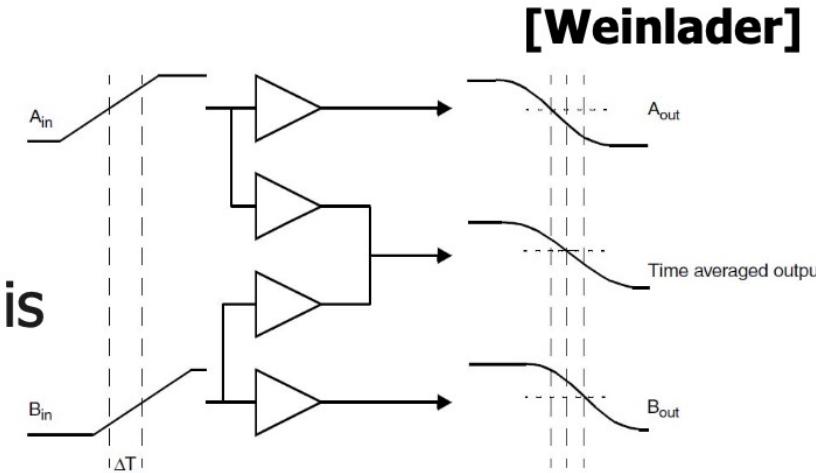
Phase Adjustment

- Many possibilities...
 - DLL vs. PLL
 - VCO vs. VCDL
 - Digital vs. analog
 - Etc.
- All boil down to adjusting delay, frequency, or both
 - More in a few weeks

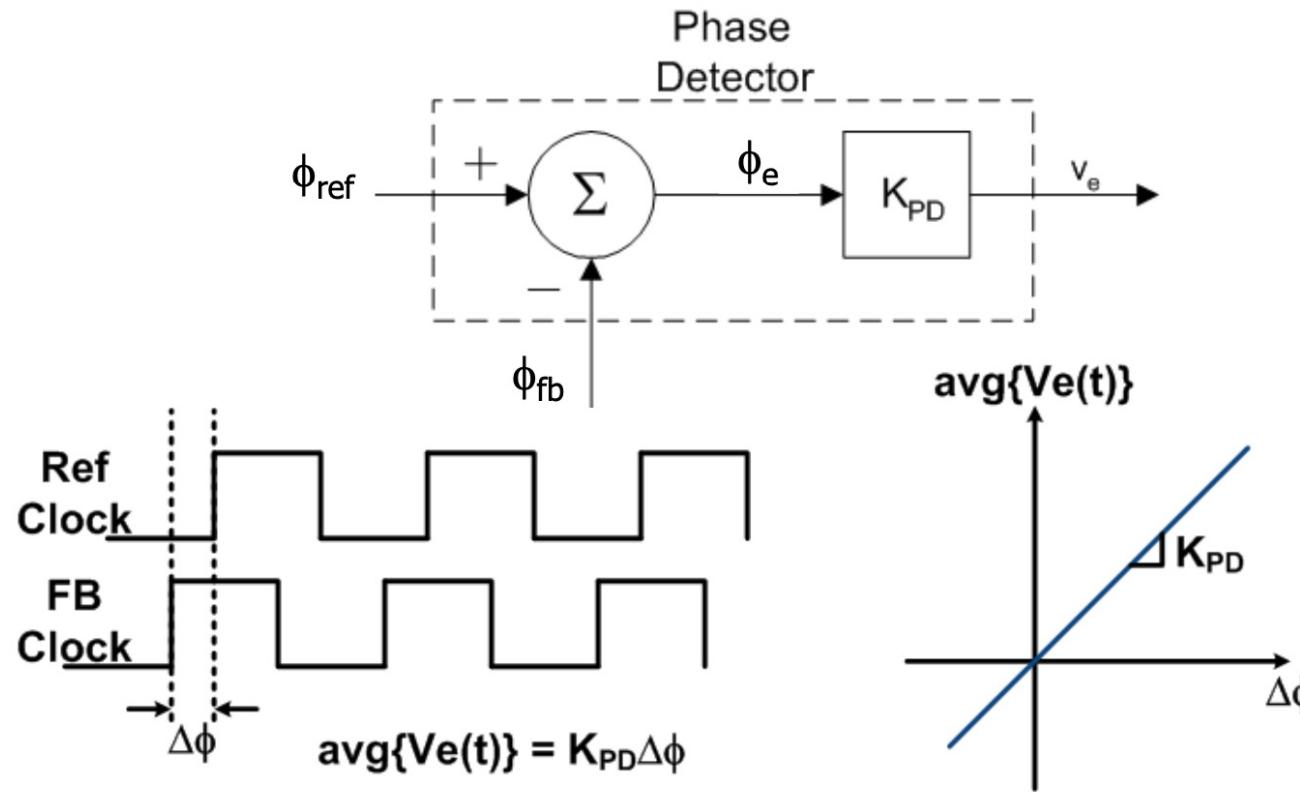
[Elad Alon]

Phase Interpolators

- Phase interpolators realize digital-to-phase conversion (DPC)
- Produce an output clock that is a weighted sum of two input clock phases
- Common circuit structures
 - Tail current summation interpolation
 - Voltage-mode interpolation
- Interpolator code mapping techniques
 - Sinusoidal
 - Linear



Phase Detector

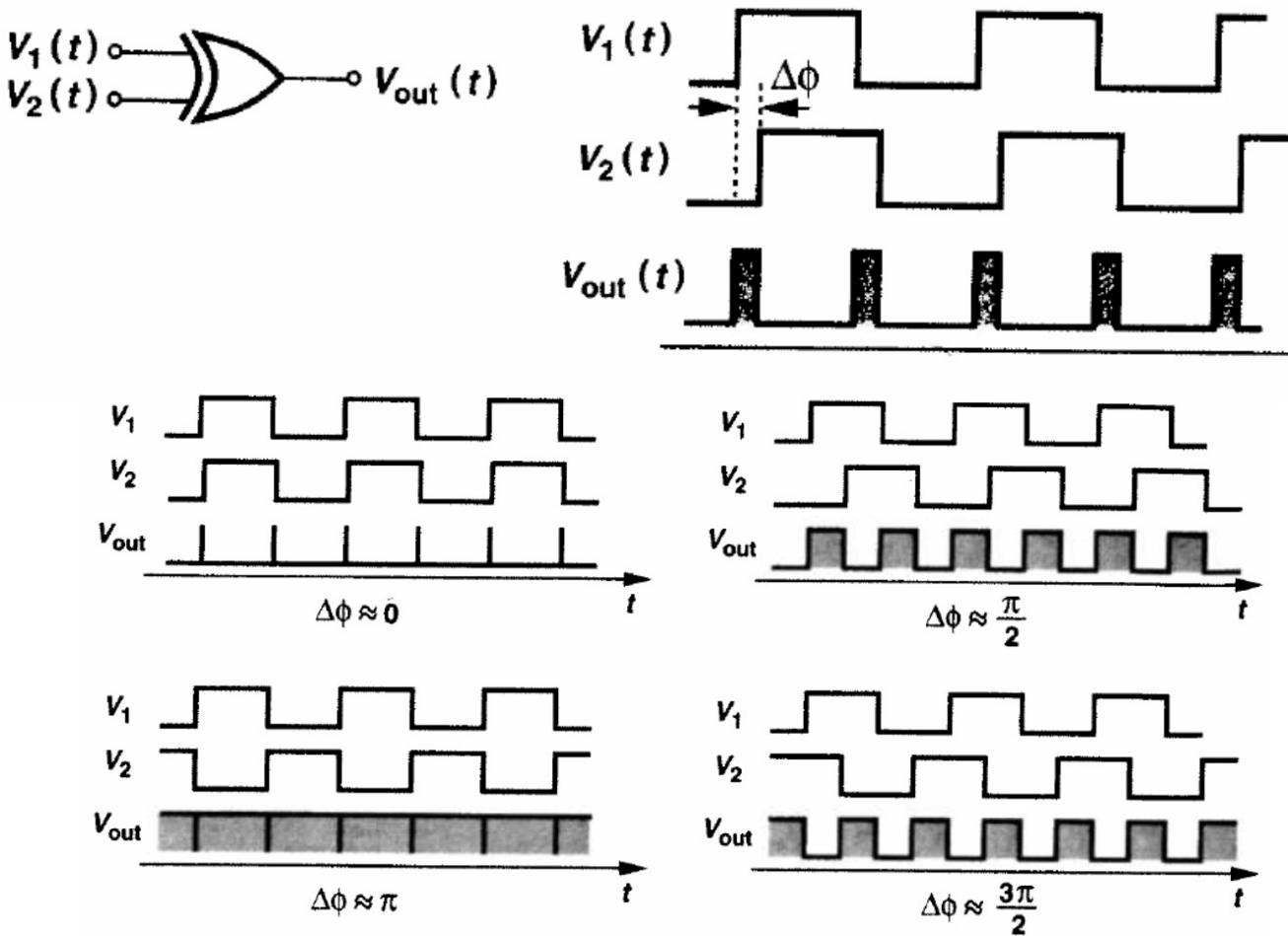


- Detects phase difference between feedback clock and reference clock
- The loop filter will filter the phase detector output, thus to characterize phase detector gain, extract average output voltage (or current for charge-pump PLLs)

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[Sam Palermo]

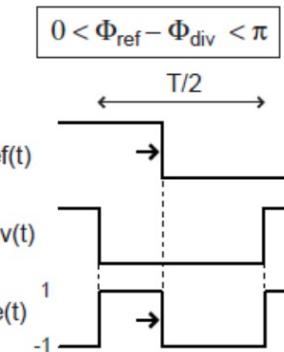
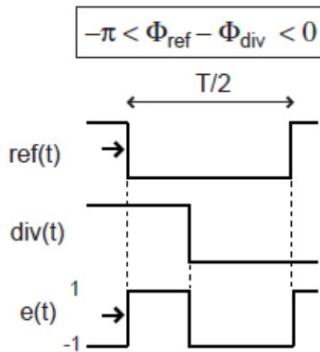
XOR Phase Detector



- Sensitive to clock duty cycle

[Sam Palermo]

XOR Phase Detector

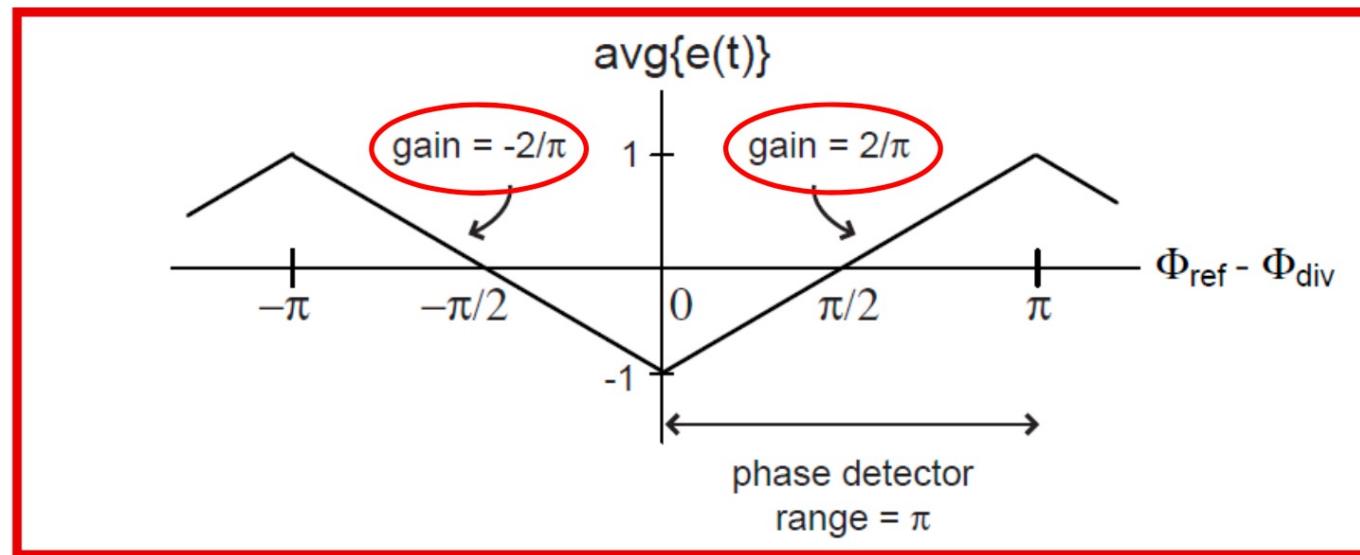


Width is same for both leading and lagging phase difference!

$$W = -\left(\frac{\Phi_{\text{ref}} - \Phi_{\text{div}}}{\pi}\right)T/2$$

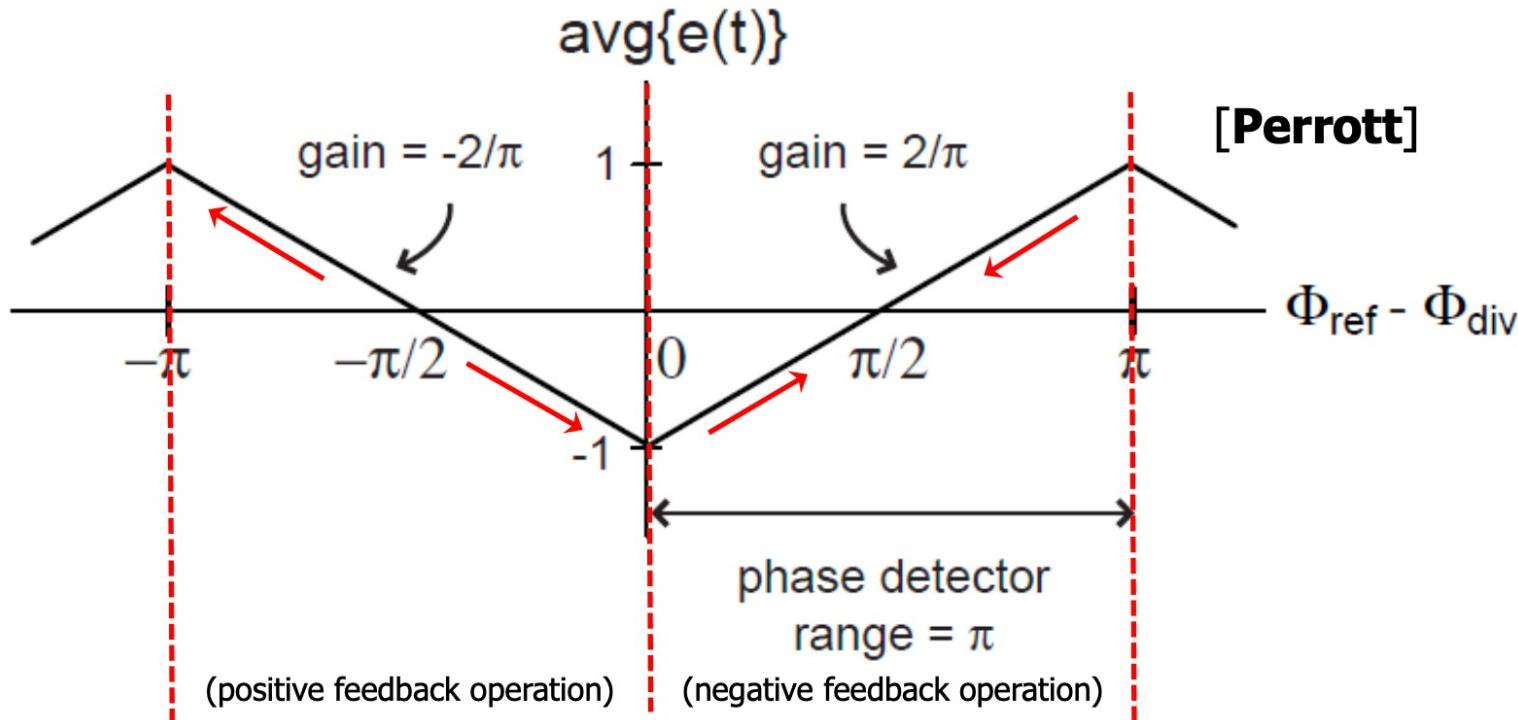
$$W = \left(\frac{\Phi_{\text{ref}} - \Phi_{\text{div}}}{\pi}\right)T/2$$

[Perrott]



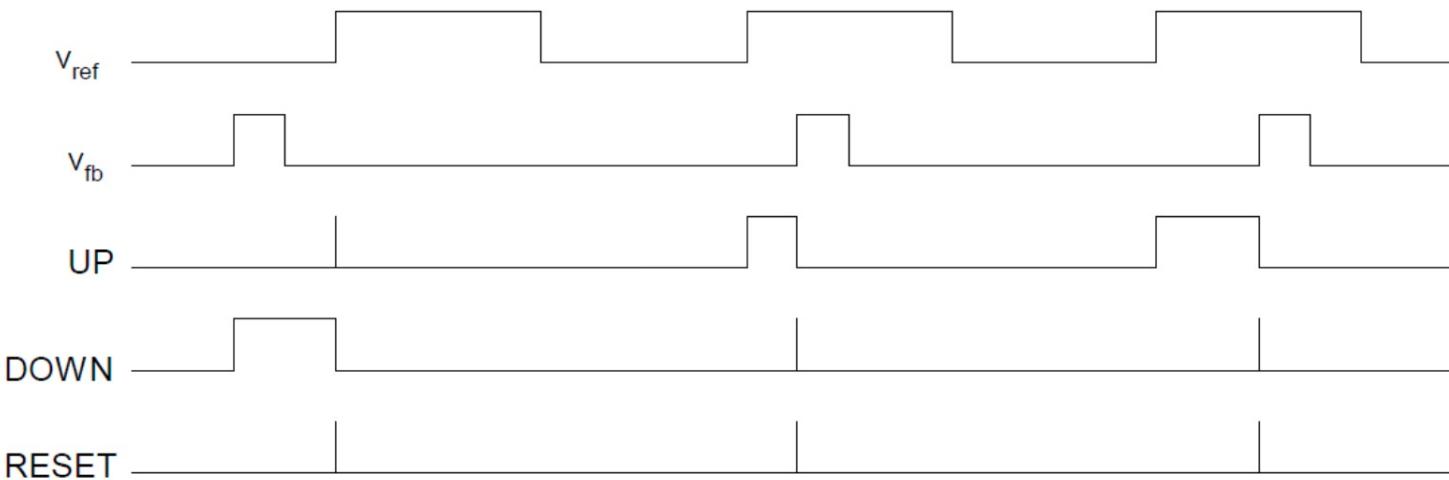
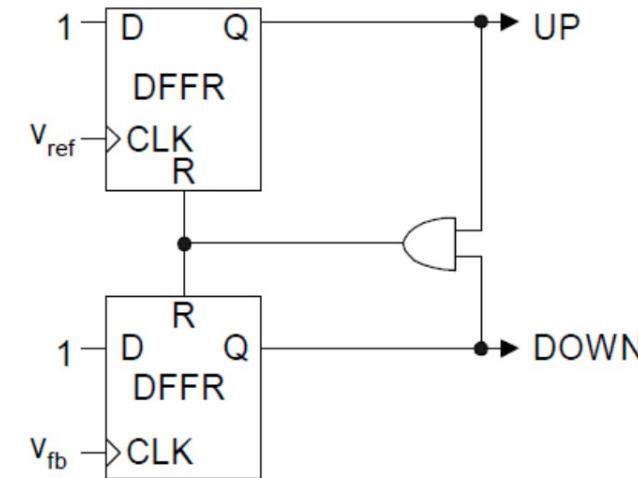
Cycle Slipping

- If there is a frequency difference between the input reference and PLL feedback signals the phase detector can jump between regions of different gain
 - PLL is no longer acting as a linear system



Phase Frequency Detector (PFD)

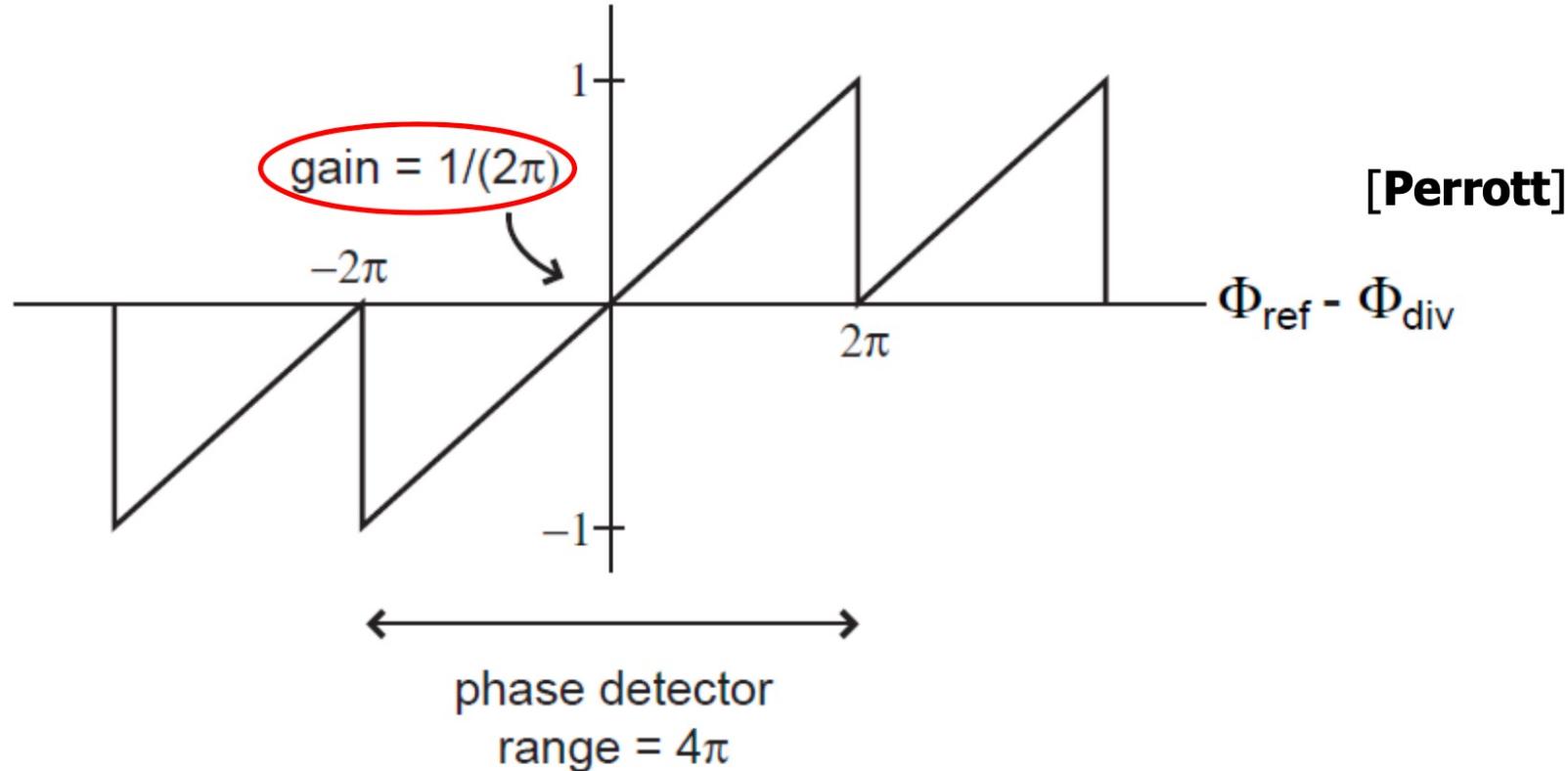
- Phase Frequency Detector allows for wide frequency locking range, potentially entire VCO tuning range
- 3-stage operation with UP and DOWN outputs
- Edge-triggered results in duty cycle insensitivity



PFD Transfer Characteristic

UP=1 & DN=-1

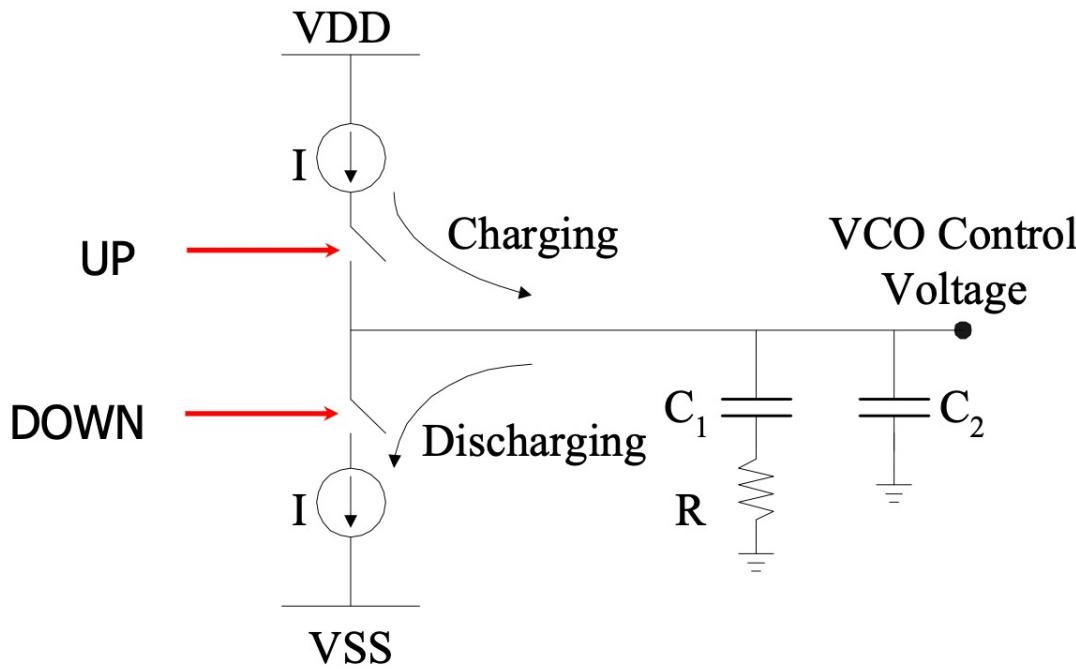
avg{e(t)}



- Constant slope and polarity asymmetry about zero phase allows for wide frequency range operation

[Sam Palermo]

Charge Pump



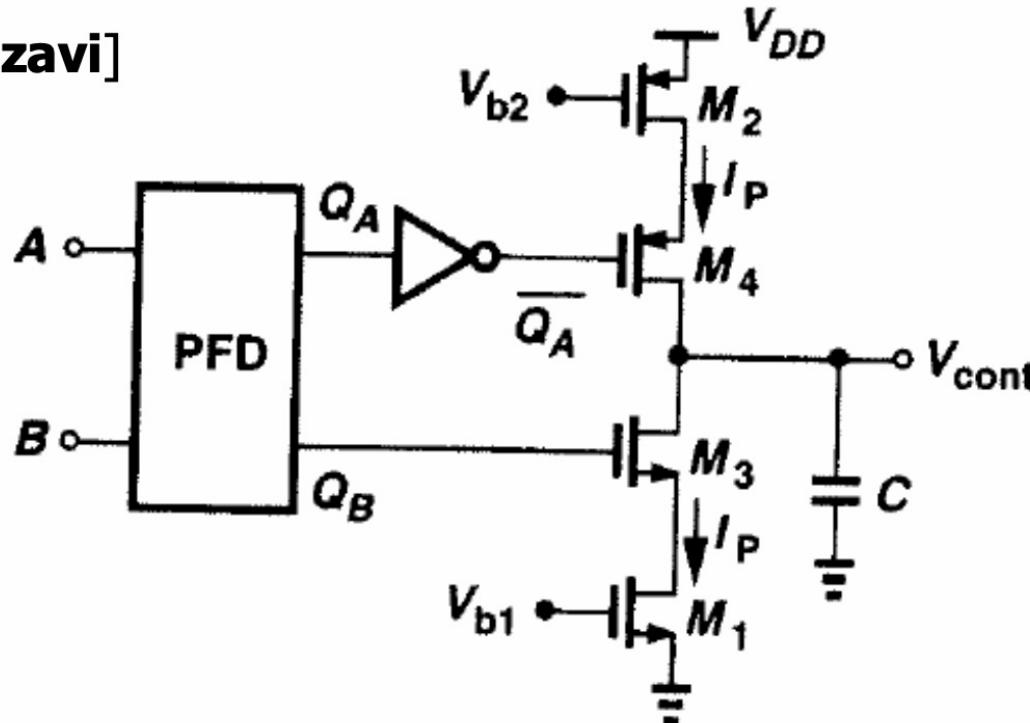
- Converts PFD output signals to charge
- Charge is proportional to PFD pulse widths

$$\text{PFD-CP Gain: } \left(\frac{1}{2\pi} \right) I_{CP}$$

[Sam Palermo]

Simple Charge Pump

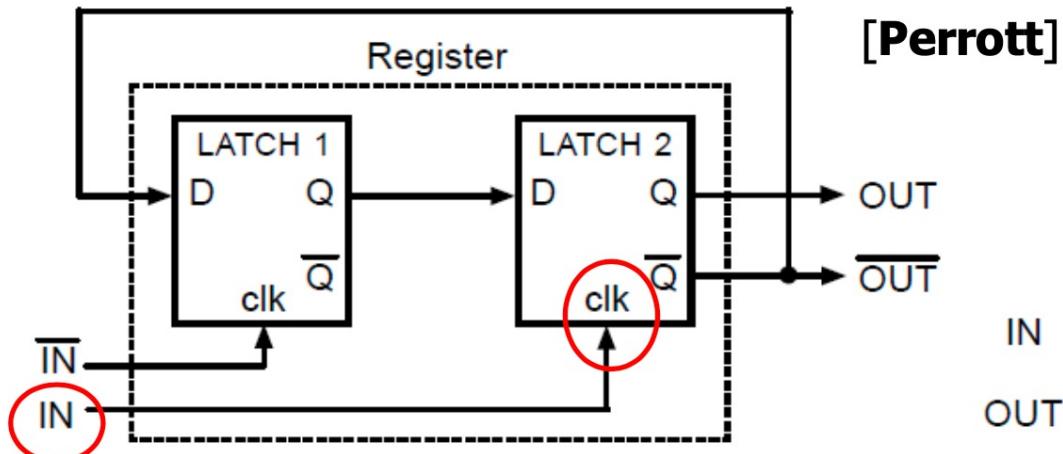
[Razavi]



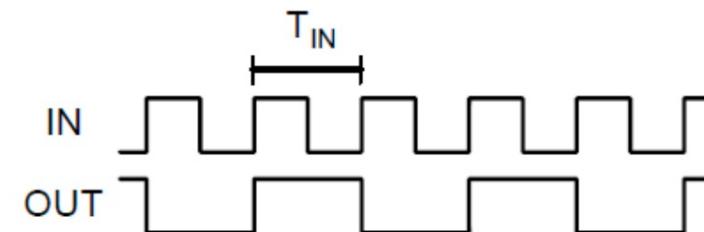
- Issues
 - Switch resistance can impact UP/DN current matching as a function of V_{ctrl}
 - Clock feedthrough and charge injection from switches onto V_{ctrl}
 - Charge sharing between current source drain nodes' capacitance and V_{ctrl}

[Sam Palermo]

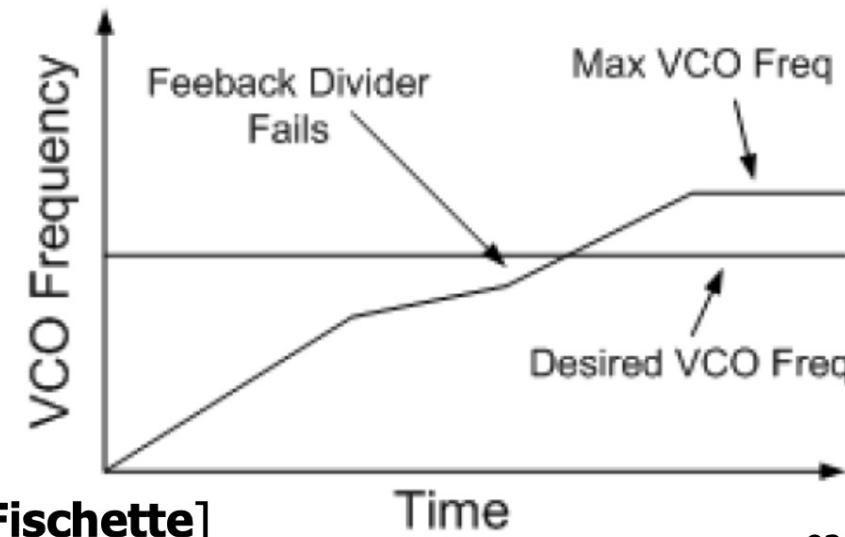
Basic Divide-by-2



[Perrott]



- Divide-by-2 can be realized by a flip-flop in “negative feedback”
- Divider should operate correctly up to the maximum output clock frequency of interest **PLUS** some margin



[Fischette]

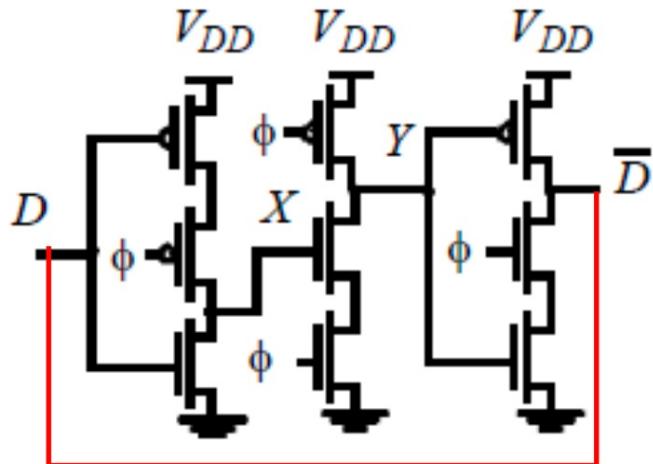
Time

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[Sam Palermo]

Divide-by-2 with TSPC FF

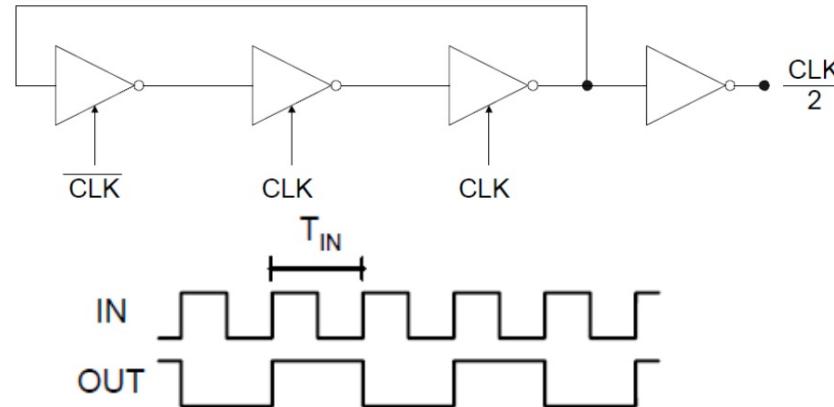
True Single Phase Clock Flip-Flop



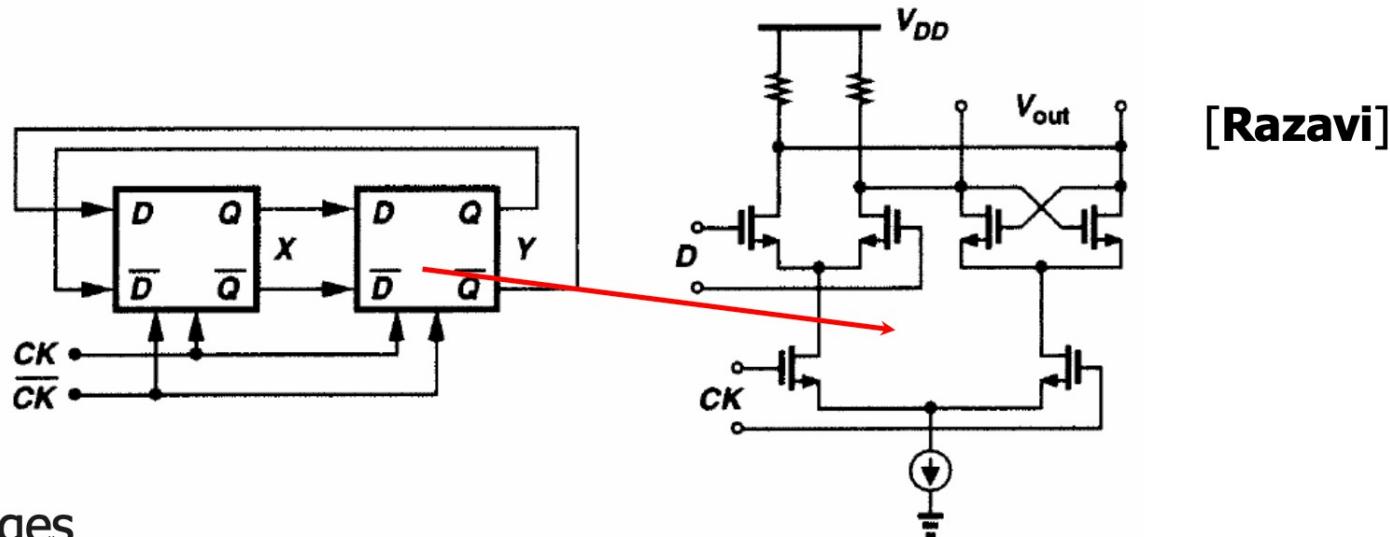
- Advantages
 - Reasonably fast, compact size, and no static power
 - Requires only one phase of the clock
- Disadvantages
 - Signal needs to propagate through three gates per input cycle
 - Need full swing CMOS inputs
 - Dynamic flip-flop may have issues at very low frequency operation (test mode) depending on process leakage

Divider Equivalent Circuit

Note: output inverter not in left schematic



Divide-by-2 with CML FF

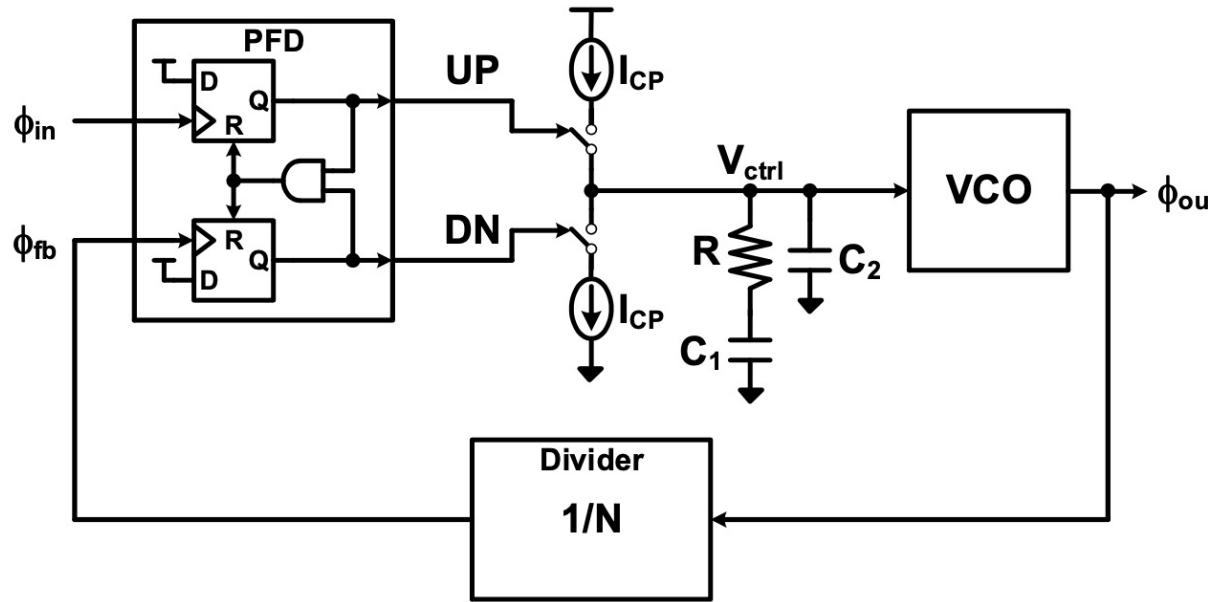


- Advantages
 - Signal only propagates through two CML gates per input cycle
 - Accepts CML input levels
- Disadvantages
 - Larger size and dissipates static power
 - Requires differential input
 - Need tail current biasing
- Additional speedup (>50%) can be achieved with shunt peaking inductors

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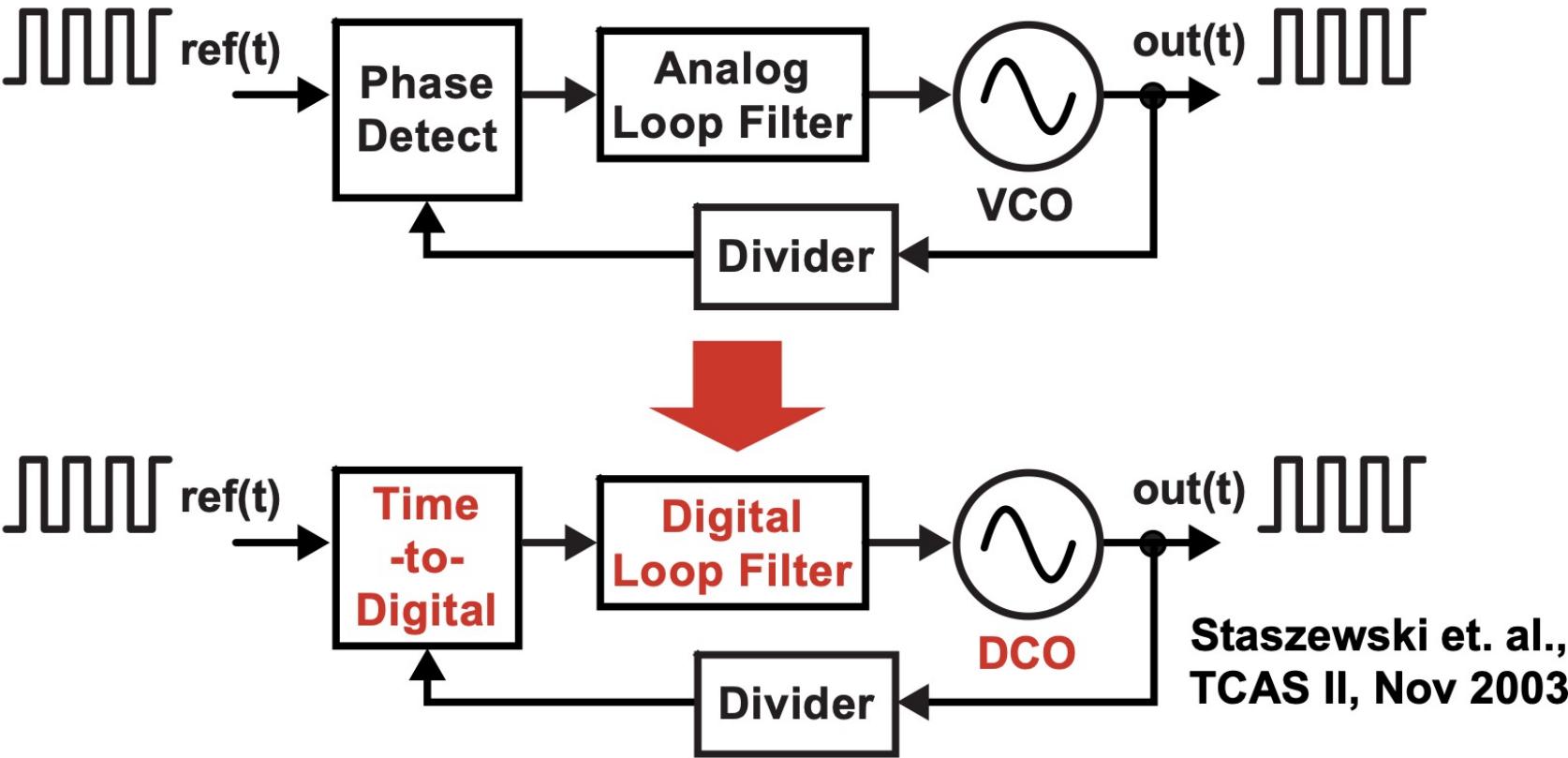
[Sam Palermo]

Charge Pump PLL



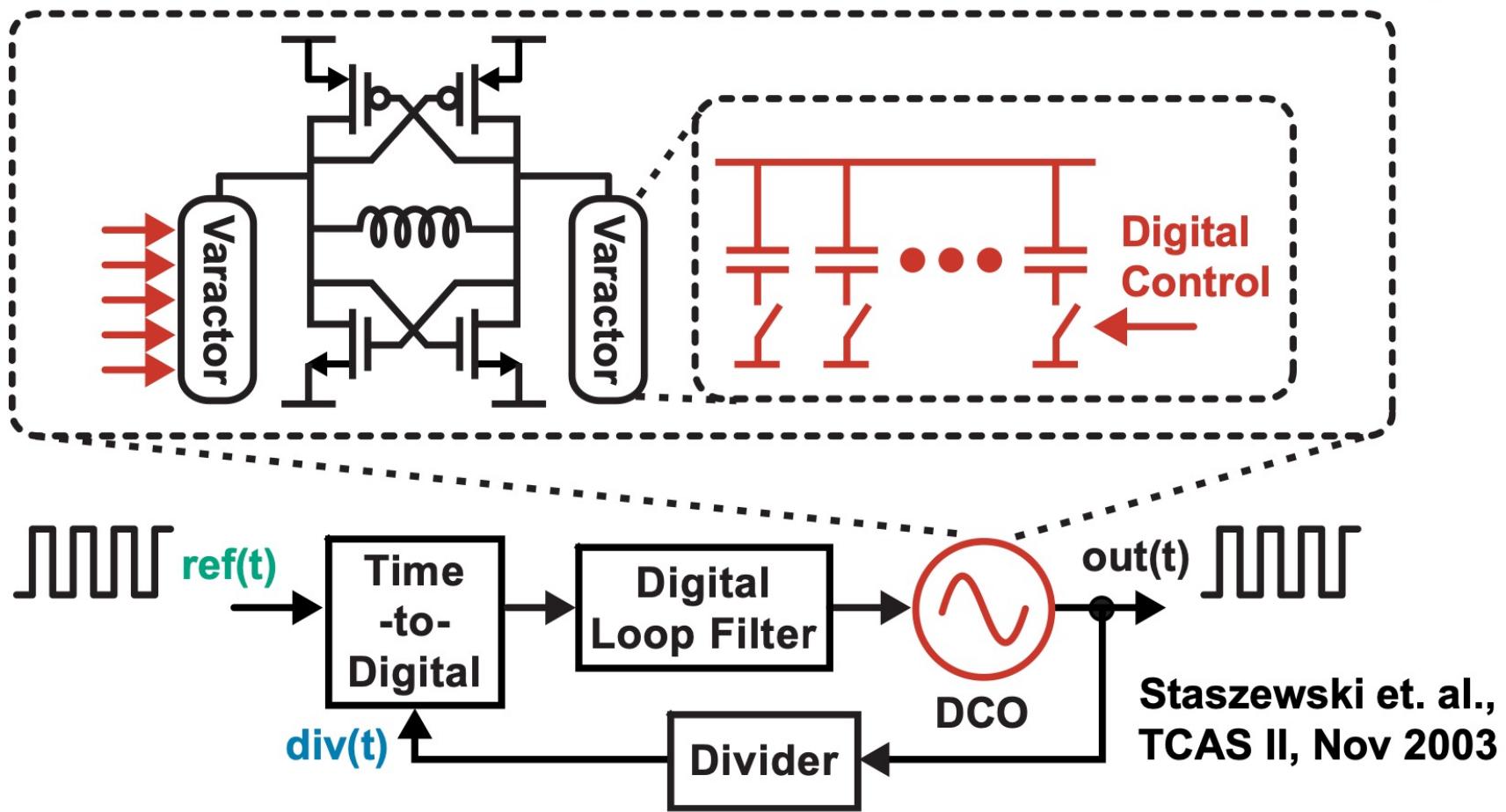
- Charge pump PLL is a common implementation
- Type-2 (2 integrators) allows for ideally zero phase error between the input and feedback phase
- Requires a stabilizing zero that is realized with the filter resistor
- A secondary capacitor C_2 is often added for additional filtering to reduce reference spurs
- Modeled as a third-order system

Going Digital ...



- Digital loop filter: compact area, insensitive to leakage
- Challenges:
 - Time-to-Digital Converter (TDC)
 - Digitally-Controlled Oscillator (DCO)

A Much More Digital Implementation



- Adjust frequency in an LC oscillator by switching in a variable number of small capacitors
 - Most effective for CMOS processes of 0.13μ and below

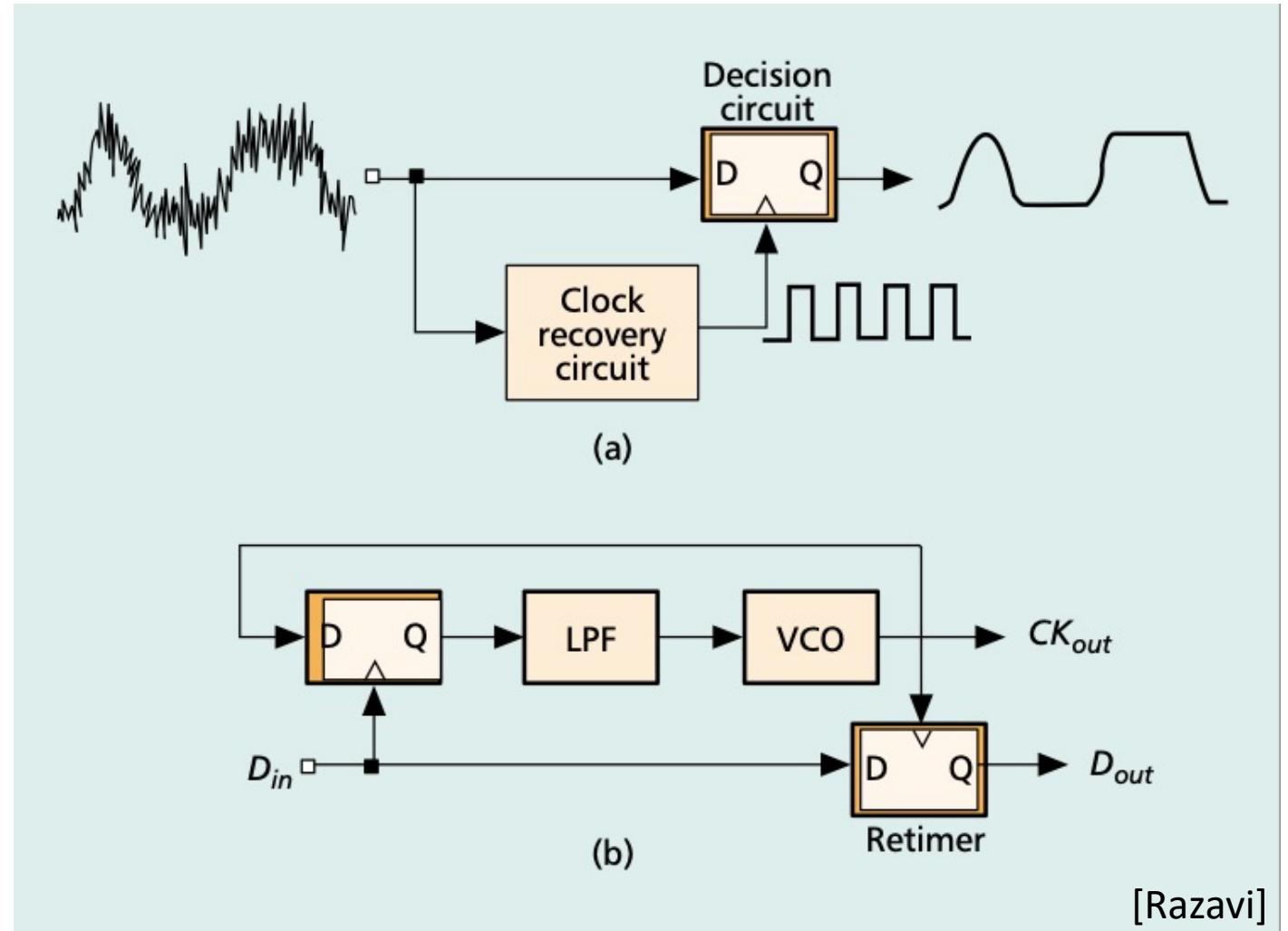
H. Perrott

In General: CDR

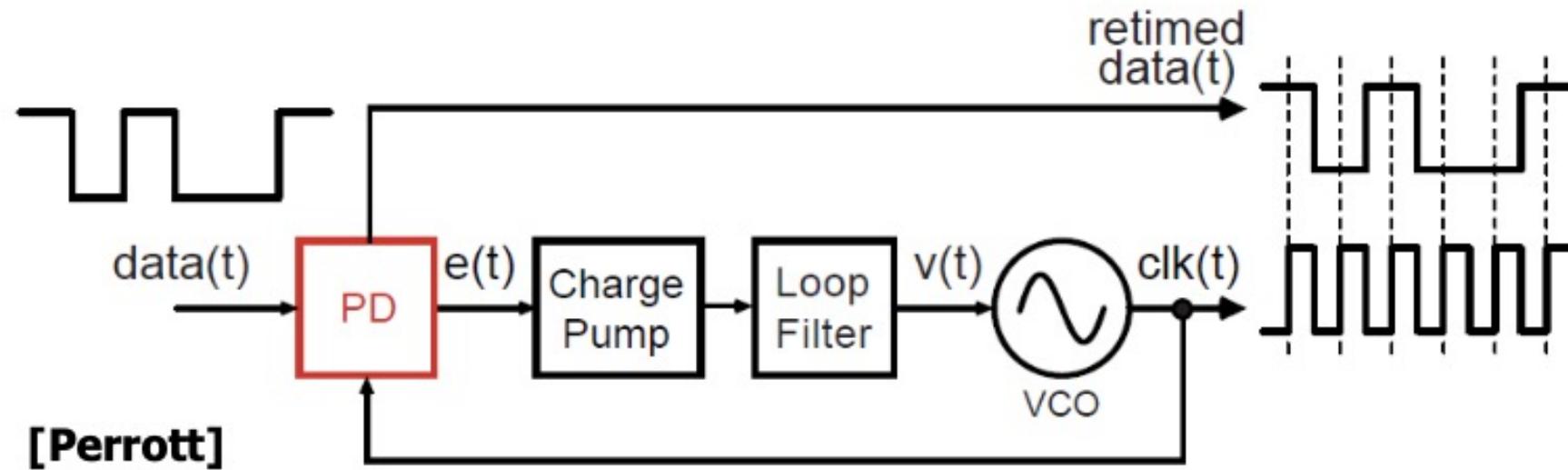
- **CDR = Clock and Data Recovery**
 - Recover clock phase and/or frequency based on data itself
 - If phase only, need a frequency reference
- **Several advantages vs. fixed timing**
 - Don't have to match delays/paths (**mesochronous**)
 - Allows separate crystals (**plesiochronous**)
- **But, CDR isn't free**
 - And places some requirements on data

[Elad Alon]

Conceptual CDR



CDR Phase Detectors



- A primary difference between CDRs and PLLs is that the incoming data signal is not periodic like the incoming reference clock of a PLL
- A CDR phase detector must operate properly with missing transition edges in the input data sequence

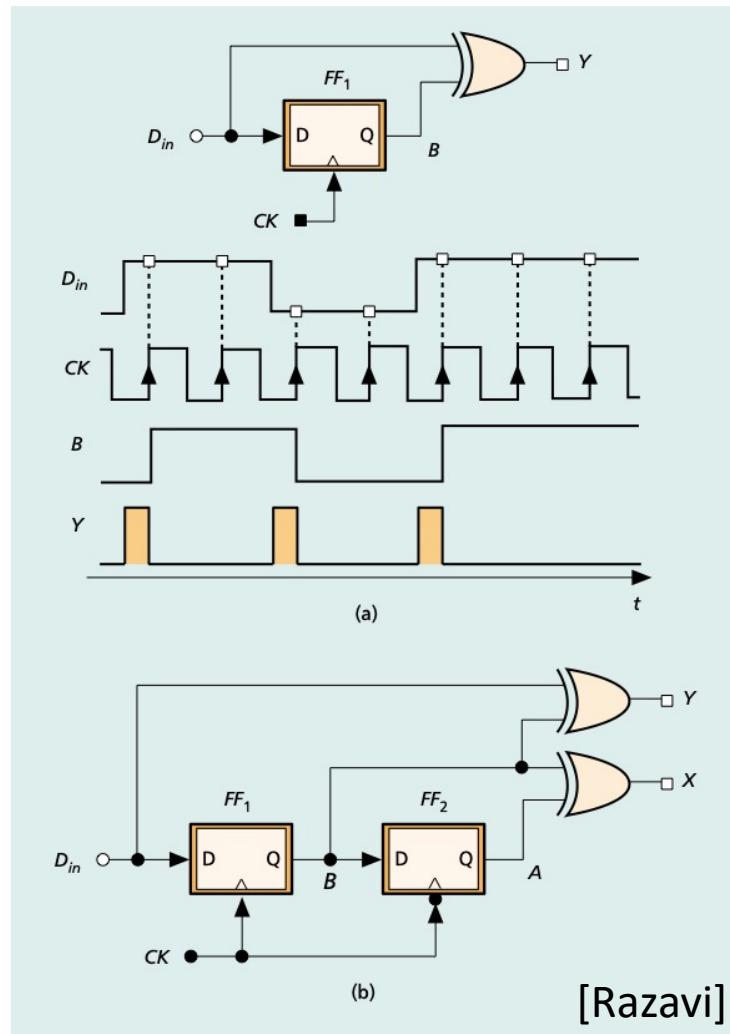
[Sam Palermo]

CDR Phase Detectors

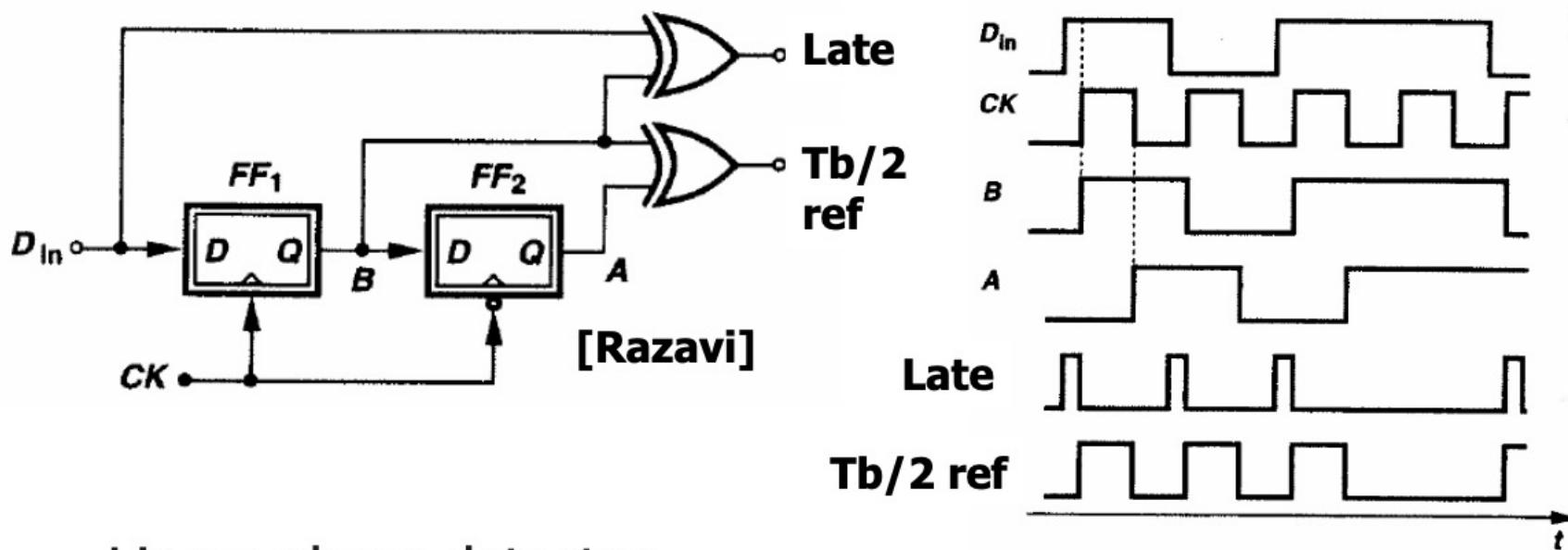
- CDR phase detectors compare the phase between the input data and the recovered clock sampling this data and provides information to adjust the sampling clocks' phase
- Phase detectors can be linear or non-linear
- Linear phase detectors provide both **sign and magnitude** information regarding the sampling phase error
 - Hogge
- Non-linear phase detectors provide **only sign** information regarding the sampling phase error
 - Alexander or 2x-Oversampled or Bang-Bang
 - Oversampling (>2)
 - Baud-Rate

[Sam Palermo]

Linear Phase Detectors



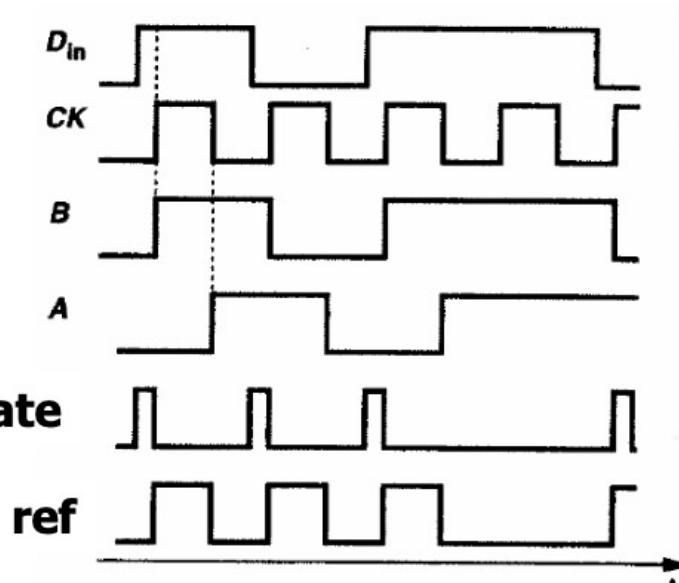
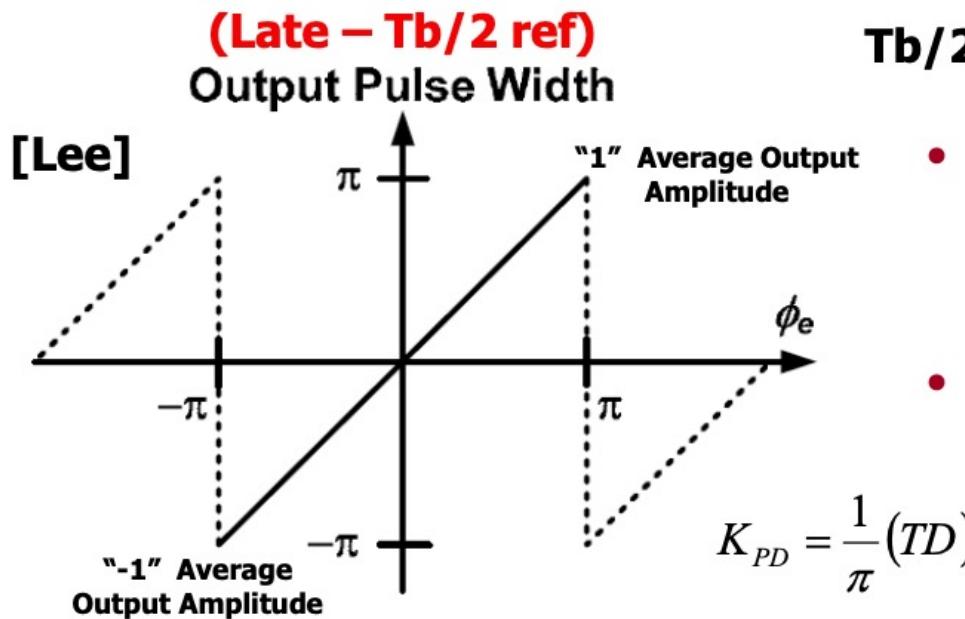
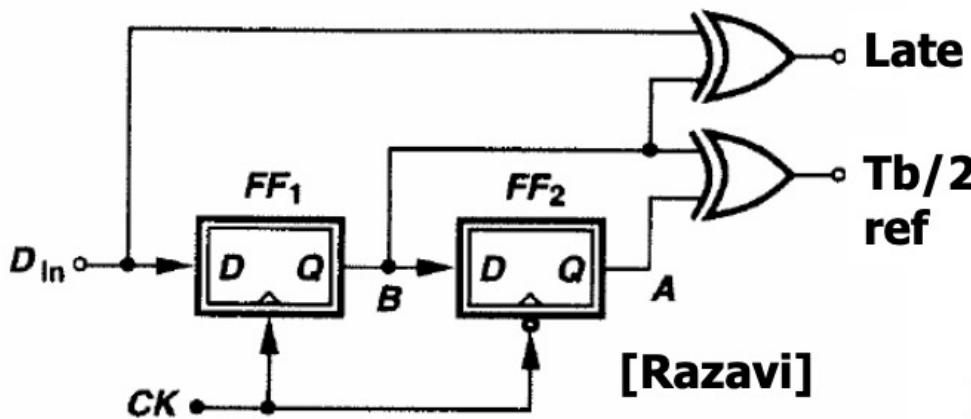
Hogge Phase Detector



- Linear phase detector
- With a data transition and assuming a full-rate clock
 - The late signal produces a signal whose pulse width is proportional to the phase difference between the incoming data and the sampling clock
 - A $Tb/2$ reference signal is produced with a $Tb/2$ delay
- If the clock is sampling early, the late signal will be shorter than $Tb/2$ and vice-versa

[Sam Palermo]

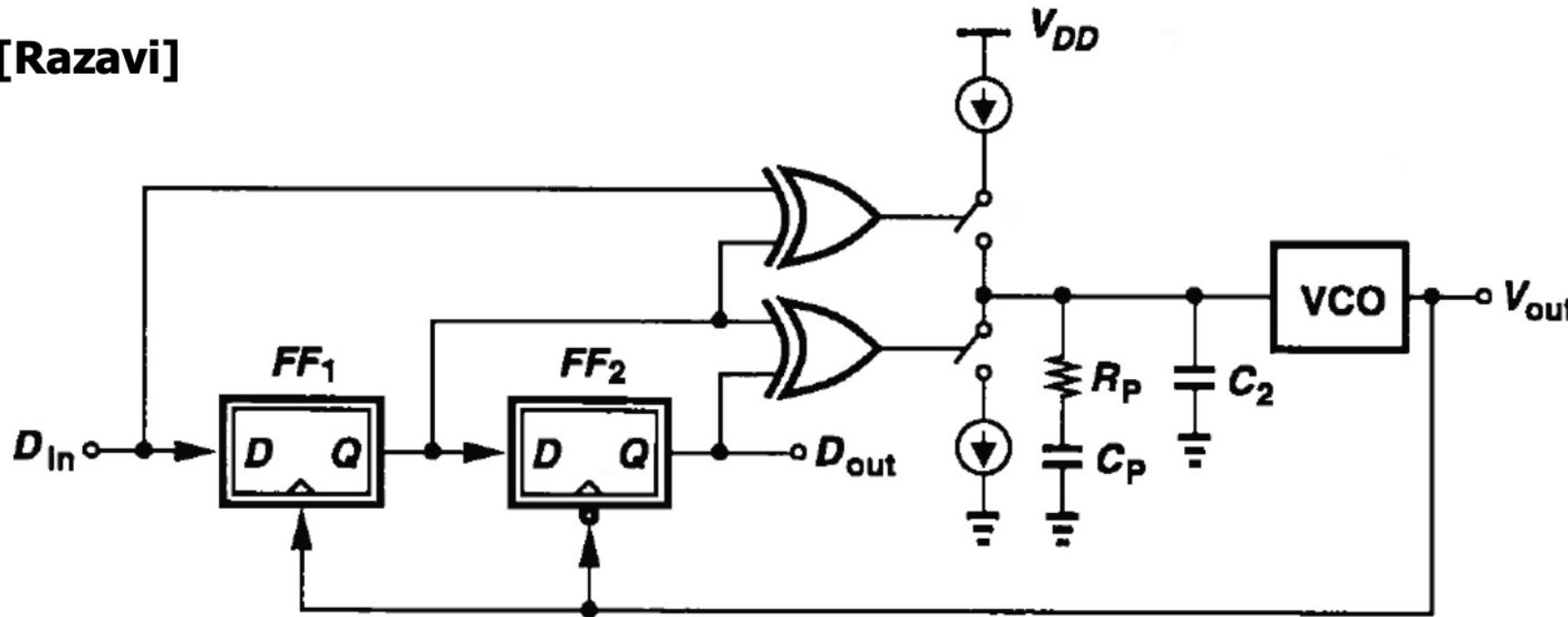
Hogge Phase Detector



- For phase transfer 0rad is w.r.t optimal $Tb/2$ (π) spacing between sampling clock and data
 - $\phi_e = \phi_{in} - \phi_{clk} - \pi$
- TD is the transition density – no transitions, no information
 - A value of 0.5 can be assumed for random data

PLL-Based CDR with a Hogge PD

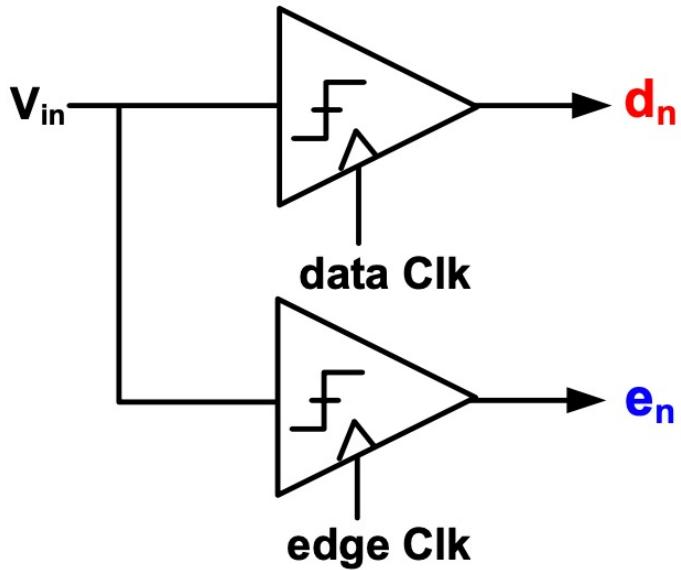
[Razavi]



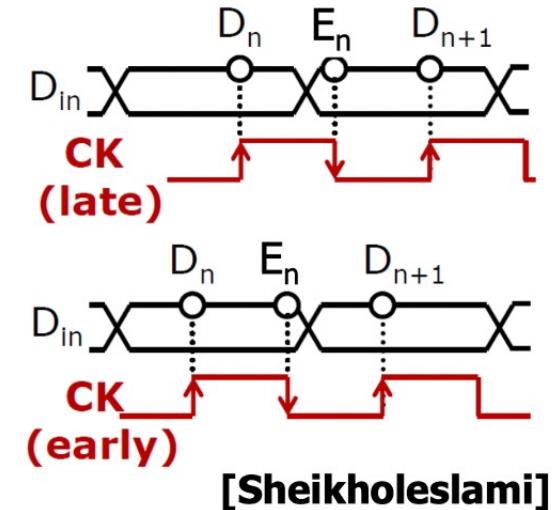
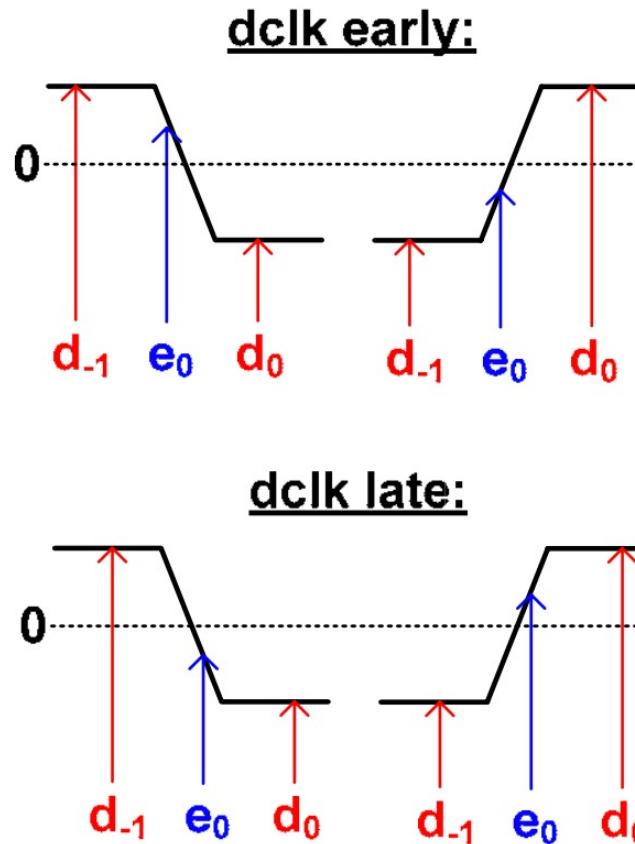
- XOR outputs can directly drive the charge pump
- Need a relatively high-speed charge pump

[Sam Palermo]

Bang-Bang (Alexander) Phase Detector



- Edge clock $T_{sym}/2$ away from data
- Derive early/late from data and edge samples:
 - $D_n: (d_n \neq e_n) \& (d_{n-1} \neq d_n)$
 - Up: $(d_n == e_n) \& (d_{n-1} \neq d_n)$



[Elad Alon]

Alexander (2x-Oversampled) Phase Detector

- Most commonly used CDR phase detector
- Non-linear (Binary) “Bang-Bang” PD
 - Only provides sign information of phase error (not magnitude)
- Phase detector uses 2 data samples and one “edge” sample
- Data transition necessary

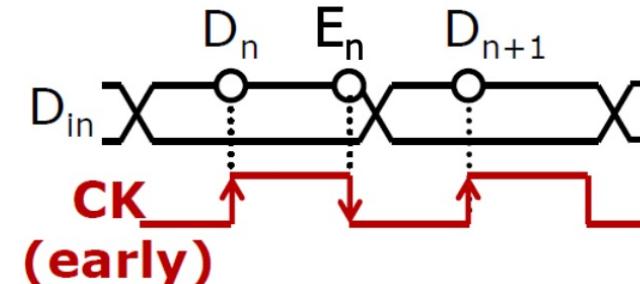
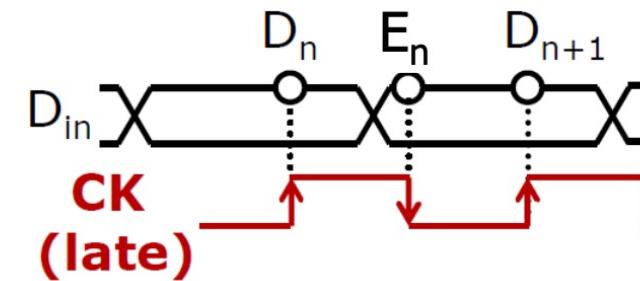
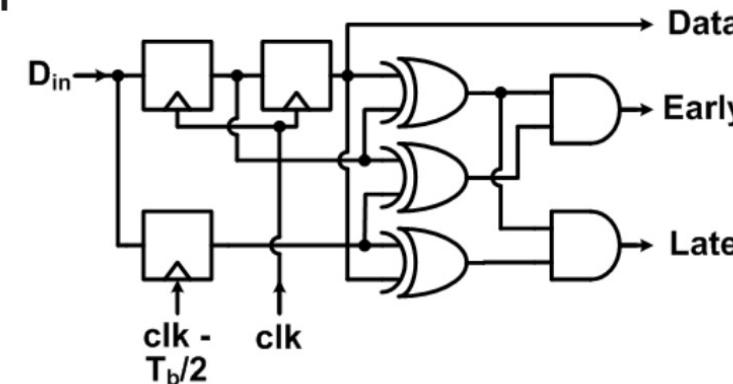
$$D_n \oplus D_{n+1}$$

- If “edge” sample is same as second bit (or different from first), then the clock is sampling “late”

$$E_n \oplus D_n$$

- If “edge” sample is same as first bit (or different from second), then the clock is sampling “early”

$$E_n \oplus D_{n+1}$$

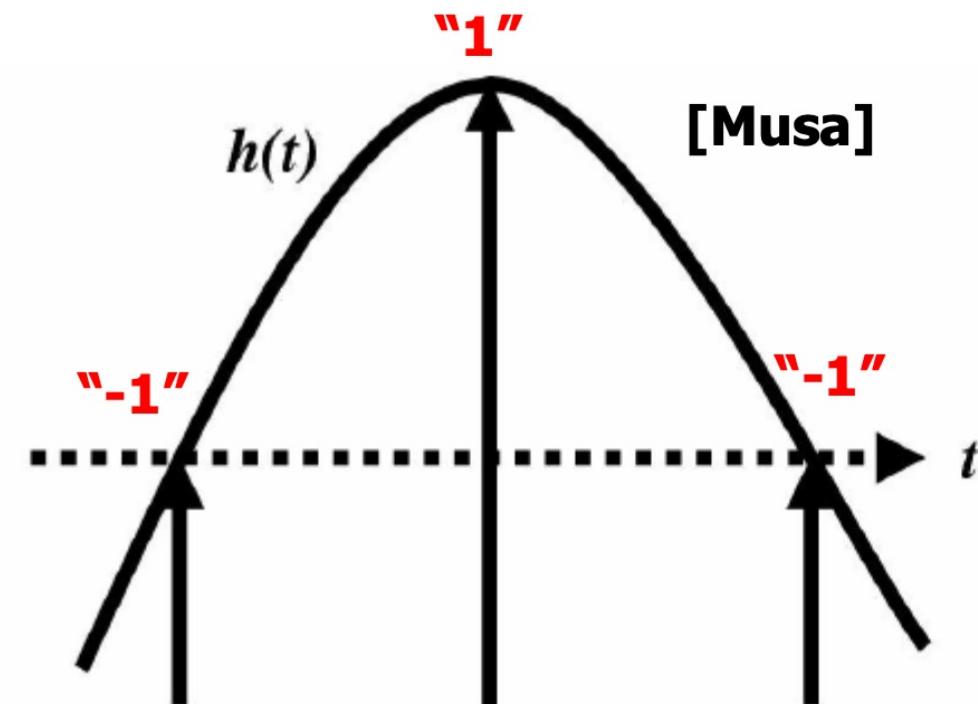


[Sheikholeslami]

[Sam Palermo]

Mueller-Muller Baud-Rate Phase Detector

- Baud-rate phase detector only requires one sample clock per symbol (bit)
- Mueller-Muller phase detector commonly used
- Attempting to equalize the amplitude of samples taken before and after a pulse



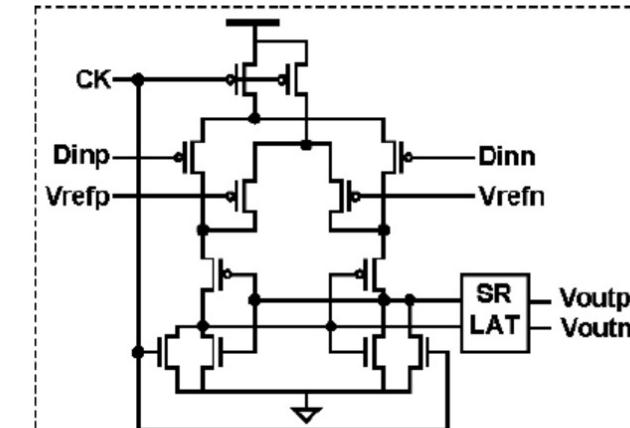
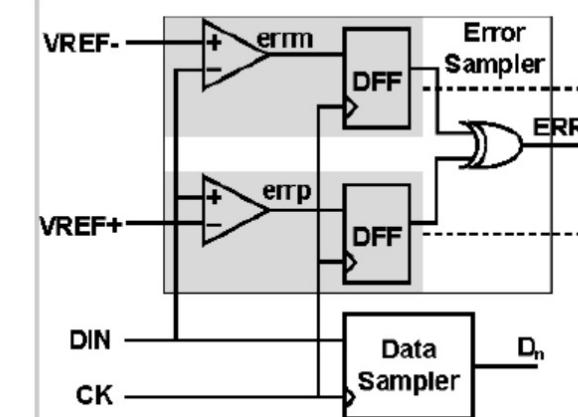
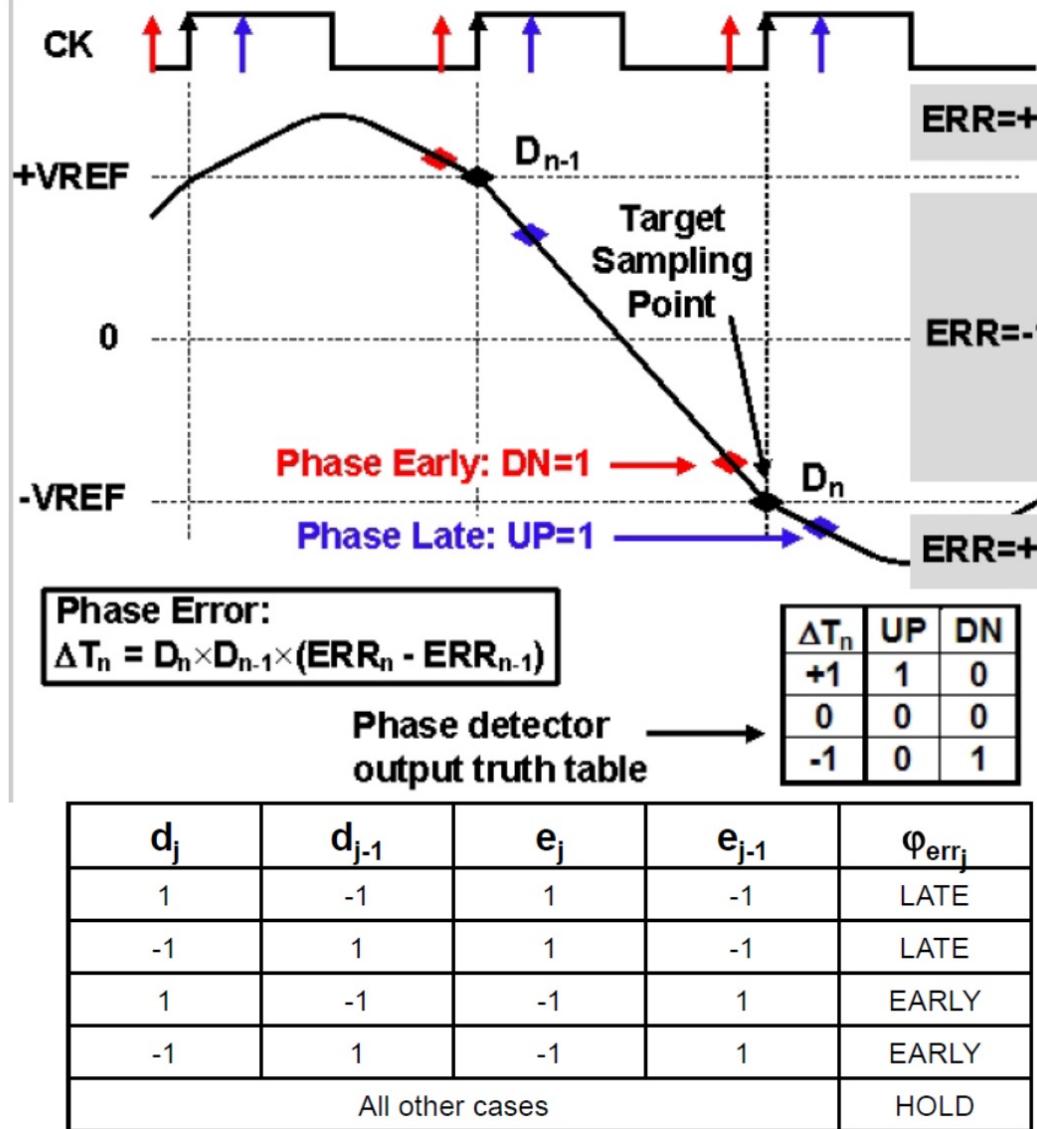
Locked Condition: $h(\tau_k - T_b) = h(\tau_k + T_b)$

Early Clock: $h(\tau_k - T_b) < h(\tau_k + T_b)$

Late Clock: $h(\tau_k - T_b) > h(\tau_k + T_b)$

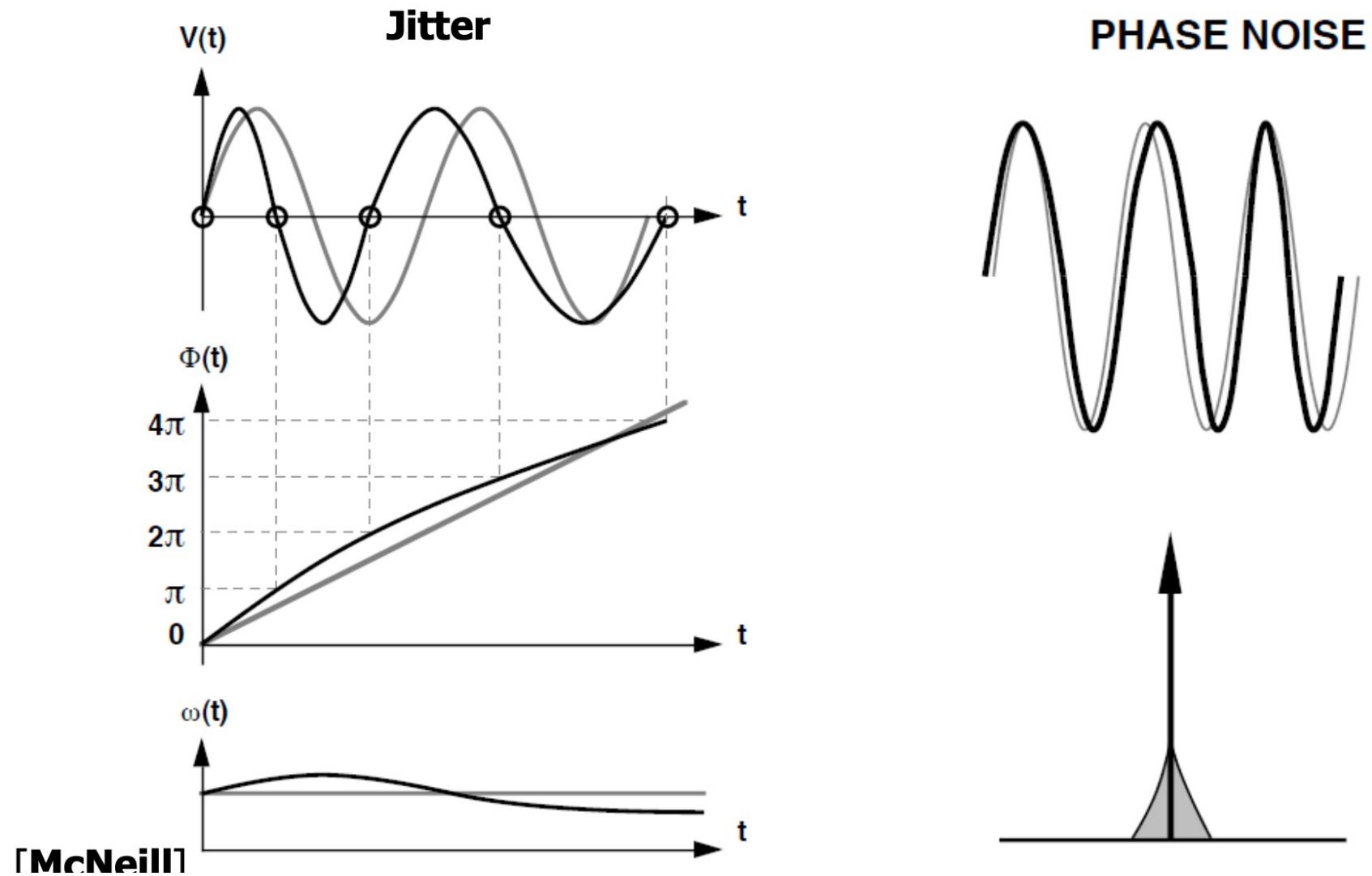
[Sam Palermo]

Mueller-Muller Baud-Rate Phase Detector



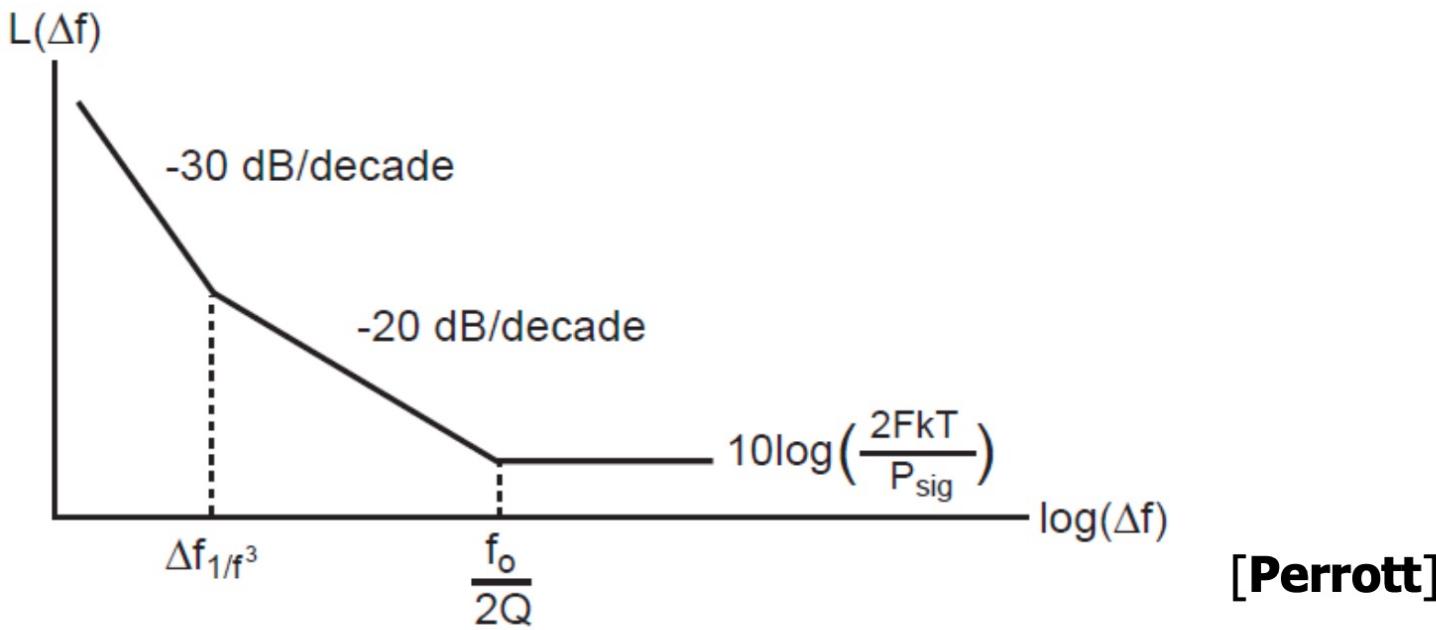
[Spagna ISSCC 2010]

Oscillator Noise



[Sam Palermo]

Oscillator Phase Noise Model



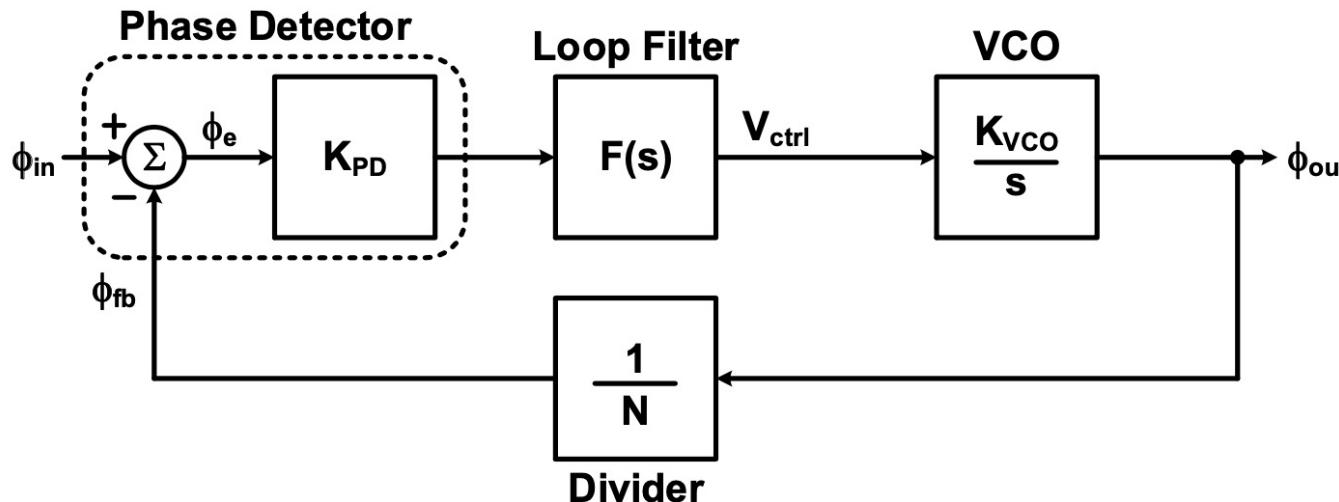
$$L(f) = 10 \log \left(\frac{\text{Noise Spectral Density}}{\text{Carrier Power}} \right) \text{ (dBc/Hz)}$$

Leeson's Model:
$$L(\Delta f) = 10 \log \left(\frac{2FkT}{P_{sig}} \left(1 + \left(\frac{1}{2Q} \frac{f_o}{\Delta f} \right)^2 \right) \left(1 + \frac{\Delta f_{1/f^3}}{|\Delta f|} \right) \right)$$

- For improved model see Hajimiri papers

[Sam Palermo]

Linear PLL Model



For Charge Pump PLL:

$$K_{PD} = \frac{I_{CP}}{2\pi}$$

$$F(s) = \frac{\left(\frac{1}{C_2}\right)\left(s + \frac{1}{RC_1}\right)}{s\left(s + \frac{C_1 + C_2}{RC_1 C_2}\right)}$$

$$H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{\frac{K_{PD} K_{VCO}}{C_2} \left(s + \frac{1}{RC_1}\right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1 C_2}\right)s^2 + \left(\frac{K_{PD} K_{VCO}}{NC_2}\right)s + \frac{K_{PD} K_{VCO}}{NRC_1 C_2}}$$

[Sam Palermo]

PLL Design Challenges

- Board-level reference clock frequencies don't scale often
 - 156MHz is a common frequency
- RX CDR bandwidth is hard to scale with PAM4 signaling and ADC-based front-ends
 - Typically 2-4MHz
- PLL bandwidth must be kept less than 10MHz for stability and to filter reference jitter
- VCO phase noise at low-frequency offsets due to flicker noise must be suppressed

32.75Gbps Transceiver PLL Simulated Jitter Numbers

Receiver Type	PLL PN @1MHz	CDR BW	RJ	RJ in UI
Analog based RX	-92.4dBc/Hz	12.7MHz	160.7fs	5.26mUI
ADC based RX	-92.4dBc/Hz	2MHz	407fs	13.3mUI

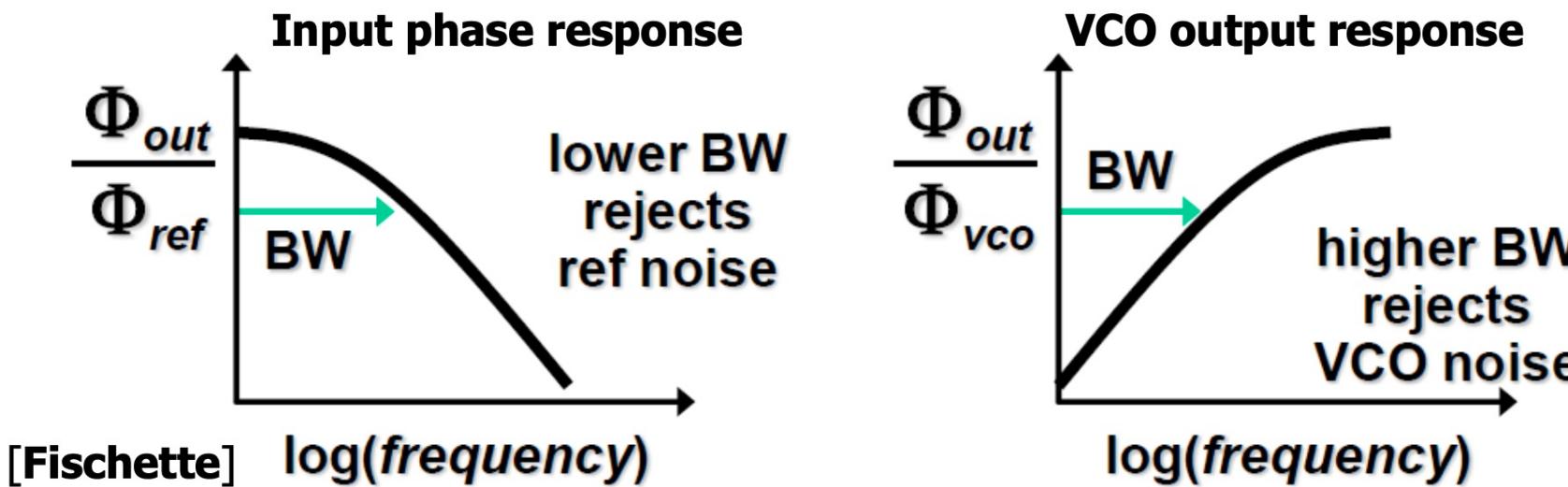
[Turker ISSCC 2019]

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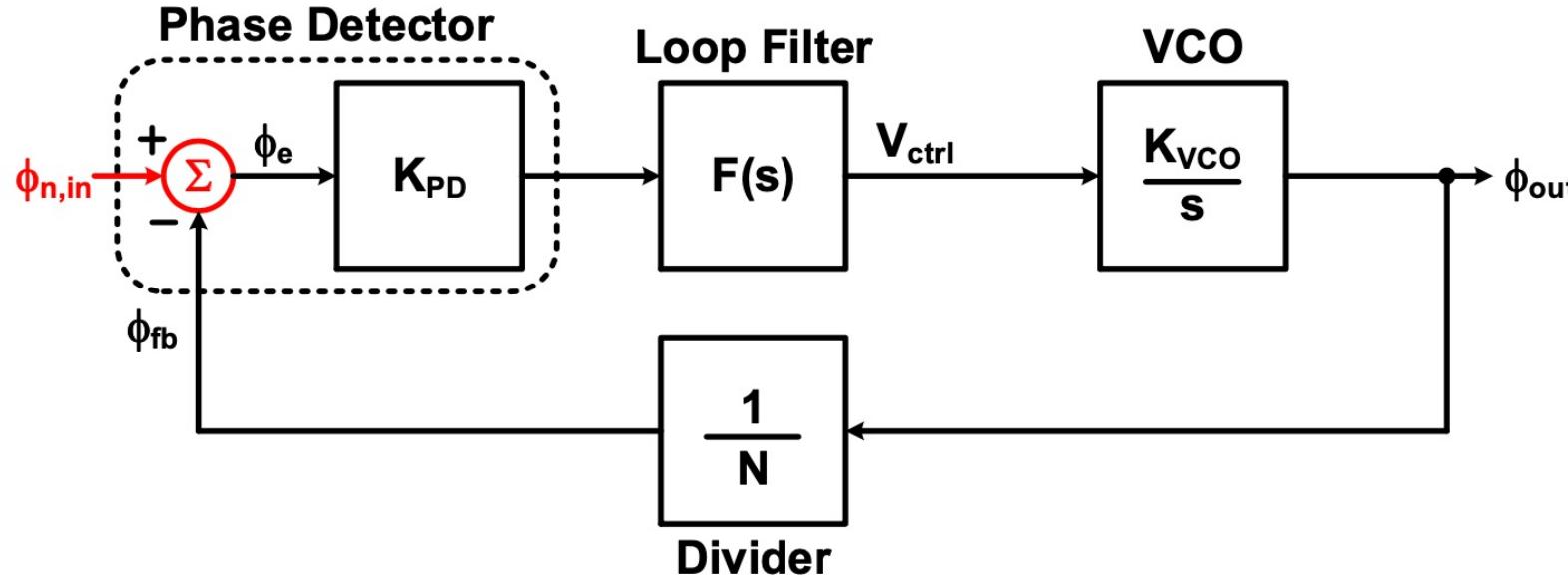
[Sam Palermo]

Understanding PLL Frequency Response

- Linear “small-signal” analysis is useful for understand PLL dynamics if
 - PLL is locked (or near lock)
 - Input phase deviation amplitude is small enough to maintain operation in lock range
- Frequency domain analysis can tell us how well the PLL tracks the input phase as it changes at a certain frequency
- PLL transfer function is different depending on which point in the loop the output is responding to



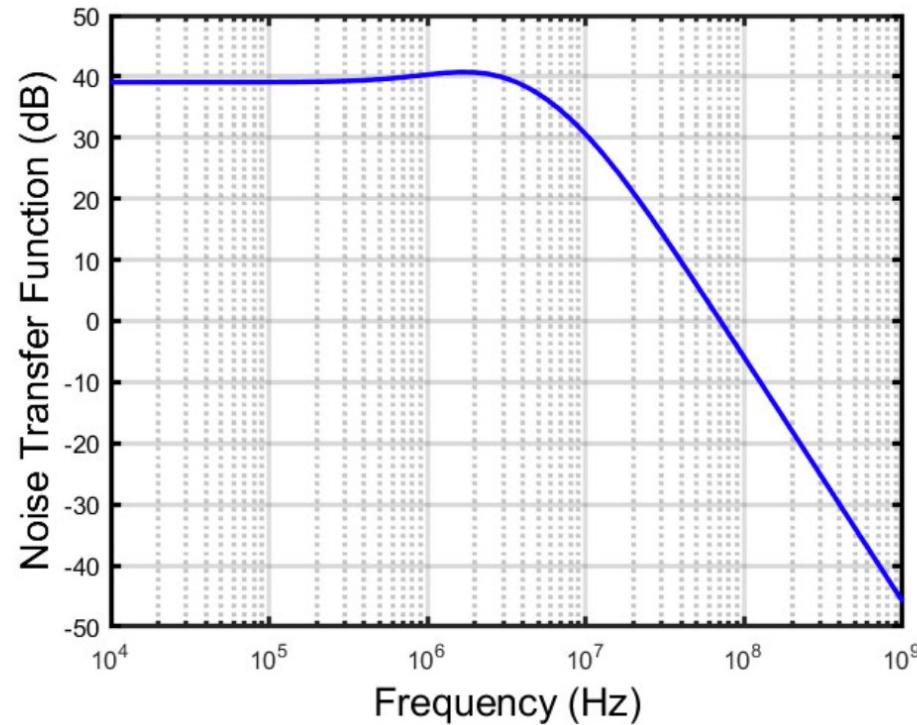
Input Noise Transfer Function



$$\text{Input Phase Noise: } H_{n_{IN}}(s) = \frac{\phi_{out}(s)}{\phi_{n_{IN}}(s)} = \frac{\frac{K_{PD} K_{VCO}}{C_2} \left(s + \frac{1}{RC_1} \right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1 C_2} \right) s^2 + \left(\frac{K_{PD} K_{VCO}}{NC_2} \right) s + \frac{K_{PD} K_{VCO}}{NRC_1 C_2}}$$

[Sam Palermo]

Input Noise Transfer Function

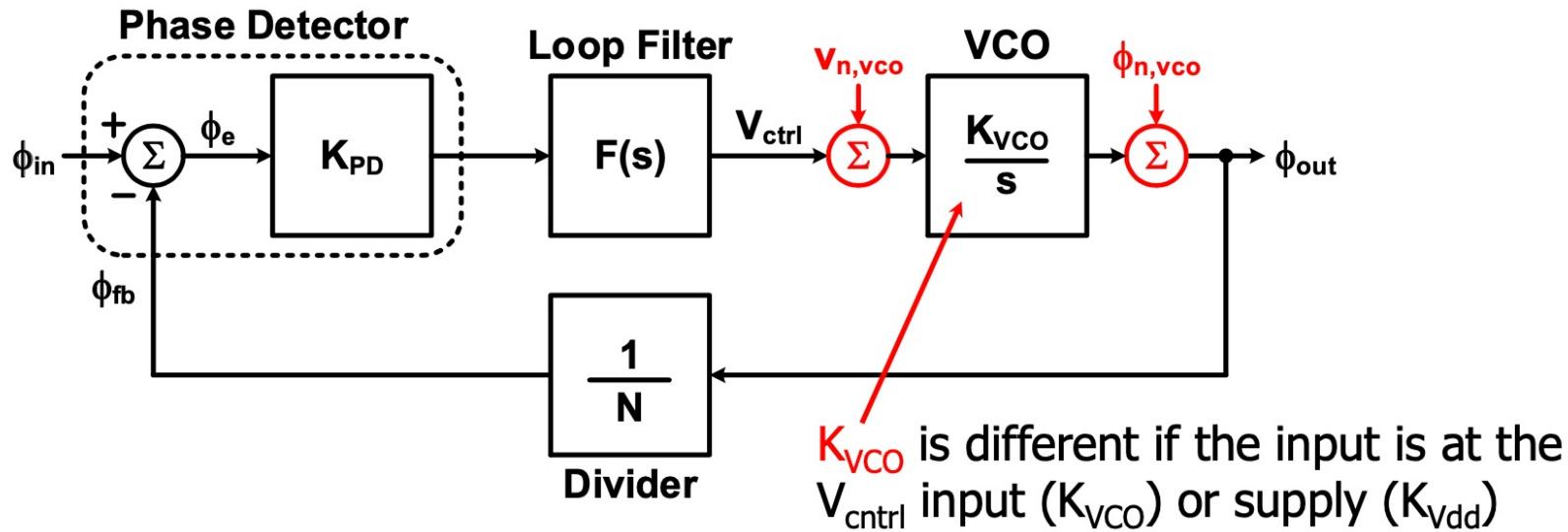


Parameter	
Fref	156MHz
N	90
Fvco	14GHz
Icp	100uA
R	22.7kΩ
C1	7.0pF
C2	500fF
Kvco	$2\pi \cdot 1\text{GHz/V}$
f _{3dB}	5.9MHz
Phase Margin	60°

Input Phase Noise: $H_{n_{IN}}(s) = \frac{\phi_{out}(s)}{\phi_{n_{IN}}(s)} = \frac{\frac{K_{PD}K_{VCO}}{C_2} \left(s + \frac{1}{RC_1} \right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1 C_2} \right) s^2 + \left(\frac{K_{PD}K_{VCO}}{NC_2} \right) s + \frac{K_{PD}K_{VCO}}{NRC_1 C_2}}$

[Sam Palermo]

VCO Noise Transfer Function

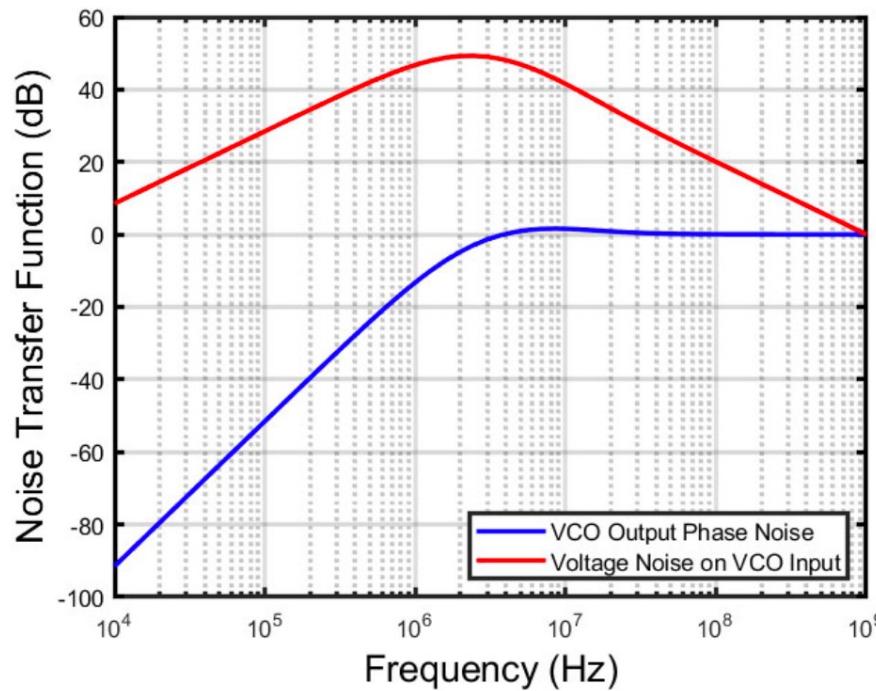


VCO Phase Noise:
$$H_{n_{VCO}}(s) = \frac{\phi_{out}(s)}{\phi_{n_{VCO}}(s)} = \frac{s^2 \left(s + \frac{C_1 + C_2}{RC_1 C_2} \right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1 C_2} \right) s^2 + \left(\frac{K_{PD} K_{VCO}}{NC_2} \right) s + \frac{K_{PD} K_{VCO}}{NRC_1 C_2}}$$

Voltage Noise on VCO Inputs:
$$T_{n_{VCO}}(s) = \frac{\phi_{out}(s)}{v_{n_{VCO}}(s)} = \frac{K_{VCO} s \left(s + \frac{C_1 + C_2}{RC_1 C_2} \right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1 C_2} \right) s^2 + \left(\frac{K_{PD} K_{VCO}}{NC_2} \right) s + \frac{K_{PD} K_{VCO}}{NRC_1 C_2}}$$

[Sam Palermo]

VCO Noise Transfer Function

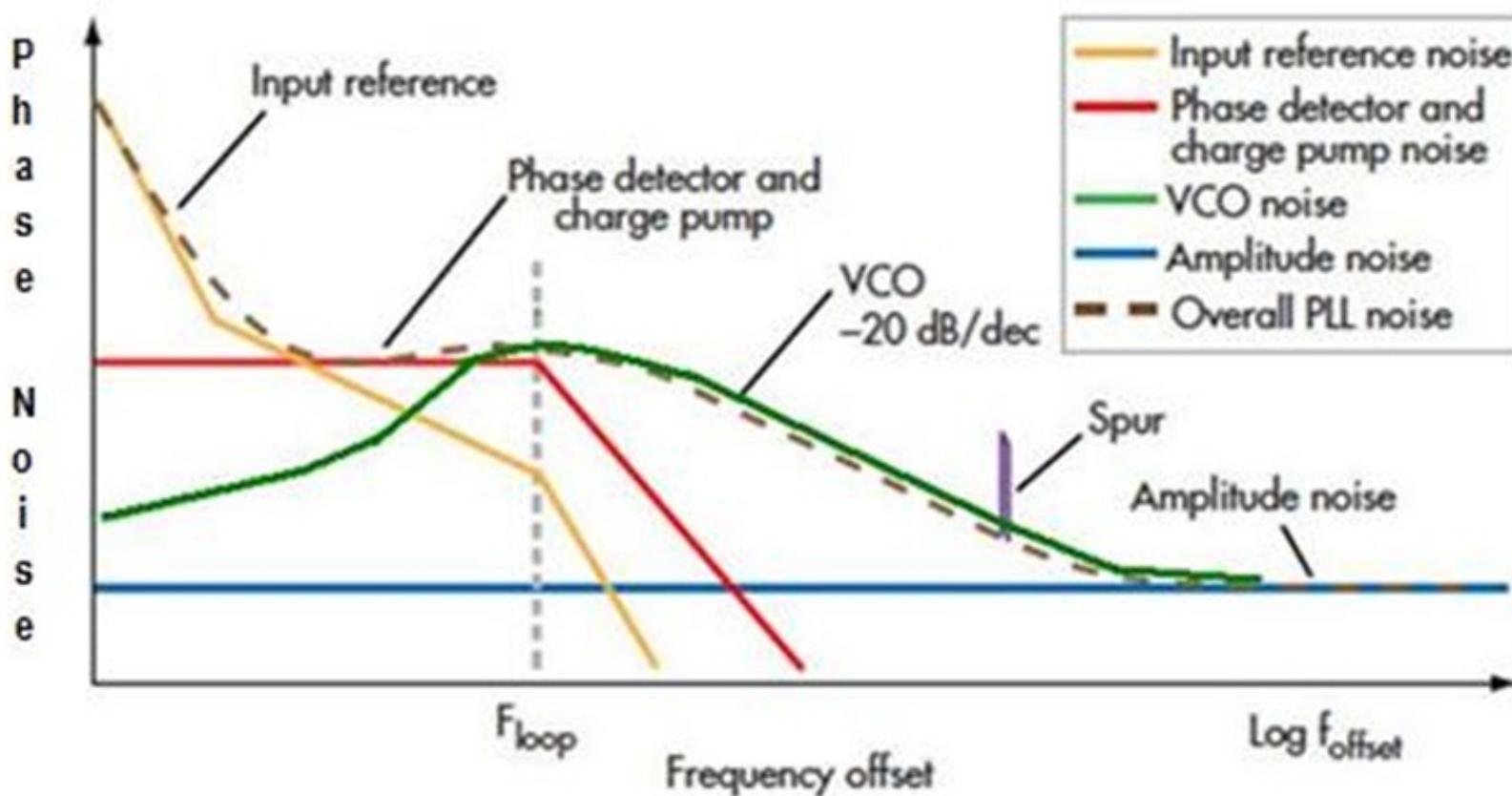


Parameter	
Fref	156MHz
N	90
Fvco	14GHz
Icp	100uA
R	22.7kΩ
C1	7.0pF
C2	500fF
Kvco	$2\pi \cdot 1\text{GHz/V}$
f _{3dB}	5.9MHz
Phase Margin	60°

VCO Phase Noise: $H_{n_{VCO}}(s) = \frac{\phi_{out}(s)}{\phi_{n_{VCO}}(s)} = \frac{s^2 \left(s + \frac{C_1 + C_2}{RC_1 C_2} \right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1 C_2} \right) s^2 + \left(\frac{K_{PD} K_{VCO}}{NC_2} \right) s + \frac{K_{PD} K_{VCO}}{NRC_1 C_2}}$

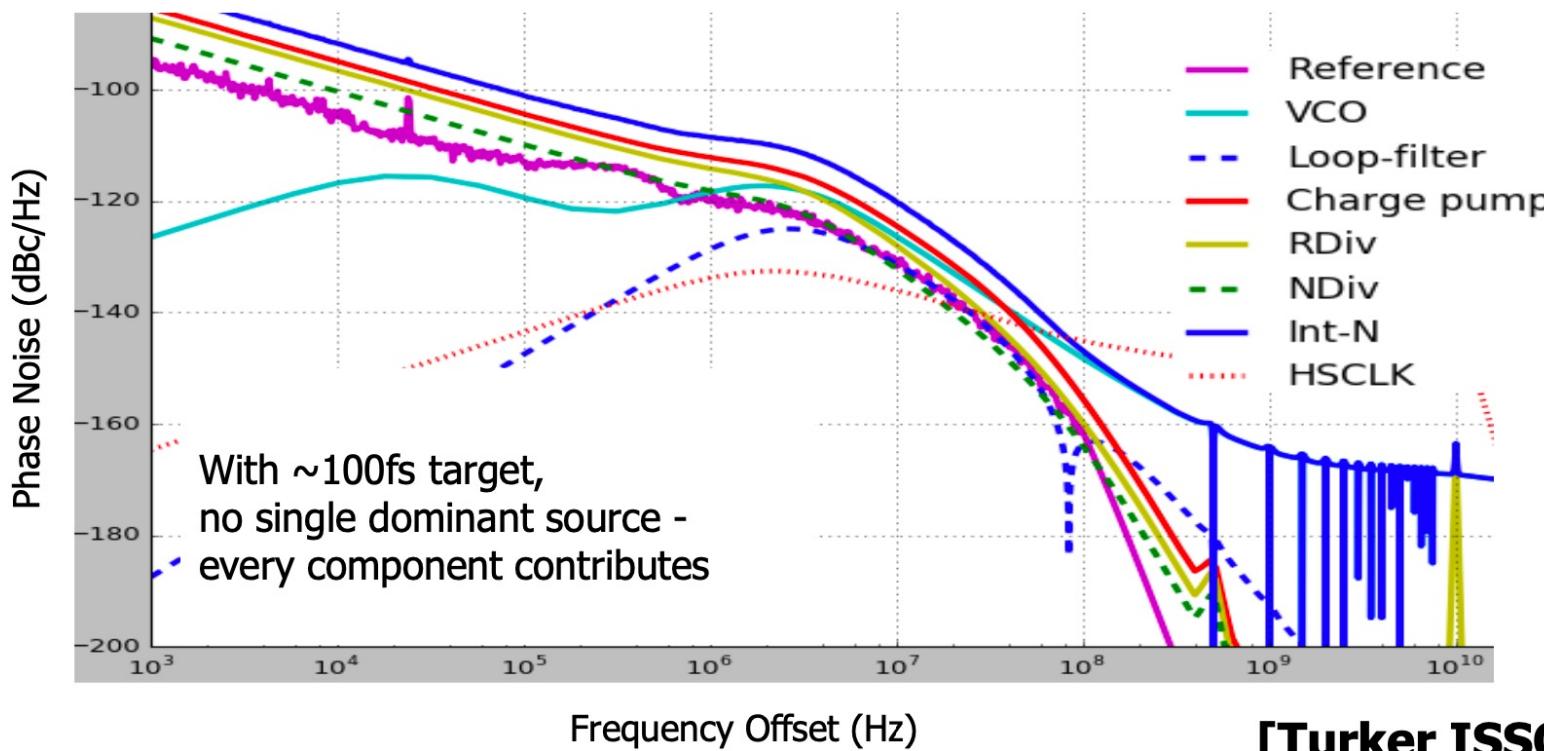
Voltage Noise on VCO Inputs: $T_{n_{VCO}}(s) = \frac{\phi_{out}(s)}{v_{n_{VCO}}(s)} = \frac{K_{VCO} s \left(s + \frac{C_1 + C_2}{RC_1 C_2} \right)}{s^3 + \left(\frac{C_1 + C_2}{RC_1 C_2} \right) s^2 + \left(\frac{K_{PD} K_{VCO}}{NC_2} \right) s + \frac{K_{PD} K_{VCO}}{NRC_1 C_2}}$

PLL's Overall Phase Noise



[Analog Devices]

28GHz PLL Phase Noise Example



- Charge pump noise dominates at low frequencies
- VCO noise at mid-band and high frequencies
- Output buffers outside loop dominate at high frequencies

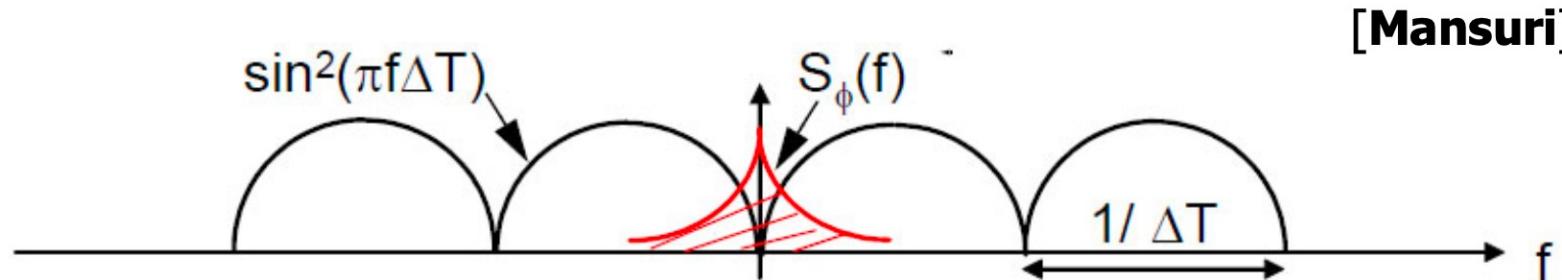
[Sam Palermo]

PLL Noise Transfer Function Take-Away Points

- The way a PLL shapes phase noise depends on where the noise is introduced in the loop
- Optimizing the loop bandwidth for one noise source may enhance other noise sources
- Generally, the PLL low-pass shapes input phase noise, band-pass shapes VCO input voltage noise, and high-pass shapes VCO/clock buffer output phase noise

[Sam Palermo]

Converting Phase Noise to Jitter



- RMS jitter for ΔT accumulation $\sigma_{\Delta T}^2 = \frac{8}{\omega_o^2} \int_0^\infty S_\phi(f) \sin^2(\pi f \Delta T) df$
- As ΔT goes to ∞ $\sigma_T^2 = \frac{2}{\omega_o^2} R_\phi(0) = \frac{2}{\omega_o^2} \int_0^\infty S_\phi(f) df$
- Actual integration range depends on application bandwidth
 - f_{\min} set by assumed CDR tracking bandwidth
 - f_{\max} set by Nyquist frequency ($f_0/2$)
- Most exact approach $\sigma_T^2 = \frac{2}{\omega_o^2} \int_0^{f_0/2} S_\phi(f) |H_{sys}(f)|^2 df$

where $|H_{sys}(f)|^2$ is the system jitter transfer function

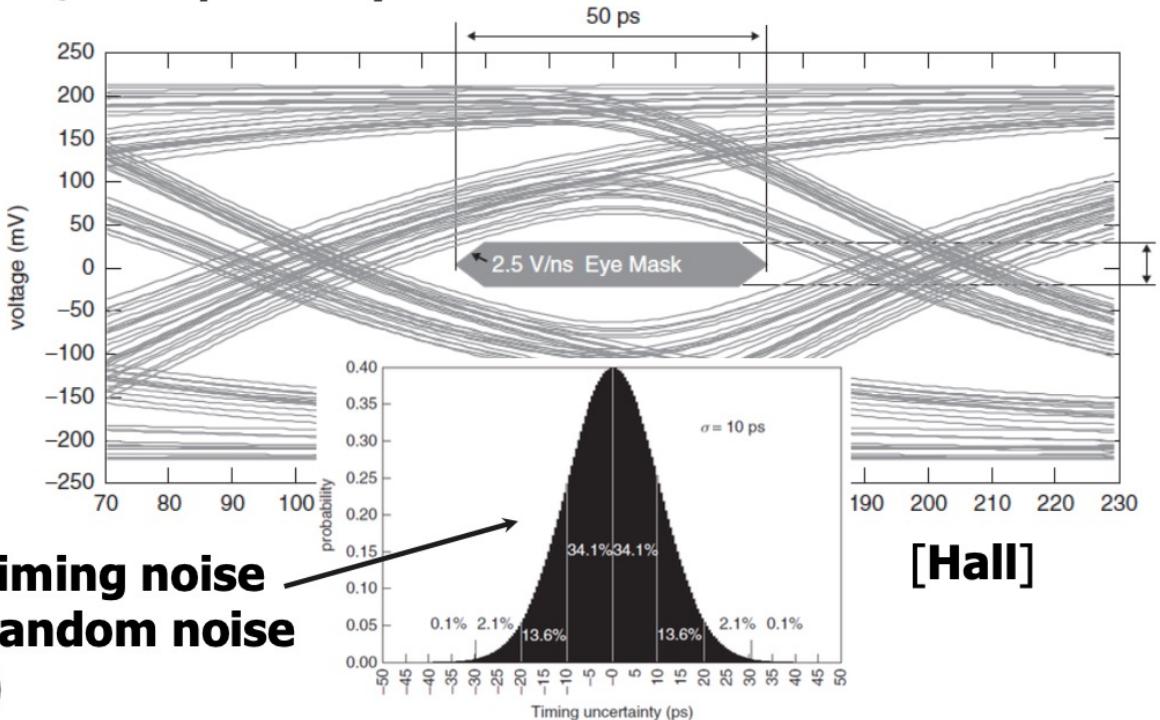
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[Sam Palermo]

Eye Diagram and Spec Mask

- Links must have margin in both the voltage AND timing domain for proper operation
- For independent design (interoperability) of TX and RX, a spec eye mask is used

Eye at RX sampler

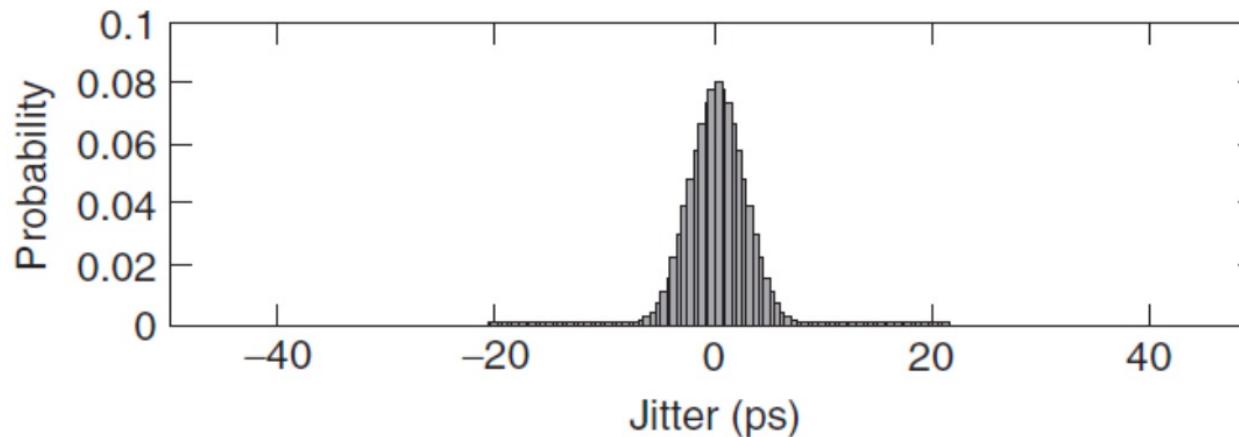


[Hall]

Random Jitter (RJ)

- Unbounded and modeled with a gaussian distribution
 - Assumed to have zero mean value
 - Characterized by the rms value, σ_{RJ}
 - Peak-to-peak value must be quoted at a given BER
- Originates from device noise
 - Thermal, shot, flicker noise

$$RJ(t) = \frac{1}{\sqrt{2\pi}\sigma_{RJ}} e^{\frac{-t^2}{2\sigma_{RJ}^2}}$$



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[Sam Palermo]

Deterministic Jitter (DJ)

- Bounded with a peak-to-peak value that can be predicted
- Caused by transmission-line losses, duty-cycle distortion, spread-spectrum clocking, crosstalk
- Categories
 - Sinusoidal Jitter (SJ or PJ)
 - Data Dependent Jitter (DDJ)
 - Intersymbol Interference (ISI)
 - Duty Cycle Distortion (DCD)
 - Bounded Uncoirrelated Jitter (BUJ)

