

# **EE 437/538B: Integrated Systems**

## **Capstone/Design of Analog Integrated Circuits and Systems**

### **Lecture 3: Overview of Equalization Techniques**

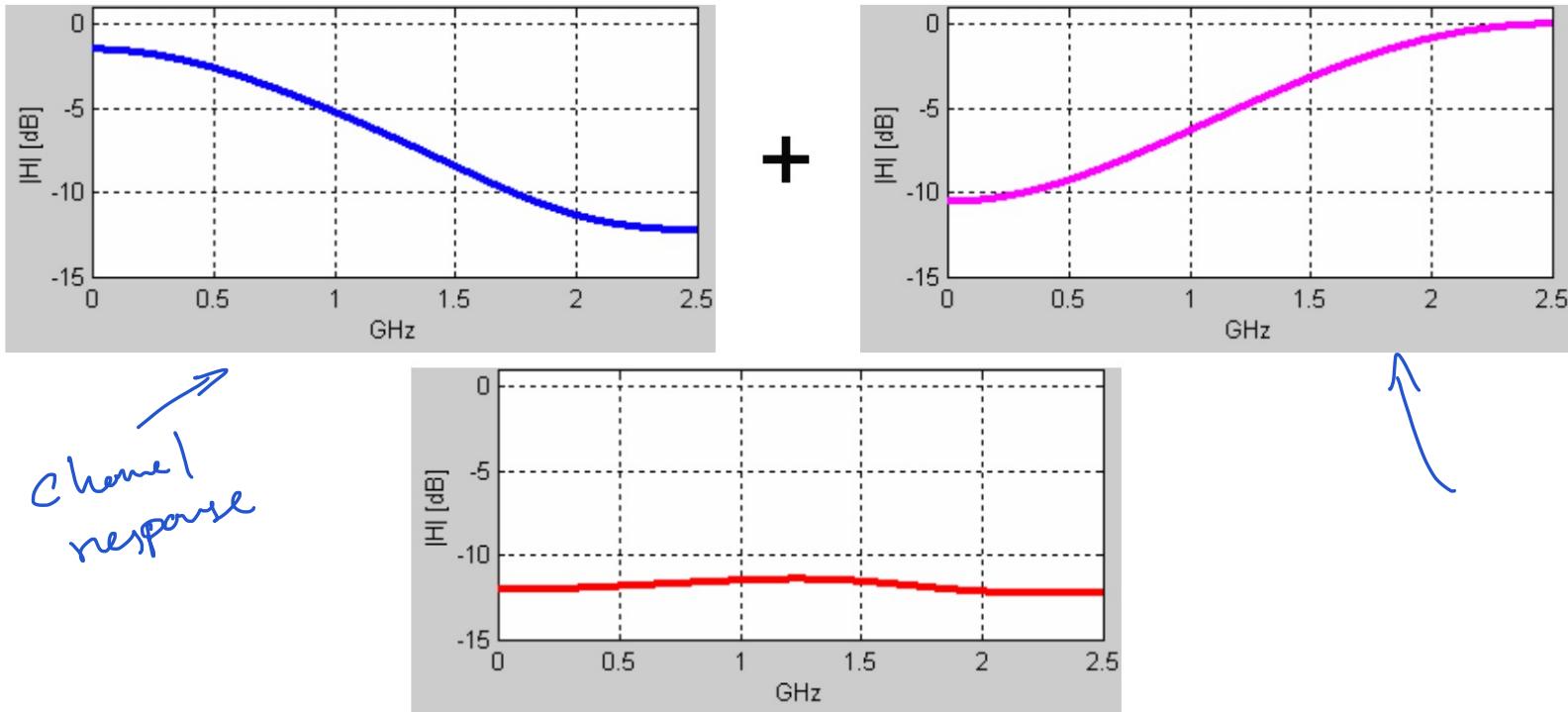
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Prof. Sajjad Moazeni

[smoazeni@uw.edu](mailto:smoazeni@uw.edu)

Spring 2022

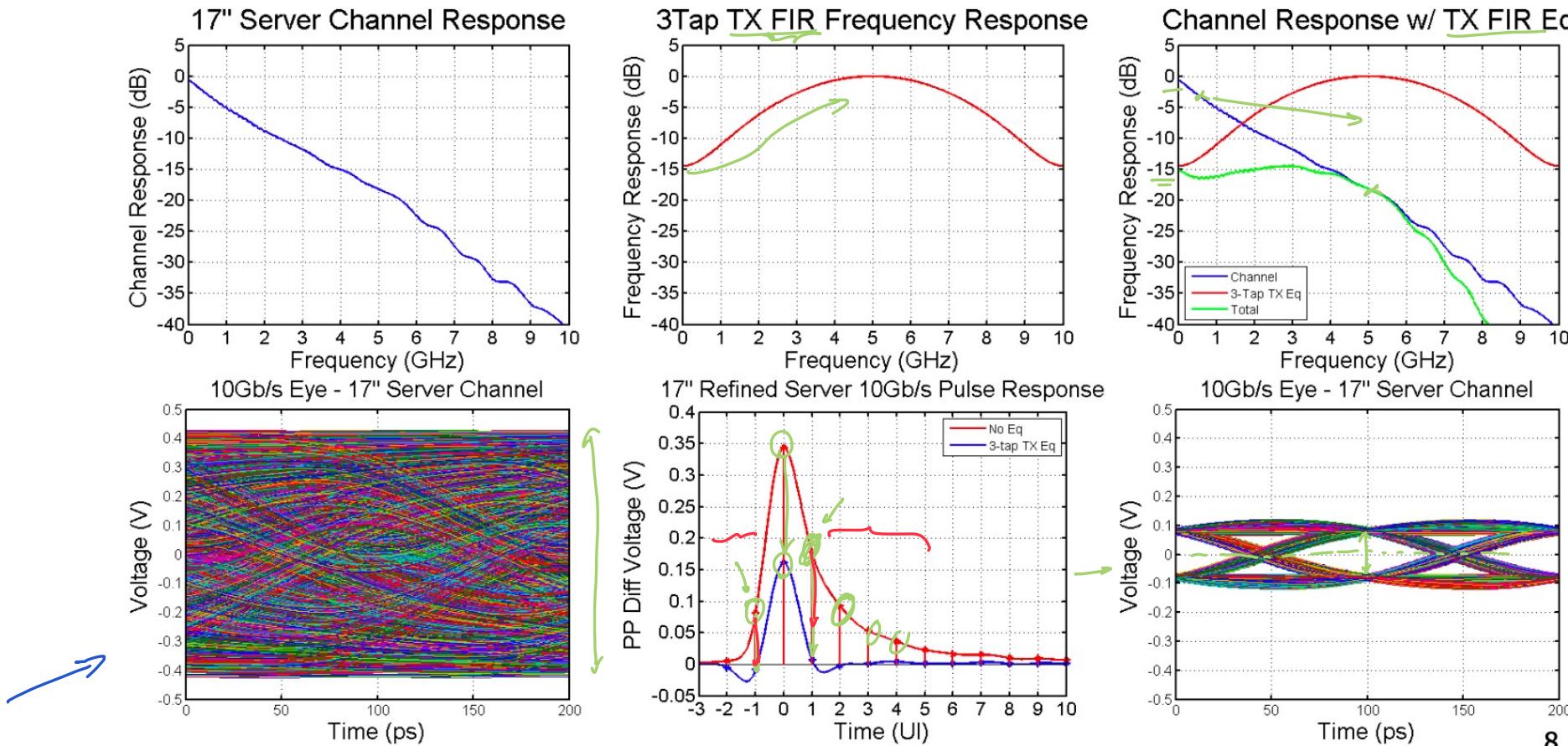
# Equalization



- **Basic goal is to “flatten” channel response**
  - I.e., in time domain, get back our nice clean pulse
  - For low-pass channel, equalizer boosts high frequencies

# Channel Equalization

- Equalization goal is to flatten the frequency response out to the Nyquist Frequency and remove time-domain ISI



# Equalizer Types

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More alphabet soup...

- CTLE, ZFE, DFE, RX FIR, MMSE, ...

- Three basic distinctions:

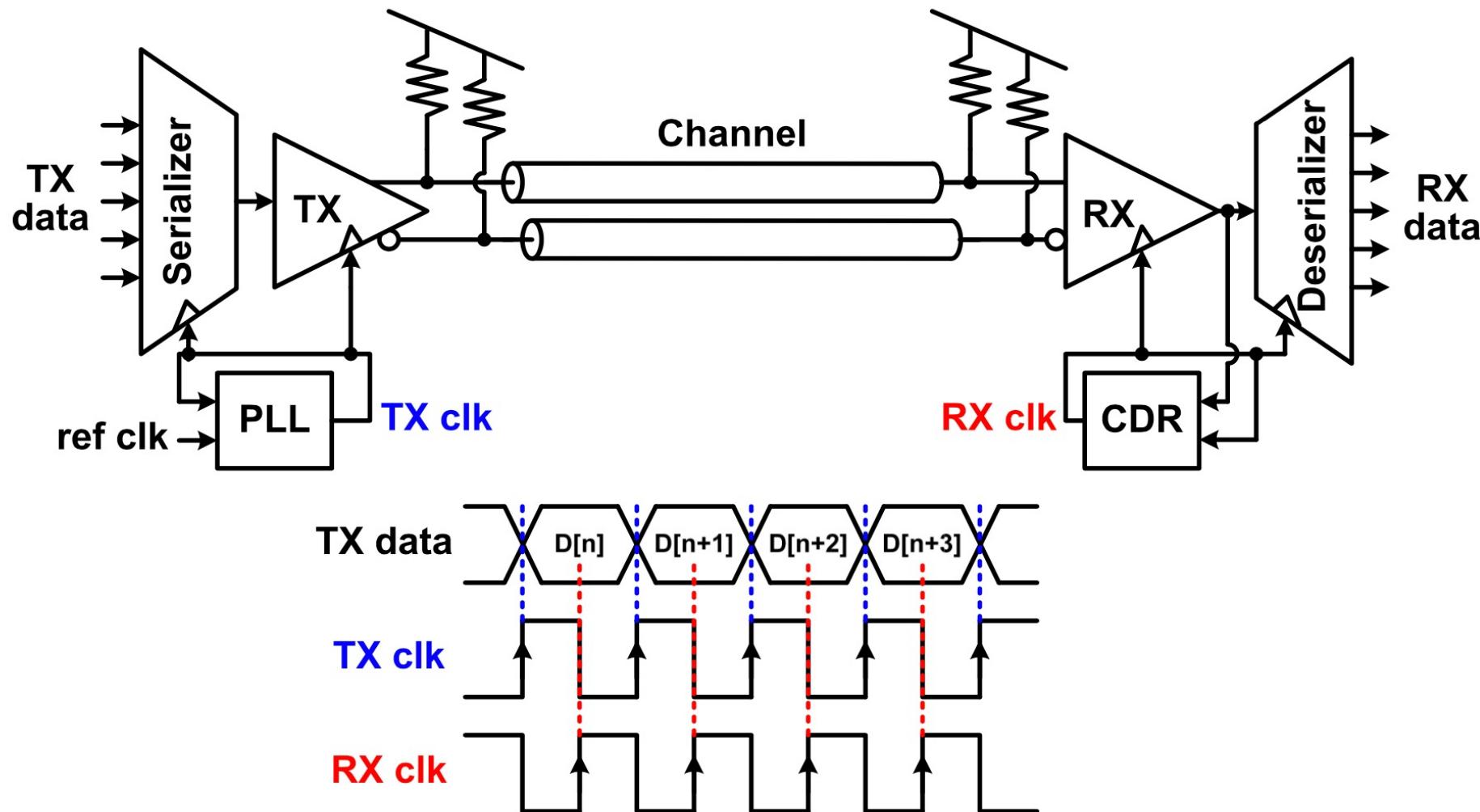
- Linear vs. Non-Linear

- ② • Continuous Time vs. Discrete Time

- ✗ • Minimize ISI vs. Minimize ISI + Noise

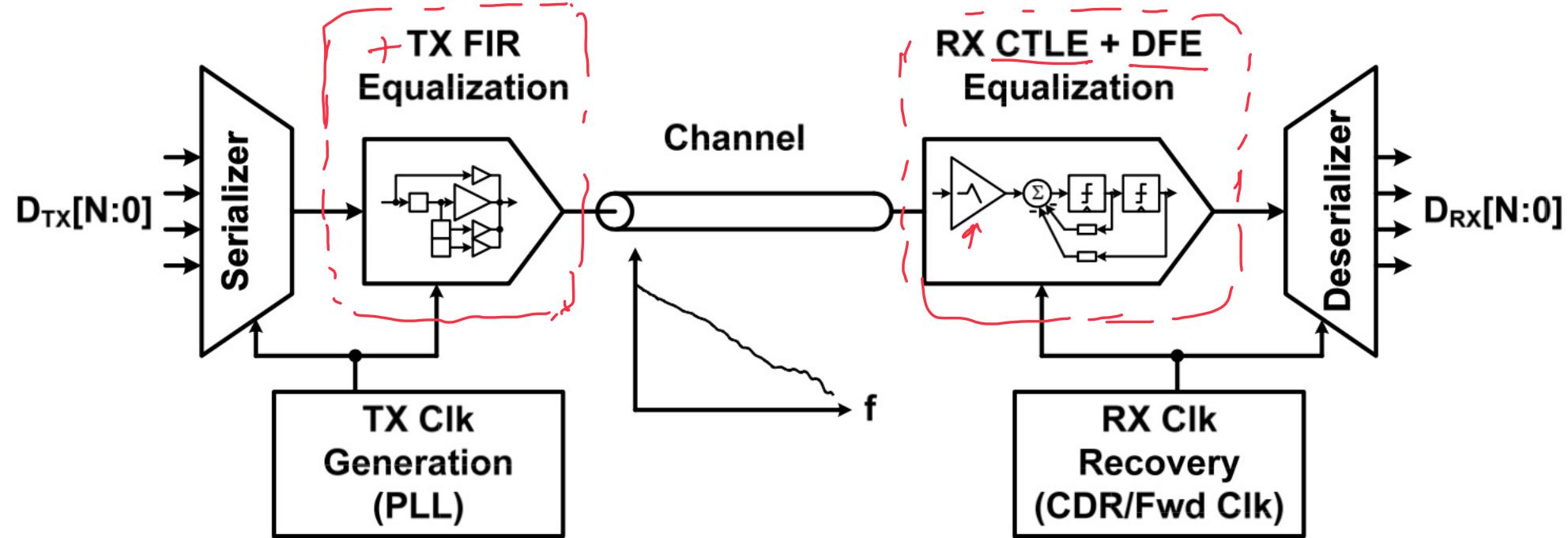
- ① • Tx vs. Rx

# High-Speed Electrical Link System



[Sam Palermo]

# Link with Equalization



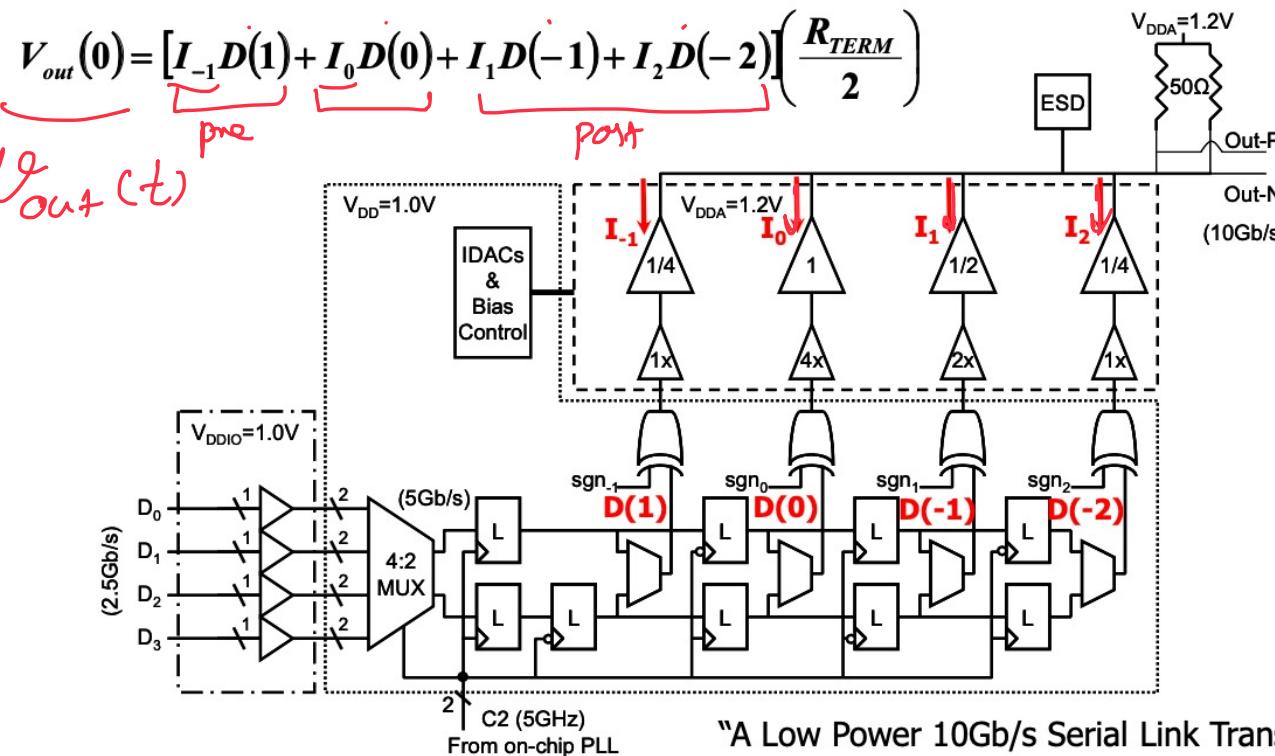
[Sam Palermo]

# TX FIR Equalization

FFE

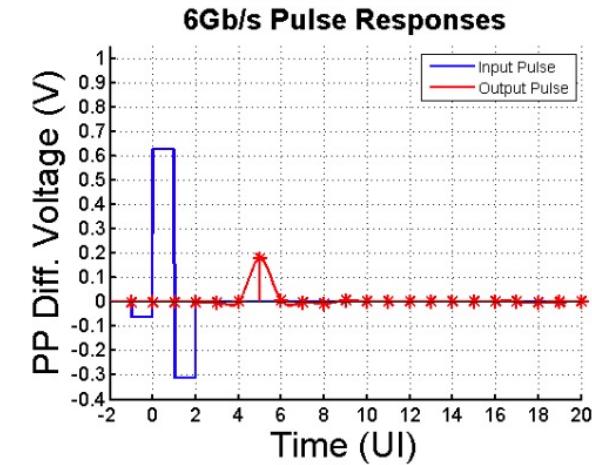
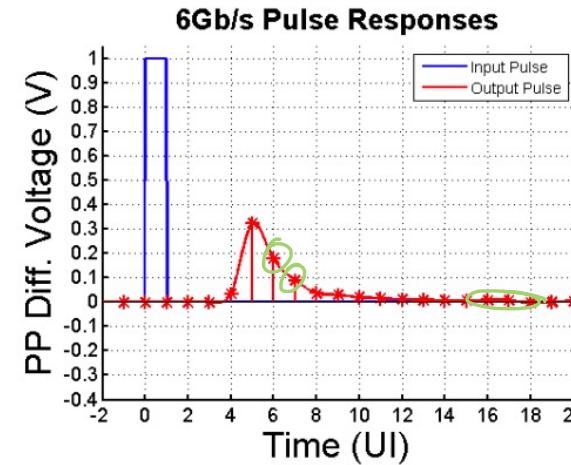
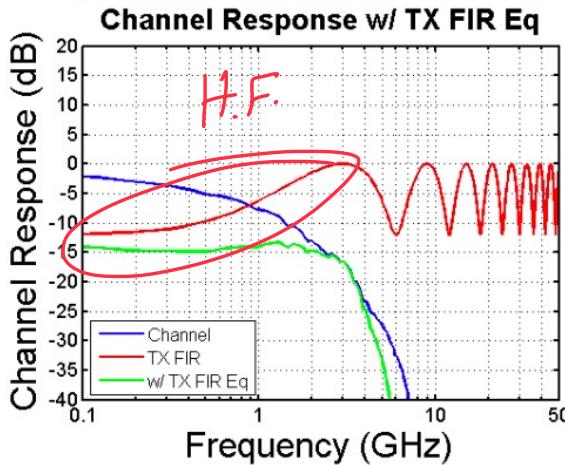
4-tap  
TX FIR

- TX FIR filter pre-distorts transmitted pulse in order to invert channel distortion at the cost of attenuated transmit signal (de-emphasis)

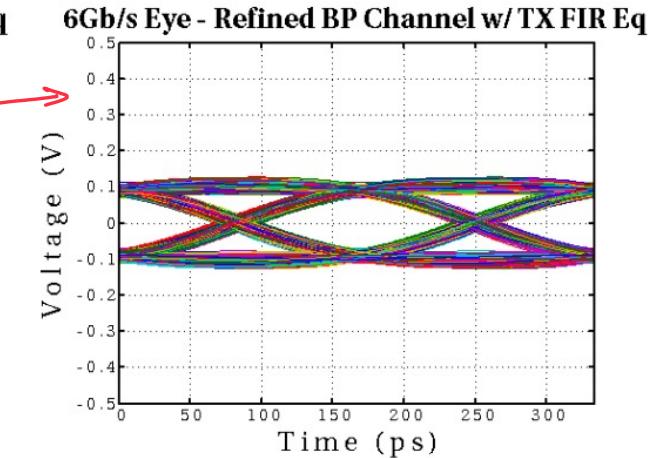
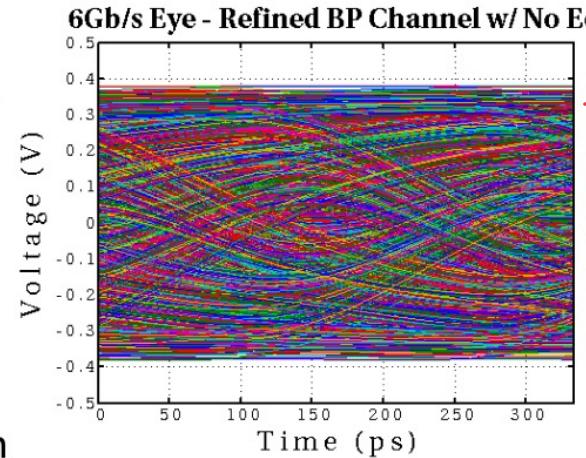


"A Low Power 10Gb/s Serial Link Transmitter in 90-nm CMOS," A. Rylyakov et al., CSICS 2005

# 6Gb/s TX FIR Equalization Example

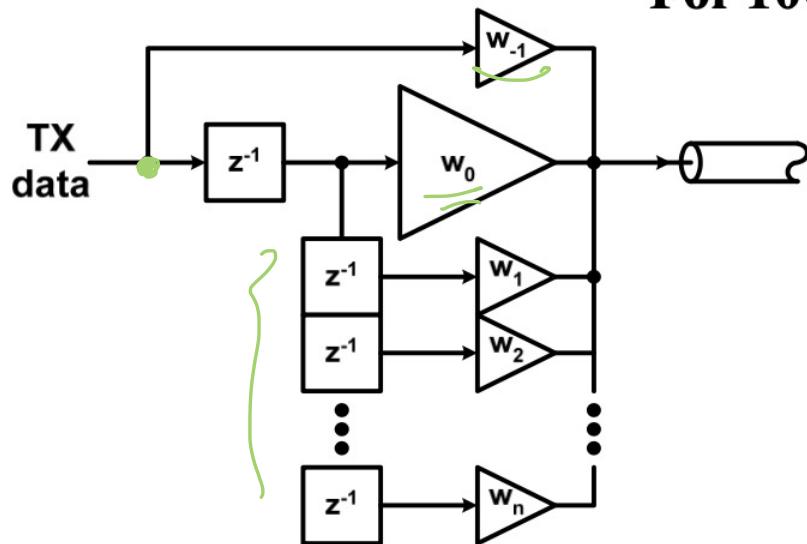


- Pros
  - ✓ Simple to implement
  - ✓ Can cancel ISI in precursor and beyond filter span
  - Doesn't amplify noise
  - Can achieve 5-6bit resolution
- Cons
  - ✗ Attenuates low frequency content due to peak-power limitation
  - Need a "back-channel" to tune filter taps



# TX FIR Equalization – Time Domain

For 10Gbps :  $W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$



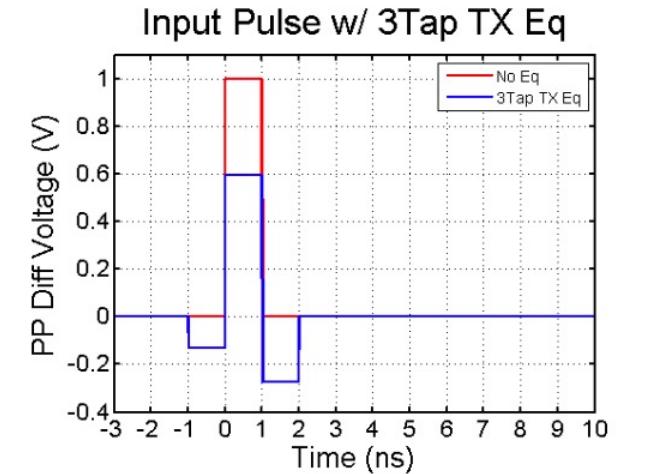
$$\mathbf{W} = [-0.131 \quad 0.595 \quad -0.274]$$

## Low Frequency Response (Sum Taps)

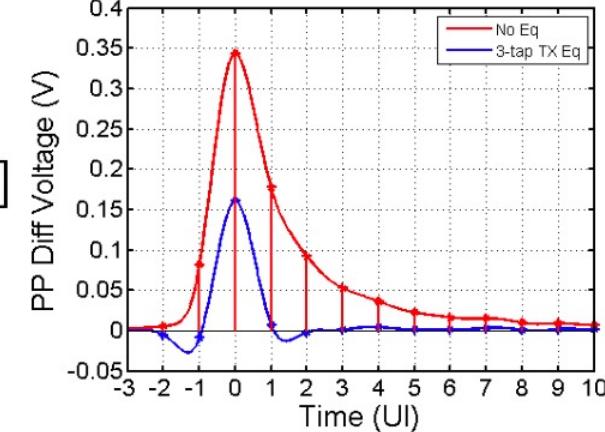
$$[\dots \quad 1 \quad 1 \quad 1 \quad \dots] * [-0.131 \quad 0.595 \quad -0.274] = [\dots \quad 0.190 \quad 0.190 \quad 0.190 \quad \dots]$$

## Nyquist Frequency Response (Sum Taps w/ Alternating Polarity)

$$[\dots \quad -1 \quad 1 \quad -1 \quad \dots] * [-0.131 \quad 0.595 \quad -0.274] = [\dots \quad 1 \quad -1 \quad 1 \quad \dots]$$



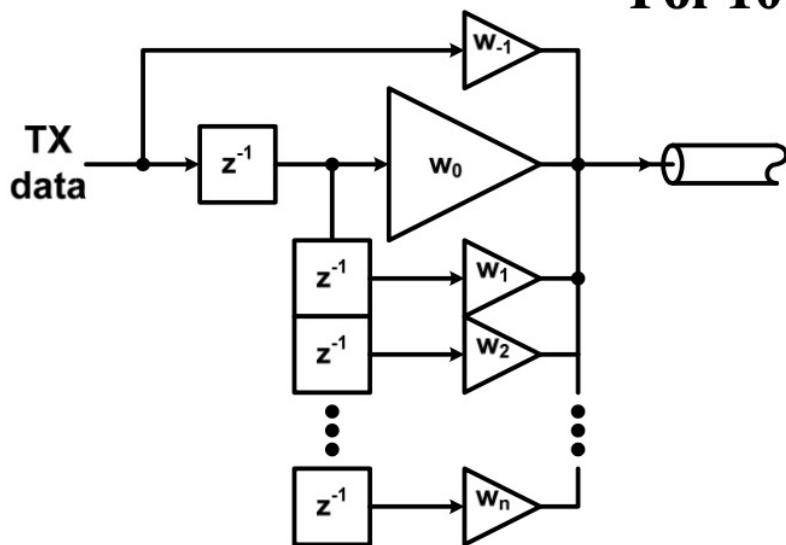
17" Refined Server 10Gb/s Pulse Response



[Sam Palermo]

# TX FIR Equalization – Freq. Domain

For 10Gbps :  $W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$

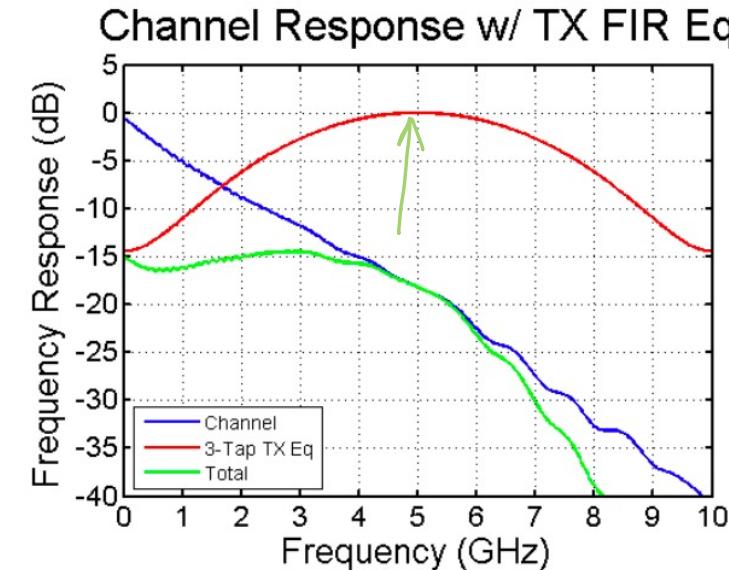


$$W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$$

$$\text{w/ } z = e^{j2\pi f T_s} = \cos(2\pi f T_s) + j \sin(2\pi f T_s)$$

Low Frequency Response ( $f = 0$ )

$$z = \cos(0) + j \sin(0) = 1 \Rightarrow W(f = 0) = 0.190 \Rightarrow -14.4dB$$



Nyquist Frequency Response  $\left( f = \frac{1}{2T_s} \right)$

$$z = \cos(\pi) + j \sin(\pi) = -1 \Rightarrow W\left(f = \frac{1}{2T_s}\right) = -1 \Rightarrow 0dB$$

- Equalizer has 14.4dB of frequency peaking

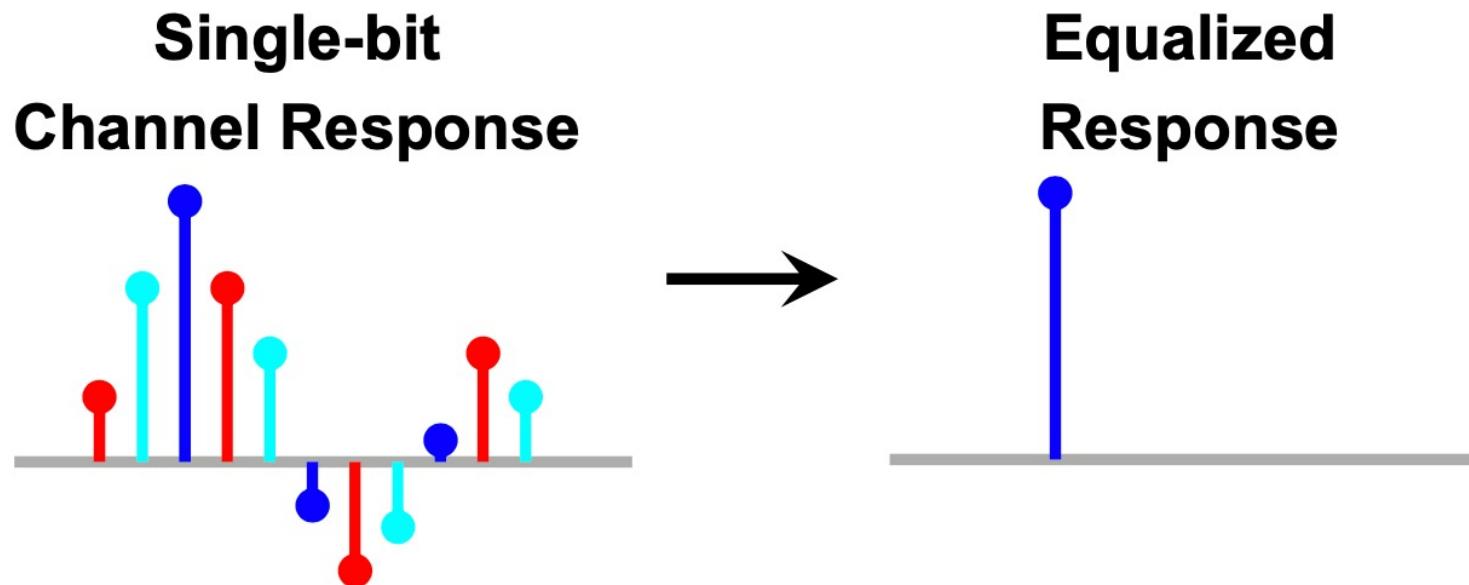
- Attenuates DC at -14.4dB and passes Nyquist frequency at 0dB

Note:  $T_s = T_b = 100ps$

[Sam Palermo]

# Setting the Coefficients

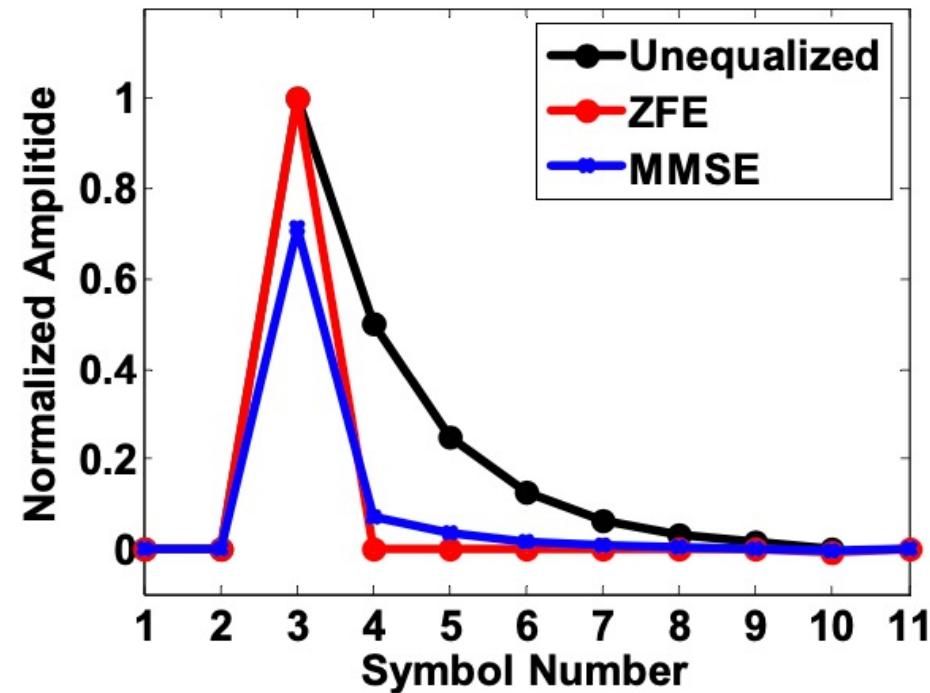
- Assume channel response is known for now
  - See later how to estimate it
- Most basic approach: zero-forcing (ZFE)



[Elad Alon]

# MMSE vs. ZFE, Limitations

- MMSE allows residual ISI
  - But amplifies noise less

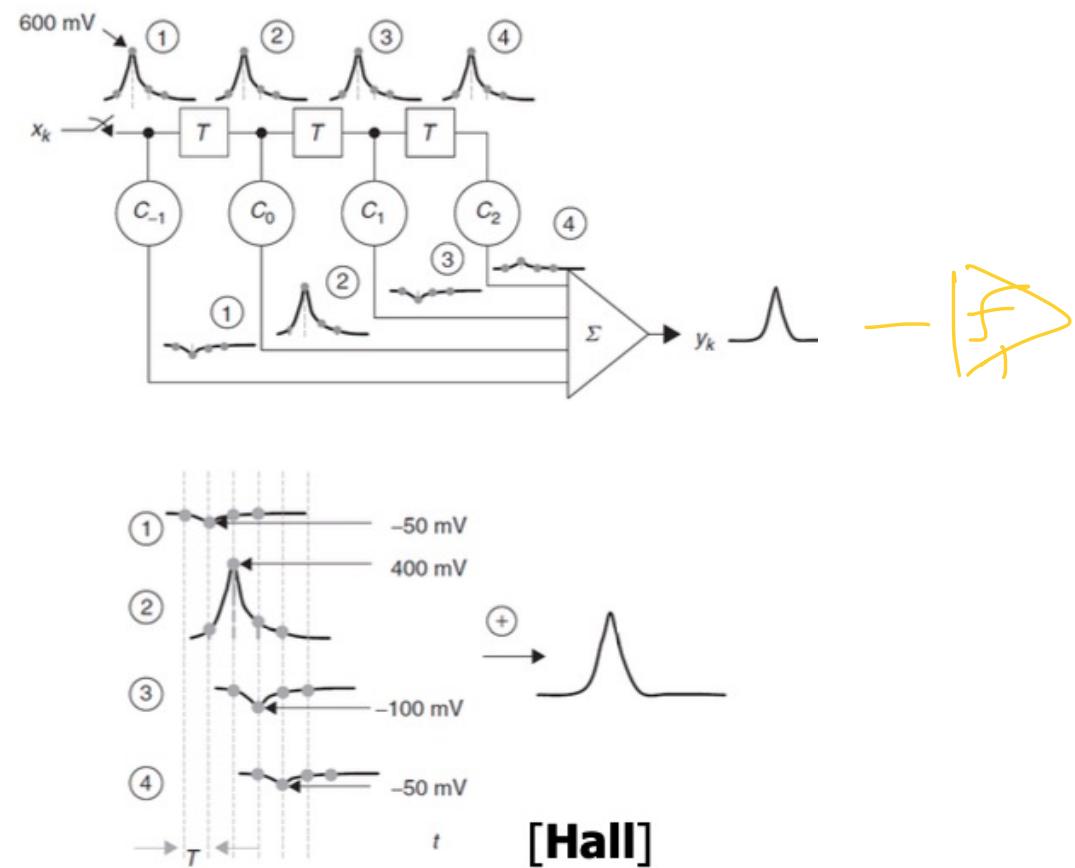


- Unfortunately, MMSE not so straightforward to apply in links
  - Harder to adapt (more later)
  - Noise may not be known

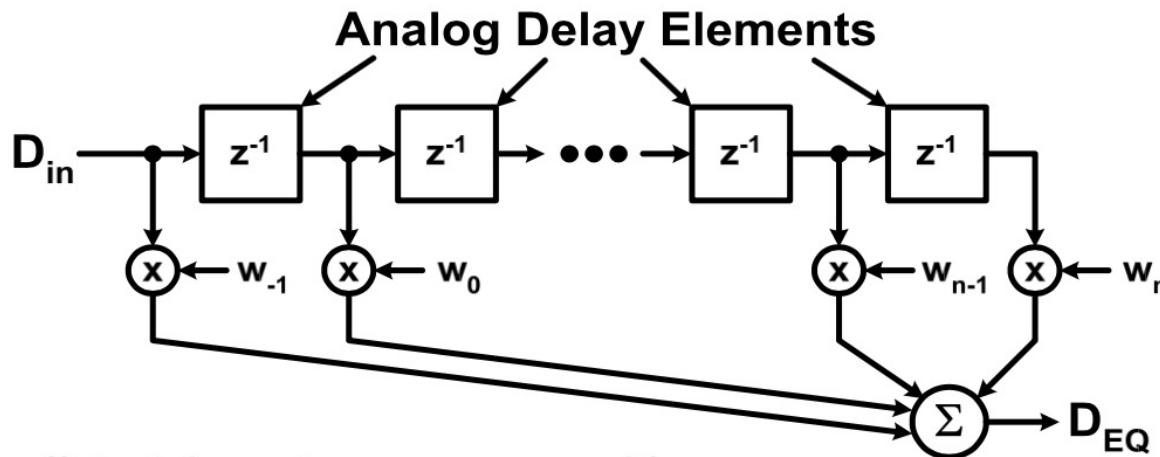
[Elad Alon]

# RX FIR Equalization

- Delay analog input signal and multiply by equalization coefficients
- Pros
  - ✓ With sufficient dynamic range, can amplify high frequency content (rather than attenuate low frequencies)
  - Can cancel ISI in pre-cursor and beyond filter span
  - ✓ Filter tap coefficients can be adaptively tuned without any back-channel
- Cons
  - Amplifies noise/crosstalk
  - ✗ Implementation of analog delays
  - Tap precision

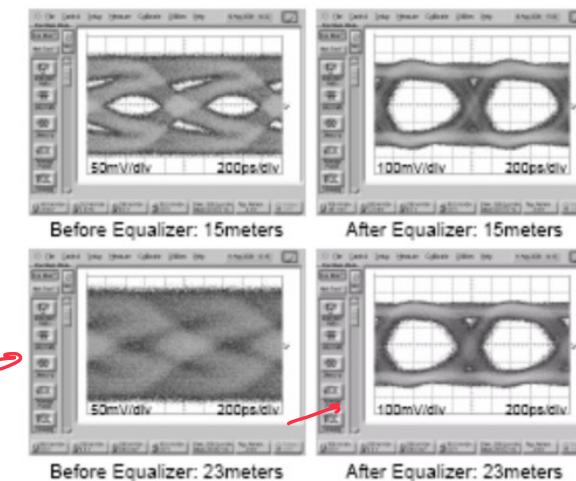


# RX Equalization #1: RX FIR



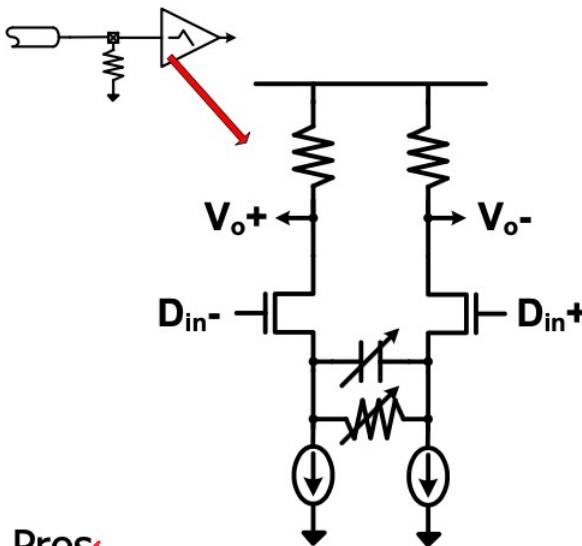
- Pros
  - With sufficient dynamic range, can amplify high frequency content (rather than attenuate low frequencies)
  - Can cancel ISI in pre-cursor and beyond filter span
  - Filter tap coefficients can be adaptively tuned without any back-channel
- Cons
  - Amplifies noise/crosstalk
  - Implementation of analog delays
  - Tap precision

Eye-Pattern Diagrams at 1Gb/s on CAT5e\*

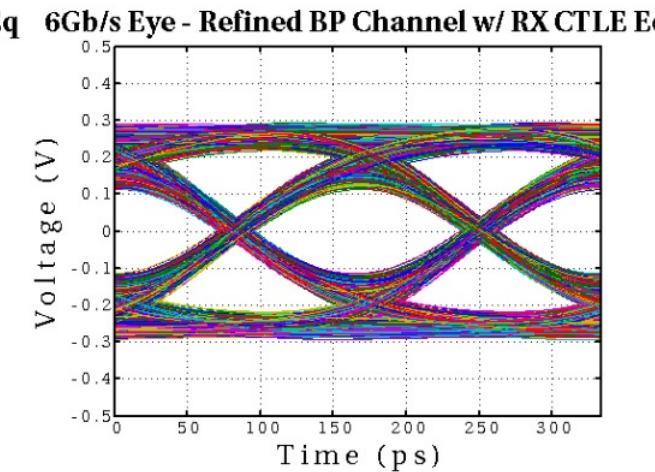
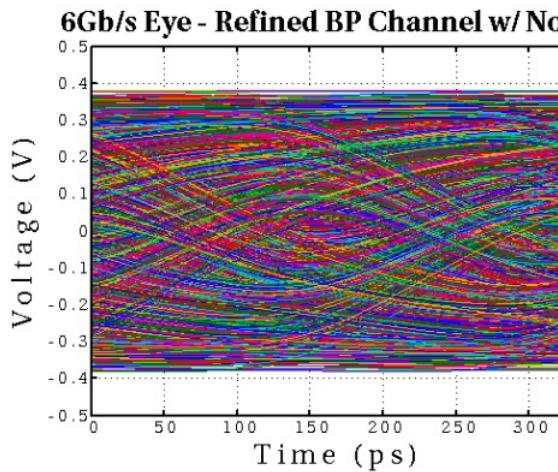
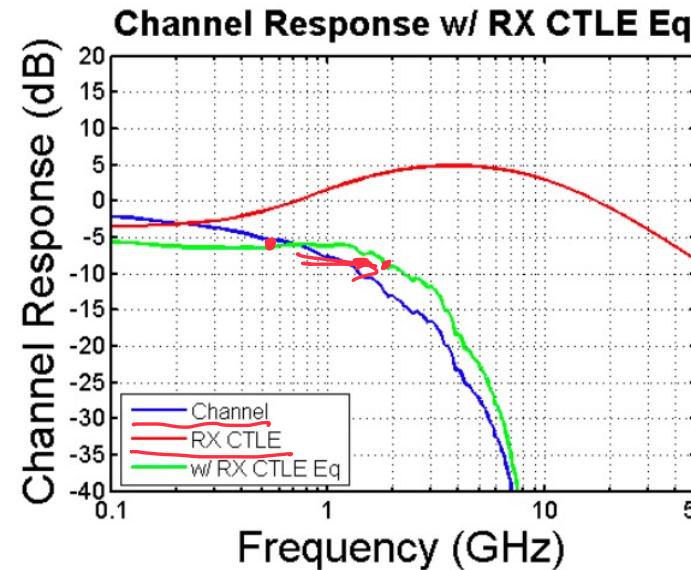


\*D. Hernandez-Garduno and J. Silva-Martinez, "A CMOS 1Gb/s 5-Tap Transversal Equalizer based on 3<sup>rd</sup>-Order Delay Cells," ISSCC, 2007.

# RX Equalization #2: RX CTLE

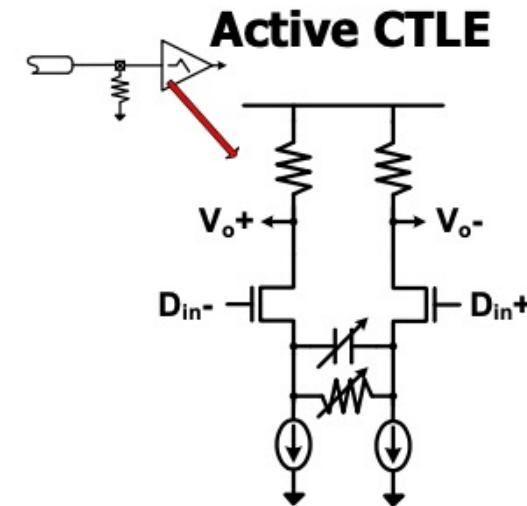
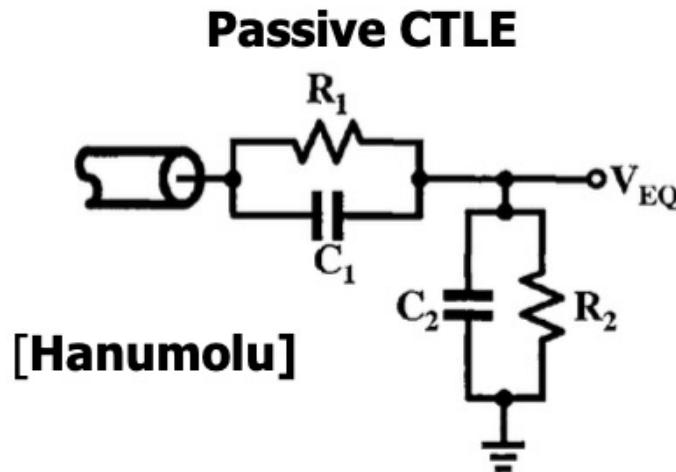
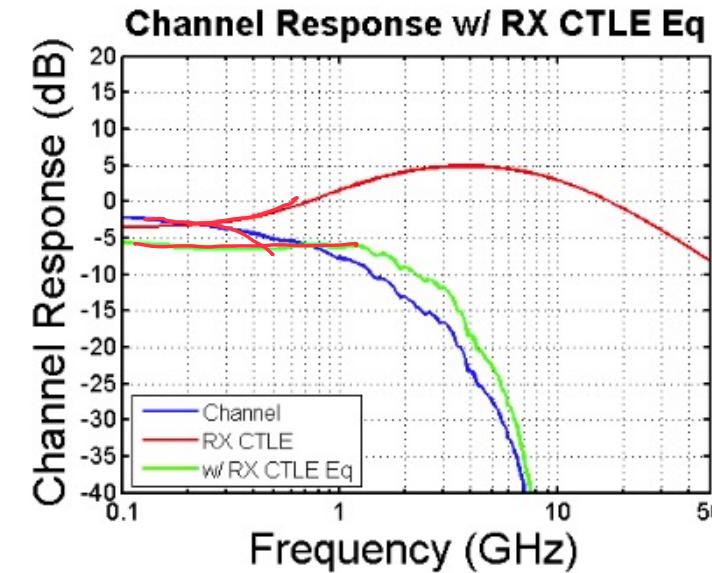


- Pros
  - ✓ Provides gain and equalization with low power and area overhead
  - Can cancel both precursor and long-tail ISI
- Cons
  - Generally limited to 1st order compensation
  - Amplifies noise/crosstalk
  - PVT sensitivity
  - Can be hard to tune



# RX Continuous-Time Linear Equalizer (CTLE)

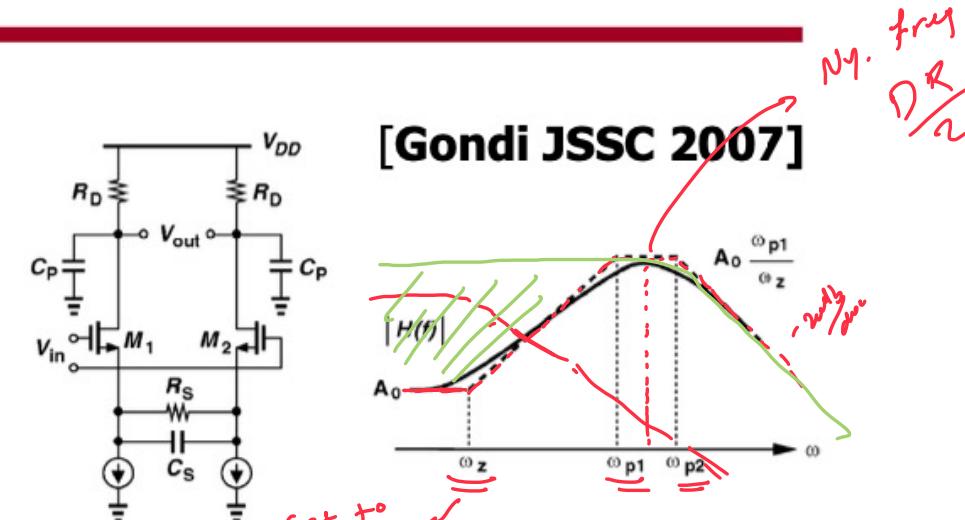
- Passive R-C (or L) can implement high-pass transfer function to compensate for channel loss
- Cancel both precursor and long-tail ISI
- Can be purely passive or combined with an amplifier to provide gain



[Sam Palermo]

# Active CTLE

- Input amplifier with RC degeneration can provide frequency peaking with gain at Nyquist frequency
- Potentially limited by gain-bandwidth of amplifier
- Amplifier must be designed for input linear range
  - Often TX eq. provides some low frequency attenuation
- Sensitive to PVT variations and can be hard to tune
- Generally limited to 1<sup>st</sup>-order compensation



$$H(s) = \frac{g_m}{C_p} \frac{s + \frac{1}{R_s C_s}}{s + \frac{1 + g_m R_s / 2}{R_s C_s} \left( s + \frac{1}{R_d C_p} \right)}$$

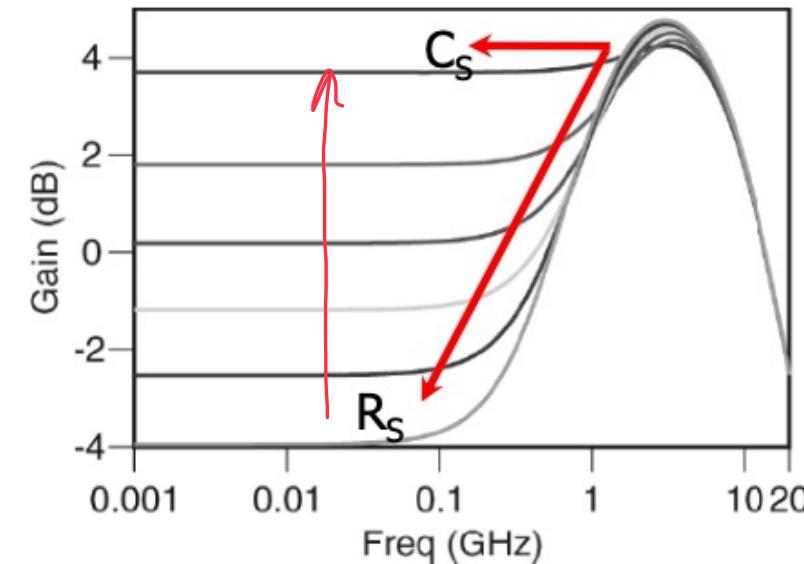
$$\omega_z = \frac{1}{R_s C_s}, \quad \omega_{p1} = \frac{1 + g_m R_s / 2}{R_s C_s}, \quad \omega_{p2} = \frac{1}{R_d C_p}$$

$$\text{DC gain} = \frac{g_m R_d}{1 + g_m R_s / 2}, \quad \text{Ideal peak gain} = g_m R_d$$

$$\text{Ideal Peaking} = \frac{\text{Ideal peak gain}}{\text{DC gain}} = \frac{\omega_{p1}}{\omega_z} = 1 + g_m R_s / 2$$

# Active CTLE Tuning

- Tune degeneration resistor and capacitor to adjust zero frequency and 1<sup>st</sup> pole which sets peaking and DC gain
- Increasing  $C_S$  moves zero and 1<sup>st</sup> pole to a lower frequency w/o impacting (ideal) peaking
- Increasing  $R_S$  moves zero to lower frequency and increases peaking (lowers DC gain)
  - Minimal impact on 1<sup>st</sup> pole

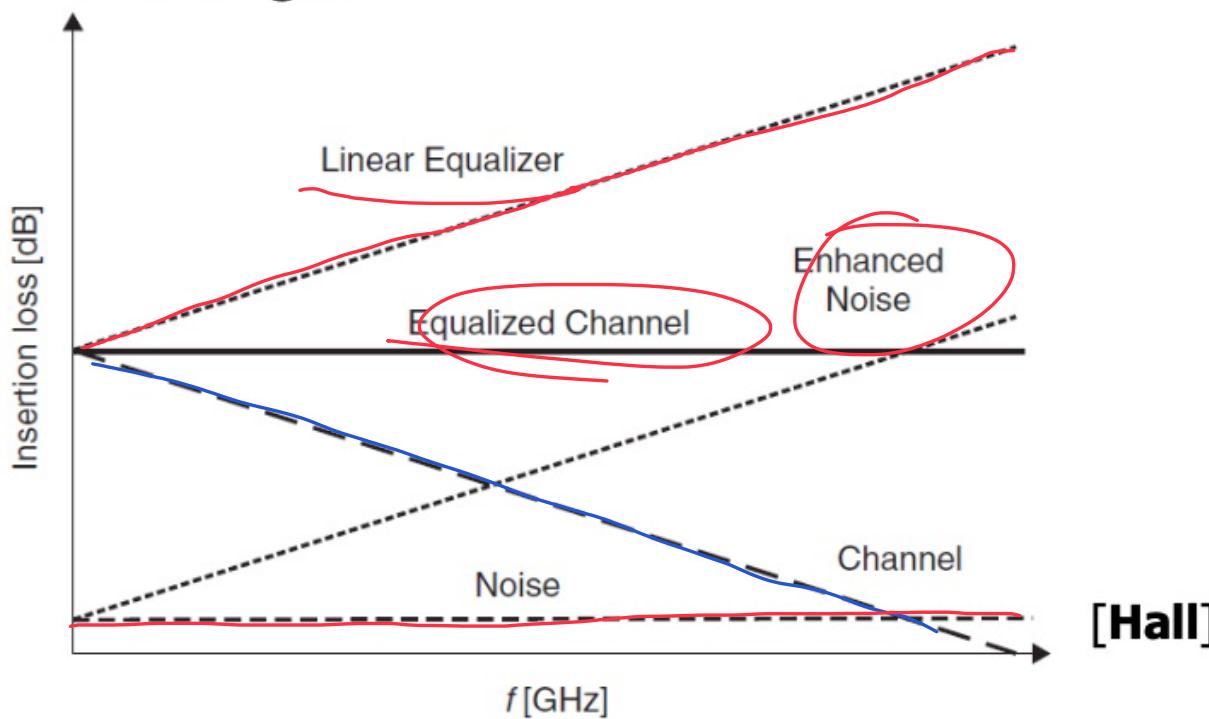


$$\omega_z = \frac{1}{R_S C_S}, \quad \omega_{p1} = \frac{1 + g_m R_S / 2}{R_S C_S}$$

[Sam Palermo]

# RX Equalization Noise Enhancement

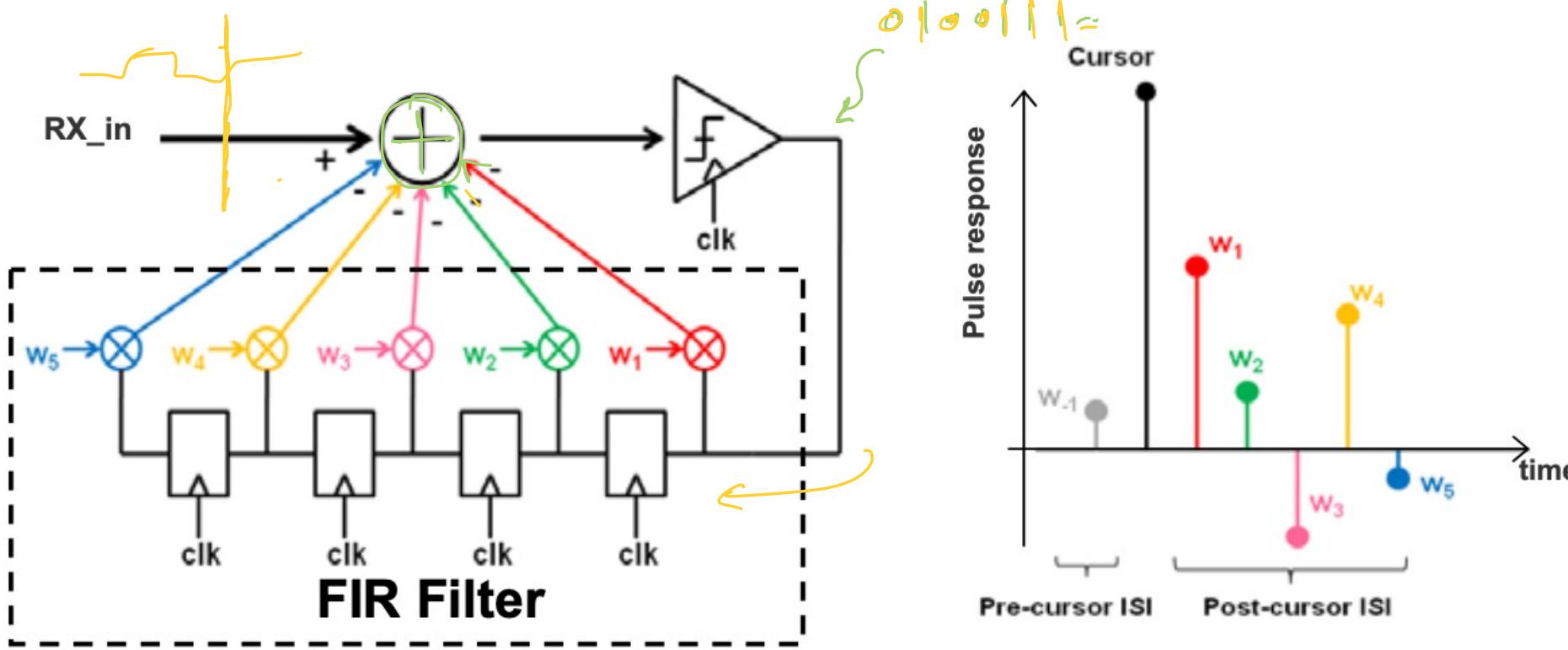
- Linear RX equalizers don't discriminate between signal, noise, and cross-talk
  - While signal-to-distortion (ISI) ratio is improved, SNR remains unchanged



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[Sam Palermo]

# Decision Feedback Equalization (DFE)



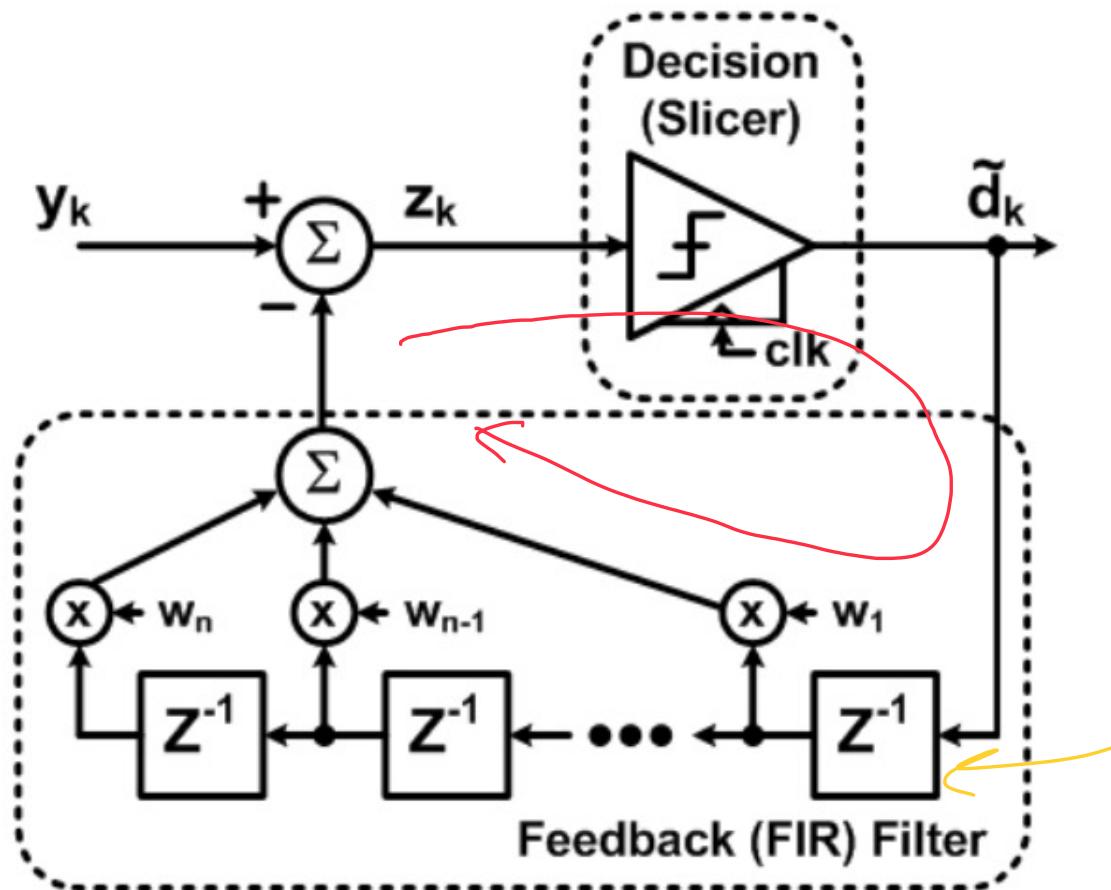
- Key advantage: no noise enhancement
  - Feedback signal based on “perfect” digital bits
  - ISI subtracted based on those bits

[Elad Alon]

# RX Decision Feedback Equalization (DFE)

- DFE is a **non-linear** equalizer
- Slicer makes a **symbol decision**, i.e. quantizes input
- ISI is then directly subtracted from the incoming signal via a feedback FIR filter

$$z_k = y_k - w_1 \tilde{d}_{k-1} - \dots - w_{n-1} \tilde{d}_{k-(n-1)} - w_n \tilde{d}_{k-n}$$



[Sam Palermo]

# RX Decision Feedback Equalization (DFE)

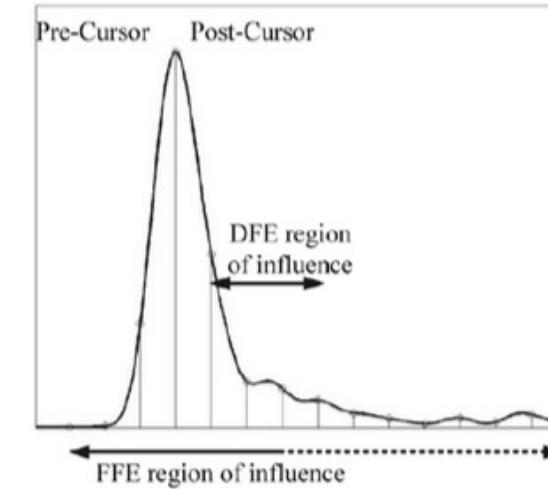
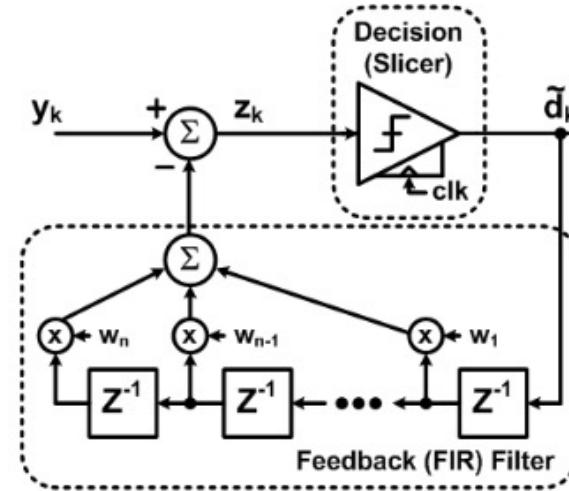
- Pros

- Can boost high frequency content without noise and crosstalk amplification
- Filter tap coefficients can be adaptively tuned without any back-channel

- Cons

- ✗ Cannot cancel pre-cursor ISI
- Chance for error propagation
  - Low in practical links ( $BER=10^{-12}$ )
- Critical feedback timing path
- Timing of ISI subtraction complicates CDR phase detection

$$z_k = y_k - w_1 \tilde{d}_{k-1} - \dots - w_{n-1} \tilde{d}_{k-(n-1)} - w_n \tilde{d}_{k-n}$$

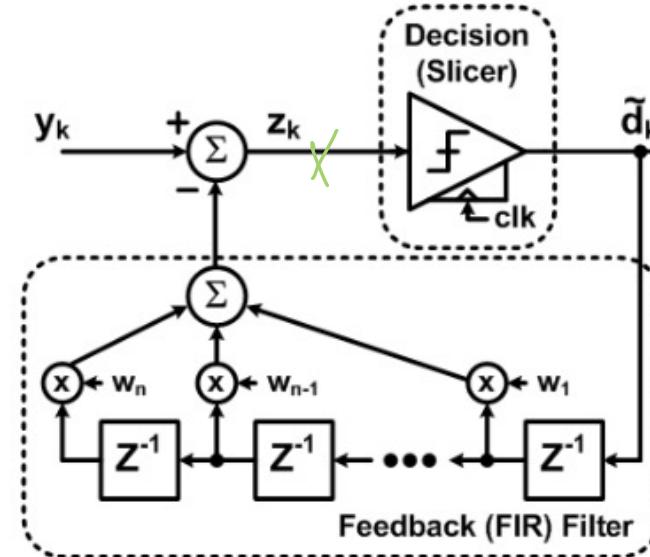


[Payne]

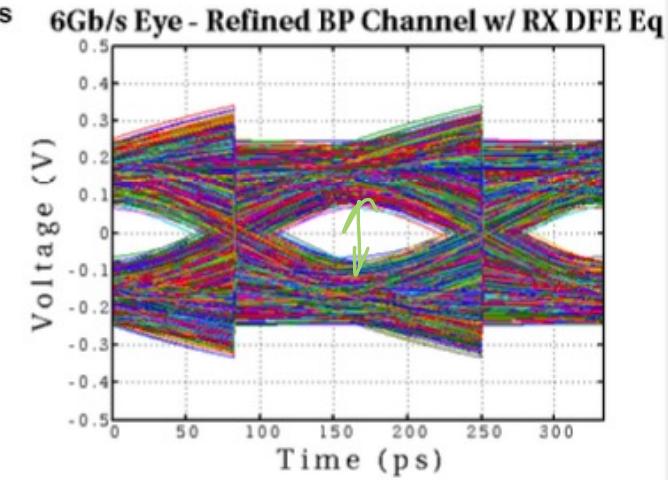
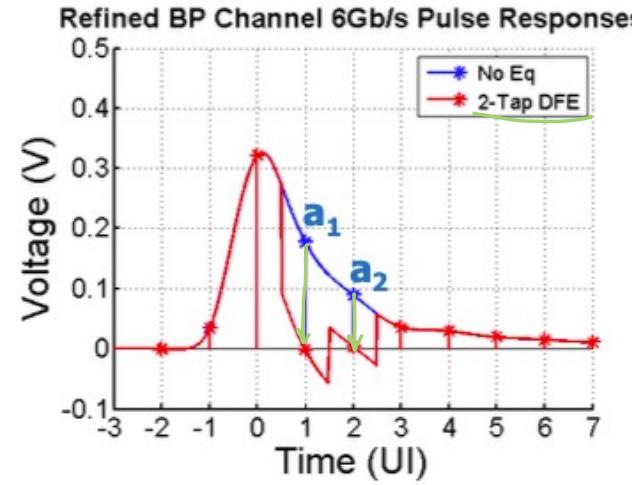
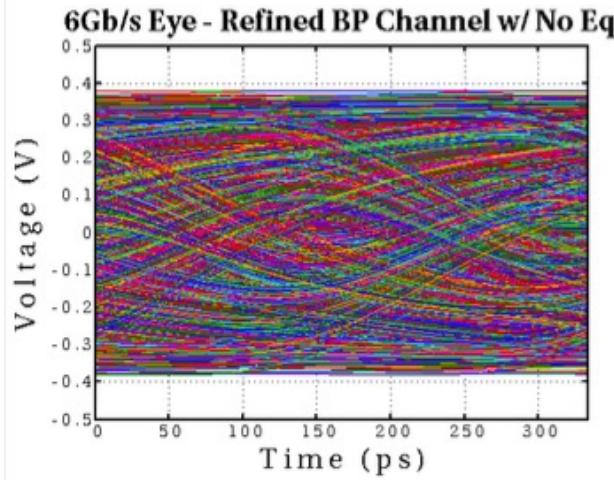
[Sam Palermo]

# DFE Example

- If only DFE equalization, DFE tap coefficients should equal the unequalized channel pulse response values  $[a_1 \ a_2 \ \dots \ a_n]$
- With other equalization, DFE tap coefficients should equal the pre-DFE pulse response values
  - DFE provides flexibility in the optimization of other equalizer circuits
  - i.e., you can optimize a TX equalizer without caring about the ISI terms that the DFE will take care of

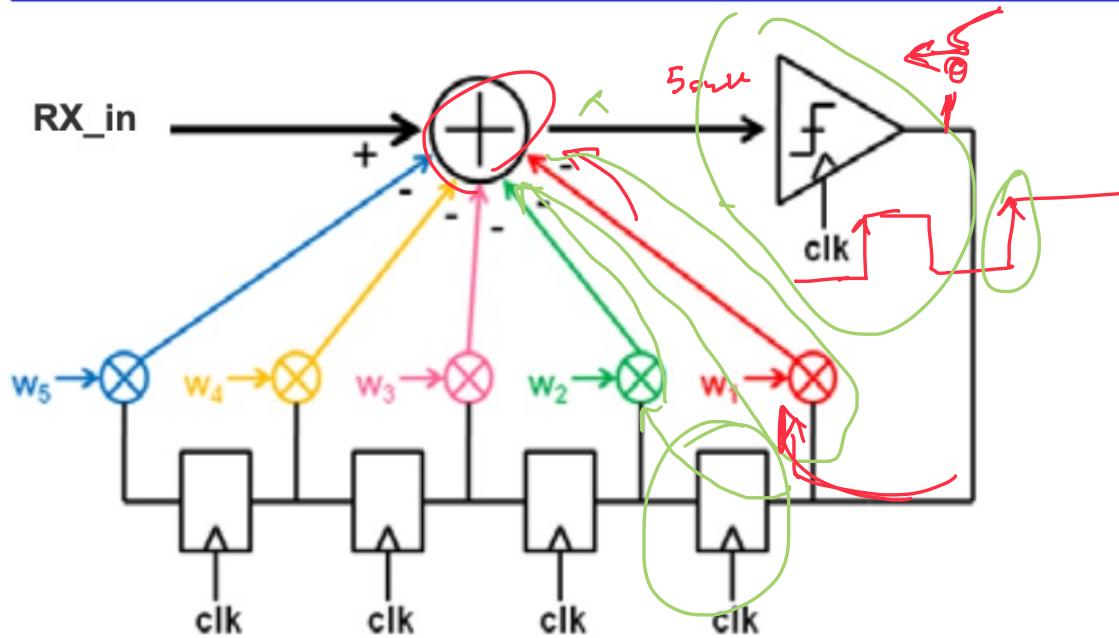


$$[w_1 \ w_2] = [a_1 \ a_2]$$



[Sam Palermo]

# DFE Issues: Timing

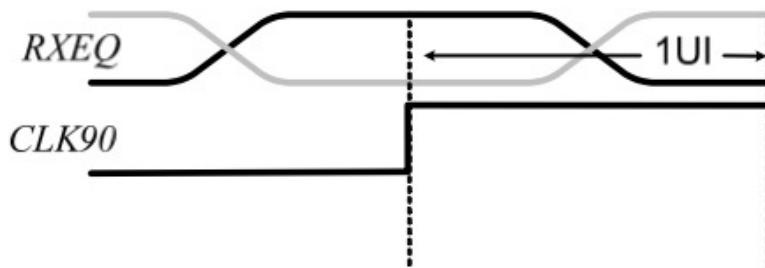
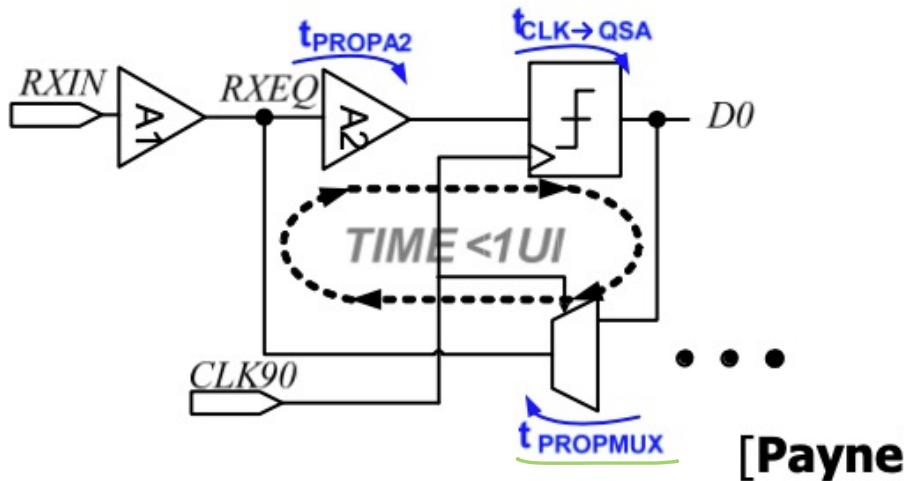


50 Gbaud → 20 ps  
3

- Need to do all of the following in at most 1UI:
  - Resolve the (small) bit
  - Scale the bit by the coefficient
  - Sum the new analog value

[Elad Alon]

# Direct Feedback DFE Critical Path

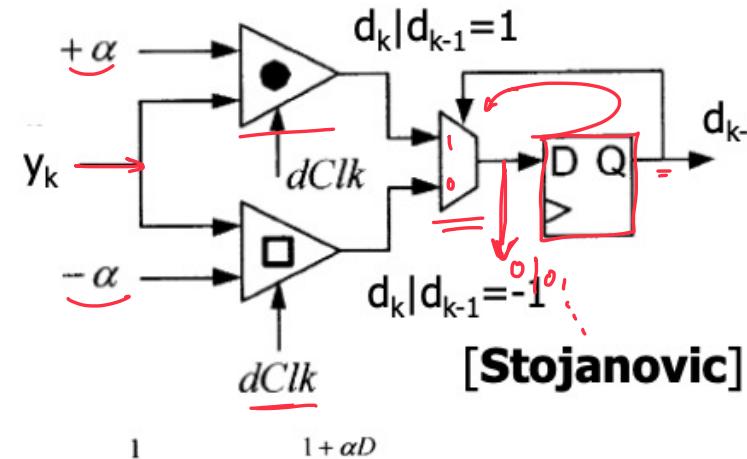
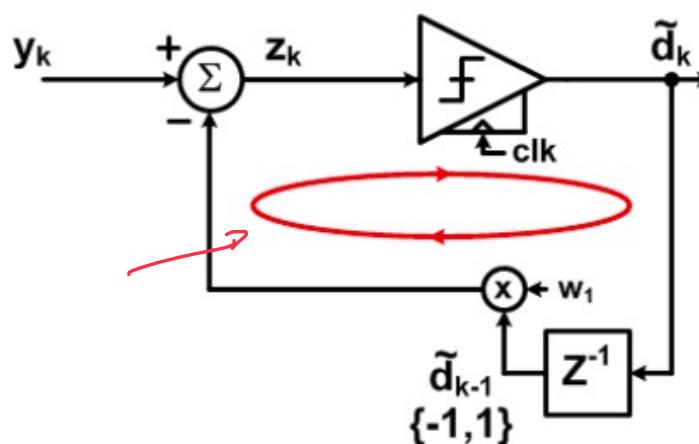


$$\underbrace{t_{CLK \rightarrow QSA}}_{\text{green}} + \underbrace{t_{PROPMUX}}_{\text{green}} + \underbrace{t_{PROPA2}}_{\text{green}} \leq 1UI$$

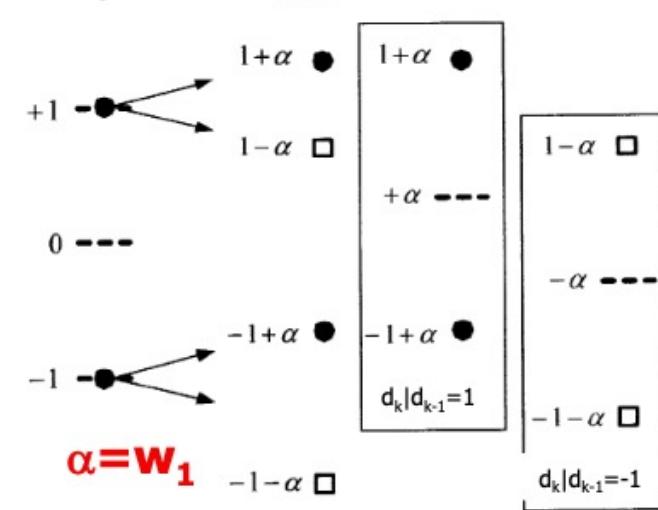
- Must resolve data and feedback in 1 bit period
  - TI design actually does this in ½UI for CDR

[Sam Palermo]

# DFE Loop Unrolling



- Instead of feeding back and subtracting ISI in 1UI
- Unroll loop and pre-compute 2 possibilities (1-tap DFE) with adjustable slicer threshold
- With increasing tap number, comparator number grows as  $2^{\# \text{taps}}$

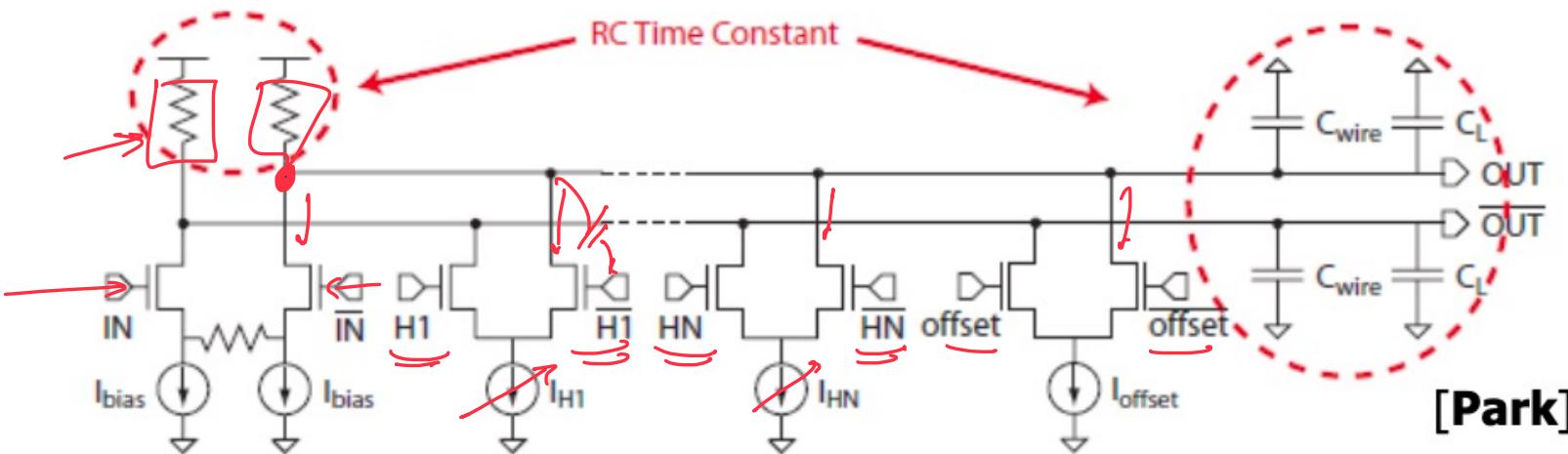


$$\tilde{d}_k = \begin{cases} \text{sgn}(y_k - w_1) & \text{"if" } \tilde{d}_{k-1} = 1 \\ \text{sgn}(y_k + w_1) & \text{"if" } \tilde{d}_{k-1} = -1 \end{cases}$$

2

[Sam Palermo]

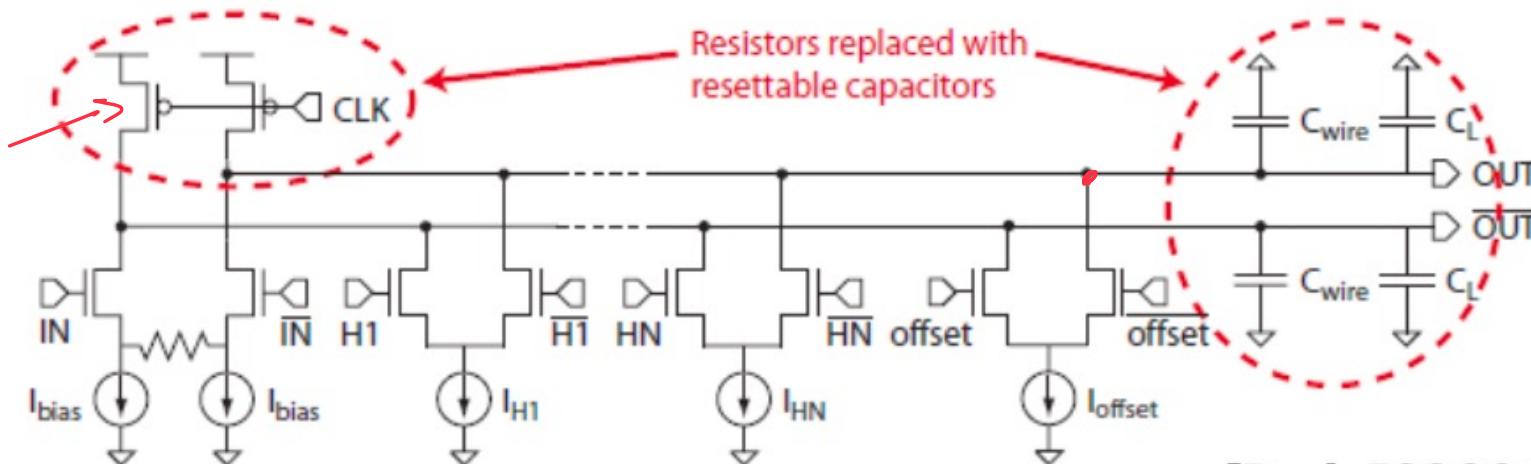
# DFE Resistive-Load Summer



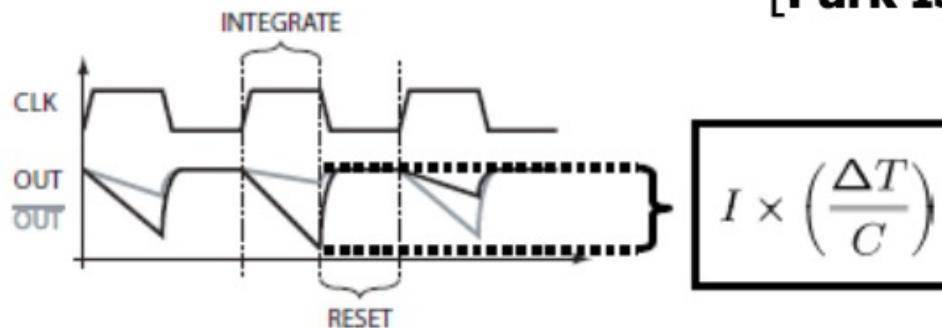
- Summer performance is critical for DFE operation
- Summer must settle within a certain level of accuracy (>95%) for ISI cancellation
- Trade-off between summer output swing and settling time
- Can result in large bias currents for input and taps

[Sam Palermo]

# DFE Integrating Summer



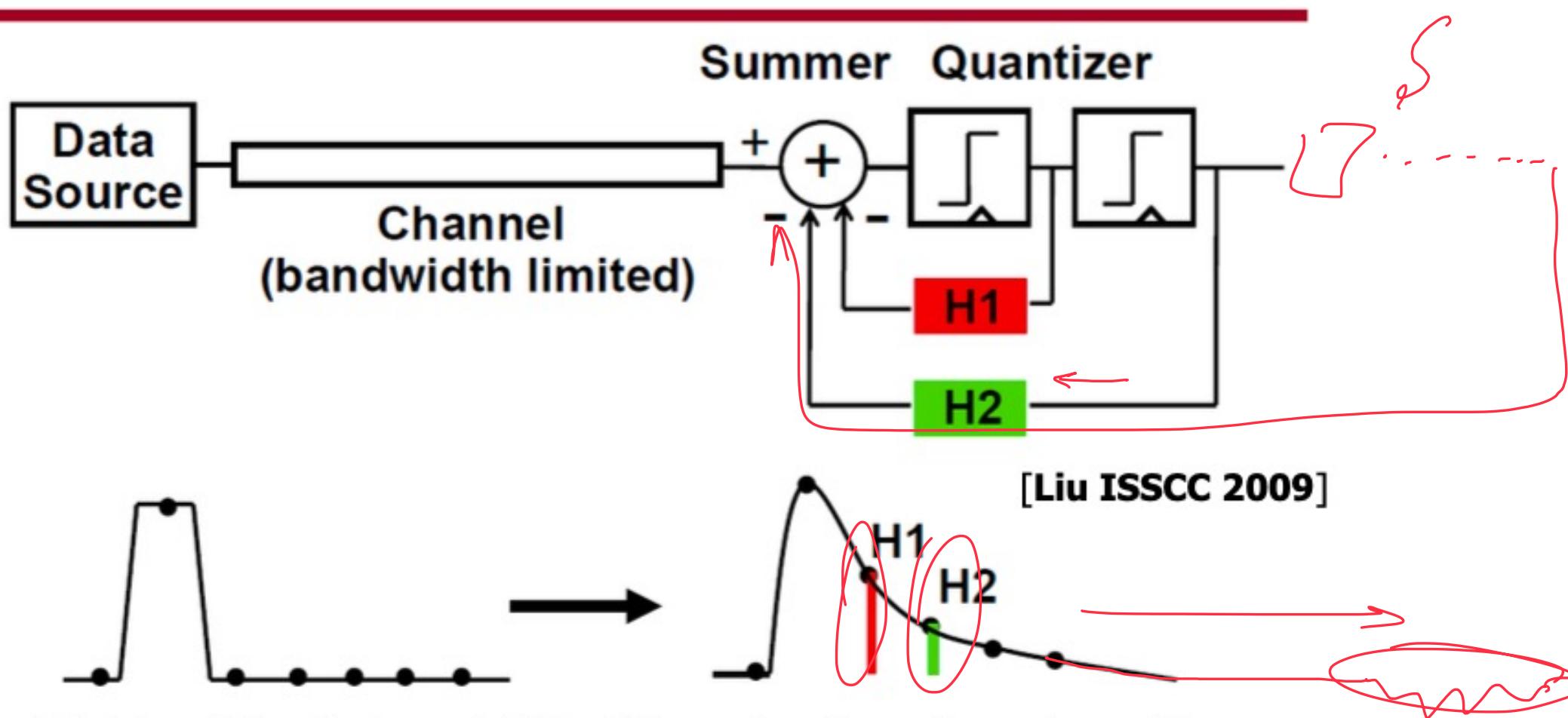
[Park ISSCC 2007]



- Integrating current onto load capacitances eliminates RC settling time
- Since  $\Delta T/C > R$ , bias current can be reduced for a given output swing
  - Typically a 3x bias current reduction

[Sam Palermo]

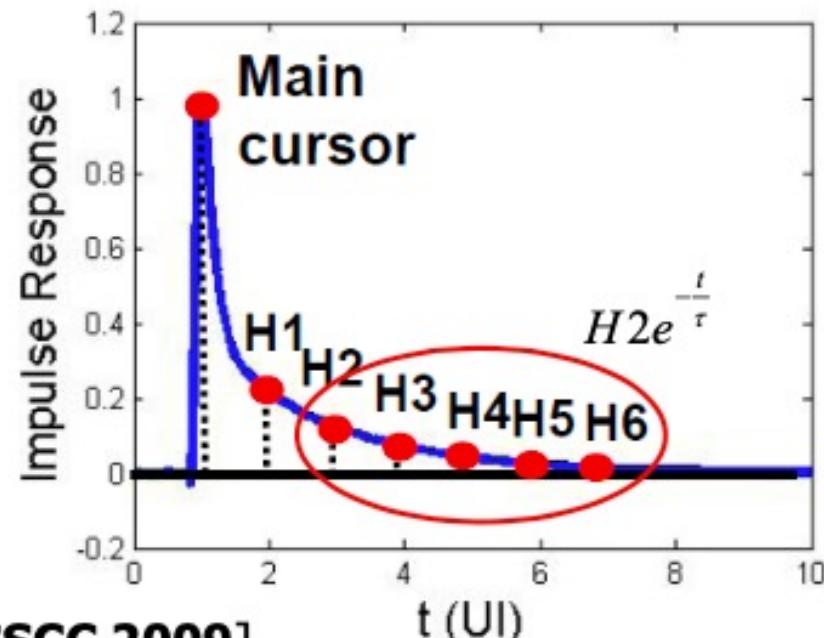
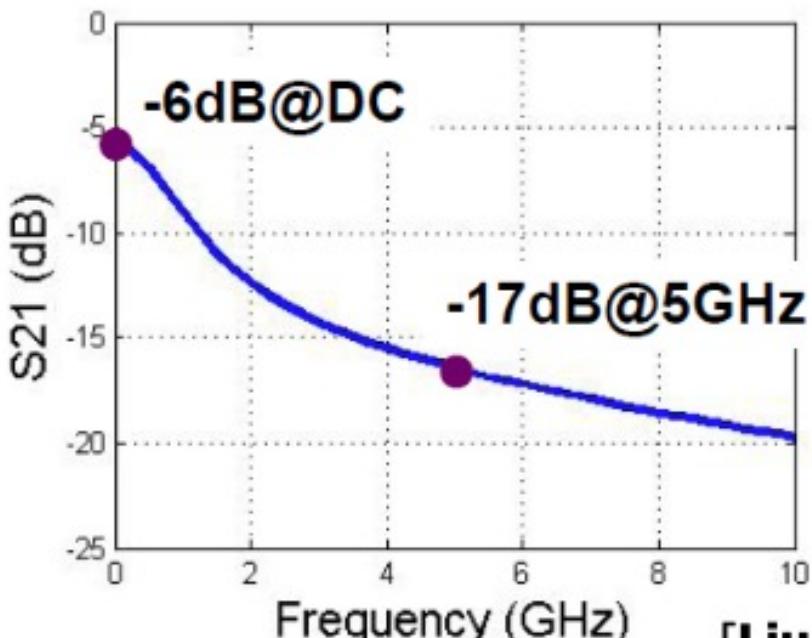
# DFE with Feedback FIR Filter



- DFE with 2-tap FIR filter in feedback will only cancel ISI of the first two post-cursors

[Sam Palermo]

# “Smooth” Channel

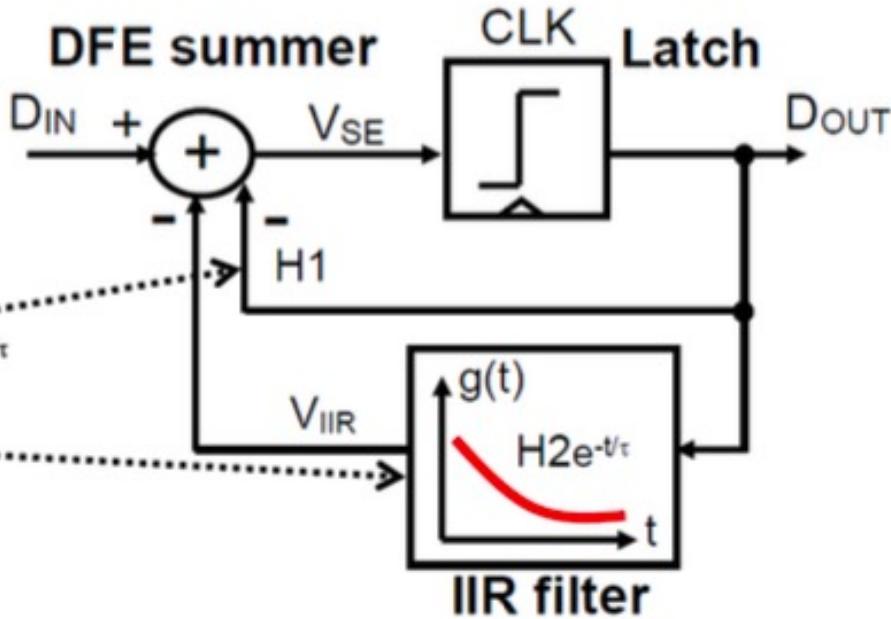
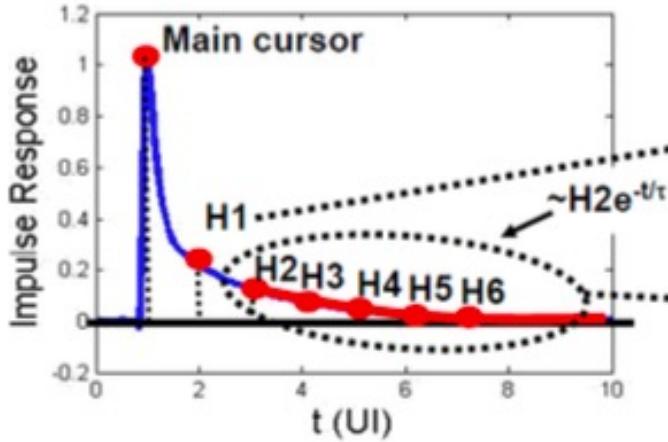


- A DFE with FIR feedback requires many taps to cancel ISI
- Smooth channel long-tail ISI can be approximated as exponentially decaying
  - Examples include on-chip wires and silicon carrier wires

[Sam Palermo]

# DFE with IIR Feedback

[Liu ISSCC 2009]



- Large 1<sup>st</sup> post-cursor H1 is canceled with normal FIR feedback tap
- Smooth long tail ISI from 2<sup>nd</sup> post-cursor and beyond is canceled with low-pass IIR feedback filter
- Note: channel needs to be smooth (not many reflections) in order for this approach to work well

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[Sam Palermo]