EE 437/538B: Integrated Systems Capstone/Design of Analog Integrated Circuits and Systems

Lecture 5: Optical TRx (Part 1)

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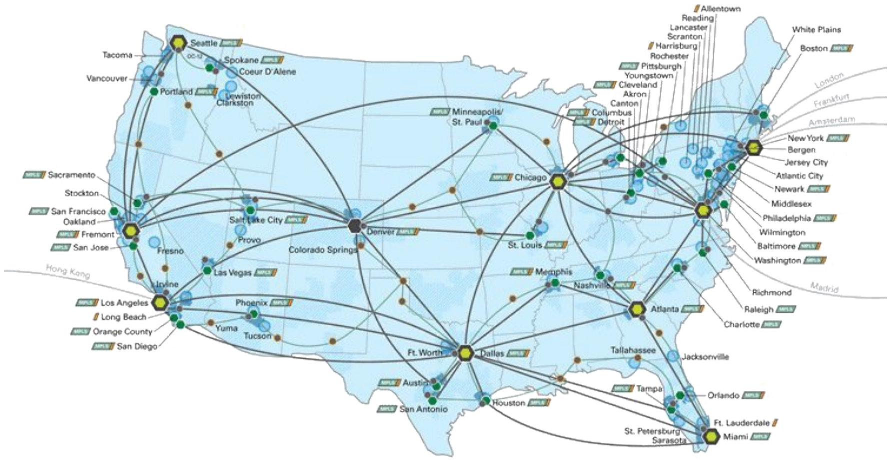
ELECTRICAL & COMPUTER ENGINEERING

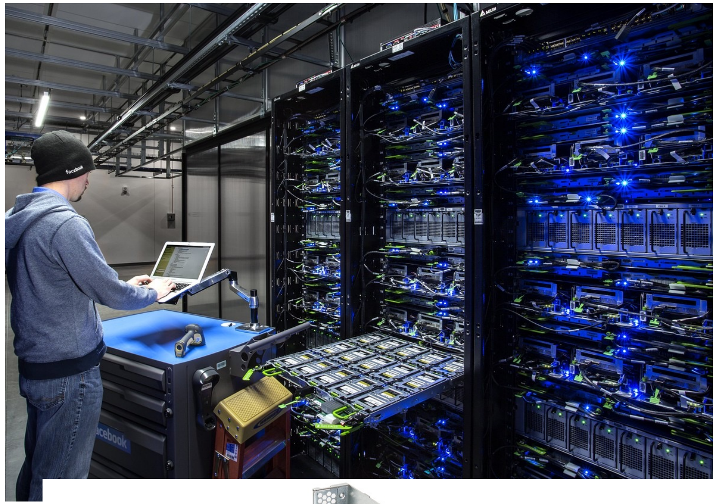
Emergence of Optical Links/Interconnects

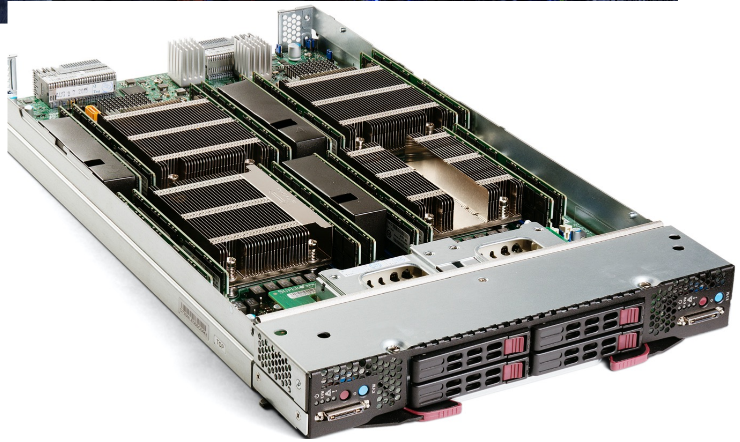
US IT Map



Large Data Centers

Server Racks/Blades





Inter-continents

inter-datacenter

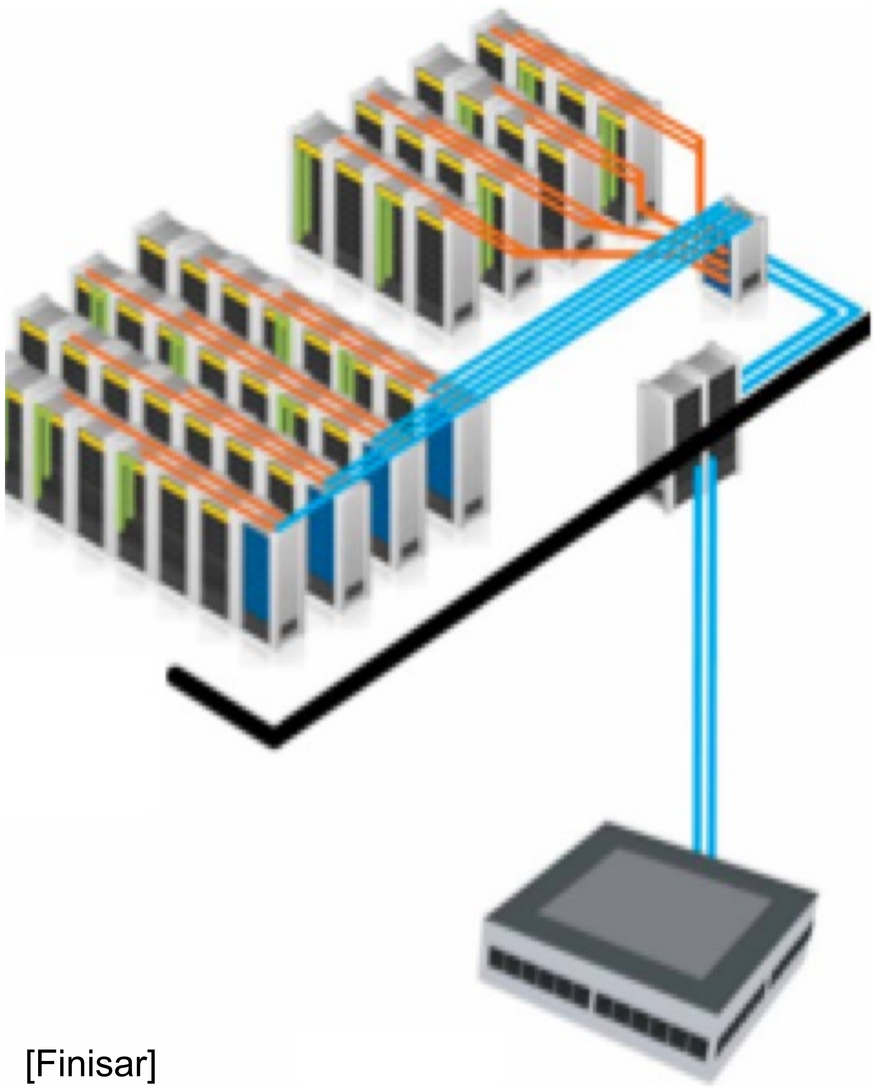
intra-data center

inter-rack

…

Chip-to-chip

Need for Optical I/O

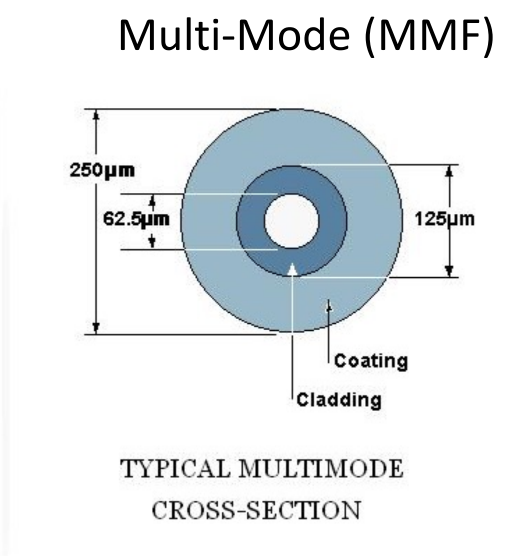


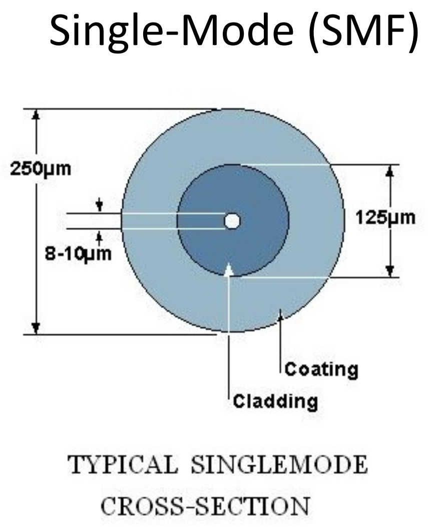
[Finisar]

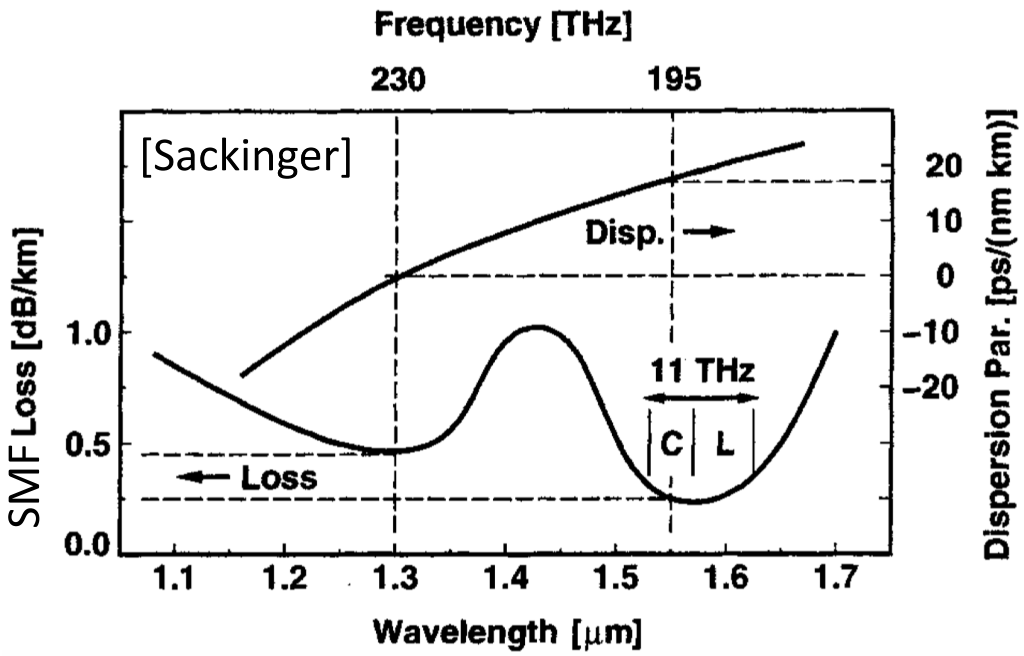
As of 2018:

Long-span Inter-building	40G → 100G → **200G/400G**		
2km/metro	Single-mode Fiber	Optical	
Inter-rack	40G → **100G** → **200G/400G**		
20m-2km 1-20 m	Single-mode Fiber Multi-mode Fiber	Optical	
Intra-rack	10G → 25G → **56G** → **100G/200G**		
0.5-3 m	Copper Channels	Electrical	

Fiber Optics



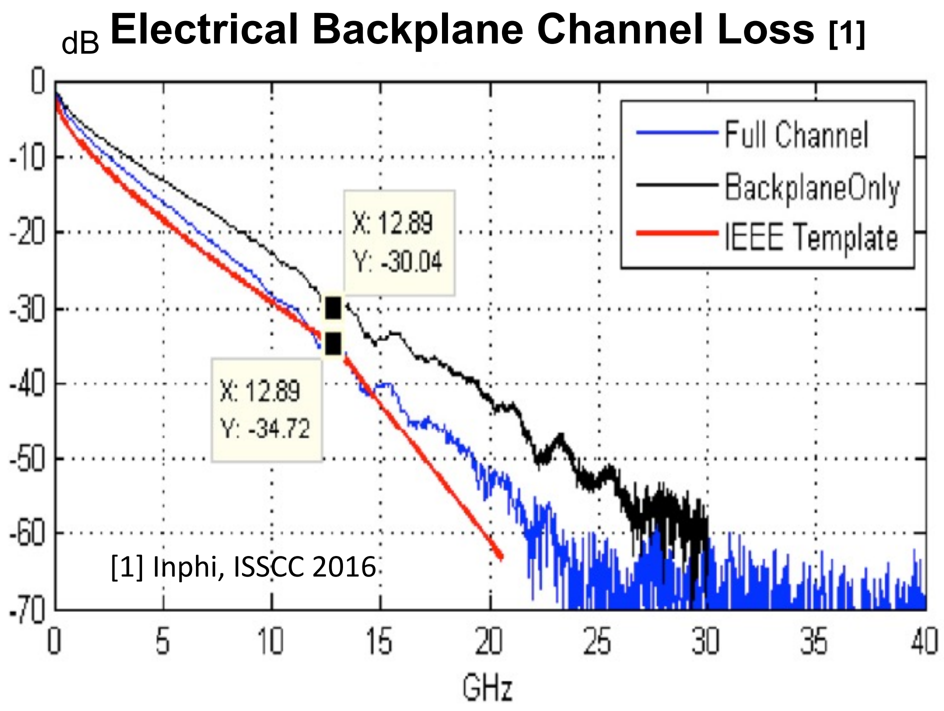


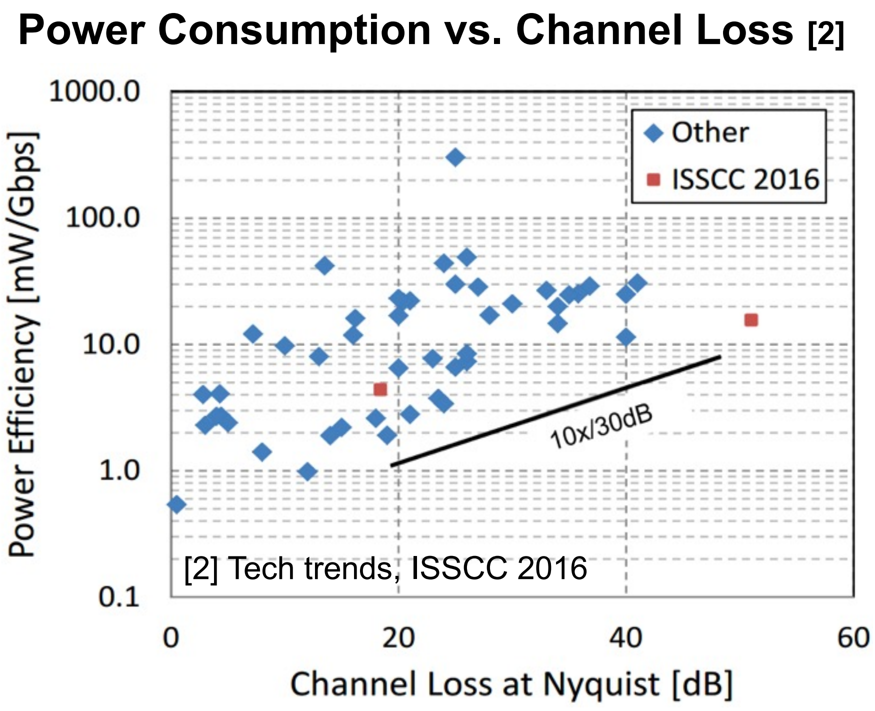


- Multi-mode vs. Single-mode fibers
  - Dispersion, Cost, …
  - MMF for short (< 300m) & SMF for longer distances
- Lowest fiber losses: *1310nm (O-band) & 1550nm (C-band)*: ~0.1db/km!
  - 1550nm for long-range communication (tele-communication)

ELECTRICAL & COMPUTER ENGINEERING

Electrical Links Limitations

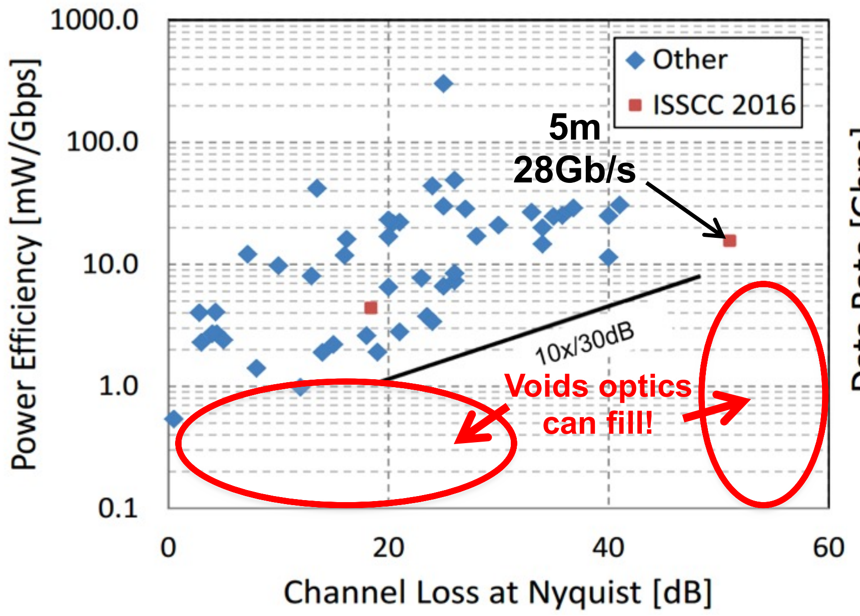




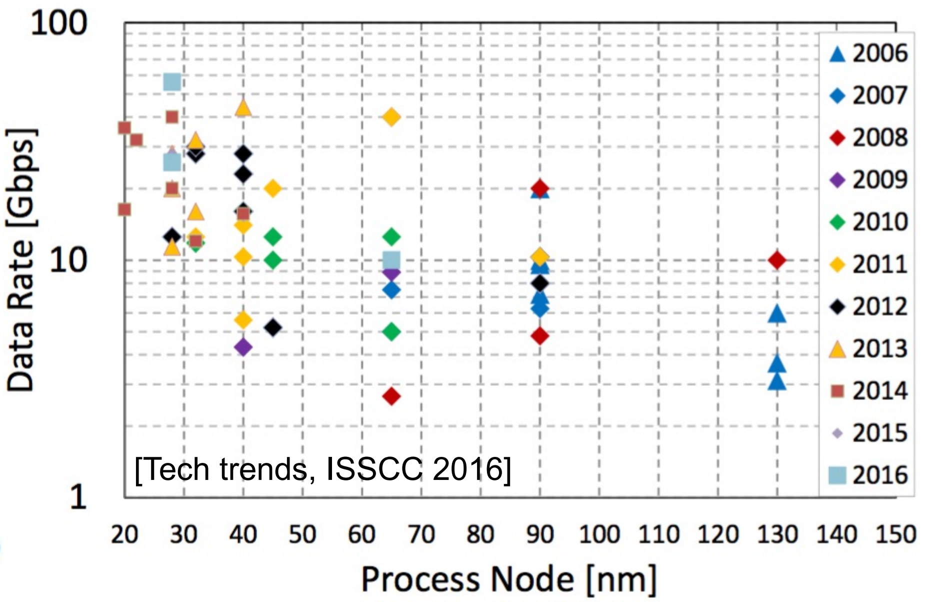
- High data rate → High channel loss → High transceiver power
- **10 pJ/bit** with -40 dB channel loss at Nyquist frequency

Electrical Links Limitations

Power Consumption vs. Channel Loss



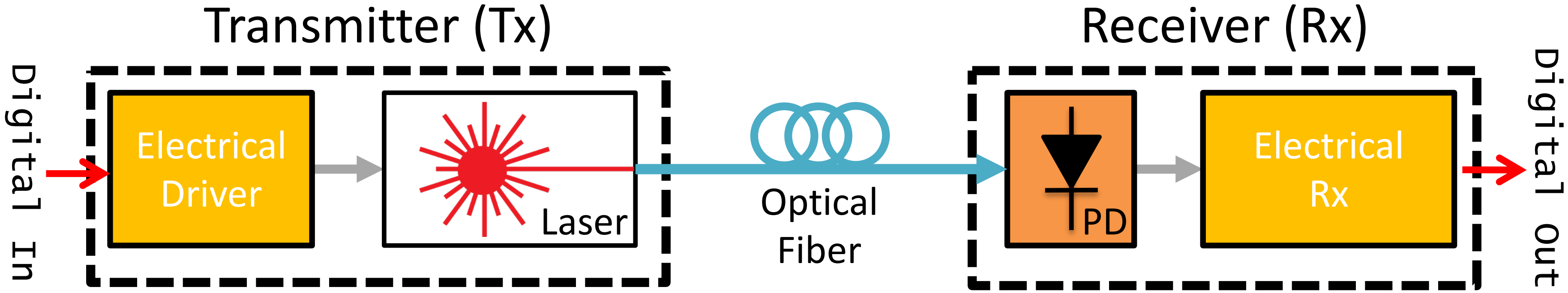
Electrical Link Data-rates Trend



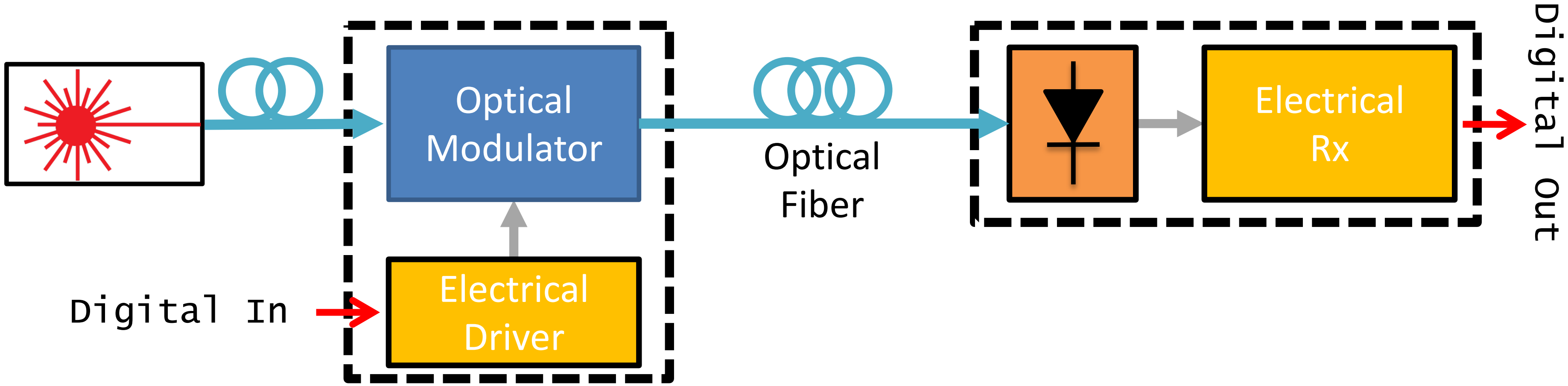
- Higher data rates & Longer channels ➔ Higher channel loss
- Moore's law !? …
- **Optical links can break this barrier!**

An Optical Link

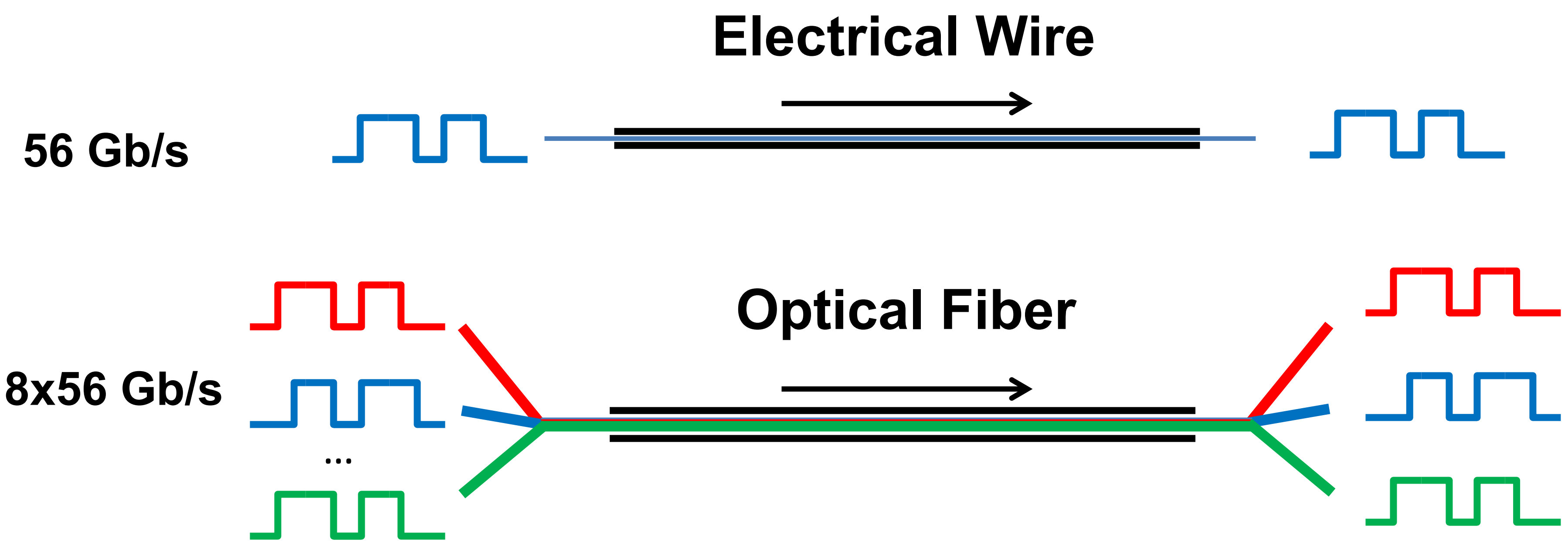
Directly Modulated Laser



Externally Modulated Laser

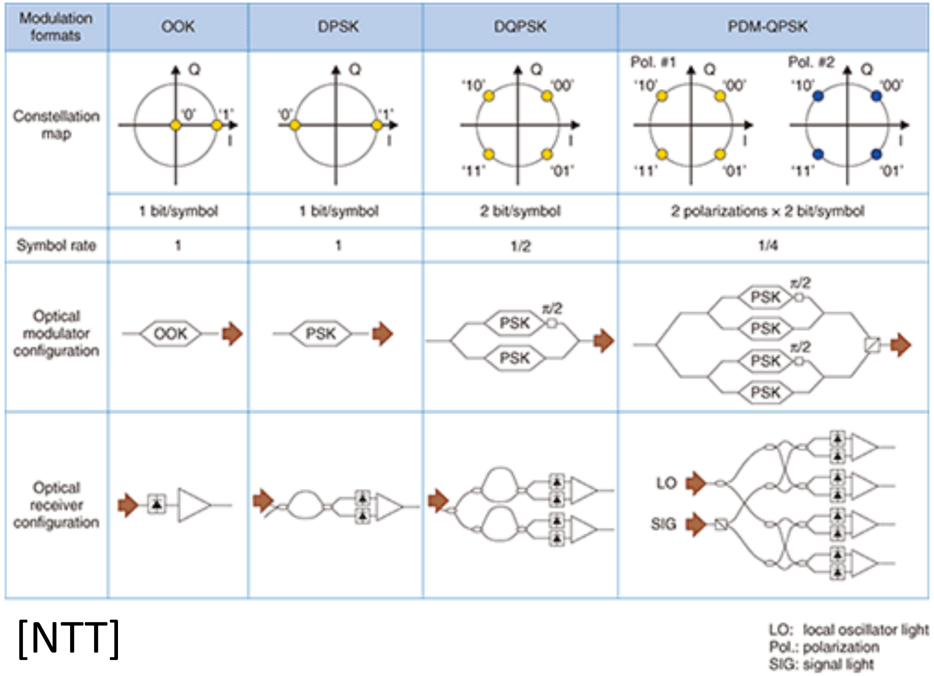


WDM Optical Signaling

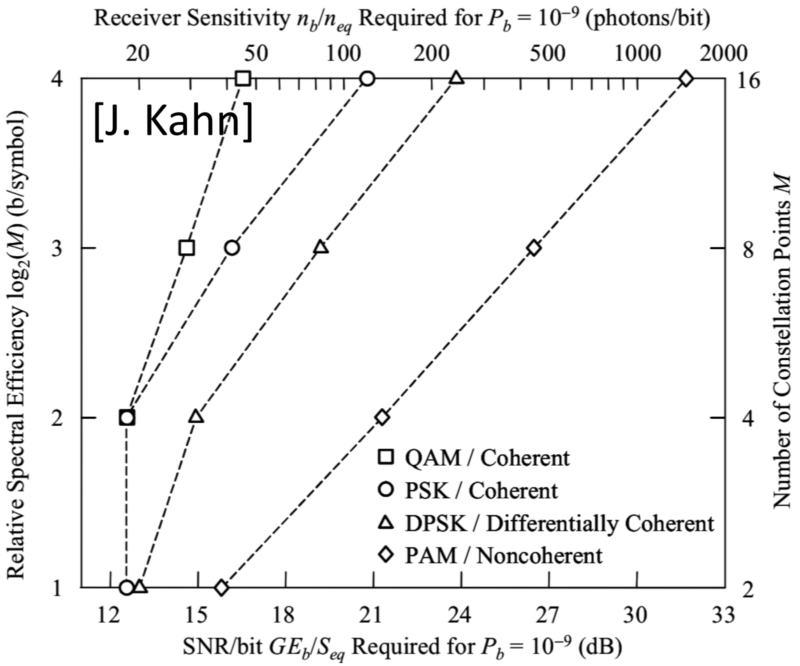


- Wavelength Division Multiplexing (WDM)
  - Boosting aggregate bandwidth per fiber
  - Coarse vs. dense WDM
- Polarization Multiplexing also a solution
- **Why cannot we do this in electrical links?!**

Modulation Formats

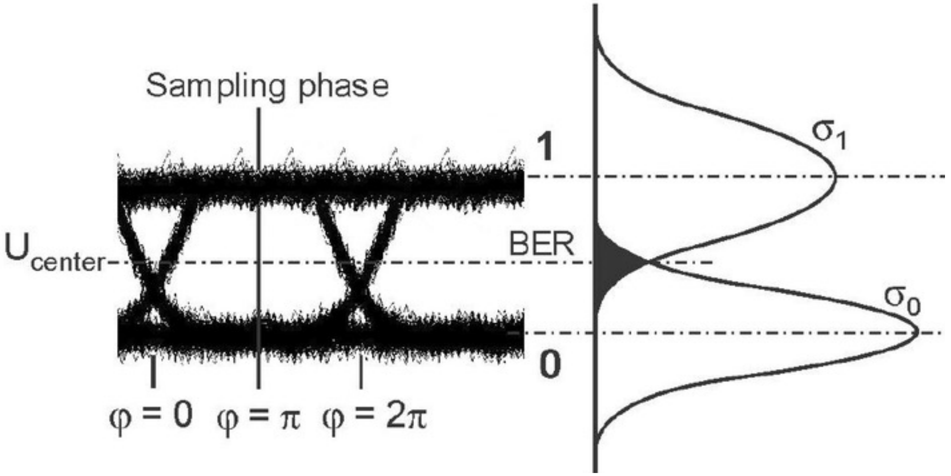


[NTT]

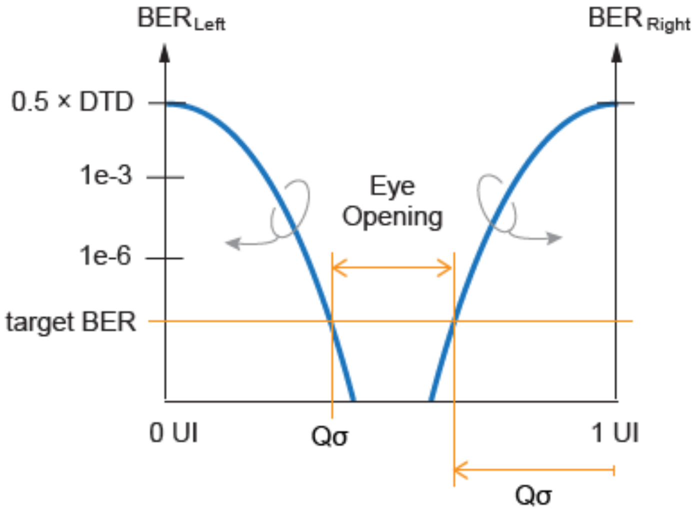


- Higher Order Mod -> Higher Spectral efficiency, but worse SNR
- Direct vs. coherent detection
- Forward error correction (FEC)
- Coherent modulations is used in long-haul, and most of other optical links use pulse amplitude modulation (PAM)

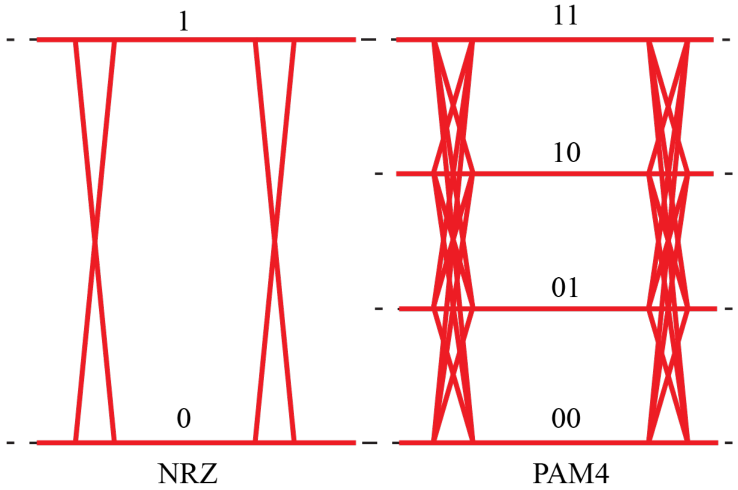
Eye-diagram & BER



Tx eye-diagram (NRZ Modulation)



Rx Bathtub curve for BER

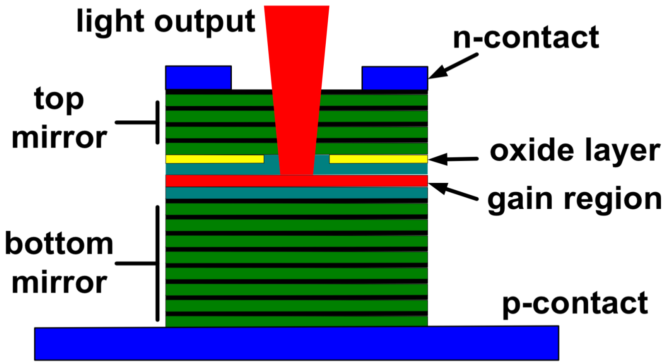


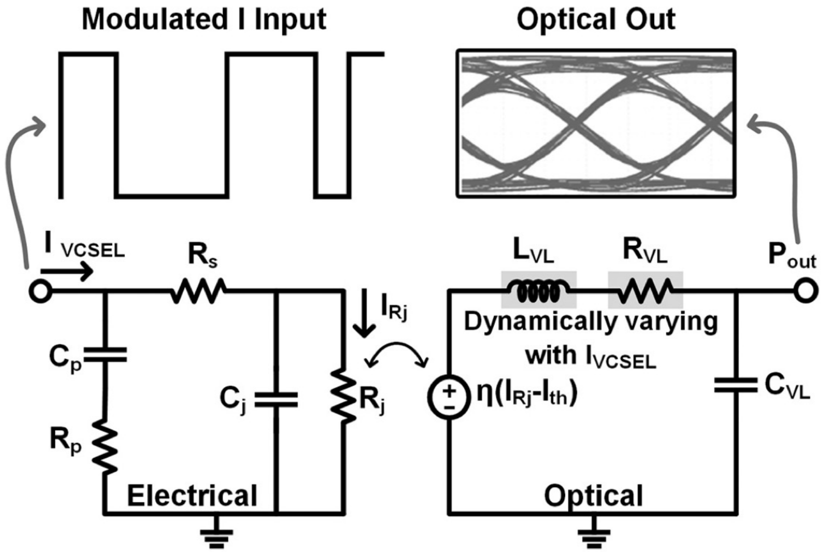
- Performance Measures of Tx & Rx
- Tx eye-diagram metrics
  - Extinction Ratio (ER), Insertion loss (IL), Optical Modulation Amplitude (OMA_{TX}), …
- Rx Bathtub curve metrics
  - Bit error rate (BER), H-eye opening, …

Directly Modulated Laser

- Requires high relaxation frequency for laser
  - Challenging packaging & integration
  - In research shown up to 50Gb/s
- Most successful case is VCSELs for short-reach links (< 100m)
  - Normally multi-mode & NIR (850nm-950nm)
  - Vertical Cavity Surface Emitting Laser (VCSEL)
- ***Not practical for high data-rates (?)***

VCSEL Cross-Section



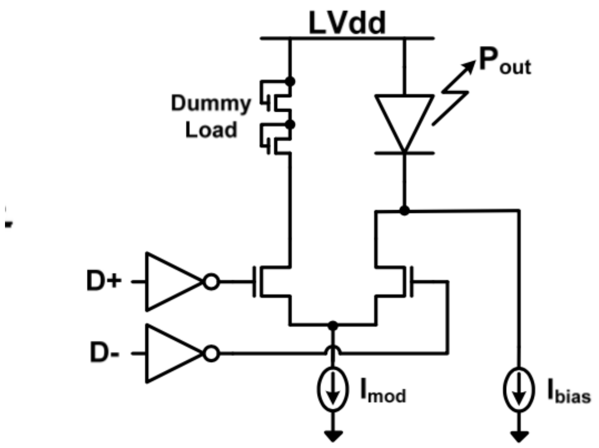


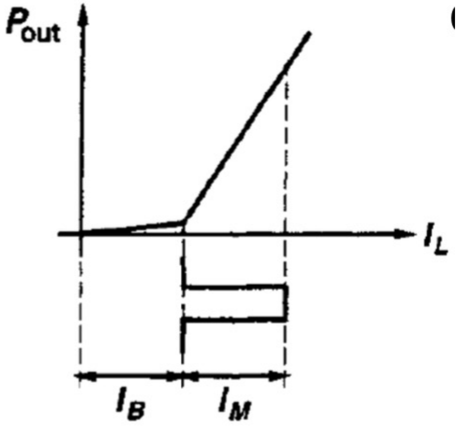
[Raj, JSSC 2016]

VCSEL based Transmitter

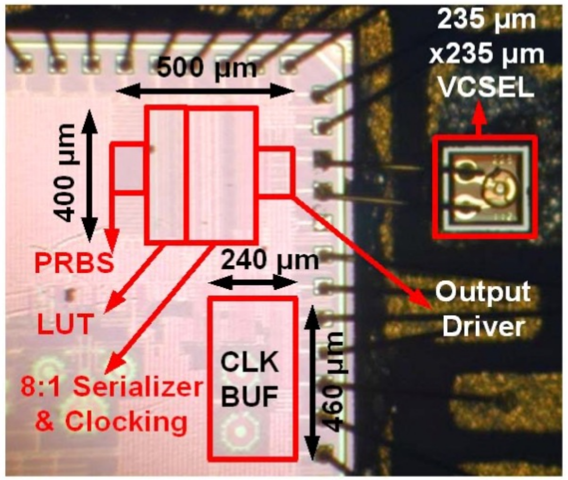
50Gb/s PAM4 Experimental Results

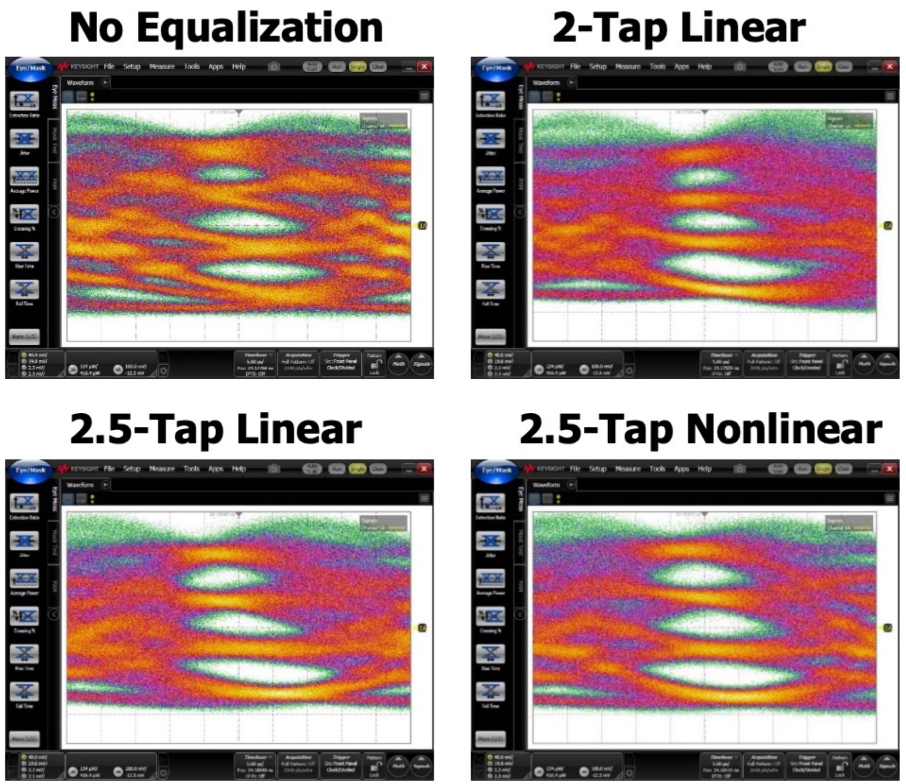
Current-Mode VCSEL Driver





[Tyagi PTL 2018]

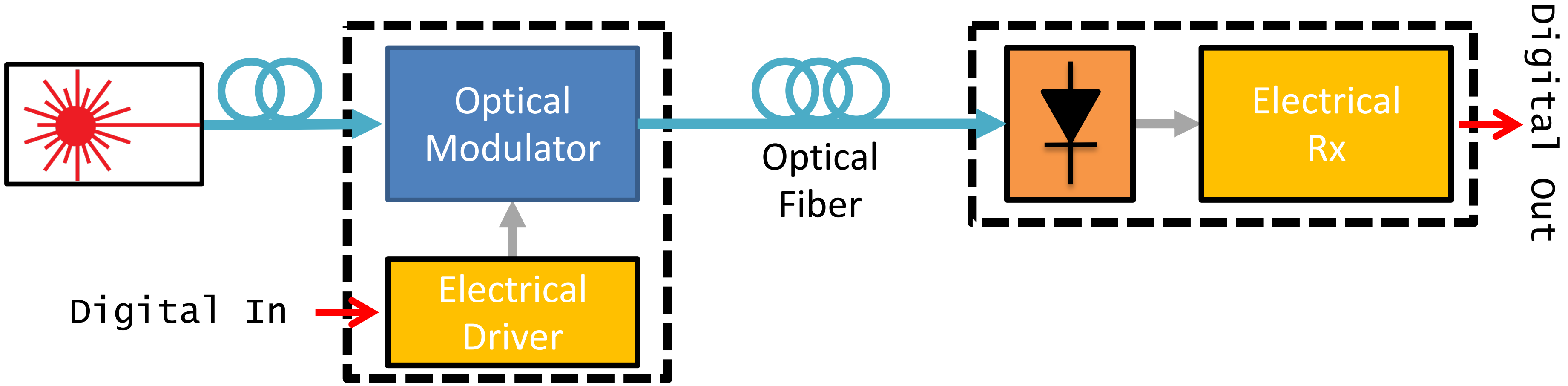




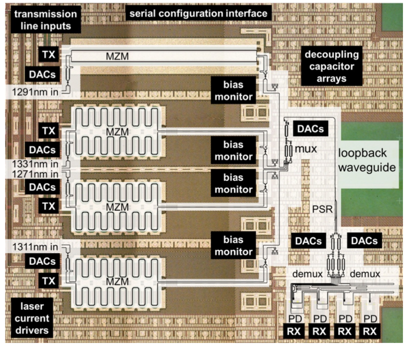
- Core transmitter area is 0.2mm^2
- 2.5 tap nonlinear equalizer improves eye height and timing alignment of the 3 PAM4 eyes

[Sam Palermo] 33

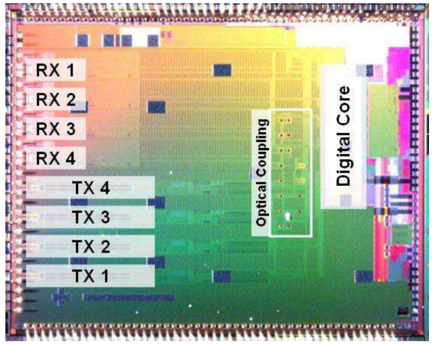
Externally Modulated Laser



Monolithic

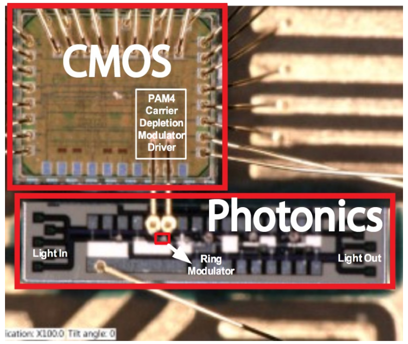


[IBM, OFC 16]

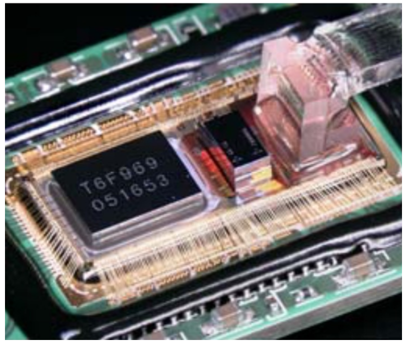


[Luxtera, Hot Chips 09]

Hybrid / 3D



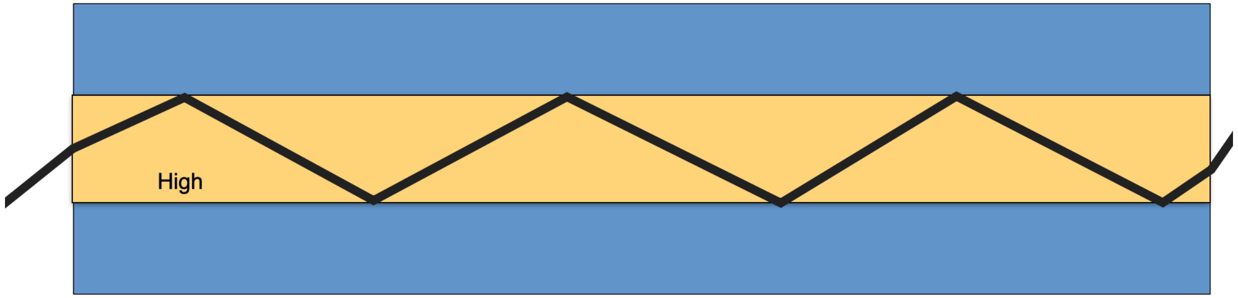
[Roshan-Zamir, OI 16]

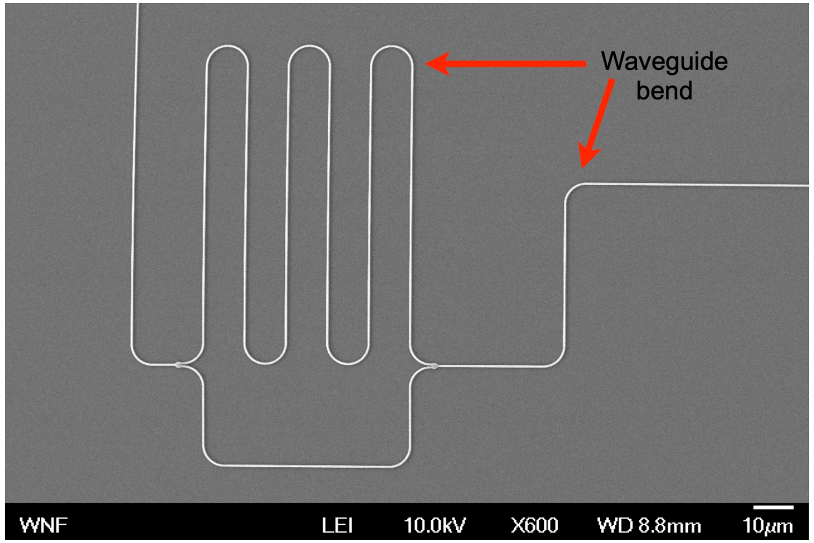


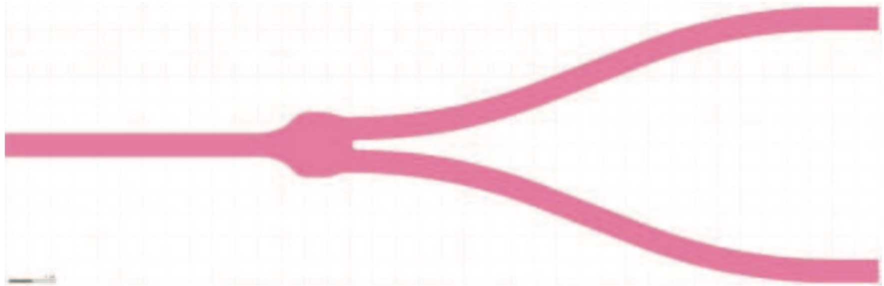
[Luxtera, IEDM 17]

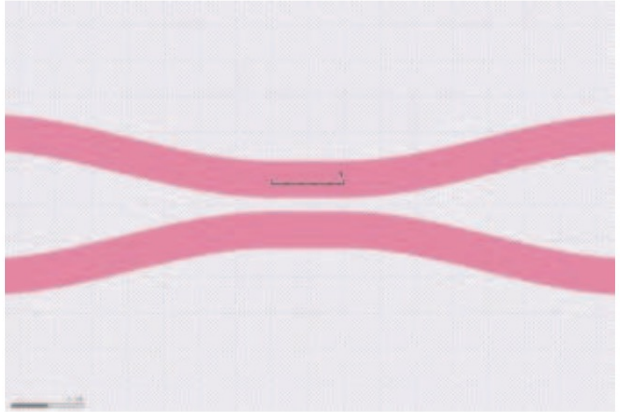
Waveguides

- Light is guided by Total Internal Reflection (TIR)
  - Requires the core of the waveguide to have a higher index of refraction (Si) as compared to the cladding (SiO_2)









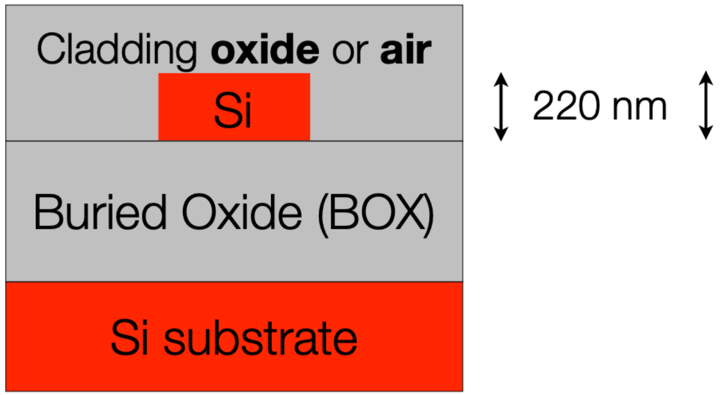
(a) Directional coupler

Waveguides in integrated photonics

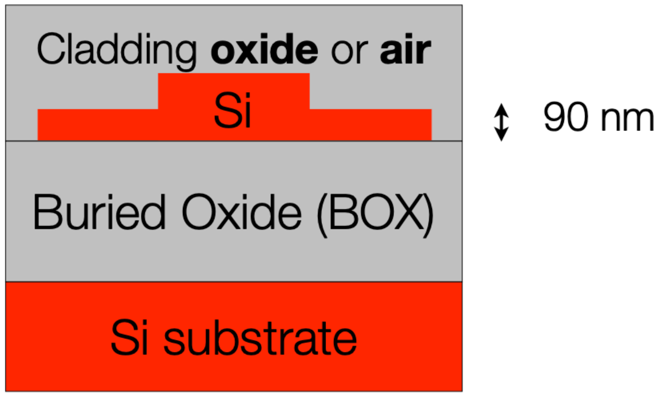
- Effective refractive index
- Mode (TE/TM)
- $TE_{00,01,\dots}$
- Loss:
  - absorption
  - Surface roughness
  - Bending loss
- "2nd" order effects:
  - Dispersion
  - Non-linearities
  - TPA, FCA, …

Waveguides – Two basic types:

- **Strip, or:**
  - Photonic Wire
  - Channel
  - Ridge (confusing)
- 2-3 dB/cm
- Used for routing, tight bends

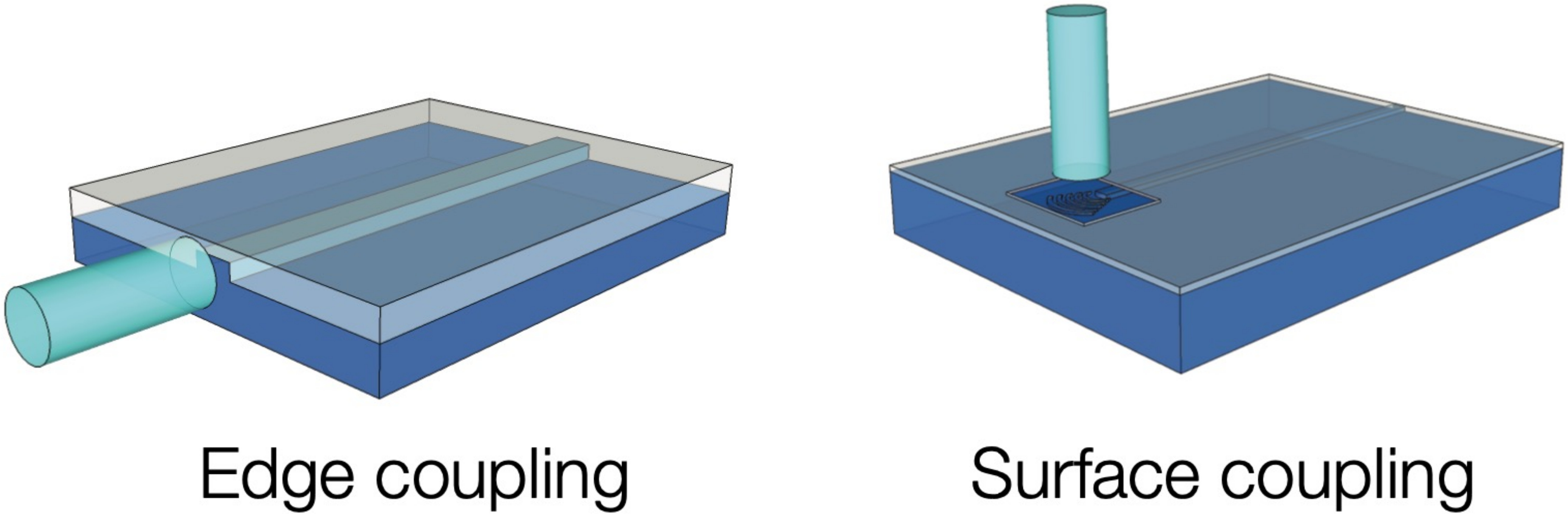


- **Rib, or:**
  - Ridge
  - Strip-Loaded Ridge
- 2-3 dB/cm
- Used for devices requiring electrical contacts (e.g., pn junctions)



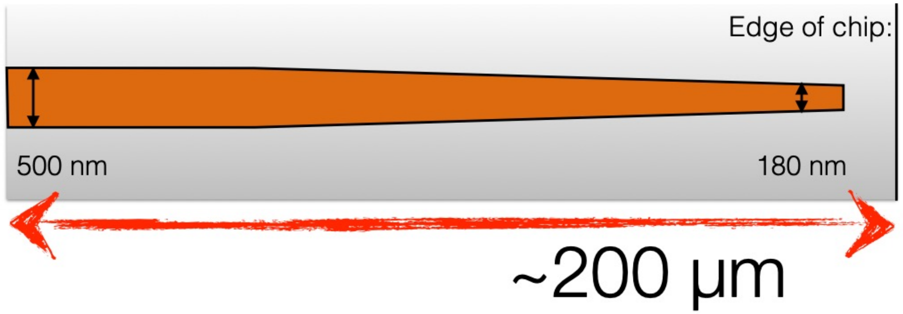
Fiber Couplers

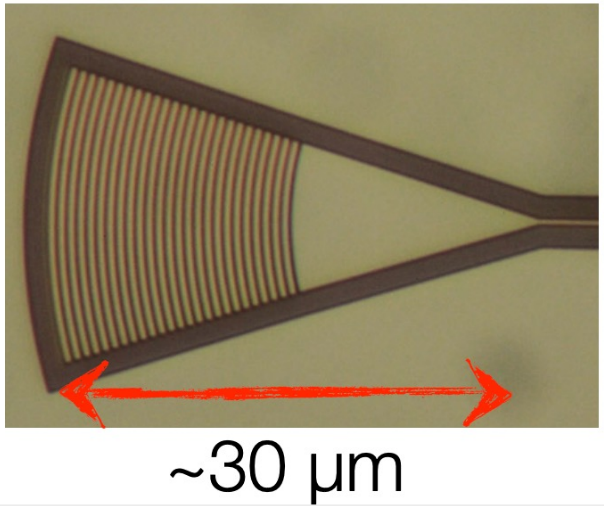
- **How to interface fiber with waveguides?**



Fiber Couplers

	Edge Coupling	Surface Grating Coupling
Pros	• Wide optical bandwidth • Support for both TE/TM polarization • Similar to existing laser & modulator edge packaging techniques • High-efficiency	• Easy alignment • Cost-effective – no post process • Location flexibility in the designs; compact • Chip/wafer scale automated measurement; • High-efficiency
Cons	• Challenging alignment (smaller mode size) • More complicated fabrication (e.g., edge facet polishing, tapers for mode expansion, access to edge of chip)	• Limited optical bandwidth • Challenge in obtaining good coupling efficiency (typically 3 dB or more) • Normal-incidence challenging for packaging





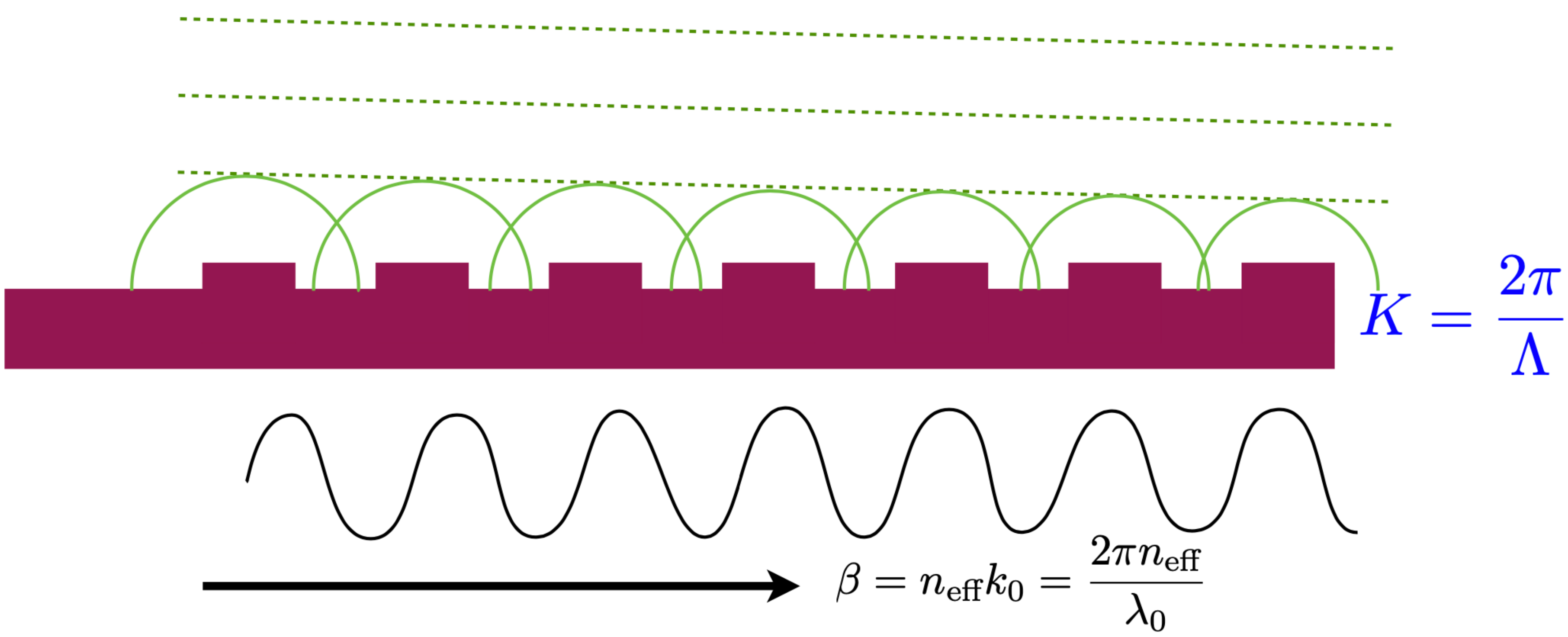
Grating Couplers

- Equation:

$$n_{\text{eff}} - \sin\theta_{\text{air}} = \frac{\lambda}{\Lambda}$$

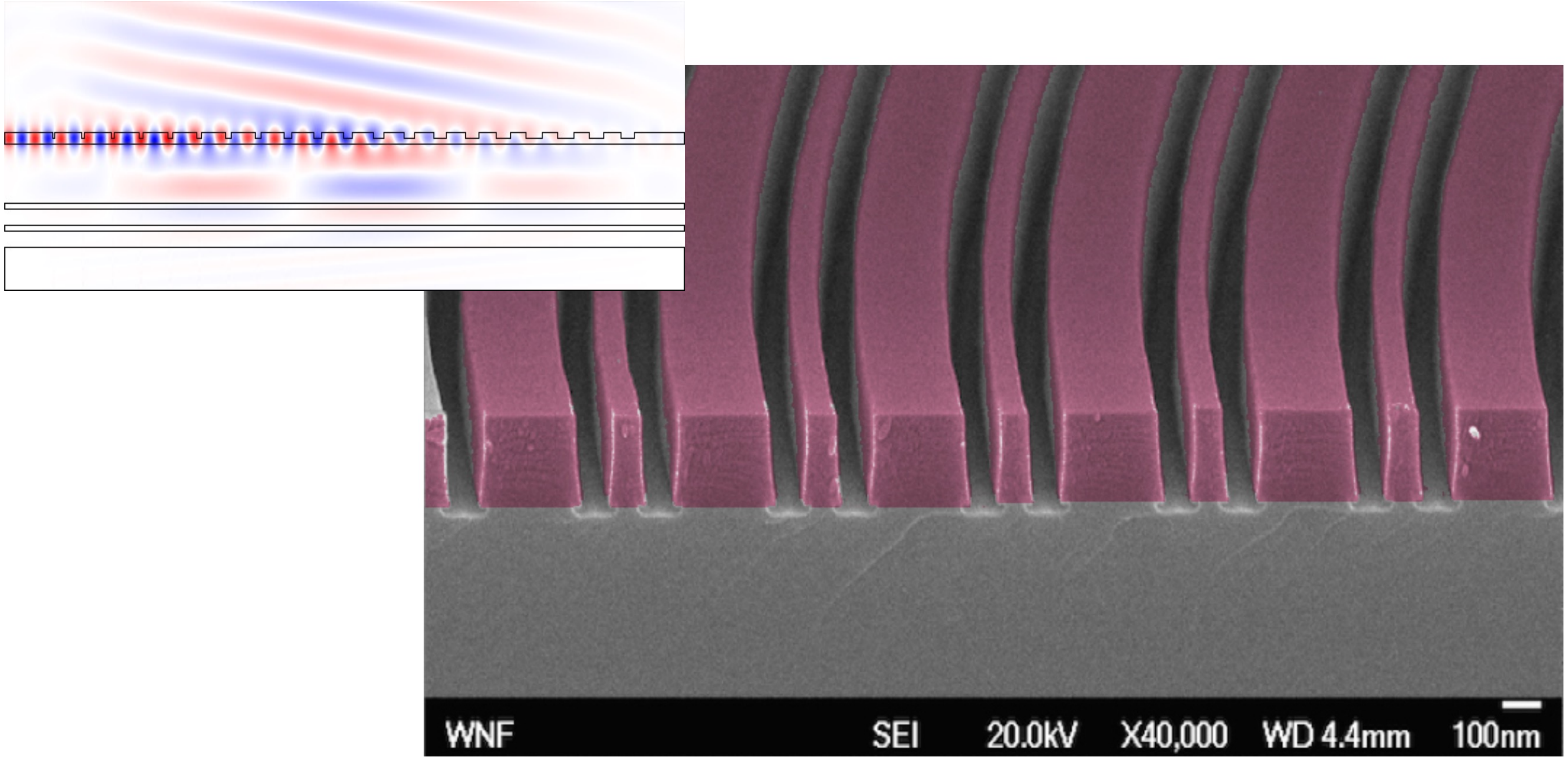
- Example design for O-band:
  - Period: 500nm
  - Angle: ~15deg
  - Loss: 2db
- **Wavelength & Polarization dependent**

- Case 2 – Optical wavelength is smaller than the grating period, $\frac{\lambda_0}{n_{\text{eff}}} < \Lambda$



- Vertical output at an angle, no 2nd order back-reflection

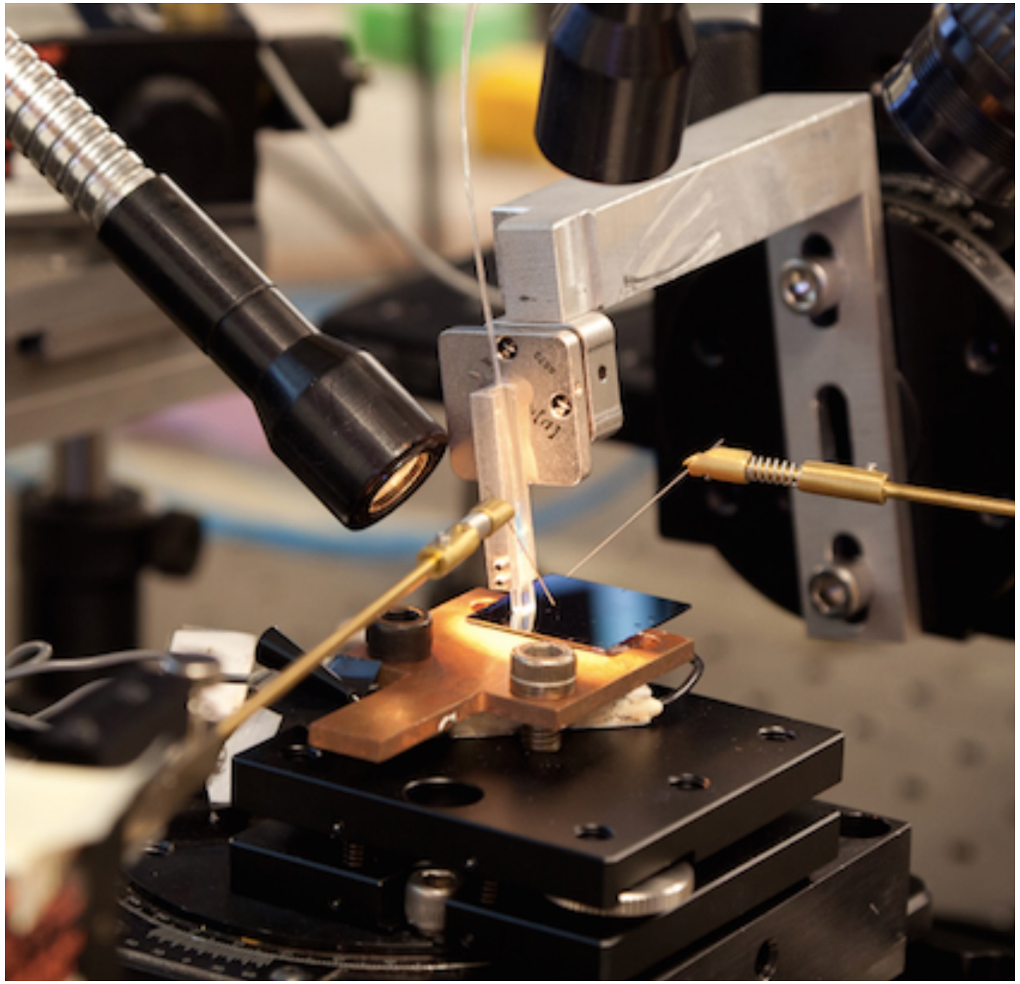
Grating Couplers (GC)

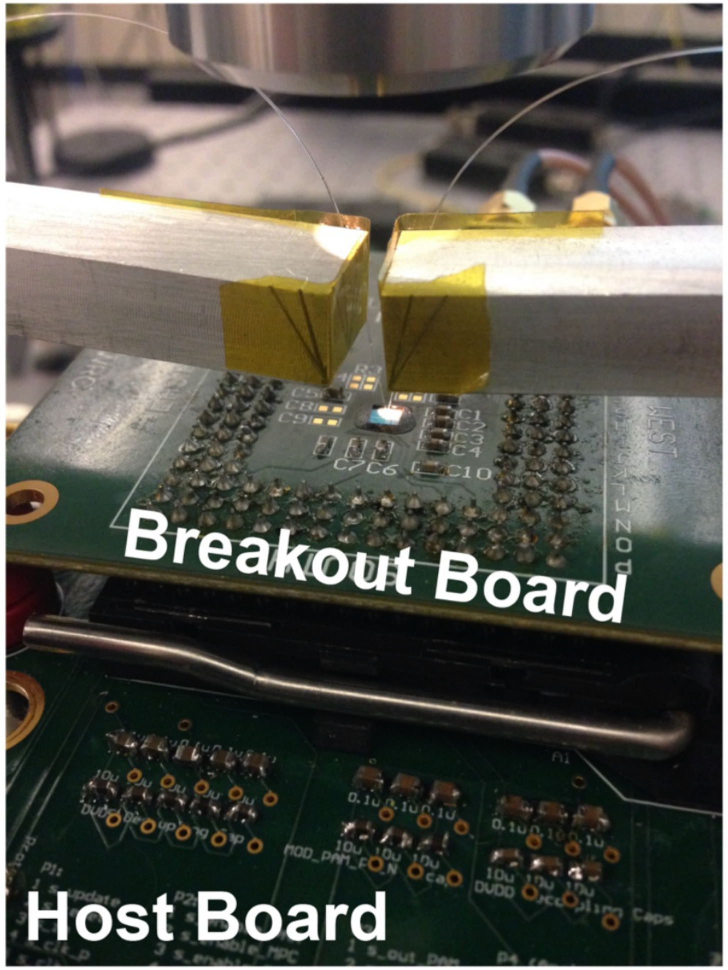


Watch these:

https://www.youtube.com/watch?v=6aDU_tfZ668
https://www.youtube.com/watch?v=KI6Vq9cF21M

Example Optical Test Setup





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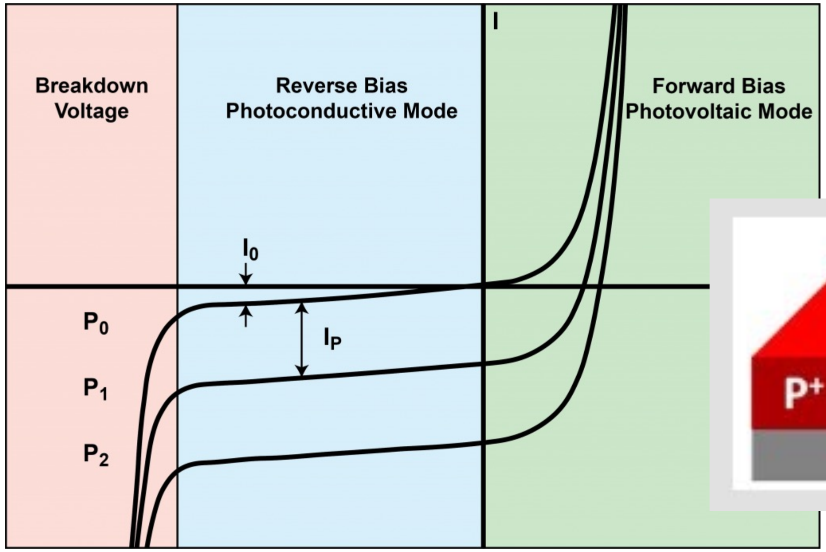
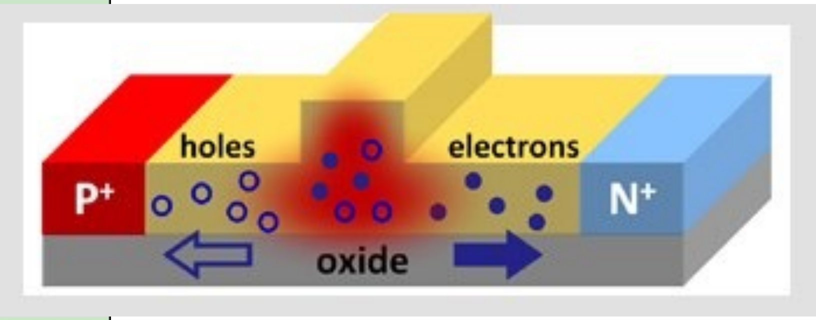
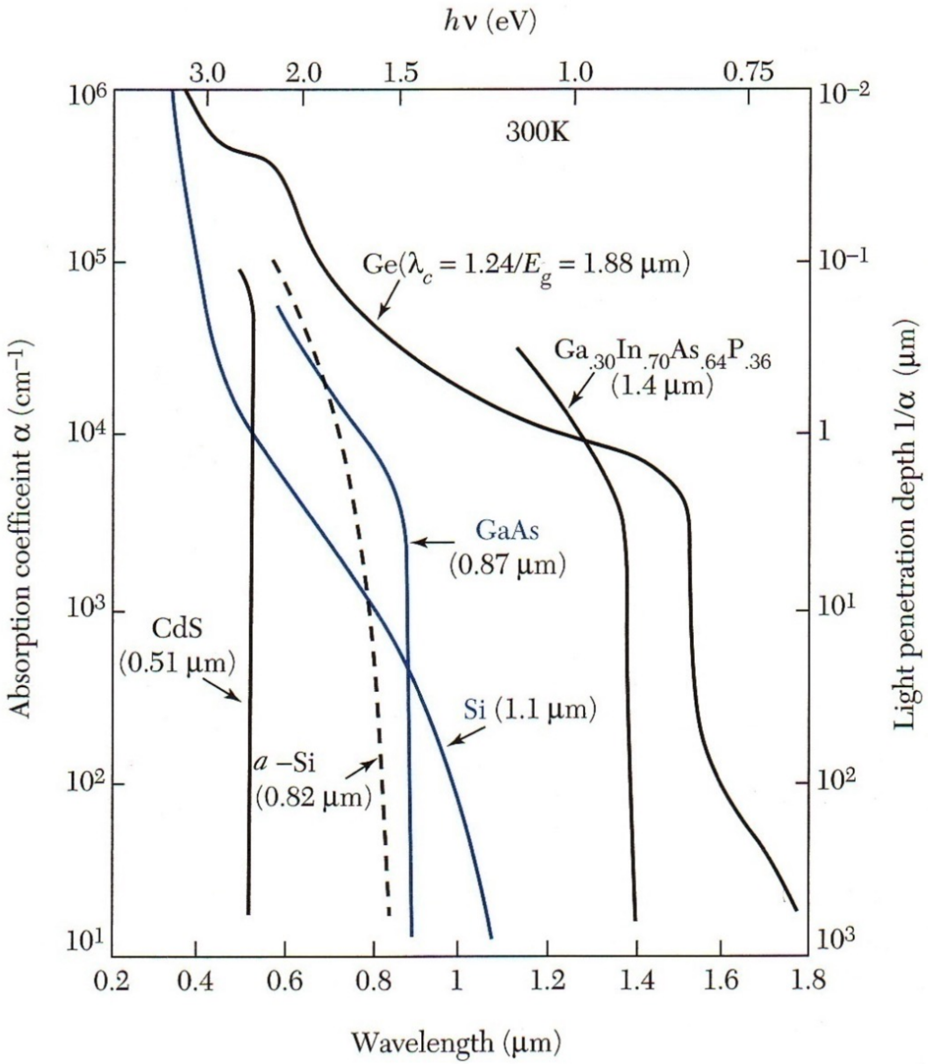
Photodiodes (PD)





[B. Jalali, UCLA]



- PIN & Avalanche Photodiodes
- Optical interconnects mostly use PIN PDs
- Ge for IR light detection
- Metrics: Responsivity (A/W), bandwidth, dark current, …

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Photodiodes (PD)

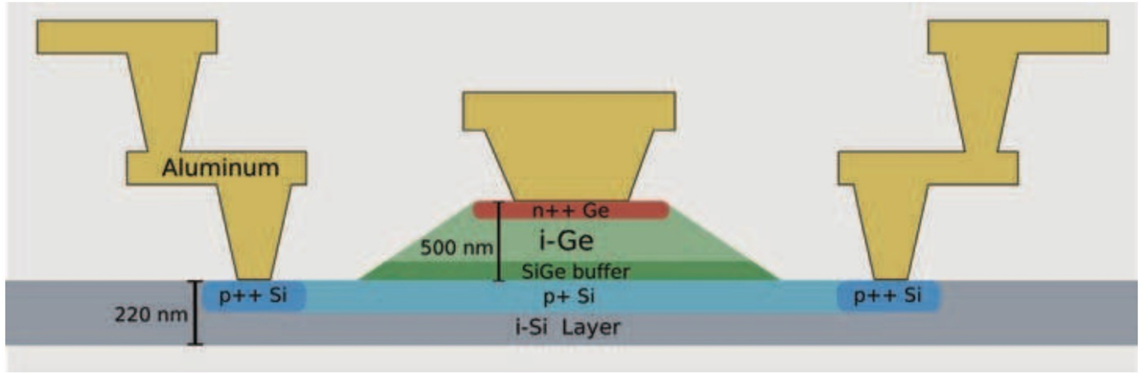
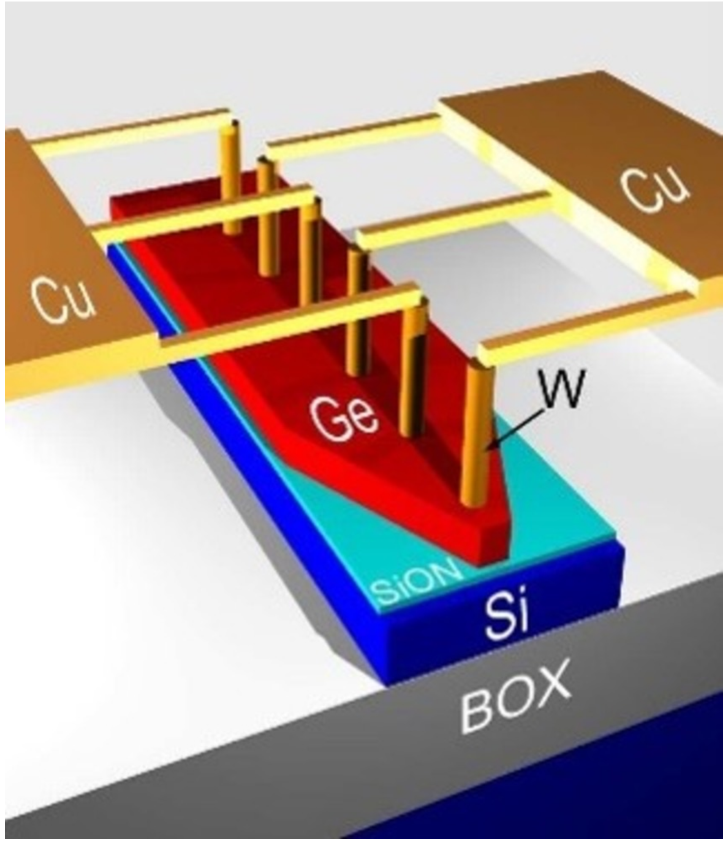
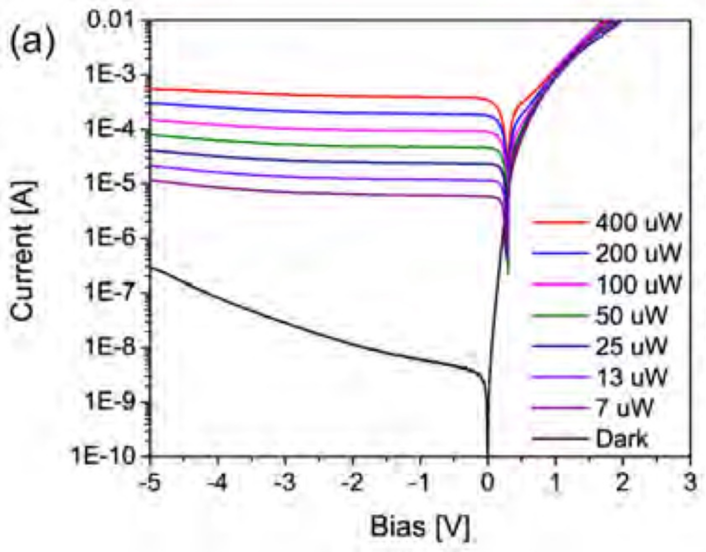


Figure 7.8 Cross-section of vertical PIN germanium-on-silicon detector.



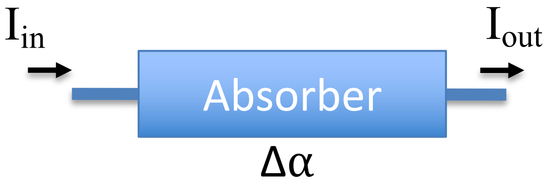
Ge integration …

- Crystalline material require epitaxy for integration
- Lattice mismatch
- High-temperature
  - >500C
- Can be monolithically integrated in CMOS (Next lecture)

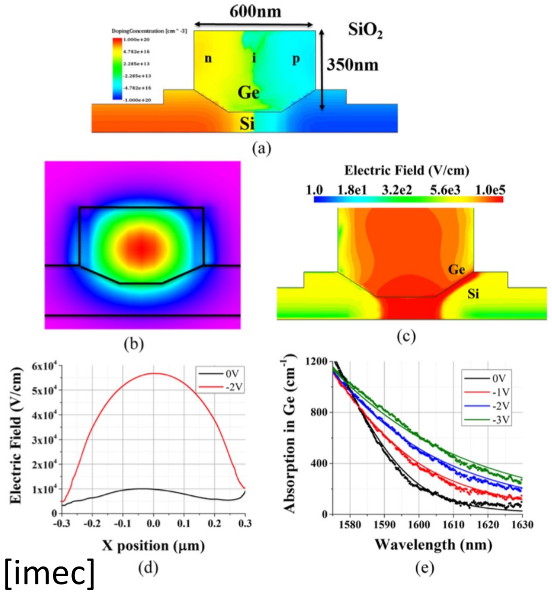


Optical Modulators

Electro-absorption based

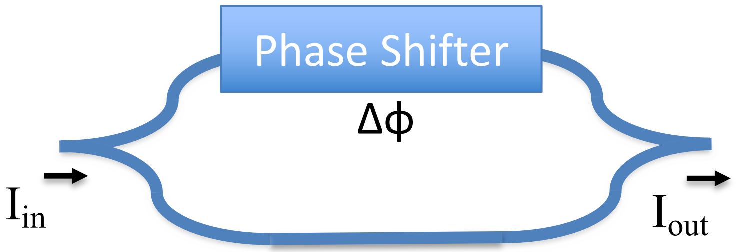


$$I_{out} = I_{in} \times e^{-\Delta\alpha . L}$$

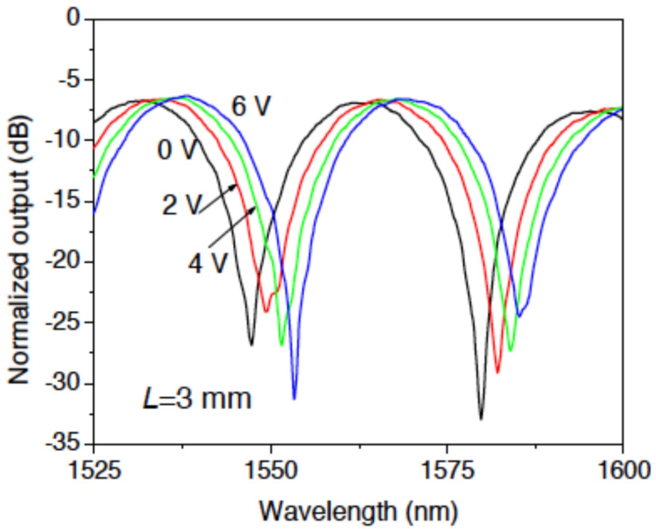


[imec]

Mach-Zehnder Modulator

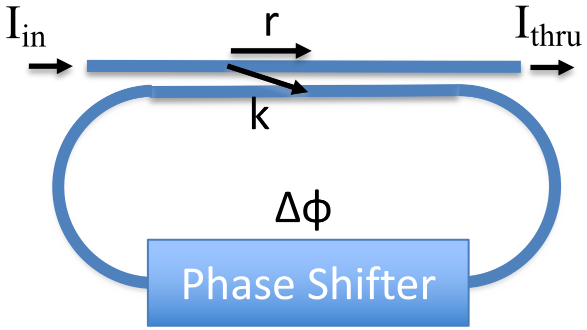


$$I_{out} = \mathrm{I}_{in} \times \cos^2 (\Delta\phi/2)$$



[A. Liu]

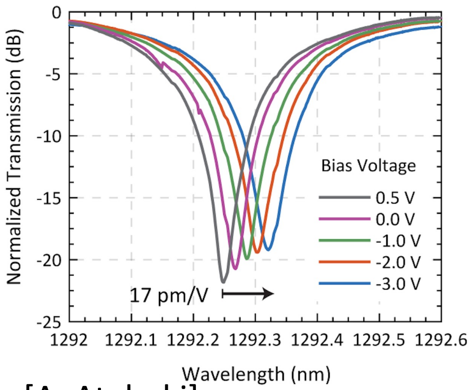
Resonant Modulator



$$\alpha = \frac{I_{thru}}{I_{input}} = \frac{a^2 - 2ar\cos(\phi) + r^2}{1 - 2ar\cos(\phi) + a^2r^2}$$

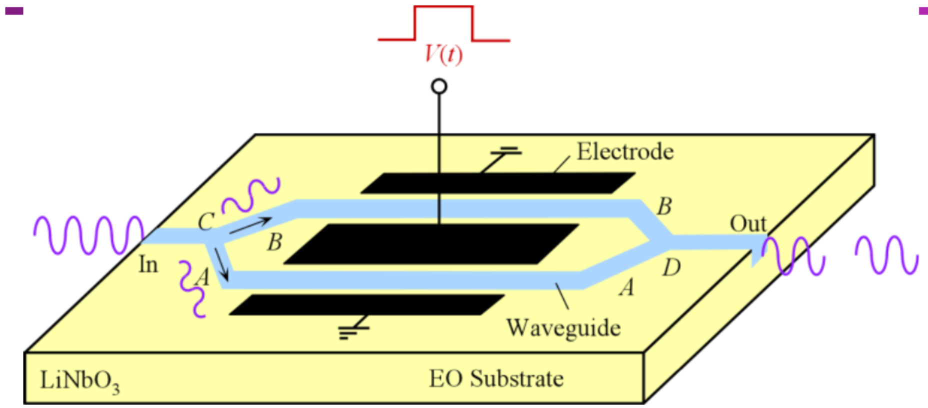
a = round trip loss

ϕ = round trip phase shift



[A. Atabaki]

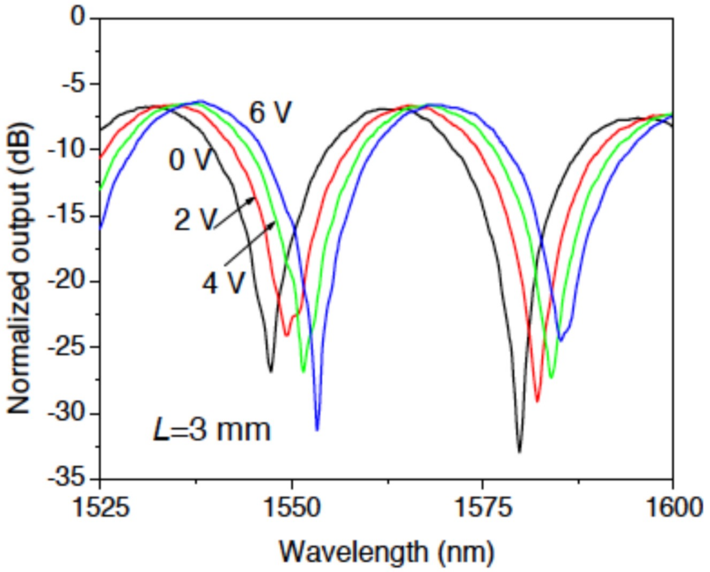
Mach-Zehnder Modulator (MZM)



Approximate analysis

Input C breaks into A and B

A and B experience opposite phase changes arising from the Pockels effect



A and B interfere at D. Assume they have the same amplitude A
But, they have opposite phases

$$E_{out} \propto A\cos(\omega t + \phi) + A\cos(\omega t - \phi) = \underbrace{2A\cos\phi}_{\text{Amplitude}} \cos(\omega t)$$

Output power $P_{out} \propto E_{out}^2$

$$\boxed{\frac{P_{out}(\phi)}{P_{out}(0)} = \cos^2 \phi}$$

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Mach-Zehnder Modulator (MZM)

- Performance Metric: Vpi.L (V.cm)

Table 1. , Performance comparison of previously reported high-speed silicon MZMs (>25 Gb/s) and devices in this work.

Reference	[17]	[15]	[25]	[27]	[24]	[26][&]	L = 2 mm	L = 4 mm	L = 6 mm
Device length (mm)[%]	1	0.12	1.35	1	3.5	2.4	2	4	6
$V_{\pi} \cdot L$ (V·cm)	4	0.5	11	2.8	2.7	2.4	2.4	2.08	1.86
V_{π} (V) *	NA	NA	NA	NA	~8	10	12	5.2	3.1
Insertion loss (dB)[#]	4	2.5	15	3.7	15	4.3	4.1	6.6	9.0
Speed (Gb/s)	40	25	40	50	40	30	~50	~40	30

MZM Drivers

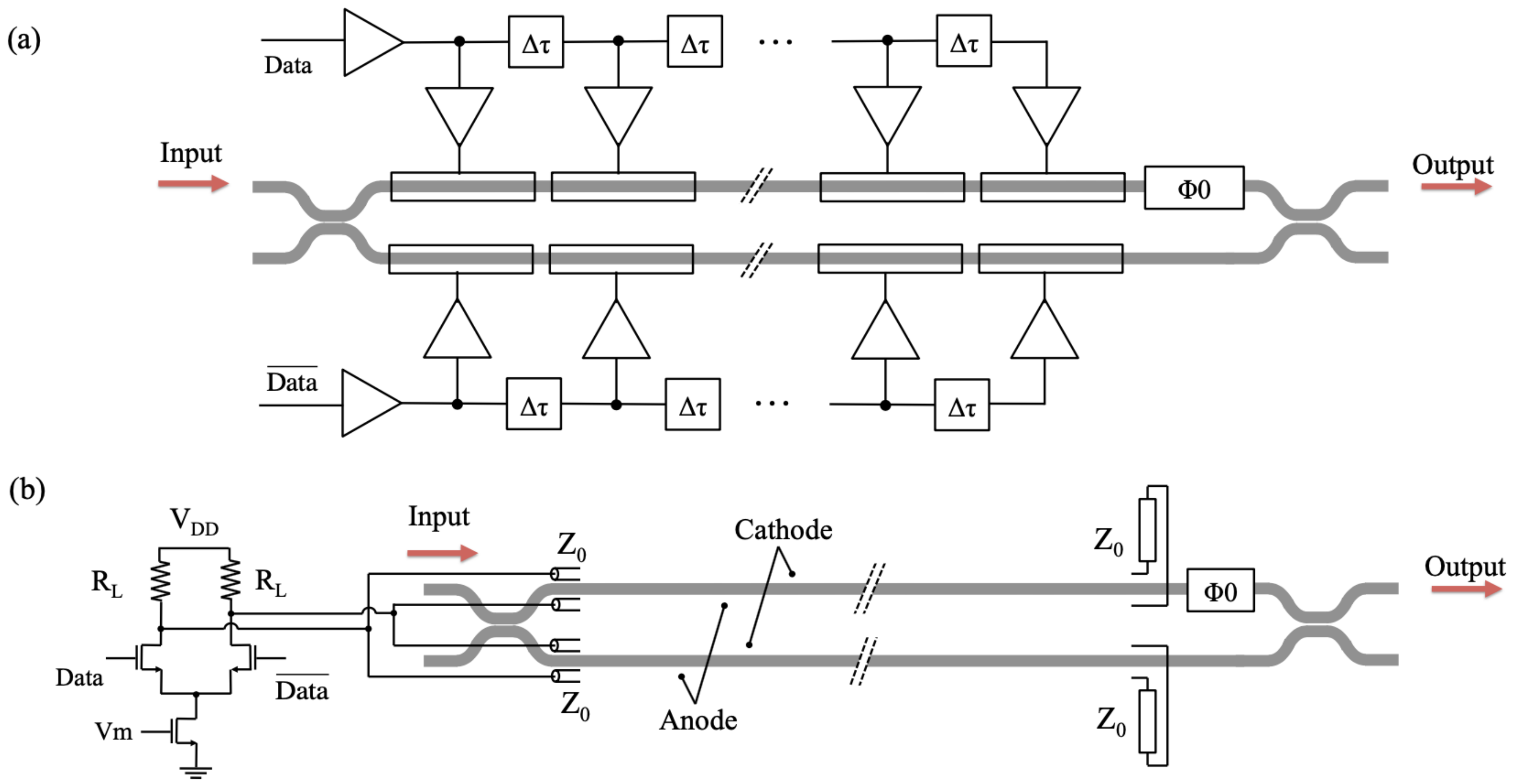
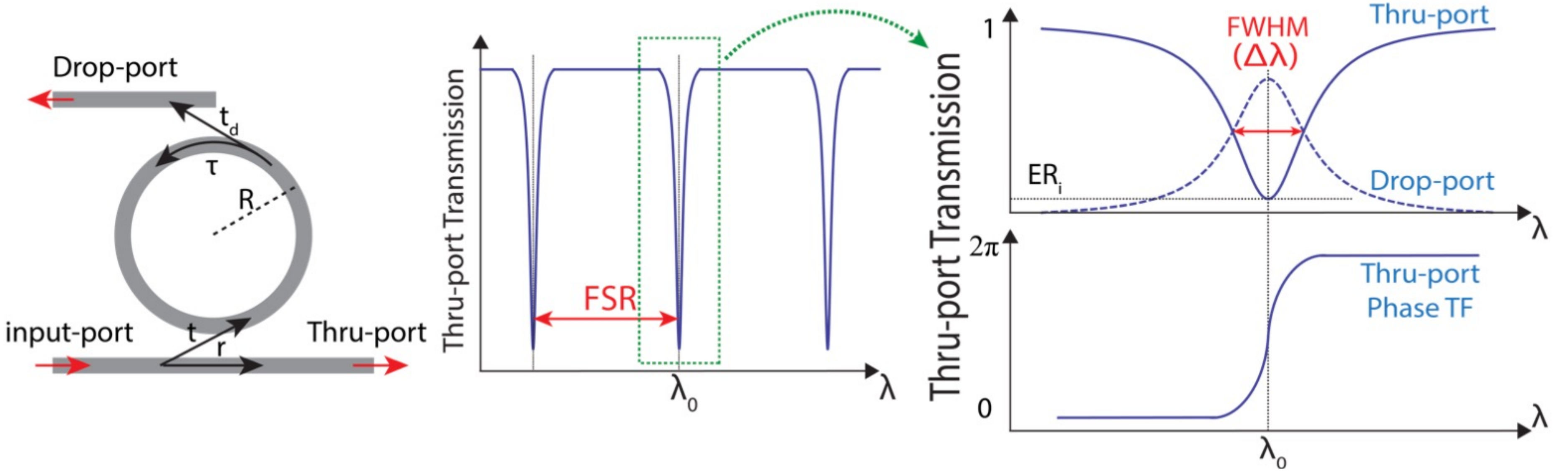
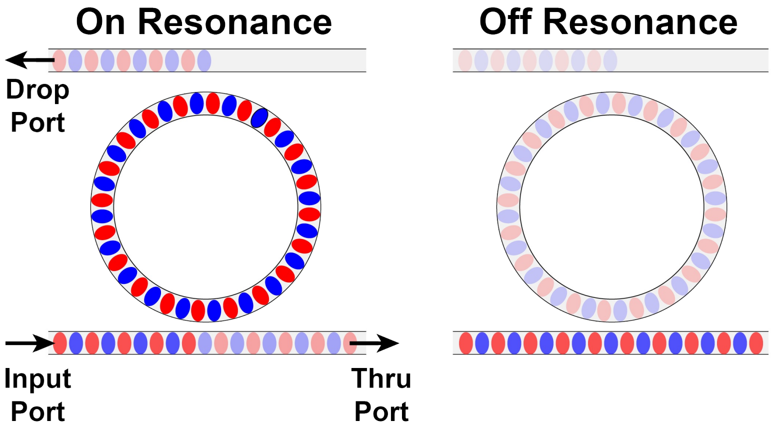


Fig. 19. (a) Architecture of Multi-stage Mach-Zehnder Modulator (MS-MZM) (b) Architecture of Traveling wave Mach-Zehnder Modulator (TW-MZM)

Micro-ring Modulator (MRM)

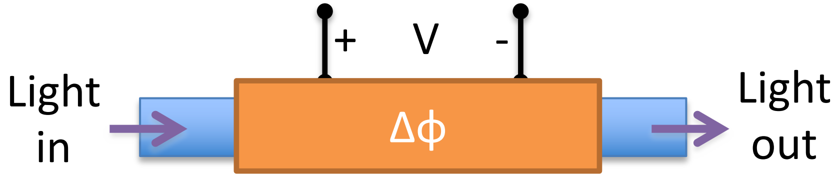


- Resonance wavelength: $\lambda_0 = n_{eff} L/m$, m = 1,2,3,...
  - Q-factor: $Q = \lambda_0 / \Delta\lambda$
- Compact device (radius of 5μm)
  - Energy & area efficient modulator/filter
- Supports wavelength division multiplexing (WDM)
- Watch this: https://www.youtube.com/watch?v=m4j2y53f1sQ



Physical Mechanisms for Optical Modulators

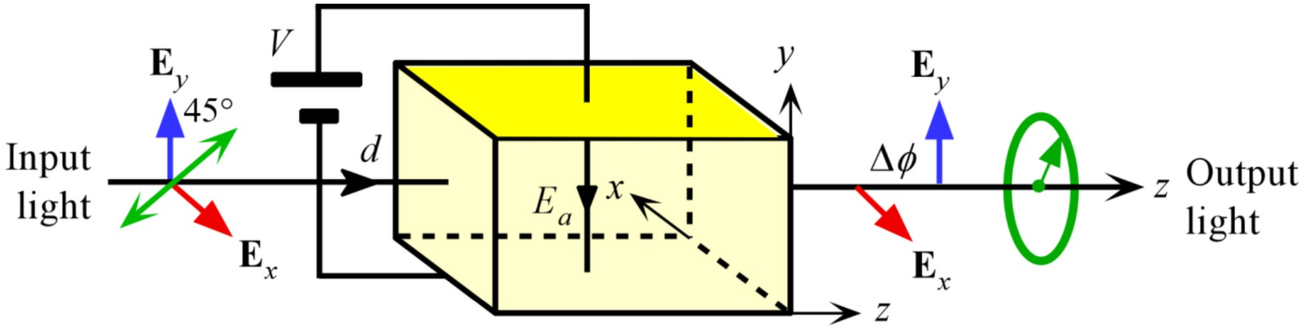
- Electro-optic modulators
  - Nonlinear crystals
  - $LiNbO_3$, GaAs, InP
- Franz-Keldysh effect
  - Sub-bandgap absorption induced by electric field
  - GaAs, InP
- Quantum confined Stark Effect (QCSE)
  - Absorption modulators in quantum wells
  - Mostly III-V, but also SiGe QWs
- Free carriers effect
  - Refractive index change due to electrons/holes
  - All semiconductors, including Si
- Thermo-optic effect
  - Refractive index change due to temperature
  - All semiconductors, including Si



$$\Delta\phi = \frac{2\pi}{\lambda}\Delta n_{\text{eff}} L$$

Pockels Effect

- LiNbO3, BaTiO3, GaAs, …
- Non-linear Organic Polymers
- Si is central symmetric and has no electro-optic effect



Field induced refractive index

New refractive index

$$n' = n + a_1E + a_2E^2 + \dots$$

Linear electro-optic effect
The Pockels effect

$$\Delta n = a_1E$$

Second order electro-optic effect
The Kerr effect

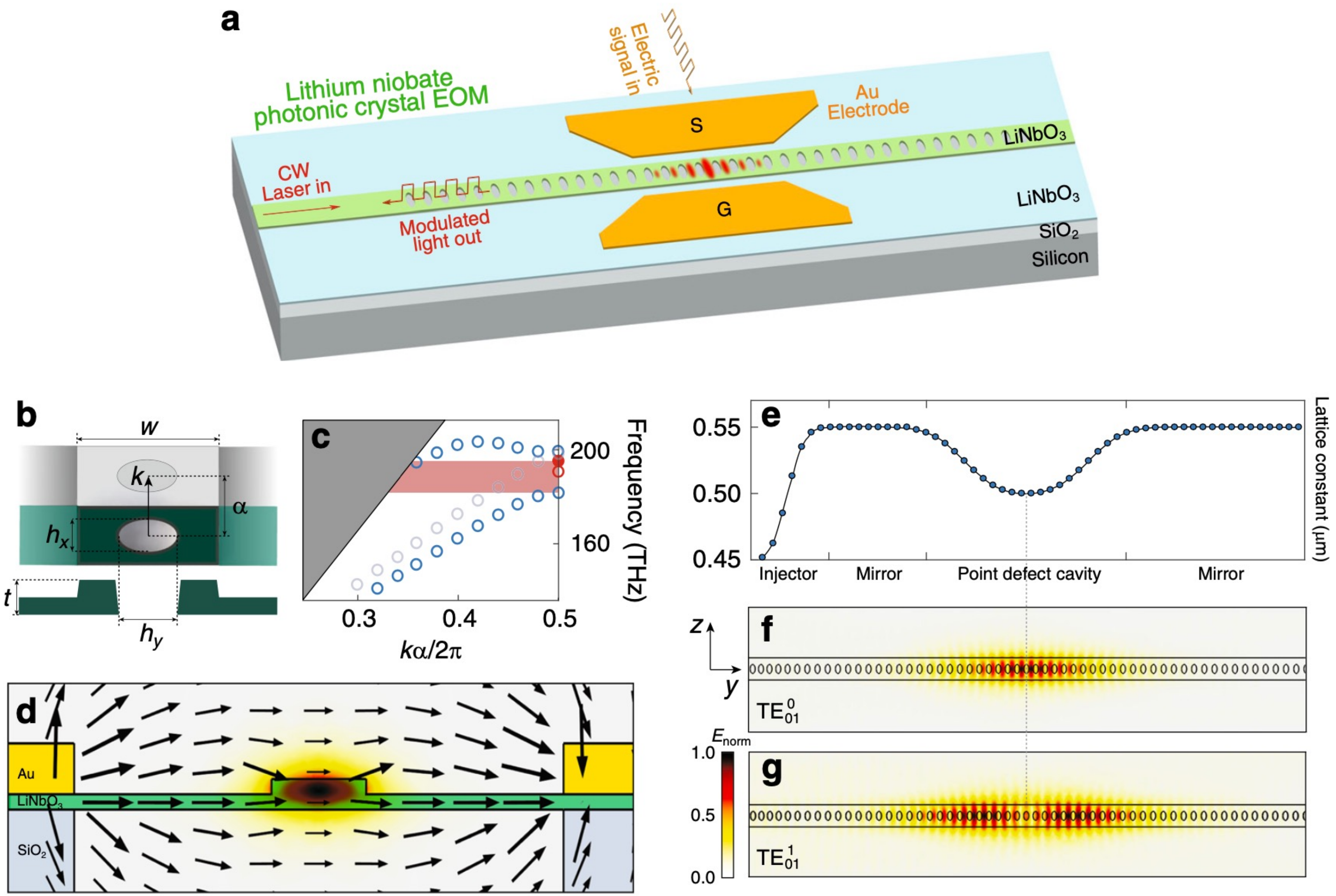
$$\Delta n = a_2E^2 = (\lambda K)E^2$$

$$\boxed{n_1' \approx n_1 + \tfrac{1}{2}n_1^3 r_{22} E_a}$$

Pockels coefficient

Applied field

$LiNbO_3$ Modulator Example



Carrier-Plasma Effect

Carriers (electron/hole) can change refractive index:

$$\begin{aligned}\Delta n &= \Delta n_e + \Delta n_h \\ &= -8.8\times 10^{-22}\Delta N_e - 8.5\times 10^{-18}(\Delta N_h)^{0.8} \\ \Delta\alpha &= \Delta\alpha_e + \Delta\alpha_h \\ &= 8.5\times 10^{-18}\Delta N_e + 6.0\times 10^{-18}\Delta N_h\end{aligned}$$

Notice: carriers also change the absorption coefficient too!

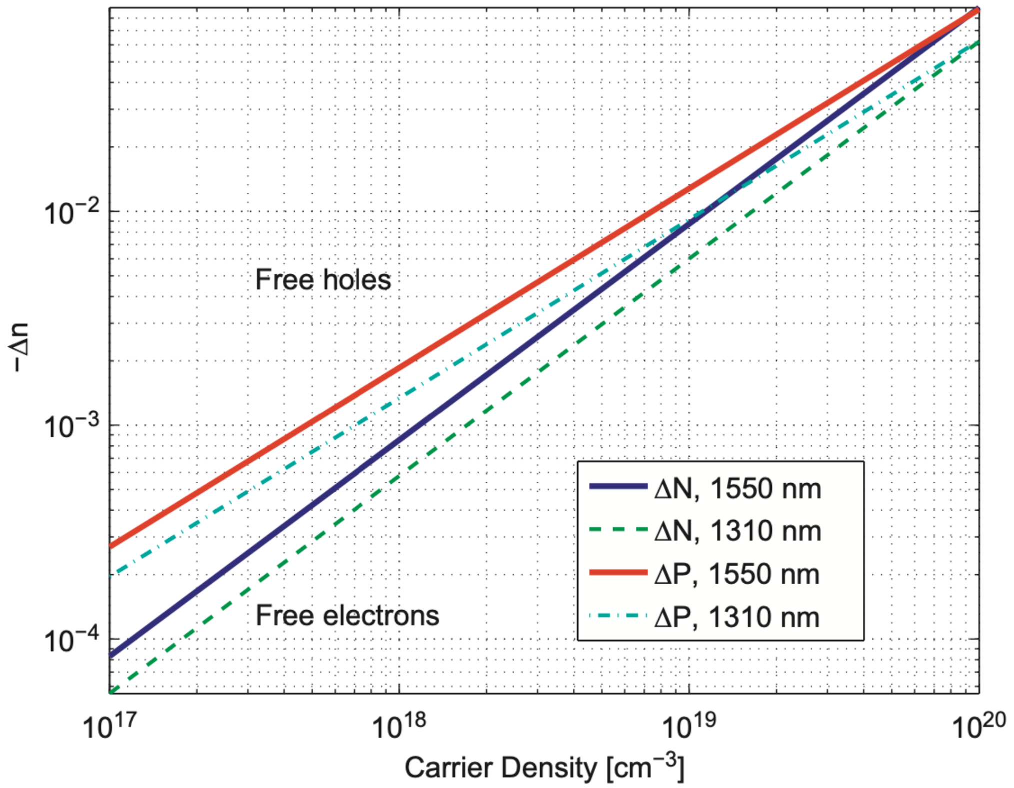


Figure 6.1 Change in index of refraction versus carrier density, Equations (6.3).

R. A. Soref and B. R. Bennett, "Electrooptical effects in silicon," IEEE Journal of Quantum Electronics, vol. 23, no. 1, pp. 123–129, Jan. 1987.

Thermo-Optical Effect in Si

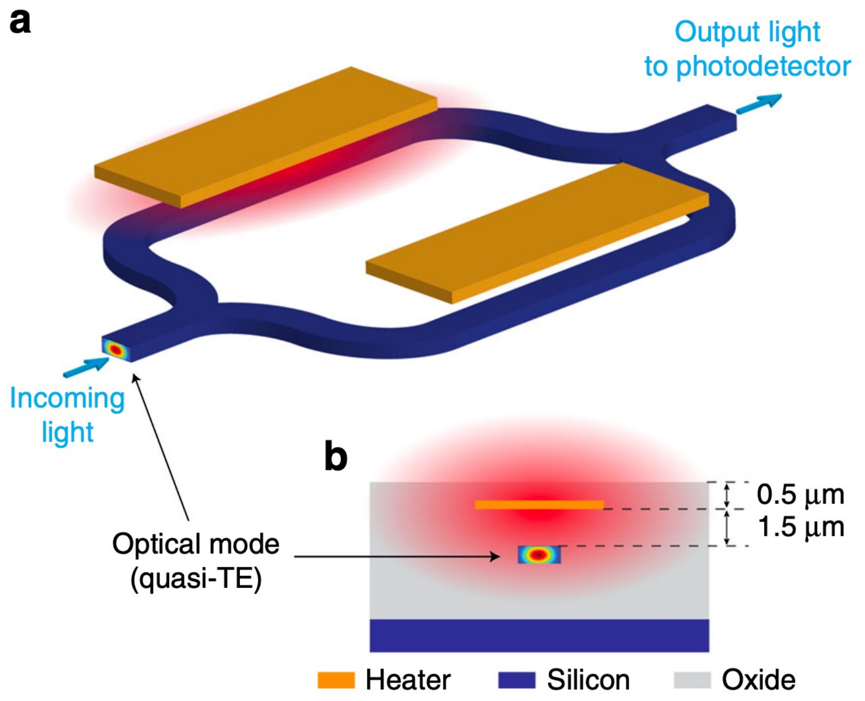
Experimentally measured data at $1.55\mu m$:

$$\frac{dn}{dT} = 9.48\times10^{-5} + 3.47\times10^{-7}T - 1.49\times10^{-10}T^2$$

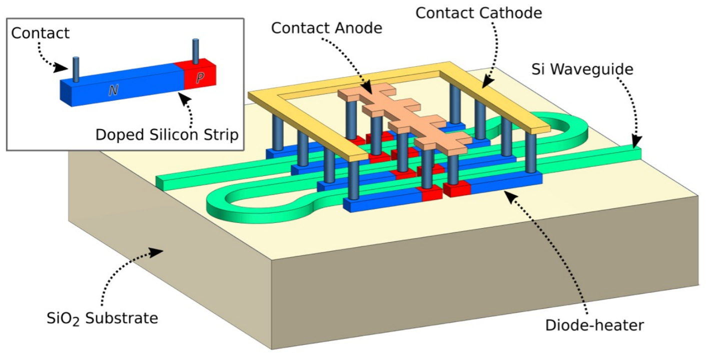
At 300K, $\dfrac{dn}{dT} \approx 1.86\times10^{-4}\ \mathrm{K}^{-1}$

With ΔT of 270K, $\Delta n \approx 0.05$

Corresponding length for π phase shift is $15.5\mu m$

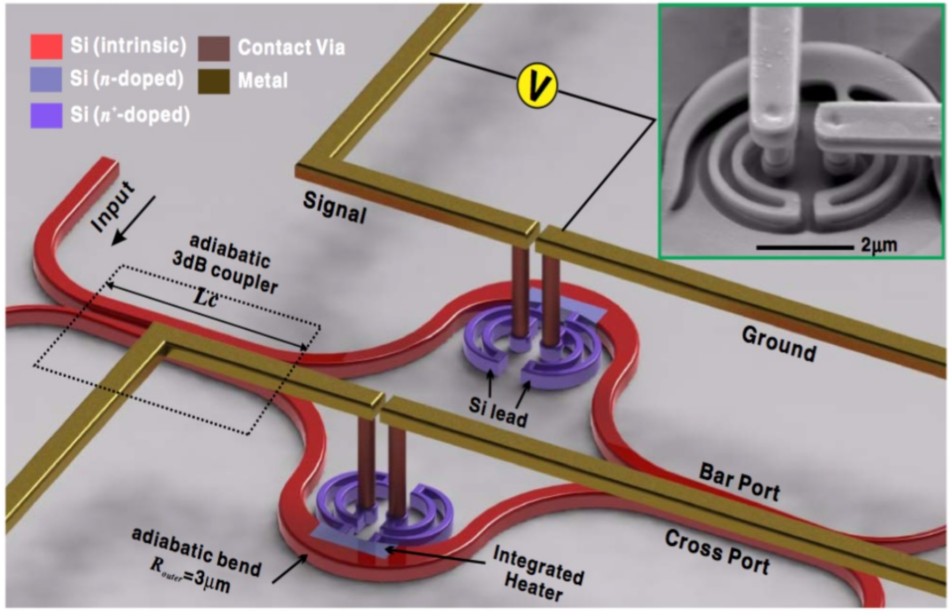


- Index change due to :
  - Thermal expansion,
  - bandgap energy reduction with temperature



ELECTRICAL & COMPUTER ENGINEERING

Thermo-Optical Effect in Si



M. R. Watts, et al., Optics Letters, 2013

- **Si thermo-optic coefficient**
  - **$dn/dT = 1.86x10^{-4}$**
  - **For $\Delta T \approx 500^{\circ}$ C**
  - **$\Delta n \approx 3\%$, $L_{\pi} \approx 10$ um**
- **Steady power consumption**
  - **$P_{\pi} \approx 10$ mW**

- Relatively strong compared with carrier effect
- Low optical loss introduced by heating
- Usually slow, limited by thermal RC time.
- Modulation time is on the order of milli-sec (For small structures, can be micro-sec)
- Too slow for modulators, but often used in tunable filters, switches, etc.
- High power consumption

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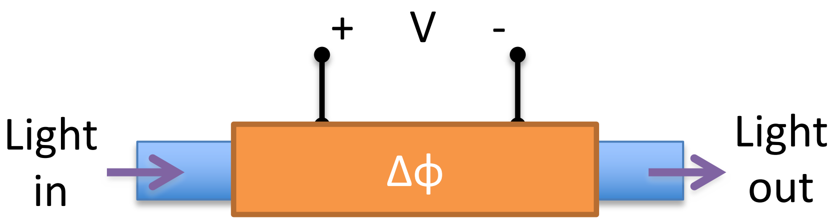
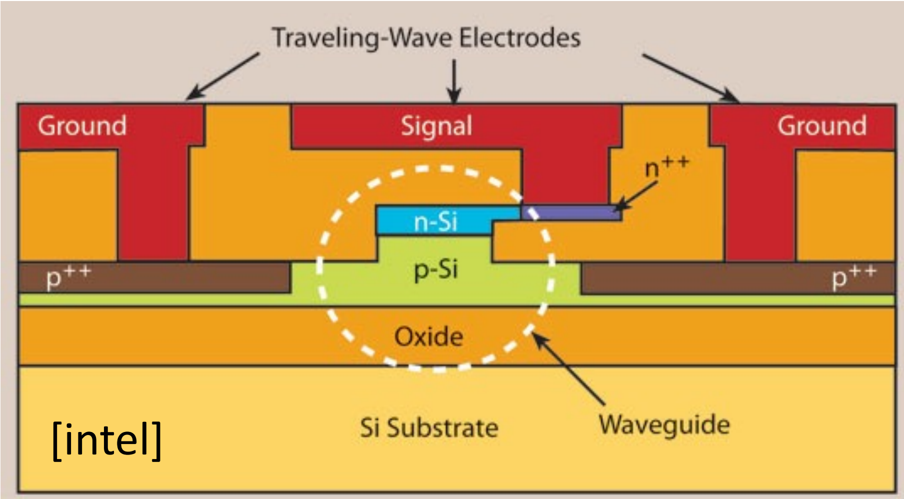
Phase Shifters in Silicon

- Pockels effect (not in Si)
- Thermal (efficient but slow ☹)
- **Carrier Plasma Effect [Soref]**
  - PN-Junction (diodes)
  - SIS-Cap

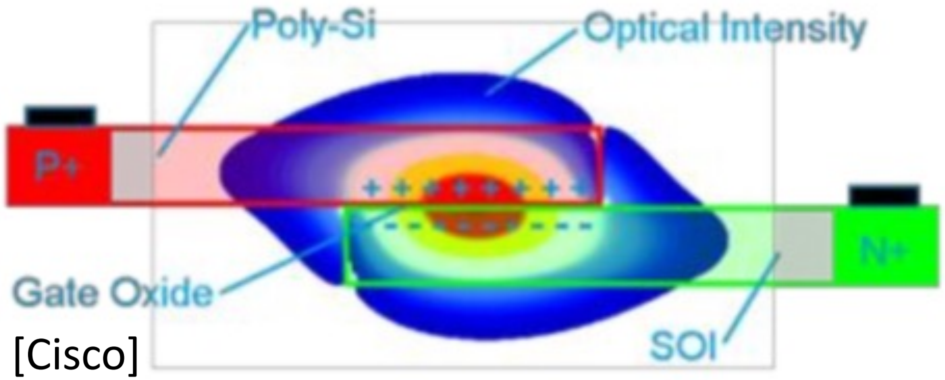


$$\Delta\phi = \frac{2\pi}{\lambda}\Delta n_{\mathrm{eff}} L$$

$$\begin{aligned}\Delta n &= \Delta n_e + \Delta n_h \\ &= -8.8\times10^{-22}\Delta N_e - 8.5\times10^{-18}(\Delta N_h)^{0.8} \\ \Delta\alpha &= \Delta\alpha_e + \Delta\alpha_h \\ &= 8.5\times10^{-18}\Delta N_e + 6.0\times10^{-18}\Delta N_h\end{aligned}$$

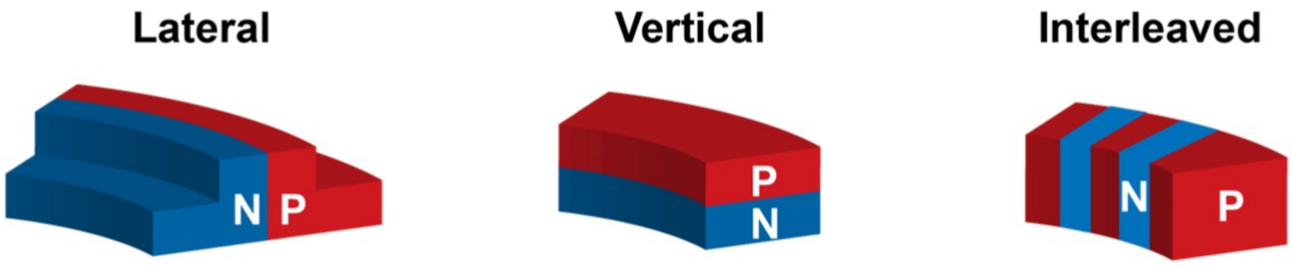


[intel]

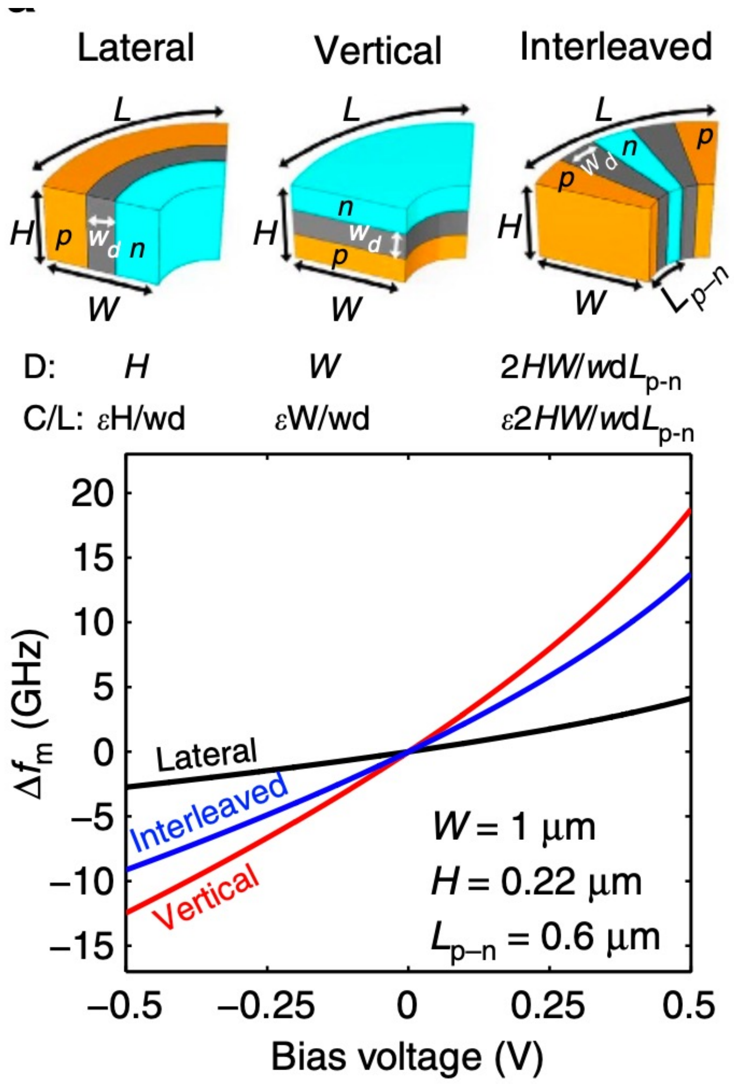


[Cisco]

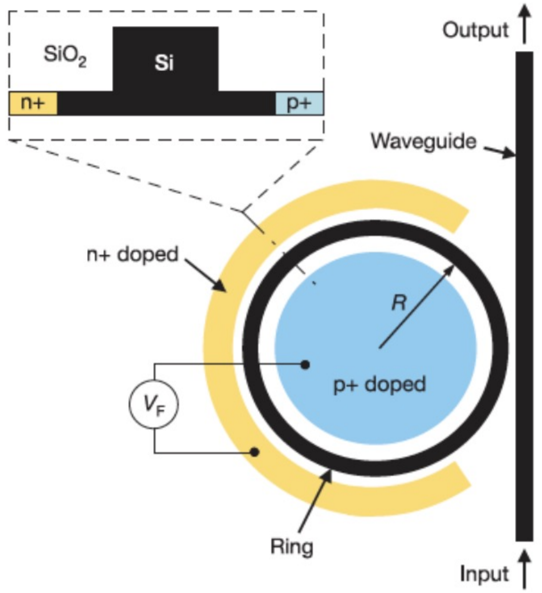
PN-Junction based Modulators

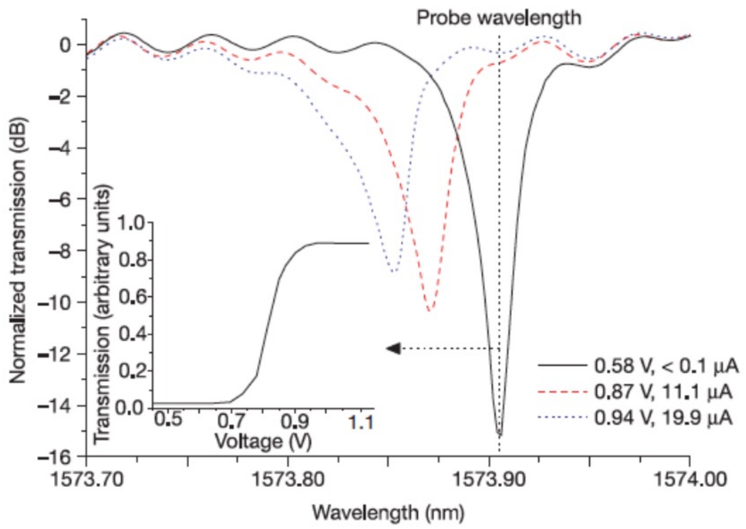


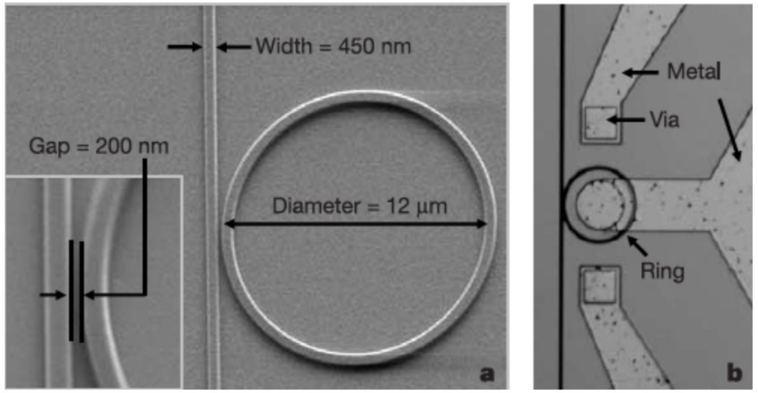
- Efficiency:
  - Max charge/V
  - Max optical mode interaction with charge
- Operation modes:
  - Carrier injection (forward bias)
  - Depletion mode (reverse bias)



Microring Modulator



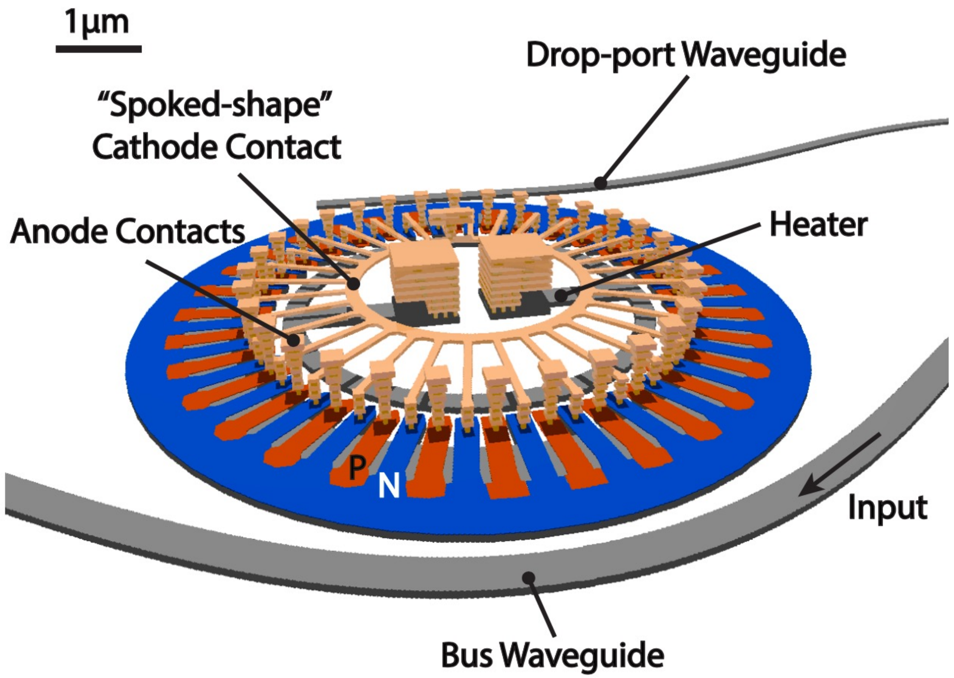




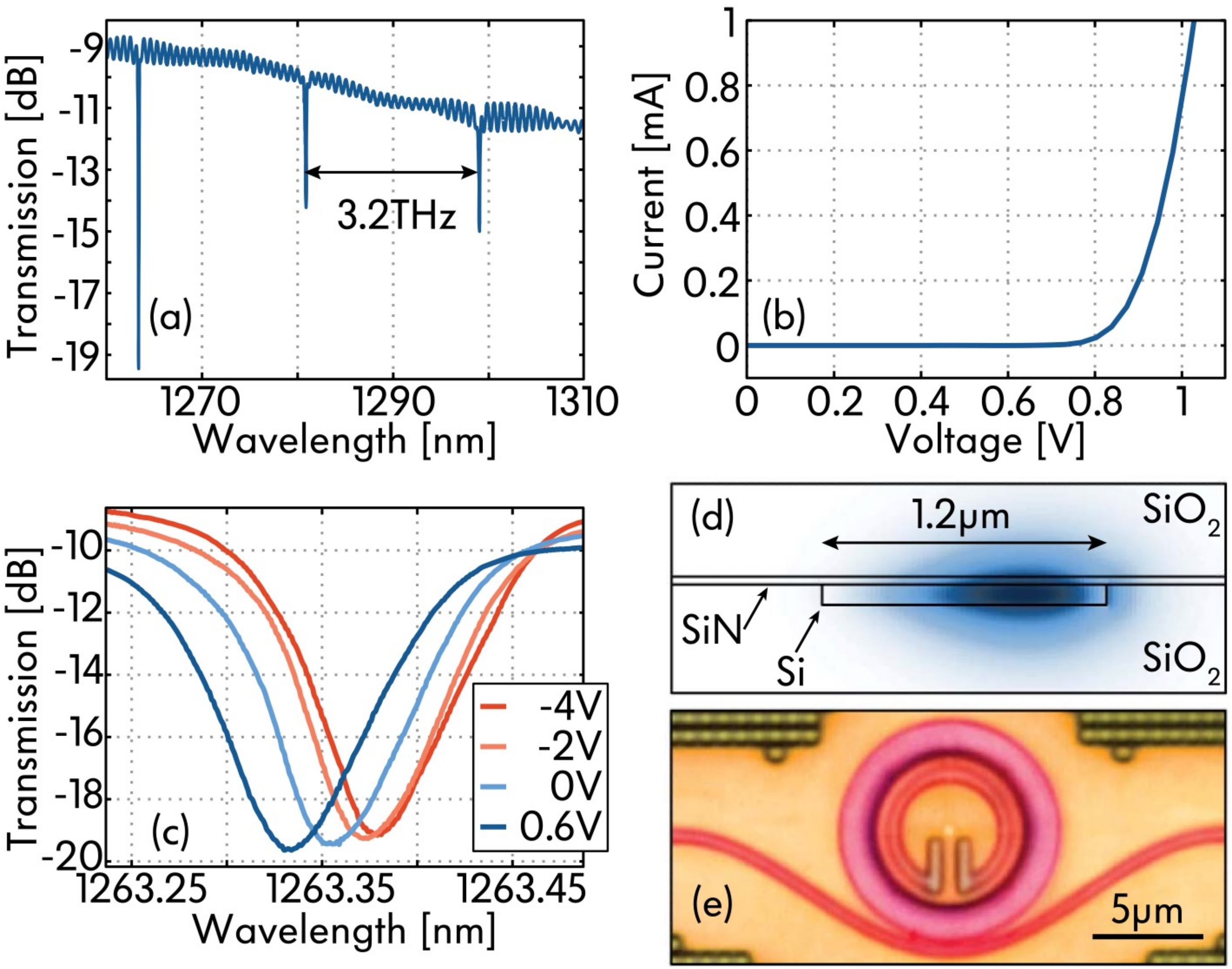
- **Use resonance in microring to enhance the modulation**
- **Reduce modulator size from millimeters to tens of microns**
- **Enhanced modulation efficiency**
- **Reduced bandwidth**
- **Must match laser/resonator wavelengths**

Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometre-scale silicon electro-optic modulator," Nature, vol. 435, no. 7040, pp. 325–327, May 2005.

MRM Example

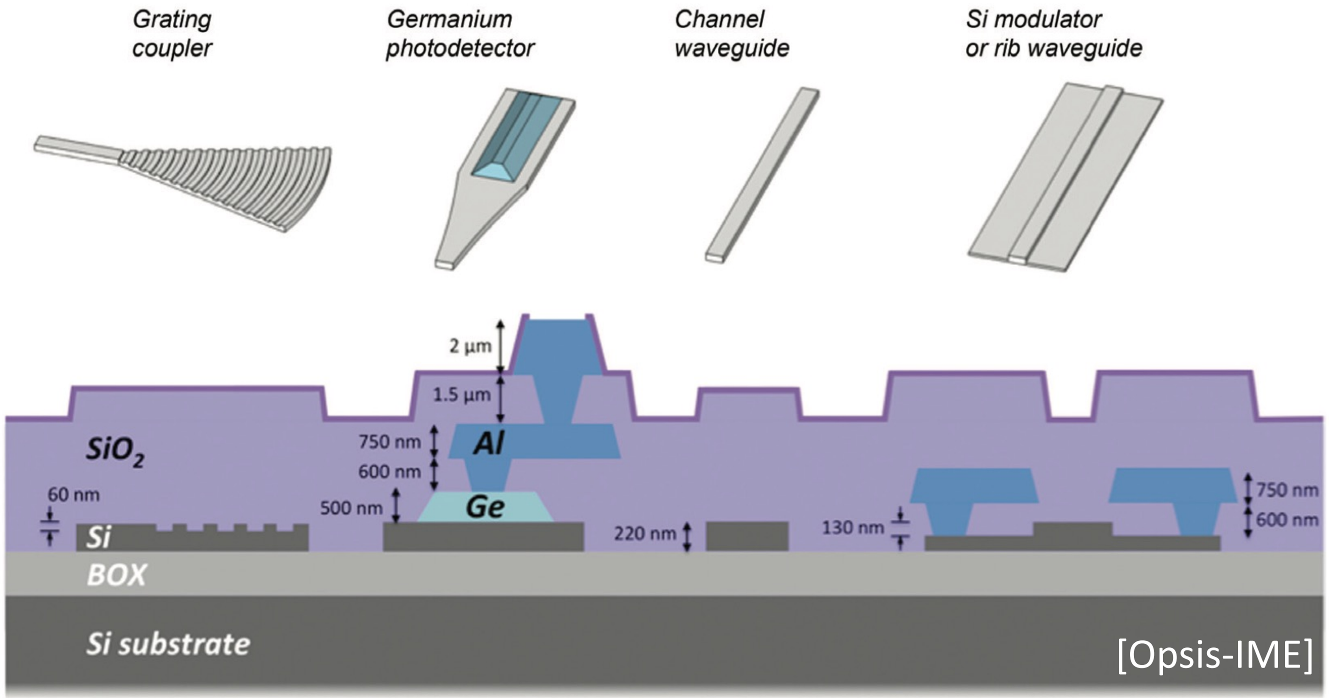


1μm
Drop-port Waveguide
"Spoked-shape"
Cathode Contact
Anode Contacts
Heater
P
N
Input
Bus Waveguide



Transmission [dB]
-9
-11
-13
-15
-17
-19
3.2THz
(a)
1270
1290
1310
Wavelength [nm]
Current [mA]
1
0.8
0.6
0.4
0.2
0
(b)
0
0.2
0.4
0.6
0.8
1
Voltage [V]
Transmission [dB]
-10
-12
-14
-16
-18
-20
(c)
-4V
-2V
0V
0.6V
1263.25
1263.35
1263.45
Wavelength [nm]
(d)
1.2μm
SiO2
SiN
Si
SiO2
(e)
5μm

SOI Photonics Process

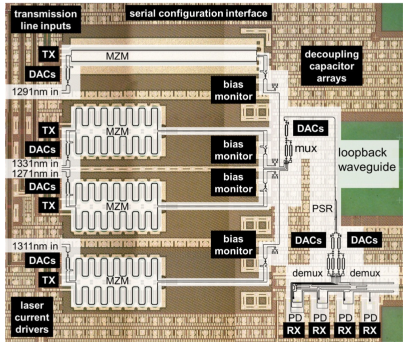


- SOI: Silicon-on-insulator
  - 220nm Crystalline Si + 1.5um Buried Oxide (BOX)
- Partial Etch on Si for patterning Grating Couplers
- Epitaxially grown Ge for photo-detection

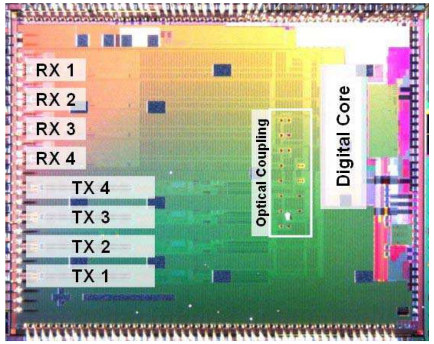
Merging Electronics & Photonic

Integration determines Energy, Cost, Speed, … !

Monolithic



[IBM, OFC 16]



[Luxtera, Hot Chips 09]

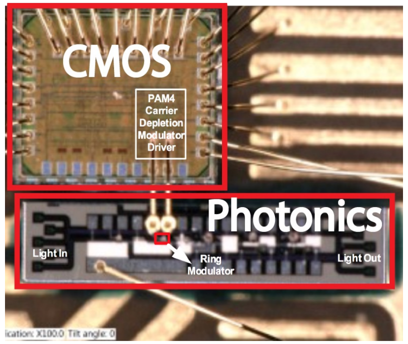
Closest Proximity

High Interconnect Density

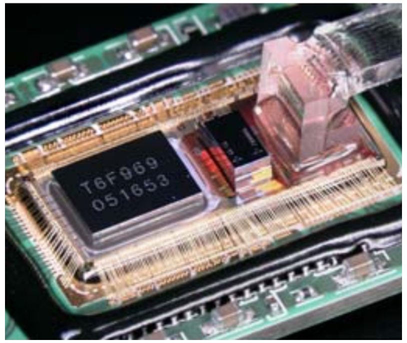
Low Cost

Old CMOS

Hybrid / 3D



[Roshan-Zamir, OI 16]



[Luxtera, IEDM 17]

Large Parasitics

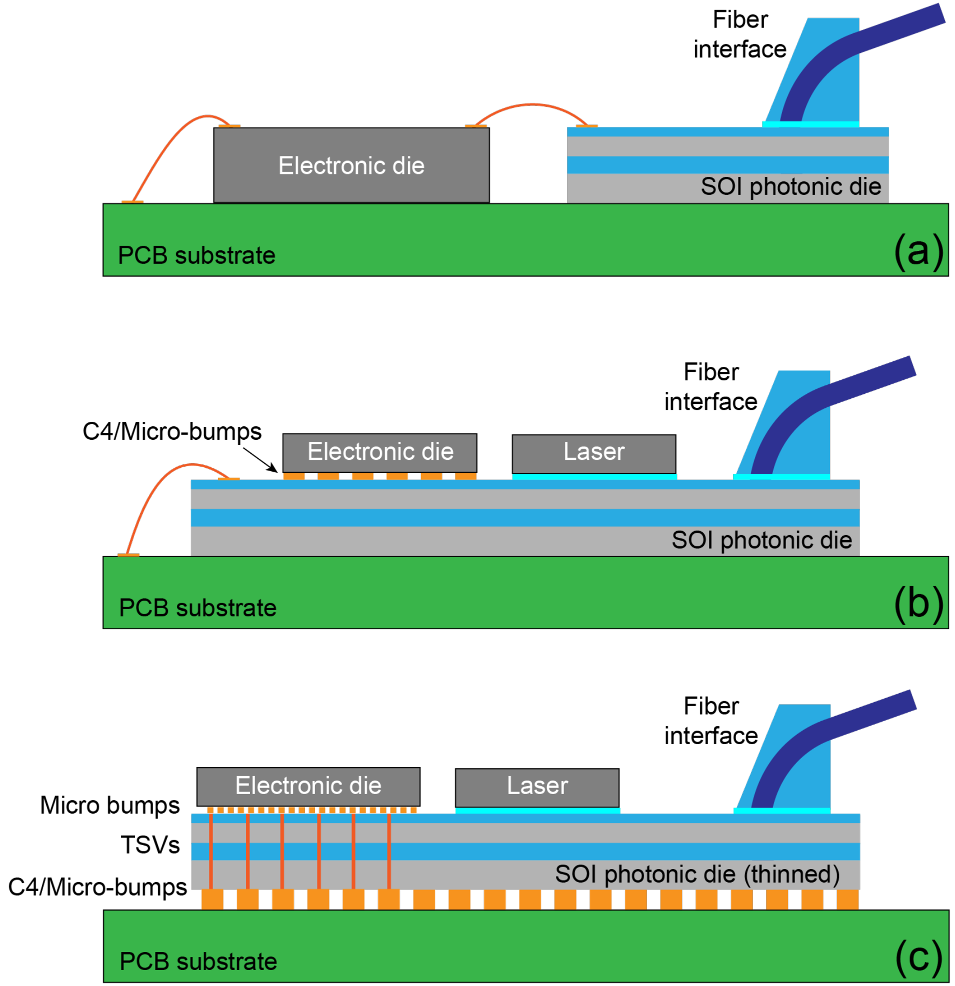
Low Interconnect Density

High Cost

Advanced CMOS

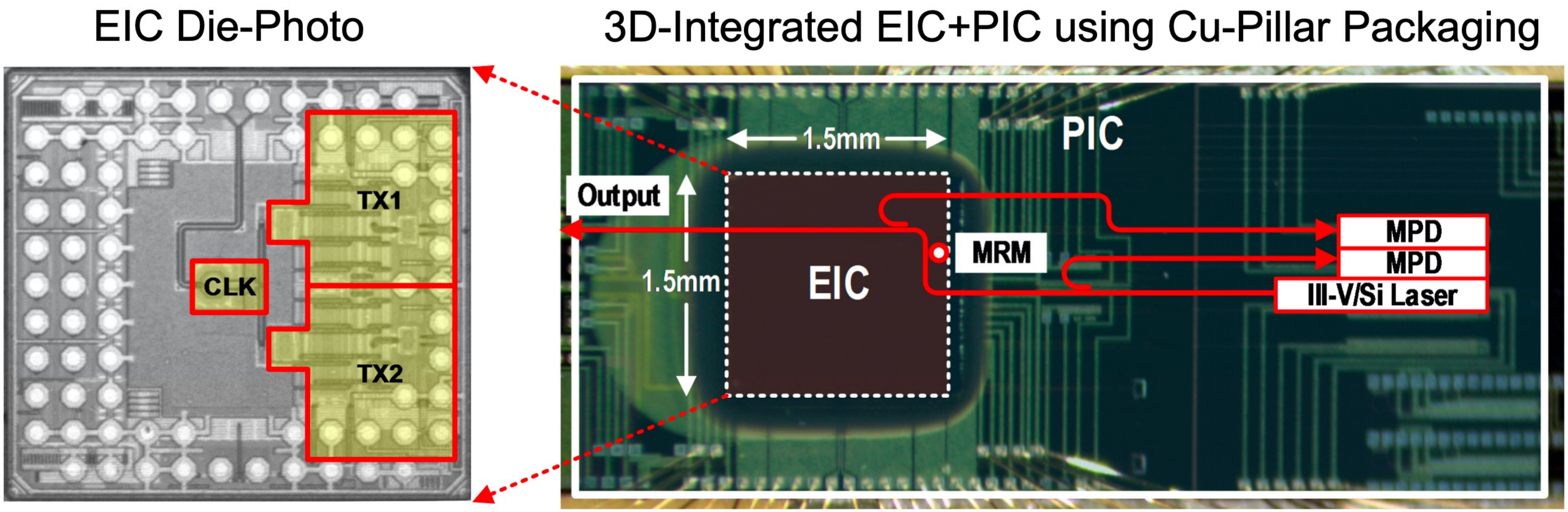
3D/Hybrid Electronic-Photonic Integration

- **Interconnects:**
  - In-between Photonic IC (PIC) and CMOS
  - Highspeed I/O & power supplies for CMOS
- **Interconnect's parasitics & density matter!**
  - Directly impacts speed, energy, and bandwidth density, …
- Cost
  - Die-level or Wafer-level
- Compatibility with 3D SoC co-packaging



ELECTRICAL & COMPUTER ENGINEERING

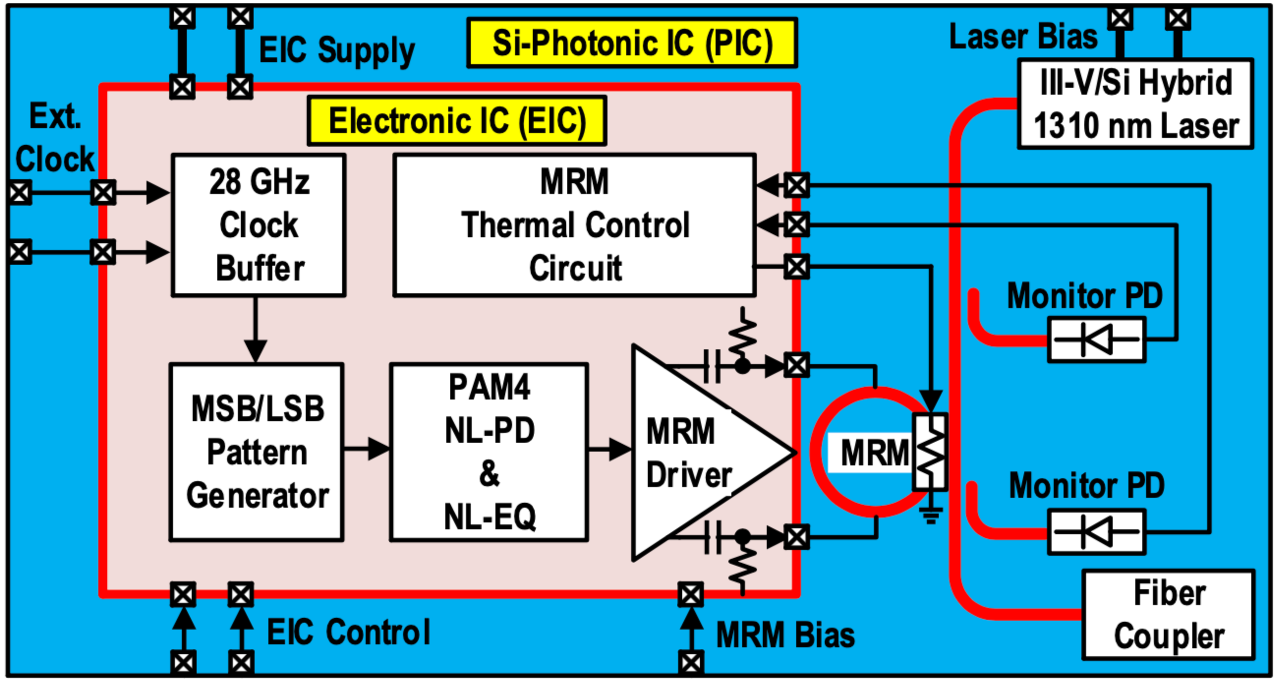
Example: Intel PAM-4 TX

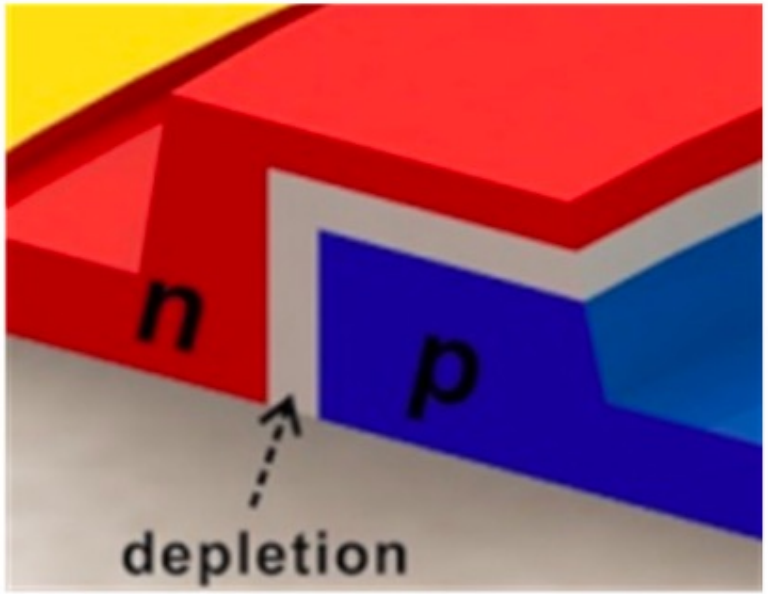


- Cu-pillars: 20-40um pitch (No TSV in PIC)
- Interconnect parasitic (including pads): 80fF (~3x modulator's capacitance!)
- 112Gb/s PAM-4 transmitter @6pJ/b

Example: Intel PAM-4 TX

3D-Integrated Si-Photonic Transmitter

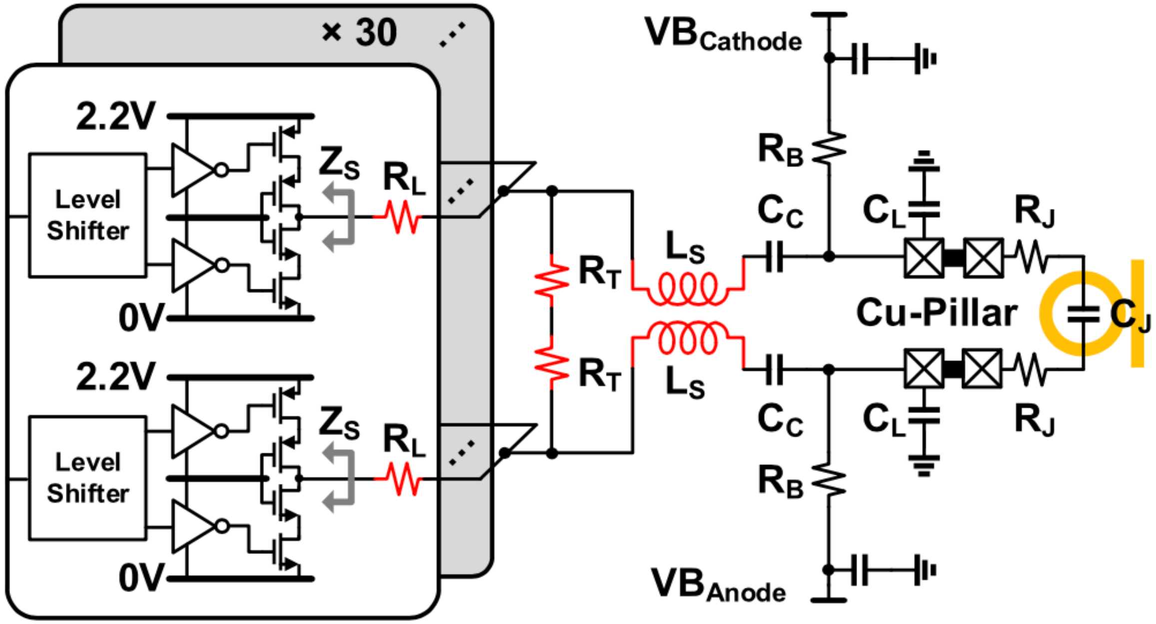




[J. Sun, OFC2018]

ELECTRICAL & COMPUTER ENGINEERING

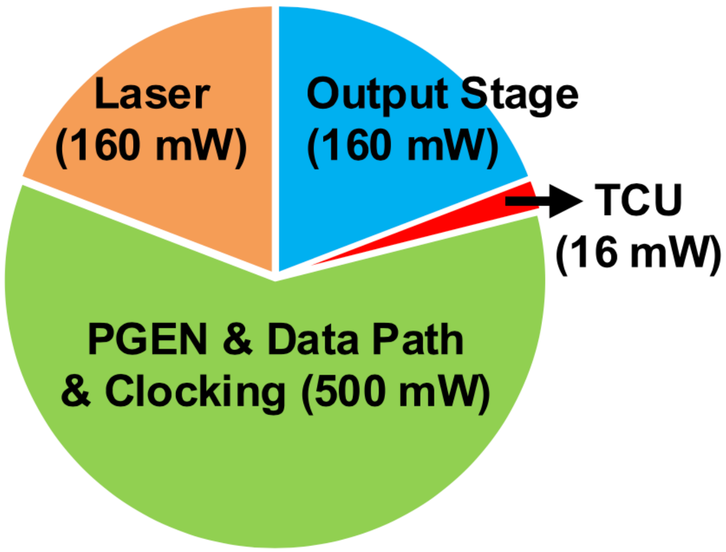
Parasitics in 3D integration



Z_S	250Ω
R_L	500Ω (1X Slice)
R_T	75Ω
L_S	100pH
C_C	2pF
R_B	40kΩ
$^*C_L$	80fF
R_J	25Ω
C_J	30fF

*EIC and PIC Pads.

OTX Power Breakdown @ 112 Gb/s



Driver VDD: 2.2V
Digital VDD: 1.2V

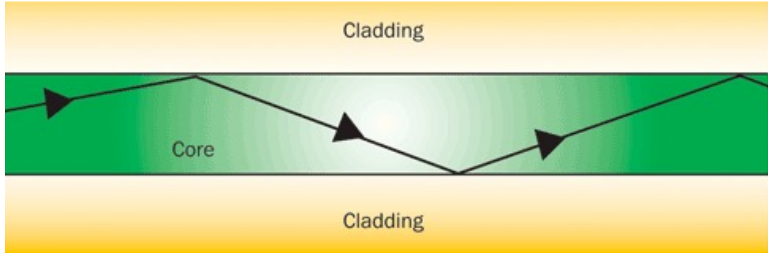
- Notice: Interconnect parasitic = 3 x device cap!!!

Comparison with 3D-Integrated MZM-TX

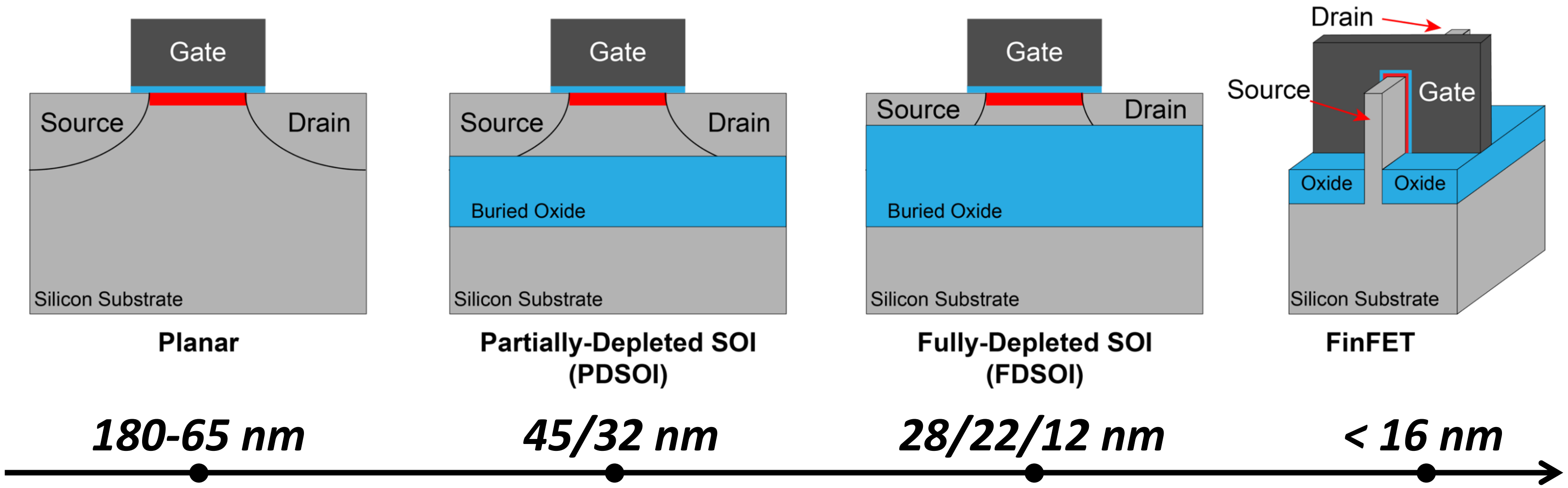
	G. Denoyer JLT 2015	E. Temporiti ISSCC 2016	C. Li BCICTS 2018	This Work
Modulator	TW-MZM	TW-MZM	Segmented-MZM	MRM
Device Size	3.36mm	3mm	7mm	20um
On-Chip Laser	No	No	No	Yes
EIC Process	130nm BiCMOS	55nm BiCMOS	16nm CMOS	28nm CMOS
Signaling	NRZ	NRZ	PAM-4	PAM-4
Data Rate	56Gb/s	56Gb/s	56Gb/s	112Gb/s
Driver Swing	$4V_{pp}$	$1.6V_{pp}$	$1.8V_{pp}$	$3V_{pp}$
On-Chip Pattern Gen. + Serializer	Yes	No	Yes	Yes
EIC Power	593mW	300mW	708mW	*676mW
EIC-only Energy-Efficiency	10.6pJ/bit	5.35pJ/bit	12.6pJ/bit	6pJ/bit

*Excluding 160mW on-chip laser power.

Monolithic Photonics in CMOS Technology



1st Step: Building a low-loss optical waveguide

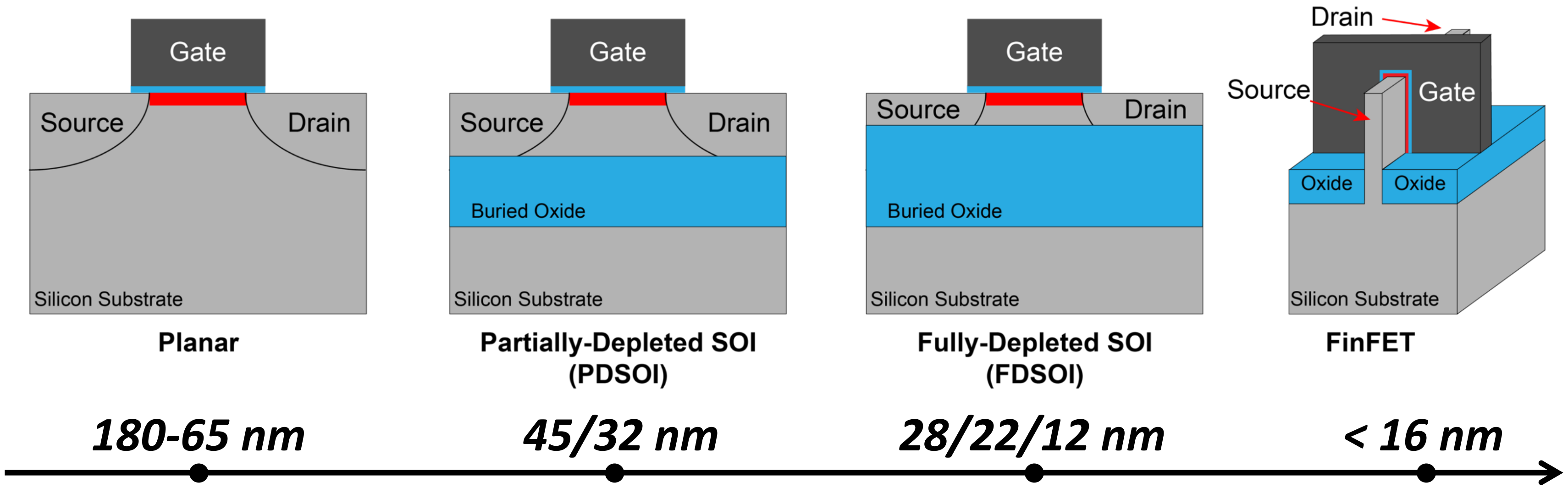


Bulk CMOS: Standard Silicon Wafers (Planar / FinFET)

SOI: Silicon-on-Insulator (PDSOI / FDSOI)

Monolithic Photonics in CMOS Technology

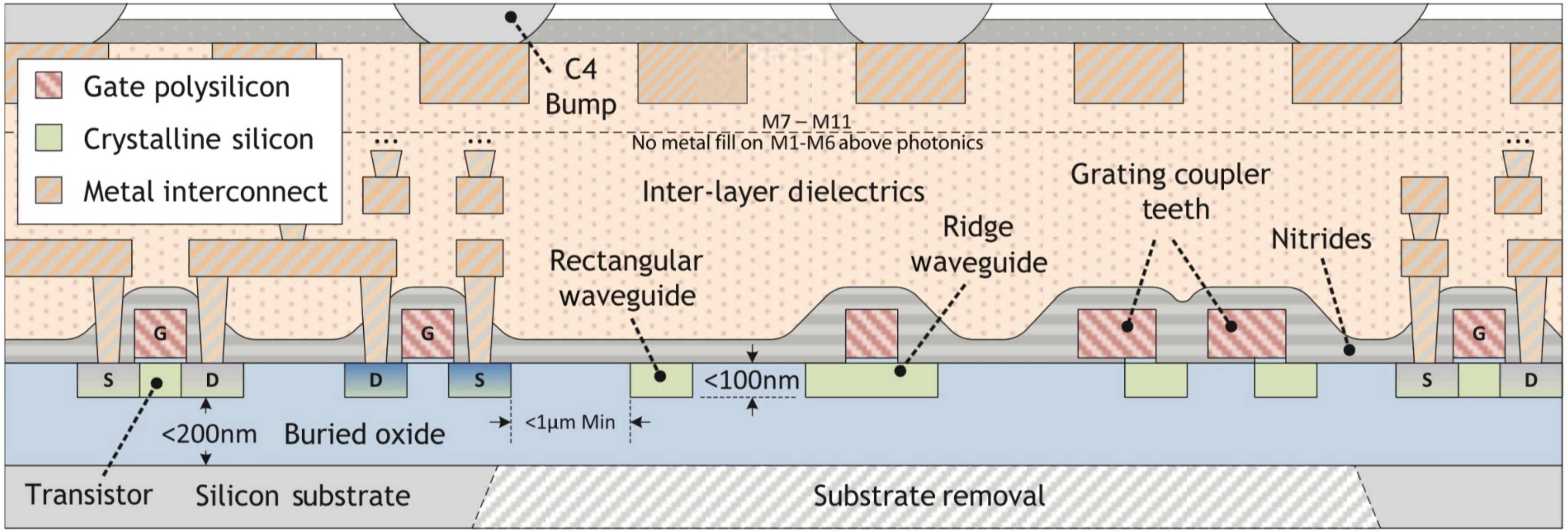
Only *PDSOI* processes can naturally provide low-loss optical waveguides without any process change



Bulk CMOS: Standard Silicon Wafers (Planar / FinFET)

SOI: Silicon-on-Insulator (PDSOI / FDSOI)

Zero-Change in 45nm SOI CMOS

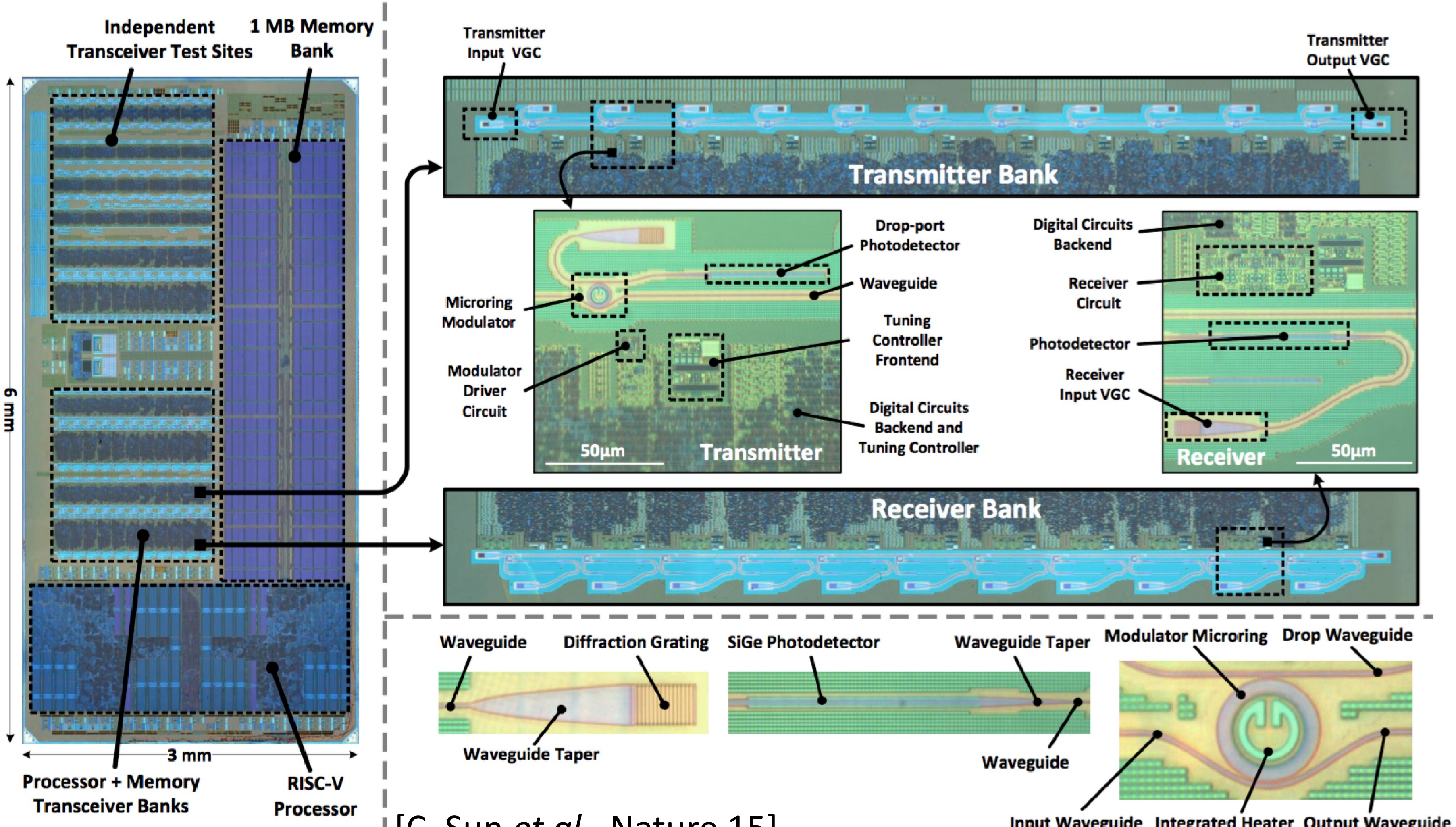


- Photonics for free! (No modification to the process)
- Closest proximity of electronics and photonics
- Single substrate removal post-processing step

ELECTRICAL & COMPUTER ENGINEERING

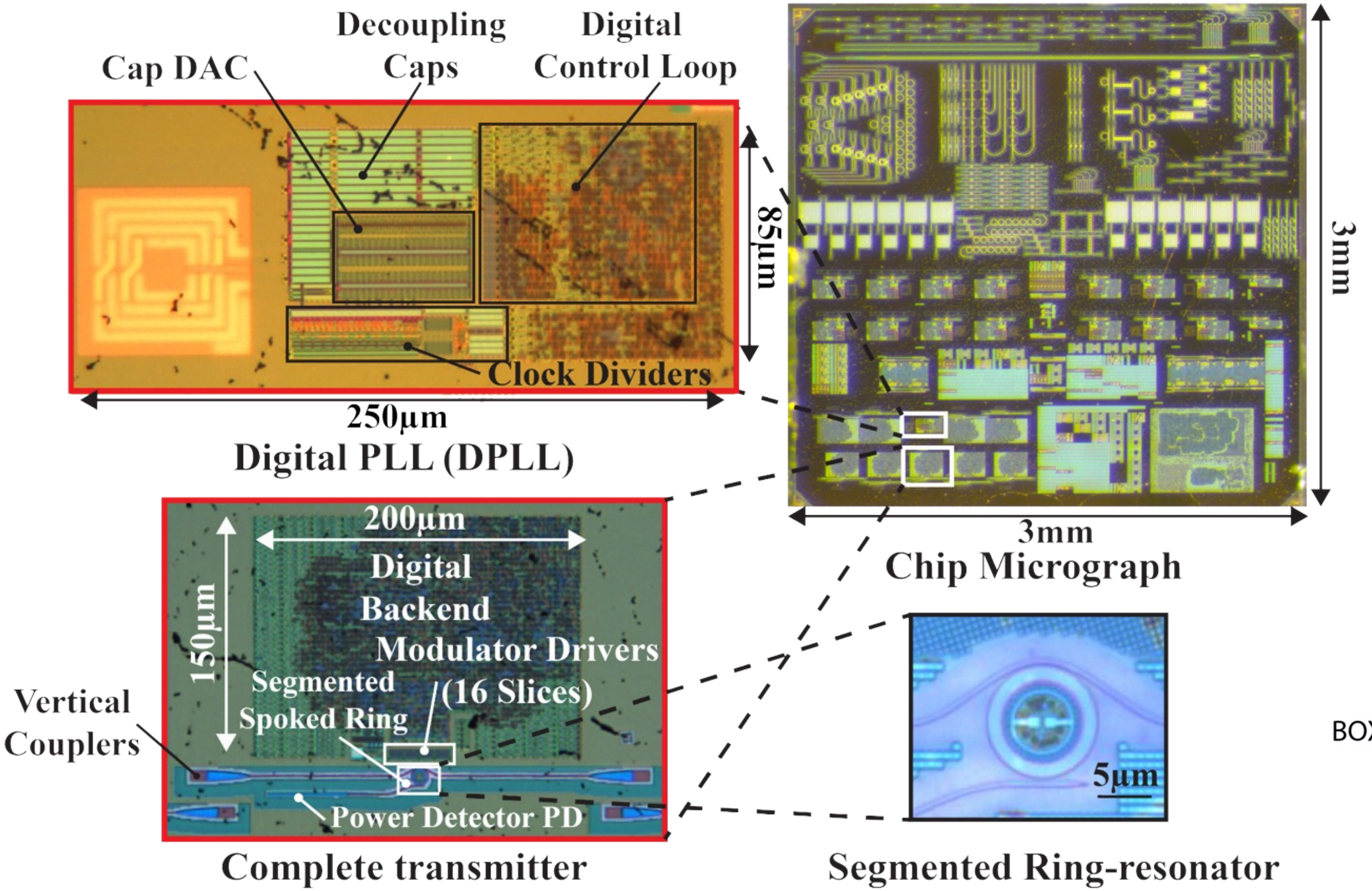
Microprocessor with Optical I/O

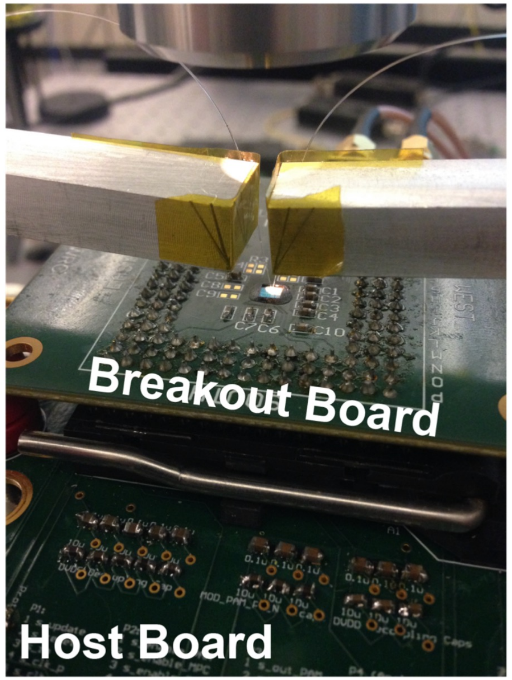
Millions of transistors + Hundreds of photonic devices

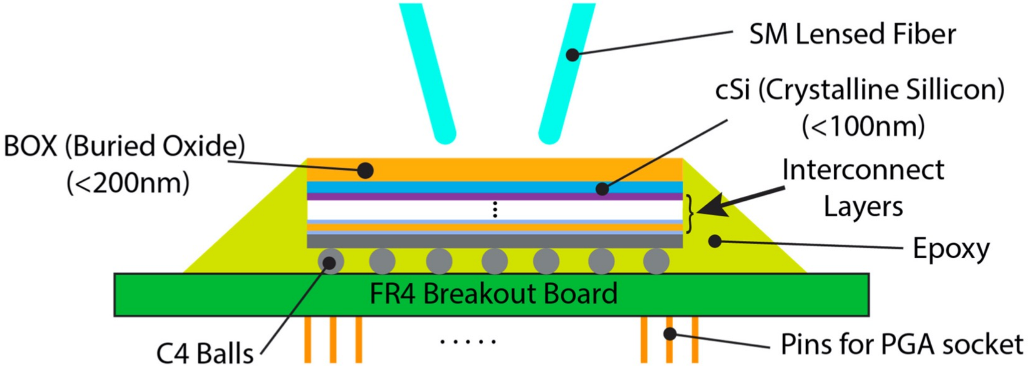


[C. Sun *et al.*, Nature 15]

Zero-change Platform



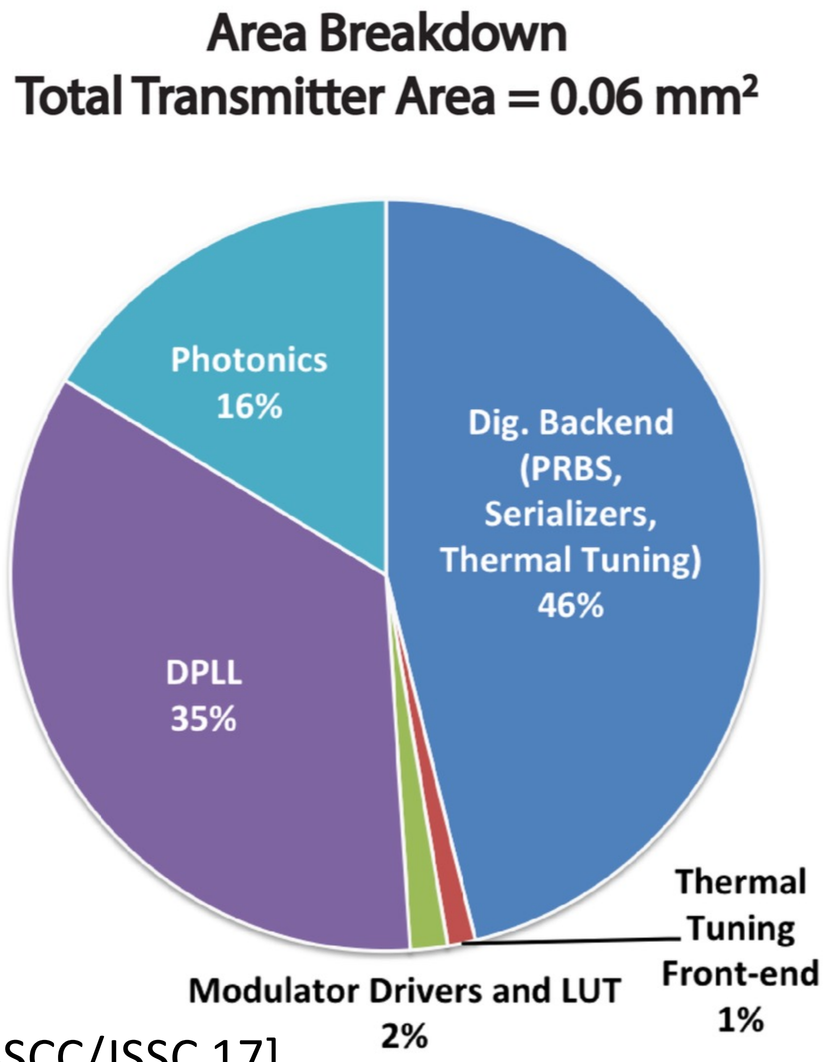


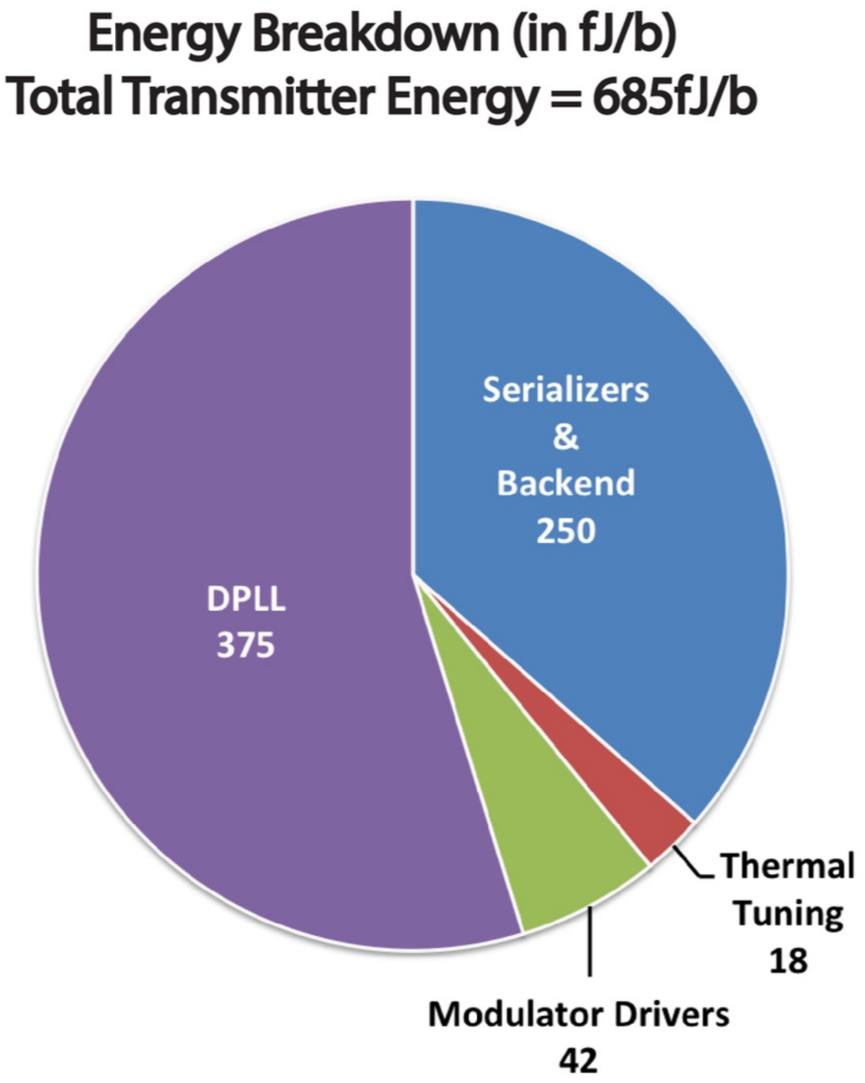


[Moazeni *et al.*, ISSCC/JSSC 17]

ELECTRICAL & COMPUTER ENGINEERING

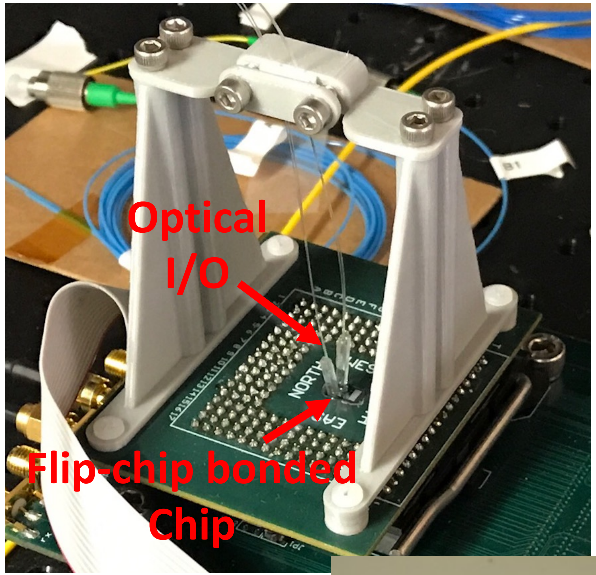
Area/Energy Breakdown

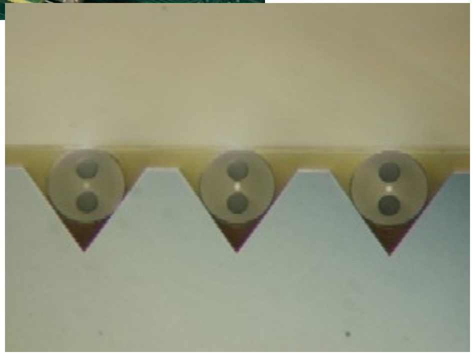




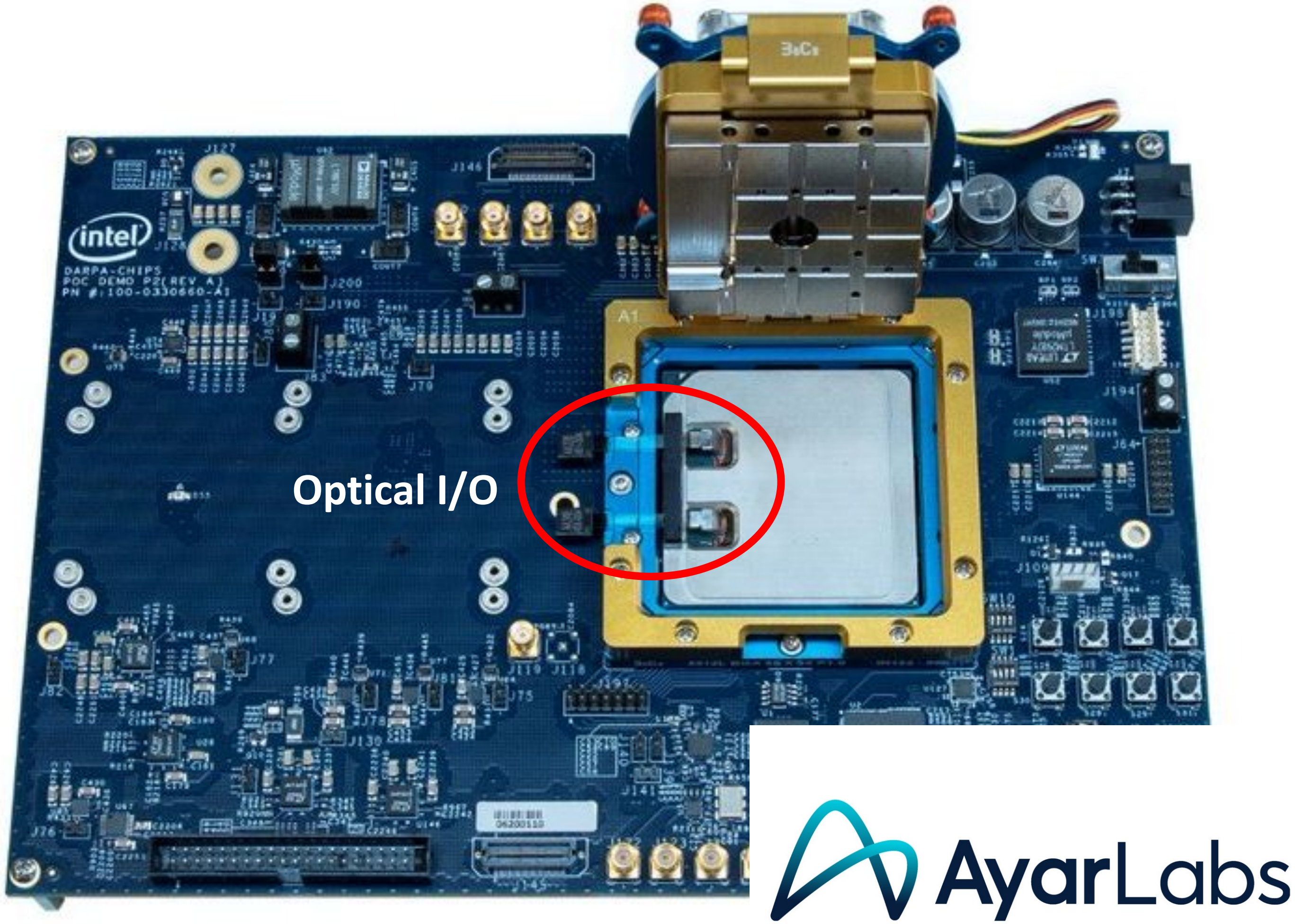
[Moazeni *et al.*, ISSCC/JSSC 17]

Optical Packaging

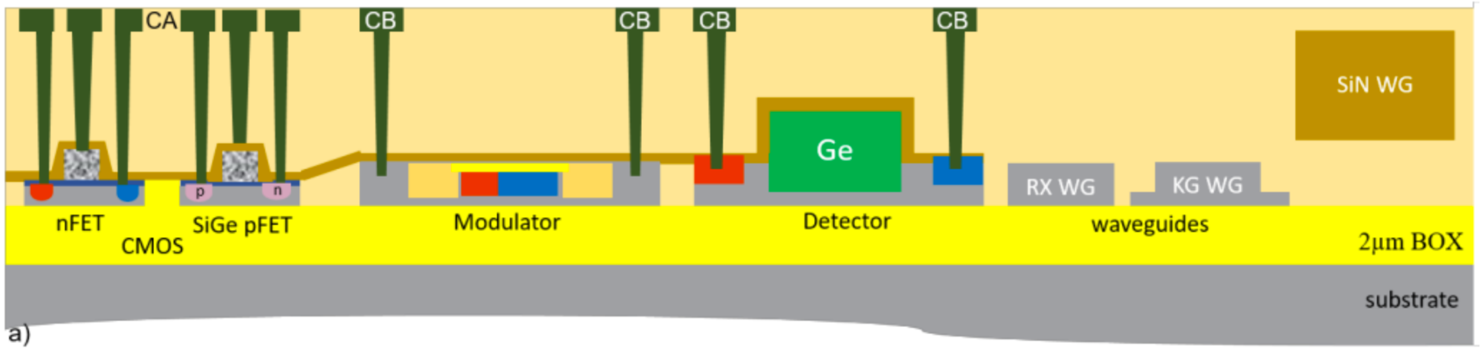


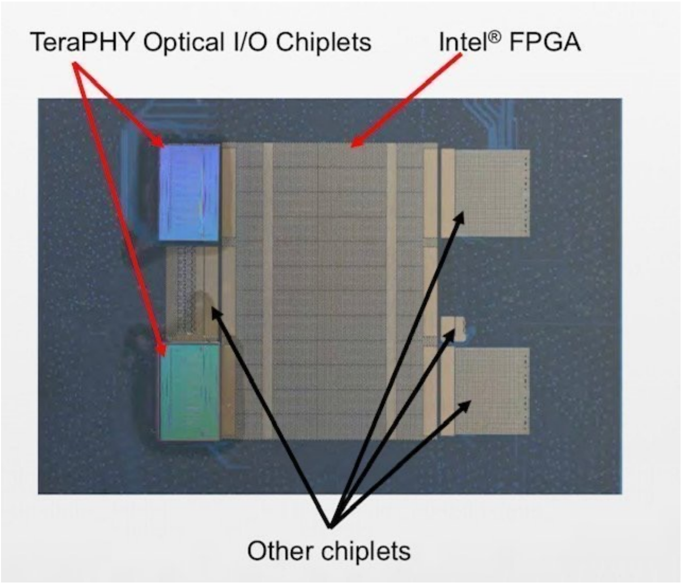


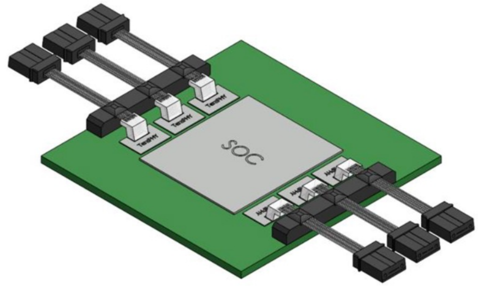
V-groove Fiber Array



45nm Monolithic SiPh (45CLO)





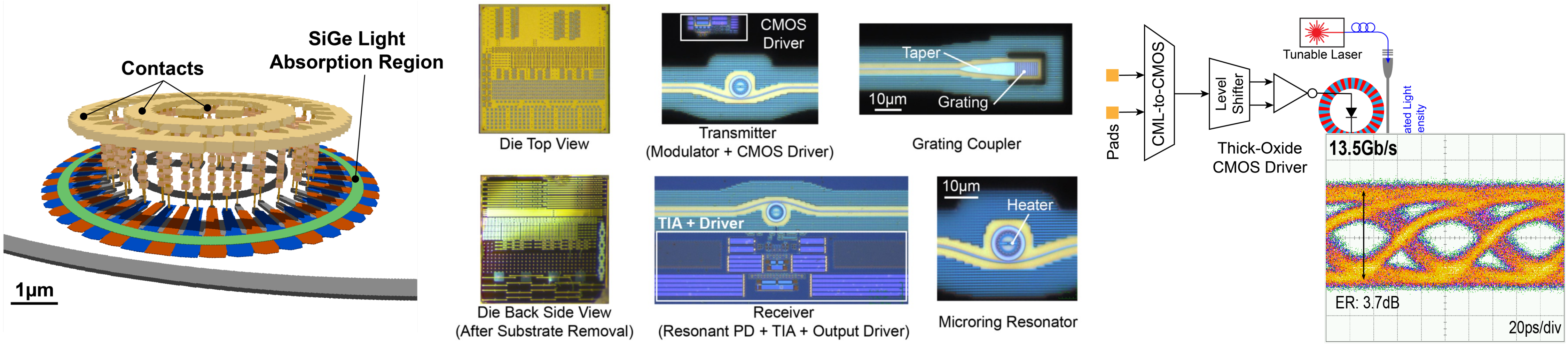


- In-package Optical I/O with Ayar Labs
- Process now commercialized and soon available by Global Foundries (called 45CLO) [starting 2021]

ELECTRICAL & COMPUTER ENGINEERING

Zero-change in 32nm SOI CMOS

- Faster than 45nm (33% faster logic)
- Extra features to improve photonics (New photodiode design using channel SiGe)
- *In-situ* device characterization & full Electro-photonic capability

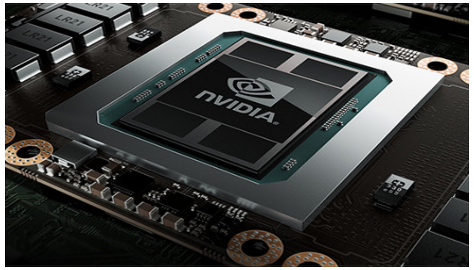


Monolithic photonics next to the fastest transistors

[Moazeni *et al.*, IEDM 17]

Photonics in Bulk CMOS

Enabling photonics for high-performance electronic chips in the state-of-the-art CMOS (sub-10*nm*)



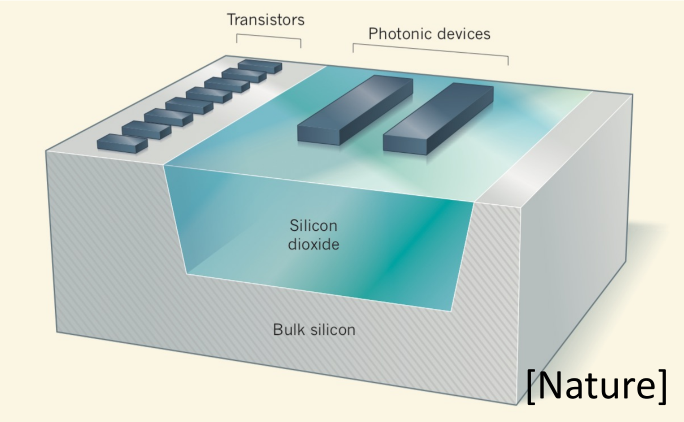
Nvidia Volta (12nm FinFET)
CPU/GPU

Broadcom (16nm FinFET)
Network Switch

Samsung (10nm LPP)
Memory (e.g DRAM)

First monolithic photonics platform in a 300mm-wafer bulk CMOS process

[Atabaki*, Moazeni* *et al.*, Nature 18]



[Nature]

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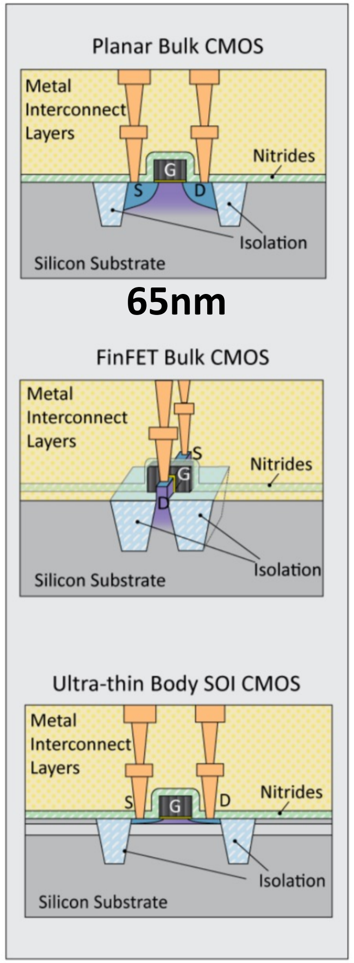
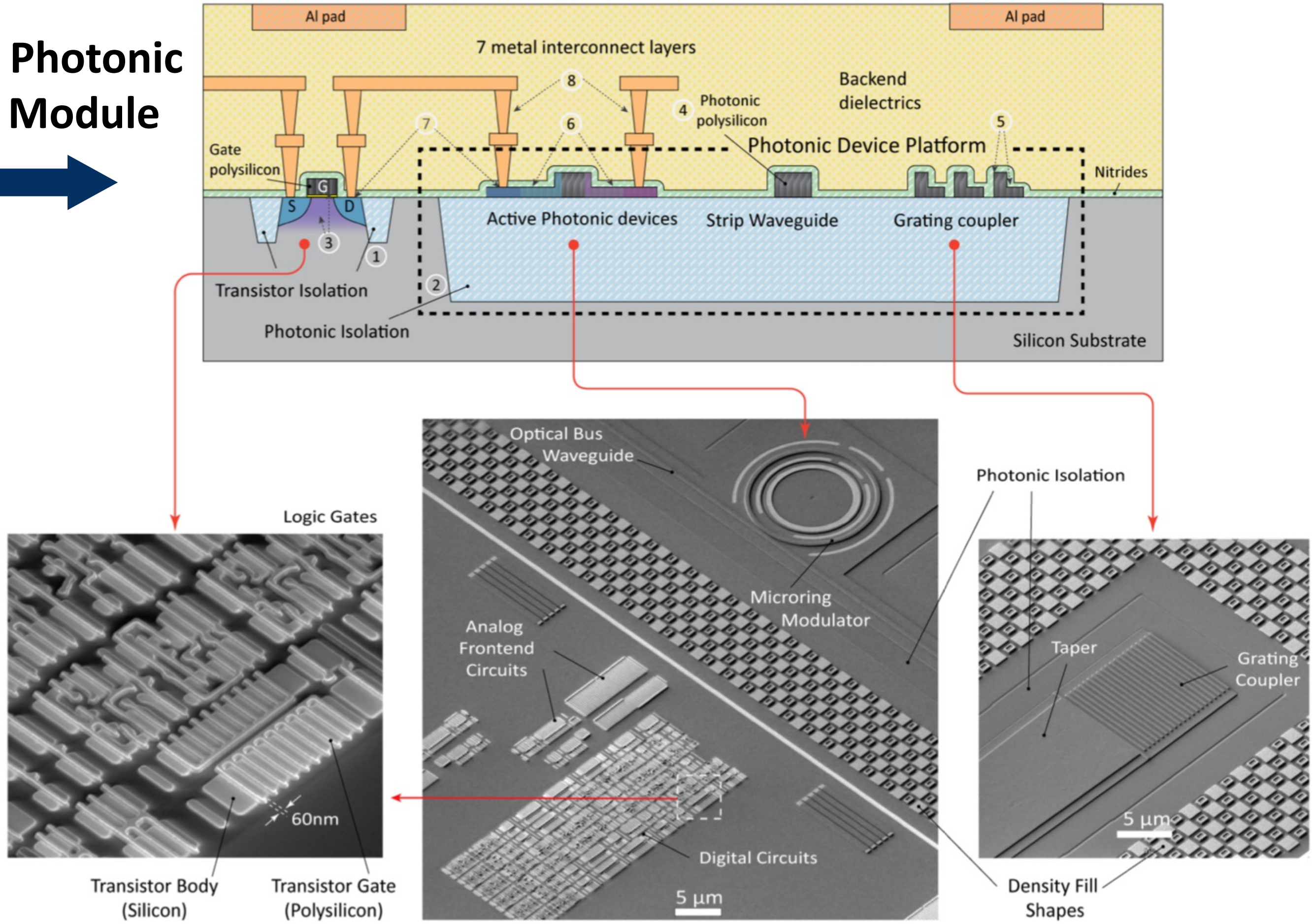
Integration Approach



Inserting Photonic Process Module

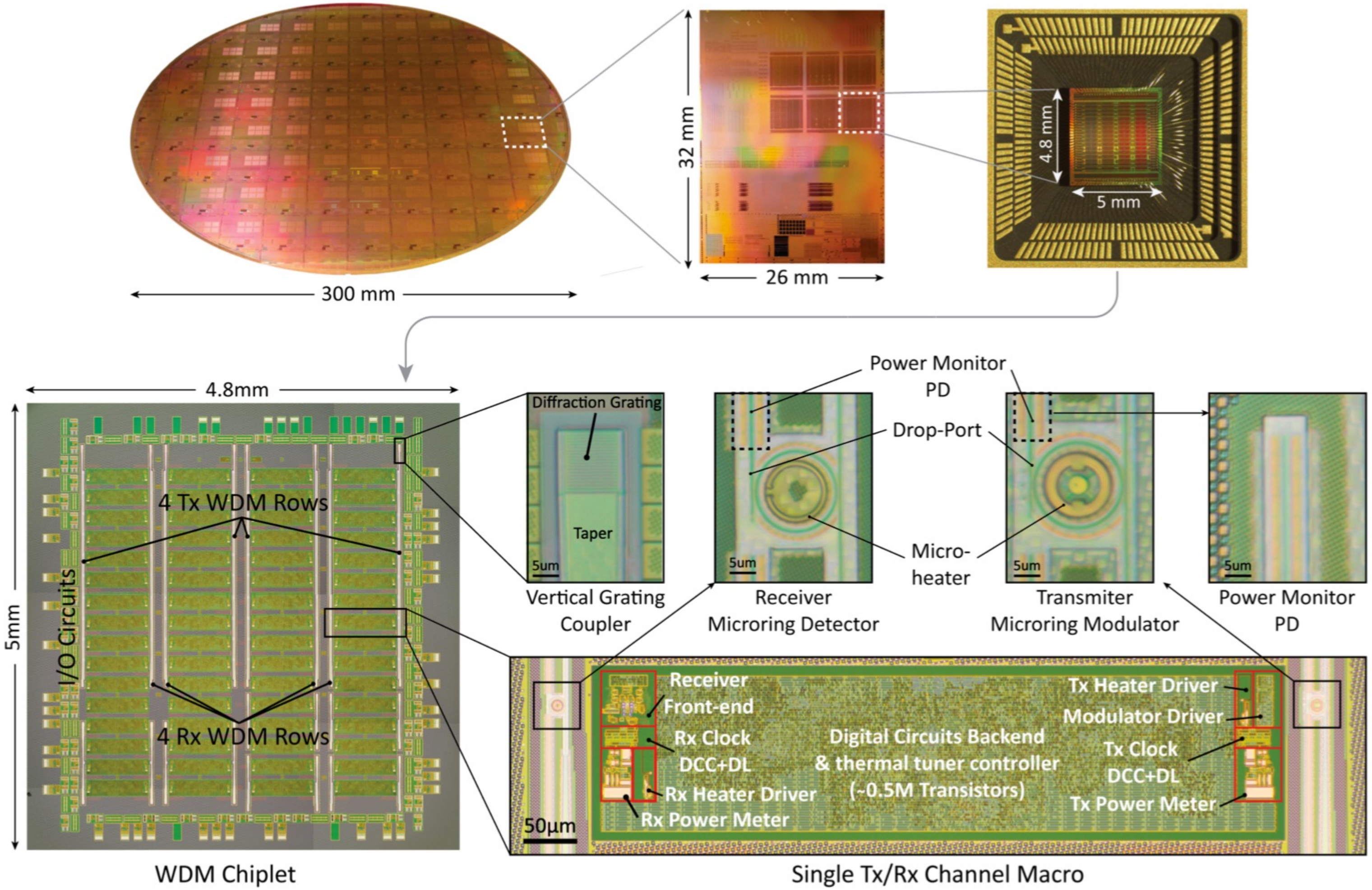


[Atabaki*, Moazeni* *et al.*, Nature 18] (*equally contributed)

ELECTRICAL & COMPUTER ENGINEERING

1st Run with Electronic & Photonics

More than 32M transistors + 200 photonic devices



[Atabaki*, Moazeni* *et al.*, Nature 18] (*equally contributed)